Thermal and Electrical Properties of Coated Conductive Substrates for Integrated Circuit Chip Mounting

By H. G. MATTES

(Manuscript received February 10, 1970)

Presently used substrates for integrated circuit chip mounting and interconnection provide limited heat sink capability and preclude the effective use of matched impedance transmission line interconnection. These characteristics can be improved by the use of very narrow microstrip lines on thin dielectric layers backed by thermally and electrically conductive material. We propose a model for calculating the effective thermal resistance of layered substrates and make calculations for a variety of materials. The thermal problem is considered for heat extraction either through the edge or through the face of the substrate. Improvements in substrate thermal conductance of an order of magnitude appear realizable compared to presently used substrates (for example, 0.625 mm alumina). We analyze the electrical parameters of narrow (0.02–0.1 mm) microstrip lines on coated substrates in the frequency range 10 MHz to 10 GHz. The characteristic impedance, propagation delay time, and attenuation are found to be frequency dependent, and efforts to minimize this frequency dependence by magnetic loading result in greater, though more constant, delay times. Losses may be significant (~2-5 dB/cm in many cases), but short line lengths due to dense circuit packing allowed by improved heat dissipating capability will minimize this disadvantage.

I. INTRODUCTION

A necessary component in realizing the potential of integrated circuit technology is the substrate upon which the integrated circuit chip is mounted. The substrate must meet several requirements to avoid deterioration of the system's performance:

(*i*) The substrate must act as a rigid, reliable mounting platform for the chip.

(*ii*) The substrate must allow the dissipation of heat produced on the chip without causing an increase in temperature which would detrimentally effect circuit operation.

(*iii*) The substrate must permit electrical connections to and interconnections between chips in a manner compatible with desired circuit performance.

(*iv*) The substrate fabrication and chip mounting must be realizable at a cost consistent with the cost requirements of the system.

Presently used substrates (for example, 0.625 mm thick Al_2O_3 ceramic wafers) are limited in their attainment of objectives *ii* and *iii* outlined above. Heat sink capability is limited by the low thermal conductivity and relatively large thickness of material necessary for mechanical rigidity and by the difficulty in extracting heat from the substrate itself. High frequency (>500 MHz) performance of beam-leaded integrated circuits suffers from the transmission line mismatch necessary with conventional substrates as is discussed below.

A new materials configuration, as shown in Fig. 1, is envisioned which would simultaneously satisfy the four basic substrate requirements listed above. A thin dielectric layer (0.001 mm to 0.05 mm thick) deposited or grown on a massive electrically and thermally conductive ground plane could allow efficient heat dissipation, effective electrical interconnection and provide a rigid, inexpensive bonding plane. It is the purpose of this paper to calculate the thermal and electrical properties of the coated substrate configuration suggested here.

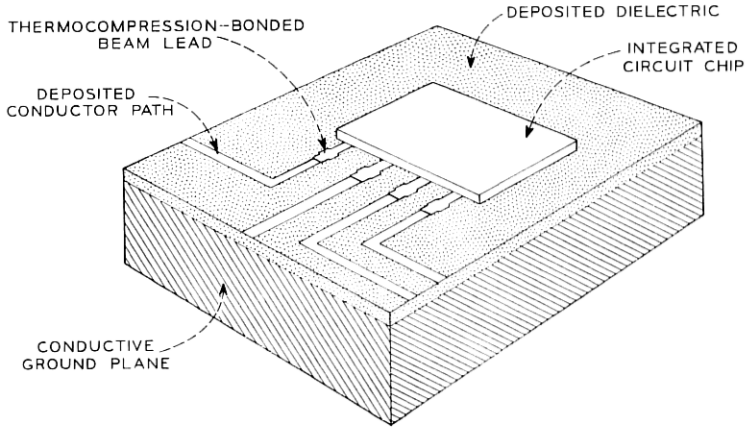

Fig. 1—Schematic drawing of layered substrate.

II. THERMAL PROPERTIES

The model used to represent the proposed substrate for calculation of thermal properties is shown in Fig. 2. All constants may be arbitrarily set, and the heat flow may be subjected to either of two distinct boundary conditions: the sides of the disk may be held fixed at a constant temperature and the top and bottom faces insulated, or the bottom face may be held at a constant temperature and the sides and top insulated. These cases closely approximate two heat sinking configurations frequently found in practice. The cylindrical geometry was chosen for ease of calculation (the square or rectangular problem, although algebraically simpler, results in a double series which presents formidable convergence problems when one is interested in a numerical result). The specific geometry should have little effect on the calculated values, and any reasonable geometry (held constant throughout the calculations)

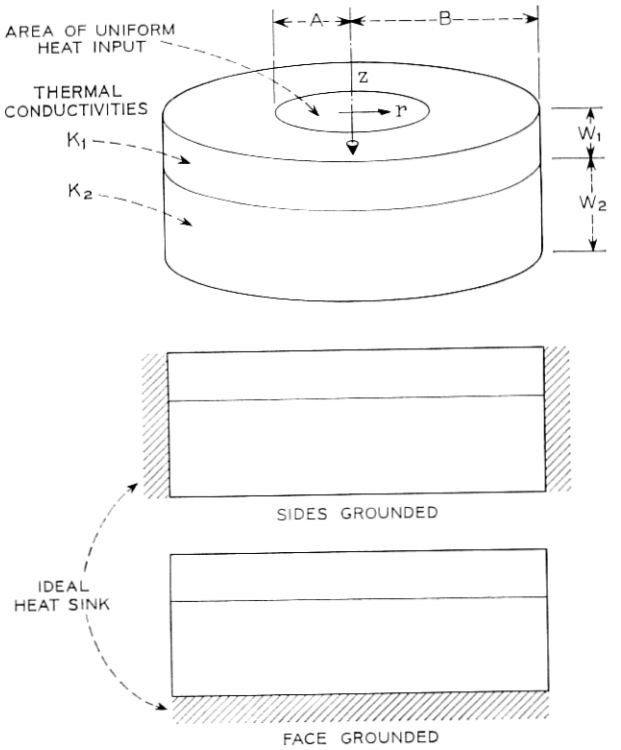

Fig. 2—Model used in calculations of thermal properties.

should provide a reliable comparison between alternate substrates. The heat input was assumed uniform over a circle of radius A, although other heat input distributions might have been chosen. As in the choice of geometry, this should have a minimal effect on the results. (Currently used beam leaded chips distribute heat over an area larger than the silicon dimensions. It can be assumed that the entire chip-beam lead structure thus forms a relatively uniform heat source on a substrate.[1])

2.1 *Algebraic Solution*

The thermal problem has already been solved for a homogeneous cylinder.[2] In the case of a layered cylinder, it is necessary to solve Laplace's equation simultaneously in both the upper and lower regions and match boundary conditions at the interface. In the calculations described in this paper, no discrete thermal resistance was inserted at the interface so the matching of boundary conditions reduced to

$$K_1 \frac{\partial T_1}{\partial z} = K_2 \frac{\partial T_2}{\partial z} \quad \text{at} \quad z = W_1 \tag{1}$$

where K_1, T_1, K_2, T_2 are the thermal conductivities and temperatures in regions 1 (upper) and 2 (lower). The insertion of a thermal resistance at the interface is trivial but was approximated as zero due to the intimate interface contact obtained by the method of materials preparation envisioned for these substrates.

Laplace's equation was solved for the two sets of boundary conditions (sides grounded and face grounded) by the method of separation of variables. In cylindrical coordinates, $\nabla^2 T = 0$ reduces to

$$T = \Psi_0 + \Psi_1 z + \sum_m \sum_n \Psi_{m,n}[A_m J_m(\delta_n r) + B_m N_m(\delta_n r)] \begin{Bmatrix} \sin \\ \cos \end{Bmatrix} m\theta \, [\exp(\pm \delta_n z)] \tag{2}$$

where boundary conditions exist to impose eigenfunction solutions in the r direction, and J_m and N_m are Bessel functions of the first and second kind respectively. The boundary condition on the grounded surfaces was given as $T = 0$ while $\partial T/\partial$ (normal) was set equal to zero on the insulated surfaces. On the top surface ($z = 0$) the boundary condition was written:

$$\frac{\partial T_1}{\partial z} = \begin{cases} \dfrac{-f}{k_1} & 0 < r < A, \quad z = 0; \\ 0 & A < r < B, \quad z = 0. \end{cases} \tag{3}$$

f is the value of heat input in (watts/unit area). This boundary condition was met by using the orthogonality properties of the Bessel functions in a Fourier-Bessel series as outlined in Morse and Feshbach and other texts.[3]

For the case in which the sides are grounded at $T = 0$, the temperature distribution is found to be

$$T = \sum_n \frac{2fA}{\beta_n^2 K_1} \frac{J_1\left(\beta_n \frac{A}{B}\right) J_0\left(\beta_n \frac{r}{B}\right)}{J_1^2(\beta_n)} \left[c_1 \cosh\left(\frac{\beta_n z}{B}\right) + c_2 \sinh\left(\frac{\beta_n z}{B}\right)\right] \quad (4)$$

where β_n is the nth zero of $J_0(r)$ and

$$c_1 = \begin{cases} \dfrac{\frac{K_2}{K_1}\tanh^2\left(\frac{\beta_n W_1}{B}\right) - \left(\frac{K_2}{K_1} - 1\right)\tanh\left(\frac{\beta_n W_1}{B}\right)\tanh\left(\frac{\beta_n (W_1 + W_2)}{B}\right) - 1}{\tanh\left(\frac{\beta_n W_1}{B}\right)\left[1 - \frac{K_2}{K_1} - \tanh\left(\frac{\beta_n W_1}{B}\right)\tanh\left(\frac{\beta_n (W_1 + W_2)}{B}\right)\right] + \frac{K_2}{K_1}\tanh\left(\frac{\beta_n (W_1 + W_2)}{B}\right)}, \\ \qquad \text{for} \quad 0 < z < W_1 ; \\ \dfrac{\tanh^2\left(\frac{\beta_n W_1}{B}\right) - 1}{\tanh\left(\frac{\beta_n W_1}{B}\right)\left[1 - \frac{K_2}{K_1} - \tanh\left(\frac{\beta_n W_1}{B}\right)\tanh\left(\frac{\beta_n (W_1 + W_2)}{B}\right)\right] + \frac{K_2}{K_1}\tanh\left(\frac{\beta_n (W_1 + W_2)}{B}\right)}, \\ \qquad \text{for} \quad W_1 < z < W_1 + W_2 ; \end{cases} \quad (5)$$

$$c_2 = \begin{cases} 1, \quad \text{for} \quad 0 < z < W_1; \\ \dfrac{\tanh\left(\frac{\beta_n (W_1 + W_2)}{B}\right)\left[1 - \tanh^2\left(\frac{\beta_n W_1}{B}\right)\right]}{\tanh\left(\frac{\beta_n W_1}{B}\right)\left[1 - \frac{K_2}{K_1} - \tanh\left(\frac{\beta_n W_1}{B}\right)\tanh\left(\frac{\beta_n (W_1 + W_2)}{B}\right)\right] + \frac{K_2}{K_1}\tanh\left(\frac{\beta_n (W_1 + W_2)}{B}\right)}, \\ \qquad \text{for} \quad W_1 < z < W_1 + W_2 . \end{cases} \quad (6)$$

For the case in which the bottom face is grounded at $T = 0$, the temperature distribution is found to be

$$T = \frac{A^2}{B^2} f(d_1 + d_2 Z) + \sum_n \frac{2fA}{\alpha_n^2 K_1} \frac{J_1\left(\alpha_n \frac{A}{B}\right) J_0\left(\alpha_n \frac{r}{B}\right)}{J_0^2(\alpha_n)} \left[d_3 \cosh\left(\frac{\alpha_n z}{B}\right) + d_4 \sinh\left(\frac{\alpha_n z}{B}\right)\right] \quad (7)$$

where α_n is the nth zero of $J_1(r)$ and

$$d_1 = \begin{cases} -\dfrac{W_1}{K_1} - \dfrac{W_2}{K_2} & 0 < z < W_1 \\ -\dfrac{W_1 + W_2}{K_2} & W_1 < z < W_1 + W_2 \end{cases} ; \quad (8)$$

$$d_2 = \begin{cases} \dfrac{1}{K_1} & 0 < z < W_1 \\ \dfrac{1}{K_2} & W_1 < z < W_1 + W_2 \end{cases}; \tag{9}$$

$$d_3 = \begin{cases} \dfrac{\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right) - \tanh\left(\frac{\alpha_n W_1}{B}\right)\left\{\frac{K_2}{K_1}\left[\tanh\left(\frac{\alpha_n W_1}{B}\right)\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right) - 1\right] + 1\right\}}{\tanh^2\left(\frac{\alpha_n W_1}{B}\right) + \left(\frac{K_2}{K_1} - 1\right)\tanh\left(\frac{\alpha_n W_1}{B}\right)\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right) - \frac{K_2}{K_1}}, \\ \qquad\qquad \text{for } 0 < z < W_1; \\ \dfrac{\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right)\left[1 - \tanh^2\left(\frac{\alpha_n W_1}{B}\right)\right]}{\tanh^2\left(\frac{\alpha_n W_1}{B}\right) + \left(\frac{K_2}{K_1} - 1\right)\tanh\left(\frac{\alpha_n W_1}{B}\right)\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right) - \frac{K_2}{K_1}}, \\ \qquad\qquad \text{for } W_1 < z < W_1 + W_2; \end{cases} \tag{10}$$

$$d_4 = \begin{cases} 1 \quad \text{for } 0 < z < W_1 \\ \dfrac{\tanh^2\left(\frac{\alpha_n W_1}{B}\right) - 1}{\tanh^2\left(\frac{\alpha_n W_1}{B}\right) + \left(\frac{K_2}{K_1} - 1\right)\tanh\left(\frac{\alpha_n W_1}{B}\right)\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right) - \frac{K_2}{K_1}}, \\ \qquad\qquad \text{for } W_1 < z < W_1 + W_2. \end{cases} \tag{11}$$

A quantitative measure of the power dissipating capabilities of a substrate is given by the thermal resistance

$$R_{\text{therm}}\left(\frac{\text{degrees C}}{\text{watt}}\right) = \frac{\Delta T(^\circ\text{C})}{q\ (\text{watts input})} = \frac{T_{\max}}{\pi A^2 f} \tag{12}$$

$T_{\max}$ clearly occurs at $z = 0$, $r = 0$ so

$$R_{\text{therm}}\ (\text{side grounded}) = \frac{2}{\pi K_1 A}\sum_n \frac{1}{\beta_n^2}\frac{J_1\left(\beta_n \frac{A}{B}\right)}{J_1^2(\beta_n)} \cdot \frac{\frac{K_2}{K_1}\tanh^2\left(\frac{\beta_n W_1}{B}\right) - \left(\frac{K_2}{K_1} - 1\right)\tanh\left(\frac{\beta_n W_1}{B}\right)\tanh\left(\frac{\beta_n(W_1+W_2)}{B}\right) - 1}{\tanh\left(\frac{\beta_n W_1}{B}\right)\left[1 - \frac{K_2}{K_1} - \tanh\left(\frac{\beta_n W_1}{B}\right)\tanh\left(\frac{\beta_n(W_1+W_2)}{B}\right)\right] + \frac{K_2}{K_1}\tanh\left(\frac{\beta_n(W_1+W_2)}{B}\right)} \tag{13}$$

and

$$R_{\text{therm}}\ (\text{face grounded}) = \frac{W_1 K_2 + W_2 K_1}{\pi B^2 K_1 K_2} + \frac{2}{\pi K_1 A}\sum_n \frac{1}{\alpha_n^2}\frac{J_1\left(\alpha_n \frac{A}{B}\right)}{J_0^2(\alpha_n)} \cdot \frac{\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right) - \tanh\left(\frac{\alpha_n W_1}{B}\right)\left\{\frac{K_2}{K_1}\left[\tanh\left(\frac{\alpha_n W_1}{B}\right)\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right) - 1\right] + 1\right\}}{\tanh^2\left(\frac{\alpha_n W_1}{B}\right) + \left(\frac{K_2}{K_1} - 1\right)\tanh\left(\frac{\alpha_n W_1}{B}\right)\tanh\left(\frac{\alpha_n(W_1+W_2)}{B}\right) - \frac{K_2}{K_1}}. \tag{14}$$

2.2 *Computer Program*

A FORTRAN IV computer program was written for an IBM 360-50 to evaluate $R_{\text{therm-side}}$ and $R_{\text{therm-face}}$. The first forty values of alpha and beta (the zeros of J_1 and J_0) are inserted in the program from the tabulated values of Watson.[4] The values of the higher zeros are obtained in the program by analysis of the asymptotic approximations for J_1 and J_0.

Since the expressions for R_{therm} take the form of infinite series, no completely precise evaluation can be made. Figure 3 shows the approximation to $R_{\text{therm-face}}$ given by truncating the summation after varying numbers of terms. Plotting data similar to Figure 3 for a range of all input parameters (A, B, K_1, K_2, W_1, W_2) disclosed several trends in the convergence of the series. The "period" of the oscillation was inversely correlated to the ratio A/B. This is mathematically consistent with the use of a Fourier-Bessel series to describe the top face of the disk. For ratios of A/B less than 0.02, the first maxima in the expression for $R_{\text{therm-side}}$ is not reached until partial sums with greater than 300 terms are evaluated. The amplitude of the oscillations in the function R_{therm} (number of terms) was positively correlated to K_2/K_1 and W_1/W_2. The damping of the oscillation (per cycle) appeared to be relatively

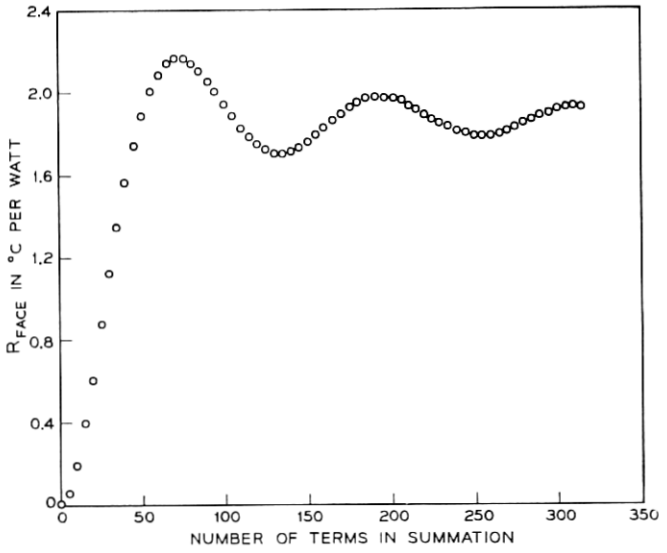

Fig. 3—Partial sums approximating R_{face} for $A = 0.0625$, $B = 3.75$, $K_1 = 0.20$, $K_2 = 2.05$, $W_1 = 0.0005$, $W_2 = 0.0625$.

independent of input data. These variabilities in the behavior of R_{therm} made determination of a precise value difficult. Additionally, only the first 314 terms of the series could be evaluated. The operation of the program was terminated at this point by a floating point overflow which occurred in the IBM-SSP subroutine used to generate the Bessel functions. Since the largest arguments of the Bessel functions are intrinsic to the problem, and are not functions of the input parameters, nothing could be done to circumvent this difficulty. It thus became necessary to evaluate R_{therm} on the basis of a truncated series of 314 terms of less.

A graphical outline of the method used to extract an approximation to the asymptotic value of R_{therm} from a finite number of terms in shown in Fig. 4. The first two local maxima, M_1 and M_3, and the first local minimum, M_2, were recorded; and the averages, A_1 and A_2, were calculated where

$$A_1 = \frac{M_1 + M_2}{2}; \tag{15}$$

$$A_2 = \frac{M_2 + M_3}{2}. \tag{16}$$

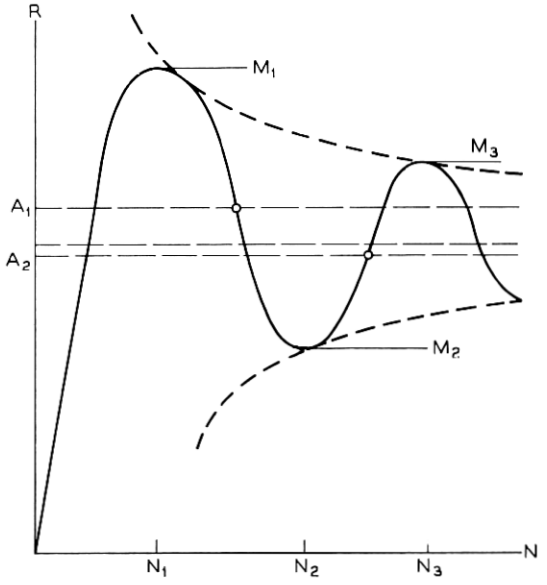

Fig. 4—Pictorial of extremum averaging technique used for improving series convergence.

In Appendix A, a theorem is stated and proved to show that the asymptotic value of R_{therm} is less than A_1 and greater than A_2. An average of the two, $(A_1 + A_2)/2$, was used as a most probable value of R_{therm}.

As a test of the accuracy of the derivation of $R_{therms-side}$ and $R_{therm-face}$ and the computer programs for generating these values, K_2 was set equal to K_1 (equivalent to a uniform, single layer cylinder) and values of R_{therm} computed for $W_1 = 0.625$ mm, $W_2 = 0$; $W_1 = 0.375$ mm, $W_2 = 0.25$ mm; and $W_1 = 0$, $W_2 = 0.625$ mm. The three cases were in complete mutual agreement, and agreed to the accuracy given with the published results of D. P. Kennedy for heat conduction in a homogeneous, isotropic cylinder.[2]

2.3 *Numerical Evaluation*

Several materials combinations were chosen for evaluation as possible substrates. Some of the considerations for inclusion were compatibility with integrated circuit techniques (for example, silicon), smooth surfaces for microdeposition of conductor paths (for example, polished silicon, cold-rolled aluminum), low dielectric constant (for example, SiON), and thermal expansion coefficient. The materials considered and the associated values of K used with them are shown in Table I. $A = 0.625$ mm and $B = 3.75$ cm were chosen as representative of typical integrated circuit chips and substrate sizes and were used in most of the calculations.

The results of these calculations for a variety of layered substrates are shown in Figs. 5 through 10. With high conductivity dielectrics (for example, Al_2O_3) the thermal resistivity of the ground plane contributes significantly to the total thermal resistance, but resistances as low as that of beryllia are attainable for a considerable range of dielectric thicknesses. Low conductivity, glassy (for example, SiON, SiO_2) dielectrics, can result in thermal resistances equal to or greater than that of alumina if glassy layers of greater than 0.03 mm thick are used.

TABLE I—THERMAL CONDUCTIVITY OF SUBSTRATE MATERIALS

Material	K (watts/cm °C)
Al	2.05
Al_2O_3 (deposited)	0.20
Al_2O_3 (sintered)	0.29
BeO	1.95
Si	0.88
Si_3N_4	0.012
SiO_2	0.012
SiON	0.012

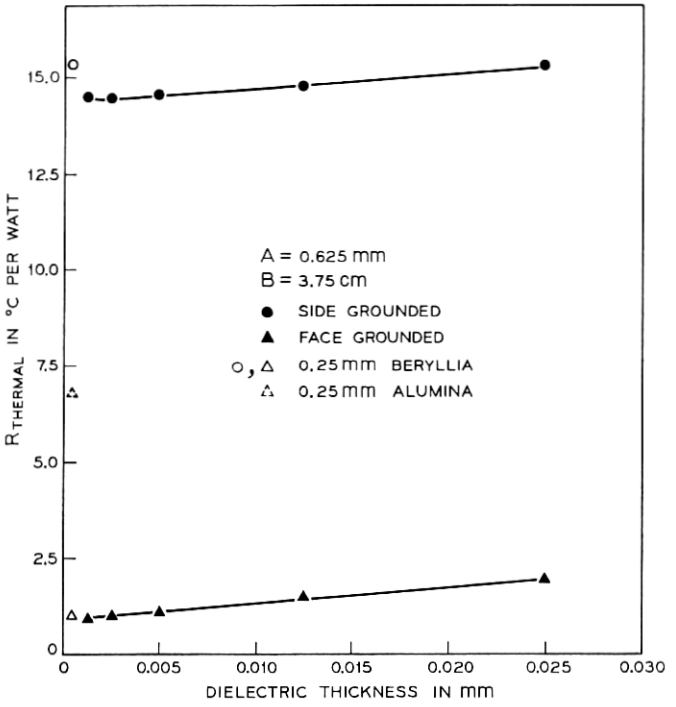

Fig. 5—Aluminum oxide on 0.25 mm aluminum.

For comparison, thermal resistances of presently available homogeneous substrates were calculated and are given in Table II.

Figure 11 shows the effect of substrate radius on $R_{\text{therm-side}}$ (the effect on $R_{\text{therm-face}}$ was $<2\%$ for $B \geqq 0.5$ cm). In the range shown, heat is presumably flowing radially at $r = B$ so increases in B add to R_{therm} at a rate proportional to $1/B$. Consequently, a "critical radius" exists above which $R_{\text{therm-side}}$ is relatively constant.

Radiative and convective heat losses will be negligible for the high conductivity layered substrates discussed in this paper. A lumped value of convective and radiation coefficient of 0.003 watts/cm.^{2} — °C results in an equivalent parallel thermal resistance of greater than 50°C/watt for all cases considered here.

2.4 *Thermal Results*

Layered substrates consisting of dielectric layers backed by thermally conducting ground planes can provide substantial improvements in heat

sink capability over alumina ceramic substrates. Ceramic substrates are commonly used in 0.625 mm thickness to provide needed strengths. Metal ground planes could be reduced to 0.25 mm thickness while maintaining physical strength greater than 0.625 mm ceramic. For situations where heat sinking the back of the substrate is possible, Al_2O_3 on 0.25 mm aluminum can provide up to twice the heat sink capability of 0.625 mm beryllia. Metal substrates have the additional advantage of convenient, low thermal barrier heat sink mounting or even direct incorporation into the heat sink structure (for example, heat pipes, finned substrates).

Although the above values of R_{therm} are significant, as given, for relative comparison of substrate materials and geometries, their absolute significance can only be assessed in relation to other parameters intrinsic to an integrated circuit heat dissipating system. V. E. Holt

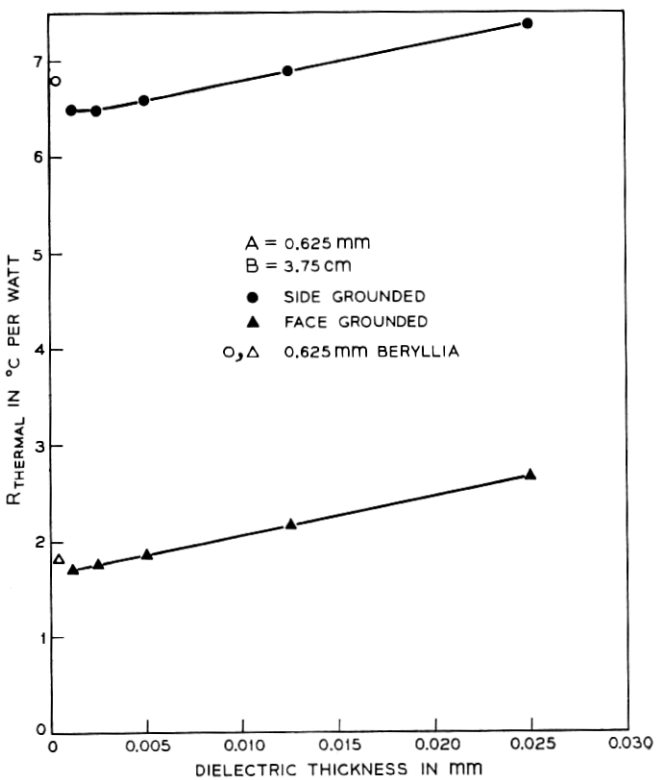

Fig. 6—Aluminum oxide on 0.625 mm aluminum.

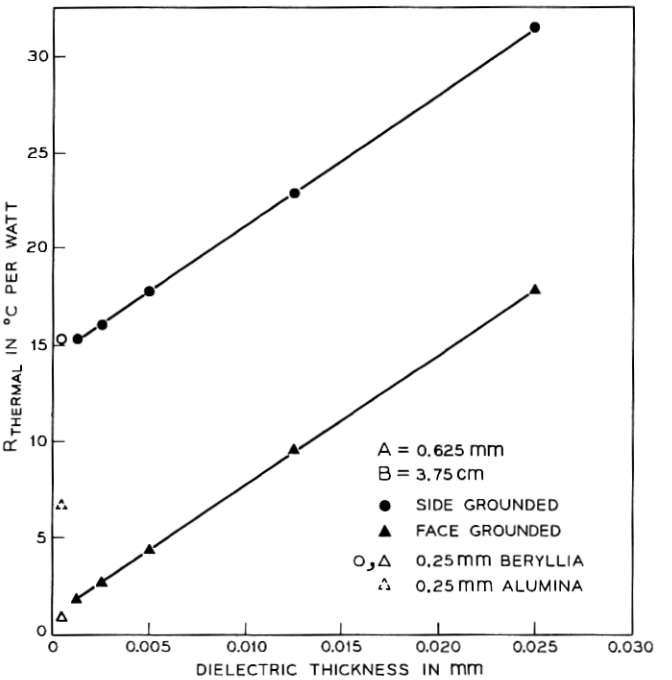

Fig. 7—Silicon oxynitride on 0.25 mm aluminum.

has found thermal barriers of 32°C/watt for 1.25 mm chips conducting heat to a substrate by means of beam leads and a resin bonding layer.[1] This value is reduced to 3 to 5°C/watt by AuSi eutectic bonding. Imperfections in the heat sink will have to be assessed in each situation encountered.

III. ELECTRICAL PROPERTIES

3.1 *Microstrip Transmission Lines*

Electrical interconnections on the proposed substrates would best be made in the form of standard microstrip transmission lines.[5] They can provide transmission line interconnects necessary for high speed pulse and microwave electronics while maintaining low values of crosstalk between adjacent lines and still provide dc and low frequency paths for other circuit requirements. The primary incompatibility of presently used substrates and beam-leaded integrated circuit chips is due to the impedance mismatch between the narrow (0.02 to 0.05 mm) beam leads

and the physically large transmission line (typically 50Ω implies 0.625 mm line width on 0.625 mm alumina).[5] The removal of this discontinuity would require narrow conductors deposited on a dielectric layer of appropriate thickness to maintain the desired transmission line impedance. The physical configuration contemplated for small microstrip lines is outlined in Fig. 12. To minimize the impedance discontinuity at the interconnection with beam leaded chips, W is restricted to 0.1 mm maximum. To minimize crosstalk, this would suggest $t_d \leqq 0.05$ mm[6]. These figures, coupled with the electrical parameters of dielectric materials sufficiently smooth to allow the reliable deposition of 0.02 mm conducting paths, are consistent with the desire to develop lines with a characteristic impedance of 50Ω, the most commonly used interface impedance for circuitry operating above 500 MHz. Under certain conditions, as seen below, it is desirable to raise the series inductance of the transmission line. For this reason, provision has been made for placing a thin layer of high permeability material between the conducting strip and the dielectric. In practice the adhesion metal of a sandwiched interconnect (dielectric—adhesion metal—gold) might serve this purpose.

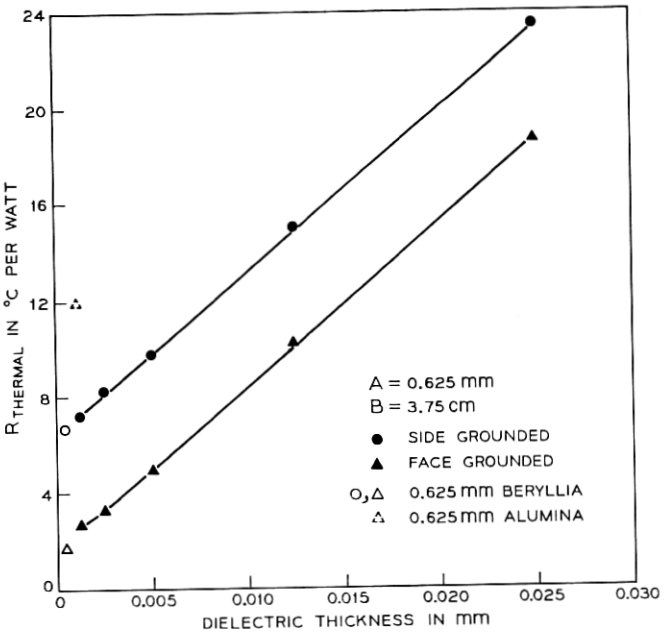

Fig. 8—Silicon oxynitride on 0.625 mm aluminum.

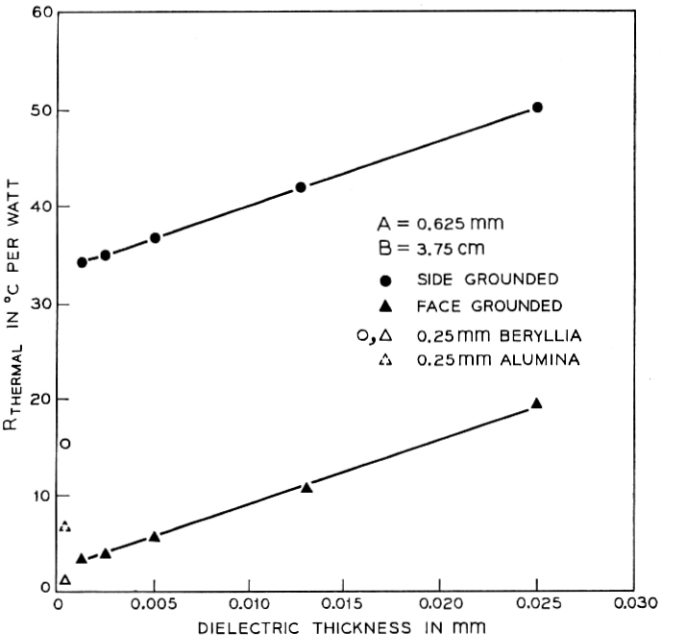

Fig. 9—Silicon dioxide on 0.25 mm silicon.

3.2 *Transmission Line Parameters*

Although many transmission modes are necessarily present in an unsymmetrical transmission line such as an unshielded microstrip, the TEM mode will be considered of dominant interest in the frequency range considered here and the line parameters will be calculated for this mode. Several authors (for example, Assadourian and Rimai,[7] and H. A. Wheeler[8]) have derived expressions for the characteristic impedance and other pertinent parameters for microstrip transmission lines. Although these formulae have been generally verified in their range of approximation[5,9,10] the physical scale of lines contemplated in the last section requires the inclusion of several terms which had been ignored in the previous derivations.

The characteristic impedance, Z_0, and propagation constant, γ, of any power transmission system are given by[11]

$$Z_0 = \left(\frac{R + j\omega L}{G + j\omega C}\right)^{\frac{1}{2}}, \tag{17}$$

$$\gamma = [(R + j\omega L)(G + j\omega C)]^{\frac{1}{2}}. \tag{18}$$

Ignoring losses (R, $G \rightarrow 0$), the propagation delay time can then be written

$$\tau = \frac{-j\gamma}{\omega} = (LC)^{\frac{1}{2}}. \tag{19}$$

The inductance of the line is given by two components: the inductance due to magnetic field energy storage in the strip conductor and the ground plane (the internal inductance); and the inductance due to magnetic field energy storage between the strip conductor and the ground plane (the external inductance). The internal inductance of the strip conductor can be derived from Ramo and Whinnery[12] and is given by

$$L_s = \frac{1}{W\omega}\left[\frac{\rho_s}{\delta_s}\frac{\sinh\left(\frac{2t_s}{\delta_s}\right) - \sin\left(\frac{2t_s}{\delta_s}\right)}{\cosh\left(\frac{2t_s}{\delta_s}\right) - \cos\left(\frac{2t_s}{\delta_s}\right)}\right] \tag{20}$$

where ρ_s is the resistivity of the strip conductor material and δ_s is the

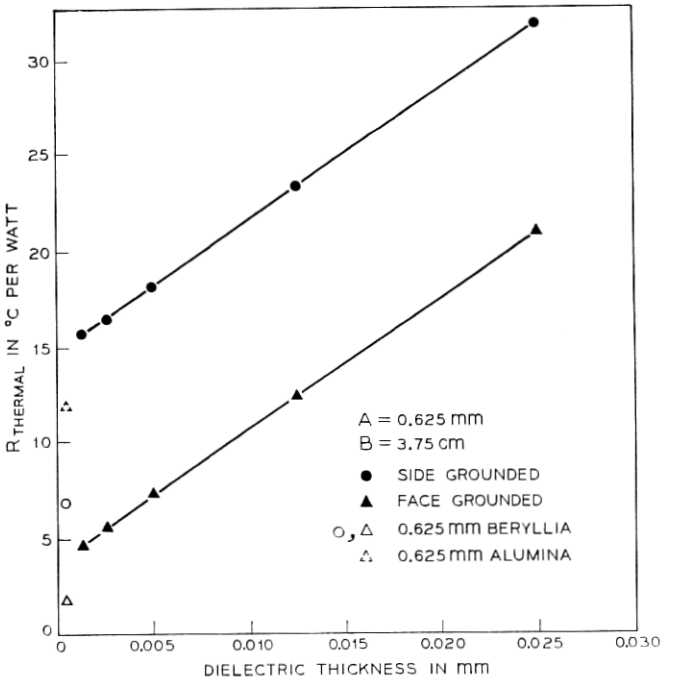

Fig. 10—Silicon dioxide on 0.625 mm silicon.

TABLE II—THERMAL RESISTANCE OF CONVENTIONAL SUBSTRATES

	$R_{\text{therm-side}}$ (degrees C/watt)	$R_{\text{therm-face}}$ (degrees C/watt)
Alumina		
0.25 mm	103	6.8
0.625 mm	46	12
Beryllia		
0.25 mm	15.3	1.02
0.625 mm	6.8	1.8

skin depth of the strip conductor at the frequency, ω, of interest. [$\delta = (2\rho/\omega\mu)^{\frac{1}{2}}$]. For the frequency range considered in this paper ($f > 10$ MHz) current spreading in the ground plane can be ignored for lines as narrow as 0.02 mm if the ground material has a resistivity $\leqq 10^{-5}$ ohm-cm. For higher resistivity materials this approximation is less valid, especially at the lower frequencies, but the approximation will be made for convenience. A more rigorous analysis in the higher resistivity case would give increased internal inductance and increased

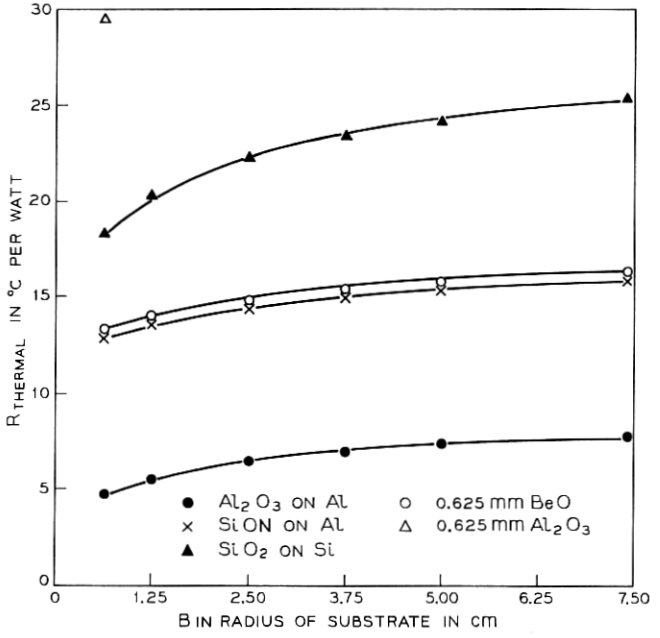

Fig. 11—Thermal resistance with side grounded $A = 0.625$ mm $W_1 = 0.0125$ mm, $W_2 = 0.625$ mm.

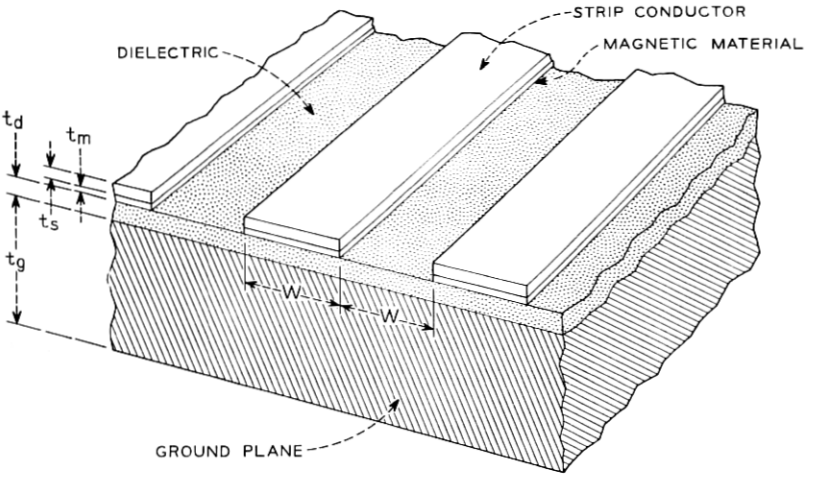

Fig. 12—Schematic drawing of microstrip transmission lines on layered substrate.

crosstalk through magnetic fields generated by spreading currents in the ground plane. The internal inductance per unit length of line due to fields in the ground plane can then be given by a formula similar to (20)

$$L_g = \frac{1}{W\omega}\left[\frac{\rho_g}{\delta_g}\frac{\sinh\left(\frac{2t_g}{\delta_g}\right) - \sin\left(\frac{2t_g}{\delta_g}\right)}{\cosh\left(\frac{2t_g}{\delta_g}\right) - \cos\left(\frac{2t_g}{\delta_g}\right)}\right] \tag{21}$$

where ρ_g and δ_g are the resistivity and skin depth of the ground plane. For the dimensional range of interest ($W > 2t_d$) the external inductance per unit length is approximately given by English and McNichol[13] as

$$L_{ext} = \frac{\mu_0}{W}(t_d + \mu_R t_m) \tag{22}$$

where μ_R is the relative permeability of the magnetic material. Total L is given by the sum

$$L = L_s + L_g + L_{ext}\,. \tag{23}$$

The total capacitance per unit length between the strip conductor and the ground plane is the sum of four components

$$C = C_T + C_g + C_f + C_e\,. \tag{24}$$

C_T is the capacitance per unit length between the top of the strip and the ground at infinity[14].

$$C_T = \frac{4\epsilon_0}{\pi} \ln 2. \tag{25}$$

C_g is the capacitance per unit length, neglecting fringing, between the face of the strip and the ground plane.

$$C_g = \epsilon_0 \epsilon_R \frac{W}{t_d} \tag{26}$$

where ϵ_R is the relative dielectric constant of the insulating layer. The additional capacitance per unit length due to the fringing fields at the edges of the strip is given by Joines[15]

$$C_f = \frac{4\epsilon_0\epsilon_R}{\pi} \ln \left[1 + \left(1 - \exp \frac{-\pi W}{2t_d}\right)^{\frac{1}{2}}\right]. \tag{27}$$

For the case where the strip conductor is not of negligible thickness, an additional contribution to the capacitance is due the capacitance between the edges of the strip and the ground plane. The expression for this term, derived in Appendix B, is

$$C_s = \frac{2\epsilon_0\epsilon_R}{\pi} \ln \left\{\frac{2t_d + 2t_s + [2(t_d + t_s)(t_d + 2t_s)]^{\frac{1}{2}}}{t_d}\right\}. \tag{28}$$

Losses on these microstrip lines will be considered as a perturbation in the calculation of the other parameters although this approximation is quite poor in several of the cases considered below. Losses in the dielectric will be ignored, being much less than the conductor losses for the geometries discussed in this paper. Under considerations similar to those for deriving the internal inductance, the equivalent series resistance is given by[11,12]

$$R = \frac{1}{W}\left[\frac{\rho_s}{\delta_s} \frac{\sinh\left(\frac{2t_s}{\delta_s}\right) + \sin\left(\frac{2t_s}{\delta_s}\right)}{\cosh\left(\frac{2t_s}{\delta_s}\right) - \cos\left(\frac{2t_s}{\delta_s}\right)} + \frac{\rho_g}{\delta_g} \frac{\sinh\left(\frac{2t_g}{\delta_g}\right) + \sin\left(\frac{2t_g}{\delta_g}\right)}{\cosh\left(\frac{2t_g}{\delta_g}\right) - \cos\left(\frac{2t_g}{\delta_g}\right)}\right]. \tag{29}$$

The attenuation per unit length of line is given by[11]

$$\alpha = \frac{R}{2Z_0} \text{ (nepers)}. \tag{30}$$

Although this expression is rigorously valid only for $|R/\omega| \ll |L|$, it will be used in all computations made in this paper. In the case where

$| R/\omega | \gtrsim | L |$, the line will have a significant reactive component in its characteristic impedance. Equation (30) for α will then contain a contribution for phase shift as well as attenuation. In this paper $| Z_0 |$, Re (Z_0), and Re (α) will be calculated.

The equations for crosstalk between adjacent, parallel strip lines derived by Kordos[6] apply directly to microstrip lines of the dimensions considered here if the characteristic impedance is calculated by the means outlined above. In these cases, Kordos derives an expression for the near end crosstalk of properly terminated parallel lines of length, l.

$$\frac{V_{ne}(s)}{V_g(s)} \simeq \frac{30 \ln [1 + (t_d/W)^2]^{\frac{1}{2}}}{\text{Re } (Z_0)(\epsilon_R)^{\frac{1}{2}}} [1 - \exp (-2s\tau l)]. \tag{31}$$

$V_{ne}(s)$ and $V_g(s)$ are the Laplace transforms of the near-end crosstalk voltage and the input signal respectively. The far-end crosstalk is approximately zero. This formula is only valid for $t_m = 0$. For $t_m > 0$, V_{ne} would be further reduced by the "keeper" effect of the magnetic material on the magnetic field of the driven line.

3.3 *Numerical Evaluation*

The formulas given above have been applied to layered substrates of the type discussed earlier. The calculations assumed that the strip conductors (Au $- 2.5 \times 10^{-6}\Omega-$cm.) should exhibit a resistance of $\lesssim 0.004\Omega$/sq. to give a dc resistance $< 1.5\Omega$/cm for the narrowest line considered, 0.02 mm. This results in $t_s = 0.00625$ mm. Silicon and aluminum were considered as possible ground plane materials. The maximum doping level in silicon which allows the preservation of a smooth surface after processing is approximately 2×10^{19} atoms/cm^3 which results in a bulk resistivity of approximately $2.5 \times 10^{-3}\Omega-$cm. The constant parameters used in the calculations are shown in Table III.

The expressions given in Section 3.2 were evaluated for a spectrum of frequencies between 10 MHz and 10 GHz for several physically realizable dielectric-ground plane materials combinations with varying

TABLE III—ELECTRICAL PARAMETERS FOR STRIPLINE CALCULATIONS

(All dimensions in cm)

ρ_s (Au) $= 2.5 \times 10^{-6}$	$t_g = 6.25 \times 10^{-2}$
ρ_g (Al) $= 2.5 \times 10^{-6}$	ϵ_R (sintered Al_2O_3) $= 9.6$
ρ_g (Si) $= 2.5 \times 10^{-3}$	ϵ_R (deposited Al_2O_3) $= 9.0$
$\mu_R = 100$	ϵ_R (SiON) $= 3.8$
$t_s = 6.25 \times 10^{-4}$	ϵ_R (SiO_2) $= 3.6$

thicknesses of magnetic material. A representative sampling of the results is shown in Figs. 13 through 20. These data are not meant to be comprehensive or complete but merely to represent the effects and trends observed in the calculations.

Figures 13 through 16 give Re (Z_0) and τ as a function of dielectric thickness and/or line width. The effect of the large internal inductance of Si on Z_0 and τ is especially apparent for thin dielectrics (where the external inductance is small). It is noted in Figs. 13 and 14 that τ passes through a local minimum at $t_d \sim 0.01$ mm mils. Below this value (for aluminum ground planes) the constant internal inductance is greater than the external inductance; and the capacitance, which decreases with t_d, causes τ to decrease with t_d. Above the minimum, as the increasing external inductance predominates, the fringing capacitance does not decrease linearly with t_d so τ rises. As t_d increases further, the equations used in this paper cease to be valid and the inductance will not increase linearly with t_d.

In Figs. 17 and 18, the solid lines show the frequency dependence of the characteristic impedance. The variation of Re (Z_0) with ω is particu-

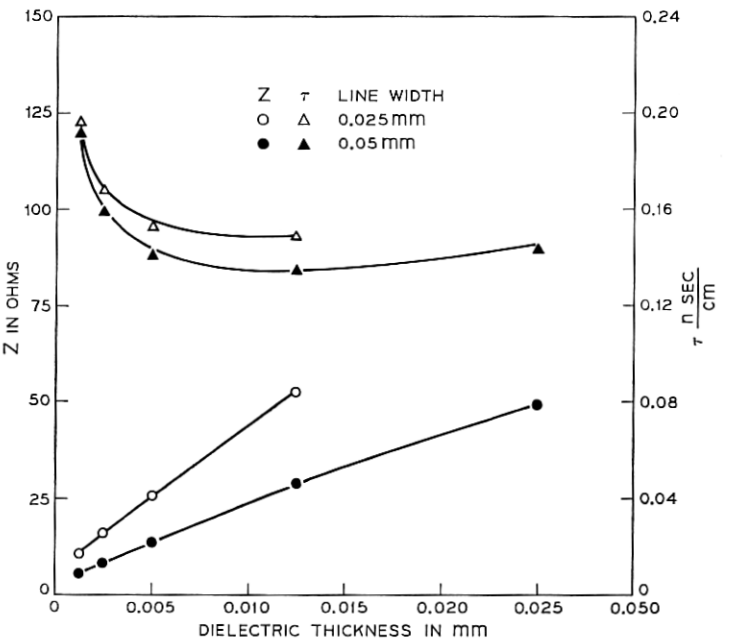

Fig. 13—Impedance and delay time at 1 GHz for aluminum oxide dielectric on aluminum ground plane.

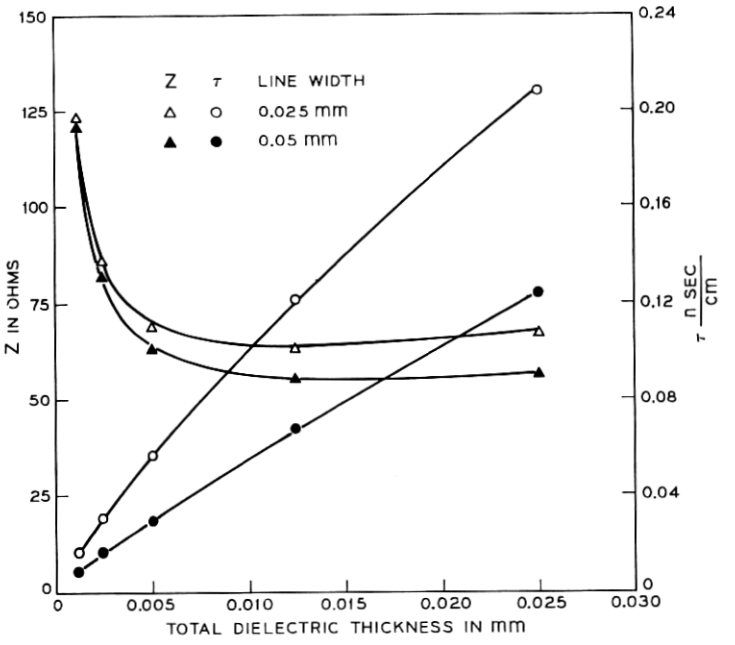

Fig. 14—Impedance and delay time at 1 GHz for silicon oxynitride dielectric on aluminum ground plane.

larly large in the case of Si since the frequency independent external inductance is small compared to the internal inductance. For pulse applications in which an impedance match is desirable over a broad frequency range, the situation may be improved somewhat by increasing the frequency independent component of the inductance. This may be done by loading the line with magnetic material, the results of which are shown by the dashed lines in Figs. 17 and 18. The open triangles show the unavoidably greater propagation delay times associated with the loaded lines. It can be seen from the deriving formulas that only the product $\mu_R t_m$ was considered significant, so materials of other permeabilities and appropriate thicknesses would be equally effective.

The losses associated with these lines have been calculated, and a sample of the results is shown in Fig. 19. Attenuation (dB/cm) is plotted for two materials configurations at each of two frequencies for a range of substrate thicknesses. The losses are particularly great for silicon ground planes (0.0025Ω-cm) and for small dielectric thicknesses (which result in low values of Z_0). The losses decrease rapidly as line width increases.

The near-end crosstalk for semi-infinite lines is shown in Fig. 20 as calculated without the influence of the magnetic material. For all geometries considered in this paper the near-end crosstalk is below 4 percent and is typically 1 percent or less. The presence of magnetic material would reduce this further.

For comparison, the transmission parameters of a 50Ω microstrip transmission line on a conventional 0.625 mm thick Alumina substrate are[5,15] given in Table IV.

3.4 *Electrical Results*

Effective transmission line interconnections for chip to chip on a layered integrated circuit substrate appear realizable. The major disadvantages are variation of impedance with frequency, appreciable delay times (and variation of delay time with frequency causing pulse distortion) and significant losses. These problems can be minimized by

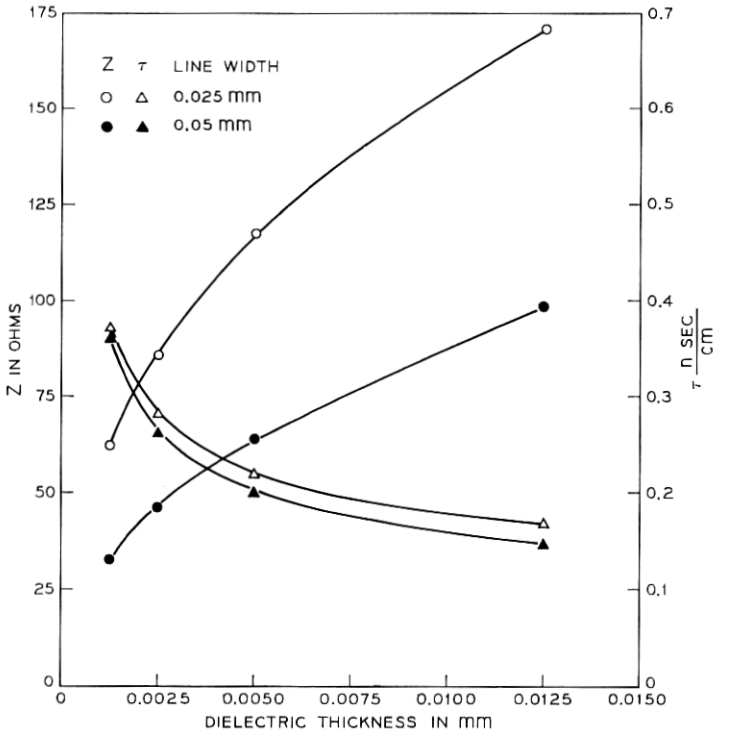

Fig. 15—Impedance and delay time at 1 GHz for silicon dioxide dielectric on silicon ground plane.

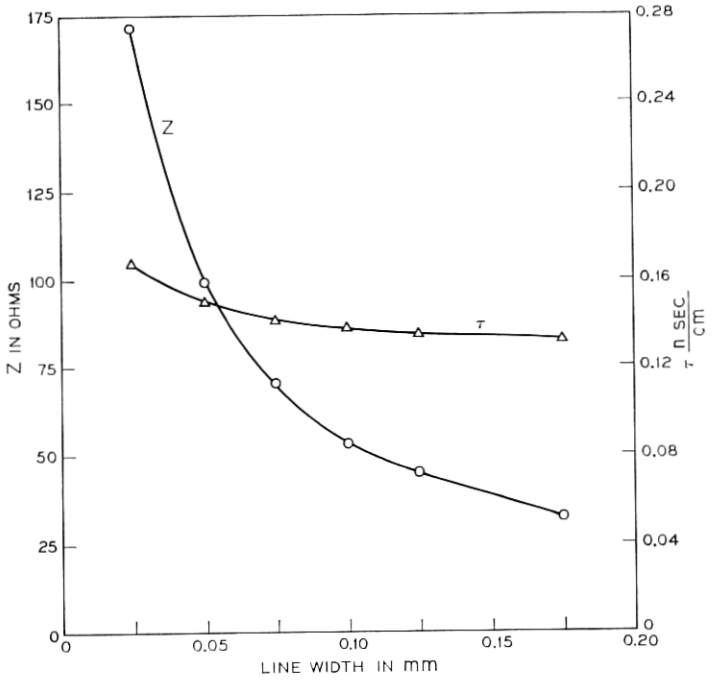

Fig. 16—Impedance and delay time at 1 GHz for 0.0125 mm thick silicon dioxide dielectric on silicon ground plane.

careful design (for example, judicious choices to t_m and μ_R). The problems of delay times and attenuation (characteristics directly proportional to the length of the line) will also be reduced by the much greater chip packing densities allowable with substrates of high thermal conductivity. Nonetheless, the high losses encountered with Si ground planes (along with its lower thermal conductivity) make this material a dubious substrate choice* except for possible special cases in which wide lines could be used for all portions of the circuitry where attenuation need be considered and where the ground returns for high current lines (for example, power supply lines) could be deposited as surface metallization.

* This configuration (0.0025 Ω-cm Si as a ground plane) should not be confused with the possible use of high resistivity Si (1500 Ω-cm) as a dielectric with gold surface metallization and a metal ground plane. T. M. Hyltin has measured the dielectric loss in microstrips with high resistivity Si dielectrics.[16] Such a dielectric, when used in the configuration discussed in this paper, would contribute an additional 0.5 dB/cm attenuation to the attenuation calculated above for aluminum ground planes.

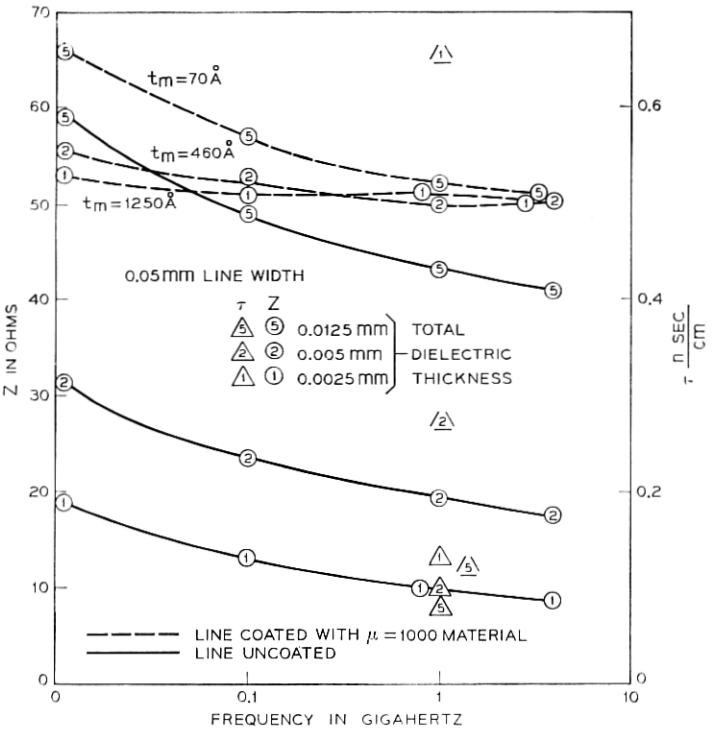

Fig. 17—Impedance and delay time for silicon oxynitride dielectric on aluminum ground plane.

In the case of aluminum ground planes, the losses on narrow (2 mil) lines are probably tolerable for present circuitry with the shortened lines due to higher packing. For longer lines, power leads, and so on, it may be necessary to use wider lines and connect to the beam leads of the integrated circuit chips through tapered section "transformers". The impedance transition need not be as great as the desired width change would indicate if t_m could be increased under the wide lines to compensate for the decreased L and increased C.

Many present applications for lower speed integrated circuit logic do not require matched transmission lines for all or any of the interconnections. The primary electrical requirement is then the completion of interconnects between integrated circuit chips with a minimum capacitance to ground. For such applications the narrow conductors envisioned in this paper would nearly compensate for the increased capacitance per unit length due to reduced t_d compared with conven-

tional 0.625 mm alumina substrates. Use of SiON dielectric ($\epsilon_R = 3.4$) would additionally improve this situation. Resistive signal loss in this application should be negligible since typical input impedances are 1–2K ohms. The possibility of shortened lead length due to higher packing densities on high thermal conductivity substrates then suggests the possibility of improved electrical performance.

IV. CONCLUSIONS

The advantages to be gained from a layered substrate are substantial from thermal considerations. The modifications of the electrical properties resulting from the layered geometry do not appear to present a significant obstacle to the development of such substrates. Indeed many improvements in electrical performance appear realizable with thin line metallization and transmission line interconnections. Layered

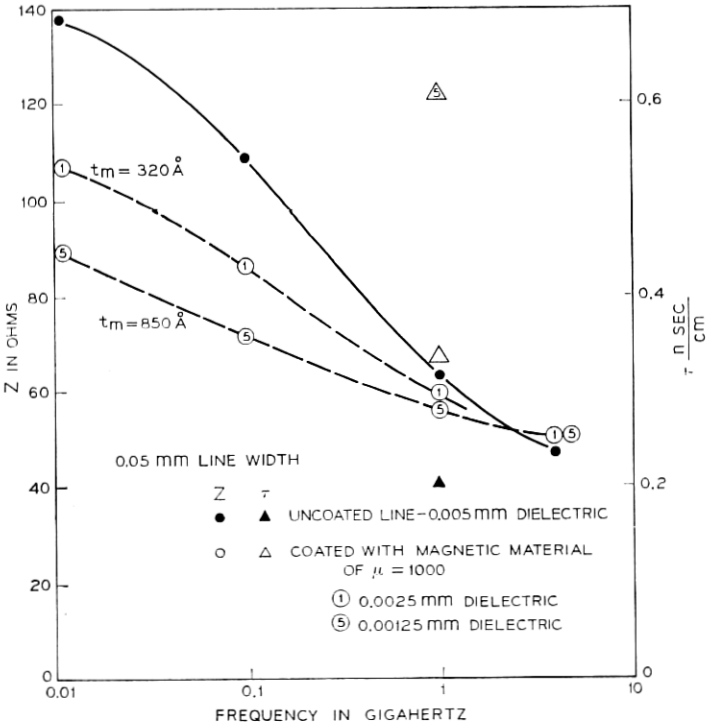

Fig. 18—Impedance and delay time for silicon dioxide dielectric on silicon ground plane.

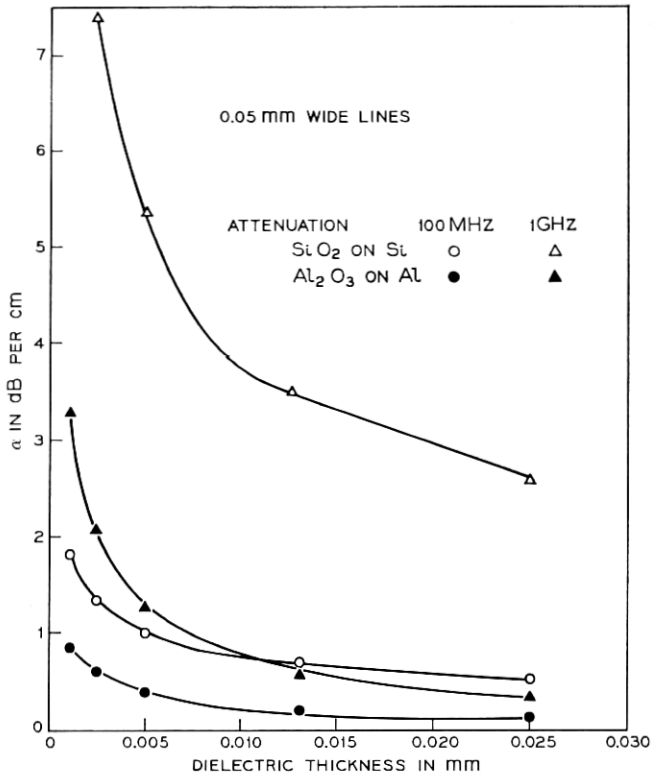

Fig. 19—Attenuation at 100 MHz and 1 GHz.

substrates with massive metal ground planes will adequately satisfy rigid mounting plane requirements, and the physical configuration of unbalanced microstrip lines allows the use of reliable, inexpensive thermocompression bonding of a beam-leaded integrated circuit chip to the substrate.

V. ACKNOWLEDGMENTS

The author would like to thank W. B. Grupen and T. P. Tignor for their comments on preliminary drafts of this paper, and A. W. Rose for his assistance in preparing the computer programs.

APPENDIX A

Averaging Technique for Improved Series Conversion

Theorem: Let $T(N)$ be a function of varying sign with zero crossings enumerated $z_0, z_1, \cdots, z_i, z_{i+1}, \cdots$ where i is chosen such that

$$\left.\frac{dT}{dN}\right|_{N=Z_i} > 0. \tag{32}$$

If

$$\left|\sum_{N=Z_i}^{Z_{i+1}} T(N)\right| > \left|\sum_{N=Z_{i+1}}^{Z_{i+2}} T(N)\right| > \left|\sum_{N=Z_{i+2}}^{Z_{i+3}} T(N)\right|. \tag{33}$$

Then

$$\frac{\sum_{N=0}^{Z_i} T(N) + \sum_{N=0}^{Z_{i+1}} T(N)}{2} < \sum_{N=0}^{\infty} T(N) < \frac{\sum_{N=0}^{Z_{i+1}} T(N) + \sum_{N=0}^{Z_{i+2}} T(N)}{2}. \tag{34}$$

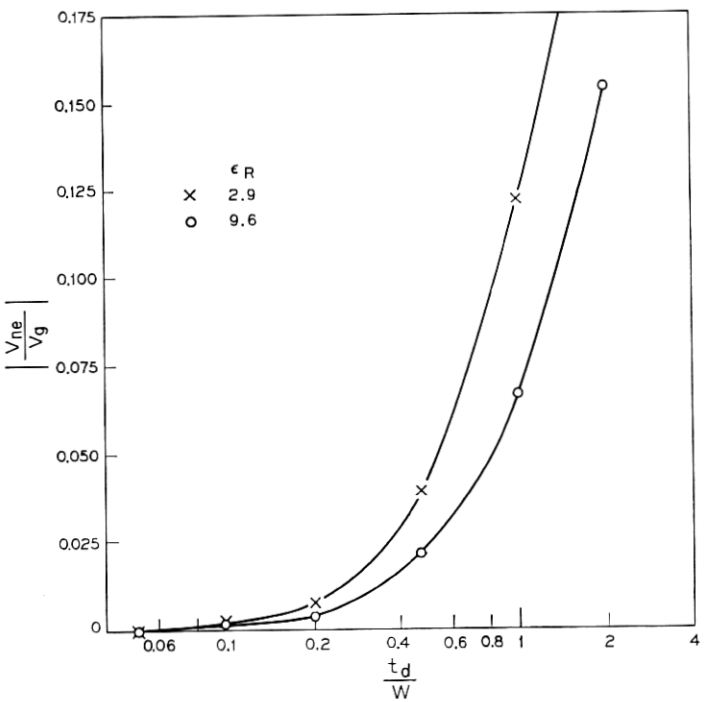

Fig. 20—Near end crosstalk between adjacent, parallel 50Ω microstrip lines ($t_m = 0$.)

TABLE IV—50Ω STRIPLINES ON 0.625 MM ALUMINA SUBSTRATES

Line width	0.625 mm
Delay time	0.05 nsec/cm
Attenuation	0.048 db/cm
Crosstalk	6.75%

Proof: (See Fig. 21)

Write

$$\sum_{N=0}^{Z_i} T(N) = S_i \tag{35}$$

from inequality (33),

$$\sum_{N=i}^{i+1} T(N) > \sum_{N=i+2}^{i+3} T(N) \tag{36}$$

so

$$S_{i+1} - S_i > S_{i+3} - S_{i+2}\,; \tag{37}$$

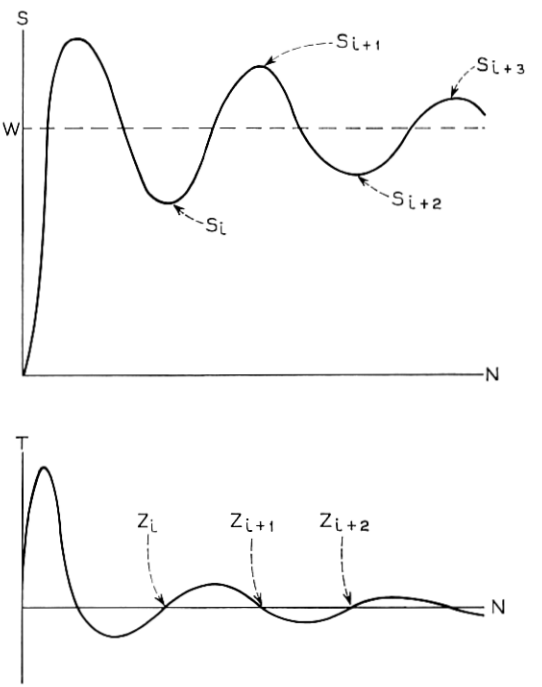

Fig. 21—Enumeration of extrema and zero crossings.

from inequality (32)

$$| S_i - S_{i+1} | > | S_{i+2} - S_{i+3} | \tag{38}$$

so

$$| S_i - S_{i+2} | > | S_{i+1} - S_{i+3} |; \tag{39}$$

similarly

$$| S_{i+1} - S_{i+3} | > | S_{i+2} - S_{i+4} | \tag{40}$$

so

$$| S_i - S_{i+2} | > | S_{i+1} - S_{i+3} | > | S_{i+2} - S_{i+4} |. \tag{41}$$

Write

$$S_\infty = W. \tag{42}$$

Inequality (41) holds for any i chosen in agreement with inequality (32) as $i \rightarrow \infty$. Then

$$| S_i - W | > | S_{i+1} - W | > | S_{i+2} - W | \tag{43}$$

define

$$A_i = \frac{S_i + S_{i+1}}{2} \tag{44}$$

but from inequality (43)

$$| S_i - W | > | S_{i+1} - W |$$

and from inequality (32)

$$S_i < S_{i+1}$$

so

$$W - S_i > S_{i+1} - W, \tag{45}$$

giving

$$S_i + S_{i+1} < 2W \tag{46}$$

so

$$A_i < \frac{2W}{2} = W. \tag{47}$$

From inequality (44)

$$A_{i+1} = \frac{S_{i+1} + S_{i+2}}{2} \tag{48}$$

but from inequality (43)

$$| S_{i+1} - W | > | S_{i+2} - W |$$

and from inequality (32)

$$S_{i+2} < S_{i+1}$$

so

$$S_{i+1} - W > W - S_{i+2}\,, \tag{49}$$

giving

$$S_{i+1} + S_{i+2} > 2W \tag{50}$$

so

$$A_{i+1} > \frac{2W}{2} = W \tag{51}$$

from inequality (47) and (51)

$$A_i < W < A_{i+1} \tag{52}$$

and the theorem is proved.

APPENDIX B

Edge-ground Capacitance for Microstrip

The capacitance from the edges of the finite thickness strip above the infinite ground plane is equivalent to the capacitance problem represented in Fig. (22a). This is equivalent to twice the capacitance represented in Fig. (22b). The conformal transformation $W = \sin^{-1}(z/t_d)$ results in the configuration of Fig. (22c). The capacitance per unit length of this configuration can be calculated by equations (26) and (27) of the text. This results in

$$C \sim \frac{\epsilon_0 \epsilon_R}{\pi} \left[\cosh^{-1} \left(1 + \frac{t_s}{t_d}\right) + \ln \left(1 + \{1 - \exp\left[-\cosh^{-1}\left(1 + t_s/t_d\right)\right]\}^{\frac{1}{2}}\right)\right].$$

For $t_s \gtrsim t_d$,

$$\cosh^{-1}\left(1 + \frac{t_s}{t_d}\right) \simeq \ln\left(2 + \frac{2t_s}{t_d}\right).$$

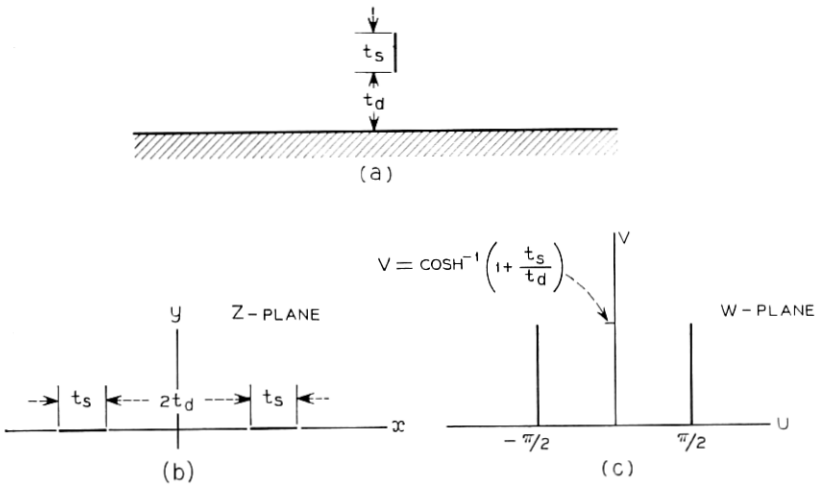

Fig. 22—Conformal mappings.

Then

$$C \simeq \frac{\epsilon_0\epsilon_R}{\pi}\left\{\ln\left(\frac{2t_d + 2t_s}{t_d}\right) + \ln\left[1 + \left(\frac{t_d + 2t_s}{2t_d + 2t_s}\right)^{\frac{1}{2}}\right]\right\},$$

$$= \frac{\epsilon_0\epsilon_R}{\pi}\ln\left\{\frac{2t_d + 2t_s + [2(t_d + t_s)(t_d + 2t_s)]^{\frac{1}{2}}}{t_d}\right\}.$$

The edge-ground capacitance is then

$$C_e = \frac{2\epsilon_0\epsilon_R}{\pi}\ln\left\{\frac{2t_d + 2t_s + [2(t_d + t_s)(t_d + 2t_s)]^{\frac{1}{2}}}{t_d}\right\}.$$

REFERENCES

1. Holt, V. E., unpublished work.
2. Kennedy, D. P., "Heat Conduction in a Homogeneous Solid Circular Cylinder of Isotropic Media," IBM Report TR 00.15072.699, December 4, 1959.
3. Morse, P. M., and Feshbach, H., *Methods of Theoretical Physics*, New York: McGraw-Hill and Company, 1953.
4. Watson, G. N., *A Treatise on the Theory of Bessel Functions*, Cambridge: Cambridge University Press, 1952.
5. Schneider, M. V., "Microstrip Lines for Microwave Integrated Circuits," B.S.T.J., *48*, No. 5 (May–June 1969), pp. 1421–1444.
6. Kordos, R. W., "Analysis of Crosstalk between Microstrip Lines," Record of IEEE Region 3 Convention (April 22–24, 1968), pp. 14.3.1–14.3.3.
7. Assadourian, F., and Rimai, E., "Simplified Theory of Microstrip Transmission Systems," Proc. IRE, *40*, No. 12 (December 1952), p. 1651.
8. Wheeler, H. A., "Transmission-Line Properties of Parallel Wide Strips by a Conformal-Mapping Approximation," IEEE Trans. of Microwave Theory and Techniques, *MTT-12*, No. 3 (May 1964), p. 280.

9. Seckelmann, R., "On Measurements of Microstrip Properties," Microwave Journal, *61*, No. 1 (January 1968), pp. 61–64.
10. Caulton, M., Hughes, J. J., and Sobol, H., "Measurements on the Properties of Microstrip Transmission Lines for Microwave Integrated Circuits," RCA Review, *27*, No. 3 (September 1966), p. 377–391.
11. Moore, R. K., *Traveling-Wave Engineering*, New York: McGraw-Hill, 1960.
12. Ramo, S., and Whinnery, J. R., *Fields and Waves in Modern Radio*, New York: John Wiley, 1956.
13. English, T. D., and McNichol, J. J., "Integrated Transmission Lines for Magnetic Thin Film Memories," IEEE Trans. on Magnetics, *MAG-1*, No. 4 (December 1965), p. 272.
14. Thomson, J. J., *Recent Researches in Electricity and Magnetism*, London: Clarendon Press, 1893.
15. Joines, W. T., unpublished work.
16. Hyltin, T. M., "Microstrip Transmission on Semiconductor Dielectrics," IEEE Trans. on Microwave Theory and Techniques, *MTT-13*, No. 6 (November 1965), p. 777.