No. 1 ESS ADF:

Autonomous Data Scanner and Distributor

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This paper describes the operation and design features of the data-scanner distributor for the No. 1 ESS ADF. The objective was to design a unit which could handle handshaking, addressing, and message transmission for a large number of duplex data lines at a low cost and with the ability to accommodate all speeds and codes now commonly used in low-speed data machines.

The storage medium chosen employs ultrasonic delay lines in a highly time-shared mode. This permitted a compact design which provides input/output capabilities to serve 512 fully duplex data lines. By using a high-speed scan, each character bit of each line is sampled many times. Thus, highly distorted input data can be successfully processed, and output data is essentially distortion free.

I. INTRODUCTION

Equipment to perform the input/output function in a data-switching system handling a large number of connecting data lines has been one of the most expensive and space-consuming parts of the system. This is due primarily to complex handshaking requirements and to the need for handling addressing and all message text by the input/output unit. To achieve an economical solution, a wired logic unit was designed with the extensive use of ultrasonic delay lines in a time-shared, multiplexed mode.

This paper describes the system organization, the logic, and the circuits that are unique to the data-scanner distributor (DSD) for the No. 1 Electronic Switching System, Arranged with Data Features (No. 1 ESS ADF). Unique designs—such as the data line circuit, the delay-line memory loops, the addressing structure, and the control unit logic—are presented. Also, some of the unique maintenance features required for an autonomous wired logic unit that were employed are described.

II. GENERAL DESCRIPTION

The autonomous DSD terminates 512 half-duplex (HDX) or full-duplex (FDX) lines operating with Baudot codes at 60, 75, and 100 words per minute; CCITT code at 66.6 words per minute; and ASCII codes at 100 and 150 words per minute. The DSD's basic function is to perform the serial-to-parallel and parallel-to-serial conversions on the data bit streams; these conversions provide a compatible interface between a large number of low-speed data lines and the ADF system and provide the time buffering needed because of speed differences at the interfaces. The DSD changes the Baudot or ASCII characters which are in serial form on the customer's line into parallel characters for efficient handling in the system and reconverts the parallel words being sent to the data stations into serial characters. The DSD must perform these functions to agree with the format of the data machines on each customer line.

A simplified block diagram of the DSD unit is shown in Fig. 1. This DSD unit is duplicated except for the line-terminating circuits and is capable of providing service for 512 FDX, low-speed asychronous data lines, each capable of being assigned to any one of six TTY rate/code types.

The DSD unit is a time-division multiplex system with 1024 time-slots—an input and an output slot for each of 512 lines. The common control of the DSD samples each line approximately 1650 times a second and stores the sample at the center of each data bit. This sampling frequency permits sending characters with a maximum of

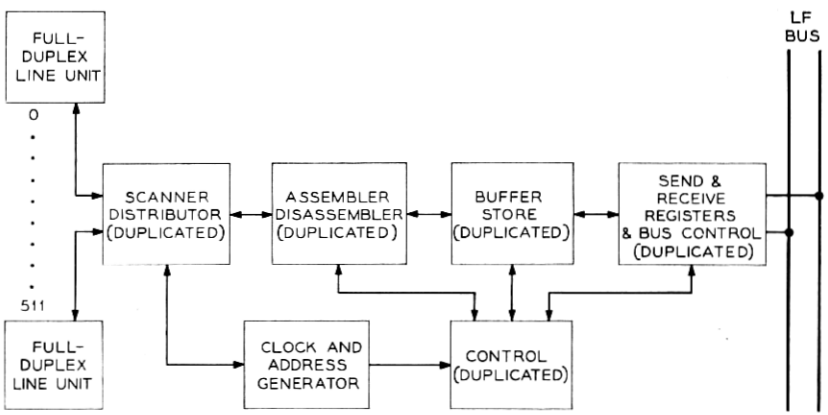


Fig. 1—Block diagram of the data-scanner distributor.

one percent distortion and accepting characters with up to 45 percent distortion at 150 baud.[1]

A high-capacity, line-address-oriented dynamic delay line memory, with access at the scan rate, is used to handle character assembly, disassembly, and control requirements. Sufficient buffering is provided to allow reasonable transfer time across the interface between the DSD and the processing system. To meet these needs, the scanner distributor provides storage for six data characters and two control words for each customer duplex line served as follows:

(*i*) an input character being assembled,
(*ii*) a completed input-data character,
(*iii*) an output-data character being disassembled,
(*iv*) three output-data characters awaiting transfer to the disassembler,
(*v*) a control word for input-character scanning, and
(*vi*) a control word for output-character transmission and sequencing.

To comply with reliability and maintenance requirements of the ADF system, the DSD has two independent, duplicate halves, each receiving inputs from a common line-terminal area but having separate access to the system. Furthermore, the two halves operate in the duplex and synchronized mode as well as in a divorced simplex mode in which either half can continue to serve the entire line-terminal load while the other half is out of service for maintenance.

The DSD communicates with the buffer control (BC) by means of the line facility bus system, which is electrically equivalent to the No. 1 ESS call-store bus system.[2] A reliable high-speed communication bus between the scanner and BC is necessary to handle the magnitude of data transfers, service requests, and maintenance operations. All DSDs in the office share duplicated send, control, and receive bus systems with each DSD capable of accessing either bus. Each scanner responds to its own name code (sent on the control bus) and communicates over either or both duplicated bus systems as directed by the central control. Central control (CC) has the option of changing or rerouting the bus assignments when a unit requires maintenance. The DSD maintenance programs update the DSD memories and resynchronize a DSD to restore it to duplicate processing when the out-of-service unit is to be returned to service.

Each DSD possesses flags in the form of ferrods which are scanned periodically to determine the state of health of each DSD. If failure

occurs, the unit divorces itself from the line circuits and operates the proper flag which, in turn, calls in the CC to perform fault recognition and diagnostics.

Power to each half of the DSD must be independent of power to the other half. However, common circuits such as line-terminal units, clock circuits, and delay-line oven heaters must receive power on a logic OR basis from separate power buses so that they are always functional as long as power is on either DSD.

III. SYSTEM OPERATION

3.1 *General*

The organization of the DSD makes it equivalent to a start-stop TTY with a capacity to handle simultaneously 512 duplex-line terminals. Each connecting line terminates in a line circuit serving each of the duplicated DSDs. A fully equipped scanner distributor utilizes 3103 No. 1 ESS type circuit boards of which 1024 are used for line termination. For every 606.06 μs, each line is addressed for 1.184 μs; this time is devoted to both inputting from the customer line and outputting to the line, assuming it is FDX.

3.2 *Input/Output Processing*

If during the input time the line is found in a "space" state (0), this fact is sent through the converging tree to the start-detect delay line and stored in the time-slot corresponding to the particular address. This operation requires 0.592 μs of the address time; similarly, during the other 0.592 μs of address time a bit is sent to the same connecting line. Since the lines are addressed in sequence, they are connected to the assembler/disassembler through a converging ORing circuit for inputting, and through a diverging ORing circuit for outputting. Each line circuit is connected through these OR circuits to the "type" gates, depending on how the TTY terminal is equipped. When the address comes up, the line-terminating circuit actuates a select circuit, which enables the proper type gates for the line being addressed for both into and out of the assembler/disassembler. A pulse from the control unit decoders enables the type gates at the appropriate count permitting data bits to be gated into the assembler during inputting time and gating the data bits out of the disassembler during outputting time. A block diagram of the input function is shown in Fig. 2.

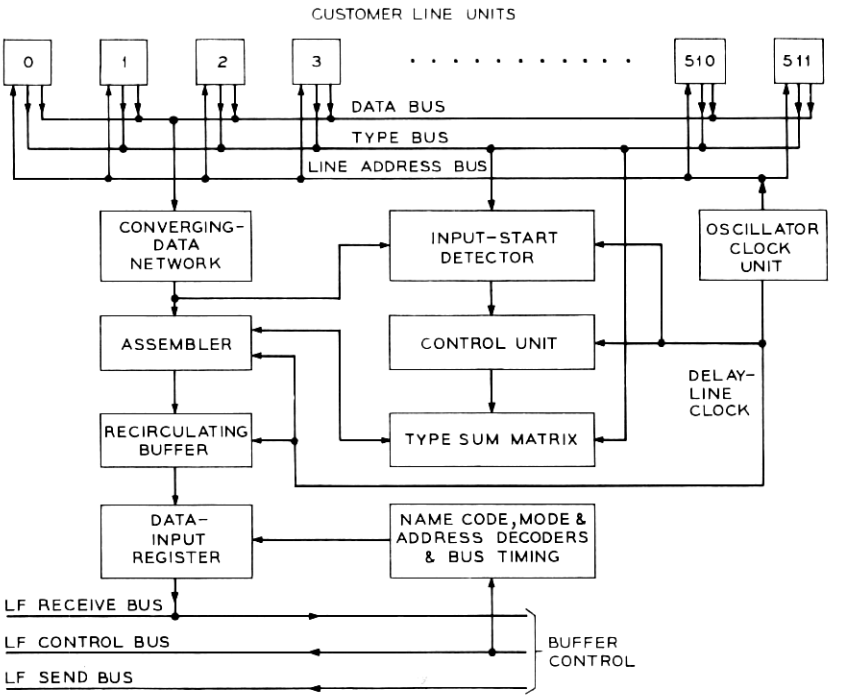


Fig. 2—Simplified functional block diagram DSD input portion.

The assembler/disassembler is a group of 11 delay lines used simultaneously to assemble and disassemble serial characters as required for data line operation: line 1 stores the start bit, line 2 stores the first data bit, etc. The number of bits stored depends on whether a Baudot or ASCII code is required for a particular line. In addition one of the 11 lines is used for parity, internally generated for maintenance purposes. The filling of the assembler/disassembler or the emptying of it is controlled from the control unit. This process is referenced to the start bit which is always the first bit of the character string.

When the counter has completed the count for a particular line address, the contents of the assembler are gated out in parallel form to the recirculating buffer. The character remains in this circulating buffer store until it finds the data-input register empty, at which time it is gated into the register along with the line address from the address counter. A service request is set up, and a parity bit is added

to the data and line address. The data now waits for the buffer control to recognize the service request and accept the contents of the data-input register.

For outputting, a similar process is followed (see Fig. 3). The control unit empties the disassembler one bit at a time to the subscriber line. When a character is completed, as determined by the control counter, the next character is gated out of the recirculating buffer in parallel form into the disassembler. Since the output buffer receives three characters at a time from BC, sequence logic is required to control orderly flow of the characters into the assembler/disassambler. Two delay lines are used to store these control bits for each customer line address.

As Table I indicates, the DSD insures a marking state on the customer line even though the line is idle. As long as a customer line is active, the control count continuously recycles, and the sequence bits rotate through the 3-count sequence for characters 1, 2, and 3 without returning to the idle state.

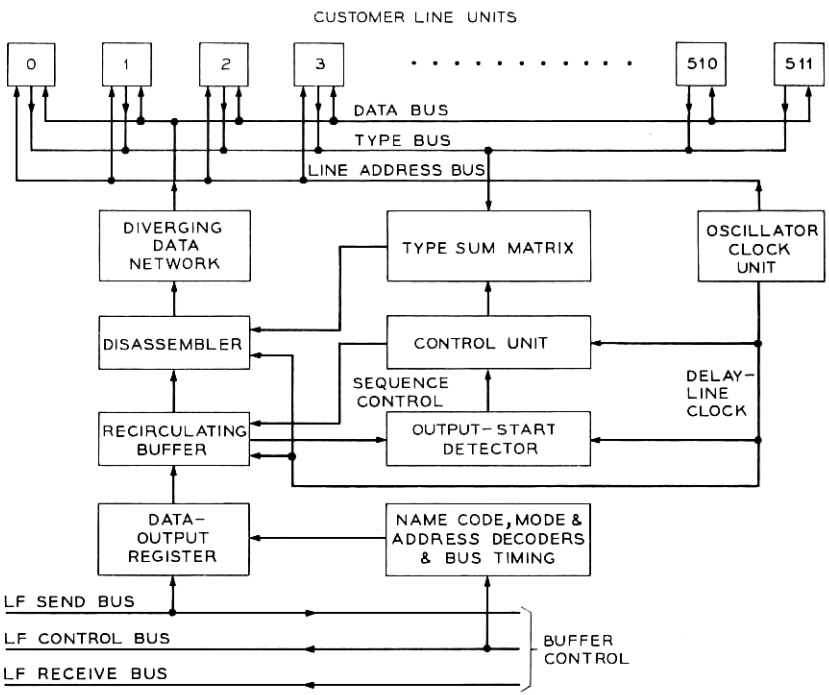


Fig. 3—Simplified functional block diagram DSD output portion.

TABLE I—SEQUENCE BITS
(Control of Buffer-to-Assembler/Disassembler Interface)

SEQ Bit 0	SEQ Bit 1	Function
0	0	Idle (Marking)
1	0	Gate Character 1 and Start Count
0	1	Gate Character 2 and Start Count
1	1	Gate Character 3 and Start Count

The sequence bits also set up a service request when the third character has been loaded into the disassembler. Along with the service request is a line address which makes it possible for the BC to fetch the proper data for the line address being served.

The control system in the DSD consists of the clock, the address counters, and the time-shared arithmetic unit. The latter unit provides the gating signals for loading and unloading the assembler/disassembler at the times required by the line types. It also provides the signals for loading and unloading the recirculating buffer at the assembler/disassembler interface. When a customer line becomes active, the start bit is added at each turn of the delay lines to the contents of the 9-bit control counter, which indexes the number by one. When the binary number in the control-unit recirculating store reaches the predetermined count for the type of line, a gate pulse is produced to transfer a character bit. Thus, it is this time-shared adder that controls the flow of characters through the DSD.

IV. MEMORY DESIGN

4.1 *Delay Line Memories*

The memory medium selected for the DSD was the ultrasonic aluminum delay line.[3] Twenty lines are housed in a 23″ by 10.3″ by 6″ temperature-controlled box. Thus, 18″ of rack space contain 61,440 bits of serial memory with a 606.06-μs recycle time. The logic involved in the delay line memory loops is shown in Fig. 4. The delay lines are nominally 300 Ω at the input and output terminals with an insertion loss of 36 dB $\pm$ 0.5 dB. To provide for the various loop-transmission tolerances, the line had to provide a 5-to-1 pulse to side lobe ratio under the worst-case bit pattern of alternate 1s and 0s. Because of the relatively high temperature coefficient of the aluminum used as the delay medium, the lines were housed in an insulated box and held at 60°C $\pm$ 0.03°C controlled by an on/off power switch with a fine mercury-

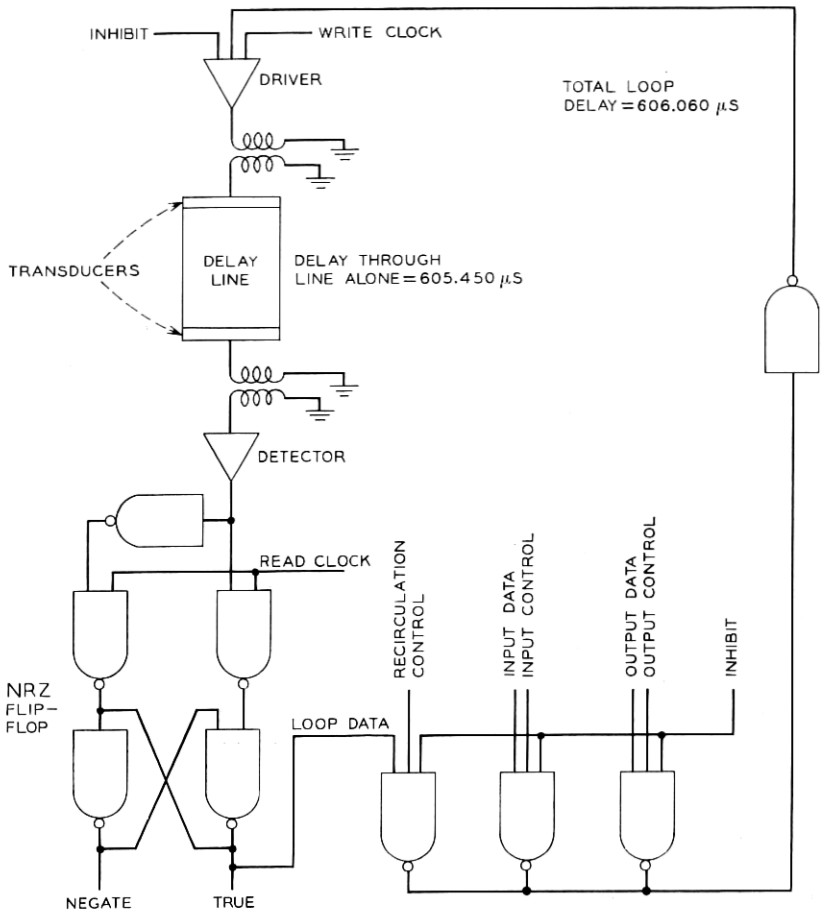


Fig. 4—Typical delay-line loop.

column thermostat as the sensing element. Two alarm thermostats are included to sense when the temperature-control circuits develop trouble. These are set to notify the system of failure in the temperature-control circuit before the line delay has changed sufficiently to cause data-processing errors. When this occurs, one of the alarm thermostats is actuated and the fault-recognition program removes the faulty DSD half from service.

To achieve the main lobe to side lobe ratio required, the piezoelectric transducers located at each end of the aluminum strip were

tuned about 25 percent higher in frequency than the scanner-clock frequency.

This technique made the side-lobe vector sum when a 0 appears between two or more 1s in a data stream to be no higher in amplitude than a side lobe of an individual isolated 1 pulse. This transducer tuning assures the required signal-to-noise ratio for any bit combination stored in a line loop. Typical waveforms for several bit patterns at the delay line output are shown in Fig. 5.

Each scanner utilizes 58 delay lines to implement both the input and output functions. The address time of 1.184 μs is divided, the first 0.592 μs is used for outputting, and the last 0.592 μs is used for inputting. The timing cycle for each delay line is shown in Fig. 6.

The 58 lines are arranged in the following functional groupings: 11 lines in the assembler/disassembler, 10 data and 1 parity; 33 lines

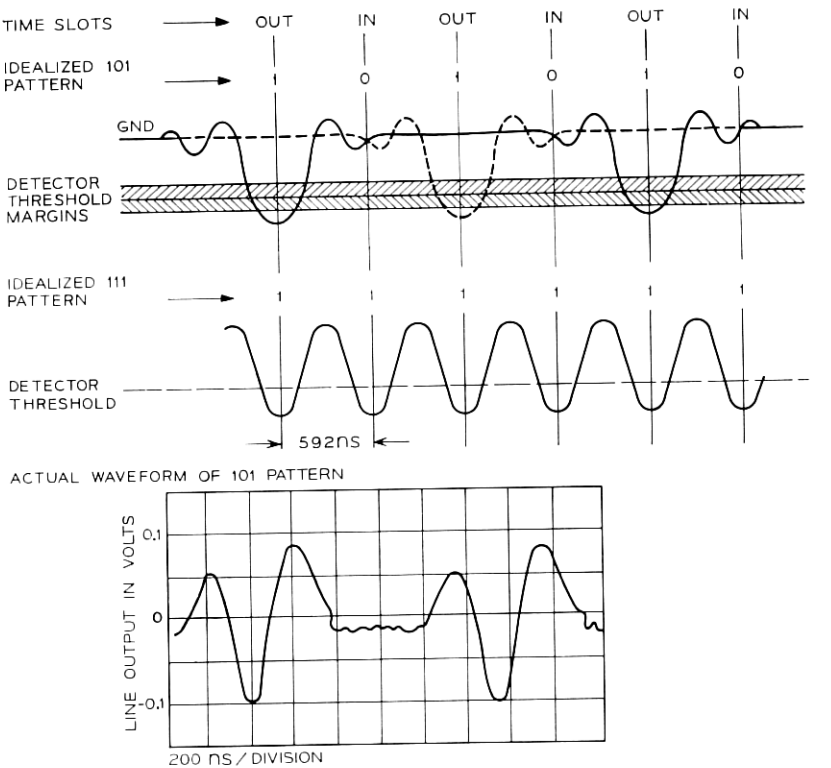


Fig. 5—Delay-line waveforms.

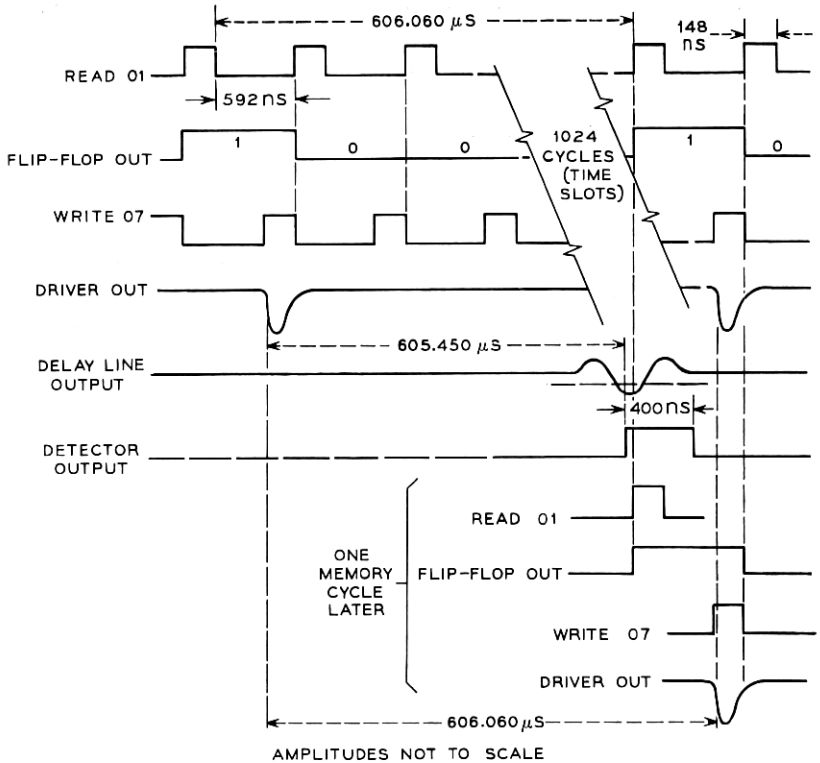


Fig. 6—Delay-line loop timing.

in buffer store, 10 data and 1 parity for each of the three characters; 14 lines in the control unit.

The delay-line driver circuit shown in Fig. 7a provides a constant drive current independent of power-voltage variations by regulating the base voltage of the driving transistor. Figure 7b shows the receiver circuit with approximately 20-dB gain stabilized by feedback plus a pulse stretcher for absorbing loop tolerances.

V. INTERNAL LOGIC STRUCTURE

5.1 *General*

A complete DSD consists of the basic functional sections as shown in Fig. 8. All normal operating logic has maintenance circuits and operational logic interspersed. Physically the duplex unit is housed

in five racks arranged symmetrically about the center rack. Common circuits such as the oscillators in the center rack and the line terminations arranged in the two end racks are equally divided.

5.2 *Clock*

The oscillator-clock unit (OCU) is designed to supply the primary timing waveforms for the DSD with no discontinuity in frequency or phase. The OCU utilizes a pair of crystal oscillators phase-locked in a master slave configuration. The design is such that a catastrophic failure of either oscillator or the phase-locked circuit by itself will cause minimal phase discontinuity of the waveforms. Figure 9 is a simplified block diagram of the OCU.

The oscillators generate the primary frequency of 3.3792 MC with

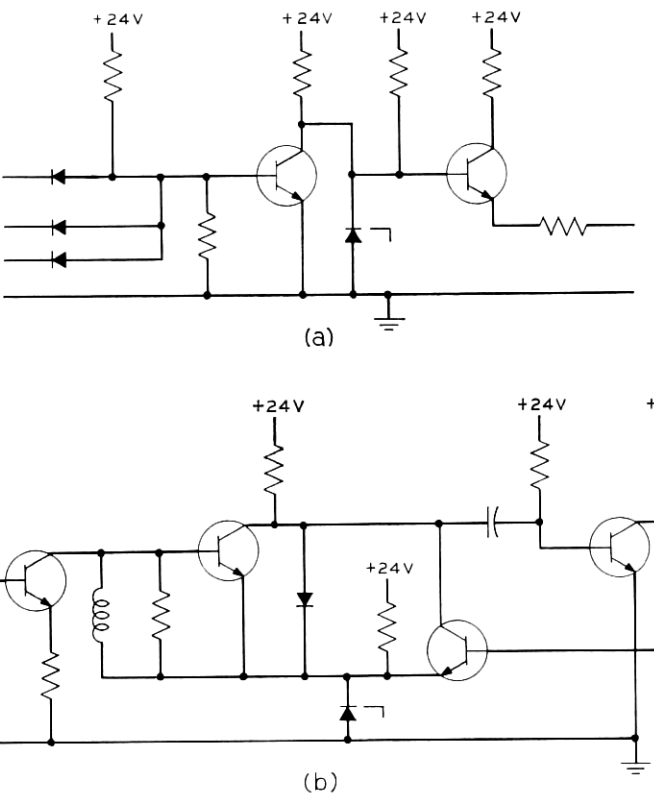


Fig. 7—(a) Delay-line driver. (b) Delay-line receiver.

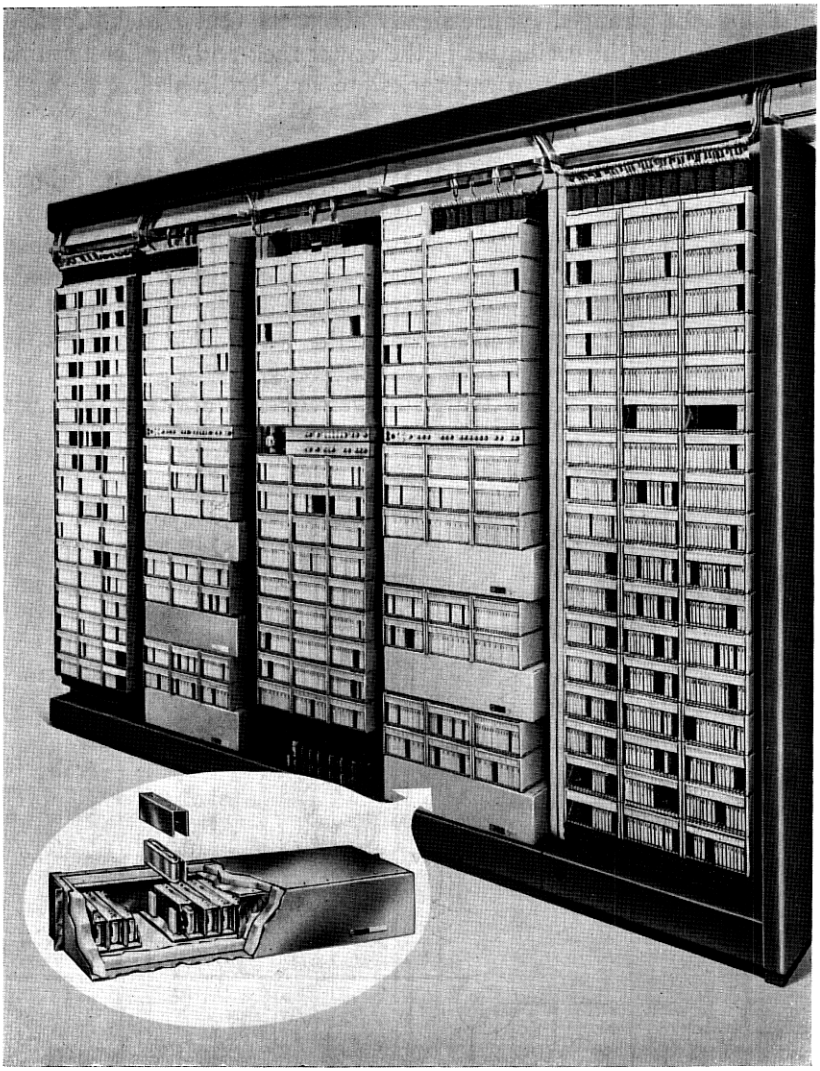


Fig. 8—DSD with detail of delay-line memory.

an accuracy of 20 ppm over a temperature of 0°C to 55°C. The phase-locked sinusoidal signal from the slave oscillator is mixed on a binary-weighted basis with the signal from the master oscillator. The resultant sine-wave output is the vector sum of the individual oscillator signals. This signal is next resolved into two phases. One phase is that of

the resultant signal itself, and the other is derived by means of a 90° (74-ns) phase-shifting network. The two phases are individually shaped into symmetrical ac-coupled square waves by means of a nonsaturating differential amplifier stage. The shaped signals are routed to individual phase-splitting circuits where each wave is further resolved into two signals 180° out of phase. In this manner the OCU produces four phases of primary clock waveforms for one simplex DSD and duplicates these stages for the other simplex DSD beginning with the binary mixer.

5.3 *Address Structure*

Each simplex DSD unit contains two sets of binary counters known as the left and right address counters, which are toggled by the high-frequency output gates of the clock. Waveforms for the address and toggle pulses are shown in Fig. 10.

The toggle is used as the least-significant bit of the 9-bit address. The eight bits of the left counter address lines 0 through 255, and the right 8-bit counter addresses lines 256 through 511. The toggle produces an interleaving of the two groups of line units so the addressing goes 0, 256, 1, 257, $\cdots$, 255, 511. In this way each counter is running at half-rate and thus permits the line-terminating logic ample time to settle before data is received or sent to the customer's line. The resultant waveforms from the left counter overlap those of the right counter by an amount equal to the toggle half-period as indicated in Fig. 10.

Figure 11 is a simplified block diagram of the address-counter sys-

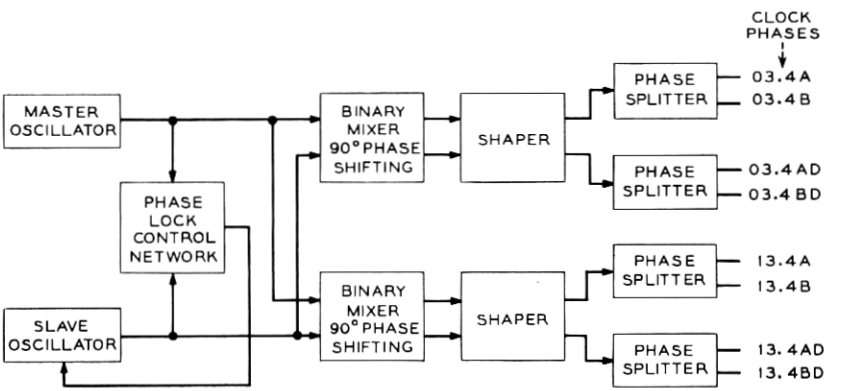


Fig. 9—Block diagram of oscillator-clock unit.

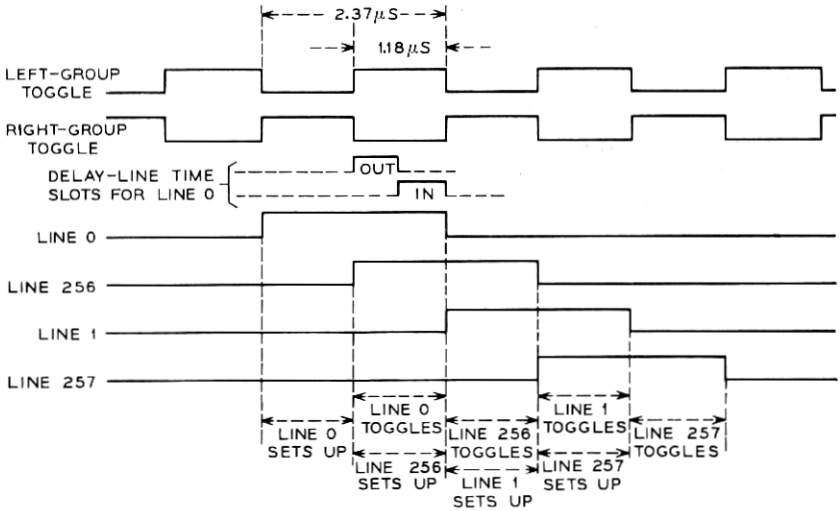


Fig. 10—Line address and toggle system.

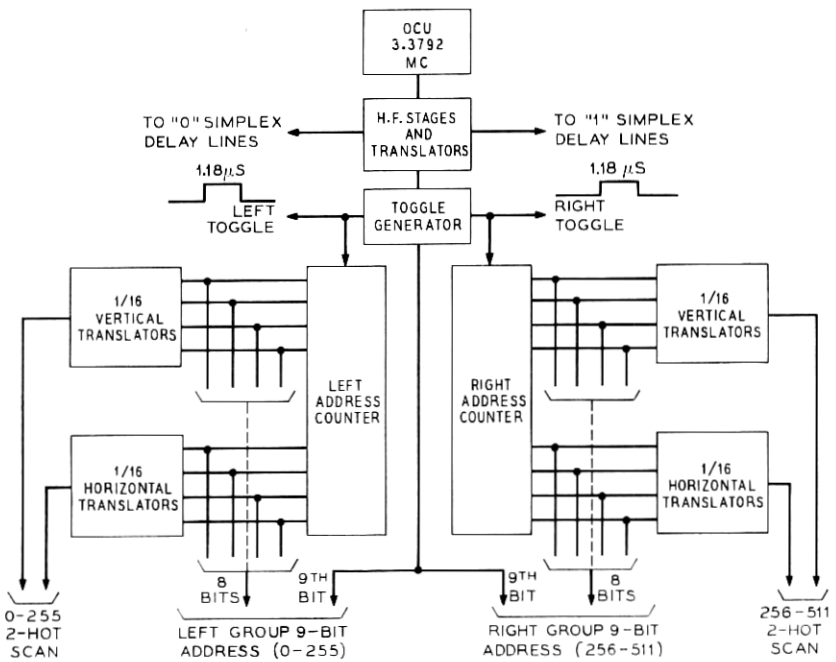


Fig. 11—Block diagram of address counters.

tem. In addition to the 9-bit address, each of the counters, left and right, drives two sets of 1-of-16 translators to develop the 2-hot scan system to the line terminals. The last stage of translation of 1-of-512 is in each line terminal unit. The matrix formed by the horizontal and vertical translator output distribution determines the sequence of line addressing.

5.4 *Data Line Input/Output Circuit*

Data is transmitted in and out of the DSD to and from the data network through standard multilead switchboard cable used in an unbalanced dc connection. It is expected that some installations of these cable lengths may be several thousand feet. Noise and crosstalk might be higher than could be tolerated with the standard No. 1 ESS logic. To provide sufficient margin, a special line-terminating pack was designed. The logic circuit is shown in Fig. 12. The logic level was

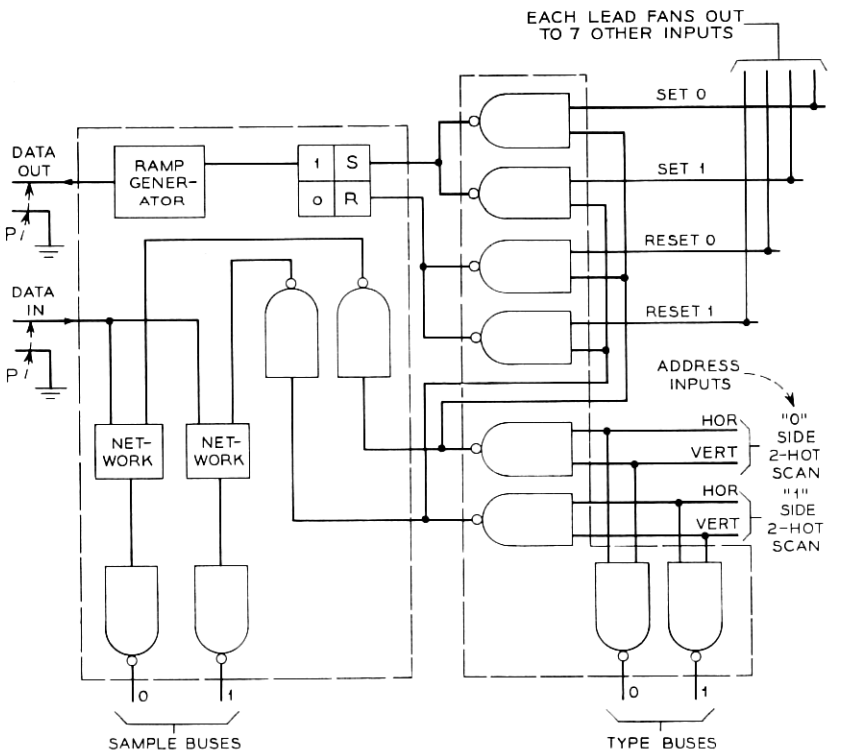


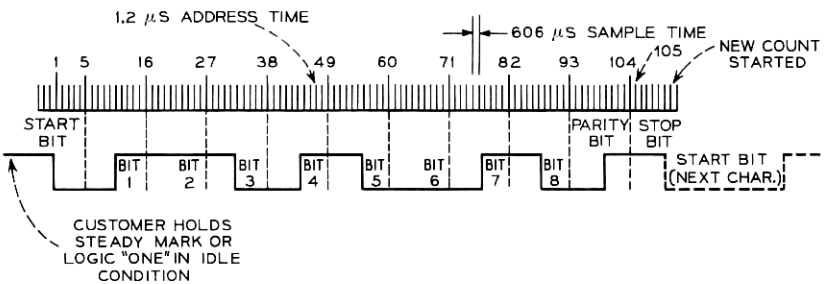
Fig. 12—Line-terminal unit.

raised to 12 V, and the leading and trailing edges of the character pulse were made to rise and fall linearly at approximately 1 volt per microsecond.

When addressed, the line unit logic is unclamped allowing input and output transmission to occur. Also, a type signal is placed on the appropriate type bus to gate this data in and out of the assembler/disassembler.

5.5 *Scan Control*

The control count at which specific actions are taken during the process of taking samples of input data or generating transitions of output data is determined by the type of code assigned to serve the line-terminating unit (LTU). Figure 13 shows an example of the control count sampling intervals for an ASCII 150-word per minute character. The element duration for this code is 6.67 ms, and the scan rate of 606.06 μs allows a minimum of 11 scans per element. As soon as an input start is detected, the control counter begins to count; when the count of five is reached a sample of the start bit, which is present on the customer's data input, is taken. The sample is within the window bounded by the middle 10 percent of the element and is thus taken at a distortionless point as required in high distortion TTY signals. Succeeding samples are taken at 11 scan intervals, such as 16 for bit 1, 27 for bit 2, and so on to the end of character count.



1. START DETECTED	CONTROL UNIT COUNT STARTED	7. BIT FIVE READ IN	COUNT 60
2. START BIT READ IN	COUNT 5	8. BIT SIX READ IN	COUNT 71
3. BIT ONE READ IN	COUNT 16	9. BIT SEVEN READ IN	COUNT 82
4. BIT TWO READ IN	COUNT 27	10. BIT EIGHT READ IN	COUNT 93
5. BIT THREE READ IN	COUNT 38	11. STOP BIT READ IN	COUNT 104
6. BIT FOUR READ IN	COUNT 49	12. END OF CHARACTER	COUNT 105

Fig. 13—Control-count intervals for inputting the TTY character K. (Binary 1101001 ASCII 150 with even parity.)

The character now assembled is transferred to the buffer by the counter after which it is reset to zero awaiting the start of the next input characters. Each of the sampling points is thus predetermined for a given code type, and a fixed-count sum can be established to enable proper sample-scanning action. The samples are derived from wired logic patterns from the outputs of the control delay line group. The control unit utilizes nine delay-line loops in addition to the start detect loop in its add-one counter section. A fast-carry logic incrementer is used to steer the counting action to the delay line loops. Figure 14 illustrates a segment of the control counter. The outputs from the counter enable the choice of any integral 9-bit code required for a sampling point. The highest sum required is determined by the slowest code type. The total number of gates required for sampling one code type depends on the number of elements in the code. A Baudot 60 line, for example, requires a count of 269 to complete the generation of an output character, but requires fewer sum gates for sampling since it is a 7-element code. The type-sum gates are an array of gates that input and output data to and from the assembler/disassembler. These gates are controlled by ANDing the type bus and the decoded control unit output and the data pulses for each of the 1024 time slots. The array of sum gates are arranged by type in a matrix. The matrix consists of a 6 by 10 gate array corresponding to the number of types (6) and the maximum number of bits in the ASCII code. All of the outputs of the type-sum matrix converge to the input gates of the assembler/disassembler.

5.6 *Assembler/Disassembler Unit*

The assembler/disassembler is a group of 11 delay-line memories used as a time-shared shift register for both input and output functions. The outputs of the type-sum matrix are fed in order to the input gates of each delay-line loop in the assembler/disassembler where the data sample bus also converges. Each element of an incoming character is sampled into the proper time slot and delay line as the simultaneous occurrence of the customer's scan interval and a particular count in the control unit take a sample of the data bit from the LTU. For example, as shown in Fig. 13 for an ASCII 150 coded line, the start element is sampled on the fifth interval after the start transition has been detected and the control count has started. The start-element sample is stored in the first delay-line loop of the assembler. In the same manner, the following elements are sampled

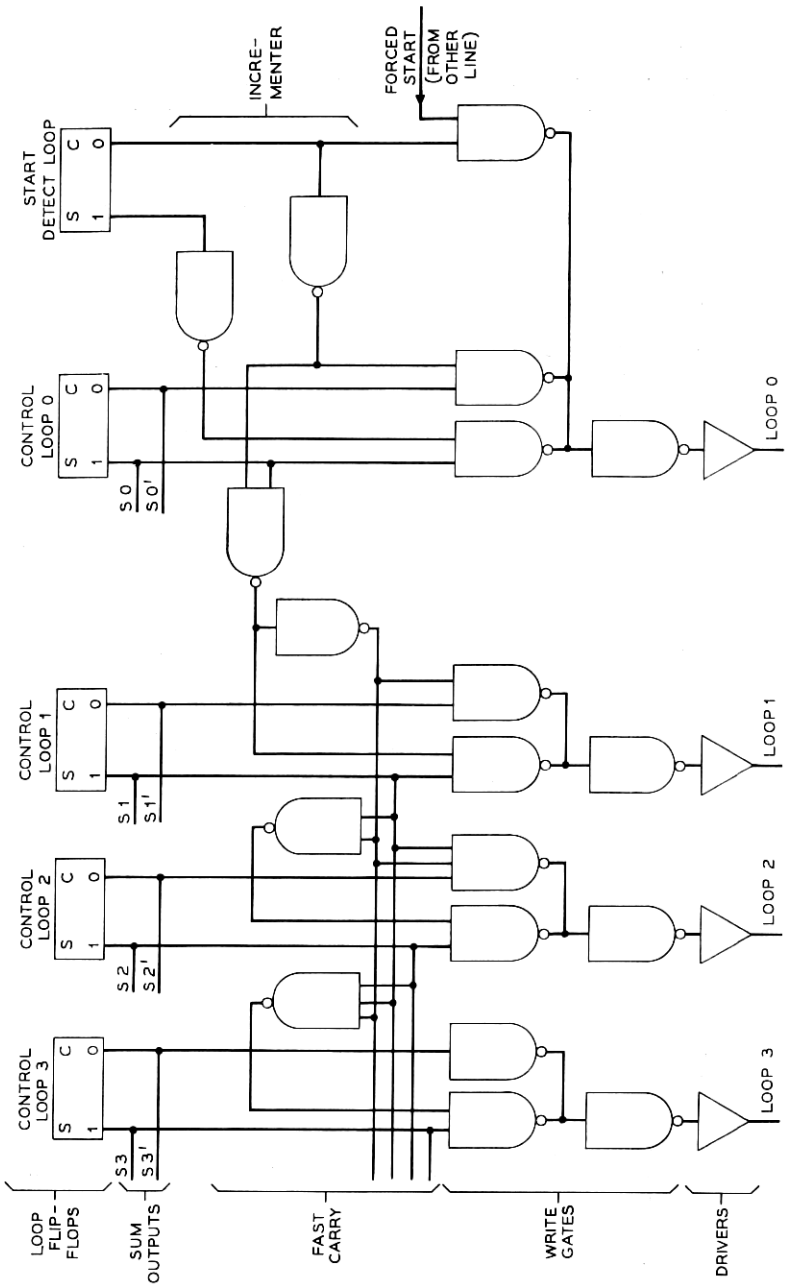


Fig. 14—Simplified sketch of control counter.

at later count intervals and are stored in proper sequence: bit 1 in the second line of the memory, bit 2 in the third line of the memory, and so on, until a complete character is stored in the same time-slot of each memory line. Each successive sample continues to circulate the delay-line memory loops until all samples have been stored for the character being assembled. When completed it will be read out in parallel form to the recirculating buffer. Each set of time-slots in the assembler is under independent control of the control unit. The assembler may be assembling at one time as many as 512 incoming characters in various stages of completion.

These functions of processing the characters through the DSD for both data input and output are controlled by the time-shared control counter described in Section 5.5.

The output time-slots of the assembler/disassembler unit are used for the disassembling process of output data. The output operation is just the reverse of the input operation. When a parallel character enters the disassembler from the recirculating buffer it is read out in serial to the customer line. An output count is started in the control unit at the time the character is read out of the recirculating buffer. At specific count increments, determined by the proper spacing for undistorted elements, the data stored is sampled out of the disassembler, element by element, to set or reset the output flip-flop in the LTU for the customer line to which it is directed.

Data in all delay lines of the assembler/disassembler is always stored in true form. A mark is represented by a logic 1 in the line, and a space is represented by a logic 0. Because the Baudot and CCITT codes do not involve as many elements as the ASCII codes, ten delay-line loops are sufficient to store all code types. Only one stop element is stored for any code type. The unused delay-line time-slots for the shorter codes remain in the cleared (logic 0) state at all times. One delay-line loop in the assembler/disassembler is used for internal parity on both input and output characters.

5.7 *Recirculating Buffer Unit*

The recirculating buffer unit is composed of a total of 33 delay-line memories sufficient for three ASCII characters plus parity for each character. These memories are addressed synchronously with those of the control unit and of the assembler/disassembler unit. Fully assembled input characters are transferred from the assembler/disassembler unit to the recirculating buffer at end-of-character count. The

assembled input character elements plus input parity from the assembler/disassembler occupy the input character 1 slots of the recirculating buffer. The character is stored in the recirculating buffer until such time as it gains access to the data-input register where it awaits a normal read request from BC to transmit the character to the system. In the output direction, the recirculating buffer receives three characters from BC. The characters await entry in proper sequence to the disassembler at the time the line address occurs. The sequence bits of the control unit are used for sequentially gating characters 1, 2, and 3 from the recirculating buffer to the disassembler. An individual parity bit is carried through the output process for each of the three characters.

5.8 *Input/Output Registers*

The DSD has seven major logic registers to transfer information between the DSD and the system. Table II lists the registers and their functions. Each of the registers is specifically interrogated by the system by means of mode orders on the control bus. Periodic scans keep input and output data flowing with the assistance of service requests to assure legitimate transfers.

TABLE II—INPUT/OUTPUT REGISTERS OF DSD

Register	Use	Function
Normal Read	Input	Transfer input character to system. (9 data bits, 9 address bits, 1 input service request bit, 1 overwrite bit)
Scan Output	Input	Transfer output service request into system. (9 address bits)
Input Maintenance	Maintenance Read	Transfer maintenance data into system. (12 data bits, 9 address bits)
Output No. 1 and Output No. 2	Output	Receive output data from system. Two registers with priority to No. 1. (Each register 33 data bits, and 9 address bits)
Output Maintenance	Maintenance Write	Receive maintenance instructions from system. (30 data bits, 9 address bits)
Error Status	Maintenance Read	Store trouble reports for transfer to system. (22 data bits)

Maintenance registers are used during routine exercises or diagnostic examinations. The status register is a fast means of reporting the states of vital functions which are internally monitored by maintenance circuits.

Entrance of an input character from the recirculating buffer to the normal-read register is a random operation controlled by the start bit of the character, which is used as the input service request, and a circuit which monitors the empty status of this register. When the normal-read register becomes empty, it accepts the next start bit that appears at the output of the recirculating buffer as a request for service for the address corresponding to the address of the start bit. Simultaneously, the character and the associated address are gated into the normal-read register. The start bit is transmitted with the data to signify that the transfer is legitimate. The overwrite bit is used to indicate when a character has stayed too long in the recirculating buffer and has been overwritten by the next character. This should not happen as long as the BC scan is frequent enough to keep up with the traffic. The BC must scan for service requests fast enough to read a character out of each of the 512 time slots of the recirculating buffer within a period less than the length of time necessary to assemble characters of the fastest code type. Thus, for a DSD connected to 512 ASCII 150 type lines, BC must scan for service requests at least once every 130 μs. The DSD responds to the normal-read mode by dumping the contents of the normal-read register onto the receive bus. This register is cleared by the receipt of an acknowledge signal from BC and is then ready to receive the next data transfer from the recirculating buffer.

The scan output register is used for the transfer of output service requests to BC. Access to the register is on a first-come first-served basis for any customer addresses requiring output service. The DSD automatically sets the output-service request bits for any active line when the output control count has proceeded through two characters and the third character has been gated to the assembler/disassembler unit for disassembly. An output-service request consists of the 9-bit line address for the line requiring service plus a bit in the service-request bit position. BC has one full character time to answer the output-service request to maintain continuous data flow. In the event that it takes longer than one character interval for the 3-character transmission to reach the output registers, the DSD will automatically produce a marking state on the customer line until BC responds with

the next three characters. Once again, the DSD must be scanned for output-service requests often enough to satisfy all 512 lines. One of the two output registers must be available before a service request can be issued but, because of the 3-character transmissions, less time is necessary to service output-service requests than input-service requests. In addition, output servicing can be temporarily deferred, if necessary, in order to devote more time to inputting when traffic is heavy.

Two output registers, identical in design, are used for the outgoing traffic in order to give the DSD more output capability. Since there is no synchronization between the appearance of the output-service request in the scan output register and the reply from BC, the data sent in response to the service request must wait in an output register before release to the RB. The output count must reach the proper level and the memory cycle must progress to an address match for the data to reach the proper time slot. Two output registers help to shorten the waiting interval as well as make more efficient use of the line facility bus time.

5.9 *Duplex Synchronization*

To achieve duplex operation of the DSD, all clock and address counters and all delay-line loops must be initialized in synchronism. Assuming that one unit is operating on-line, the initialization program resets and holds the counters and clears the delay lines of the off-line unit. This is done after first divorcing all matching circuits between the two units and disconnecting the off-line unit from the LTU. The held counters are released to continue counting when the counters of the on-line unit pass through the zero state. Both sets of counters are thus synchronized and are continuously matched to insure that they stay together. Delay-line synchronization is automatic as long as the high-frequency clock stages are synchronized but the data content of the memories must be allowed to update gradually. Output time slots can be updated by ceasing the flow of output data temporarily until all active customer lines can be restarted in the off-line unit and reach an equivalent all-marking state in both units. Input time slots are updated by a process known as forced start, wherein the control unit of the off-line unit is cross-coupled to the input start detect circuit of the on-line half so that input counts are established simultaneouly in both halves. After a fixed interval of time long enough (three character times at the lowest data rate) for the memories to equalize, duplex operation can be restored.

VI. MAINTENANCE FEATURES

6.1 *General*

DSD maintenance is complicated by the use of time-division techniques and by the restricted access to the delay-line memories. In addition, the large number of customer lines terminating in the DSD requires extensive converging and diverging networks which make per line fault-detecting difficult. Further complications arise from the duplex nature of the DSD and the necessity for keeping two on-line units in synchronism. To satisfy the maintenance requirements for the DSD, several special techniques had to be provided. These techniques were designed to enable rapid detection of faults and to allow reconfiguration and diagnosis with no interference to normal data processing.

The two major categories of DSD maintenance can be classified as:

(*i*) External—that which applies to the interface circuits of each simplex.
  (*a*) Line facility bus checks.
  (*b*) Match checks between simplex halves.
(*ii*) Internal—that which applies to the circuits contained within each simplex.
  (*a*) Internal parity.
  (*b*) Automatic disconnects.

One of the techniques used extensively throughout the DSD is known as the 1-hot (or 1-cold) check. This technique is used to monitor circuits where only one out of many similar inputs is to be active at a single instant of operation. The 1-hot check is particularly adapted to the many converging and diverging functions of the DSD. It is also efficient for monitoring-address translators and counter circuits. Special networks and detectors were developed to perform this function.

Another feature used quite extensively in the DSD involves the use of special registers and control-write instructions to direct the extraction of information from any of several points in the data-processing sequence. A total of 23 points in each unit may be interrogated by the control-write point procedure. In addition, use is made of the same access method to set or reset control flip-flops and clamp or hold counters for diagnostic examination. A total of 66 control-group instructions are used for these purposes.

The DSD has been designed to make it possible to repair either

unit without interfering with the operation of the other. Each unit has a completely independent power system and access by program for maintenance purposes. The primary functions such as oscillator, delay-line oven heaters, and customer-line terminals are supplied with ORed power to maintain continuous service. Use of the control group program modes to isolate a unit by divorce or disconnect aids in insuring independence. The DSD also contains eight test-line terminals, each dedicated to a different code type (two are duplicated); these terminals may be used as vehicles for test messages in the course of diagnosis of trouble. Finally, the DSD makes use of visual indicators such as the phase-lock meter for the oscillator and under-and-over temperature alarm circuits as well as lights for the ovens as aids in trouble diagnosis.

6.2 *External Maintenance Checks*

The maintenance techniques classified as external include those associated with line facility bus transmissions and those that match the status of one simplex unit against the other. Transmission checks are similar to those used in the No. 1 ESS and consist of odd parity, all-seems-well (ASW), and acknowledge functions. Cross-coupled match checks are made between on-line simplex halves to detect operational differences that will arise from a fault condition appearing in a simplex. These external matches are generally not capable of determining which unit is in trouble; when a match failure occurs, however, each unit detects the mismatch and inhibits its own ASW signal. In addition, ASW and acknowledge signals are cross-coupled to prevent either of the duplexed units from starting to process data before the other. Information obtained from internal maintenance circuits is used to localize the trouble. These internal checks cause an automatic disconnect of output from the faulty unit to prevent mutilation of data to the customer. Table III lists all external maintenance facilities and their functions.

6.3 *Internal Maintenance Facilities*

The maintenance techniques classified as internal include circuits which are self-contained in each unit and which generate and check internal parities, monitor counters and translators, and perform 1-hot checks on converging and diverging functions. Most internally detected troubles automatically disconnect the output of the faulty unit immediately to prevent mutilation of customer data. Circuits which

TABLE III—EXTERNAL MAINTENANCE

Send Bus Parity (Data) Control Bus Parity (Mode and Address) Stored Parity (Name Code) All Seems Well (ASW) Address Error Bit (ADE) Acknowledge (ACK) Mode Decoder 1-Hot (1/16)	Fault Recognition in Communications
Duplicate Bus Transmission Send and Receive Bus Selection Control Modes	Communications Diagnosis
Forced Start Cross-Match Type Bus Cross-Match Sample Bus Cross-Match Output (Set-Reset) Bus Cross-Match Output Register Cross-Match Address Counter Cross-Match Acknowledge Cross-Match ASW Cross-Match	Duplex Fault Recognition
Monitor Bus Scan Points Central Pulse Distributor	DSD Status Tests

can take such drastic action are limited to those that can determine without outside reference which unit is bad. An input disconnect is never applied automatically; nor can a unit disconnect its output if the other unit is already disconnected. Each unit has a disconnect inhibit to prevent such an occurrence. Control write instructions and control group orders utilize special registers and flip-flops to set up and examine internal circuits of each unit and are therefore classified as internal maintenance.

As a check against the operation of the delay-line loops of the assembler/disassembler and recirculating-buffer units and associated gates and registers, an internal parity is generated and carried through in both input and output directions for every character processed. These internal parities are both odd and are independent of bus parities. Table IV lists the internal-maintenance facilities and their functions:

6.4 *One-Hot Monitors*

The term 1-hot applies to a monitor that looks for one low-level signal out of a group of high-level signals. Conversely, a 1-cold monitor

TABLE IV—INTERNAL MAINTENANCE

Input Data Parity Output Data Parity High-Frequency Toggle Match	Delay Line Fault Recognition
Type Bus (1/192) Type Code (1/6) Type-Sum Gates (1/13)	1-Hot Monitors
Sample Bus (1/32) Set-Reset Bus (1/64) Horiz. Address Trans. (L&R) (1/16) Vert. Address Trans. (L&R) (1/16)	For Logic Diagnostic
Trouble Flip-Flops Divorce Flip-Flops Disconnect Flip-Flops Disconnect-Inhibit Flip-Flops R0, S0, S1 Flip-Flops	Configuration Control
Oscillator Level Detectors Phase Lock Meter Address Counter (L-R) Match	Timing Fault Recognition
Output Maintenance Register Input Maintenance Register Error Status Register Address Error Register	Programmed Maintenance Access and Communication

looks for one high-level signal out of many low-level signals. In each case, a multidiode network connects the entire group to be monitored to the input of a detector. The diode networks for use in 1-hot applications are poled oppositely to those for use in the 1-cold applications. In this way, the same detector design may be used for both cases, and similar voltage levels may be used at the input to the detector to distinguish between normal and alarm conditions. Figure 15 shows a chart of the various input-voltage levels versus output-logic levels for the normal condition (1-hot) and the alarm conditions (no-hot, two or more hot). Conditions for the 1-cold case are also shown. The logic states of the detector outputs, A and B, are used to control the alarm logic. Normally quiescent, as long as a 1-hot (or 1-cold) condition prevails during a given time interval such as an address interval, the logic will set a cell in the error status register if an alarm state occurs. The output of the detector is strobed by a timing pulse to prevent false setting of cells during transitions between intervals. An input-voltage level within 6 to 12 volts dc is interpreted by the detector as normal, in either the 1-hot or 1-cold case, and the logic circuitry takes no action during the interval. The

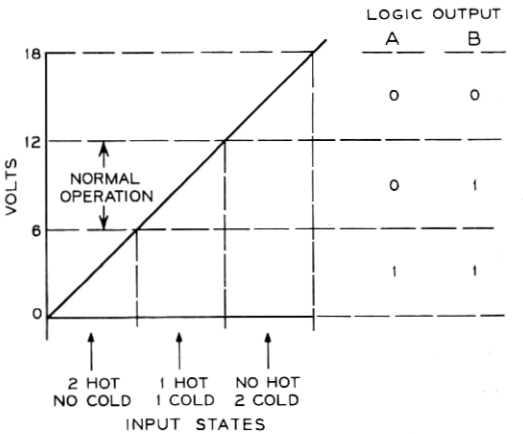


Fig. 15—Hi-Lo detector output states.

normal voltage level is established by the diode network as long as current is drawn through only one diode path in the network as a result of the 1-hot (or 1-cold) situation. However, should no diodes, or more than one diode, conduct current the voltage at the detector changes accordingly, and the output of the detector assumes one of the alarm states.

6.5 *Maintenance Registers*

Three of the major logic registers not described previously are used exclusively for maintenance and diagnostic purposes. Listed in Table IV are the three major maintenance registers which in turn accept maintenance instructions into the DSD, transfer data resulting from these instructions back to BC, and store status reports for transfer to BC.

The output maintenance register stores control write instructions and control group orders sent to it by BC over regular data bit positions of the send bus under the control mode of operation. Once stored in the output-maintenance register, the data is translated into an instruction or order which in conjunction with a match of the accompanying line address, and in some cases, a control unit count, performs operations as follows:

(*i*) Directs a parallel word readout from any one of several stages in the DSD input or output process including delay-line loops of the assembler/disassembler unit, recirculating-buffer unit, and control unit, and other registers and gates of importance

(*ii*) Sets or resets specified flip-flops for such purposes as bus configuration, divorce, disconnect, and maintenance detector tests.

Readout operations directed by the output-maintenance register store data in the input-maintenance register which then requires a control read to complete the transfer to BC. The data is stored in the input-maintenance register at the instant of the address match and if required, at the instant of the count match specified by the contents of the output-maintenance register. An address match occurs once every memory cycle (606.06 μs) but storage can be delayed for any multiple of memory cycles by requiring that a control-count match coincide with the address match. Thus, any point within the assembly or disassembly process can be examined to the closest integral memory cycle of any address.

The input-maintenance register stores data and address bits representing the answer to a control write instruction directed to the DSD by BC. One cell of this register records the fact that data has been gated into the input-maintenance register and is ready for transfer to BC. The output of the cell is monitored by a ferrod which operates to inform the system that the data is ready for interrogation and transfer to BC. A subsequent control-read mode is used to release the contents of the input-maintenance register to the receive bus. After the input-maintenance register has performed the readout to the receive bus, it is cleared by an acknowledge from BC.

The error-status register stores the trouble reports from maintenance circuits within the DSD unit. There are 22 specific cells in the error-status register. Each cell monitors a particular function at periodic intervals determined by timing pulses arising from the mode transmission or generated by the internal clock. When a failure is detected, the error-status cell associated with the circuit in trouble is set. Some, but not all, of the 22 cells inhibit the ASW for the associated unit so that the system will be informed quickly in case of trouble in the DSD; in the other cases, a slower method of reporting to the system exists in the form of a summary ferrod activated when any one of the 22 cells is set. The error-status register must be interrogated by a control read mode before it transfers its contents to BC via the receive bus. The error-status register is reset by CPD under normal circumstances although a maintenance-program reset is available for diagnostic purposes.

A fourth register, of considerable importance to diagnostics, the address-error register, is used to store the A and B bits from 1-hot

monitors and the address (6 bits) interval during which a 1-hot detector exhibits an alarm state. This register, which does not have a direct-access path to the bus system as do the other three buses, communicates via the input maintenance register.

VII. SUMMARY

A data-scanner distributor has been designed that achieves performance and low cost-per-line objectives. The extensive use of No. 1 ESS hardware resulted in a design with the reliability and maintainability consistent with No. 1 ESS.[4] The unit is designed for 512 low-speed FDX data subscriber line connections.

A very compact design was achieved by the use of ultrasonic delay lines in a highly time-shared fashion. The unit is fully duplicated utilizing 116 delay lines in the two units. By scanning every input bit many times under control of the high-speed time-shared counter, the DSD can accept highly distorted input data as well as transmit essentially distortionless data.

Maintenance circuitry allows detailed diagnosis of the DSD by CC programs. Also, the DSD possesses certain internal-check circuits providing the DSD the ability to divorce a faulty unit in case one of them fails these checks. This function is provided to prevent garbled subscriber messages when hardware failures occur.

VIII. ACKNOWLEDGMENTS

Many people contributed to the design and development of the data-scanner distributor. Mr. R. E. Swift contributed significantly to the fundamental system-design concepts. Messrs. E. J. Aridas and I. D. Leer made outstanding contributions in satisfying many of the difficult timing and logic-design objectives. Messrs. N. L. Davis and E. H. Young were responsible for the development of the delay-line memories. Mr. G. A. Van Dine was responsible for several circuit pack designs, and Mr. A. E. Leitert was responsible for the equipment design.

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