B.S.T.J. BRIEFS

A Self-Reorganizing Synchronization Network

By J. V. SCATTAGLIA

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This paper describes a method of increasing the reliability of synchronization in a network of remote clocks. A common synchronization technique embodies the master-slave relation where one particular clock is a reference for the others. The geometry of a typical network can be likened to a "tree" structure. The master clock transmits its signal, simultaneously, over several transmission links to synchronize slave oscillators at the ends. The slaves retransmit the reference signal to other slaves one link away. This process is iterated as the system expands. Each slave has only one input; hence, a network of this type can be disabled, in varying degree, by the failure of any clock or transmission link.

The probability of failure can be reduced by creating redundant paths between nodes in the network. These paths can consist of more than one link and include the intervening clocks. This allows bypassing of a disabled clock or reorganization of synchronization authority.

To implement such a system we need interrogation equipment at each clock station to decide which incoming path has the highest priority for a given situation. If the reorganization takes place automatically, we can refer to it as a "self-reorganizing synchronization network." Application of this scheme in a large "tree" network can become very complex.

A technique which provides orderly organization of complex networks was patented by G. P. Darwin and R. C. Prim (Patent No. 2,986,723). Their system, in its most general form, requires a three-part "signature" to be transmitted, along with the synchronizing signal, from each local clock.

The technique proposed here simplifies the system controls by constraining network geometry to advantageous geometrical patterns. These patterns are subject to predetermined reorganizational rules. The advantages offered are: (*i*) simpler interrogation equipment; (*ii*) adaptability to multilevel systems, i.e., subgroup, supergroup, regional, local, etc.; (*iii*) more predictable reliability; (*iv*) large networks can be designed in orderly blocks.

The specific geometrical network to be described here will be referred to as the "wheel."

Wheel Network. Fig. 1(a) illustrates a wheel configuration, e.g., a regional network. Clock M, the primary master of the wheel, would be the regional master. Peripheral units A to F are secondary or local clocks. M is likely to have more stringent requirements than A to F; hence it has only outgoing paths. A to F are identical clocks and neighbors are connected by two-way paths.

M can be connected by two-way paths to adjacent regional masters to become a peripheral clock in a larger wheel.

The set of numbers at each input to a clock denotes alternate priority values of that path. The existing value is a reflection of the transmitting clock's source of synchronization. A description indicating the input-output relations for all conditions is too lengthy for this short paper.

Examples of path structures for several conditions are illustrated in Figs. 1(b) to 1(e). The presiding master clocks and each path's priority value are indicated. Clock A has first preference in becoming master of

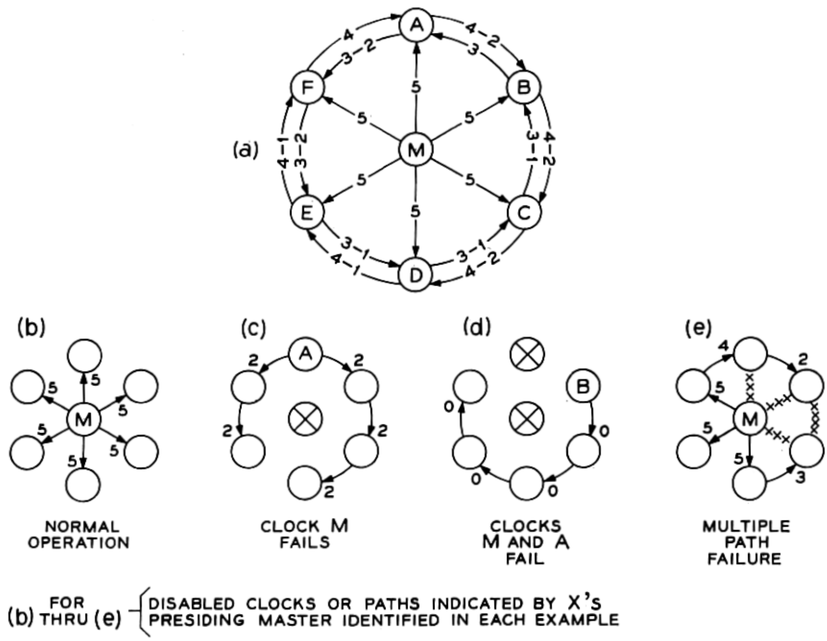

Fig. 1 — Self-reorganizing wheel network. In parts (b) through (e), the disabled clocks or paths are indicated by x's; the presiding master is indicated in each example.

the peripheral clocks upon failure of the primary master. A discontinuity in the priority ratings of signals "passing through" A prevents "closed loop" conditions in the periphery that could otherwise occur on failure of the primary master.

Interrogation Circuitry. This network is very simple to implement because there is a maximum of only two "modes" to be identified at any input. The essentials for a typical station, clock "C" for example, are shown in Fig. 2. The illustration assumes a dc transmission path. The presence of a signal on a path is indicated by a dc bias added to the synchronization signal at the transmitter. At the receiver the dc operates a particular relay. The two modes of a peripheral input are indicated by a positive or negative bias. If the primary master input is active, relay switch (RS) #5 closes contact 5A. The master synchronization signal is thus directed to the local clock's comparator. Contact 5A simultaneously disconnects all other inputs from the comparator. The remaining function of relay #5 is to close contacts 5B and 5C which will add the appropriate dc bias to the outgoing signals. If now the master input is absent, the priority chain looks for the next highest input

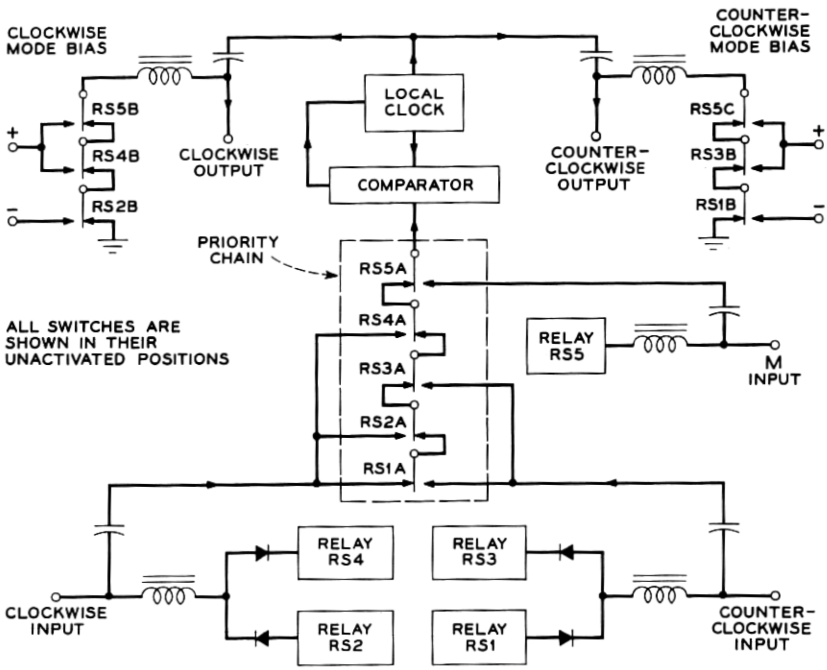

Fig. 2 — Clock station "C."

present. The clockwise rule to cover the situation shown in Fig. 1(d) is implemented by connecting the clockwise ac input to the unactivated contact on 1A. If none of the inputs is present, the local clock free runs but can still synchronize its clockwise neighbor.

Description of a dc system was for simplicity of illustration. Other indications of priority could be employed: e.g., tone modulation with tuned reed relays for ac analog systems and simple codes for digital systems.

Point-Contact Wafer Diodes for Use in the 90- to 140-Kilomegacycle Frequency Range

By W. M. SHARPLESS

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In millimeter wave systems, one of the most important components is the first converter or mixer. This brief paper describes a recently developed point-contact diode of the wafer type which operates efficiently as a first converter in the frequency range 90 to 140 kilomegacycles (F-band).

Fig. 1 is a photograph of the wafer diode and its holder. The assembly is quite similar in appearance to the diode-holder combination designed for the 45- to 75-kmc range.[1] The tuning procedure is also the same. The wafer is inserted in the holder and moved transversely to the waveguide, thereby adjusting the location of the point-contact relative to the guide to effect a resistive match. (The pin at the left of the wafer slides in a chuck on the inner conductor of the coaxial low-frequency output circuit.) The wafer is then locked in position by means of the knurled clamping knob, and the reactance of the diode is tuned out with the waveguide piston at the rear of the holder.

The present design differs from the older one in the use of smaller waveguide (RG 138/u instead of RG 98/u) and, most importantly, in the addition of the milled slots on either side of the wafer which encompass the rectangular window containing the point-contact diode. When the wafer is inserted in the holder, these slots engage small guiding shoes which automatically align the window of the wafer with the waveguide sections in the holder to better than 0.0005 inch; this accuracy is essential at the extremely high frequency of operation. The method of forming

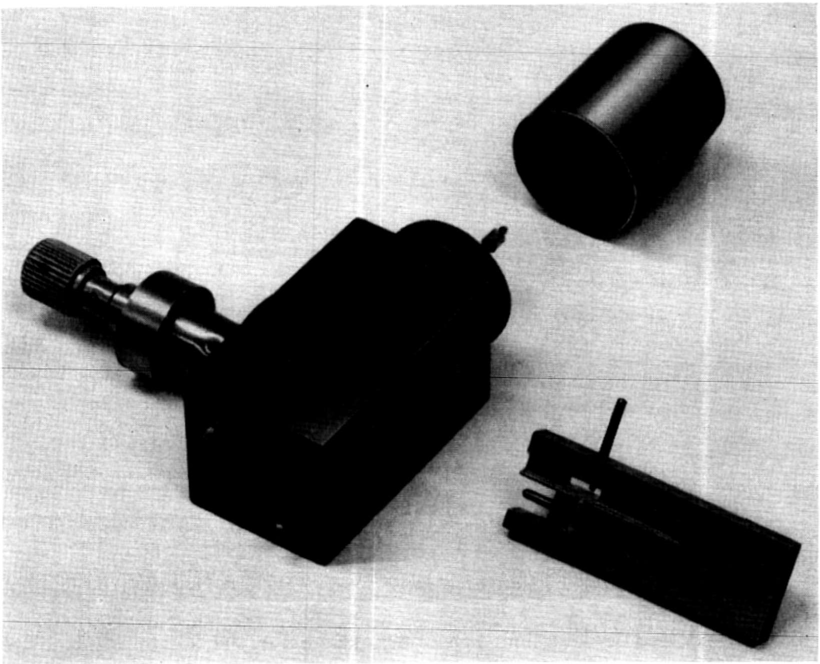

Fig. 1 — Millimeter-wave point-contact wafer diode and holder for use in the 90- to 140-kmc frequency band.

the rectifying junction is also different in the present design. The older units used boron-doped silicon which required that the units be "tapped" into adjustment. The present units use aluminum-doped silicon and do not require tapping. For very high frequency operation, tapping should be avoided if possible since it tends to increase the point-contact area.

The apparatus used to evaluate the diodes is shown in Fig. 2. It constitutes a complete double-detection measuring system. Many of the millimeter wave components shown had to be developed in order to measure the conversion loss of the diodes.

The conversion losses of several types of diodes mounted in the new wafer units are listed in Table I. The measurement consisted of determining the ratio of the millimeter-wave power input to the converter, measured by a calorimeter,[2] to the 60-mc output power measured by comparison with a known signal level obtained from a calibrated signal generator. The conversion loss quoted includes the heat losses of the waveguide input circuits of the diode as well as the losses associated with the output circuitry. The diodes were matched at 115 kmc, were

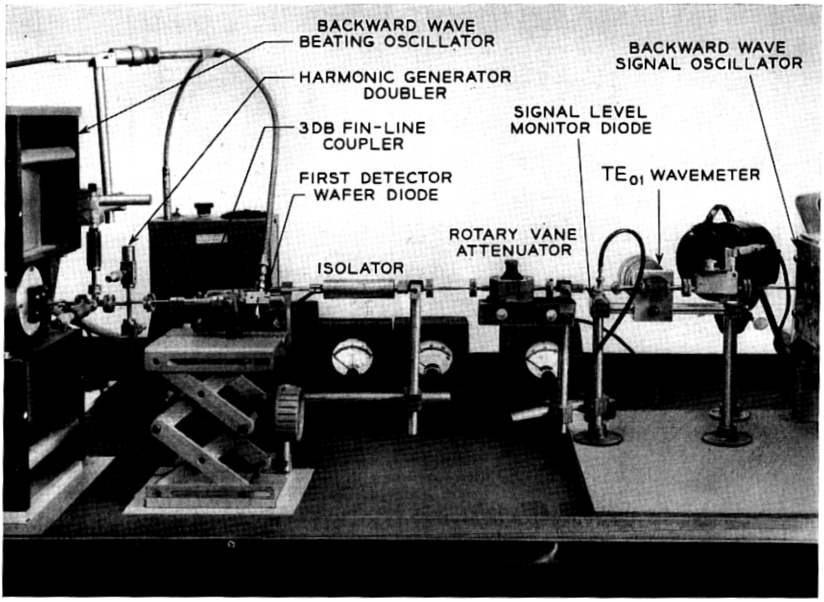

Fig. 2 — A double-detection measuring system for the 90- to 140-kmc frequency band.

optimumly biased, and were driven with 0.6 milliwatt of local oscillator power.

If one assumes a 12-db diode with a noise output ratio, N_R, of 2, which is 30 per cent above the value measured at 55 kmc for similar units, it may be calculated that a balanced converter followed by an IF amplifier with a 4-db noise figure will yield an over-all receiver noise figure of 18 db at 115 kmc. Noise figures very near this value were obtained in practice.

The important contributions of Messrs. E. F. Elbert and S. E. Reed are gratefully acknowledged.

Table I — Conversion Losses

Type of Diode	115-kmc Conversion Loss in db
Average silicon diode (25 units)	12.4
Best silicon diode	11.1
Best gallium arsenide diode	9.9
Best germanium backward diode[3]	11.5

REFERENCES

1. Sharpless, W. M., Wafer-Type Millimeter-Wave Rectifiers, B.S.T.J., **35**, November, 1956, pp. 1385–1402.
2. Sharpless, W. M., A Calorimeter For Power Measurements at Millimeter Wavelengths, IRE Trans. Microwave Theory and Techniques, MTT-**2**, September, 1954, pp. 45–47.
3. Burrus, C. A., Backward Diodes for Low Level Millimeter-Wave Detection, IEEE Trans. Microwave Theory and Techniques, MTT-**11**, September, 1963.