Proceedings of the First Annual *WIRELESS* Symposium

JANUARY 12-15, 1993
SAN JOSE CONVENTION CENTER, SAN JOSE, CA

Sponsored by
Microwaves & RF and **Electronic Design** Magazines

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Technical Proceedings of the First WIRELESS Symposium and Exhibition

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Advanced Materials for Wireless Applications

Session Chairperson: Robert Deitz,
Microwave Printed Circuitry (Lowell, MA)

REVIEW OF FABRICATION TECHNOLOGY FOR ADVANCED MATERIALS

ROBERT DEITZ
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LOWELL, MA

1. MATERIALS FOR HIGH FREQUENCY USES

A. Frequency ranges 500 MHz - above 20 GHz
B. Dielectric constant control
C. Low loss tangent
D. Uniform properties
E. Comparison to standard PCB materials

2. ARTWORK PREPARATION

A. Rubylith - cut and peel method, accurate but more expensive these days.
B. Hand taping not recommended for microwave applications due to rough edges and tape overlaps.
C. 1:1 film - prepared by either a reduction of rubylith or from photoplot.
D. Film or Glass - Must use stable polyester based film. OK for short runs, but for long term stability should be put onto glass. Use as a master.
E. Laser plotting - fast and reasonably inexpensive. Plotter should have at least a ¼ mil pixel size. Must examine corners carefully, no stairstep around the radius.
F. Etch compensation - needs to be added to compensate for etch factor. Can be added by micro-modification, or when plotting or cutting the master. Typically will use a ¼ mil per side for ½ oz. copper and a ½ mil per side for 1 oz. copper. This would be for straight print and etch. For plated through boards little or no compensation is needed due to the plating used as an etch resist.

3. IMAGING

A. Two types of resist available - dry film photoresist and wet, dip coated photoresist. Method of application is different for each resist.
B. Dry film photoresist is used for plated-through hole boards, or when plating from an alkaline plating bath.
C. Wet film photoresists are used primarily for print and etch processes or when plating certain acid plating baths.
D. Due to the thinner coating of the wet film resist, it has better resolution capabilities than the dry film resists. With wet resists it is possible to etch a 2 mil line or space on ½ oz. copper which would be difficult with dry film resists.

4. ETCHING

A. High frequencies require close control of line widths which in turn requires close tolerances. Standard tolerances for print and etch are +/- ½ mil on 1 oz. copper and +/- 1 mil on 1 oz. copper. For parts with plated through holes the tolerances are +/- 1 mil for ½ oz. copper and +/- 1.5 mils for 1 oz. copper.
B. The geometry of the etched line is important in that the design equations depict ideally a rectangular line where in reality the line is more trapezoidal shaped. The closer the line is held to the rectangular shape, the more closely the design parameters will be met. The importance in etching is not just the complete removal of the copper in the unwanted areas, but to do this while maintaining a good line geometry. This requires very close control of the etching and process parameters.
C. With circuits used at microwave frequencies, the finished line width is always measured at the base of the line, not at the top surface. If the etching is properly done this should represent the true line width.
D. Due to the dimensional stability of various materials it is necessary to use additional processes to control the movement of the substrate. During etching, the materials, particularly thinner substrates, will change dimensionally. This change causes problems when trying to maintain accurate positioning of the circuits, especially with bonded striplines. A double etching technique can be used to minimize this change. This involves a two step etching process. The first etch is with an oversize artwork to remove the bulk of the copper to be etched. This is followed by a heat cycle to further stabilize the material. The final circuit pattern is then etched. This process will generally stabilize most materials and prevent further movement.

5. PLATING

A. Drilling and machining parameters have a direct effect on the plating of the PTFE based materials. Different speeds and feed rates must be used than are used for epoxy based materials. Due to the variety of materials, woven, non-woven, and ceramic filled, the parameters need to be adjusted for each of the materials. It is best to determine empirically the best parameters for your companies equipment and processes.

The main thing object is to obtain good clean holes with no smear. PTFE smear cannot be removed by chemical means and will affect the reliability of the through hole plating.

B. Because PTFE resins are non-wettable special treatments must be utilized to make the surface wettable in order to accept plating deposition. This is generally done using a form of sodium etchant. These etchants are available commercially. Any PTFE surface exposed to the sodium etch will be made wettable and therefore plateable.

C. Once the surface has been properly treated it is possible to use any of the standard PWB processes such as plated through holes or plated edges. The holes can be plated to meet the requirements of Mil-P-55110. Wrap around plating of the edges to establish good grounds is also feasible. Most of the plated holes and edges are used to establish ground connections.

D. Plating finishes available are: copper, tin/lead, tin, electroless copper, electroless nickel, and gold. New processes have been developed for plated through holes on aluminum backed materials. (Heavy metal backed) With these processes it is possible to plate any of the above metals on aluminum.

6. BONDED SUBSTRATES

A. Differences between microstrip and stripline

B. Bonding films available - 6700, Polyguide, FEP, Pyralux, conductive films (SRS and Ablestik)

C. Preparation prior to bonding - sodium etch or bond without, direct fusion bonding

D. Special bonding applications - conductive bonding to aluminum, curved (conformal) bonding

7. SUMMARY

As frequencies increase and control of electrical parameters become more important the use of PTFE based materials will grow due to the excellent electrical properties. It will become necessary to be able to process these materials and hold the tolerances required.

Copper-Foil-Clad Laminates and Substates for Commercial Applications

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Applications for PTFE based laminates continue to grow in number. As a material supplier in a more competitive market, Arlon is challenged in both the manufacture of existing products and the development of innovative products to satisfy today's and tomorrow's designs.

Woven fiberglass reinforced PTFE and nonwoven fiberglass reinforced PTFE are most widely available. The market for these PTFE based substrates has traditionally been military microwave applications, where the electrical performance of the laminate is absolutely critical. Some of the technology from the military applications has been adapted to applications for commercial and consumer products. This growth has allowed PTFE laminate manufacturers certain economies of scale, making the laminates and their encompassing technology available outside the military.

With the introduction of various ceramic fillers into the PTFE matrix, several new avenues are opened to designers in different fields. Grades are available which allow a choice of circuit miniaturization, temperature stable electrical performance or pricing comparable to high performance thermoset laminates.

The first two of the ceramic loaded PTFE laminates are high performance (and high cost) materials, with requirements as stringent as those for the mature technology of "conventional" PTFE based laminates. The third, which was most recently developed, has been introduced for applications extending from high speed digital to commercial microwave devices.

Early evolution of the PTFE based laminate was lead by the need for better performance at the available (higher) frequencies. Designs called for lower dielectric constants and lower dissipation factors. Low dielectric constants allow faster signal propagation in traditional wiring board applications.

Printed wiring boards were replaced by printed circuit boards, where the length of a circuit element was based on the wavelength at that frequency. As the frequencies increased, the traces on the PTFE based substrates were, indeed, transmission lines. The low dissipation factor (loss tangent) would yield higher signal to noise ratios for these transmission lines.

Using a conventional epoxy/fiberglass laminate, the electrical package designer is required to route all of the wiring traces such that all of the discreetly mounted components are included in the scheme. The only requirement for the epoxy/fiberglass laminates is that they are electrical insulators.

In applications which would use the PTFE laminate, tighter tolerances are required for both dielectric constant and thickness. Here, the laminates, were not going to be used as ordinary printed wiring boards; they would be used as components themselves. Increasing performance requirements has provided the impetus for the manufacture of "conventional" PTFE based laminates to "component" standards.

Components which can be integrated into the circuitry would not have to be mounted discreetly upon the substrate. This capability of PTFE based laminates reduces the system cost and improves reliability.

Several types of PTFE based laminates are available to the designer for commercial signal processing components. The fundamental groupings include woven fiberglass reinforced PTFE, nonwoven fiberglass reinforced PTFE and ceramic loaded PTFE. In short, a complete product range is available for engineers to optimize their designs on PTFE based laminates.

Woven Fiberglass Reinforced PTFE:

The most common PTFE based laminates are woven fiberglass reinforced. These have been produced since the early 1950's. The first laminates of this type generally had a dielectric constant of about 2.7 to 2.8, relatively low compared to a typical laminate of epoxy/fiberglass ($\epsilon_r = 4.6$). Today, the company names have changed, but the product lines DiClad® (from Continental Diamond Fiber) and CuClad® (from 3M) are now manufactured by Arlon's Microwave Materials Division.

In addition to the electrical applications, many of the early PTFE laminates were also used in mechanical or chemical applications. Bearing pads for shifting loads and chemically inert gaskets were common uses for reinforced PTFE. These applications did not use copper foil.

With copper foil laminated to each side, the woven fiberglass/PTFE provided several advantages over its epoxy counterparts. The low dielectric constant allowed much faster propagation of signal in circuits where speed was essential. In addition, the dissipation factor was an order of magnitude lower, even as tested at 1 megahertz (MHz). More signal would be carried faster with less electrical loss.

Control of the PTFE resin coating of the fiberglass cloth is unmatched by epoxy/fiberglass laminators. The coating weight is controlled to well within one percent. This allows PTFE laminators to achieve the tight mechanical (thickness) and electrical (dielectric constant) tolerances which are necessary in the application of these substrates.

Woven fiberglass/PTFE remains the most proliferate among the varieties of PTFE based laminates. But, even within this general category, there are several distinctions to be made, each with its own advantages.

Among the first distinctions between laminate grades is that made on the basis of dielectric constant. By itself, PTFE has a dielectric constant of 2.07; electrical grade fiberglass has a dielectric constant of 6.0. The dielectric constant of the composite laminate is a function of the PTFE resin to fiberglass weight ratio. This ratio is manipulated to achieve laminates with dielectric constants ranging from 2.15 to 2.70; laminate base thicknesses range from as little as 0.002" (0.05 mm) or greater than 1 inch (25 mm).

The military specification document MIL-P-13949 recognizes type GT as having a dielectric constant up to 2.8; GX laminates have a dielectric constant between 2.40 and 2.60, inclusive. In chosing between type GT and GX for an application, they are typically differentiated by the test method, amount of testing and acceptable tolerances.

GT material is tested for dielectric constant and dissipation factor at 1 MHz by a two fluid capacitance cell (well below microwave frequencies). The tolerance for the dielectric constant is ± 0.05 or about a four percent range. Dissipation factor for GT grade laminates is about 0.001 by the same test. This compares to a dissipation factor of 0.02 for epoxy/fiberglass at the same frequency.

GX grade, on the other hand, while it is essentially the same material, is tested for dielectric constant and dissipation factor at 10 gigahertz (GHz), well in the scope of microwave frequency. The standard tolerance for the dielectric constant is ± 0.04, 20 percent tighter than the tolerance for GT grade. The dissipation factor is also tested at X - band. The maximum allowable value is 0.0023. Typical values are about 0.0020.

GY grade materials have a dielectric constant between 2.15 and 2.40. They are tested by the same method as is used for the GX grade. Here, the dielectric constant tolerance is still ± 0.04, but typical is ± 0.02. This grade had typically been reserved for applications where the loss factor was most critical. Thus, the maximum allowable dissipation factor is 0.0015.

As each of these grades is a combination of PTFE and fiberglass, the electrical and mechanical properties of the laminate are related. The first important compromise is between the inherently better dimensional stability of the higher dielectric constant (ϵ_r = 2.4 to 2.6) laminates versus the superior electrical loss factor of the lower dielectric constant laminates (ϵ_r less than 2.4).

GT and GX grades, with their additional fiberglass, have much better dimensional stability during processing than a GY grade laminate. These grades resist etch shrinkage and are more easily handled by equipment set for conventional laminates.

GY grade laminates tend to shrink more when the copper is etched. This may cause relative difficulty in achieving precise circuit patterns or control over relative position of machined features.

However, a typical GX laminate, with a dielectric constant of 2.50, has a loss tangent of about 0.002, while a GY laminate with a dielectric constant of 2.20 has a loss tangent of 0.0009. The additional fiberglass in the GT and GX grades, which is beneficial during fabrication, results in an electrical penalty, in that they have considerably higher loss tangents.

Another consideration is the relative cost of the different laminates. The two constituents in each of these types of laminates is PTFE and fiberglass. Fiberglass cloth is relatively inexpensive when compared to PTFE. Naturally, a GX grade laminate with a dielectric constant of 2.60 and composed of 65% PTFE, can be expected to be much less expensive than the GY grade with an dielectric constant of 2.20, which has approximately 91% PTFE.

However, there are several compromises made with regard to the laminate properties. A leading commercial application of woven fiberglass reinforced PTFE is for Low Noise Amplifier (LNA) circuits for 12 GHz Direct Broadcast Satellite (DBS) receivers. Some designs use GY grade (ϵ_r = 2.20), while other designs use a GT or GX grade (ϵ_r = 2.60).

In either design, the noise factor of the LNA is a measure of its performance. Each design uses

several field effect transistors to amplify the incoming signal. The quality of these components, which are mounted to each substrate, are as important to the noise factor as the substrate. The field effect transistor, another significant cost item, along with choice of PTFE substrate, creates another cost versus performance trade. The designer is left to complete the exercise.

Woven Fiberglass Reinforced PTFE:
Crossplied or Non-Crossplied

Compared to its epoxy/fiberglass counterpart, the range of dielectric constant within a PTFE based laminate is minimal. Some of this range owes to the directionally dependent properties of the fiberglass cloth. Dielectric constant is measured in the z direction of the laminate (that is, through its thickness). However, it is measured with respect to the x and y axes (or machine and cross-machine directions). Testing laminates for this difference shows a directional shift of about 0.010 to 0.015 depending on the amount and style of fiberglass cloth in the laminate.

Apart from the nominal dielectric constant, there is another distinction within the class of woven fiberglass/PTFE laminates. To eliminate any property changes owing to directional orientation, laminates within the CuClad® product line are manufactured with crossplied fiberglass. Alternating layers of PTFE coated fiberglass are oriented at 0° and 90° as the substrate is pre-constructed prior to lamination. This technique provides a finished substrate with isotropy of both electrical and mechanical properties with respect to the machine and cross-machine directions.

Many designers of antennas for various applications have chosen CuClad® for its electrical isotropy. The electrical length of the elements of the antenna are critical to its performance. The small change in dielectric constant associated with a directional change in a non-crossplied laminate is enough to compromise that performance.

This contrasts the manufacture of DiClad® laminates, which are not crossplied. They are, however, offered in much larger sheet sizes. DiClad® laminates are offered in a maximum sheet size of 36" x 72", while the crossplied CuClad® laminates have a maximum dimension of only 36" x 36".

Without isotropy, the electrical designer may be required to adjust lengths of electrical elements to account for dielectric constant shift depending on the element's orientation to the fiberglass weave. Elements oriented along the warp direction typically behave as if they are on lower dielectric constant material. Alternatively, the circuit or system can be designed to tolerate a larger bandwidth, but some electrical performance will be sacrificed.

To accomplish the design goal, adjusting circuit element lengths to account for the directional change in dielectric constant, the effort must be coordinated with the fabricator and the supplier of the PTFE laminate material. Both parties must track the orientation of the laminated sheet and any smaller panels cut therefrom. This practice is done regularly, but designs using CuClad ® have been able to circumvent it.

The crossplied laminate obviates these considerations. Neither the laminate vendor nor the fabricator need track the orientation of panels prior to and during circuit fabrication. The engineer designs the circuit elements according to the reported nominal dielectric constant. Regardless of circuit orientation on a given panel, the performance should be equivalent.

As mentioned earlier, a disadvantage of the crossplied construction is that it limits the sheet size to a longest dimension equal to the width of the fiberglass cloth. For some applications, the circuit will be longer than a crossplied laminate; the longer dimension is absolutely critical.

Antennas for Personal Communications Networks (PCN) are just such an application. In other cases, the preferred panel size for fabrication can be cut more favorably from a rectangular sheet than it can from a square sheet.

Nonwoven Fiberglass Reinforced PTFE:

Historically, nonwoven fiberglass reinforced PTFE were the next class of PTFE laminates to be developed. They are available in a similar range of dielectric constants as their woven fiberglass counterparts. The exception is that ceramic filler can be more readily introduced into the nonwoven composite, allowing higher dielectric constants to be achieved. Discreet values of 2.17, 2.20 and 2.33 are standard products.

The military specification document MIL-P-13949 recognizes nonwoven fiberglass reinforced PTFE based laminates with dielectric constants between 2.15 and 2.40. The grade designations are types GP and GR. The test methods for these laminates are the same as those described earlier, in reference to type GT, GX and GY grades of woven fiberglass reinforced PTFE based laminates. Tolerances for the mechanical and electrical properties are the same as for the GY grade.

Similar to the crossplied woven fiberglass reinforced PTFE substrates, nonwoven fiberglass reinforcement offers relative isotropy in the x-y plane. The design and fabrication advantages owing to isotropy are described earlier.

Fabricators perceive a different benefit from the nonwoven fiberglass reinforcement. In machining, the cutting tool "sees" a uniform material. Woven reinforcement, in contrast, presents "hard" fiber bundles and a "soft" matrix. If proper machining parameters are not chosen for the woven fiberglass reinforced PTFE, the tool can tend to push the fiber bundles through the matrix rather than cut them. Fabricators often describe better quality holes and other machined features when they are using nonwoven fiberglass reinforced PTFE. Parameters such as RPM and feed rates may not be as critical.

Military applications of this material are numerous. Several missile programs use nonwoven fiberglass reinforced PTFE as the material for "wrap-around" antennas. These antennas are formed to the circumference of the missile.

Among commercial applications, nonwoven fiberglass reinforced PTFE is being used as the substrate material for switching circuitry in telecommunication equipment.

Ceramic Filled PTFE:

One of the advantages of PTFE as the resin system is the ability to achieve very low dielectric constants. In applications where the primary goal is high speed of signal propagation, this is especially important. Applications at microwave frequencies typically require the dissipation factor to be very low.

Mechanically, woven fiberglass and nonwoven fiberglass reinforced PTFE based laminates each have a high "z" axis thermal coefficient of expansion (TCE). The fiberglass reinforcement is oriented only in the x-y plane. Thus, with thermal expansion in the x-y plane restricted, the PTFE resin forces expansion in the "z" direction.

The choice of ceramic filler, in ceramic loaded PTFE, allows the low dissipation factor to be preserved. A choice of dielectric constants and desirable packaging, electrical, mechanical or

economical advantages are offered.

Fabricators realize some benefits of the uniformly mixed ceramic loaded PTFE based laminates when machining. Usually, a wide range of speed and feed parameters can yield a high quality hole surface. However, the hardness of the ceramic particles will shorten tool life, and the bits will have to be replaced more often.

Ceramic Filled PTFE:
High Dielectric Constant Laminates

Ceramic filled PTFE offers the property of a significantly higher dielectric constant than is available with either the woven or nonwoven fiberglass reinforced PTFE. The dielectric constant is higher than even epoxy/fiberglass. Arlon is offering dielectric constants of 6.0, 10.2, 10.5 and 10.8. These are the products IsoClad® GR6: $\epsilon_r = 6.0$; CuClad® Epsilam 10: $\epsilon_r = 10.2$; and DiClad® 810: $\epsilon_r = 10.2, 10.5, 10.8$.

At microwave frequencies, circuit trace lengths are specifically designed around the wavelength. At any particular frequency, the speed (C) of propagation of the signal is proportional to the speed of that signal propagating through a vacuum (C_0) divided by the square root of the dielectric constant ϵ_r:

$$C = C_0 * (1/\sqrt{\epsilon_r})$$

Signal speed is also equal to the frequency (ν) multiplied by the wavelength (λ).

$$C = \nu * \lambda$$

As signal propagates through a dielectric material, the frequency of the signal does not change, but the speed of propagation, which is proportional to the inverse of the square root of the dielectric constant of the material, does. It necessarily follows that, at a particular frequency, only the wavelength can change with respect to the dielectric constant of the material through which it is propagating:

$$\nu * \lambda = C_0 * (1/\sqrt{\epsilon_r})$$

Since ν and C_0 are constants, they can be eliminated for the purpose of this discussion. Thus, the wavelength, like the speed, is inversely proportional to the dielectric constant of the material:

$$\lambda \propto (1/\sqrt{\epsilon_r})$$

What this means to the designer is that, using a high dielectric constant substrate, the circuit board can be miniaturized. In comparison, a board which had been designed on $\epsilon_r = 2.20$ material could be redesigned on $\epsilon_r = 10.2$ material, resulting in a circuit much less than half the length.

Holding dielectric thicknesses constant, a substrate with a dielectric constant of 10.2 also reduces the width of a constant impedance line considerably. For instance, the width of 50 Ω line, on material which is 0.025" thick, is reduced by more than a factor of three. This fact is often exploited for very low impedance lines, such as those which connect power amplifiers.

Accordingly, with both the length *and* width of the substrate reduced, the package weight is also significantly decreased. This type of substrate is used where weight and/or space are at a premium.

An important use of high dielectric constant material is for commercial aircraft. The United States Federal Aviation Administration has mandated collision avoidance systems for passenger aircraft. Engineers at Rockwell International designed the front end of the transmit/receive module of their Tactical Collision Avoidance System (TCAS II) on DiClad 810. The space and weight savings for TCAS II, an *airborne* collision avoidance system, are obvious benefits.

Another difference owing to the ceramic filler is higher thermal conductivity in comparison to other PTFE based laminates. Designers can take advantage of both miniaturization, more easily matching feed lines to low impedance power transistors, and high thermal conductivity, sinking the heat generated from a power transistor, for instance, to an integral ground plane. Westinghouse Electronics uses DiClad 810 extensively as the substrate for radar power amplifiers.

High cost is associated with high dielectric constant substrates. The manufacture of this type of substrate costs considerably more than the manufacture of conventional PTFE/fiberglass laminates. The designer will also have somewhat greater electrical loss. These cost and performance considerations limit but, as evidenced by TCAS II, do not preclude high dielectric constant substrates from the commercial market.

An important consideration for the fabricator and the designer is the fabricator's etch tolerance. This is dependent on the cladding thickness and the individual ability of the fabricator. At microwave frequencies circuit lengths and widths are critical to performance. Because the circuit dimensions on high dielectric constant substrates are less than half that on low dielectric constant substrates, the relative magnitude of the etch tolerance is more than twice.

Ceramic filled PTFE substrates are also offered with a dielectric constant of 6.0. This compromise allows some miniaturization while mitigating the negative effects of etch tolerance on the consistency of circuit performance.

Ceramic Filled PTFE:
Thermally Stable PTFE Based Laminates

The aforementioned types of ceramic filled PTFE products have been on the market for up to 20 years for the newest (ceramic filled PTFE - high dielectric constant) and 40 years for the oldest (woven fiberglass/PTFE). Among the newest PTFE based laminates are those formulated to offer superior thermal stability with regard to mechanical *and* electrical properties.

The dielectric constant of IsoClad® LTE is nominally 2.94. This is somewhat higher than the PTFE/glass laminates, but it is still lower than most thermoset based laminates. More importantly, the dissipation factor at 10 GHz is about as low as a PTFE/glass laminate with a dielectric constant of 2.33 (about 0.0013).

Previously, the electrical designer would be required to make considerations for dielectric constant change with temperature. The types of laminates discussed previously are all relatively stable with temperature in comparison to epoxy/fiberglass and most other combinations including a thermoset resin. But compared to IsoClad® LTE, the contrast to "conventional" PTFE based laminates is as striking as the comparison of the "conventional" PTFE based laminates to epoxy/fiberglass.

Both fiberglass reinforced PTFE and high dielectric constant ceramic filled PTFE have a temperature coefficient of dielectric constant ($TC\epsilon_r$) which is on the order of a few hundred parts per million per degree centigrade. The coefficient is negative; ϵ_r decreases with increasing temperature.

In contrast, the new product has a $TC\epsilon_r$ which is on the order of 30 parts per million at its highest absolute value. At temperatures below 20°C the coefficient is negative, while it is positive above that temperature.

To the designer, the near zero $TC\epsilon_r$ of IsoClad® LTE can simplify the entire system. On conventional PTFE based laminates, given a physical length for a circuit element, its electrical length changes as the dielectric constant of the substrate changes with temperature. At a fixed frequency, the circuit will become less well matched to the wavelength. IsoClad® LTE assures, through its low $TC\epsilon_r$, that the performance of the circuit remains constant as the ambient temperature changes.

The combination of raw materials which gives this substrate a low $TC\epsilon_r$, also yields greater mechanical stability. This mechanical stability is manifest in its low thermal coefficient of expansion (TCE). The TCE of IsoClad LTE is just 25 parts per million per degree centigrade (ppm/°C). High dielectric constant ceramic filled PTFE based laminates also enjoy a low TCE (as low as 35 ppm/°C), just without the electrical stability (low $TC\epsilon_r$).

Plated through hole reliability for IsoClad LTE is especially enhanced by the low TCE. In "conventional" PTFE/fiberglass laminates these electrical connections are often suspect. Woven and nonwoven fiberglass reinforced PTFE based laminates, especially those having the least amount of fiberglass, have up to 10 times the TCE of copper. The TCE of IsoClad LTE nearly matches that of copper (the TCE of copper used for plating through holes is 18ppm/°C), imposing little stress on that metallization through thermal cycling.

Thermal stability is manifest in both electrical and mechanical properties. Together these properties represent extraordinary reliability. Applications such as satellite communications,

where maintenance and field repair are inconvenient, enjoy these benefits.

Ceramic Filled PTFE:
Commercial Grade Laminates

Another class of new laminates is designed to offer dielectric constants similar to some thermoset laminates. Nominal dielectric constants are 3.50 and 4.50, each with a tolerance of $\pm$ 0.15, but dissipation factors for these laminates are still similar to those of the GT and GX grades of PTFE/fiberglass.

Using coating technology from the PTFE/glass laminates, AR350L and AR450L will have much better dielectric constant uniformity, both within a sheet and between sheets, than thermoset based laminates of similar dielectric constants. To the designer, this uniformity and the aforementioned low dissipation factor allow much better impedance control and a higher signal to noise ratio.

Thermoplastic pre-pregs developed for use with AR350L and AR450L have several advantages over their thermoset based counterparts. Electrically, these "pre-pregs" AR350Pand AR450P will match the performance of the laminate material for dielectric constant and dissipation factor. For the fabricator, throughput for multilayer lamination will increase dramatically.

Specifically, multilayer lamination throughput benefits significantly through the use of thermoplastic pre-pregs. Typical thermoset lamination uses longer, more complicated temperature cycles for proper cure and often requires post cure operations. Thermoplastic pre-pregs require only that a temperature high enough and a time long enough for sufficient melt be realized. Melt flow will allow the thermoplastic to wet all the surfaces to which it will bond.

A thermoplastic adhesive achieves bond as it is cooled to below its melt point. The rate at which its cooled is insignificant to measured electrical and mechanical properties. No elaborate (and long) cure cycle is necessary. Time for multilayer lamination cycles can be reduced by as much as a factor of five.

If the designer or the fabricator prefers, conventional pre-pregs can also be used to manufacture multilayer circuits with the AR350L and AR450L laminates. They can either be used instead of the AR350P and AR450P pre-pregs or following one in sequential lamination. Circuits using only the FR-4 pre-preg have been manufactured by prototype fabricators.

Designers anticipate that this combination of materials will sacrifice some electrical performance relative to using the new materials with the pre-pregs which have been developed specifically for this application. Notwithstanding, the benefits of this new grade will demand attention.

Considerations for machining are reportedly few. However, it is imperative that holes which will be plated through do not have smeared PTFE on their walls. Accounts are that the new material is "forgiving" compared to conventional woven fiberglass or nonwoven fiberglass reinforced PTFE.

These new laminates and pre-pregs are expected to cost more than epoxy/fiberglass laminates and pre-pregs. Pricing should be competitive with high performance thermoset resins such as Bismaleimide Triazine (BT). However, much of the cost will be returned through greater fabrication throughput and reduced fabrication costs.

With superior electrical performance, it can be expected that this will allow use of AR350L and AR450L in applications where electrical performance considerations would prohibit the use of

conventional epoxy/fiberglass and many other high performance thermosets. Critical impedance matching, in higher frequency computer back planes, for instance, is expected to be an important application for this product.

Although PTFE based laminates have been in existence for much of the time that more common epoxy/fiberglass laminates have been used, they have typically been reserved for high frequency, high performance applications. The technology that used frequencies which warrant the use of PTFE based laminates were commonly in the military or research fields.

However, as more communication, data and other information is carried without wires, many of the available frequency bands for traditional transmission equipment are occupied or otherwise previously allotted. The occupied, "traditional" frequency bands seldom exceed 1 GHz.

The available frequency bands are at microwave frequencies. PTFE based laminates are designed for consistent high electrical performance at these frequencies. Specifically, PTFE has a low dissipation factor and a degree of dielectric constant control not found in the conventional thermoset based laminates. These properties are the basis on which the commercial high frequency applications will rely on and be manufacturable with PTFE based laminates.

From Antenna to DSP: Components for RF/IF Signal-Processing

Session Chairperson: Ian Bruce,
Analog Devices (Norwood, MA)

**Paper presented by Bob Clarke.*
***Revised paper to appear in Microwaves & RF, July 1993.*

Delivered by Bob Clarke at *Wireless Symposium* , San Jose, CA on January 12 1993

Analog Signal Processing: Mixers and AGC Amplifiers

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Overview

The invention of the superheterodyne receiver, more than sixty years ago[1], marked a major step forward in radio receiver design. It addressed basic problems associated with the then-prevalent "tuned-radio-frequency" (TRF) receiver, the most difficult of which was that of maintaining tight matching of the frequency response of many selective circuits, all operating at some *variable* frequency, as these were tuned over their full range.

The pivotal concept was to translate a selected incoming signal to a *fixed* "intermediate" frequency (IF), in order that the tuned circuits providing the all-important selectivity between closely-spaced carriers could now operate at this one optimal frequency, and be tailored to achieve very exact bandpass characteristics. For certain applications, such as the reception of code using a pulsed carrier with little sideband energy[2] it was for the first time possible to use very narrow-bandwidth "crystal filters" based on quartz resonators.

The key components which made the superheterodyne possible were, first, a ***mixer***, which converted the incoming RF to the (usually, though not universally) lower IF, by multiplying it by a *variable* frequency from the second key element, a ***local oscillator*** (LO), such that

$$\underset{\text{(Fixed)}}{f_{IF}} = \underset{\text{(Some range)}}{f_{RF}} - \underset{\text{(Variable)}}{f_{LO}}$$

The characteristics of the mixer (chiefly, its intermodulation distortion and noise floor) and the local oscillator (its long- and short-term frequency stability) dominated the overall performance, as remains true today. This is because these critical components

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1 Armstrong, Edwin R., "The Super-Heterodyne: Its Origin, Development, and Some Recent Improvements." Proceedings of the I.R.E., vol. 12, no. 5 (October, 1924)

2 Somewhat misleadingingly called "continuous-wave", or CW, transmission.

must operate in the more difficult raw-RF domain, where little selectivity is available, and thus intermodulation between several incoming signals is more likely.

Later, as operation at higher RF frequencies grew in importance, a second advantage of the superheterodyne became apparent, namely, that high gain could be achieved more readily at a lower intermediate frequency (commonly, 455kHz, more recently, 10.7MHz). Further, to cope with a very large dynamic range of the received signal, automatic gain control (AGC) was incorporated into the multi-stage IF amplifier. More sophisticated receivers also used automatic frequency control (AFC) to cope with residual frequency drift in the LO, a practice largely eliminated by the availability of very accurate frequency-locked oscillators, nowadays using digital synthesizer techniques. Even later in the development of the superheterodyne architecture, two, or even three, stages of frequency conversion were used, to provide in effect a frequency "sieve" through which spurious by-products of the mixing processes were unlikely to pass.

This evolution has left us with a more or less standard superheterodyne architecture. In recent years, digital techniques are being found to a greater extent in the latter end of the signal processing chain. **Figure 1** shows a modern dual-conversion superheterodyne receiver using linear IF amplifiers. Demodulation to baseband, and possibly some further selectivity, is here accomplished by digitizing the output of the second IF amplifier using an ***analog-to-digital converter*** (ADC) and applying this to a ***digital signal processing*** (DSP) block. AGC is effected via this DSP, but ***variable-gain amplifier*** (VGA) sections (usually, *voltage*-controlled amplifiers, or VCAs) are still required to compress the dynamic range to the point where a relatively low-resolution ADC (usually 8-bits, providing a theoretical dynamic range of 48dB) may be used.

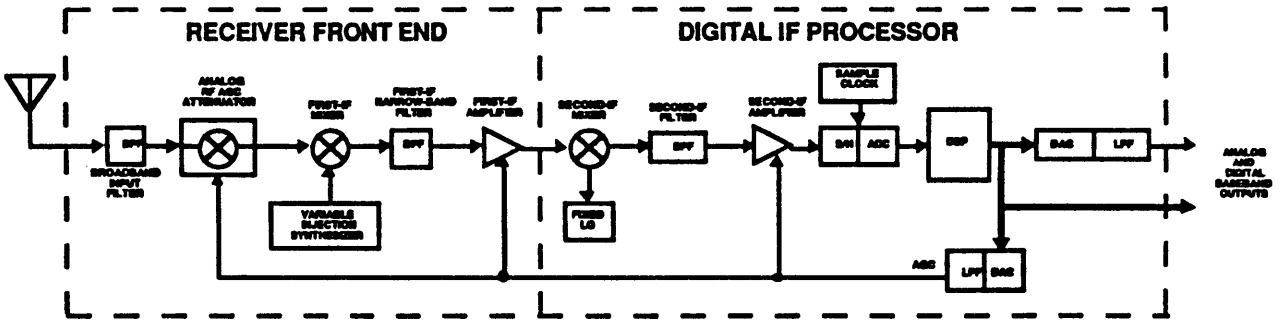

Figure 1. A Modern Superheterodyne Receiver

Of course, many variations of this generalized theme are to be found. Depending on the application, the receiver may use single, dual, or triple conversion and either a fully-analog or DSP baseband section. Whatever the choice of architecture, however, the designer will generally need (in discrete, small-scale monolithic, or specialized ASIC form) mixers, oscillators, filters, RF and IF amplifiers (either linear, or limiting, or sometimes logarithmic), and various types of demodulator, depending on the modulation technique(s) with which the receiver must cope. Analog Devices, Inc. now supplies many of the components for use in high-performance receivers.

Mixers

A mixer[3] is a nonlinear three-port element providing frequency conversion. The two input ports accept the RF and LO signals; these are subjected to multiplication, and the product at the third (output) port includes a strong component at the desired IF, along with a variety of unwanted spectral components. A linear four-quadrant multiplier[4] could be used for this purpose, but its noise performance is much poorer than a circuit optimized for mixing, which in the simplest case provides a linear response only on the RF input, the *phase* of which is *sign-alternated* (0/180°) by the LO input. We will return to this circuit later. Nevertheless, we can understand mixer behavior more readily by assuming *linear* multiplication at this point.

Multiplication in the time domain corresponds to addition and subtraction in the frequency domain. This is easily demonstrated. Given two cisoidal[5] input signals, say, $A\cos\alpha t$ and $B\cos\omega t$, representing the RF and LO inputs respectively, an ideal mixer (which for now is taken to mean one which exactly multiplies its RF and LO inputs) would generate the output

$$A\cos \alpha t \; B\cos \omega t \qquad \text{Eq. (1)}$$

which can be expanded to

$$\tfrac{1}{2} AB \{ \cos (\alpha+\omega) t + \cos (\alpha-\omega) t \} \qquad \text{Eq. (2)}$$

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3 This term is also used in a video and audio context to refer to a totally different element, providing a *linear* combination of two or more inputs.

4 For example, the 500MHz current-output AD834, the 250MHz voltage-output AD835 or the general-purpose 10MHz AD734.

5 That is, either purely sinusoidal or co-sinusoidal, waveforms which differ only in phase positioning.

The two most important features of this process are (1) the appearance of *sum* and *difference* frequencies in the output function[6], and (2) the *fundamental* 6 dB loss (due to the factor of $^1/_2$ in the expansion) in the amplitude of either the sum or difference outputs. When the (usually much higher) sum frequency is used as the IF, the mixer is referred to as an *up-converter*; conversely, the term *down-converter* refers to the use of the (usually much lower) difference frequency as the IF, which is the more common situation.

Of itself, the 6 dB loss would only put an increased burden on the noise performance required of the first stage of the following IF amplifier. More problematical is the fact that, for a *down*-converter, the broadband noise at the mixer input generates an ***image*** (by folding of the α-ω spectrum about the zero-frequency axis) at the IF, so doubling the noise power in the IF passband, leading to a 3 dB worsening of the effective mixer noise, and thus a 3 dB reduction in the dynamic range, referred to the RF port.

Practical mixers generate considerably more complex outputs because of unintentional nonlinearities in the amplitude response, as well as from many subtle mechanisms related to time-varying elements, particularly junction capacitances, within the circuit devices. It is for this reason very desirable to place the first stage of IF filtering as close as possible to the mixer output[7].

For practical reasons (related primarily to noise performance), a linear multiplier is not ideal for mixer applications, nor is there generally any advantage to using such. One reason for this is that IF filtering must be used anyway, so the absence of strong harmonics of the IF — a possible advantage of the linear multiplier when driven by a cisoidal input at its LO port — is unimportant. Another reason is that many modern local oscillators generate square-wave outputs, which is actually desirable in achieving low mixer noise[8].

Thus it is that high-performance mixers, such as diode-transformer (passive) and most IC (active) mixers, use essentially a *switching* (or commutating) process[9]. The *sign* of the

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6 Note that these are not synonymous with upper and lower sidebands, which refer rather to spectral components (at both the sum and difference frequencies) which extend above (upper sideband) and below (lower sideband) the carrier frequency.

7 Either that, or ensure that and signal-handling stages between the raw mixer output and the filter are designed to be ultra-linear. There are many practical details which need to be considered in this regard.

8 Note that while *harmonic* purity is not required of a local oscillator, other types of spectral purity are.

9 The terms "singly-balanced modulator" and "doubly-balanced modulator" are sometimes used to describe particular integrated-circuit structures to implement the mixer function.

signal transmission from the RF port is alternated between normalized binary values of +1 and –1, by an LO input which would ideally be a perfect square-wave. In practice, this can be approximated quite well at moderate frequencies (with today's technologies, this could mean up to about 100MHz, depending on power limitations) but the LO waveform becomes progressively more rounded, and the mixer's switching-time more pronounced, at higher frequencies.

Once again resorting to an idealization to provide rapid insight, a square-wave LO signal at an angular frequency ω can be expressed as the sum of a series of odd harmonics given by its Fourier transform, the first four terms of which are

$$\frac{4}{\pi}\left(\cos \omega t - \frac{1}{3}\cos 3\omega t + \frac{1}{5}\cos 5\omega t - \frac{1}{7}\cos 7\omega t\right). \qquad \text{Eq. (3)}$$

Given an RF signal of normalized amplitude, that is, $\cos\alpha t$, the fundamental IF output (omitting the higher-order terms) has an amplitude

$$\frac{4}{\pi}\cos \omega t \cos\alpha t \qquad \text{Eq. (4)}$$

which expands to

$$\frac{2}{\pi}\left(\cos (\omega + \alpha)t + \cos (\omega - \alpha)t\right) \qquad \text{Eq. (5)}$$

Note that, for a switching multiplier, the normalized insertion loss is only 3.9 dB (that is, $20 \log_{10} \frac{2}{\pi}$). However, although the noise performance is much improved over a linear multiplier cell, the doubling of the output noise in a down-converter, due to the image of the noise at the RF port, remains.

The design and application of passive diode-transformer mixers has been widely treated in the literature and will not be discussed here[10]. Their main advantages are: (1) good linearity when properly driven and terminated; (2) high operating frequencies — to several gigahertz — using low-capacitance Schottky (sometimes, GaAs) diodes, and (3) relatively low cost due to very large manufacturing volumes. Their chief disadvantages are (a) poor isolation between ports; (b) the need for large amounts of LO power to drive

10 A good overview of practical matters is to be found in any of the annual handbooks issued by the American Radio Relay League (ARRL), 225 Main Street, Newington, CT 06111.

the diodes; (c) high absolute insertion loss, and (d) the requirement for very careful matching at the IF port.

Figure 3 shows a common form of diode-transformer mixer, using four diodes; two-diode forms are also used. Passive mixers generally have 8 to 10 dB of insertion loss and a similar noise figure. The signal-handling capability and the third-order distortion are roughly proportional to the LO drive level. High intercept diode-ring mixers can require +27 dBm (500 mW) or more of LO drive.

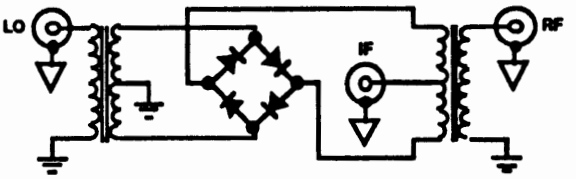

Figure 3. Typical Diode-Ring Mixer

The insertion loss of the passive mixer often requires that it be followed by a Class A low-noise amplifier, which may consume another 500 mW or even more if large signal swings are to be accommodated. The passive mixer's fussy sensitivity to termination often requires the use of a diplexer at the IF port. In some "passive" mixers, the diodes are replaced by FETs which are driven into hard conduction by the LO drive.

Discrete active mixers use transistors — most commonly FETs, sometimes double-gate devices — operating with essentially linear bias conditions. ***IC mixers*** generally use bipolar transistors, and comprise an RF input section which provides voltage-to-current conversion and a two- or four-transistor current-mode switching core, which introduces a more or less abrupt sign-change into the signal path between the RF input and the IF output, controlled by the LO signal. **Figure 3** shows a typical IC mixer.

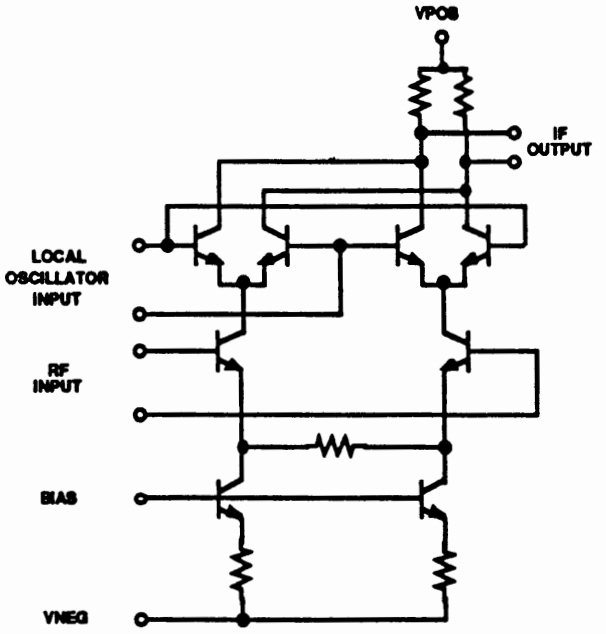

Figure 3. A Typical IC Mixer

The main advantages of active mixers are: (1) conversion gains — of typically 10 to 20 dB — can be achieved; (2) much lower local-oscillator power is needed; (3) excellent isolation between ports is achieved, resulting, for example, in very little radiation of the local oscillator signal from the RF port; (4) they can incorporate a modest amount of variable gain control for AGC purposes; (5) they are essentially termination-insensitive at the IF port; (6) an LO preamplifier can be included to lower the required LO drive to very low levels (say, –20 dBm), and, (7) they lend themselves to higher levels of system integration. The chief disadvantages are: (a) a somewhat poorer dynamic range than passives and (b) typically lower operating frequency limits. However, the advances in IC process technologies over the past decade has led to some dramatic advances in integrated-circuit mixers such that their many advantages will generally outweigh the disadvantages in future products.

The power consumption of active mixers is roughly proportional to signal handling ability — the wider the dynamic range, the higher the supply power. This is because the voltage-to-current converter section must (for almost all RF applications) be a Class-A circuit, using current-sources and resistors to define the maximum RF input, often specified in terms of the "1 dB compression point" (that level at which the output is 1 dB below the ideal value extrapolated from the small-signal response) and the "third-order

intercept" (that extrapolated input level at which the amplitude of the fundamental and the third-order products in the IF output are equal). But low noise demands the use of low-valued resistors (comparable to 50 Ω) to achieve a low noise figure, thus requiring very large bias currents (sometimes many tens of milliamperes) to support the peak inputs without significant intermodulation distortion.

The Analog Devices' **AD831** is a good example of a modern high-performance mixer optimized for use in critical applications where a combination of high third-order intercept (+30dBm) and low noise figure (12dB) are essential. This IC is usable at RF inputs to 800MHz, and includes a wide-bandwidth (100MHz) low-noise IF amplifier which can be configured to provide gain. A variable bias option permits operation at lower power when relaxed performance is permissible. **Figure 4** shows the general topology of the AD831.

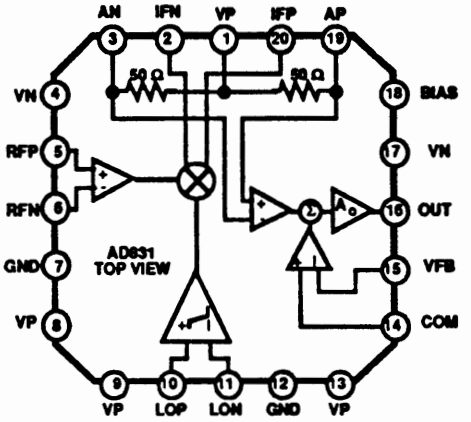

Figure 4. General Schematic of the AD831 High-Performance Mixer

Mixers are often preceded by a ***low-noise amplifier*** (LNA), frequently using silicon MOSFETs below 300 MHz, silicon bipolar transistors up to roughly 1 GHz, and GaAs MESFETs to over 10 GHz[11]. The choice of gain for this amplifier is very critical: it should be just high enough so that its noise dominates the overall mixer performance, which in practice means that the output noise of the LNA needs to be about 6 dB above that of the RF port of the mixer. Any higher gain would only reduce the dynamic range.

11 These ranges are very fluid as silicon IC technologies continue to broaden in applicability.

IF Filtering

The mixer's output has one desired spectral component — the chosen IF, usually the difference frequency — and a host of undesired outputs, due to the presence of the many unwanted signals at the RF input, as well as cross-products arising from unavoidable spurious nonlinearities within the mixer. Thus, bandpass filtering is necessary to select just the desired output from the mixer.

In the case of the AD831, filtering may be added directly at the mixer's core's differential outputs. This may be as simple as shunting the internal resistive loads (2 x 50 Ω) with external capacitors, to heavily attenuate the sum component in a down-conversion application (**Figure 5**). The corner frequency of this one-pole low-pass filter should be placed about an octave above the difference-frequency IF. Thus, for a 70 MHz IF, a -3dB frequency of 140 MHz might chosen, using capacitors of 22.7 pF.

When driving an IF ***bandpass filter*** (BPF), proper attention must be paid to providing the optimal source and load terminations so as to achieve the specified filter response. The AD831's wideband highly-linear output amplifier helps in this connection. Figure 5 indicates how its low-impedance (voltage source) output can drive a doubly-terminated band-pass filter. The 6 dB loss of conversion gain so incurred can be made up by the inclusion of a feedback network (the two 49.9 Ω resistors) which increases the gain of the amplifier by 6 dB (X2). Higher gains can be achieved, using different resistor ratios, but with concomitant reduction in the bandwidth of this amplifier. Note also that the Johnson noise of these gain-setting resistors, as well as that of the BPF terminating resistors, is ultimately reflected back to the mixer's input; thus they should be as small as possible, consistent with the permissible loading on the amplifier's output.

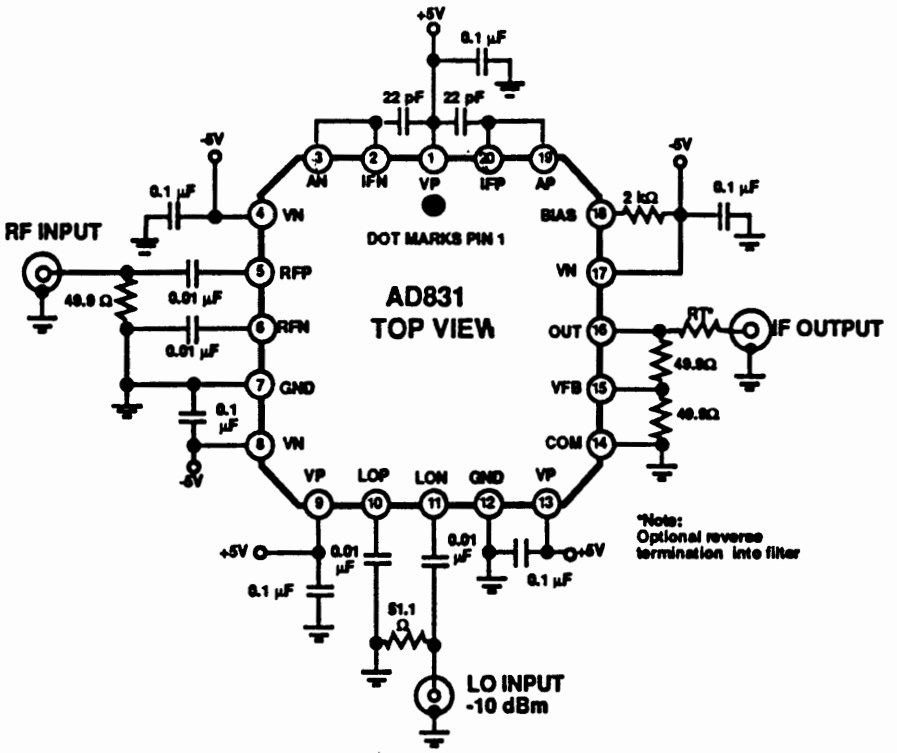

Figure 5. A Typical Down-conversion Mixer using the AD831

IF Amplifiers

IF amplifiers provide almost all of the gain in a superheterodyne receiver, and also allow this gain to be varied for AGC purposes. A well-designed IF amplifier will add a minimum of noise and distortion to the signal. An AGC range of 60 to 90 dB is usually required. While numerous circuit topologies are used, the focus here will be on the *variable-gain* requirement; the gain is assumed to be controlled by an AGC *voltage*.

A popular approach to the design of a voltage-controlled amplifier is to use the reliable exponential relationship between collector current and base-emitter voltage in a bipolar junction transistor, through which means it is possible to achieve a gain-control range of several decades. A widely-used circuit topology[12] is shown in **Figure 6.**

The RF signal voltage V_Y is first converted to a complementary pair of currents, which are here denoted as $(1+Y)I_Y$ and $(1-Y)I_Y$, by a voltage-to-current (V/I) converter formed

12 W. R. Davis and J. E. Solomon, "A High Performance Monolithic IF Amplifier Incorporating Electronic Gain Control," IEEE Journal of Solid State Circuits, December, 1968. (Reprinted in "Analog Integrated Circuits," Alan Grebene, Ed., IEEE Press, New York. 1978)

by Q1, Q2 and R_Y. The "modulation index" Y has a *maximum* range of ±1; in practice, it will have an upper value of about 0.75, in order to minimize distortion due to the nonlinear V_{BE} of the transistors. To a good approximation, $Y = V_Y/I_YR_Y$ (when I_YR_Y is very much greater than the thermal voltage kT/q).

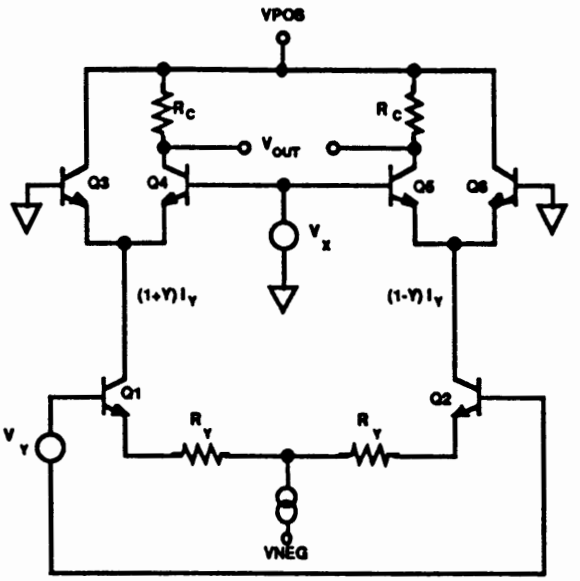

Figure 6. The Controlled Cascode Cell.

The signal-plus-bias currents are then applied to a "current-fork", Q3 through Q6, that steers some fraction, $0 \le X \le 1$, of the signal currents to the output load resistors, and dumps the remainder to the positive supply. These transistors also act as a cascode stage, which extends the frequency range of the amplifier; because of this feature, we will refer to this cell as a "controlled cascode".

The parameter X is determined by the gain-control voltage V_X. It is readily shown that

$$X = \frac{\exp(V_X/V_T)}{1 + \exp(V_X/V_T)} \qquad \text{Eq. (6)}$$

where V_T is the thermal voltage kT/q, which is 25.85 mV at T = 300 K (about 27°C). At this temperature, X is 0.99 when V_X = 120 mV and 0.01 when V_X = –118 mV. If the system gain is normalized to 0 dB when X = 1, the loss is 6 dB for V_X = 0.

Figure 7 shows the decibel value of the current gain of the cascode as a function of V_X at three temperatures.

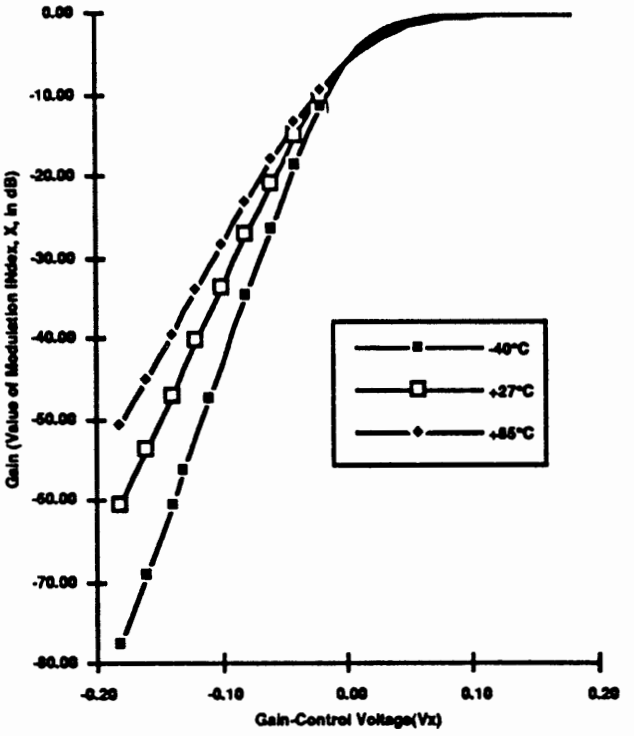

Figure 7. Decibel Gain of the Controlled Cascode

Several potential problems are immediately apparent from this graph. First, this circuit is really a voltage-controlled *attenuator*, rather than a voltage-controlled amplifier. Consequently, when this circuit is followed by a high gain stage to recover the lost signal, the noise performance at minimum attenuation may be disappointing. We will return to this in a moment.

Second, the circuit's control function is not "linear in decibels"; it approaches this condition only for very high attenuation values. Third, the attenuation is a strong function of temperature; this, and the nonlinear control function, may not matter too much in closed-loop AGC systems, but both would be troublesome in "swept-gain" VCA applications, or in feed-forward AGC systems. The temperature-sensitivity can be addressed using special resistors to form an attenuator between the actual gain-control voltage and the base nodes, where the required form is proportional to absolute temperature (PTAT).

Apart from these obvious weaknesses, this cell has additional, more subtle, problems. First, notice that the lower end of the input dynamic range is fundamentally limited by the Johnson noise of R_Y. Now, if this resistor is reduced to the point where acceptable noise performance is achieved, the upper end of the dynamic range will also be reduced, due to the onset of distortion, and eventually clipping, unless very large values of bias current I_Y are used to extend the input voltage range (which, as we've seen, is roughly $I_Y R_Y$).

For example, suppose we wish to achieve a short-circuited input noise spectral density of 1.5 nV/√Hz at 300 K (which corresponds to 15 μV RMS, or -83.5 dBm, in a 100MHz bandwidth). Then R_Y can be no more than 149 Ω. But this assumes that Q1 and Q2 have no ohmic resistances; in practice, their base resistances ($r_{bb'}$) must be subtracted from R_Y to maintain the desired total noise resistance. Even well-optimized monolithic transistors may have $r_{bb'}$ values of 25 Ω, typically requiring R_Y to be no more than 100 Ω.

Now postulate that a maximum input of 1 V RMS must be handled with a total harmonic distortion of less than –60 dBc. (At moderate frequencies the distortion will be third-order, but there will be increasing odd- and even-order components at high frequencies.) To meet this last requirement when R_Y = 100 Ω, it can be shown that the two currents I_Y must each be at least 23 mA; using typical ±5V supplies, this would correspond to an expenditure of almost half a watt in just the voltage-to-current converter!

As if that were not bad enough, we have yet to include the noise due to the controlled cascode part of this circuit. This is negligible only when this cell provides a maximum voltage gain (of $2R_C/R_Y$ when X = 1) that is much greater than unity. Let the noise at the input (due to $2r_{bb'} + R_Y$) be E_a, and that in the load circuit (at the very best, due to $2R_C$ alone) be E_b. The total noise at the output, E_{no}, for the maximum gain condition, where noise performance is critical, is

$$E_{no} = \{ (2R_C/R_Y)^2 E_a^2 + E_b^2 \}^{0.5} \qquad \text{Eq. (7)}$$

Referred to the input, this is equivalent to a noise of

$$E_{ni} = \frac{\{ (2R_C/R_Y)^2 E_a^2 + E_b^2 \}^{0.5}}{2R_C/R_Y} \qquad \text{Eq. (8)}$$

Noting that $E_a = S_\Omega(2r_{bb'} + R_Y)^{0.5}$ and $E_b = S_\Omega(2R_C)^{0.5}$, where S_Ω is the ohm-normalized noise-spectral density and setting $r_{bb'}=0$ for simplicity (and also to show the fundamental limitations more clearly) we can write

$$E_{ni} = S_\Omega R_Y^{0.5} (1 + R_Y/2R_C)^{0.5} \qquad \text{Eq. (9)}$$

The first part of this expression is simply the Johnson noise of R_Y. E_{ni} is increased in direct proportion to the second factor, requiring that $2R_C$ be much greater than R_Y. When $R_C = 2\ R_Y$, for example, the noise is increased by about 12 % or 1 dB. In our example, therefore, we might decide to use $R_C = 400\ \Omega$. But this raises a practical problem: if a value of $I_Y = 23$ mA were used to maintain acceptable distortion levels, the maximum voltage drop across the load resistors R_C would need to be nearly 15 V at full gain and full signal, requiring an inordinately high supply voltage. That problem can be addressed by using a more "classical" reactive load (such as a parallel-tuned LC circuit, or a more complex LC filter) having a low DC resistance. However, modern receivers make extensive use of ceramic resonators which do not provide this DC path, necessitating the inclusion of RF chokes as loads.

Further noise and distortion is generated by the base resistances and capacitances of the cascode transistors. Optimization of these transistors is difficult, since the use of large devices to lower $r_{bb'}$ noise only results in higher capacitances. At low gains, HF signal feedthrough occurs via the parasitic T-network formed by the C_{JE} — $r_{bb'}$ — C_{JC} of these transistors, causing aberrations in the AC response.

Thus, in numerous ways this type of VCA cell fails to meet the exacting requirements of many modern IF systems, although it remains appealing where some concessions to noise, distortion and gain-accuracy can be made. It is a simple cell for use in embedded applications, and provides the highest possible bandwidth for a given process technology. Variable-gain amplifiers built along these lines are available for use up to about 1 GHz.

The X-AMP Concept

Two new dual-channel voltage-controlled amplifiers, the **AD600** and **AD602**, have recently been introduced by Analog Devices. They differ radically from the circuit just discussed. The input signal is applied to a passive seven-section R-2R resistive ladder network, providing from 0 dB to 42.14 dB (7 X 6.021 dB) of attenuation at the various taps. Using a proprietary technique, these taps can be continuously interpolated, and the variably-attenuated voltage is applied to a *fixed-gain amplifier* that uses negative feedback to enhance gain accuracy and linearity. The 42.14 dB range of the attenuator is centered to provide a nominal 40 dB gain range with 1.07 dB of over-range at each end. The term "X-AMP", coined to apply to this architecture, is a reference to the exponential gain function which it inherently provides, that is, the gain control is "linear-in-dB". **Figure 8** is a simplified schematic of an X-AMP.

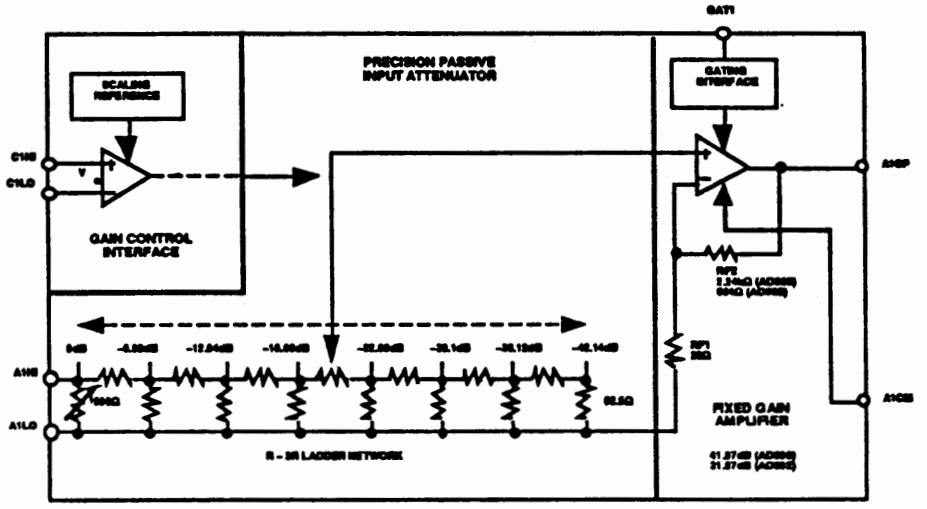

Figure 8. Simplified Schematic of an X-AMP

The X-AMP provides the unusual combination of low noise (1.4 nV/√Hz), good signal-handling capabilities (1 V RMS at the input, 2 V RMS at the output), a constant 3 dB bandwidth of DC to 35 MHz, constant phase and group-delay characteristics, low distortion (–60 dBc to 10 MHz) and low power consumption (125 mW maximum per channel). One disadvantage is some applications is the low input resistance of 100 Ω, but this is laser-trimmed to be within ±2 %, which simplifies interfacing in many cases.

The two channels of the AD600 and AD602 are independent, and may be cascaded for a gain range of up to 80 dB in one package. Separate high-impedance, differential gain-control interfaces are provided; the gain is precisely calibrated to 32 dB/Volt (31.25 mV/dB). In the AD600 the gain for each section is 0 dB for $V_G = -625$ mV, 20 dB for zero V_G, and 40 dB for +625 mV. When V_G exceeds these values, the minimum gain becomes –1.07 dB and the maximum is 41.07 dB. The AD602 is similar, except that each VCA provides a gain[13] of –11.07 dB to 31.07 dB.

Thus, for the AD600, the gain of each amplifier is

$$G_{dB} = 32*V_G + 20 \qquad \text{Eq. (10a)}$$

while for the AD602 it is

$$G_{dB} = 32*V_G + 10 \qquad \text{Eq. (10b)}$$

A new product, the **AD603**, is a ***single-channel*** X-AMP in an eight-pin format. It is optimized for IF applications, providing a basic gain range of –11.07 dB to 31.07 dB from DC through 70 MHz. Using a simple pin-strap (**Figure 9**) the gain range becomes +8.93 dB to +51.07 dB, with a –3 dB bandwidth of about 7 MHz. Using one external resistor, any gain range in between these extremes can be provided, with pro-rated bandwidth. The gain-scaling is slightly different, requiring 25 mV/dB, that is, exactly 1V for a 40 dB gain-change; the control interface remains fully-differential, has an input impedance of about 50 MΩ and provides a somewhat larger common-mode range, and lower bias currents, than the AD600/2.

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13 The importance of the rather precisely-specified limits values for the gains will later be understood in connection with the various gain-sequencing schemes used in practical applications to be presented.

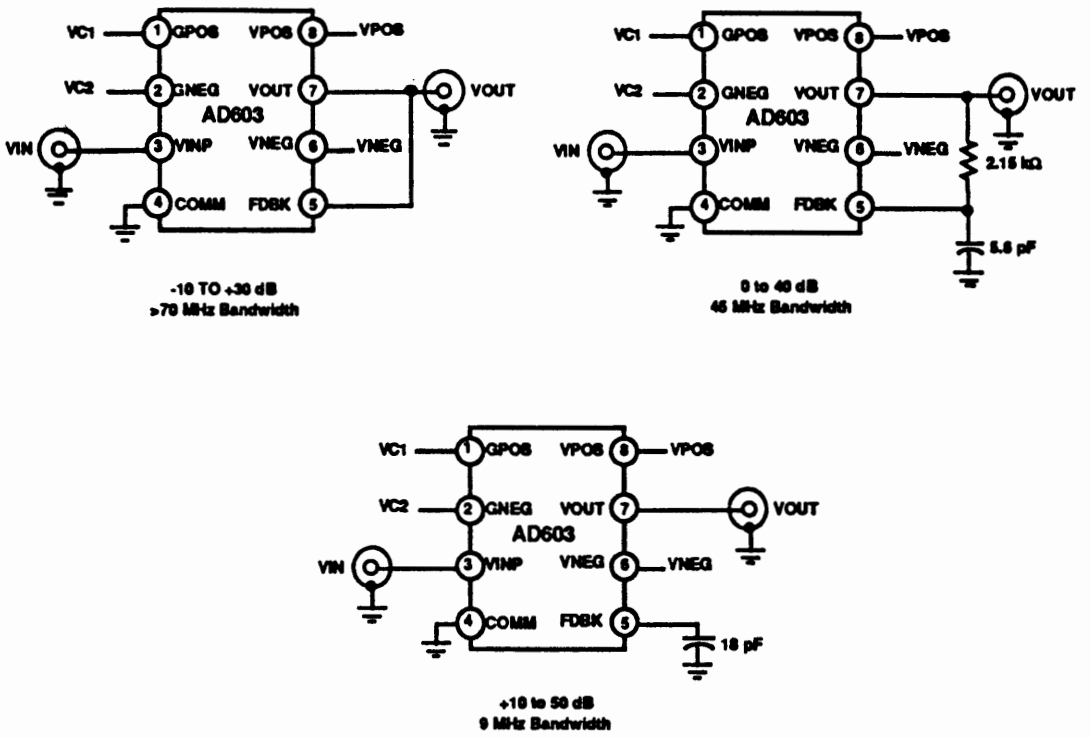

Figure 9. Pin-strapping to Set the AD603 Gain

(The capacitors are optional and serve to extend the bandwidth)

The two sections of an AD600 or AD602 or two AD603s can optionally be operated in *parallel*, to achieve an input noise spectral density of 1 nV/√Hz with no compromise in other aspects of performance.

60 dB AGC System with Optimal Signal-to-Noise Ratio

By way of illustration, we show how to use the AD600 in a 10.7MHz IF application. Recall that each section provides a gain range of about –1 dB to +41 dB with independent control. These two sections can be cascaded to provide a maximum gain of 82 dB (2*41 dB), as shown in **Figure 10**, but the inclusion of a doubly-terminated, lossy BPF lowers this by approximately 20 dB, as indicated on the figure, to 62 dB. The minimum gain is therefore –22 dB (that is, 2*(–1 dB) – 20 dB).

This amplifier system includes a simple one-transistor detector, which also provides a means to integrate the AGC error signal[14]. However, this may be omitted and gain control effected by DSP if desired. In either case, the fact that the gain control voltage is "linear-in-dB" means that the AGC voltage bears an exact correspondence to the decibel level at the input, that is, it provides an accurately-calibrated RSSI (Received Signal Strength Indication) function.

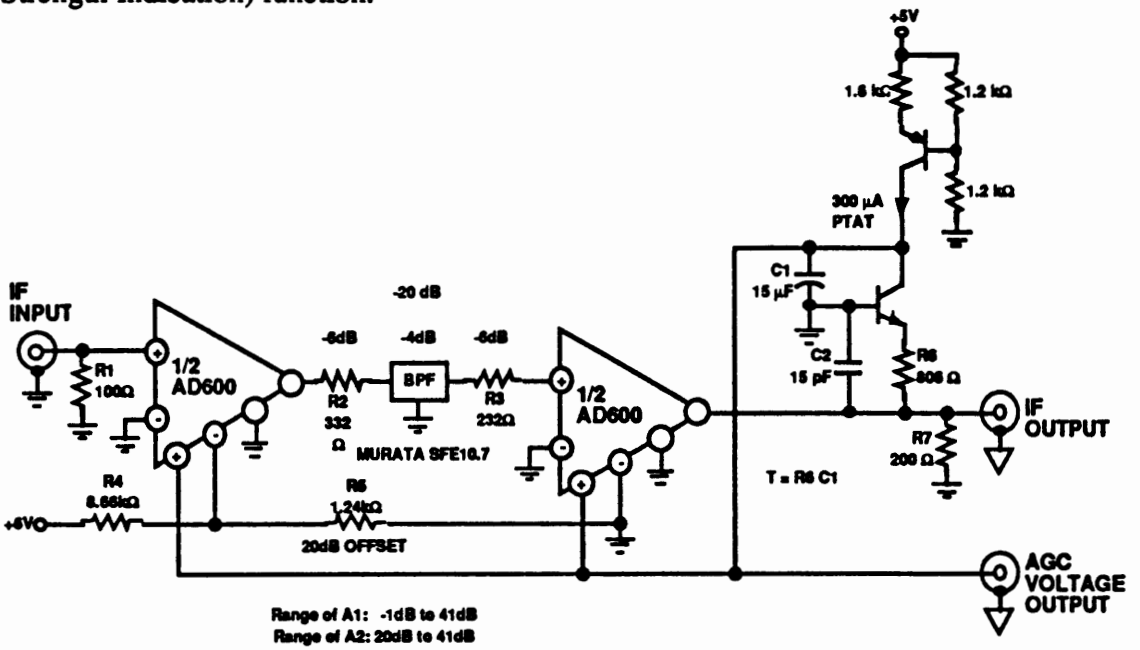

Figure 10. 60 dB AGC Amplifier

It is not necessary to provide any nonlinear shaping of the control signal because the gain of each X-AMP section remains accurate (at its minimum or maximum value) even when the control input is overdriven. The only care needed is in providing the correct amount of offset between the two sections to use the full gain range possible in each half of the AD600. In this system, A2 compensates for the 20-dB loss due to the bandpass filter and termination resistors, which leaves only half of its range, while A1 provides the full 42 dB. R4 and R5 provide this gain-control offset between the two amplifier sections, ensuring smooth transitions between the gain segments of each section.

The input impedance of this system is optionally padded to 50 Ω by the addition of R1 in shunt with the 100 Ω input resistance of the AD600. The output can drive 2V RMS into a final load of 200 Ω. For illustrative purposes, a 10.7 MHz ceramic filter (Murata SFE10.7) that requires 330 Ω terminations at both source and load is used.

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14 The operation of this detector is explained at length in the AD600/2 data-sheet.

An interesting aspect of this amplifier is the behavior of the complete AGC loop under rapidly-changing input levels. Using a relatively small value for C1 the response time can be fast enough to allow the use of the AGC voltage as a signal output; for some modulation modes, the exponential nature of the transfer function is tolerable. **Figure 11** shows the AGC output in response to different input levels, when the 10.7 MHz signal is modulated to a depth of 50 % by a 10 kHz square-wave. The constant 6 dB difference between the maximum and minimum signal levels results in a constant 188 mV (6 dB * 31.25 mV/dB) variation on the AGC line.

Figure 11. AGC Response (see text)

A Log-Limiting IF Amplifier

Systems that use phase- or frequency-modulation often require an IF amplifier that provides an ***amplitude-limiting*** response. In many cases, the overall phase-shift in this amplifier must be very stable with fluctuations in the signal level. Some digital-mobile radio standards also require accurate signal measurement (Received Signal Strength Indication, or RSSI) in order to control transmitter power levels at both the mobile and fixed stations, thus ensuring the use of the minimum power to maintain reliable communications. This function is appropriately provided by a ***logarithmic amplifier.***

The Analog Devices' **AD606** was developed for such applications. It is a complete monolithic nine-stage logarithmic amplifier having a dynamic range of over 80 dB (from –75 dBm to at least +5 dBm) and providing a limiting output with a gain of 100 dB. It is usable to 70 MHz and consumes only 65 mW from a single 5 V supply. It may be rapidly powered-up or down (to about 100 µA) by a CMOS-compatible logic input.

Figure 12 shows a typical application of the AD606. The nominal slope at the low-impedance RSSI output is 37.5 mV/dB up to 15 MHz; it drops to 35 mV/dB at 45 MHz. Optional adjustments R1 and R2 allow accurate calibration of the slope and intercept. The hard-limited output is 200 mV (pk-pk) minimum across the typical 200Ω load resistor (R3 in Figure 12). The phase at this output is maintained to within ±3° over the 80 dB range at 10.7 MHz.

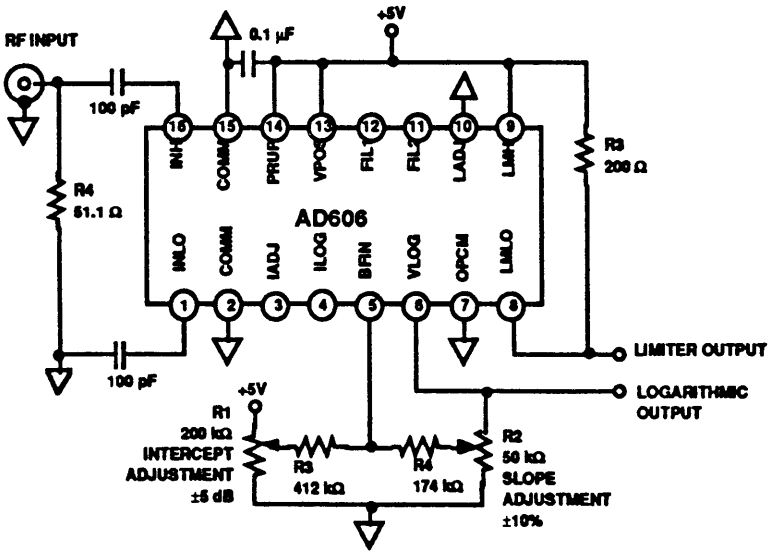

Figure 12. The AD606 80-dB Log/Limiting IF Amplifier

A 250-MHz Voltage-out Analog Multiplier

Analog multipliers are useful in a variety of signal-processing applications. They may, for example, be used as voltage-controlled amplifiers, exhibiting a *linear* gain-control function, where the signal level and the required control range are both moderate. In the past, these have usually been limited to two types: (1) "analog computing" multipliers, with low to moderate bandwidths (1 MHz for the industry-standard AD534, or 10 MHz for the AD734, which may also be used as an analog divider with a 60-dB gain range) and operating at high signal levels (±10 V full-scale) and requiring ±15-V supplies, or (2) very high bandwidth multipliers such as the popular AD834, having open-collector outputs.

The **AD835** is an advanced analog multiplier which is fabricated using a very fast dielectrically-isolated complementary-bipolar process, providing four-quadrant operation from X- and Y-inputs of nominally ±1V and a voltage output capable of driving loads as small as 25 Ω. In its basic mode of application its 3 dB bandwidth is 250 MHz. This multiplier has much lower noise than the AD534 or AD734, making it attractive in signal-processing applications as a gain-control element.

The function provided is, in its most complete form

$$W = \frac{(X_1-X_2)(Y_1-Y_2)}{1V} + Z \qquad \text{Eq. (11a)}$$

where W, X, Y and Z are all voltages. The concept of this multiplier can be more readily appreciated by setting $X = X_1-X_2$, $Y = Y_1-Y_2$ and $Z = 0$, when we can write

$$W = XY \qquad \text{Eq. (11b)}$$

provided it is understood that all signals are expressed in *Volts*.

The AD835 is packaged in an 8-pin format, and in spite of its high bandwidth is very versatile and easy to use. A useful feature of the AD835 is the capability to add another signal to the output using the variable "Z" in Eq. (11a), a voltage applied to pin 4. We will here show three applications of the use of this feature: a wideband voltage-controlled amplifier, an AM modulator and a frequency-doubler. Of course, the AD835 may also be used as a square-law detector (with its X- and Y-inputs connected in parallel), useful to well over 250 MHz, since this is only the bandwidth limitation of the *output* amplifier.

A Wideband Voltage-Controlled Amplifier

Figure 13 shows the AD835 configured to provide a gain of nominally 0 to 12 dB. (In fact, this range extends from well under –12 dB to about +14 dB). R1 and R2 set the gain to be nominally X4. The attendant bandwidth reduction that comes with this increased gain can be partially offset by the addition of the peaking capacitor C1. Although this circuit shows the use of dual supplies, the AD835 can operate from a single 9-V supply.

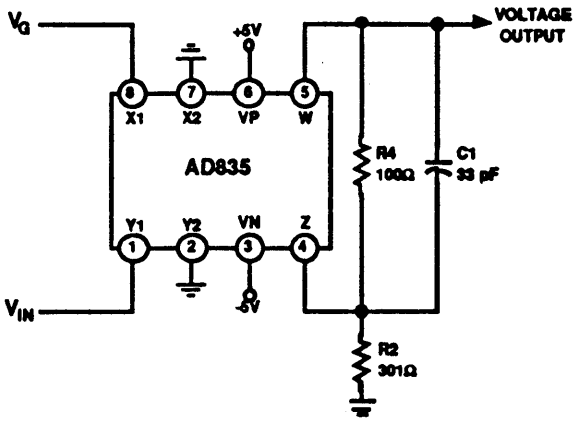

Figure 13. Voltage-Controlled 50 MHz Amplifier using the AD835

The AC response of this amplifier for gains of 0 dB (V_G=0.25V), 6 dB (V_G=0.5V) and 12 dB (V_G=1V) is shown in Figure 14. The phase may be inverted by the sign of V_G.

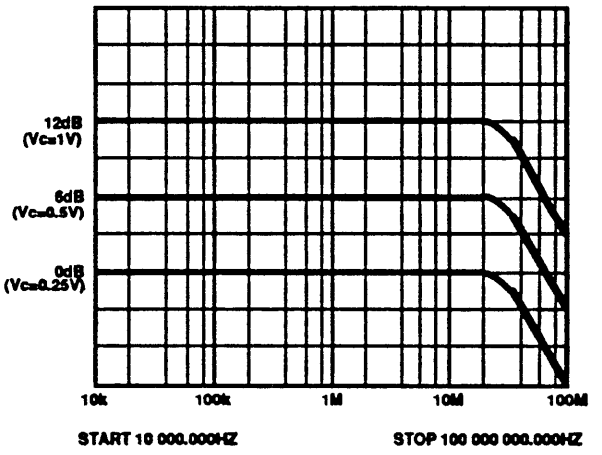

Figure 14. AC Response of VCA

An Amplitude Modulator

Figure 15 shows a simple modulator. The carrier is applied both to the Y-input and the Z-input, while the modulating signal is applied to the X-input. For zero modulation, there is no product term, so the carrier input is simply replicated at unity gain by the voltage-follower action from the Z-input. For X = +1 V, the RF output is doubled, while for X = –1 V it is fully suppressed. That is, an input of X = ±1V corresponds to a modulation index of 100 %. Carrier and modulation frequencies can be up to 300 MHz, that is, somewhat beyond the nominal 3-dB bandwidth.

Of course, a suppressed-carrier modulator can be implemented by omitting the feedforward to the Z-input.

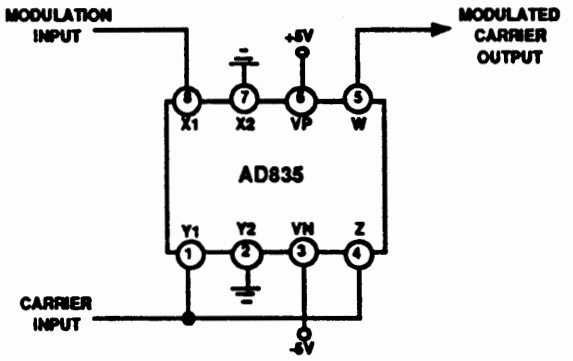

Figure 15. Simple Amplitude Modulator using the AD835

Frequency-Doubler

Finally, **Figure 16** shows a frequency-doubler which provides a relatively constant output over a moderately-wide frequency range, determined by the CR product of C1 and R1. The voltage applied to the X- and Y-inputs are exactly in quadrature at a frequency $f=1/2\pi C_1 R_1$ and their amplitudes are equal. At higher frequencies, the X-input becomes smaller while the Y-input increases in amplitude; the opposite happens at lower frequencies. The result is a double-frequency output, centered on ground, whose amplitude of 1 V for a 1 V input varies by only 0.5 % over a frequency range of ±10 %. Because there is no "squared" DC component at the output, sudden changes in the input amplitude do not cause a "bounce" in the DC level.

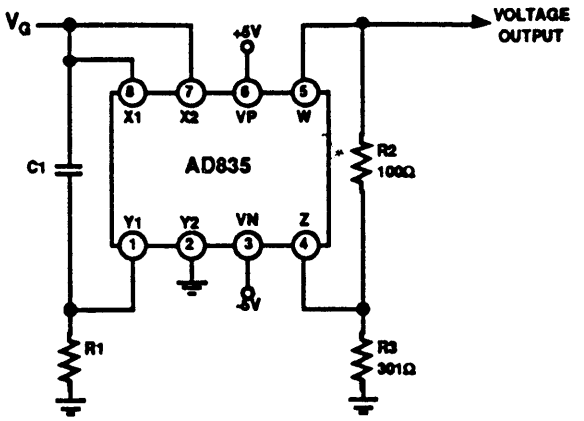

Figure 16. Broadband "Zero-Bounce" Frequency-Doubler

Summary

While there is a clear progression toward highly-integrated ASICs for modern high-volume communications applications, many of the key challenges remain in the area of high-performance analog-signal manipulation using moderate scales of integration. By focusing on some of the key challenges in this area, Analog Devices has been able to achieve some major performance advances. Thus, the AD831 the first monolithic mixer to provide a third-order intercept of +30 dBm with a noise figure of 12 dB and to include a high-bandwidth low-noise output amplifier affording high conversion gains; the X-Amp concept, embodied in the AD600, AD602, and AD603, provides a unique combination of low noise, low power, wide bandwidth and low distortion, with the added benefit of exactly-calibrated "linear-in-dB" gain control; the AD606 is the first monolithic nine-stage log-amp to be offered, and operates at only 65 mW from a single 5-V supply; the AD835 four-quadrant analog multiplier uses an advanced IC technology to provide a 250 MHz bandwidth in a voltage-output format. These, and a broad range of high-speed amplifiers and A/D converters, as well as a growing catalog of DSP products, provide a wide variety of solutions to the designer of state-of-the-art communications systems.

Digital Signal Processing in Wireless Communications
Focus on Digital Transmitters

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ABSTRACT
In communication systems, modern transmitter and receiver designs use digital signal processing (DSP) microprocessors. DSPs can compute complex mathematical expressions over ten times faster than a conventional microprocessor of similiar complexity. In a receiver, DSPs are used to demodulate signals from IF to baseband. In a transmitter, a DSPs are used to modulate the baseband signal to IF and to precondition the outgoing signal before it is attenuated by the channel. If the baseband signal is data instead of voice, a DSP can be used to decode the complex analog signal that represents the data to binary information. DSP based transmitters can be used to encode digital information. A DSP's reprogrammability makes possible a modem that employs different encoding and decoding schemes. DSPs can improve noise performance of a transceiver using digital filters and automatic gain control. The same circuit can be used to transmit and receive either sampled voice or data. This paper surveys the use of DSPs in radio transmitters.

INTRODUCTION
Digital signal processors are used extensively in telecommunication systems for cancelling echos, detecting tones, conferencing multiple voice channels, and compressing sampled voice data. DSPs are commonly used in central office (CO) switches, private branch exchanges (PBX), and voice mail. The advantage of DSP is reconfigureability since it executes programs from RAM.

The DSPs discussed in this paper are general purpose and fully programmable. They execute instructions from memory as the CPU in a personal computer does. By downloading a different program to the DSP, the system's function can be altered. Another advantage of a digital signal processor over analog componenets is the ability to process multiple channels through a single signal path. For example, one DSP can detect touch tones on 30 telephone lines simultaneously.

Some available DSPs are designed to perform a single function such a modulation/demodulation, modem signal decoding, or digital filtering. These components perform one function with higher throughput than a general purpose DSPs and are often required in high bandwidth digital radios where multiple channels of information or voice are multiplexed in a single band. These components are necessary in high speed radio modems (100Kbits/second). These components are typically more expensive than a general purpose DSP.

DSP PERFORMANCE
A DSP has performance limitations. The limit is the number of instructions that can be completed between samples. A DSP that executes instructions at 16MHz and uses an A/D converter (ADC)

that samples at 8KHz can process 2000 instructions (16MHz/8KHz) every sample interval. If there are 10 input channels, the processor must divide the 2000 instructions into 200 for each channel. System performance is dependent the processor's instruction rate, the ADC sample rate and the number of channels to be processed. The fastest DSPs available have 20MHz-40MHz instruction rates.

In real-time imaging applications, pixels arrive at a 10MHz sample rate minimum. A 40MHz DSP would only have four instructions (40MHz/10MHz) per pixel. Four instructions are hardly enough programming steps to enhance an image or to recognize an object on the production line.

In the case of radio communications, the baseband signal has a bandwidth of 4KHz-25KHz depending on the nature of the information. High fidelity audio uses over 20KHz per stereo channel. "Toll quality" voice is limited less than 4KHz of bandwidth. V.32 modems encode 9600bits/second data onto an analog signal using less than 4.8KHz bandwidth. DSPs are used in consumer audio products, telecommunication systems, and high speed modems.

RADIO TRANSMITTER

Figure 1 is a radio transmitter design that incorporates a DSP. The DSP generates the baseband signal. If the baseband signal is voice, an ADC is required for the microphone input. A CODEC circuit combines a voice band (300Hz-3700Hz) ADC, an antialiasing filter, voice band DAC, and DAC reconstruction filter in a single integrated circuit. The DSP used in this example is the ADSP-2115 from Analog Devices, a 16-bit DSP. The voice CODEC is the Analog Devices AD28msp01, a device that includes a 16-bit ADC. The DSP interfaces to the CODEC over a serial port. If the baseband signal is binary information, the data originates from a host microprocessor. The DSP's second serial port can interface to the host.

Voice is usually sampled at 8KHz. The sampled voice is modulated to an intermediate frequency (IF). In an analog transmitter, the baseband signal is modulated to IF by being multiplied or mixed with a sine wave at the intermediate frequency. The same applies for a digital transmitter, but the multiplication occurs in software. The baseband signal is multiplied by a digital sine wave stored in DSP memory. The multiplier output product is written to a DAC (Analog Devices DAC-16). The DSP is performing two tasks. One task is processing incoming voice at an 8KHz input sample rate. The other task is writing 456KHz modulated voice to the DAC at a 1.824MHz rate (4 times 456KHz). The DSP can divide its master clock to generate the master and sample clocks for the CODEC's ADC, but the 1.824MHz clock is best handled by a separate oscillator to avoid jitter noise caused by the DSP's master clock. Jitter caused by the DSP's master clock has a negligible effect on 8KHz voice band ADC.

The CODEC's ADC sample rate is 8KHz. The signal may be processed at baseband, but must be interpolated or upsampled to 1.824MHz for modulation. The DSP is used to perform the interpolation function (Figure 2). The interpolation factor between 8KHz and 1.824MHz is 228. The simplest interpolation is linear interpolation where the 227 interpolated samples are calculated by finding the values on a straight line between two 8KHz samples. Linear interpolation will introduce distortion since it appoximates the original signal. Another option is to perform an interpolation filter using finite impulse response (FIR) or feedforward filters. The interpolation

filter generates 228 samples from each 8KHz sample. Interpolation filters with a large interpolation factors are typically performed in stages. In this example (Figure 2), the original 8KHz signal is interpolated by 4 to 32KHz. In the next interpolation stage, the 32KHz signal is interpolated by 3 to 96KHz. In the last stage, the 96KHz signal is interpolated by 19 to 1.824MHz. Interpolating in stages does not require any less performance from the DSP, but does reduce the number of filter coefficients stored in memory and improves distortion.

The digital IF sine wave in RAM is actually four values. A full 456KHz sine wave is a 360 degree cycle. To represent this signal at a four times sample rate (1.824MHz), means to divide the signal into four 90 degree phases, thus represent the sine wave with four values (0,1,0,-1) in memory. Every 1.824MHz interrupt will require a multiply of one of these values times the interpolated voice sample. After the multiply, the product is written to the DAC. The DAC output goes through a simple analog reconstruction filter. The remaining processing required to modulate to RF is accomplished using analog components.

MODULATION SCHEMES

In the above example, the baseband signal is modulated by the sinusoidal signal, creating a double sideband - suppressed carrier (DSB-SC) signal. As shown in Figure 3a, there is not any energy at the IF frequency, only at the two sidebands. In software, if a DC component is added to the baseband signal before multiplying by the IF sine wave, energy will be present at the carrier frequency (Figure 3b). This is amplitude modulation (AM). The sum of the DC component, a programmed constant, and the ADC sample from the CODEC should limited to 16-bits or overflow occurs. The ADC sample must be arithmetically attenuated by the DSP before it is added to the DC component.

The other modulation technique worth mentioning is single-sideband (SSB). Referring to Figure 3a, the baseband signal is replicated by the IF mixer on both sides of the IF frequency. A single-sideband transmitter requires that only one of the two sidebands is transmitted. DSPs can be used to filter one sideband simplifying the RF section.

DATA ENCODING

Radios are used to transmit binary data. In the case of digitized voice, the data rate is 64Kbits/second or more. Using linear predictive coding (LPC) speech data compression algorithms, the data rate can be compressed to 4Kbits/second. LPC algorithms require a DSP to perform mathmatical analysis on short time intervals of incoming voice samples. The DSP reduces the sampled voice into speech coefficients that define the pitch and model the vocal tract of the speaker. These coefficients, when received, are used to synthesize the original speech. LPC algorithms are used to reduce transmitted data in the next generation digital cellular systems in North America, Japan, Europe, and Austrailia.

In telemetry systems, binary information (ones and zeros) are transmitted as samples of 16-bit magnitude (Figure 4a) at four times (4X) the data rate. If the binary data rate is 2400 bits/second, the output sample rate is 9600Hz. When this signal is transmitted it suffers degradation due in part to harmonics caused by the sharp transistions between one and zero samples. These

harmonics increase the bandwidth of the signal and the likelihood of bit errors. The DSP typically applies a low pass or pulse shaping FIR filter to the signal before transmission (Figure 4b).

If the data is redundant, the resulting signal's spectrum is limited to a narrow band making it more susceptible to narrow band noise and making error recovery more difficult. The data can first be scrambled using using a binary polynomial. This process will make the bit pattern more random thus increasing its bandwidth. The receiver can unscramble the pattern as long as it uses the same polynomial in its decoder. Since a DSP is a microprocessor, it is well suited for such encoding. If a higher data rate is required, using the above described scheme, more bandwidth and a higher output sample rate is required.

Another possibility is to encode the signal using quadrature amplitude modulation (QAM). QAM maps two, three, or four bit symbols onto a complex signal constellation (Figure 5). Each symbol is represented on this signal map as a complex number. This complex number is applied to the system shown in Figure 6. The real and imaginary components are both applied to separate pulse shaping filters. Both filters have identical response. The filtered real component is multiplied by the cosine wave of frequency greater than one half the bandwidth of the symbol rate. The filtered imaginary component is multiplied by a sine wave of frequency greater than one half the bandwidth of the symbol rate. Both products are summed. The resulting signal has bandwidth less than if the data was not encoded and is easier to recover on the receiver.

One example is V.32 modems. Although the V.32 specification was created for wired systems, it encodes 9600 bit/second data into 5-bit symbols at 2400 symbols/sec. The symbol picks up an extra bit for noise immunity, error correction, and error detection. The resulting signal uses less than 4.8KHz bandwidth when modulated onto a 2400Hz subcarrier. The motivation of the V.32 standard was to allow higher data rates on the bandlimited (5KHz-10KHz) telephone system. Using less bandwidth also applies in radio comunications. Less bandwidth per channel allows more channels to be allocated in a frequency band. Since a radio channel is not bandimited as is a telephone line, higher data rates are possible.

In a radio transmitter that broadcasts data, the DSP encodes data, upsamples the baseband signal to the IF sample rate, and modulates the baseband signal to IF. The only limitation is the number of DSP instruction cycles available to accomplish the task.

CONCLUSION

DSPs are currently being used in wireless telephone systems (both private and public), AM radio transceivers, and in wireless data communications systems. A DSP can be used to perform multiple functions that typically require many discrete analog components. In most cases a DSP is more cost effective than a discrete analog approach. This is most true when the system has different modes of operation (modulation schemes, voice/data input). The RF section of the system will continue to be handled by discrete analog components including amplifiers, frequency generators (PLL or DDS), and narrowband filters. As DSPs execute instructions at faster rates and the costs of DSPs, ADCs, and DACs decrease, DSP will more prevalent in communications equipment.

REFERENCES

[1] R. Groshong and S. Ruscak, "Undersampling Techniques Simplify Digital Radio", Electronic Design, May 23, 1991, Penton Publishing

[2] R. Groshong and S. Ruscak, "Exploit Digital Advantages In An SSB Receiver", Electronic Design, June 13, 1991, Penton Publishing

[3] "DSP Tutorial, Modulation, Fourier Series, and Sampling Theory", Spread Spectrum Scene, October 1992, El Granada, CA: RF/Spread Spectrum, (415)726-6849

[4] R. Higgins, "Digital Signal Processing in VLSI", Analog Devices Technical Reference Books, Englewood Cliffs, NJ, Prentice Hall, 1990

[5] R. Crochiere and L. Rabiner, "Multirate Digital Signal Processing", Englewood Cliffs, NJ: Prentice Hall, 1983

[6] L. Couch II, "Digital and Analog Communication Systems", New York, NY: Macmillan, 1993

[7] "The American Radio Relay League Handbook, 1993", Newington, CT: American Radio Relay League, 1992

[8] Analog Devices, "ADSP-2100 Family Applications Handbook, Volume 4", Norwood, MA: Analog Devices, 1990

[9] Analog Devices, "ADSP-2100 Family User's Manual", Englewood Cliffs, NJ: Prentice Hall, 1993

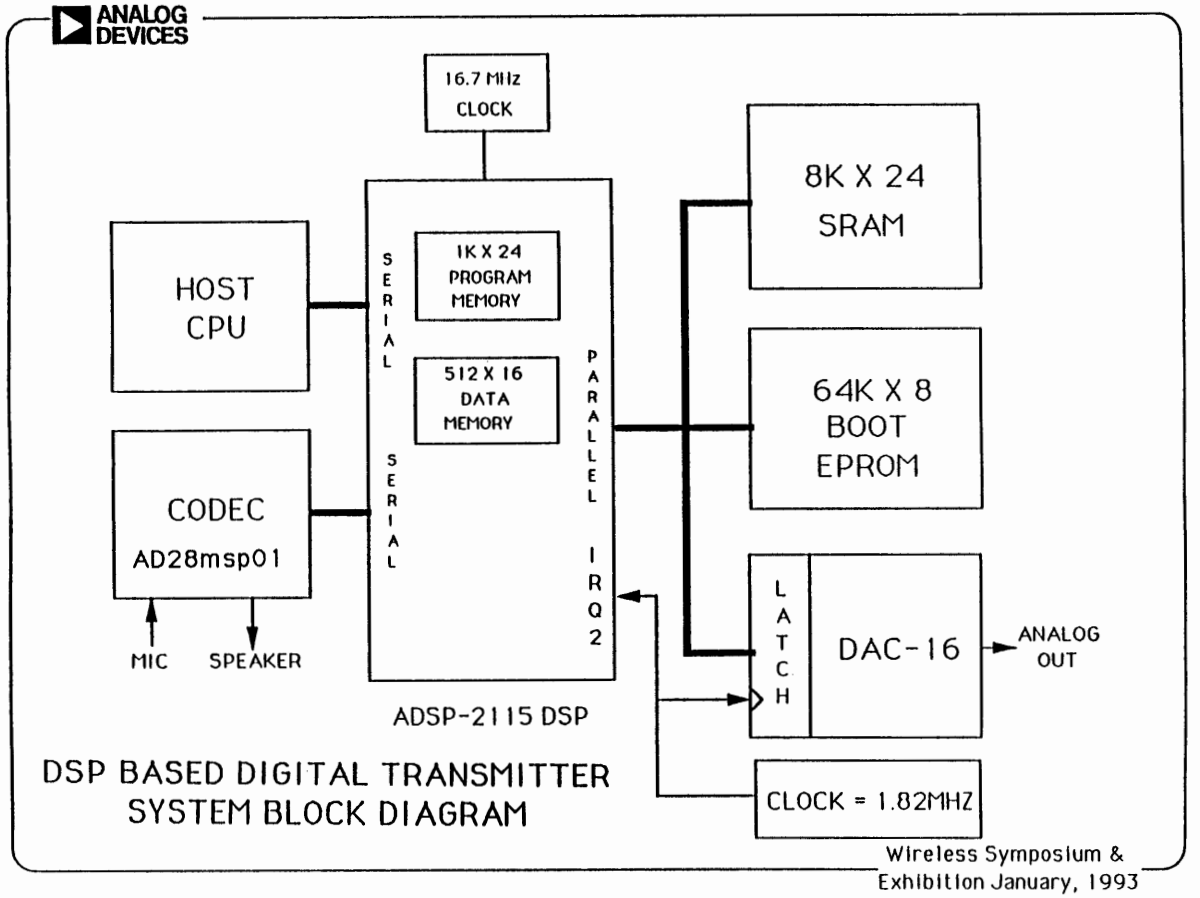


FIGURE 1

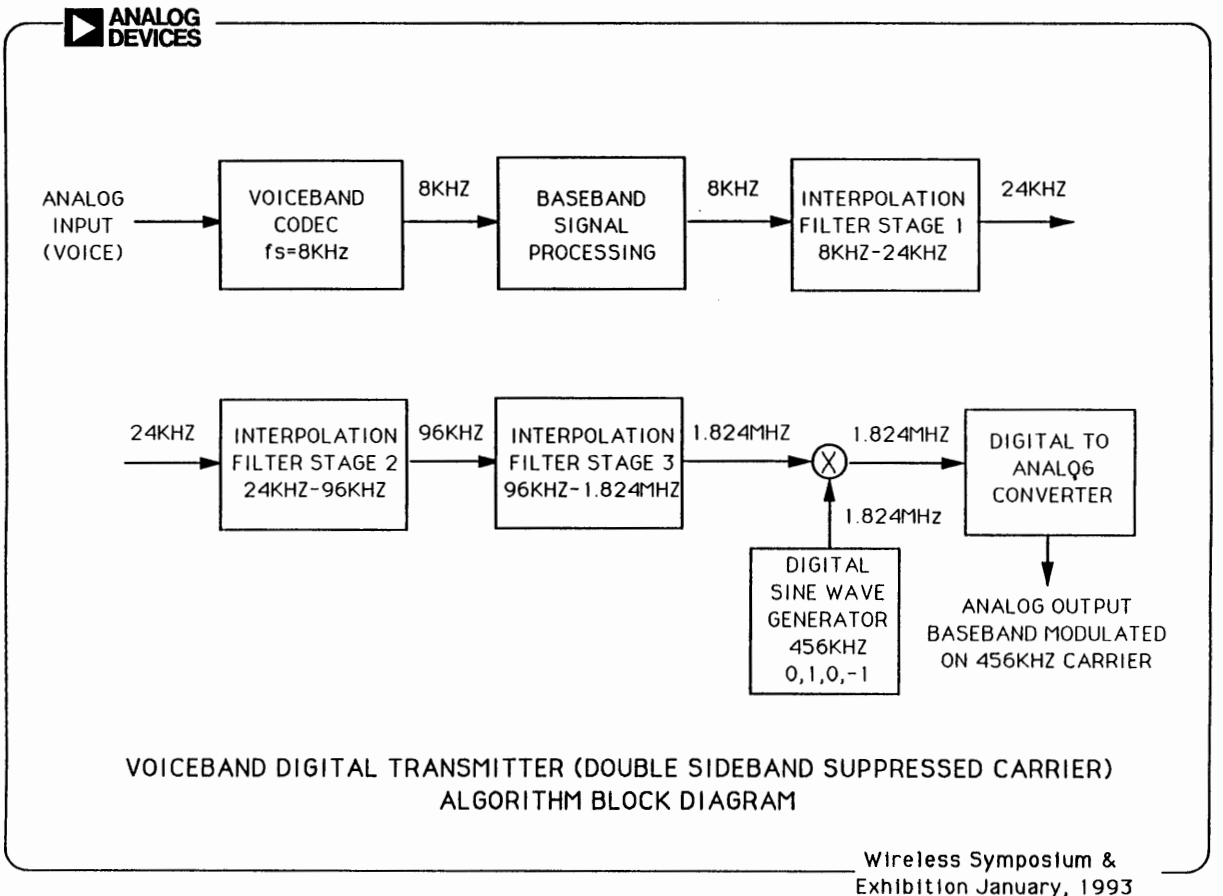
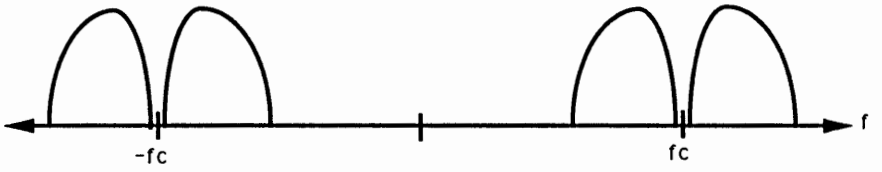


FIGURE 2

ANALOG DEVICES

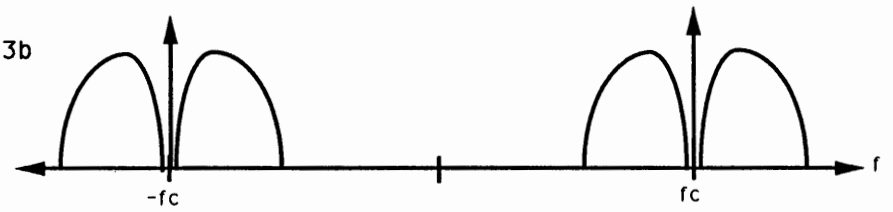
Double Sideband Suppressed Carrier

FIGURE 3a



Amplitude Modulated

FIGURE 3b



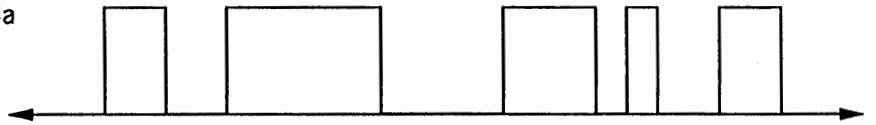
MODULATION TECHNIQUES

Wireless Symposium & Exhibition January, 1993

ANALOG DEVICES

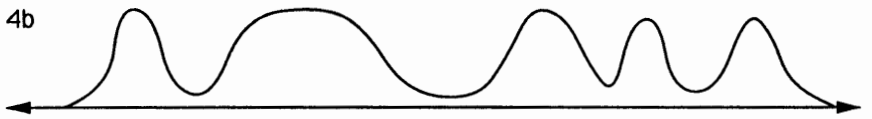
Telemetry Signal Without Pulse Shaping Filter

FIGURE 4a



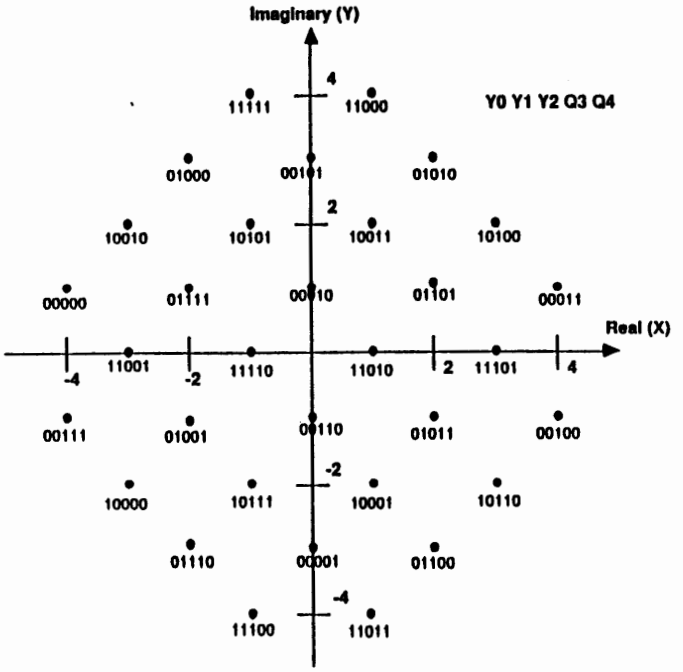
Telemetry Signal With Pulse Shaping Filter

FIGURE 4b



PULSE SHAPE FILTERING BINARY SIGNALS

Wireless Symposium & Exhibition January, 1993



V.32 MODEM SIGNAL CONSTELLATION

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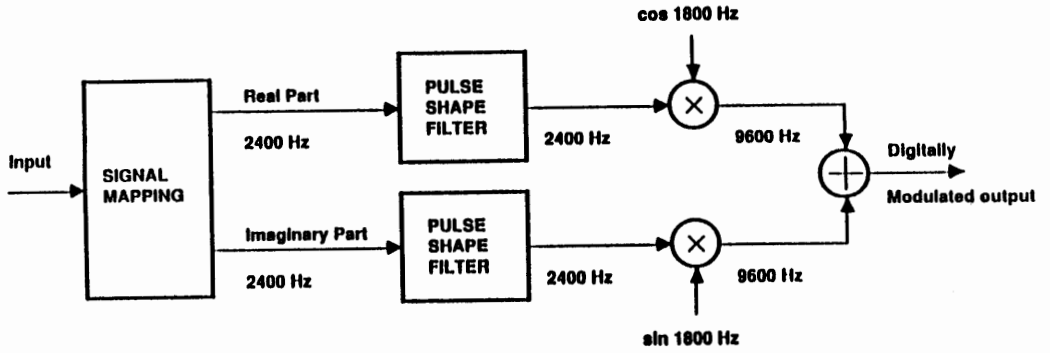
FIGURE 5



MODEM SIGNAL MAPPING AND QUADRATURE AMPLITUDE MODULATION

Wireless Symposium & Exhibition January, 1993

FIGURE 6

Lumped and Distributed Circuits for Wireless Communications

Session Chairperson: Mark McDonald, *Wireless Communications, National Semiconductor (Santa Clara, CA)*

Key Topics in Radio System Design

John G. Freed
Teletec Corporation

I. *INTRODUCTION*

A radio system designer faces many challenges in the design of an RF communications system. Two of the key issues affecting the quality, and ultimately the financial success of a wireless system, are reliable coverage and freedom from interference. The subscriber is the first to notice substandard performance in these areas. Proper planning from the beginning can avoid a disaster.

II. *PLANNING THE COVERAGE AREA*

In the design of the system, the engineer must balance the subscriber unit to base site and base site to subscriber unit ranges. When planning the system, the engineer must consider the propagation unique to the frequency and terrain, the transmitter power output, receiver sensitivity, and antenna gain. Much study of propagation has been done [1] and will not be treated in any depth here since the designer has little control over it.

The system engineer has control over base station and subscriber unit transmitter power, receiver sensitivity, and antenna gain. In planning the system coverage, the designer needs to consider the desired communication range and then refer to one of the various references on propagation to determine the amount of attenuation that must be overcome to provide the grade of service necessary for the system. Roughly speaking, the number obtained covers the free space path loss, fading, shadowing caused by buildings and trees, and an additional factor for grade of service. Once the link loss is known the system engineer can specify the power output, receiver sensitivity, and antenna gain required to make up this loss.

The base station is generally not a problem because it is powered from the commercial power mains and situated where a gain antenna can be used. This is contrasted to the subscriber unit which must be battery operated and physically small which puts severe restrictions on transmitter power and antenna gain. With these limitations in mind, the system design can proceed. The system gain available to cover the link loss is found by comparing the EIRP, or effective isotropic radiated power available from the transmitting end of the link to the effective receiver sensitivity at the receiving end of the link. The EIRP is found by multiplying the transmitter power output in watts by the

transmitting antenna gain expressed as an algebraic ratio with an isotropic antenna assumed to have a gain of one. Usually it is easier to express the transmitter power in dBm, decibels above one milliwatt, and add the antenna gain in dBi, or decibels above an isotropic antenna. As an example, suppose a transmitter has an output of 1 watt (+30 dBm) and is connected to an antenna with a gain of 2 (+3 dBi). The EIRP is then given by

$$\text{EIRP} = 1 \text{ watt} \times 2 = 2 \text{ watts}$$

or in the more commonly used logarithmic terms,

$$\text{EIRP} = +30 \text{ dBm} + 3 \text{ dB} = +33 \text{ dBm}$$

Sensitivity of a receiver is the amount of input signal that must be applied to the receiver input to produce a specified signal-to-noise ratio (or bit-error-rate) at the output. The effective sensitivity at the receiving end of the link is found by dividing the receiver sensitivity in microvolts by the receiving antenna gain expressed as an algebraic ratio. Once again, it is usually easier to perform this calculation with numbers expressed as decibels. In this case, the effective receiver sensitivity is the receiver sensitivity in dBm minus the antenna gain in dBi. For example, suppose a receiver has a sensitivity of -116 dBm and is connected directly (no transmission line loss) to an antenna with a gain of 2 dBi. The effective receiver sensitivity is

$$\text{Sens}_{\text{eff}} = -116 \text{ dBm} - 2 \text{ dB} = -118 \text{ dBm}$$

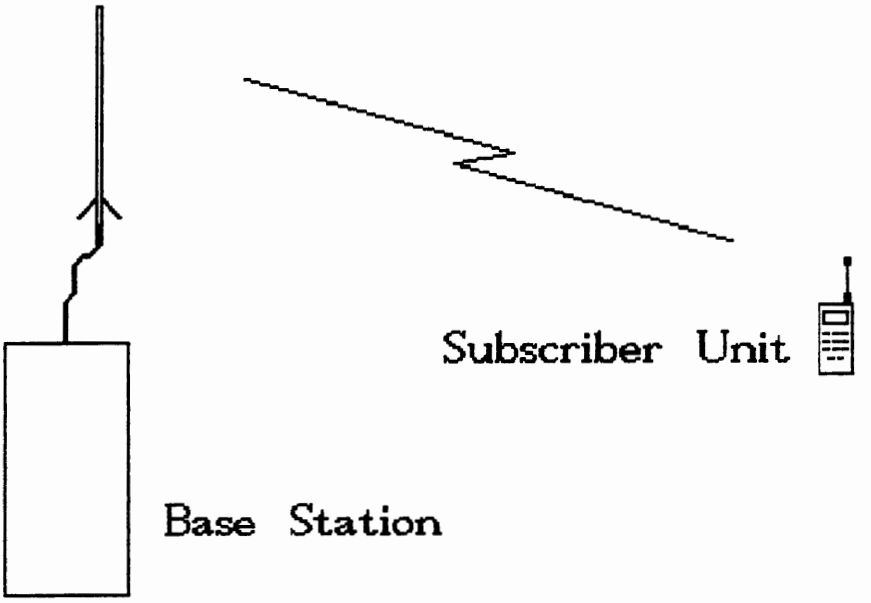
Once the EIRP and effective receiver sensitivity are known, the system gain is found as the difference between the EIRP and the effective receiver sensitivity. With the values from above, the system gain is found as

$$\text{System Gain} = +33 \text{ dBm} - (-118 \text{ dBm}) = 151 \text{ dB}$$

Next the calculation is repeated in the opposite direction. The receiving end of the link is now the transmitting end and vice versa. The goal of the system planner is to have these two numbers for system gain as close to equal as possible. Suppose that the base station to subscriber unit system gain is 170 dB and the subscriber unit to base station system gain is 160 dB. Under these conditions the subscriber unit can hear the base station at a greater distance than the base station can hear the subscriber unit. To the customer this problem would be apparent as areas where the subscriber unit could hear the base station but be unable to initiate calls.

Shown in Fig. 1 is a good example of system gain planning. An example of bad planning is shown in Fig. 2. To correct the situation in Fig. 2, the system designer might want to reduce the base station power, reduce the base station antenna gain, increase the subscriber unit receiver sensitivity, increase the

subscriber unit antenna gain, or probably some combination of these.



Antenna Gain	+6 dBi
TX Power	+30 dBm
RX Sensitivity	-119 dBm

Antenna Gain	+6 dBi
TX Power	+27 dBm
RX Sensitivity	-116 dBm

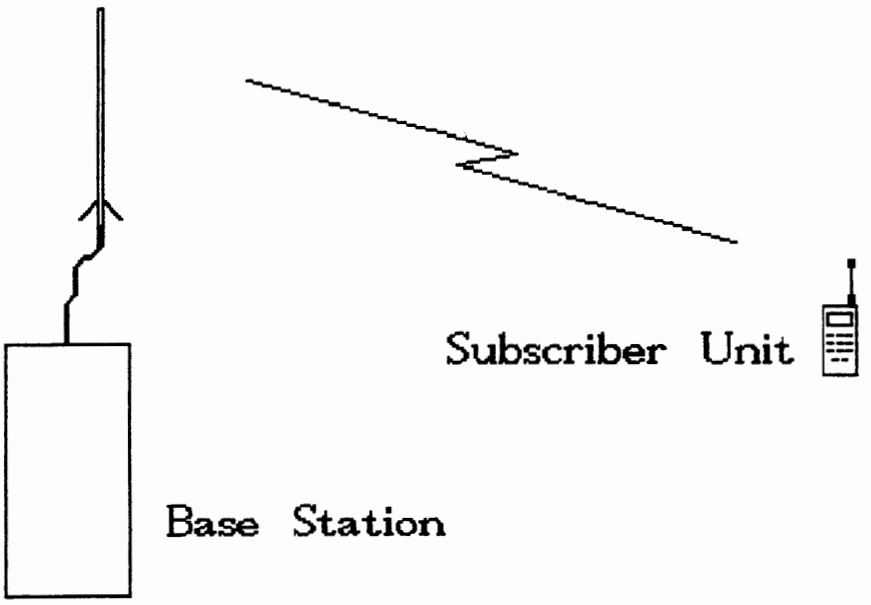
Base to Subscriber Unit

TX Power	+30 dBm
TX Antenna Gain	+6 dBi
TX EIRP	+36 dBm
RX Antenna Gain	0 dBi
RX Sensitivity	-116 dBm
RX Sens eff	-116 dBm
System Gain	152 dB

Subscriber Unit to Base

TX Power	+27 dBm
TX Antenna Gain	0 dBi
TX EIRP	+27 dBm
RX Antenna Gain	+6 dBi
RX Sensitivity	-119 dBm
RX Sens eff	-125 dBm
System Gain	152 dB

Fig. 1



Antenna Gain	+10 dBi
TX Power	+37 dBm
RX Sensitivity	-120 dBm

Antenna Gain	0 dBi
TX Power	+27 dBm
RX Sensitivity	-116 dBm

Base to Subscriber Unit

TX Power	+37 dBm
TX Antenna Gain	+10 dBi
TX EIRP	+47 dBm
RX Antenna Gain	0 dBi
RX Sensitivity	-116 dBm
RX Sens eff	-116 dBm
System Gain	163 dB

Subscriber Unit to Base

TX Power	+27 dBm
TX Antenna Gain	0 dBi
TX EIRP	+27 dBm
Rx Antenna Gain	+10 dBi
RX Sensitivity	-119 dBm
RX Sens eff	-129 dBm
System Gain	156 dB

Fig. 2

III. *REDUCING THE EFFECTS OF INTERFERENCE*

Interference rejection is required to protect users of a channel from undesired signals that appear on channel, i.e., other users, interference sources appearing on adjacent channels, and interference such as intermodulation and spurious responses that arise from nonlinearities internal to the equipment.

A. *CO-CHANNEL INTERFERENCE*

The problem of interference from other users on the same frequency can be reduced by allowing sufficient distance between areas where frequencies are reused. The coverage area of each base station should be studied thoroughly and enough separation margin should be designed in to allow for interference-free reuse of the channels. Another factor to consider is the co-channel rejection of the receiver. The co-channel rejection capability of a receiver is a measure of the receiver's ability to receive a desired on-channel signal at a certain level with a minimal specified degradation in output signal-to-noise ratio (or bit-error-rate) in the presence of an undesired signal on the same channel [2]. Co-channel rejection is usually specified as the difference in decibels between the two signals with a low number being desirable. Unfortunately, the system designer is not entirely free to specify this. It is largely a function of the type of detector used to demodulate the received signal. However, it is important to keep the concept in mind and if the choice is possible, specify units with low co-channel specification.

B. *ADJACENT CHANNEL INTERFERENCE*

Interference sources that appear on adjacent channels can manifest themselves in one of two ways. If a receiver is receiving a signal on one frequency and a signal appears on another frequency the selectivity of the receiver rejects the undesired signal. A typical subscriber unit might have selectivity of 70 dB. As long as any off-frequency signal is less than 70 dB above the sensitivity point of the receiver there is no problem. The receiver can not reject unwanted signals more than 70 dB above sensitivity and these signals appear at the detector along with the desired signal and create interference. To counter this, the system engineer might want to specify a high selectivity specification for the unit. Unfortunately it may not be feasible from a cost standpoint to specify selectivity any higher than absolutely necessary.

C. *SPURIOUS AND INTERMODULATION INTERFERENCE*

The second way that off-channel signals can create interference is by mixing in the nonlinear stages of the unit. Any nonlinear component can be represented by an infinite power series relating the output to the input [3]. For simplicity, if two undesired signals are applied to a nonlinear circuit, the output will be of the form

$$f_{spurious} = Mf_1 \pm Nf_2$$

where M and N are integers. Any response created in this manner is a spurious response. The most severe product is the third

order intermodulation product which occurs when M = 2 and N = 1 or when M = 1 and N = 2. In a channelized system third order intermodulation causes undesired signals at one and two channel spacings away from the desired signal to mix and produce an interfering output on the desired frequency. In fact, the undesired signals can lie at any integral multiple of one and two channel spacings from the desired signal. Fig. 3 shows two signals being applied to a nonlinear circuit and the output containing the two signals and the undesired third order products. When one of the undesired products falls on the operating channel of the radio, it interferes with the desired communication and the radio is said to suffer from IM distortion.

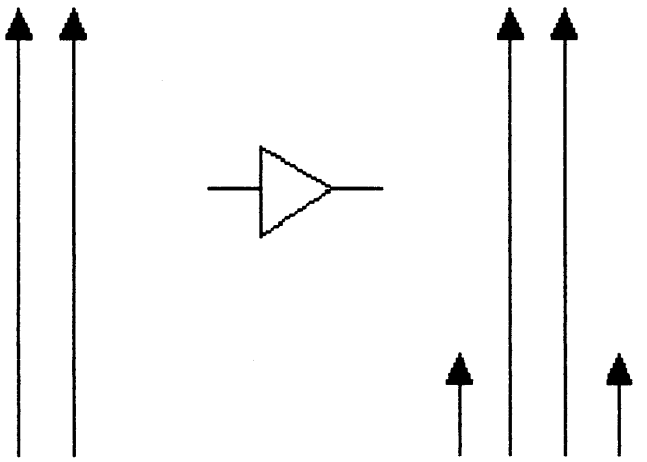


Fig. 3

This is another area where the obvious solution to specify better performance is not as simple as it seems. The system engineer needs to keep in mind the tradeoffs that occur when trying to make the system less susceptible to third order intermodulation distortion. Providing a higher level of rejection to this interference almost always requires that the active circuits in the equipment be capable of handling larger signals. This means higher operating voltage and current. While this isn't too severe a problem in a base station, it is a serious problem in a lightweight battery powered subscriber unit. Where does the designer make the tradeoff between interference rejection and

battery lifetime? Minimizing spurious responses while conserving operating current requires creative design.

IV. *CONCLUSION*

The design of a wireless communications system is a complicated undertaking. Good coverage and freedom from interference are two of the major items that must be addressed if the system is to be successful. This paper has attempted to present a brief look at the key points to be considered when planning a system to ensure balanced coverage and to minimize interference. By keeping these points in mind, the system planner will have a better chance of getting the system right the first time.

V. *REFERENCES*

[1]. W. C. Y. Lee, *Mobile Communications Design Fundamentals*. Indianapolis, IN: Howard W. Sams and Co., 1986, pp. 49-95.

[2]. EIA/TIA Specification Number TR45.3, Project Number 2216, March 1991, p. 24.

[3]. Franz McVay, "Don't Guess the Spurious Level," *Electronic Design*, February 1, 1967.

A 2 GHz BiCMOS Low-Noise Amplifier and Mixer

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National Semiconductor

Wireless Communications Group

Abstract

A low-noise amplifier and mixer IC has been designed for wireless communication applications operating at frequencies up to 2 GHz. The integrated device is fabricated in a BiCMOS process with bipolar device f_T's of 15 GHz and 0.8 μm CMOS channel lengths. The amplifier provides 16.4 dB of gain with a 2.8 dB noise figure at 1GHz. The Gilbert-cell mixer operates with 3.9 dB of conversion gain and a 3rd-order output intercept point of 1dBm. Total supply current for the LNA and mixer is 16.9 mA, and less than 1 μA in power-down mode.

I. INTRODUCTION

Virtually all wireless receivers include amplification and frequency conversion stages. Small form-factor battery-operated personal communications devices will continue to depend on low-power active circuits with increasing levels of integration. This paper describes a silicon integrated circuit that includes a low-noise amplifier (LNA) and a mixer. The IC provides a power-down function to help reduce current consumption in low duty cycle applications. The circuit operates with input frequencies up to 2 GHz, and can provide IF output frequencies up to 1 GHz. Signal inputs and outputs are matched to 50 Ohms over the range of operation, and circuit performance is compatible with current communications standards such as DECT [1]. Previous monolithic silicon devices that combine LNA and mixer functions on a single die do not cover this frequency range.

II. PROCESS DESCRIPTION

The LNA/ mixer IC is fabricated in a single-poly, oxide-isolated BiCMOS process [2] which is suitable for high-frequency mixed analog and digital circuits. Active device cross-sections are shown in Fig. 1. Minimum CMOS drawn gate length is 0.8 μm and bipolar NPN devices have 15 GHz f_T. Typical device parameters are given in Table 1. Also, the process includes low-parasitic capacitance polysilicon resistors and area-efficient capacitors. The completed die uses two metal interconnect layers. A photograph of the die is shown in Fig. 2.

III. LOW-NOISE AMPLIFIER

A. Circuit design

Fig. 3 shows the LNA schematic diagram. Shunt feedback lowers the input impedance of the common-emitter stage to create a nominal 50-Ohm input match without causing severe noise figure degradation [3]. In designing the LNA, the goal was an acceptable compromise among the various performance requirements, as a strong interdependency exists between several performance parameters. To achieve noise figure requirements, Q_1 must be scaled so as to have a low base resistance, since the r_b of Q_1 is the largest single noise source in the amplifier. A large input device, however, operates at low current density and has increased parasitic capacitances so that the

f_T	15 GHz
C_{jeb}	3.3 fF
C_{jcc}	2.9 fF
β	90 A/A
L_{eff} (MOS)	0.6 um
V_{TN}	0.75 V
V_{TP}	0.95 V

Table 1. Typical Device Parameters

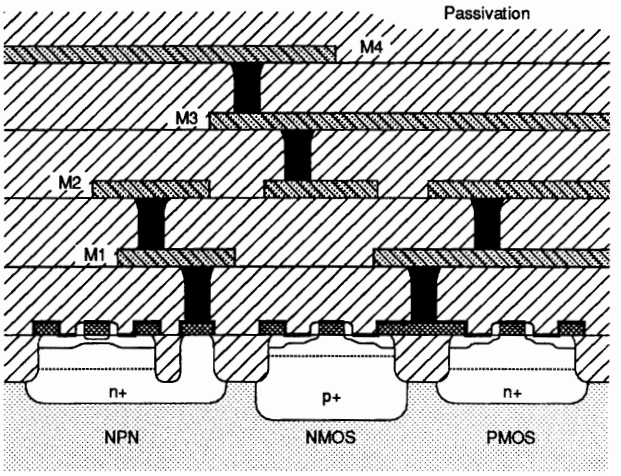


Fig. 1 - NPN and CMOS device cross-sections

speed of the device is sub-optimal. For these reasons, a large input device is in direct conflict with gain-bandwidth and input VSWR requirements. Supply current requirements add another dimension to the design compromise, as bias levels will affect all of the performance parameters mentioned here, in addition to directly determining maximum signal levels and related linearity parameters such as P_{1dB} and OIP_3.

A simple but effective power-down feature is implemented through the use of a large PMOS switch, M_1. During operation the switch is closed to provide bias to the amplifier. In power-down mode, the switch is open and the supply current drawn by the amplifier is determined by the leakage current of the switch, which is well below 1μA. Typical turn-off and turn-on recovery times are in the range of 100ns, and are determined primarily by the size of the external coupling capacitors, which experience some charging and discharging as the amplifier is cycled through power-down.

Fig. 2. Die Photograph

Supply Vcc	5	V
Icc, on	7.9	mA
Icc, off	< 1	uA
Max. Input Freq.	2	GHz
Gain, 1GHz	16.4	dB
P1dB Out, 1GHz	-7.4	dBm
OIP3, 1GHz	3.3	dBm
Noise Figure, 1GHz	2.8	dB
Inp. Return Loss	12.1	dB
Out. Return Loss	13.6	dB

Table 2. LNA Characteristics

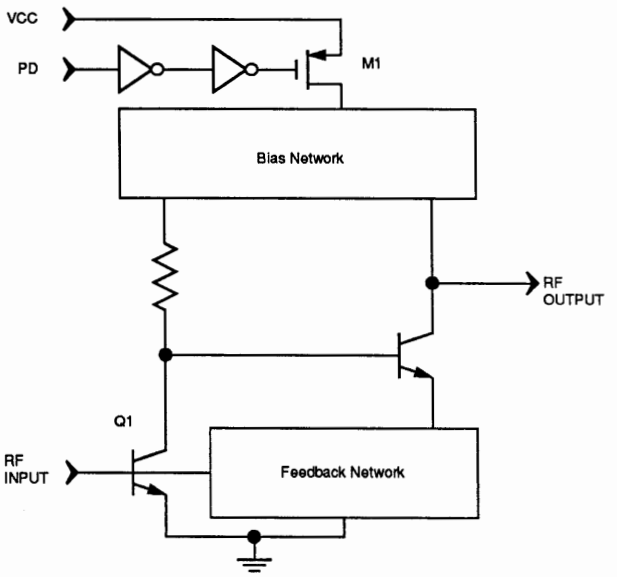


Fig. 3. LNA Schematic

B. Measured Results

Table 2 presents a summary of measured performance parameters for the LNA [4]. Amplifier supply current is 7.9 mA with a 5.0 Volt supply. Fig. 4 shows gain of the amplifier versus frequency, and illustrates the broadband behavior of the device. The amplifier provides usable gain beyond 2 GHz, and at DECT frequencies (1.9 GHz), the amplifier gain is 13.5 dB. Fig. 5 shows noise figure versus frequency. As transistor gain drops with increasing frequency, noise figure gradually increases. Noise figure is 3.8 dB at 1.9 GHz.

Fig. 4. LNA Gain vs. Frequency

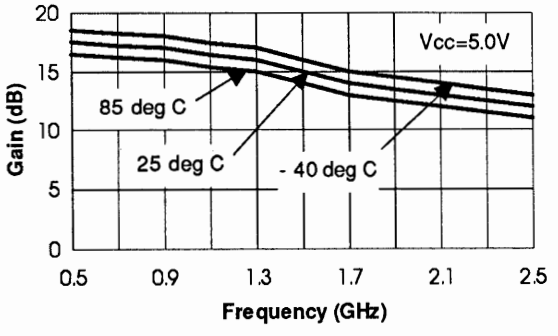
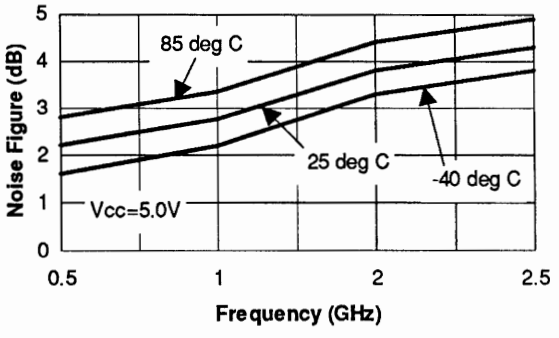


Fig. 5. LNA Noise Figure vs. Frequency



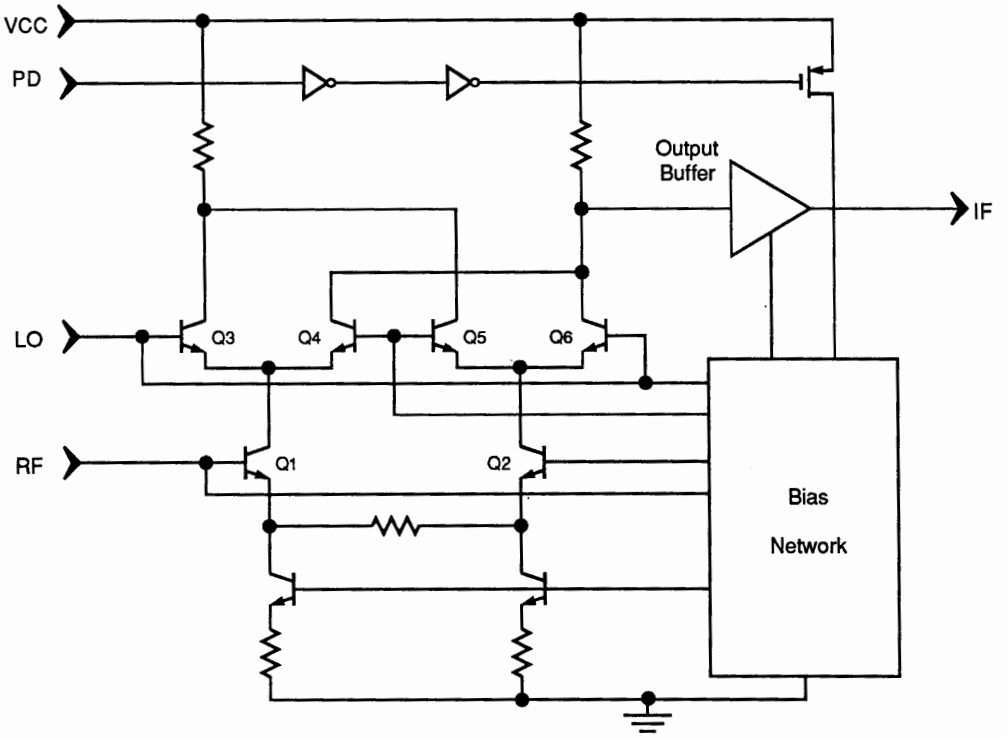


Fig. 6. Mixer Schematic

IV. MIXER

A. Circuit design

Fig. 6 shows the schematic of the mixer circuit. The mixer is based on a Gilbert cell. Although a circuit of this type inherently operates in a differential manner, the circuit has been configured with single-ended inputs and outputs since this is the most convenient mode of operation for most applications. Single-ended I/O's avoid the use of balun devices which may add significant cost to the receiver, and help simplify circuit board layout by reducing the number of signal-carrying traces that must be routed. Transistors Q_1-Q_6 compose the Gilbert cell and an output buffer matches the multiplier output to the 50 Ω load. Other transistors provide biasing. Broadband input terminations for the RF and LO inputs are accomplished by means of on-chip terminating resistors and on-chip DC blocking capacitors. The inputs are effectively matched to 50 Ω at frequencies above 100 MHz. The IF output impedance is determined by the output impedance of the output buffer, which is approximately 50 Ω up to frequencies in excess of 1 GHz.

Power-down for the mixer is again accomplished through the use of MOS switches. During power-down the switches disable all biasing and supply current is limited to device leakage currents, which are well below 1 μA. As for the LNA, typical turn-off and turn-on recovery times are 100-200 ns, and are dependent on external blocking capacitor values.

Supply Vcc	5	V
Icc, on	9	mA
Icc, off	< 1	uA
Max. Input Freq.	2	GHz
Conversion Gain, 1GHz RF, 110 MHz IF	3.9	dB
P1dB Output, 110MHz IF	- 8.2	dBm
OIP3, 110MHz IF	0.9	dBm
Noise Figure (SSB), 1.9GHz	21	dB
LO to RF isolation, 1GHz	33	dB
LO to IF isolation, 1GHz	28	dB
RF Return Loss, 1GHz	22.9	dB
LO Return Loss, 1GHz	25	dB
IF Return Loss, 1GHz	15.4	dB

Table 3. Mixer Characteristics

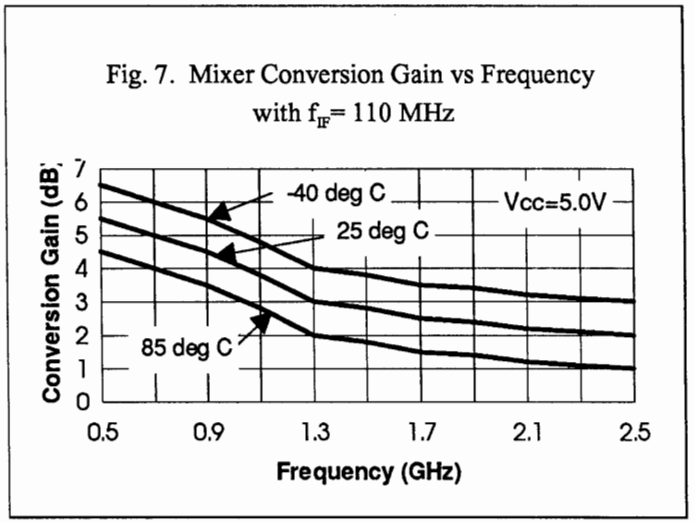


Fig. 7. Mixer Conversion Gain vs Frequency with f_{IF}= 110 MHz

B. Measured Results

Table 3 summarizes measured performance parameters for the mixer. Supply current for the mixer is 9.0 mA with a 5.0 V supply. As shown in Fig. 7, the mixer provides conversion gain up to and beyond 2 GHz. Conversion gain is 2.3 dB at 1.9 GHz.

V. CONCLUSION

A single-chip BiCMOS low-noise amplifier and mixer has been described. The IC has been designed for ease-of-use in a variety of applications at frequencies up to 2 GHz. Fabricated in an advanced BiCMOS process, the circuit takes advantage of bipolar device performance in critical signal paths, and makes use of CMOS devices to create convenient biasing and power-down features.

VI. ACKNOWLEDGMENTS

Andy Dao and Don Ferris provided characterization data for the IC. Also, the Wireless applications and design staff contributed through helpful suggestions and discussions. All contributions are gratefully acknowledged.

VII. REFERENCES

[1] ETSI, European Telecommunications Standard ETS 300 175-1: "Digital European Cordless Telecommunications (DECT) Common Interface Part 2: Physical Layer".

[2] A. Iranmanesh, V. Ilderem, M. Biswal, B. Bastani, "A 0.8μm Advanced Single-Poly BiCMOS Technology for High-Density and High-Performance Applications", *IEEE J. Solid-State Circuits* (1991) 422-426.

[3] I. Kipnis, J. F. Kukielka, I. Wholey, and C. P. Snapp, "Silicon bipolar fixed and variable gain amplifier MMIC's for microwave and lightwave applications up to 6 GHz", *IEEE MTT-S Dig.* (1989) 109-112.

[4] LMX2215 data sheet, National Semiconductor, to be published.

High Efficiency Crystal Oscillator at High Frequencies

Sheng H. Lee and Alvin K. Wong, Philips Semiconductors

***Abstract*— For the new 900 MHz wireless market, designers are required to implement a much higher front IF frequency. As a result, a new type of high frequency crystal oscillator has been created. This new circuit overcomes the heavy bias and difficult tuning problems associated with the conventional Colpitts crystal oscillator at frequencies above 60 MHz. The result is an oscillator with minimum bias current and flexible tuning capability.**

I. INTRODUCTION

In the past, while there were many proposals made to modify the basic Colpitts crystal oscillator circuit to extend its usable frequency range above 60 MHz, none of them has ever addressed the issue of how to accomplish the goal with minimum current draw. This is of paramount importance when one considers the ever shrinking hardware as well as battery sizes. Therefore, the original Colpitts oscillator model was revisited to determine the factors that cease the oscillation at high frequencies, and develop an elegant solution to counter the negative force. The result is a 95.55 MHz crystal oscillator using a scant 0.2 mA current, yet generating 300 mV_{RMS} signal at the mixer load. The active device is from the NE605 receiver IC, which has a compatible built-in LO stage with the same bias current. In the discussions below, the design steps and their associated equations are listed, but the mathematical derivations are not included.

II. CIRCUIT ANALYSIS

A. Universal Circuit Model

Any linearized, time-invariant circuit can be reduced to a parallel L/C/R circuit if the bandwidth of interest is small and, depending on the value of R, the time-domain waveform will vary significantly, which is shown in Fig. 1.

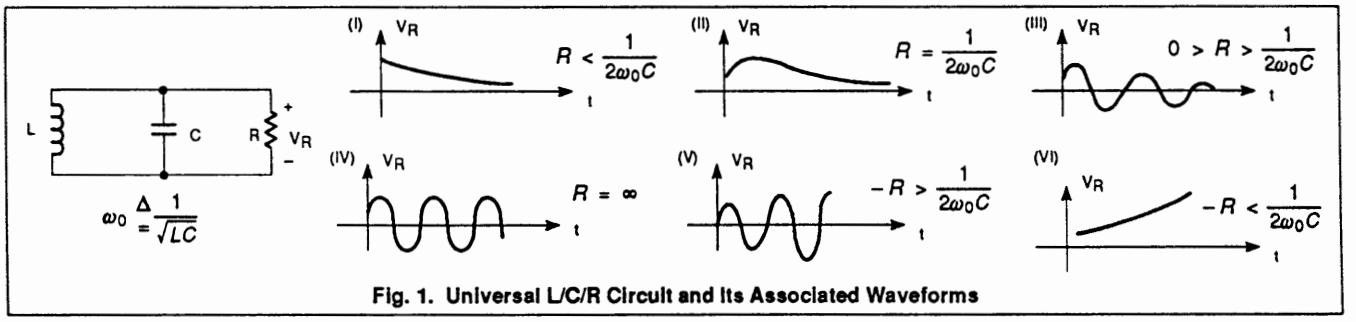


Fig. 1. Universal L/C/R Circuit and Its Associated Waveforms

It is obvious that only negative resistance can meet the start-up condition of oscillation. This is possible because the negative resistance is generated by the device that has an amplitude-dependent gain, so regardless of whether the amplitude builds up from Fig. 1, category (V) or (VI), it would wind up with category (IV) in equilibrium.

B. Basic Oscillator Model

A typical L/C type Colpitts oscillator using Philips Semiconductors NE605 and its simplified AC schematic diagram is shown in Fig. 2.

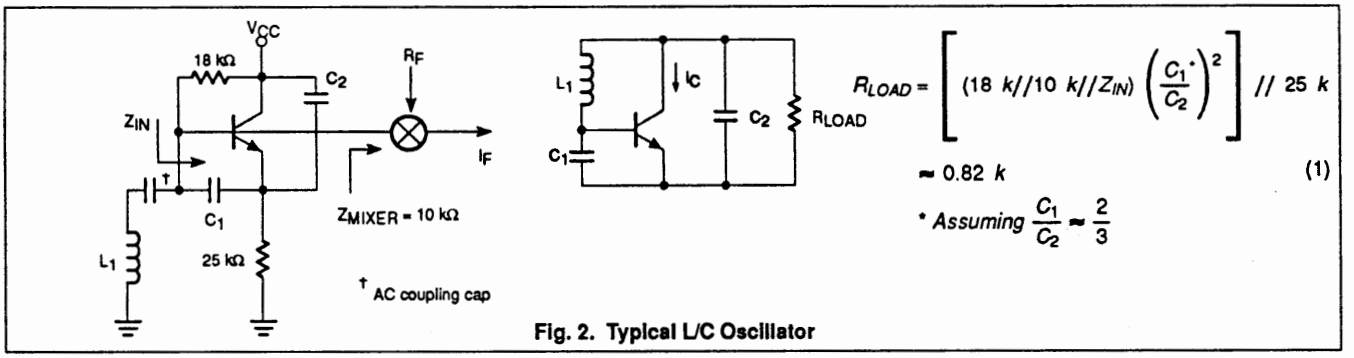


Fig. 2. Typical L/C Oscillator

Typically the device has a default bias current of 0.2 mA and an estimated AC current gain of 20 at 95.55 MHz, with a resultant input impedance (Z_{IN}) of 2.6 kΩ for the device. Therefore, we can assume that

$$Z_{IN} \gg \frac{1}{\omega\ C_1} \tag{2}$$

$$(18k//10k) \gg \omega\ L_1 \tag{3}$$

without losing the generality, the circuit can be further reduced to new equivalent circuit in Fig. 3.

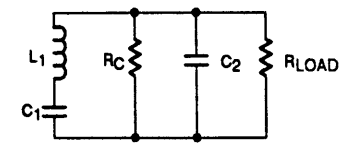


Fig. 3. Equivalent Circuit for L/C Oscillator

where the device output impedance is given by

$$R_C \underset{=}{\Delta} \frac{V_{C2}}{i_C} = \frac{-C_1}{G_m C_2} \tag{4}$$

and the transconductance at room temperature is defined as

$$Gm = \frac{I_{DC}}{26} \tag{5}$$

where I_{DC} is in [mA] and G_m is in [S].

Comparing this circuit to that from Fig. 1, we conclude the condition for oscillation:

$$\frac{C_1}{GmC_2} < R_{LOAD} \tag{6}$$

and, by default, the frequency of oscillation is

$$\omega_0 L_1 = \frac{1}{\omega_0 C_1} + \frac{1}{\omega_0 C_2} \tag{7}$$

In general designers can choose the condition of

$$\frac{C_1}{G_m C_2} \ll R_{LOAD} \tag{8}$$

if the maximum output power is preferred over the minimum distortion. The same circuit can also be viewed from a different angle using the phasor diagram as shown in Fig. 4, which clearly demonstrates the creation of negative resistance from the device due to the out-of-phase condition between V_{C1} and V_{C2}.

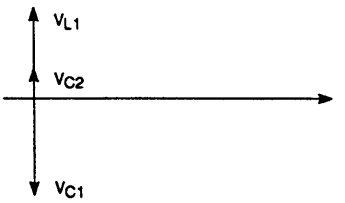


Fig. 4. Phasor Diagram for L/C Oscillator

C. Crystal Oscillator Model

So far an ideal oscillator model has been discussed and the only limitation on the frequency of oscillation is the G_m factor from the device. This is why 20 GHz oscillator, using the transistor as the active device, is feasible when high quality L/C components (or their equivalents) are used. But this is no longer true when the crystal is substituted for the inductor regardless of the frequency performance of the device. In order to fully understand the impact of the crystal, the previous simplified model will be extended by adding a resistor in series with the inductor L_1 as shown in Fig. 5 and its associated phasor diagram in Fig. 6.

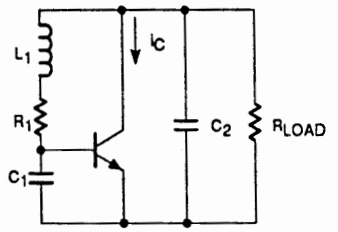
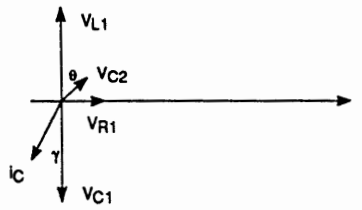


Fig. 5. Simplified Crystal Oscillator Model



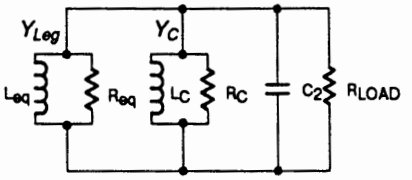
$$\text{where } i_C \triangleq |G_M| e^{-j\gamma} V_{C1} \tag{9}$$

γ : Phase lag of the device output current which is about 20° at 95.55 MHz

$$\tan\Theta \triangleq \frac{R_1}{\omega L_1 - \frac{1}{\omega C_1}} \tag{10}$$

Fig. 6. Phasor Diagram for Crystal Oscillator

Judging from the relative phase relationship between V_{C2} and i_C, we know the device output admittance is complex and both its real and imaginary parts are negative if $\gamma < \theta$. The equivalent circuit and the governing equations are shown in Fig. 7.



$$R_{eq} = \frac{R_1}{\sin^2\Theta} \tag{11}$$

$$L_{eq} = \frac{2R_1}{\omega \sin 2\Theta} \tag{12}$$

$$R_C = \frac{-\omega C_1}{|G_m Y_{Leg}| \cos(\Theta - \gamma)} \tag{13}$$

$$L_C = \frac{C_1}{|G_m Y_{Leg}| \sin(\Theta - \gamma)} \tag{14}$$

Fig. 7. Equivalent Circuit for Crystal Oscillator

D. Advanced Crystal Oscillator Model

Since part of the precious power is being converted to the inductance instead of the much needed negative resistance, the ability for the device to oscillate is diminished due to the conservation of energy. Therefore, an inductor L_2 is added in the base of the device to realign V_{C2} and i_C out of phase. The new schematic diagram, the associated phasor, its equivalent circuit as well as key design equations are shown in Fig.s 8, 9 and 10, respectively.

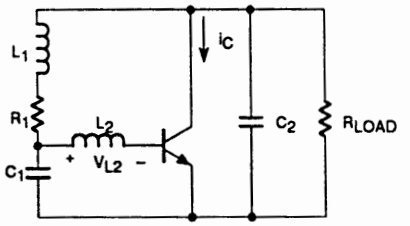
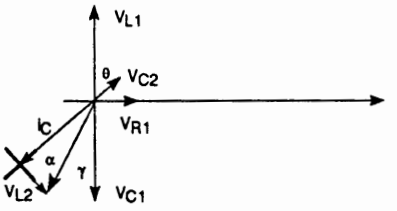
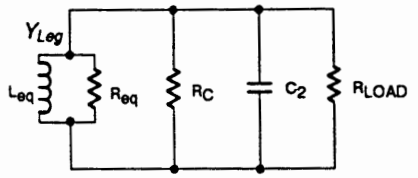


Fig. 8. Proposed New Crystal Oscillator Model



$$\text{where } \Theta \triangleq \alpha + \gamma \tag{15}$$

Fig. 9. Phasor Diagram for New Crystal Oscillator



$$R_C = \frac{-R_1\omega C_1}{|G_M|\sin\Theta\cos\alpha} \quad (16)$$

$$\tan\alpha = \frac{\omega L_2}{Z_{IN}} \quad (17)$$

Fig. 10. Equivalent Circuit and Design Equations

One very important aspect of the results from Eq. (16) is that when ω increases, R_C decreases in value. Since θ is a function of ω, it also influences the R_C value, although to a lesser degree. This explains why a 100 MHz crystal oscillator is more difficult to build than a 1 GHz L/C type oscillator. In general, R_{LOAD} is much greater than R_{eq}, when the crystal is in place, so the condition for oscillation can be derived from Eq. (11) and Eq. (16), and is as follows:

$$\frac{|G_m|}{\omega_0 C_1} > \frac{\sin\theta}{\cos\alpha} \quad (18)$$

And the frequency of oscillation becomes

$$\omega_0 L_{eq} \underset{=}{\Delta} \frac{1}{\omega_0 C_2} \quad (19)$$

III. EXAMPLE FOR LOW-POWER CRYSTAL OSCILLATOR AT 95.5 MHZ

Now we will show how to apply the theory to build a 95.55 MHz crystal oscillator. First, a model for the crystal is presented in Fig. 11.

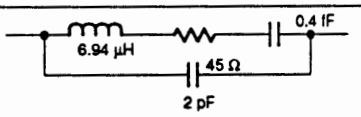


Fig. 11. 95.545 MHz Crystal Model

Eq. (12) and Eq. (19) can thus be combined to give

$$C_2 = \frac{\sin 2\theta}{2\omega_0 R_1} \leq \frac{1}{2\omega_0 R_1} = 18.5\ pF \quad (20)$$

A standard value of 15 pF is chosen for C_2, which results in 27° for θ. After substituting values for α and θ in Eq. (18), the upper bound for C_1 is as follows:

$$C_1 < \frac{|G_M|\cos\alpha}{\omega_0 \sin\theta} = 28\ pF \quad (21)$$

In the meantime, Eq. (1) and Eq. (8) give a loose lower bound of

$$C_1 \gg \frac{C_2}{1800|G_M|} = 1\ pF \quad (22)$$

versus another loose lower bound from Eq. (2) for C_1

$$C_1 \gg \frac{1}{Z_{IN}\omega} = 0.64\ pF \quad (23)$$

The final value for C_1 is selected to be 10 pF after considering the constraints from Eq. (21), Eq. (22) and Eq. (23). Furthermore, since the crystal operates at the higher overtone mode, it is necessary to suppress the lower order oscillations by substituting parallel L/C for C_2. As for the value of L_2, 537 nH is required based on Eq. (17), however only the standard value of 560 nH will be used for the final circuit.

The final finished part using the Philips Semiconductors NE605 as the active device is shown in Fig. 12, which operates at a scant 0.2 mA current by default.

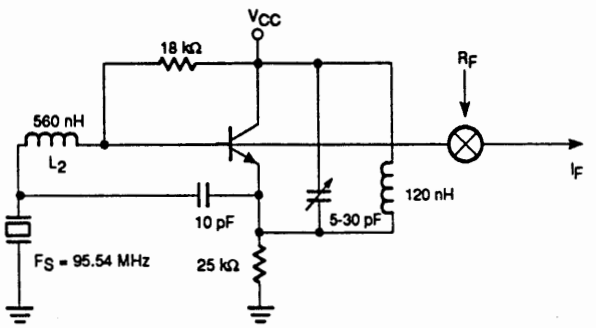


Fig. 12. Example for 95.55 MHz Crystal Oscillator

As confirmation, the same oscillator is tested with and without the added inductor L2 while the DC power is turned on and off. In Fig. 13 we can see that the effect of Y_C is quite inductive and almost pushes the trace along the constant conductance circle and only generates 70 mV_{RMS} at the emitter after the alignment. The output voltage can be increased to 220 mV_{RMS}, however, if the bias current is raised from 0.2 mA to 1 mA. On the other hand, in Fig. 14 the trace was pushed along the real axis to the negative resistance region and reaches 220 mV_{RMS} at the emitter after the alignment. The base voltage is about 300 mV_{RMS} in this case, which is consistent with the values of C_1, cos α and C_2. Moreover, the tuning sensitivity in Fig. 13 is so high that only a narrow range of capacitance for C_2 can make the circuit oscillate, while the circuit from Fig. 14 is so flexible that the output voltage only changes gracefully if the capacitance for C_2 is varied over a broad range. This is fully expected because if the circuit oscillates, the frequency is always close to F_S for a crystal oscillator. So the value of L_{eq} in Eq. (10) must be self-adjusted to nullify L_C from Eq. (12), which can be out of the range if L_C and C_2 already resonate much above F_S. In another experiment, the value of C_1 was increased gradually and the oscillation stopped when C_1 exceeded the limit, 28 pF, set by Eq. (21).

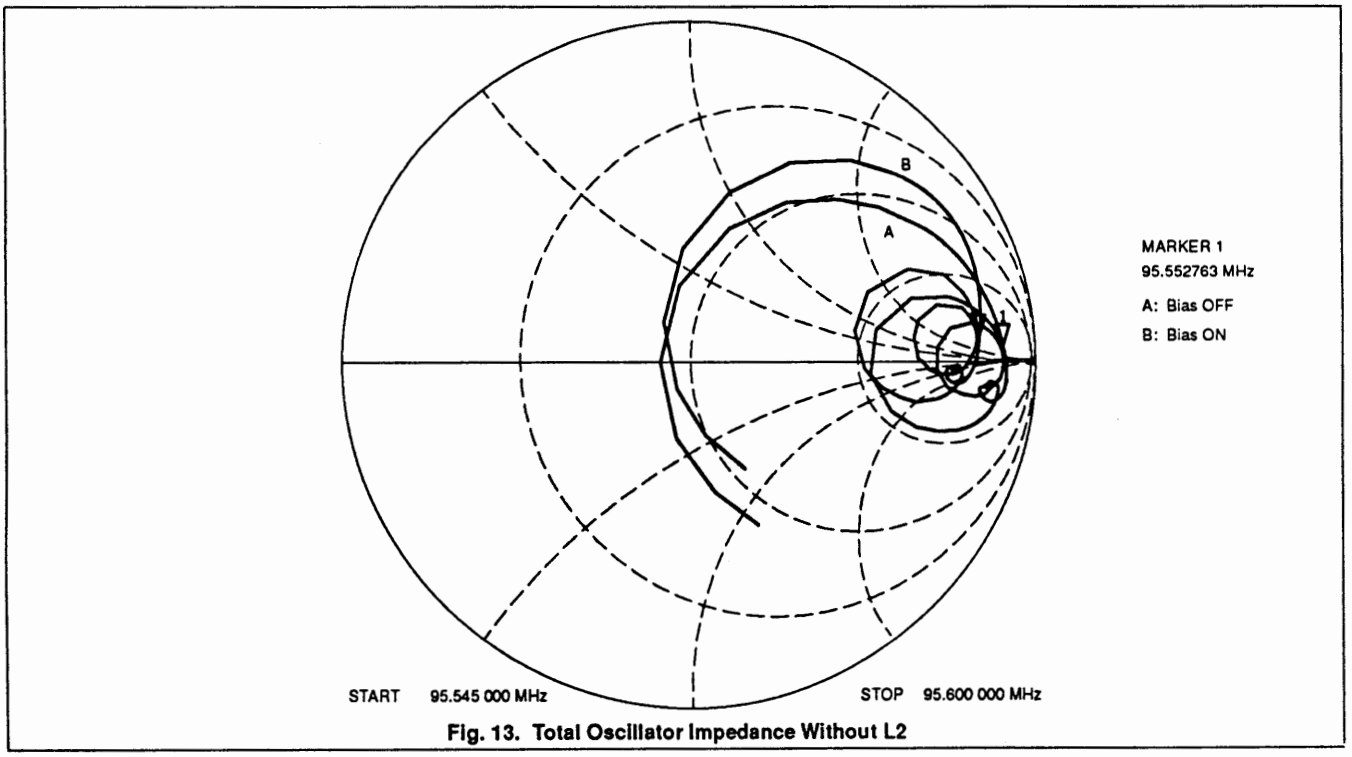


Fig. 13. Total Oscillator Impedance Without L2

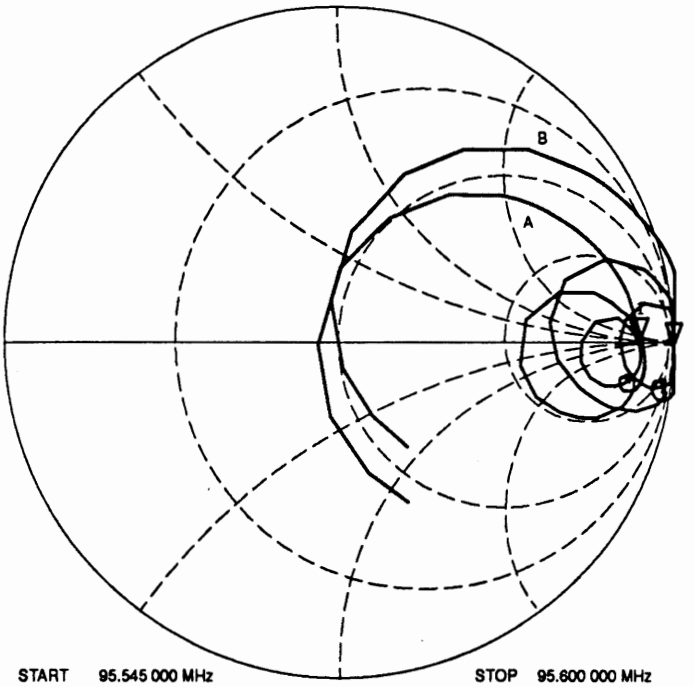


Fig. 14. Total Oscillator Impedance With L2

IV. CONCLUSIONS

In conclusion, an elegant solution is proposed by inserting an inductor in the base of the device for the classic Colpitts oscillator. This extends the margin for oscillation at frequencies above 60 MHz without resorting to the customary solution of increasing the bias current. The result is an oscillator which easily achieves strong output power, at the same time affording 80% current savings. This leads to longer battery life and lower production cost for the portable set.

V. ACKNOWLEDGEMENTS

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A 2.2 GHz PLL Frequency Synthesizer

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Abstract - A 2.2 GHz monolithic integrated circuit PLL frequency synthesizer for DECT cordless, PCN, WPABX, and WLAN applications is described. The low power circuit operates at 2.7v and 12mA with standby currents of less than 100 µA. The chip features a selectable 64/65 or 128/129 dual-modulus prescaler, an internally regulated charge pump with tristate capability, and a microcontroller compatible serial data interface. The circuit is fabricated on a 0.8 µm BiCMOS process with 15 GHz fT bipolar transistors.

I. INTRODUCTION

PLL frequency synthesizers are used prevalently today as electronic tuners in radios, TVs, and phone systems. These synthesizers, as shown in Fig. 1, take a stable reference signal (crystal oscillator) and in conjunctions with an external Voltage Controlled Oscillator (VCO) generate local oscillator (L.O.) signals using phase locked loop techniques [1]. The integrated synthesizer being reported in this paper is particularly well suited for battery applications at 2 GHz because of its low phase noise, low power, and low spurious attributes. Though not the lowest power solution to date at this frequency [2], this device represents a higher level of integration and performance than previously available.

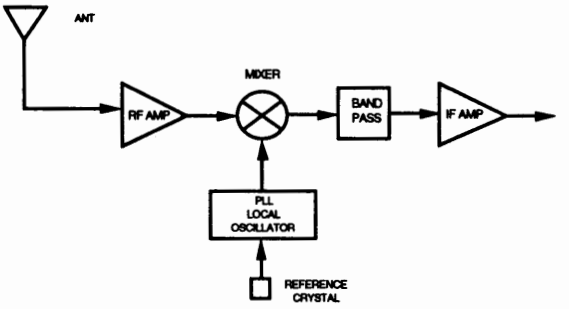

Fig. 1: System Diagram

II. PROCESS DESCRIPTION

This device was fabricated using National Semiconductor's ABIC IV (BiCMOS) process. This process features a 15 GHz fT , .8µ feature sizes, and tungsten plug contacts and resistors. The design utilizes two of the process's four available metal layers and one silicided poly layer. A profile of the process is shown in Fig. 2. The minimum MOS gate and NPN emitter sizes are 1.2 x .8 µm and 1.6 x .8 µm respectively. The metal pitch is 2.5 µm and the 1 µm contacts and vias may be concentrically stacked.

III. CIRCUIT DESCRIPTION

A simplified block diagram of the PLL synthesizer is shown in Fig. 3. It is comprised of a 14 bit reference frequency (R) divider, an 18 bit dual modulus high frequency (N) divider, a serial control register for loading the two counters, and a phase comparator / charge pump block. An external VCO is also used in conjunction with the synthesizer blocks to close the feedback loop.

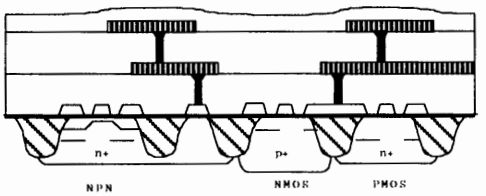

Fig. 2: Process Profile

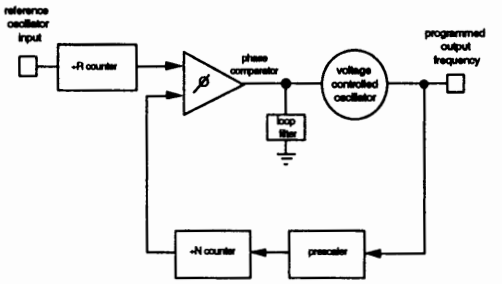

Fig. 3: Synthesizer Logic Diagram

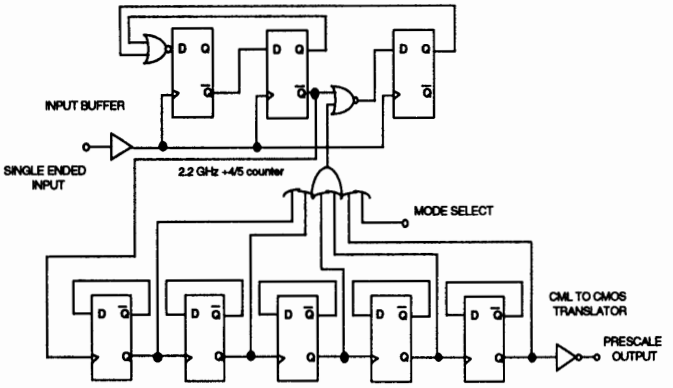

Fig. 4: Prescaler Frontend

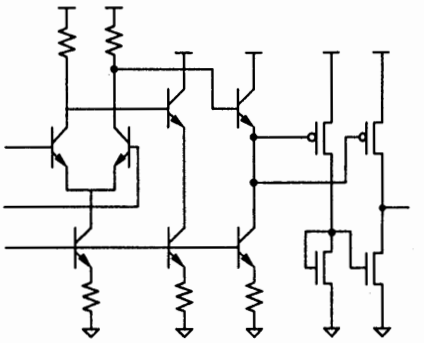

Fig. 5: CML to CMOS Translator

Device operation is attained by first dividing the frequency of a reference signal down to the desired tuning resolution of the system. This tuning resolution is usually some divisible fraction of the spacing between radio channels. The phase comparator drives the frequency of the external VCO in the direction which when divided down by the N counter equals the stepping resolution established by the R counter. The phase comparator accomplishes this by detecting the arrival of phase edges from the two counters and issuing a correction signal to the VCO which is proportional to the difference in their phases. When the phase and frequencies of the two counters outputs' agree, the frequency of the VCO will be the selected N modulus multiple of the tuning resolution.

The R counter is implemented entirely in CMOS and is composed of ripple toggle flip flops drawing less than .5mA at 30MHz The dual modulus N counter is implemented using a selectable bipolar 64/65 or 128/129 prescaler followed by 18 CMOS counter bits [3]. The frontend of the CML prescaler, shown in Fig. 4, consists of a 4/5 divider block followed by 5 toggle CML flip flops and a CML to CMOS translator (Fig. 5). Ninty-five percent of the device's 12 mA typical current budget is consumed in the prescaler as shown in Fig. 6. The current in this block is held constant over its 2.7v to 5.5v range by a bandgap voltage regulator. The 2.2 GHz input buffer provides a sensitivity range of -15 to +6 dBm. The attributes of the bipolar transistors utilized in the frontend are listed in Fig. 7. The device geometries shown in Fig. 8 have emitter areas of 2.56 square microns and are double base stripped.

Block	(μA)
Bandgap	300
CML Toggles	150
Translator	200
OR gate	200
Input Bias	150
4/5 Counter	5300
Input Buffer	4300
CMOS logic	500
Total	12000 μA

Fig. 6: Current Distribution

Parameter	Value
fT (150μA)	15 GHz
emitter area	0.8 x 1.6 μm
Ccs	12 fF
Cbe	5.3 fF
Cbc	10 fF
re	100 Ω

Fig. 7: Device Attributes

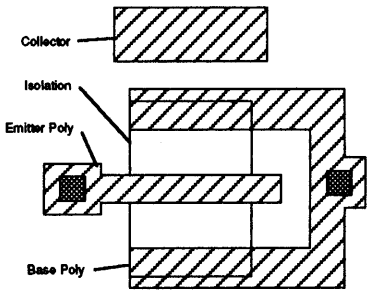

Fig. 8: Bipolar Geometry

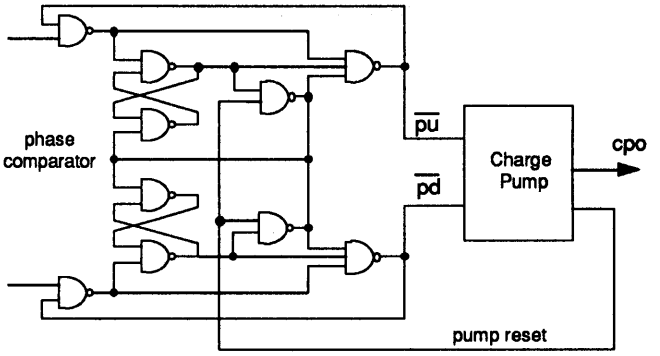

Fig. 9: Phase Comparator Reset Logic

The type-4 digital phase comparator / charge pump block incorporates two features which contribute to its low phase noise and spurious characteristics [4,5]. The first is a deadband elimination circuit, shown in Fig. 9, which ensures that a charge pump dead zone cannot occur near zero phase offset [6]. This technique guarantees that the charge pump generators have in fact responded to the phase comparator before allowing the phase comparator reset logic to activate. Phase comparator deadband is one of the primary sources of jitter in phase locked loops of this type.

The second charge pump feature minimizes reference frequency spurs. Similarity in the current generating structures for the pump up and down circuits ensure that the magnitudes of the pump up and down current sources and the turn on and off times are matched. This matching minimizes the momentary pump up or down excursions on the charge pump line which contribute to VCO FMing at the reference rate. The deadband elimination circuitry inherently also ensures that reference frequency sideband spurs are minimized. The charge pump feedback signals allow the generators on only long enough to eliminate potential deadband yet not contribute any excess active pump time. Excess pump time adds directly to the up or down excursions on the charge pump line by the amount the absolute magnitudes of the current generators differ.

IV. DIE DESCRIPTION

The die is composed of approximately 35% bipolar and 65% CMOS devices. The die photograph of Fig. 10 shows the three major functional blocks from left to right; the counters, the phase comparator / charge pump, and the prescaler. Three separate power supply buses were utilized in the design to mimize noise and jitter. The input and output buffers and ESD clamps were contained to one power bus, the CMOS logic to a second bus, and the prescaler block to the third. These precautions also helped to ensure that the VCO input sensitivity was not degraded by either output buffer or internal CMOS rail to rail logic switching spikes.

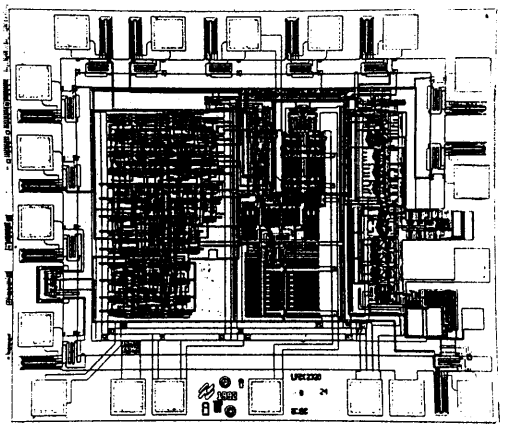

Fig. 10: Die Photograph

V. SYSTEM MEASUREMENTS

Phase noise measurements were taken of the 3 volt system at 1890 MHz with a 1.728 MHz reference frequency. The loop filter parameters were selected to be appropriate for DECT (Digital European Cordless Telecommunications) type systems with a lock time target of 80 µsecs. A -77dBc/Hz phase noise measurement at 10KHz (-120dBc/Hz at 1MHz) is shown in Fig. 11. The phase noise performance degraded approximately 7 db at +85 degrees C.

The reference frequency spurs are apparent in Fig. 12 down -68dB from the 1890 MHz carrier. (a 2nd order loop filter was used with a 12 KHz cutoff frequency.) A small degradation in reference spurs was observed as the supply voltage was increased.

A power dissipation curve is shown in Fig. 13. The internal bandgap regulator controls the variation in current to .9 mA over the -40 to +85 degrees C range (at 3v) and limits the variation over the 2.7v to 5.5v supply range at any given temperature to .8 mA.

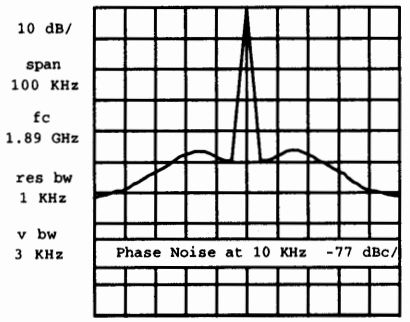

Fig. 11: Phase Noise

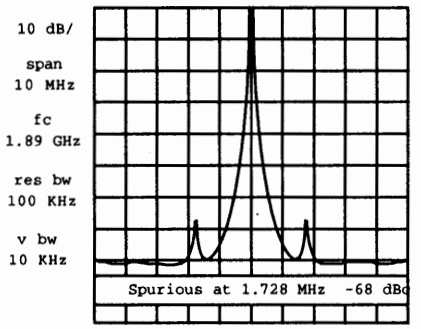

Fig. 12: Spurious

VI. CONCLUSIONS

A fully integrated silicon BiCMOS PLL frequency synthesizer function has been accomplished with performance characteristics suitable for DECT 2.2 GHz, low power, 3 volt cordless applications. The device exhibits phase noise of -77dBc/Hz at 10KHz from1890 MHz, with the reference frequency spurs down 68dBc at 1.728MHz. In addition, an input sensitivity of less than -15 dBm was attained at 2.2 GHz while consuming less than 35mW of power.

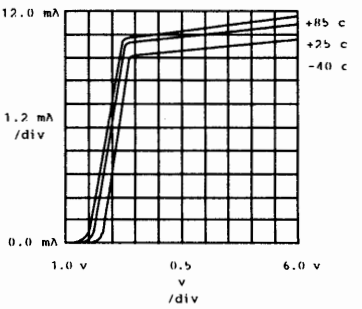

Fig. 13: Icc vs. Vcc

REFERENCES

[1] John Hatchett, "Adding to PLL Chips' Functions Speeds RF Synthesizer Design", Electronics, pp. 148-154, Oct. 9, 1980.

[2] Moriaki Mizuno..., "A 3 mW 1.0 GHz Silicon ECL Dual Modulus Prescaler IC", IEEE Journal of Solid-State Circuits, vol. 27, No. 12, pp. 1794-1798, Dec. 1992.

[3] Floyd M. Gardner, "Phaselock Techniques" Wiley & Sons Inc., p. 78, 1966.

[4] Dr. Roland E. Best, "Phase-Locked Loops, Theory, Design, & Applications" McGraw-Hill Inc., pp. 7-14, 1984.

[5] Mark O'Leary, "Practical approach Augurs PLL noise in RF synthesizers", Microwaves & RF, pp. 185-194, Sept. 1987.

[6] D. Byrd, G. Tietz, C. Davis, "Guaranteed Zero Deadband Phase Comparator / Charge Pump with Minimized Phase Offset", U.S. patent #4,814,726 1989.

A 3 VOLT ANALOG AUDIO PROCESSING CHIP SET FOR BATTERY OPERATED SYSTEMS

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Abstract **— An analog audio processing chip set which implements companding and audio filtering in two ICs has been developed. In order to maximize performance the compandor chip is designed in bipolar technology and the audio filtering is implemented in CMOS. The ICs use 3V supply, draw low current, and are packaged in 20-pin SSOP (Shrink Small Outline Package) which make them attractive for portable battery operated systems.**

I. INTRODUCTION

The recent trend in the electronics manufacturing industry is to produce low power, high performance technologies to support the design and development of personal information and communication terminals. Particularly in the Electronic Data Processing and Telecom markets these technologies have produced low power, highly integrated, and small packaged ICs which have been used to design numerous transportable, and hand-held systems with an ever smaller size and light weight.

Analog audio processing is one of the major building blocks for a number of wired and wireless telecommunication systems. The performance of the audio block, its size, and its power consumption are critical to the success of the final product. This article introduces a 2-chip analog audio processing subsystem consisting of Companding (Compressor/Expandor), and audio filtering. This chip set is low power, highly integrated, and can be used in cellular and cordless telephones.

II. FEATURES AND FUNCTIONALITY

The criteria for processing audio signals depend largely on the medium in which they are transponded. Typically the medium provides a limited dynamic range channel which is less then that needed by the audio signal to be transmitted and received without loss in fidelity. In FM systems, such as cellular, this dynamic range translates to a maximum deviation from center frequency (±12 kHz for Cellular) before the carrier spills over to the adjacent channels. Also, the transmission medium introduces noise that is proportional to the square of the audio frequency, which is summed to the signal, and eventually heard by the receiving party. To meet these criteria we need key audio processing functions as follows: (1) Allow a wide dynamic range signal to be transmitted through a restricted dynamic range channel (30 kHz for cellular), (2) treat high frequency noise by maintaining a good signal to noise ratio (S/N), (3) maintain voice quality in the presence of noise and distortion, and (4) restrict the signal level from increasing beyond a certain limit to prevent over modulation. This has been achieved with the introduction of companding, pre-/de-emphasis filtering, noise cancellation, and limiting circuitry, respectively.

This audio processing chip set, termed APROC2, implements these key functions in two ICs, the SA5752 for companding and noise cancellation, and the SA5753 for pre-/de-emphasis filtering and limiting. The audio functions have been partitioned between two chips in order to maximize performance, yet maintain enough features in each chip to be utilized individually in the system. Together the SA5752 and SA5753 make up a complete analog audio processing sub-system, from microphone input to modulating signal output, and from a demodulated signal input to audio signal output. In the transmit path, a voice signal produced by a microphone enters at the low noise programmable preamplifier, is band pass filtered, compressed to fit the channel's dynamic range, emphasized to maintain a good S/N for higher audio tones, and then limited and low pass filtered to produce an audio band signal suitable for FM modulation over the cellular network.

In the receive path the demodulated signal enters at the input of the audio band pass filter, and goes through the reverse process, i.e. de-emphasis and expansion. The resultant audio signal feeds an external audio amplifier (e.g. TDA7050) that drives a speaker or an earpiece. Fig. 1. shows the signal path inside APROC2 and the key functions that contribute to improving the S/N ratio and sensitivity of the system. The shaded blocks represent signal processing inside the SA5753.

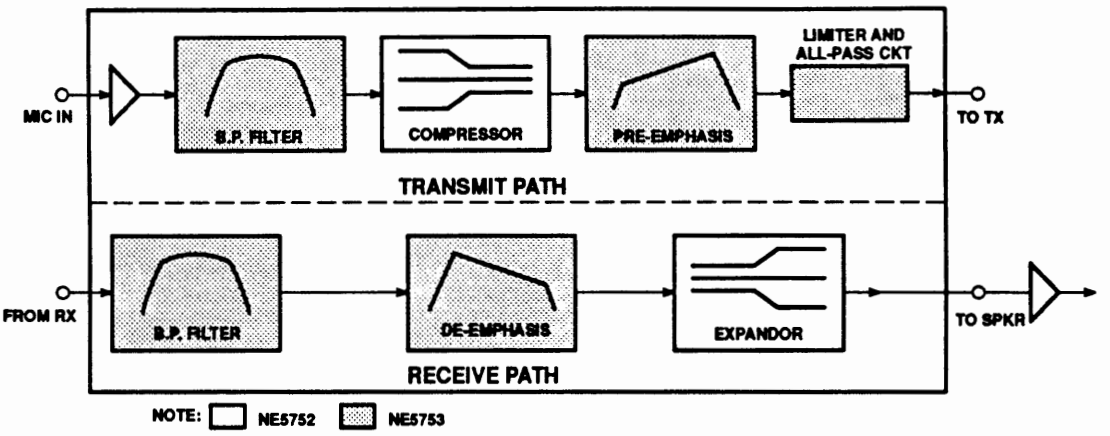

Figure 1.Key Functions of the SA5752 and SA5753 that Contribute to Improving the S/N Ratio and Sensitivity of the System.

A. Companding Chip

In the Tx path there is a 2:1 input to output compression translating to 1 dB of change in output level for every 2 dB change in input. In the Rx path, the expandor circuit performs the inverse of the compressor, i.e., input to output expansion is 1:2. The compandor's 0 dB or unity gain level is fixed at 77.5 mV_{RMS}. Two other features are present inside the SA5752: a low-noise preamplifier with variable gain setting (up to 40 dB), and an adjustable threshold noise canceller with VOX (Voice Operated Transmission) circuit providing programmable attack and decay time constants. The pre-amp gain can be set by an external resistor to produce the system's 0 dB level (77.5 mV_{RMS}) from the output signal of a variety of microphones. In the absence of an audio signal (no speech into microphone) or when the audio signal drops below a set threshold, the noise cancellation circuit reduces the overall gain by 10 dB. When the audio signal resumes, the gain is increased back to the normal level. In the meantime the VOX control signal can be used to disable or enable the transmit power amplifier (PA) consistent with the variation in the gain. SA5752 has a power down pin which is typically controlled by the SA5753. During power down mode all internal capacitors remain fully charged to achieve minimum power up time.

B. Audio Filtering Chip

The SA5753 IC contains 6 dB/octave pre-emphasis and de-emphasis filters, 4th order receive and transmit band pass filters (300 - 3000 Hz), a 5th order (3000 Hz) transmit low pass splatter filter, and a soft limiter circuit guaranteeing a maximum carrier frequency deviation of 12 kHz. Additional features have been integrated into the SA5753 as a result of an optimal architectural division, making the SA5753 very attractive for cellular radio applications. These include a DTMF generator, and programmable gain blocks for volume control and on-chip trimming. A two-wire serial bus interface (I^2C) links the SA5753 to the system's master control block. I^2C is used to program the DTMF generator, set the volume level, program the deviation attenuators so that no manual trimming is necessary, and to power down the device. The SA5753 also has features which distinguish it from its predecessor the SA5751: a transmit and receive mute functions with programmable polarities, on-chip summing amplifier combining the audio, DTMF, and DATA coming from an external data processor (also SAT, ST tones), and a default mode whereby the device is configured to operate and meet the EAMPS standard without any external control.

III. CHOICE OF TECHNOLOGY

The compandor chip is developed with bipolar technology to make use of the large dynamic range of the exponential relationship between V_{BE} and I_C in BJT devices. This device is manufactured using Philips Semiconductors' low power oxide isolated process (HS3).

The filter chip, on the other hand, is developed with CMOS technology, using switch capacitor design techniques because of the availability of high quality capacitors in MOS integrated circuits. Switch capacitor techniques are widely used in audio frequency filter design where the resistors are replaced by capacitors and digital switches in order to eliminate the requirement of integrating large values of resistors (which can be in the MΩ) to meet the long time-constant of audio filters. This results in a small die size, and mitigates the stringent accuracy and stability requirement of integrating resistors and capacitors because neither the fabricated values nor the temperature induced variation of the

R and C elements track each other. SA5753 is manufactured using Philips Semiconductors' low power high density BiCMOS process, known as QUBiC.

IV. A System Solution

APROC2 is particularly suited for analog cellular telephones because it meets the EAMPS and ETACS cellular standards. Fig. 2 shows a complete EAMPS/ETACS system block diagram of which the APROC2 is an integral part. The system controller communicates to APROC2 via a two-wire Inter-IC bus called I²C bus.

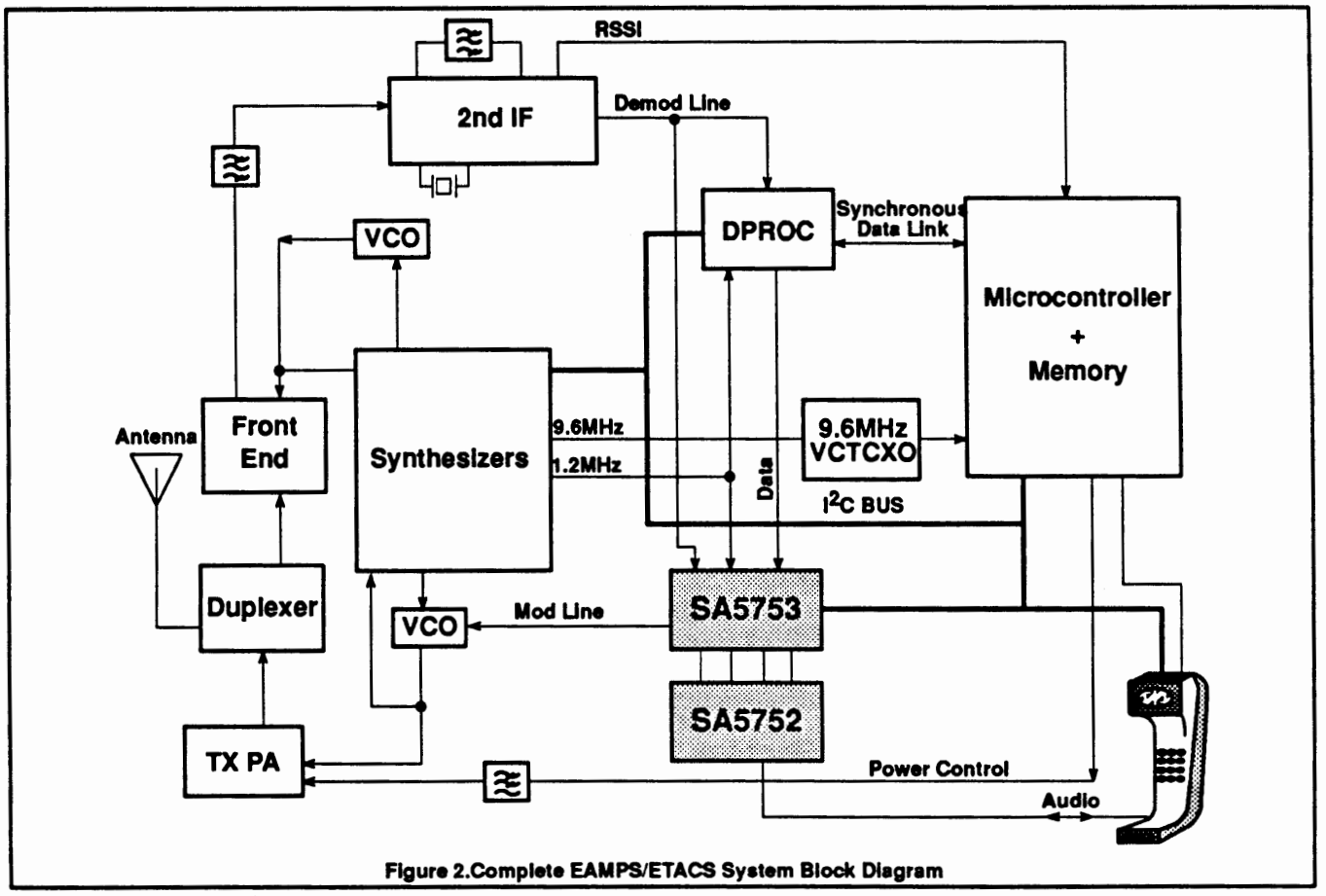

Figure 2.Complete EAMPS/ETACS System Block Diagram

This I²C control bus is a powerful means for networking between the ICs of a system. Typically the system controller acts as the bus master while the remainder of the ICs act as slaves. In systems like cellular telephones the I²C bus traffic generates digital switching noise which may couple into the synthesizer block and introduce phase noise. For this reason it is recommended that minimal I²C traffic should be maintained during conversation. With this in mind, the SA5753 has been designed to include an index addressing mode into its configuration registers bank so that only the necessary registers are addressed and modified for any change in the configuration. This will minimize I²C access and reduce digital switching which can cause noise and higher current consumption. Another system feature is the availability of the default mode which allows the use of this chip set in audio processing applications where there is no microcontroller or I²C bus available. Both SA5752 and SA5753 can operate with a supply ranging from 2.7 to 5.5 V. Current consumption is rated at 2.0mA and 2.7mA at 2.7V; 200μA and 600 μA in standby mode for SA5752 and SA5753, respectively. They are smaller than their predecessors the SA5750 and SA5751 (APROC1), while the SA5753 has extra programmable attenuators, an extra on-chip summing amp, and has more I²C control registers than the SA5751. APROC2 is packaged in two 20-pin SSOP packages (Shrink Small Outline Package) with dimensions (6.2x6.4 mm). When placed side by side, the two ICs interface directly with a small number of DC blocking caps, indicating a high degree of functional integration. Fig. 3 shows an application diagram of the APROC2. With its low power and small physical area, APROC2 is ideal for portable, battery powered applications.

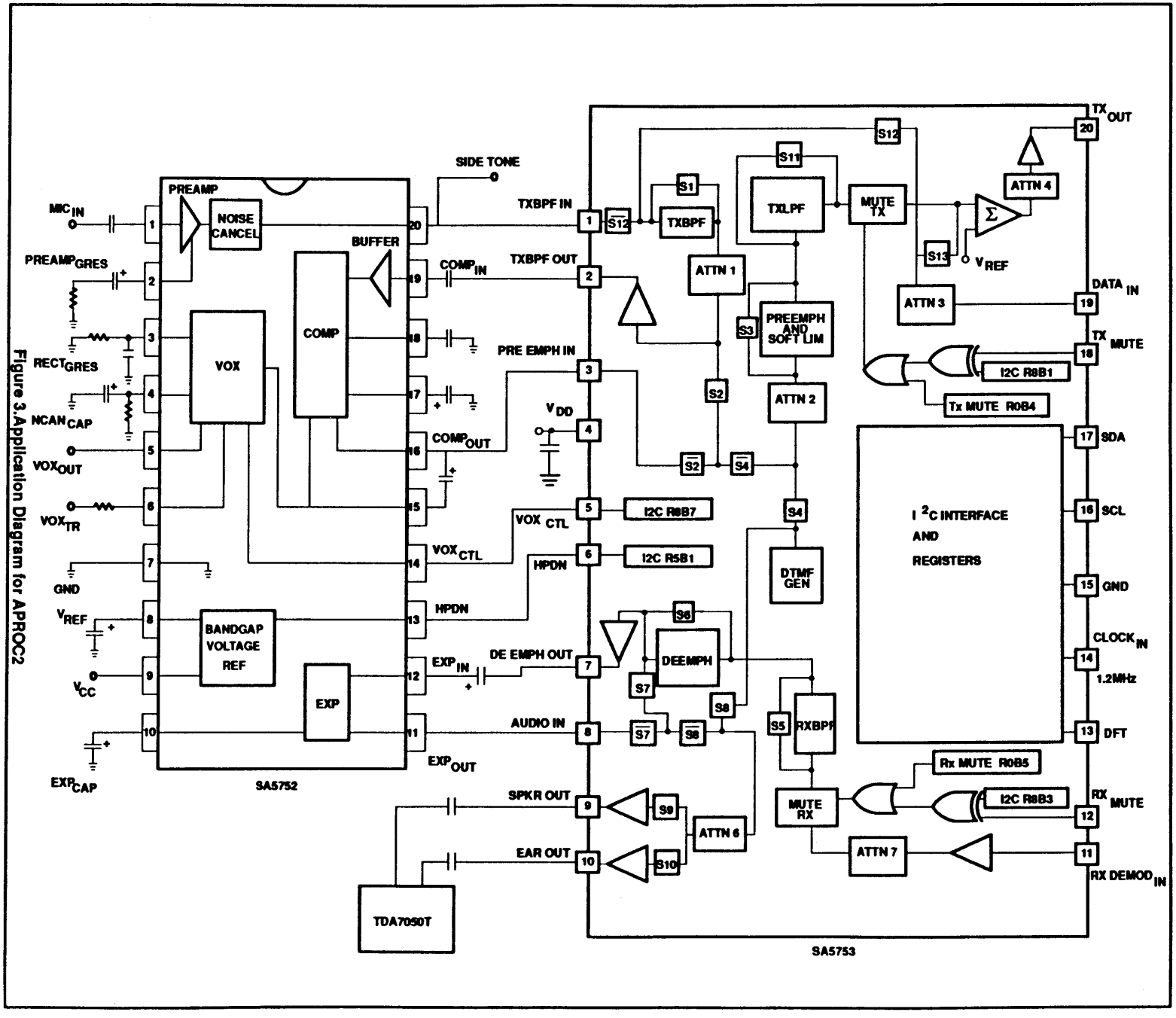

Figure 3.Application Diagram for APROC2

V. CONCLUSION

We have introduced a system solution consisting of an analog audio processing chip set suitable for EAMPS/ETACS. It is made up of a compandor chip and an audio filter chip. This chip set has significant improvements over its predecessor (APROC1) in functionality and real estate (20-pin SSOP vs 24 and 28-pin SOL for SA5750 and SA5751, respectively). Its integrated functions, low power consumption, and small size make it attractive for a variety of portable, battery operated audio systems.

Automotive Electronics Systems and Measurements

Session Chairperson: Jack Browne,
Microwaves & RF (Hasbrouck Heights, NJ)

Coaxial Vector Network Analysis Through 67 GHz: Addressing Millimeter-Wave Commerical Applications

by
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I. Introduction

Nature provides several "bands of opportunity" in the microwave frequency spectrum that may be exploited by modern communication systems. These frequency bands are characterized by unique transmission phenomena such as high or low atmospheric attenuation. Depending on the application, these characteristics influence fundamental design criteria - frequency, bandwidth, power, size - of a communication system.

One millimeter-wave frequency band used by many existing and emerging systems is the oxygen absorption band at and around 60 GHz. At 62.5 GHz, the free space signal absorption coefficient peaks at nearly 20 dB per kilometer at sea level (Figure 1) - providing a form of natural isolation. Antennas at these frequencies also provide extremely narrow beam widths and high gain in a fraction of the size of lower frequency microwave antennas. These transmission properties support efficient point-to-point communications and reduce the potential for signal interference. Hence, for systems that demand localized, secure, non-interfering communication, this frequency band is one obvious choice.

As communication systems move to millimeter-wave frequencies, development engineers will require measurement instrumentation to characterize both system-level and component performance - at actual operating frequencies. Manufacturing engineers will also require efficient and economical instrumentation to make complex measurements on potentially high volume products. Modern vector network analyzers (VNA) provide complex (real and imaginary) scattering parameter and non-ratioed parameter measurement capability in frequency, time, and frequency with time gate domains. VNAs offer powerful insight into the transmission and reflection properties of millimeter-wave communication systems.

II. Commercial Applications

Secure military communications (satellite-satellite, man-tank, submarine-submarine) make up most of the communication systems operating in the 60+ GHz millimeter-wave absorption band. However, the natural advantages of this frequency band also lend themselves to several emerging commercial (non-military) applications.

Automotive Anticollision Radar

Automobile manufacturers are making significant investments in supplemental safety and control systems that operate at millimeter-wave frequencies - i.e. forward-looking collision avoidance/automatic braking radar, rear-looking blind zone/backup radar, and intelligent cruise control. These systems rely on active and passive remote sensing technology to glance the surrounding environment and warn the driver of an impending collision. In order to be effective in a variety of driving environments, these radar systems must overcome several basic problems related to signal propagation and interference.

Millimeter-wave automotive radar has inherent advantages over alternate implementations. First, millimeter-wave radar is able to "see through" bad weather conditions such as fog, rain and snow. Whereas, other radar systems, such as infrared, rely on a clear line of sight. Second, signal interference can be minimized by taking advantage of the high atmospheric absorption

near 60 GHz. Once radar systems are placed into a large number of automobiles, mutual interference will adversely affect system performance. So, it is important that transmitted signals not travel much beyond a defined sensing radius where they might interfere with another vehicle's radar.

Traffic Control Systems
Traffic congestion is a common problem in urban areas around the world. Several proposed traffic control systems aim to regulate and smooth traffic flow. In Europe, projects like PROMETHEUS will transmit information regarding route guidance, road pricing, and road condition, etc. between road and vehicle. Other proposed systems include toll booths with automatic debiting systems that will recognize passing vehicles. As in other automotive applications, the 60 GHz band offers the advantages of limited range, low interference in a potentially high-multipath environment, and the ability to travel through bad weather with little distortion.

Millimeter-Wave Radio Links
Millimeter-wave links provide a cost effective and secure form of localized communication. Signals travel between rooftop antennas rather than across underground coaxial or fiber optic cable. In comparison, installation of a wireless millimeter wave system is faster and costs far less than a system requiring routing of coax or fiber optic cable. Millimeter-wave components and systems also provide significant size and performance advantages. A 60 GHz (1 ft. diameter) parabolic antenna provides the same gain and much narrower beam width at a fraction of the size of an equivalent 10 GHz microwave antenna (6 ft. diameter). The narrow beam width is well-suited for secure point-to-point communications as signal power occupies a much smaller area. Today, millimeter-wave power device technology can support the required transmission signal levels at a reasonable cost.

Radio Local Area Networks
Millimeter-wave communication within buildings eliminates the need for cables that connect computers and workstations to a Local Area Network (LAN). Radio LANs provide freedom of movement for individual network nodes as they are no longer "tied" to a coaxial or fiber optic connection. In manufacturing, a mobile robot can perform tasks at various locations in the facility while maintaining constant communication with a central controller. In office environments, computers can be easily moved from desktop to meeting rooms or other locations in the building. Indoor millimeter-wave LANs naturally provide localized, and thus, secure communication. Transmissions within a building do not travel well through walls or outside the building.

III. Measurement of Millimeter-Wave Communication Systems

Fundamental S-Parameter Measurements
The traditional use for VNAs is measuring the fundamental S-parameters of two-port devices. VNA technology has evolved to better address these measurements by incorporating sophisticated error-correction, automatic signal reversing, and broadband frequency coverage. Today, VNAs are available that provide single connection frequency coverage from 40 MHz to 67 GHz in coax and 33 GHz to 110 GHz in waveguide bands. A variety of calibration techniques address different media types: coaxial, waveguide, microstrip, etc. Non-ratioed signal measurements of multi-port and/or frequency conversion devices (i.e. mixers, converters, etc.) are now accommodated with dual source control capability and specialized test set configurations.

Device Modeling and Model Verification
With the advent of powerful workstation computers and software, device modeling and simulation has become an important step in the product development process. Device performance can now be simulated and evaluated before investing in fabrication. In the past, VNAs were used to

measure the S-parameters of a device at microwave frequencies (typically <40 GHz). These measurements were then used to develop mathematical models of device performance. Once a model was established that correlated with measured data, one could extrapolate performance to higher frequencies. Unfortunately, such extrapolation usually surpassed one's ability to measure and verify actual performance. Modern VNAs address this fundamental problem with millimeter-wave frequency coverage. Now, design engineers can develop models to higher frequencies and verify there extrapolations through 67 GHz (coax) and/or 110 GHz (waveguide).

Antenna Measurements
Characterization of an antenna involves measuring its reflection and radiation characteristics. Typical measurements include match, gain, radiation pattern, bandwidth, and polarization. A VNA can measure all of these parameters at a single (CW) or multiple millimeter-wave frequencies. Long distance antenna ranges can be accommodated by remoting the system signal source up to five miles from the test set receiver and mainframe.

Transmission Time Domain Measurements
In both automotive and radio LAN applications, the presence of multipath signals and interference must be taken into account. Using the time domain transmission (S21) measurement capabilities of the VNA, one can measure the relative amplitude and phase angle of short- and long-range multipath signals. This measurement is very similar to radar cross section (RCS) measurements that measure the reflections or "signatures" of surrounding objects.

An example illustrates the basic measurement concepts. The setting consists of two metal plate reflectors of different sizes, placed at different distances from the transmit/receive antenna (Figure 2). In this case, the transmit and receive antenna are located at the same position. However, a separate receive antenna could be located some distance away from the transmit antenna. Measurements are made from 60 to 65 GHz with 501 frequency data points - providing approximately 30 meters of unaliased range.

The VNA system is calibrated by first placing a short across the antenna and performing a transmission frequency response calibration. The short is then removed, and the antenna is aligned with the targets. Figure 3 shows the time domain transmission (S21) characteristics over 0 to 8 meters from the antenna reference plane (marker values are "round-trip" - twice the actual linear distance(s) between objects). Marker 1 is placed on the antenna leakage signal . Marker 2 is placed on the response of the first object (4"x12" metal plate). Marker 3 is placed on the response from the second object (24" x 48" metal plate).

The VNA's time gating capability allows one to isolate the response from the first object (Figure 4) . Linear Magnitude graph type is chosen prior to gating to provide a "sharper" display of each discontinuity. Once the time gate is activated, one may return to the frequency gated by time (FGT) domain and view the relative amplitude and phase angle response of the object versus frequency (Figure 5).

In a real world application, the two metal plates could be replaced with automobiles in a radar simulation or file cabinets and desks in an office LAN environment. In any case, it is clear that this measurement technique, traditionally used in military applications (i.e. RCS), can be adapted to conceptually similar commercial applications. Time Domain gating allows one to identify and analyze troublesome multipath and reflected responses.

Summary
Commercial systems are being specified to operate in the oxygen absorption band at and around 60 GHz. This millimeter-wave "band of opportunity" provides high free space signal absorption, a natural form of isolation, for secure and localized communications. Automotive anticollsion radar,

traffic control systems, radio links, and local area networks are a few of the emerging millimeter-wave commercial applications.

The Vector Network Analyzer is one measurement tool that may be used by engineers to develop and test millimeter-wave communication components and systems. Broadband coaxial frequency coverage to 67 GHz and in waveguide bands to 110 GHz supports fundamental S-parameter measurement, on-wafer device characterization, antenna measurement, and gated time domain measurement capabilities.

References

1. Briere, P., Perea, E., de Saint Leger, O., "System and technology aspects of future digital cellular phones in Europe", GaAs IC Symposium, October 1991, Monterey, Tech. Digest 33-36.

2. Detlefsen, J., Rozmann, M., Troll, T., Zeilinger, "System aspects and design of an automotive collision warning PN code radar using wavefront reconstruction", MTT-S Conf. 1992, Albuquerque, Symp. Digest 625-628.

3. Goel, J., Tan, K.L., Stones, D.I., Chan, R.W., Streit, D.C., Peratoner, S., Schellenberg, J, "60 GHz power amplifier using PHEMT", MTT-S Conf. 1992, Albuquerque, Symp. Digest 587-589.

4. Haese, N., Benlamlih, M., Cailleu, D., Rolland, P.A., "Low-cost design of a quasi-optical front-end for on board mm-wave pulse radar", MTT-S Conf. 1992, Albuquerque, Symp. Digest 621-623

5. Kotaki, M., Takimoto, Y., Akutsu, E., Fujita, Y., Fukuhara, H., Takahashi, T., "Development of millimeter wave automotive sensing technology in Japan", Invited Paper, MTT-S Conf. 1992, Albuquerque, Symp. Digest 709-712.

6. Li, Z.W., Menzel, W., "A 61 GHz doppler radar using inverted strip dielectric waveguide", MTT-S Conf. 1992, Albuquerque, Symp. Digest 629-632.

7. Meinel, H., "Applications of microwaves and millimeterwaves for vehicle communications and control in Europe", MTT-S Conf. 1992, Albuquerque, Symp. Digest 609-612.

8. Meinel, H.;Jackson, P., "Progress in the commercial applications of microwaves: a review", Microwave Engineering Europe, November 1992, pp. 23-31.

9. Meinel, H., "Millimetre-wave commercial applications and technologies", Microwave Engineering Europe, November 1991, pp. 9-20.

10. Ogawa, H., Polifko, D., "Fiber optic millimeter-wave subcarrier transmission links for personal radio communication systems", MTT-S Conf. 1992, Albuquerque, Symp. Digest 555-558.

11. Readout: "Fibre, mm and microwave comms blend together", Microwave Engineering Europe. June/July 1992, pg. 21.

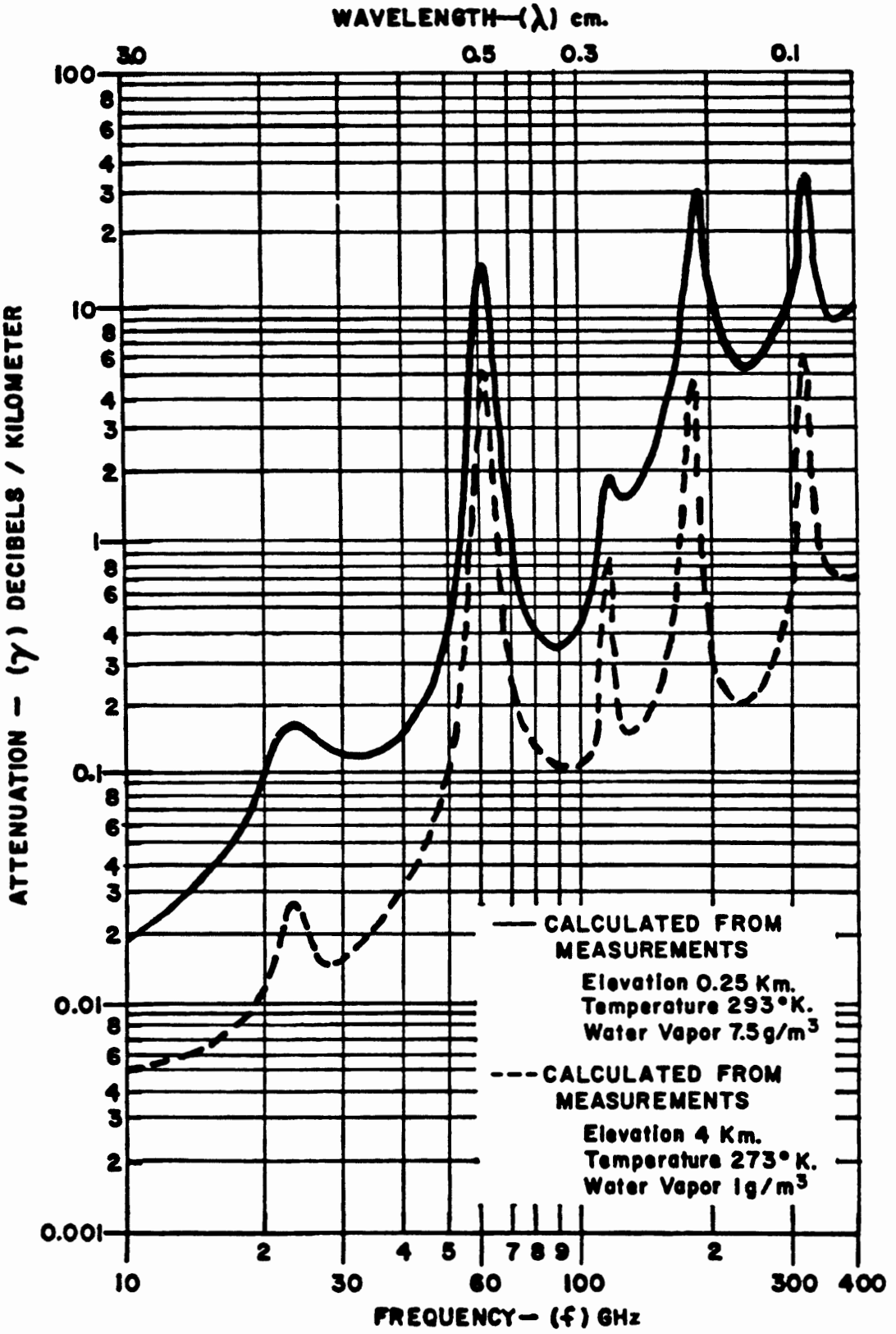
12. Rembold, B., "Communication systems at millimeter waves", 22nd EuMC 1992, Espoo, Conf. Proceedings, Vol. 1, pp. 53-72.

13. Saito, T., Okubo, N., Kawasaki, Y., Isaji, O., Suzuki, H., "An FM-CW radar module with front-end switching heterodyne receiver", MTT-S Conf. 1992, Albuquerque, Symp. Digest 713-716.

14. Takimoto, Y.; Kotaki, M., "Automotive anticollision radar", Applied Microwave, Fall 1992, pp. 70-82.

15. Williams, D.A., "Millimetre wave radars for automotive applications", MTT-S Conf. 1992, Albuquerque, Symp. Digest 721-724.

Figure 1. Atmospheric Attenuation



CALCULATED COMBINED WATER VAPOR AND OXYGEN ATTENUATION

Figure 2. Example measurement setup

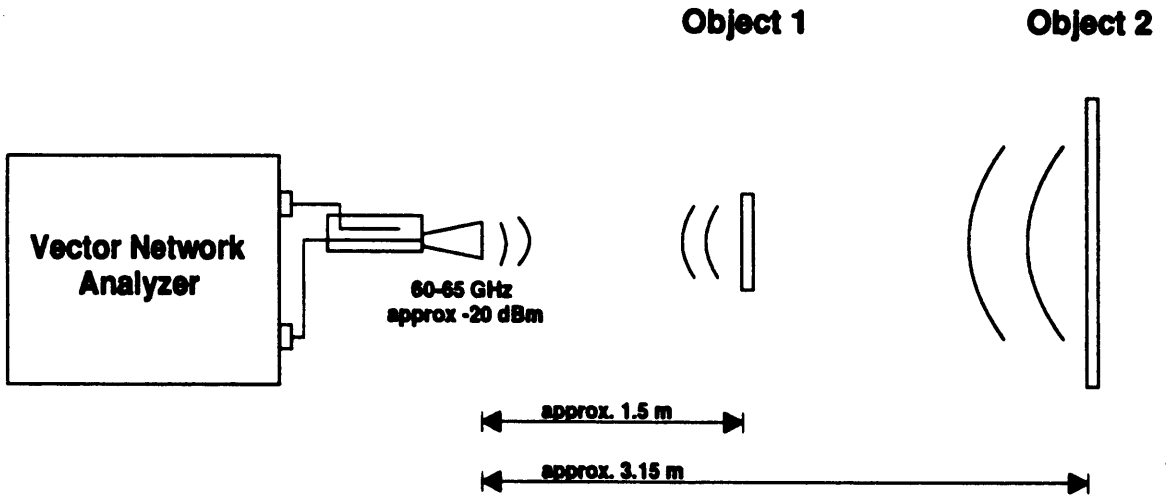


Figure 3. Time Domain response of Objects 1 and 2

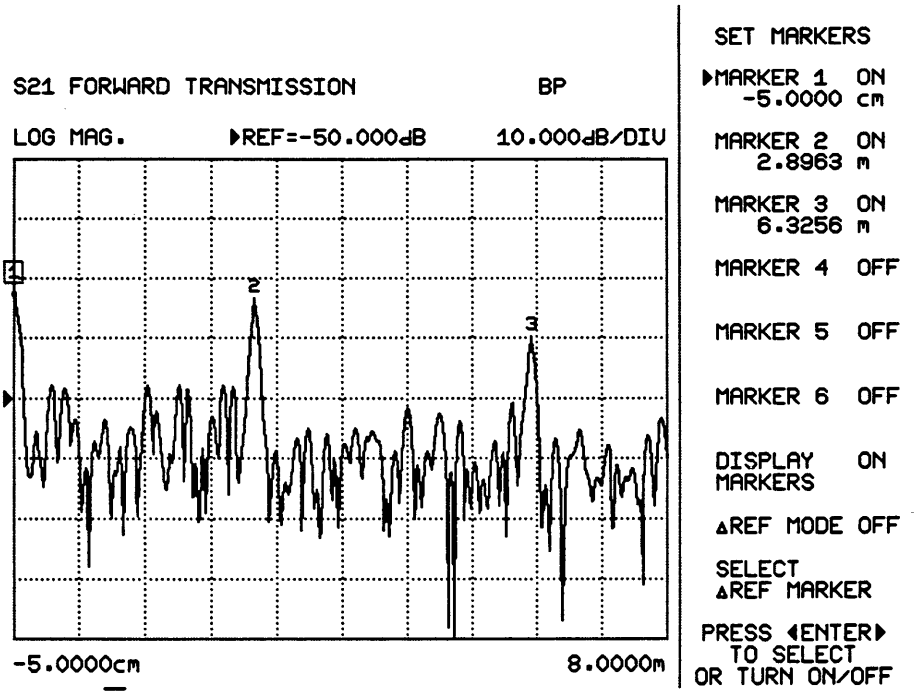


Figure 4. Time Domain gate applied to isolate the response of Object 1

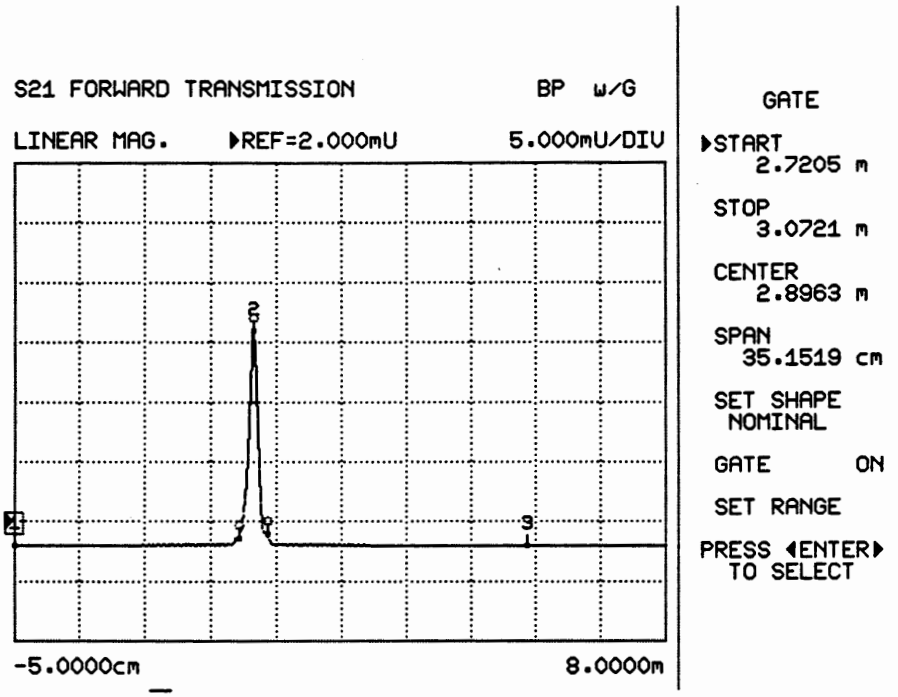
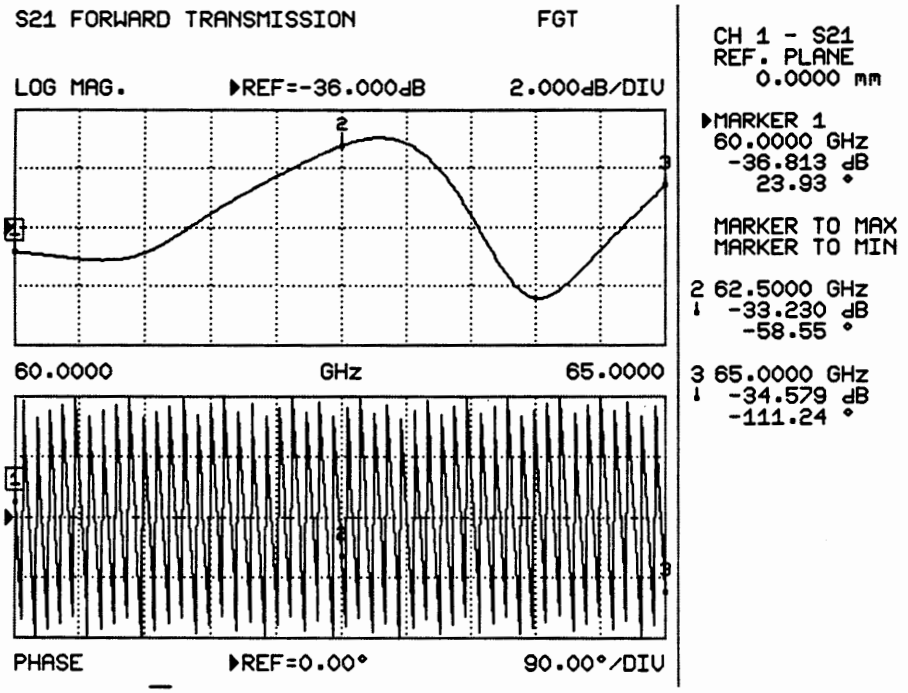


Figure 5. Response of Object 1 in the Frequency Gated by Time Domain



MONOLITHIC COMPONENTS FOR 77 GHz AUTOMOTIVE COLLISION AVOIDANCE RADARS

Lamberto Raffaelli*

ABSTRACT

This paper will examine design methodology and test results of monolithic components specifically designed for a 77 GHz collision avoidance radar. In addition cost-trade-offs between a fundamental 0.15 micron pseudomorphic HEMT based approach and a multiplied 0.25 micron power MESFET based solution will be discussed.

INTRODUCTION

Automotive Collision Avoidance Systems include a Sensor capable of detecting the presence of obstacles in front of the vehicle, a signal processor to identify those obstacles that pose a real threat to the driver and a display to present the data to the driver.

The optimum sensor for automotive applications should satisfy high antenna directivity and small volume requirements; in addition the system should be fully operational during adverse weather conditions such as dense fog or rain. The sensor needs also to offer high reliability and low unit production cost.

Millimeter-wave radars provide significant advantages as compared to alternative technologies (such as laser-based systems) and successfully meet most of the requirements with cost being the only challenge. These systems have been mainly developed for low volume military applications based on waveguide and/or hybrid components. These technologies being labor intensive, do not lend themselves to low production cost. In addition at Millimeter-wave frequencies, integrated circuit bond wires, particularly in areas subject to high VSWR will hinder performance and repeatability.

In order to reduce production cost, automotive radars need to rely on GaAs Monolithic Components. Alpha Industries has been developing Monolithic Technology at Millimeter-wave frequencies for the last ten years, mainly for defense contracts such as SADARM, Longbow, SDI, and MIMIC.

The technology already developed find a unique opportunity to be inserted in collision avoidance production programs with projected costs, as already demonstrated for military customers at similar frequencies, fully compliant with automotive radar program requirements.

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MONOLITHIC TRANSCEIVER

In Europe the allocated frequency band for Collision Avoidance Radars is 76 to 77 GHz. The system architecture has different options available: the source could use either a fundamental or a multiplied approach, the modulation technique could take advantage of either FMCW or pulsed techniques; we could also use two separate receiving and transmitting antennas or combine the two functions in one.

In order to cover most system requirements, Alpha Industries is developing the following Monolithic Chips:

* VCO (38 GHz or fundamental)
* Driver Amplifier
* Doubler
* Down Converter
* 77 GHz Pin Switch

38 GHz VCO Chip

The 38 GHz VCO MMIC Chip is shown in Fig.1. The design uses a 0.25 x 400 micron power MESFET in common source configuration and two double mesa integrated varactors (1), one for frequency tuning and one for temperature compensation. The drain of the power MESFET is connected to the output through a coupler that transforms the impedance and decouples the oscillator. The double mesa varactor technology was specifically designed to reduce the diode series resistance and improve the Q of the resonator, therefore resulting in lower VCO phase noise as compared to a planar varactor process. Typical performance is as follows:

* Frequency	38-38.5 GHz
* Pout	+10 dBm
* Tuning BW	600 MHz
* Temp. Stability	Less than 1 MHz/°C
* Phase Noise	-100 dBc/Hz @ 1 MHz offset

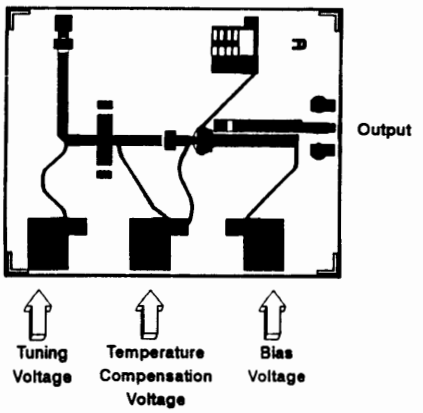

Fig. 1
38.5 GHz VCO Chip

DRIVER AMPLIFIER CHIP

GAMMA[1] Monolithics has already developed and tested power amplifiers in Ka-band based on our standard 0.25 micron power MESFET process. Output power exceeding 3 watts has been achieved using basic cells which combine four standard 400 micron power MESFET devices. Test data for one of these cells is reported in Fig. 2. By using an amplified source in Ka-Band multiplied up to 77 GHz, we can very easily achieve the power levels (10-20 dBm) required for a collision avoidance system.

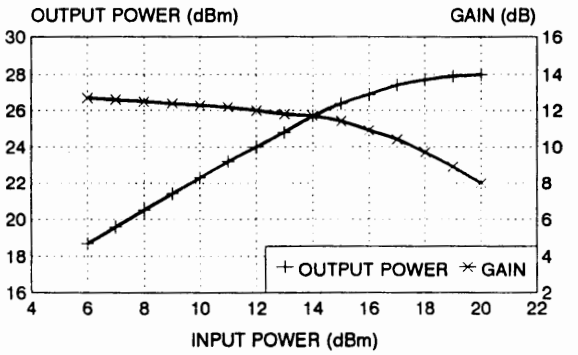

Fig. 2
Gain and Power Output
of a 400 mW Power Amplifier

38.5 to 77 GHz DOUBLER

Multipliers in W-Band could utilize either FET or Varactor Monolithic Technology(2). A Varactor-based doubler is preferred because of better conversion efficiency and superior bias and temperature stability. In addition, our VCO design integrates two high Q double mesa varactors with power MESFET material; therefore further monolithic integration of the varactor function with either the VCO or the power amplifier is an available option. A simulation of the monolithic doubler yielded better than 8 dB conversion loss at 77 GHz.

DOWNCONVERTER

A 60 GHz subharmonic mixer has been already fabricated and tested for a space communication program.

The use of a 30 GHz LO signal reduces the power required at the fundamental frequency without compromising the noise figure performance by more than approximately 1 dB as compared to a fundamental down-converter.

The mixer chip used two anti-parallel Schottky diodes to produce a virtual Lo signal at 60 GHz. The diode exhibits a series resistance of 6 ohms and a capacitance of 0.035 pF, allowing efficient frequency conversion at 60 GHz. Conversion loss is typically 6-7 dB across a 10% bandwidth. It is felt that this conversion loss can be improved by 1-2 dB by optimizing the diode structure to produce lower series resistance and capacitance. The mixer, due to the self-biased nature of the subharmonic configuration, requires as little as +6 dBm LO drive.

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[1] GAMMA Monolithics is a partnership between Alpha Industries, Woburn, Massachusetts, and Martin Marietta, Baltimore, Maryland.

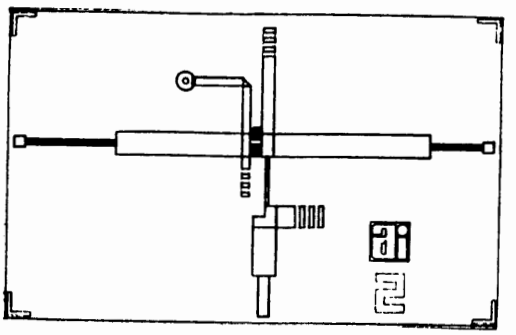
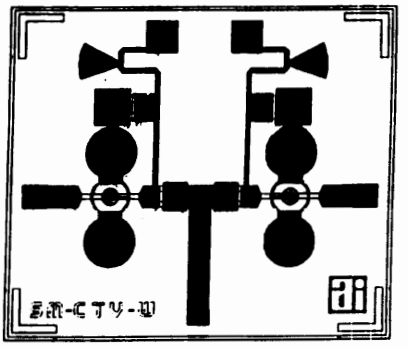


Fig. 3
77 GHz Subharmonic Mixer Chip

A simulation of a 77 GHz mixer, presently in fabrication at Alpha was performed using the same diode utilized in the V-band mixer described earlier. The simulation gave us a noise figure of 6.5 dB DSB when inserted into a balanced rat-race mixer configuration, (see Fig. 3) and 7.5 dB in a subharmonic-type down converter.

77 GHz PIN SWITCH

At 77 GHz monolithic pin-based switches are definitely offering superior performance as compared to their FET-based counterparts. Considering that in the Transceiver the power amplifier function is the major cost driver, we opted for the PIN-based solution as compared to a more integratable FET-based approach. The lay-out of a 77 GHz SPDT is represented in Fig. 4. The design yielded 25 dB of isolation and 1 dB loss at 77 GHz.



Measured Performance @ 77 GHz:

Insertion Loss: 1.0 dB
Isolation: 24 dB

Figure 4
77 GHz SPDT Pin Switch

MULTIPLIED VERSUS FUNDAMENTAL APPROACH

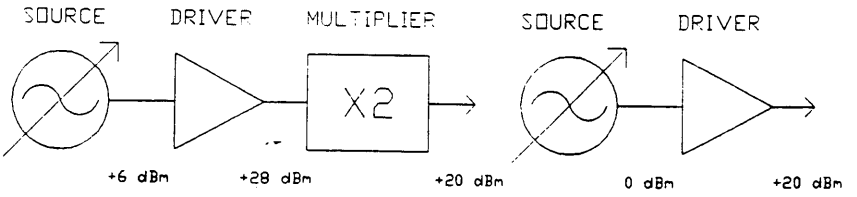
The source at 77 GHz could take advantage of either a fundamental or a multiplied approach. Let's assume an output power requirement of 100 mW and a times two multiplier conversion loss of 8 dB. (See Table 1)

The positive feature of a signal multiplied from an amplified source at 38.5 GHz is that it relies on 0.25 micron GaAs power MESFET technology that is already in production in Alpha Industries. On the other hand, assuming a monolithic varactor multiplier conversion loss of 8 dB, to generate 20 dBm at 77 GHz, would require 28 dBm of power at 38.5 GHz, which makes the driver amplifier at least twice as large and its Fet output periphery a minimum of three times as wide as compared to the buffer in W band.

At 77 GHz the device required is based on a 0.15 micron Pseudomorphic HEMT. This technology, although demonstrated, is not as mature from a manufacturing point of view.

On the positive side, it will deliver a monolithic chip with half the size or less. In terms of yields, at 77 GHz the shorter gate length and the more complex material structure could be balanced off by the reduced gate periphery.

Assuming 4" wafers and 30% chip sort yields, a 1995 cost projection derives a chip cost of $45 for the multiplied source. At 77 GHz, with the same overall yield, the chip cost is down to $22.50.



	MULTIPLIED (38.5 GHz x 2)		FUNDAMENTAL (77 GHz)	
	6 dBm	28 dBm 20 dBm	0 dBm	20 dBm
FET REQUIRED				
Type	Power Mesfet		Pseudomorphic	
Gate Length	0.25 Micron		0.15 Micron	
Gain	8 dB (at 38.5 GHz)		7 dB at (77 GHz)	
Power Density	300 mW/mm (at 38.5 GHz)		150 mW/mm (77 GHz)	
TECHNOLOGY STATUS	Mature		Under Development	
DRIVER AMPLIFIER				
Number Stages	3		3	
Fet Output Periphery	2.1 mm.		0.666 mm.	
SOURCE FET PERIPHERY	400 Micron		200 Micron	
REAL ESTATE				
VCO	4 mm^2 (actual)		2 mm^2 (projected)	
Multiplier	1 mm^2 (projected)		N/A	
Overall Size	18 mm^2		9 mm^2	
Wafer Cost/mm (assuming 4" wafer)	$2.50 (30% yield)		$2.50 (30% yield)	$5 (15% yield)
Overall Cost (1995 projection)	$45		$22.50	$45

Table 1
Source Alternatives

CONCLUSIONS

It is true that 30% yields in W band have yet to be proven, but it is also true that 30 % yields in Ka-Band is today, based on recent experience, a conservative projection for the foreseable future. The GaAs technology is progressing very fast when we consider that only a few years ago the 1 micron MESFET was the only process in production. The automotive sensor business is offering GaAs monolithic circuits an unprecented opportunity to be inserted in large volume programs. To be successful in this market the engineers have to focus on how to bring the required processes, from wafer fabrication to assembly and test, in a real low cost manufacturing environment.

References

1. McDermott, M.G. et al, "Integration of High-Q GaAs Varactor Diodes and .25 μm GaAs MESFET's for Multifunction Millimeter-Wave Monolithic Circuti Applications", IEEE Trans. on MTT, vol. 38, no. 9, Sept. 1990, pp. 1183-1190.

2. Lamberto Raffaelli and Earle Stewart "Millimeter-wave Monolithic Components for Automotive Applications", Microwave Journal, Vol. 35, no. 2, February 1992.

110-GHz Wafer Probe Enables Cost-Effective Millimeter-Wave Circuit Applications

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Cascade Microtech Inc.
Beaverton, Oregon

I. Introduction

Millimeter wave monolithic integrated circuit (MIMIC) technology has matured to a high degree under such programs as the DARPA MIMIC effort. The original intent was to develop cost-effective millimeter wave frequency (i.e., >30 GHz) circuits for such applications as radar front ends for missile seekers and aircraft systems. With the declining military market there has been a strong push to commercialize this technology for application such as automotive collision avoidance radar and local area communication networks (LAN).

For any of these applications, wafer probes are required for characterization and testing of the circuits while they are still in wafer form. The circuits must be tested at the wafer level, since inserting defective devices into systems typically raises the cost of using MIMICs to an unrealistic level. The cutting edge for many applications of MIMICs is in the 50 to 110 GHz region. For this reason, DARPA has funded the development of wafer probes for use in the V-band (50 to 75 GHz) [Navy Phase III MIMIC] and W-band (75 to 110 GHz) [Army Phase III MIMIC] frequency ranges. This paper will discuss the development of these probes with emphasis on the W-band probe, since it is at the cutting edge of wafer probing technology.

A brief review of wafer probes is presented in section II. Section III and IV discuss the technical aspects of the waveguide input wafer probes and section V presents measured data for these probes and some device measurements. Conclusions are in section VI.

II. Review of Wafer Probe Technology

At frequencies below 65 GHz, the wafer probe can be linked to the chosen test equipment via a coaxial cable [1]. Figure 1 shows traditional coaxial input wafer probes. Inside the probe body there is a coax-to-coplanar waveguide (CPW) transition. The coplanar waveguide is formed by depositing a layer of gold on the lower surface of an alumina probe board and guides the signal to the probe tip. This structure is known as the probe board. At the tip of the probe board a hard metal, such as nickel, is deposited on the CPW metalization to form fingers. These fingers make contact with the device under test (DUT) on the wafer

surface. Typically coplanar pads are formed at the DUT test ports to allow contact with these probe fingers.

A waveguide-to-CPW transition was required to extend the upper frequency limit of wafer probes, since commercially available coaxial cable assemblies overmode above 65 GHz [2]. Figure 2 shows an operational diagram for a waveguide input wafer probe. Rectangular waveguide enters a transition section where the dominant TE10 mode of the waveguide is converted to a coplanar field pattern. The coplanar mode is then launched on a CPW probe board similar to that described above. Figure 3 shows a pair of V-band probes probing a GaAs wafer. Notice the waveguide entering the far end of each probe, and the bias cable attached to the side of the probe.

III. The Transition

Figure 4 illustrates the transition process in greater detail. The rectangular waveguide input is illustrated in (a), which supports the TE10 mode as shown. Next, a ridge is gradually introduced, which forms the quasi-TEM field pattern as in (b). The ridge-trough waveguide is formed by gradually adding a trough below the ridge as shown in (c). By lowering the ridge into the trough, the electric field is split and rotated forming a coplanar field, with a characteristic impedance of 50 ohms in this case. This field pattern is similar to that found in a coplanar waveguide as illustrated in (d). The final step is to launch the coplanar mode into a 50-ohm CPW transmission line. The CPW line is inverted, as shown in (e) to bring its grounds into contact with the lower surface of the waveguide. The signal line of the CPW is attached to the ridge with a gold bond ribbon. This completes the transition process.

A test fixture was constructed to confirm the transition design. For W-band, a WR-10 rectangular waveguide was transitioned to 50-ohm ridge-trough waveguide and then back to WR-10 waveguide. Having rectangular waveguides at each port of the test fixture allowed testing with a HP-8510C waveguide test set for use at W-band. Figure 5 shows the insertion loss (S21) and return loss (S11) of the transition. Since the measured insertion loss is actually for two transitions (i.e. back-to-back), the appropriate scale for S21 is half the measured loss to give the effective loss for a single transition. The insertion loss is less than 0.7 dB from 75 to 106.5 GHz rising to 0.8 dB at 110 GHz. The return loss is better than 15 dB over the entire band, except at two spots.

IV. The Probe Board

The CPW probe board design presented two primary challenges: low insertion loss, and low crosstalk between probes when two or more probes are in close proximity while probing some device. Insertion loss in CPW transmission lines is generally attributed to radiation loss and conductor loss when low-loss dielectric

substrates are used. At the onset of the CPW design, radiation loss was expected to be the dominant insertion loss factor based on prior research [3]. Using a similar approach, the predicted radiation loss was computed for three CPW transmission lines on alumina, having gaps of .001, .002, and .004 inches (G in Figure 6). In each case the signal line width (W) was increased to maintain 50-ohms characteristic impedance. Figure 7 shows the results a which imply that radiation loss increases with gap size.

To verify these predictions a radiation study was conducted. This consisted of measuring the insertion loss (S21) of three coplanar waveguide (CPW) transmission lines, all 1.00 inch long. The three CPW lines differ in gap and signal line dimensions (see Table 1). In each case W and G are chosen for a characteristic impedance of 50 ohms. Figure 8 shows the results which are opposite of what was predicted. The implication is that radiation loss is negligible and that the signal line width (W) dominates. It is speculated that this dominance is due to the reduction of signal line resistance with increasing width.

The tests were conducted on a .020" thick alumina substrate. This allowed scaling these 0 to 50 GHz results to those of a .010" thick substrate, with W and G half the size listed in Table 1, over the 0 to 100 GHz range. This scaling implied that no moding would take place, based on the monotonic nature of the data.

From these results the CPW probe boards were designed for primarily low conductor loss, since the radiation loss was no longer viewed as a major concern. At the probe tip the gaps and signal line width of the CPW line are reduced through a tapered region to give the required separation of the nickel fingers to match the device under test (DUT). To minimize radiation off the probe tip, this taper must maintain a constant characteristic impedance. Excess radiation can couple to another probe tip during multi-port measurements. This can perturb data, particularly where low signal levels are involved, such as S12 in FET measurements.

V. Functional Probe Data.

Figure 9 illustrates the construction techniques employed for an actual probe. The probe block is split into upper and lower halves as shown. An insulating layer is placed between the two halves to provide dc isolation. Quarter wavelength RF chokes generate a virtual ground where the waveguide interior surface is split to minimize RF losses.

The alumina probe board is captured in a pocket that is machined into the upper block. The probe board is oriented such that the metalized ground-signal-ground lines are facing down, since this is the surface that must contact the wafer. A bond ribbon joins the signal line (shown by a dashed line) to the ridge

after the probe is situated in the upper block. When the lower block is joined to the upper block the probe board is clamped into place. This clamping also brings the ground metalization of the probe board into electrical contact with the lower block. The end result is that the signal line and ground lines are electrically isolated and may be biased by applying a voltage to the upper and lower block halves respectively. In the event of probe board breakage, the two halves may be separated and a new probe board installed.

The performance of actual V-band and W-band wafer probes are shown in Figures 10 and 11, respectively. The insertion loss (S21) is typically 3± 1 db for both probes, with a worst case of 4 db and 4.2 dB for each respectively. Two reflection coefficients are shown for each probe: S11 and S22. These are the reflection coefficients at the rectangular waveguide input port and at the tip of the alumina probe board, respectively.

With a pair of V-band probes, a pseudomorphic MODFET was tested, using a setup similar to that shown in Figure 2. Figure 12 shows the S21 data for this device. The device has S21=1 at 58.5 GHz. Passive devices such as capacitively couple filters have also been characterized, even when their insertion loss exceeded 30 db. At this time, no devices have been made available for testing with the W-band probes, but similar performance is expected.

VI. Conclusions

Under the Phase III MIMIC program, waveguide input wafer probes were successfully developed covering 50 to 110 GHz in two bands. These probes are required to allow MIMICs to be fully tested and characterized at the wafer level. This testing is essential if MIMICs are to be financially feasible for insertion into both military and commercial systems.

VII. References

[1] K.E. Jones, E. W. Strid, and K. R. Gleason, "mm-Wave Wafer Probes Span 0 to 50 GHz," Microwave J., Apr. 1987.

[2] E.M. Godshalk, "A V-Band Wafer Probe Using Ridge-Trough Waveguide," IEEE Trans. Microwave Theory Tech., vol.T-39, pp. 2218-2228, Dec. 1991.

[3] M. Riaziat, R. Majidi-Ahy, and I.J. Feng, "Propagation Modes and Dispersion Characteristics of Coplanar Waveguides," IEEE Trans. Microwave Theory Tech., vol. MTT-38, pp. 245-251, March 1990.

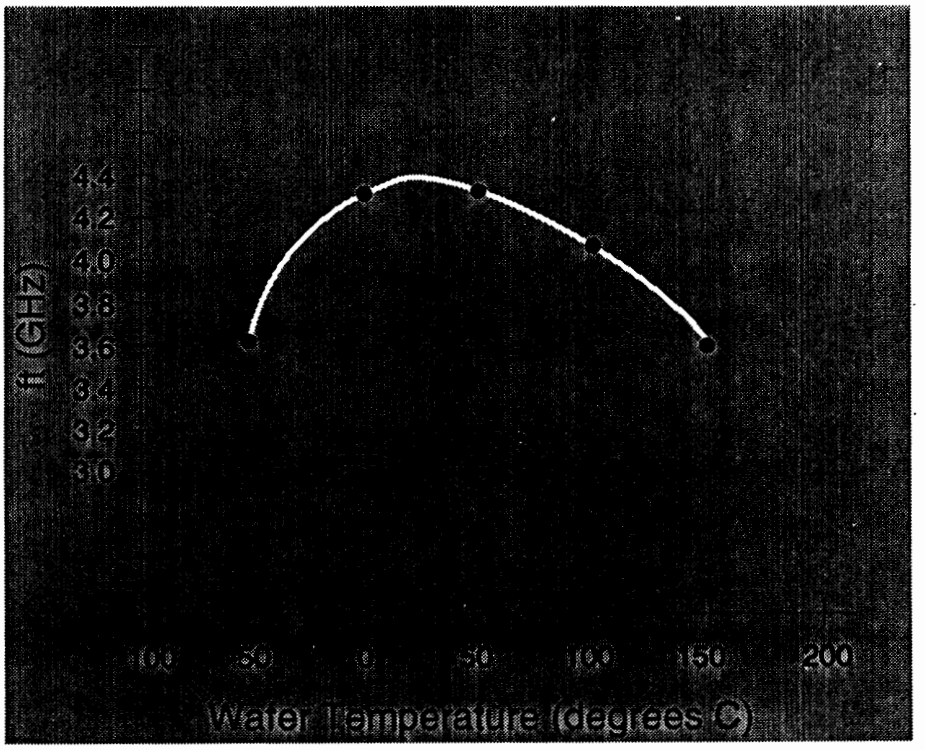

Figure 1. Typical ft Temperature dependence of a 2x3 micron bipolar transistor (Ic = 10 mA).

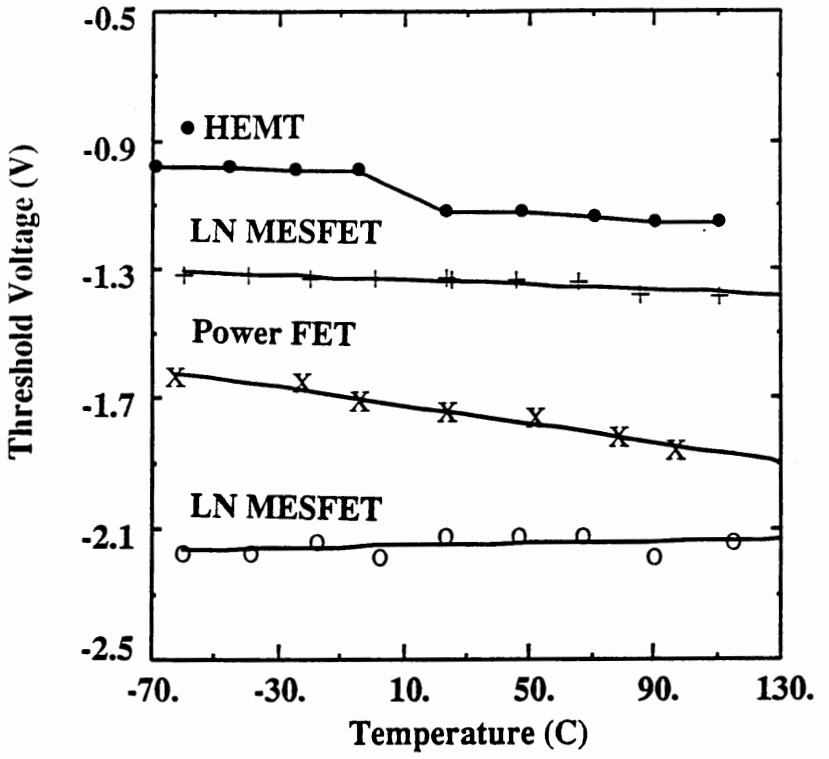

Figure 2. Differences in MESFETs and HEMT threshold voltages versus temperature

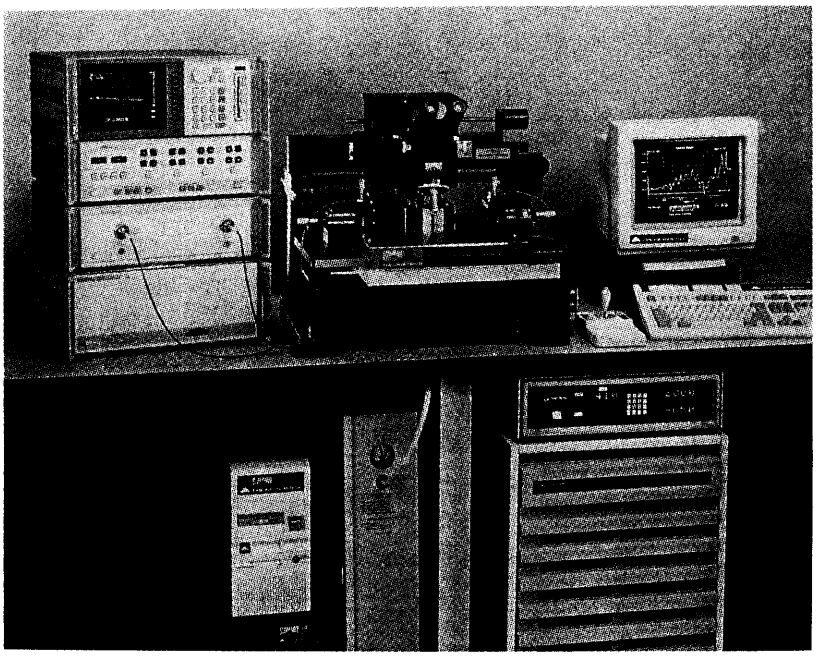

Figure 3. The Summit 10600 Thermal Probing System shown with an HP 8510 Network Analyzer.

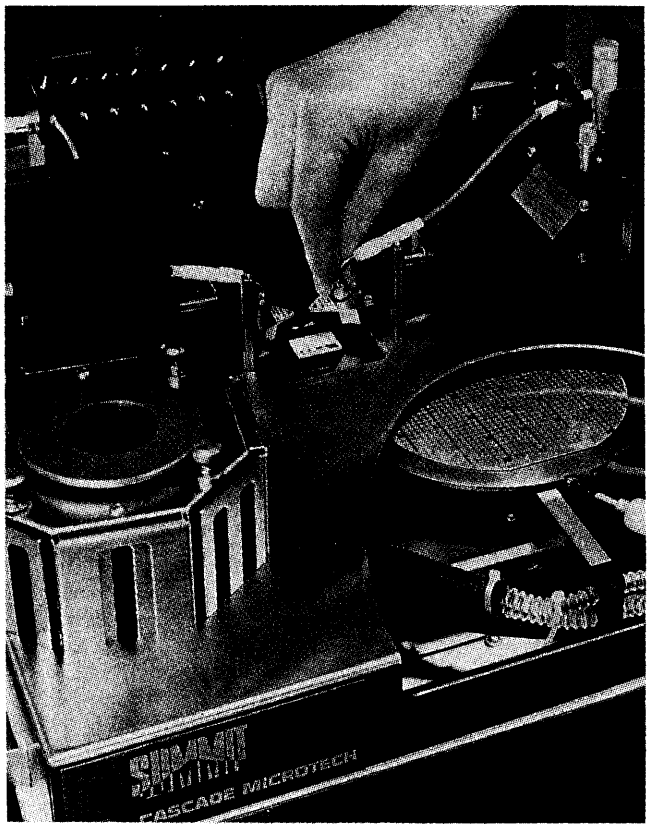

Figure 4. Close-up of the small volume Summit MicroChamber™ and thermal chuck assembly.

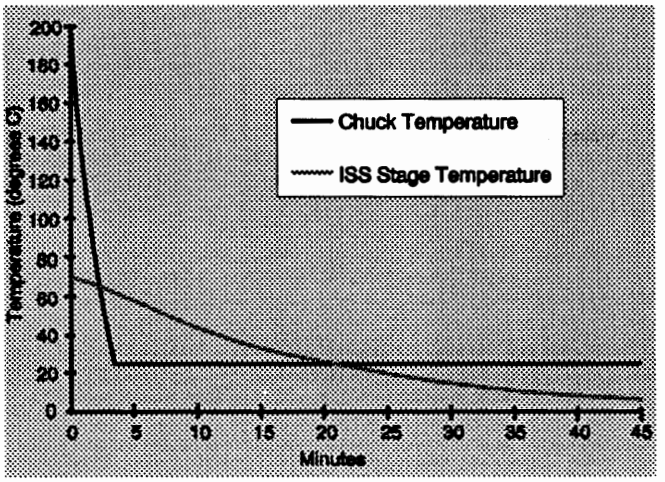

Figure 5. Temperature excursions of wafer stage and ISS stage over time.

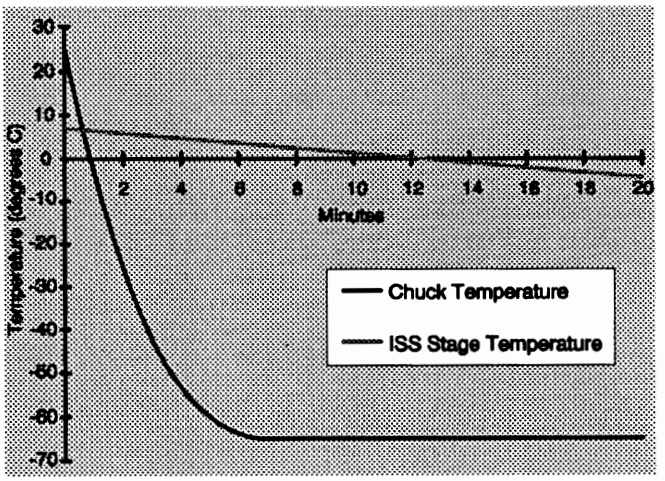

Table A.

When reading taken	Room temperature Cal stability value (dB)	At-temperature Cal stability value (dB)
After room temp. cal	-55	n/a
After 125 deg. cal	-32	-50
After 125 device measurement	-20	-40
After 50 deg. cal and measurement	-36	-55
After -60 deg. cal and measurement	-25	-36
Return to room temp	-35	n/a

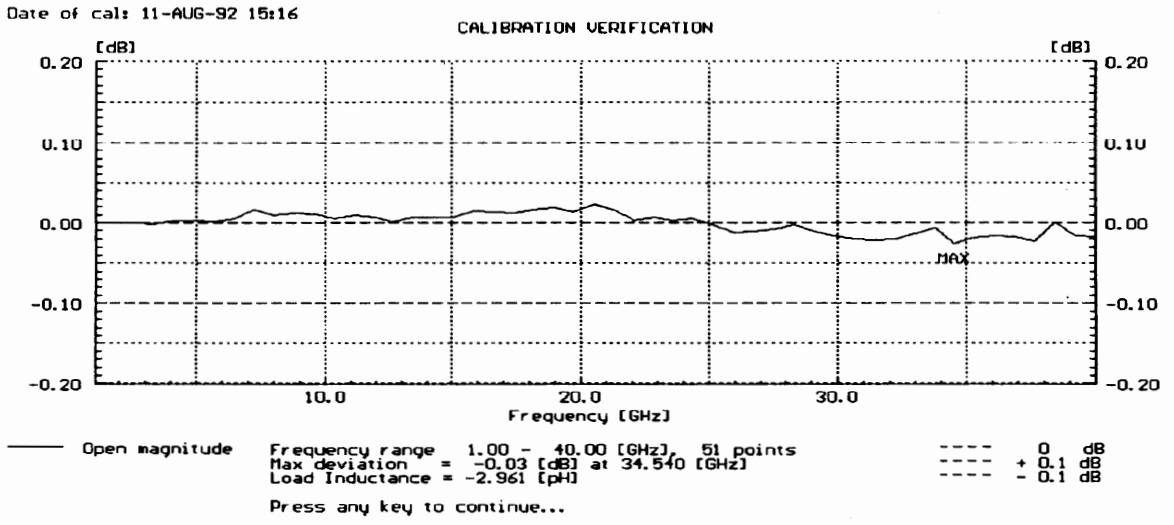

Figure 6. Plot of calibration stability on the Summit Thermal Probing System.

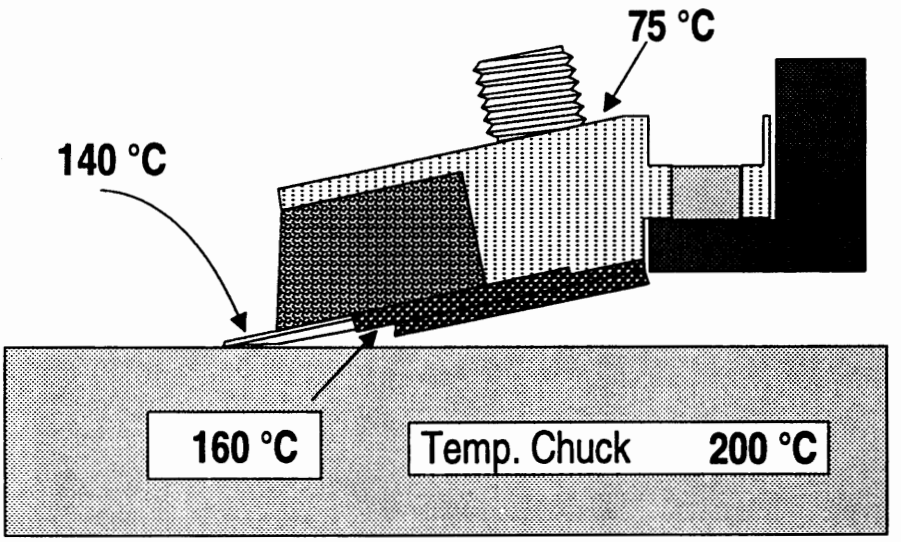

Figure 7. Temperature readings across a WPH probe when the chuck is at 200° C.

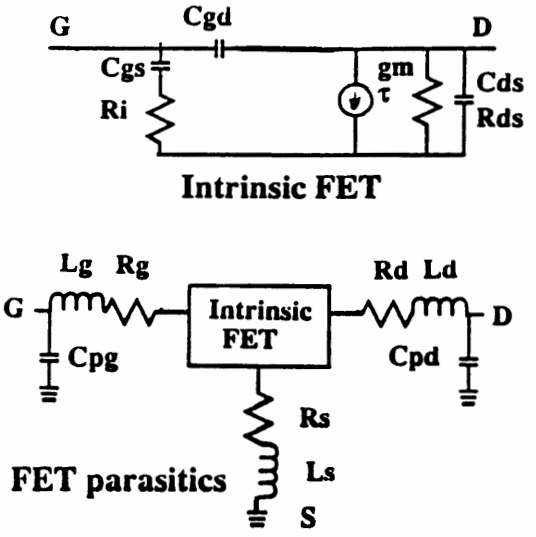

Figure 8. FET equivalent circuit.

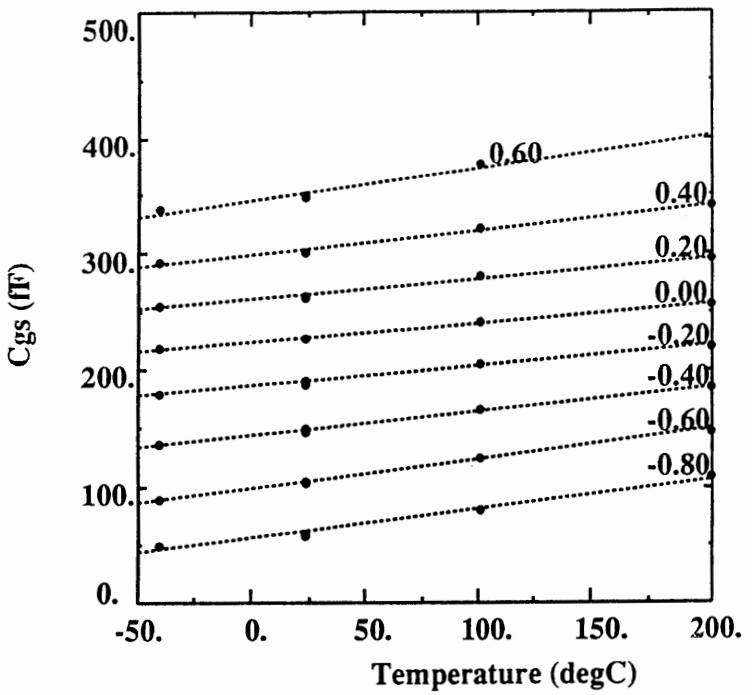

Figure 9. Temperature dependence of gm at various gate voltages.

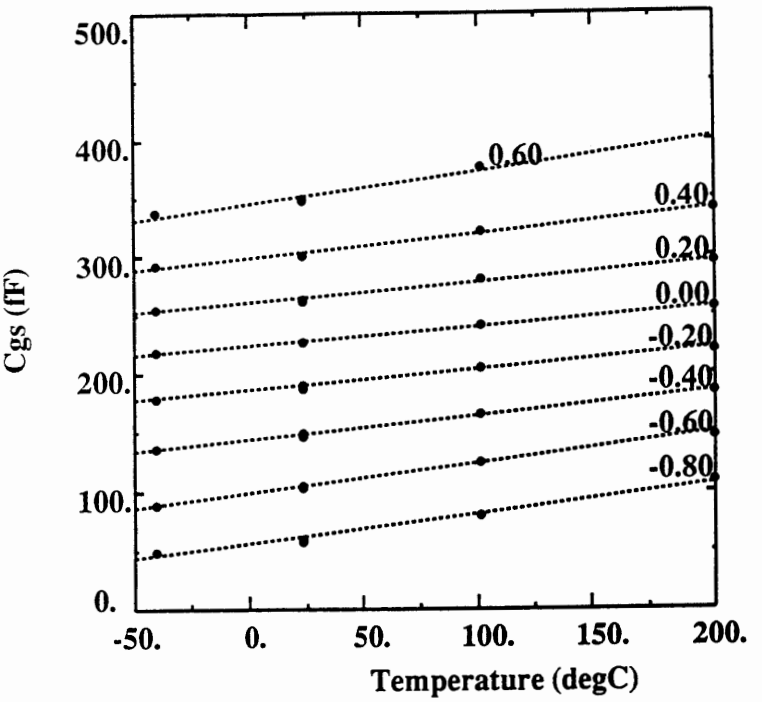

Figure 10. Temperature dependence of Cgs at various gate voltages.

Temperature Coefficients and Percent Differences for Cray MESFETs

Parameter	B(RT)	B(T)	Δ(RT)	Δ(200)	Δ(-40)
gm (Idss)	-1.09(-3)	-1.16(-3)	0.8%	-0.2%	-0.4%
Cgs (Idss)	0.91	0.74	0.45	2.6	-0.74
Cgd(Idss)	-0.22	-0.11	-1.4	-2.0	0.47
Rds(Idss)	0.2	0.7	-1.0	-7.3	2.2
τ (Idss)	1.7	2.1	-0.04	-4.0	2.9
Ri(Idss)	2.4	1.6	-2.5	6.4	-6.2
f_t(Idss)	-1.69	-1.62	0.66	1.9	0.6
g_m/ Cgs+ Cgd	-1.65	-1.64	0.45	1.0	0.25
Rs	1.44	1.52	0	-1.3	0
Rd	2.03	1.87	0.3	0.23	-2.0
Rg	5.2	4.2	0.6	2.3	-12.6
Ld	1.2	0.43	1.1	19	-2.
Lg	2.6	1.4	-2.2	11	-9.
Cpg	2.4	1.15	-1.9	14	-6.3
Cpd	2.2	1.23	1.0	9.4	-2.0
Cgd,pinch	0.44	0.51	-0.7	-1.3	0
Idss	0.8				
δV_p	-1.57mV/°C				

Table B

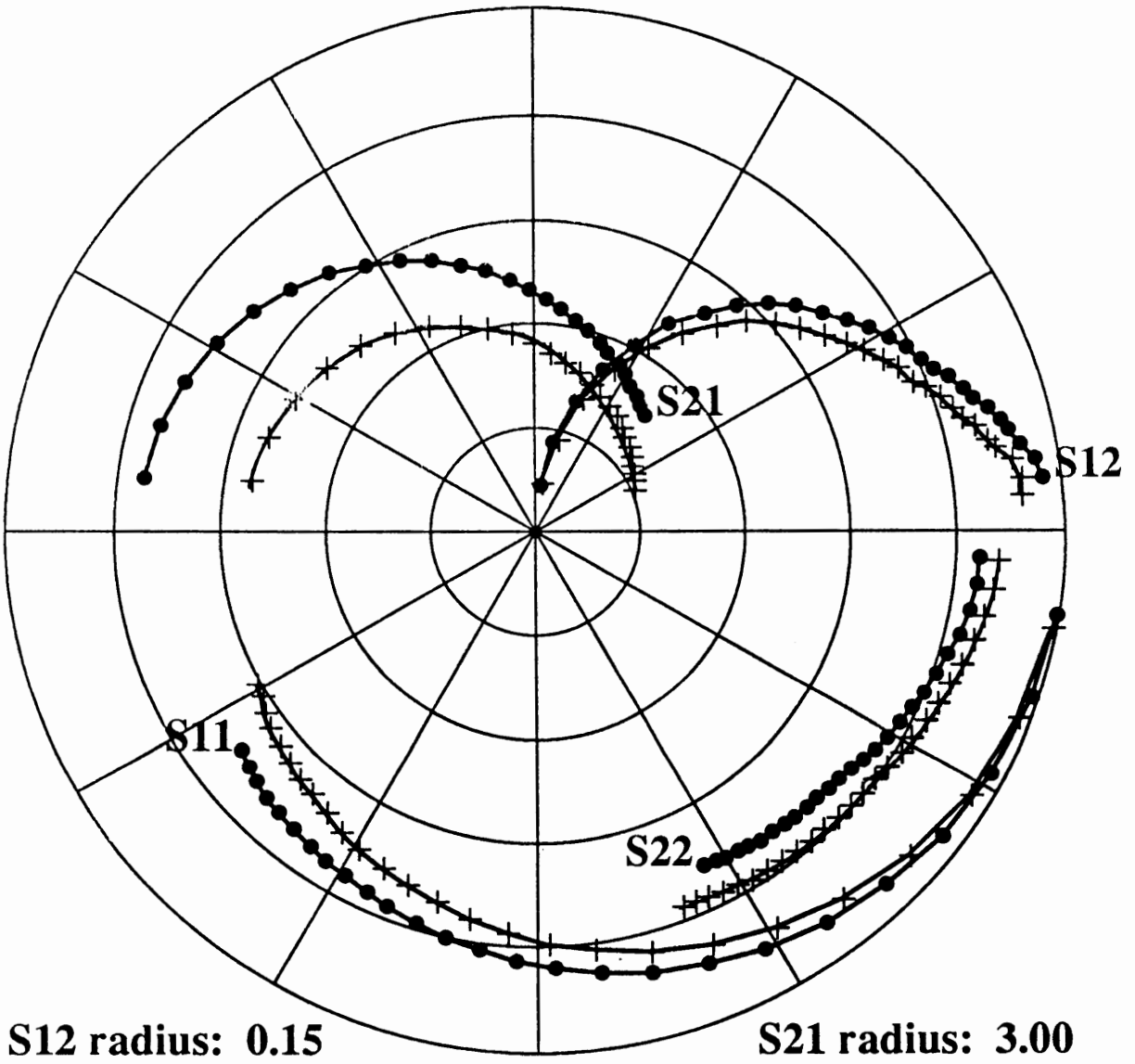

Figure 11. S-parameters at Idss at -40° (•) and 200° (+)

Device Characterization with an Integrated On-Wafer Thermal Probing System

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Background

Most wireless IC applications require operation at temperatures that fluctuate widely from the ambient temperature used in the test environment. As wireless applications become more technically demanding and are driven toward higher yields, accurate device models based on temperature-dependent RF equivalent circuits become critical. Several large semiconductor companies are now actively monitoring or controlling chuck temperature in production for commercial applications.

Wireless applications across the world subject communications systems to extremes ranging from the bitter chill of an Alaskan winter to the scalding heat of an Ecuadorian summer. Customers demand performance in these wide ranging thermal environments requiring survival of ICs in both storage and operating conditions. Characterizing the performance of these ICs over temperature is most economically accomplished at the wafer level.

Historically, high-frequency on-wafer measurements over temperature have been prohibitively expensive and inefficient. Previous test setups have involved a collection of probe station, Plexiglas dry box, probes, and cables. These setups take weeks to install and debug since the components are autonomously designed. Since a dry box encapsulates the entire probe station, these systems also provide poor throughput due to the large volume that must be purged to avoid frost at low temperatures. Also, the issues of on-wafer calibration accuracy and stability caused by temperature-related probe and cable drift have been erroneously ignored.

Temperature-dependent device models

In order for ICs or communication systems to perform effectively over temperature, accurate, temperature-dependent device models must be generated. Both silicon- and GaAs-based devices are being designed into wireless systems. Measurements of silicon bipolar devices at Cascade Microtech show that f_t as a function of temperature can be non-linear (Figure 1). To accurately characterize f_t at any temperature, parasitic pad capacitance must be determined and removed. Cascade's algorithm first measures and stores a "dummy device," consisting of only the pads and interconnects. Subsequent measurements are calculated by subtracting the "dummy" from actual device data to obtain a correct f_t. Interestingly, competing physical factors contribute to

a curvilinear f_t response versus temperature for a single bias point. The bias point could be adjusted to find the optimal f_t at any given temperature. A thorough evaluation for a GaAs MESFET is presented[1] to understand several potential temperature dependent physical factors including:

- the materials factors (energy gap, Nc, Nv, dielectric constant)
- the electron saturated velocities and mobilities
- the contact resistance
- the Schottky-barrier height and the surface potential
- trap-related phenomena.

In summary, for the devices measured, the temperature coefficients suggest a stronger dependence of the electron velocity and a weaker dependence of the electron mobility on temperature than previously thought. The most dominant factor where these GaAs MESFET performance data is concerned is the reduction of the electron velocity with temperature. This causes f_t values and thus gain values to decrease significantly with temperature, even for devices biased at a constant current. HEMT devices also exhibit much stronger shifts in threshold voltage near 0° C than MESFETs, indicating trapping effects and making derivation of linear temperature coefficients impossible (Figure 2). Thus, temperature stable circuit designs with HEMT technology is more difficult.

Measurement setup and algorithms

High-frequency measurements were made at -40, 23, 100 and 200° C with the Cascade Microtech Summit Thermal Probing System (Figure 3) and microwave probes. The 23° C measurement was repeated at the end of the sequence to verify that the device and system was stable. Transitions to sub-zero temperatures were expedient since the Summit uses a MicroChamber™ environment (Figure 4) enclosing only 7.0 liters, to allow purging in a matter of minutes instead of hours required with traditional Plexiglas dry boxes that surround an entire probe station. At each temperature, the system was recalibrated using LRRM calibrations with automatic load inductance correction[2]. This load inductance compensates for the micron-level misplacement of the probes on the standards to obtain the correct reference reactance. Two sets of measurements were taken over a series of bias conditions using the room temperature calibration and an at-temperature calibration. The at-temperature calibration was performed about fifteen minutes after making a chuck temperature change, roughly three times the thermal time constant of the probes and cables.

Calibrations were performed by contacting a separate ISS, or impedance standard substrate, located on a separate thermally-isolated stage. When the

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[1]R. Anholt and S. Swirhun, "Experimental Investigation of the Temperature Dependence of GaAs FET Equivalent Circuits," IEEE Transactions on Electron Devices, Sept. 1992.
[2]A. Davidson, K. Jones, E. Strid, "LRM and LRRM Calibrations with Automatic Determination of Load Inductance, " ARFTG Digest, Winter 1990.

main chuck is at -65° C, the calibration chucks stabilize at -5° C (Figure 5). The calibration substrates, consisting of shorts, thrus, and loads are relatively insensitive to temperature. The element most affected by temperature is the 50-ohm resistor, exhibiting a TCR of -100 ppm/°C. Therefore, worst-case deviations of the resistor for a -65 to 200° C wafer chuck excursion adds only a 0.7% error.

The microwave probes are constructed to withstand the large thermal excursions, especially high heat. Even after prolonged exposure, Figure 6 shows that the most temperature-sensitive component of the probe, the coaxial connector, is comfortably below its rated specification of 85° C. The air flow purge minimizes the thermal coupling between chuck and probes and cables. RF cables tend to exhibit significant phase changes with temperature so recalibration is generally recommended for temperature excursions of greater than 25° C.

The Cascade Microtech Thermal Probing System offers sophisticated software algorithms for fast and easy network analyzer calibrations at-temperature. To get a good comparison, the probes were left in contact with the device while the different calibration sets were recalled. This removes the unwanted effect of measurement errors caused by varying probe placement, which is the leading cause of poor on-wafer high-frequency measurement repeatability. After each measurement run, a calibration stability reading was taken to understand quantitatively the changes from continued temperature settling of probes and cables (Table A). This test requires a measurement of an open so no probe placement issues are raised. Generally, Cascade Microtech recommends recalibrating whenever the cal stability gets worse than - 40 dB or 1% (Figure 7). To further reduce probe placement errors when measuring multiple devices on a wafer, a look-up table can be created by the Summit station to store x-y stage correction values which compensate die-to-die movements for wafer expansion effects as a function of temperature.

Effects of system calibration on FET temperature-dependent equivalent circuits

The device used in the experiment was a 2 x 75 x 0.8 micron MESFET. The layout is a symmetric multi-finger, ground-signal-ground arrangement with active fingers pointing in the direction of the gate-drain probe axis. Figure 8 shows the equivalent circuit for this device. Previous investigations used only a single room temperature calibration, which may have lead to erroneous derived temperature coefficients, especially for capacitances which may be susceptible to changes in transmission line lengths with temperature. About 8 gate biases were measured at Vds = 2V, then 3 cold-FET and one pinched-FET measurement was made at Vds = 0 V.

The direct extraction technique[3,4] was employed involving three cold-FET measurements (Vg = 0.8, 1.0 and 1.2 V) to derive the source, drain, and gate

[3]R. Anholt and S. Swirhun, "The measurement and analysis of GaAs MESFET parasitic capacitances," IEEE MTT vol. 39, pp. 1243-1246, July 1991.

resistances and inductances. At high temperatures, however, the alpha-method gave inconsistent ratios of the channel to source resistence, forcing the value to be fixed at the room-temperature measurement. The pinched-FET measurement (Vg = -4.0 V, three volts below pinchoff) was used to estimate pad capacitances, as no dummy-FET or width-dependent capacitance data was available for this layout. The difference between Cgs and Cgd for the pinched FET is approximately equal to the gate-pad capacitance Cpg, and Cds is equal to the sum of the drain-pad capacitance, Cpd, and the active-FET drain-source capacitance. The part due to Cpd was estimated at room temperature and the ratio of Cpd to the total pinched-FET value of Cds was kept constant for other temperatures. Empirically, the best value of Cpd gives the best hot-FET S_{12} fits. Also, the resulting value of Cpd and Cpg are approximately equal given the symmetric layout. The resulting direct-extracted equivalent circuit parameters generally had less than 3% variations from 1 to 26 GHz.

Figures 9 and 10 show typical temperature dependent equivalent circuit parameters for gm and Cgs at various gate voltages (Vds = 2V). The data is quite consistent and easily fits to

$$P(Vg,Vds,T)=P(Vg,Vds,To)(1+B(T-To))$$

where To=0° C and B varies with gate and drain voltages. This FET exhibited a very steep threshold-voltage shift with temperature, and as a result the Ids and gm values tended to have negative temperature slopes at high Vg (due to reduced electron saturated velocity at high temperature), whereas they show a positive slope at low Vg due to the lower threshold voltage.

Table B summarizes the resulting temperature coefficients B. For each parameter, B(RT) was derived using S-parameters measured with the original room-temperature calibration. B(T) was obtained by using the at-temperature calibration. The largest differences in the B coefficients are in the pad capacitances Cpg and Cpd as well as in the inductances Ld, Lg, and Ls. Ls is not shown since its value is nearly zero. We believe the differences in B values for Rds, τ, and Ri are secondarily due to pad capacitance deviations since emperical studies show that these parameters are very dependent on what is assumed for these inductances and capacitances.

Differences in the B coefficients are generally due to very small differences in the extracted equivalent circuit parameters. To test their significance, a comparison to the relative change Δ in each parameter due to using the room-temp or at-temp calibration at 200° and -40° C was performed. The S-parameters are shown in Figure 11. S-parameters for room-temp measurements done at the start and end of the session was provided in Δ(RT) for system stability information. If the difference in parameters at 200° or -40° C is not much larger than Δ(RT), the differences in B coefficients are insignificant. For example, Cgs was measured at 223.8 and 224.8 fF in the room-temp measurements, so Δ=0.45%. At 200° C, Cgs was extracted at 253.6 and 260.1

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[4]R. Anholt and S. Swirhun, "Equivalent-circuit parameter extraction for cold GaAs MESFETs," IEEE MTT vol. 39, pp. 1247-1252, July 1991.

yielding a Δ=2.6% so we conclude that the difference of 9.1 and 7.3x10^{-4}/° C in B for Cgs is significant. However, the differences in the f_t values and the pinched-FET value of Cgd are not.

Conclusions

A turnkey thermal probe station can minimize the setup and debug time needed to gather over temperature S-parameter data for equivalent circuit extractions and RF circuit designs. Simple software-aided routines and ergonomic controls make it feasible to gather data over a wide range of temperature settings to capture non-linear effects such as the Vt of a GaAs HEMT or the f_t of a silicon bipolar device. One-button calibrations at each measurment temperature yield more accurate FET equivalent circuit temperature coefficients, especially for the parasitic pad capacitances and inductances.

Acknowledgements: The authors would like to thank Tom Myers at Cascade Microtech for providing helpful test software modifications.

Integrated-Circuit Technologies for Wireless Applications

Session Chairperson: Dan Millicker, *Hewlett-Packard Co., Communications Components Division (Newark, CA)*

HEWLETT PACKARD

Direct vs. Dual Conversion
Quadrature (vector) Modulation

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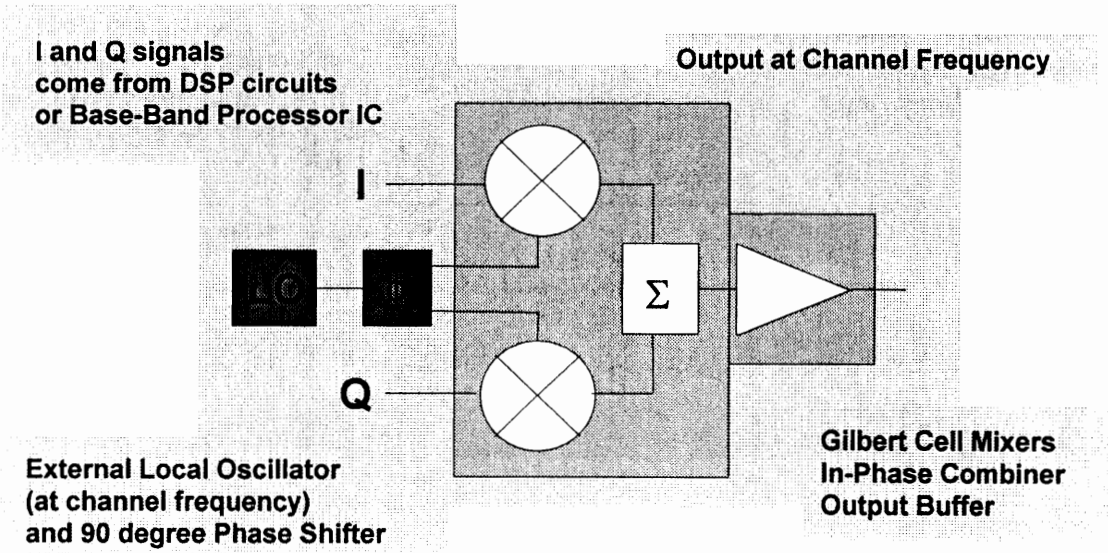
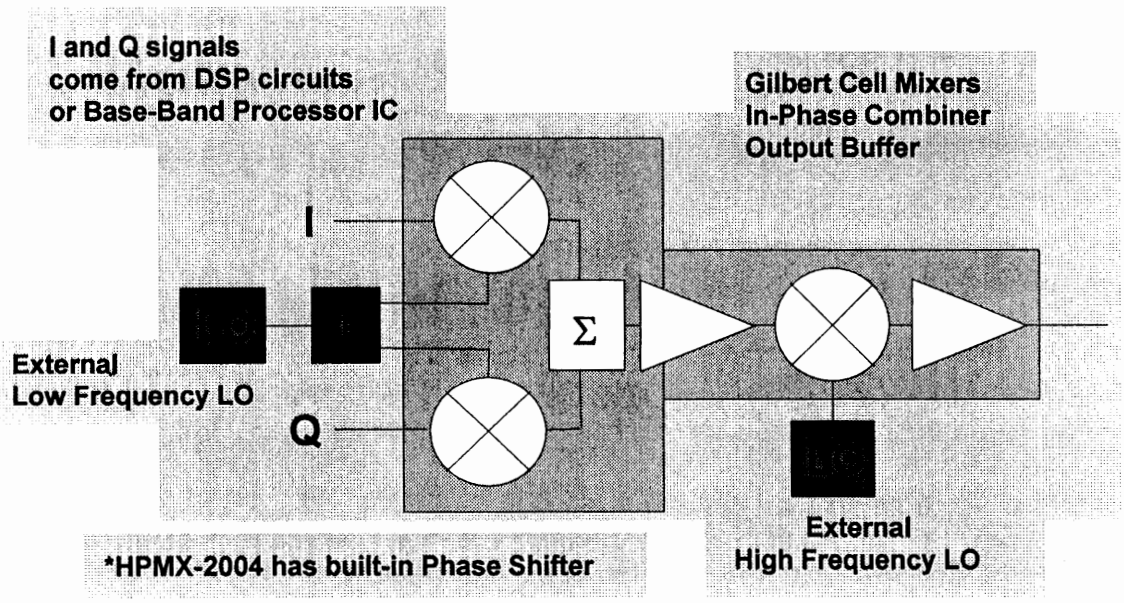
Direct Conversion (HPMX-2001)



Dual Conversion (HPMX-2002, HPMX-2004)



Direct Conversion

(+)
Simple
Low DC Power
Low Cost

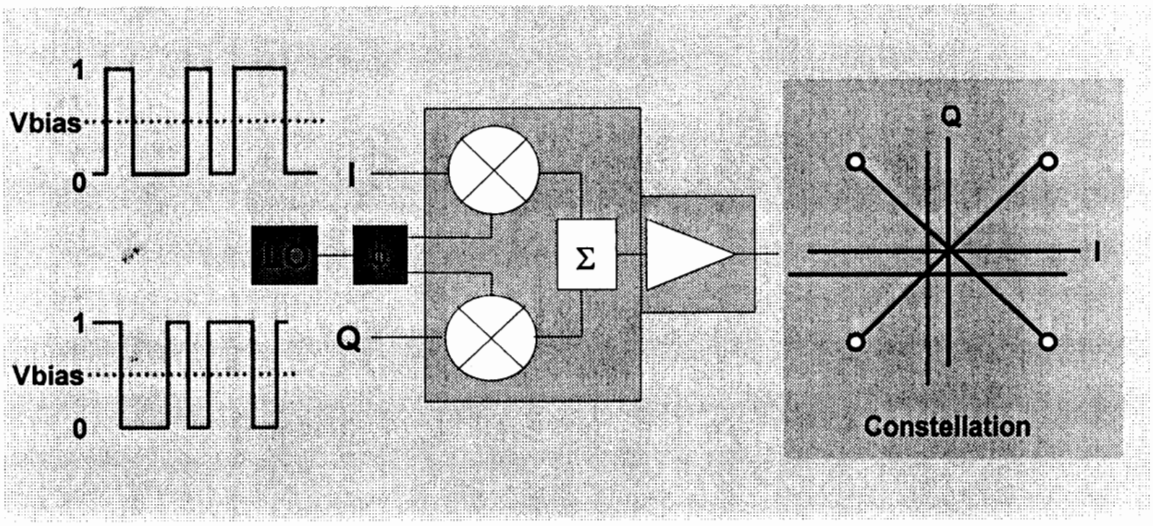
(-)
Filters
Shielding

Dual Conversion

(+)
Cheap Filters
Better Isolation

(-)
More Filters
More Complex
DC Power?

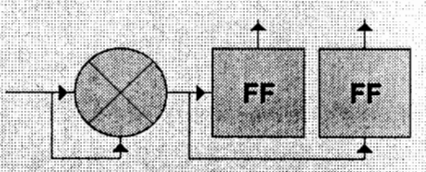
LO Leakage



Adjusting Vbias at I and Q shifts the I and Q axes onto the "ideal" axes.

Phase Shifters

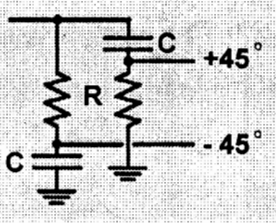
Hybrids (Murata, Shoshin)



Active "Digital" Phase Shifter
(HPMX-2004 uses this technique)

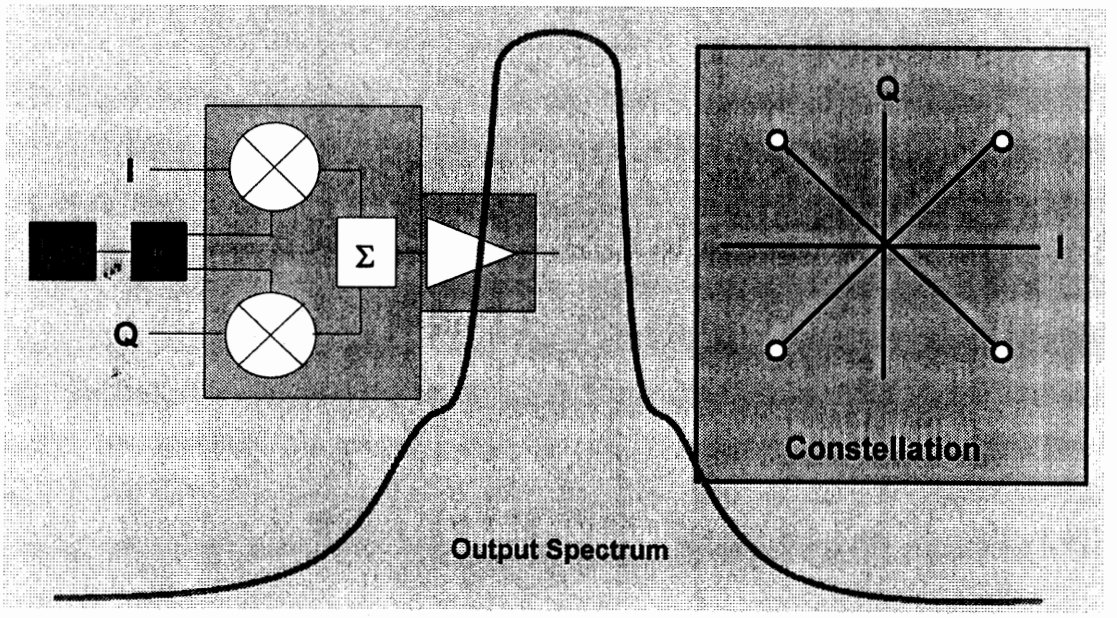
LO input

$f_{LO} = 1 / (2\pi RC)$

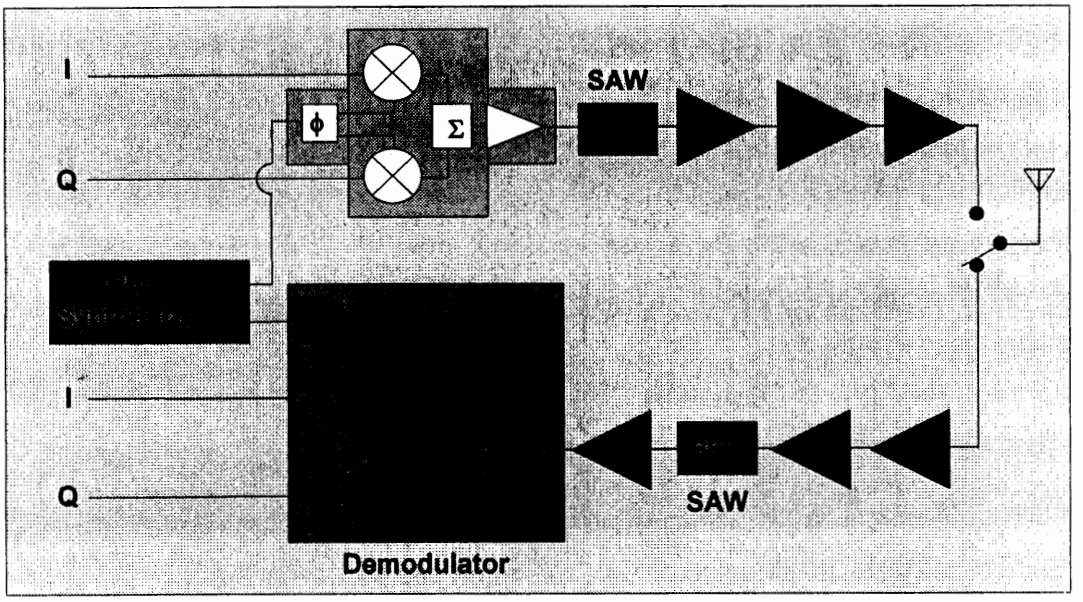


RC networks

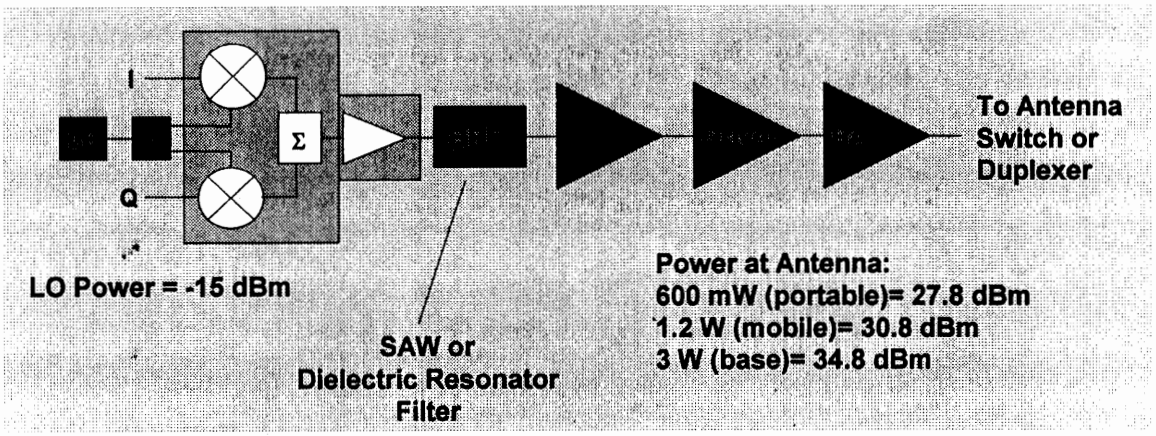
Direct Conversion



Direct Conversion

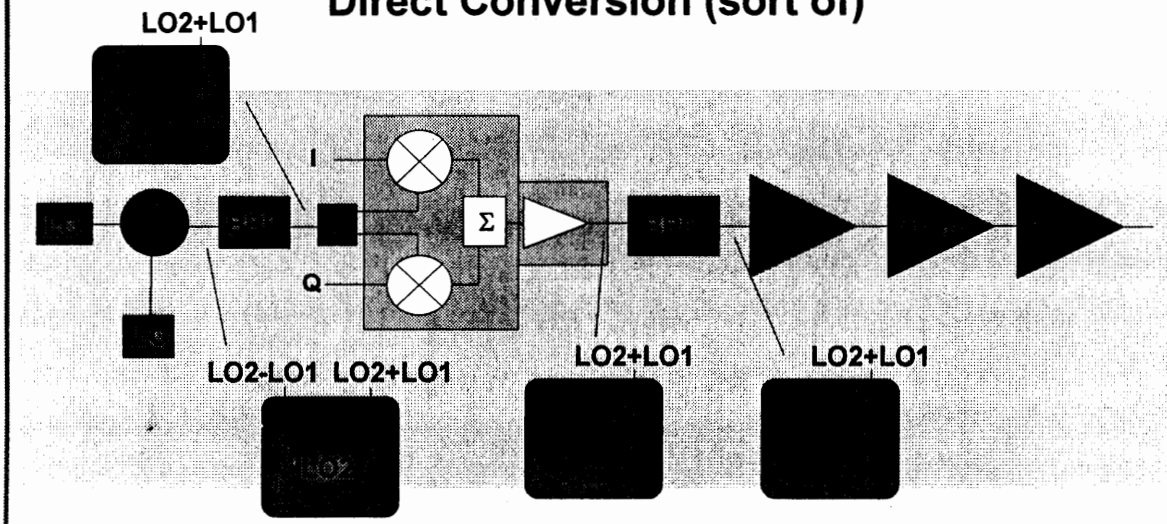


Direct Conversion Transmitter



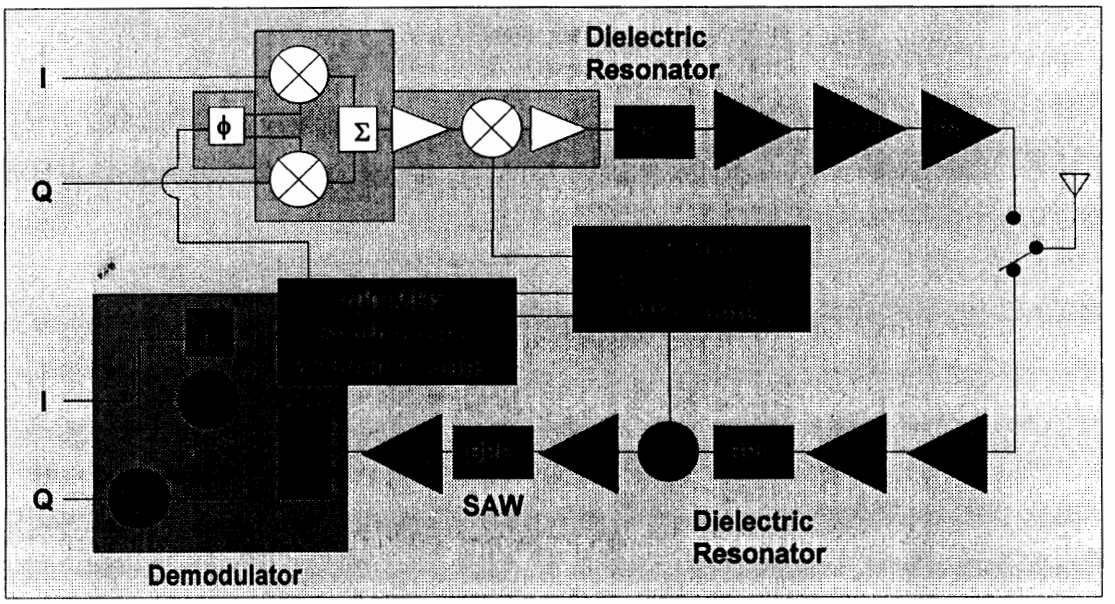
Problem: amplified signal leaks back into LO causing spurs and other
Solution: Metal shields over LO and modulator with careful attention to
all leads going in and out of shields

Direct Conversion (sort of)

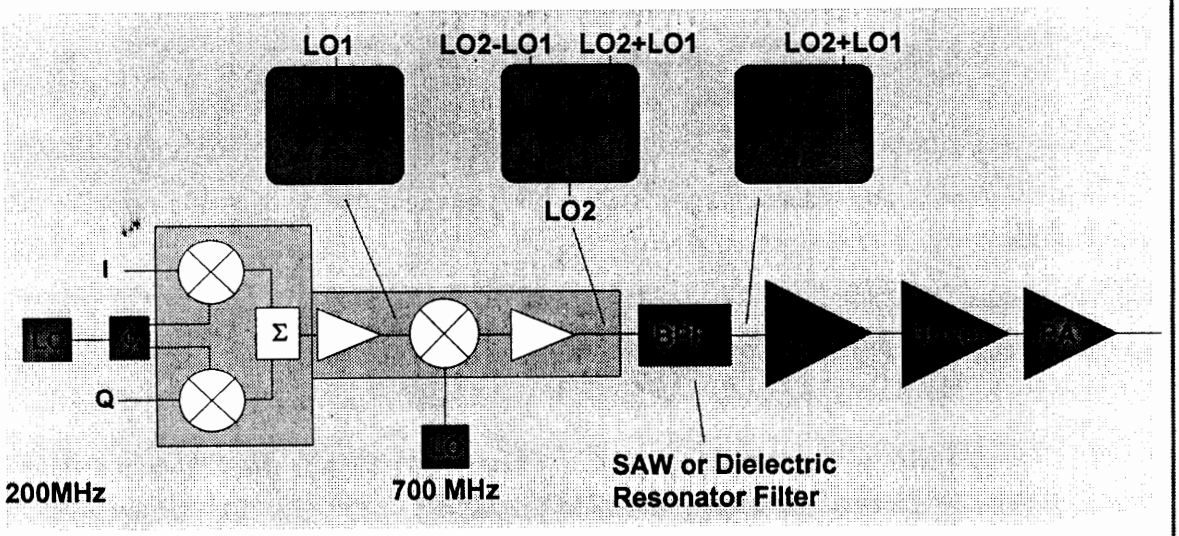


Problem: Shielding is impractical, reverse isolation too low
Solution: Use mixer and filter at input of modulator to allow
use of radio on LO frequency

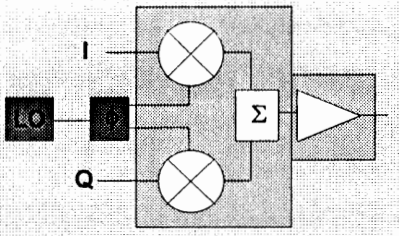
Dual Conversion



Dual Conversion (HPMX-2002, HPMX-2004)



Direct Conversion

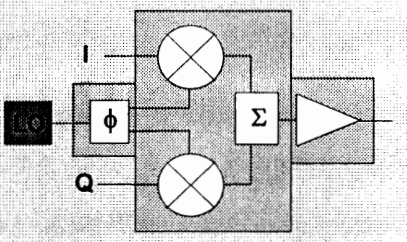


HPMX-2001

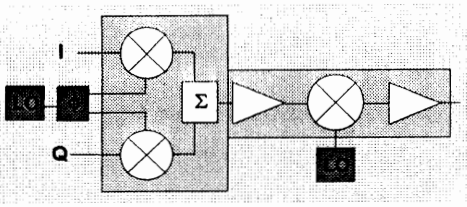
Pout = -9.5 dBm (900 MHz)
Id = 20 mA
LO: DC - 2000 MHz

HPMX-200C (coming soon)

Pout = +4 dBm (900 MHz)
Id = 39 mA
LO: 800 - 1000 MHz

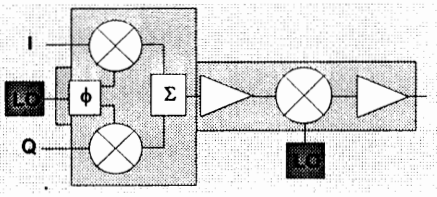


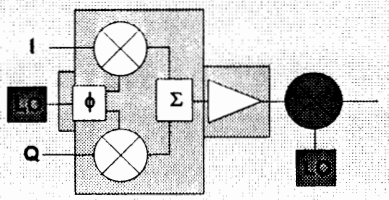
Dual Conversion



HPMX-2002
Pout = -11 dBm (800 MHz)
Id = 12.2 mA
LO1: 40 - 300 MHz
LO2: 250 - 2000 MHz
Output: 250 - 2000 MHz

HPMX-2004
Pout = -13 dBm (800 MHz)
Id = 30 mA
LO1: 40 - 240 MHz
LO2: 250 - 2250 MHz
Output: 250 - 2000 MHz

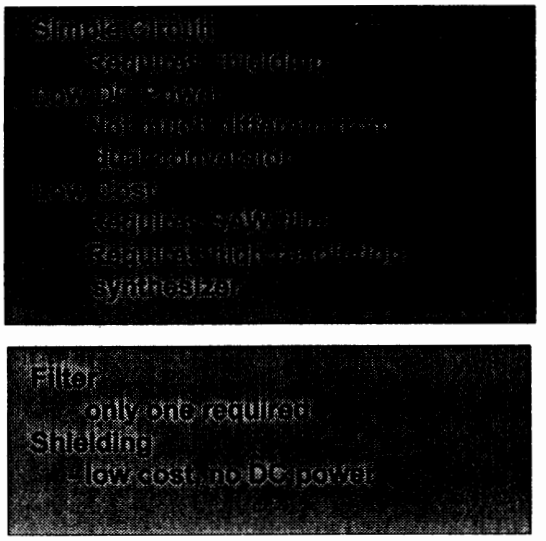




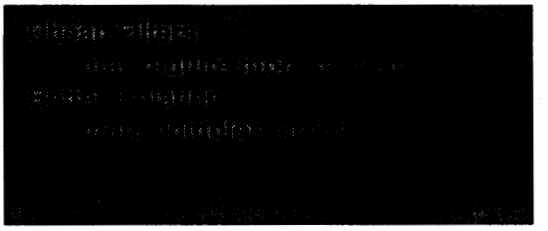
HPMX-200E (coming soon)
Pout = -4.5 dBm (100 MHz)
Id = 16 mA
LO: 45 - 200 MHz

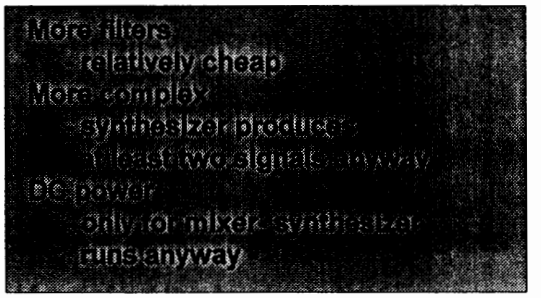
Direct vs. Dual Conversion

Direct Conversion:



Dual Conversion:





Choose your Headache!

Silicon Bipolar RF Integrated Circuits for Cellular Radio and Wireless Applications

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Communications Components Division
Hewlett Packard Company
Newark, California 94560

I. Introduction

The current development of digital cellular radio systems with high spectral efficiency places significant demands on the associated r.f. components. This includes high levels of r.f. performance with low noise, high power, and adequate suppression of undesired signals. These requirements are combined with desired operation at low voltage and current to prolong battery life, and a high level of integration to reduce the overall system size and cost.

A typical radio system is illustrated in Fig. 1. RF components on the transmit section include a quadrature modulator to up convert DSP (digital signal processing) data. This is followed by a driver and output amplifier capable of power control. The receive side includes a low noise amplifier (LNA), a down-converting mixer, and appropriate phase-locked loop circuitry. This paper will discuss the quadrature modulator, the driver amplifier, and the LNA and down-converting mixer circuits for use in the 800 MHz to 960 MHz communication bands.

The ISOSAT-II silicon bipolar IC technology used to fabricate these circuits is illustrated in Fig. 2. Bipolar devices feature a transition frequency f_T of 10 to 20 GHz, and a maximum frequency of oscillation f_{max} of 25 GHz. A thick field oxide and a low resistance gold metallization system are used to achieve low parasitics for interconnections and polysilicon resistors. This structure also provides for high-Q capacitive and inductive elements [1]. The use of LC elements for reactive tuning can significantly improve the overall performance of these circuits.

II. Quadrature Modulator

As digital modulation techniques are incorporated into wireless communications to increase system capacity, the quadrature modulator becomes an increasingly important component. Ideally, its basic function is to provide a one-to-one correspondence between the input voltage at the in-phase (I) and quadrature-phase (Q) ports and the amplitude and phase of the output signal.

Two fundamental methods are commonly used to achieve this modulation: a direct modulation of the r.f. signal (approximately 900 MHz) and a two-stage up-conversion process involving the modulation of an i.f. signal (approximately 100 MHz) followed by an up-conversion to the r.f. band. Two ICs were developed to perform the quadrature modulation required by these systems.

The basic functional diagram for both the 100-MHz and 900-MHz quadrature modulators is shown in Fig. 3 [2]. A carrier frequency ω_c is applied to an RC-based phase shifter that generates two signals in quadrature, $\sin(\omega_c t)$ and $\cos(\omega_c t)$. These signals are then applied to the LO sections of two Gilbert-cell based double-balanced mixers that are driven by appropriate I-Q representations of digital data. The outputs of the two mixers are then summed and amplified.

Single-ended high-frequency outputs are desirable since they eliminate the need for output combining circuitry such as baluns. The amplifier topology in both quadrature modulators is designed to provide single-ended operation. In the case of the 900-MHz version, the output is matched internally to a 50-Ω impedance using a shunt-L series-C network. The on-chip matching not only provides the user with an ac-coupled 50-Ω output line, but also improves the power efficiency by eliminating losses associated with matching a high-impedance node external to the IC.

A variety of measurements can be used to characterize the performance of a quadrature modulator. Many are based on the correspondence between the input plane (I-Q modulating voltage) and the output plane (r.f. amplitude and phase). Figure 4 depicts the basic mapping function. The input axes I and Q are the voltages of the I and Q modulation ports above their reference voltage. The output is ideally proportional to

$$I \cdot \sin(\omega_c t) + Q \cdot \cos(\omega_c t). \tag{1}$$

Mapping of a variety of inputs is investigated. For the 900-MHz quadrature modulator they are:

1) a high power output versus frequency with I = Q = 1.25 V (above a reference level of 2.5 V) (point A, Fig. 4);
2) a leakage output power versus frequency with I = Q = 0 V (at the reference level) (point B, Fig. 4);
3) a sequence of points to determine the amplitude and phase mapping uniformity of the modulator (points C, Fig. 4).

Additionally, a low-frequency modulating signal ω_m can be applied to the I-Q ports with the following spectral results:

4) a single sideband up-conversion spectrum obtained from

$$I = 1.25\,V \cdot \sin(\omega_m t),\ Q = 1.25\,V \cdot \cos(\omega_m t); \tag{2}$$

5) a double sideband up-conversion spectrum obtained from

$$I = 1.25\,V \cdot \cos(\omega_m t),\ Q = 1.25\,V \cdot \cos(\omega_m t). \tag{3}$$

Figures 5 through 9 show the results of these tests for the 900-MHz quadrature modulator. The high power sweep (Fig. 5) corresponds approximately to a 0.5-dB gain compression level. The optimum power at 900 MHz, as well as the low output VSWR, result from the reactive output impedance matching used. Figure 6 shows the LO leakage versus frequency. This parameter is highly sensitive to internal device-to-device variations and can be improved by 10 to 20 dB by individually applying small offset voltages to the I and Q ports. Gain and phase mapping errors are shown in Fig. 7. A sequence of relative output amplitudes and phases are obtained from S_{21} measurements as the input I-Q vector traces a circle of 1.25-V magnitude. Ideally, the magnitude of S_{21} should remain constant and the phase of S_{21} should track the phase of the input I-Q vector. Deviations from the average magnitude and phase are shown versus input angle of the I-Q vector. Applying low-frequency quadrature inputs results in a single sideband up-conversion spectrum shown in Fig. 8. In addition to the desired sideband, the LO leakages and image suppression are also visible. Caution must by used in evaluating non-linear products from this spectrum since the signal, if passed through a limiting amplifier, would further suppress unwanted tones. Figure 9 shows a measurement of third-order distortion products. Here a two-tone output of a quadrature modulator is obtained from dual in-phase I and Q inputs. The third order products are at 35 dB below the fundamental tones of 0 dBm while the device is biased at 5 V and 37 mA.

III. Driver Amplifier

The driver amplifier receives a signal from either an up-converting mixer or a direct quadrature modulator and amplifies it to an output level of about 200 mW. Since the driver amplifier must consume a large amount of current in order to deliver the required output power level, heat dissipation must be carefully considered. The desirable characteristics of a driver amplifier are thus small size, low cost, good power efficiency, and ease of use in circuit board design. In many of the emerging digital cellular communication systems there is also a need for output power control over a wide range.

A driver amplifier for use in the 800 MHz to 960 MHz communication bands was developed to meet the above objectives. It is housed in a low-cost and compact S0-8 narrow body surface mount plastic package with improved heat dissipation capability. The topology of Fig. 10 was chosen for broad band operation, stability, and high efficiency. The amplifier consists of 3 gain stages, each contributing about 10 dB of small-signal gain. The first stage is a CE-CC configuration driving a CE second stage through a coupling capacitor for optimum voltage swing. These two stages have on-chip resistive loads to set proper bias level and to provide the appropriate gain. Additionally, interstage reactive matching is used to achieve maximum power efficiency. The final stage is a CE configuration with an open collector and is matched to 50 Ω externally with a shunt-L series-C network for best performance. At 900 MHz, a shunt inductor of 10 nH and a capacitor of 10 pF were used. The inductor is thus small enough to be printed on a PC board.

The driver amplifier has an on-chip biasing circuit to stabilize the amplifier gain for temperature and process variations. With $V_{CC1} = 4.5$ V, $V_{CC2} = 6$ V, and $V_{control} = 2.2$ V (which results in a total bias current of 180 mA), the amplifier achieves a measured small-signal gain of 32 dB, an output 1-dB compression point of 22.5 dBm, a third-order intercept point of 30 dBm, and a noise figure of 9.5 dB. The input return loss is 12 dB. Figure 11 shows the measured output power and small-signal gain versus frequency.

The output power can be varied over a 50-dB range with a control bias signal of 0 to 2.5 V on the second and third stages. The measured output power as a function of control voltage and frequency is shown in Fig. 12.

IV. Integrated LNA and Mixer

A family of combined low noise amplifier and mixer circuits has been developed for use in the 900-MHz cellular or 1900-MHz PCN and DECT applications. These circuits which are intended to operate as the front end for communication systems, achieve low noise performance, wide dynamic range with acceptable impedance matching over the voltage range of 3 V to 5 V.

The basic LNA topology as shown in Fig. 13 is a two-stage non-feedback circuit with reactive matching at both the input and output, and the two stages are coupled via an on-chip capacitor for optimum voltage swing. The first stage is optimized for a low noise figure and 50-Ω input impedance matching. The second stage uses emitter degeneration to set the overall gain and functions as a class-A output stage. The output impedance is matched externally to 50 Ω with a shunt-L series-C network. The LNA achieves required electrical specs through the use of user-supplied off-chip tuning elements. The input impedance and noise figure of the circuit are

approximated by

$$Z_i \approx \left(r_{b1} + \omega_T L_{g1}\right) + j\omega\left(L_{g1} - \frac{1}{\omega^2 C_{\pi 1}}\right), \tag{4}$$

$$NF \approx 1 + \frac{r_{b1}}{R_S} + \frac{g_{m1}}{2R_S|\beta(j\omega)|^2}\left[\left(r_{b1} + R_S\right)^2 + \omega^2\left(L_{g1} - \frac{1}{\omega^2 C_{\pi 1}}\right)^2\right] \tag{5}$$

$$\approx 1 + \frac{r_{b1}}{R_S} + \frac{1}{2g_{m1}R_S}\left[1 + \omega^2 C_{\pi 1}^2\left(r_{b1} + R_S\right)^2\right]$$

where ω_T is the transition frequency, R_S is the source resistance, and L_{g1} is the effective inductance at the emitter of Q_1. It is apparent from (4) and (5) that a proper input device size and a careful board layout are necessary to ensure a low noise figure and 50-Ω input impedance matching.

The basic mixer topology as shown in Fig. 14 is a double-balanced active mixer for good isolation and low LO leakages. Again, through the use of LC reactive elements, the mixer achieves a lower noise figure than previously reported Gilbert-cell active mixers for the same input linearity [3]. It also achieves narrow-band matching at the RF port with simple LC matching elements. The single-ended conversion gain of the circuit is approximated by

$$G_C \approx \frac{1}{2}\left[\frac{g_{m5}}{1 + g_{m5}(R_E / 2)}\right]\left[\frac{a_1}{2}\right] R_{Leff}\sqrt{\frac{R_S}{R_L}} \tag{6}$$

where

$$\lim_{V_{LO}\to\infty}\left[\frac{a_1}{2}\right] = \frac{2}{\pi} = -3.9\ dB$$

is due to the LO switching action. R_S is the source resistance, R_L is the load resistance, R_{Leff} is the effective output impedance, and R_E is the emitter degeneration. As a test vehicle, a separate mixer/IF circuit using the topology of Fig. 14 was implemented on the HP BCA-02 transistor array. The circuit uses a single supply of 3 V and draws a bias current of 11 mA for the mixer and 7 mA for the IF amplifier. With an RF frequency of 1900 MHz and an LO frequency of 1800 MHz, the mixer/IF circuit achieves a measured conversion gain of 13 dB and a noise figure of 11 dB. Figure 15 shows the conversion gain versus RF frequency for a constant IF frequency of 100 MHz. Also shown is the input return loss at the RF port. The conversion gain as a function of RF frequency for a constant LO frequency of 1800 MHz is shown in Fig. 16.

Each LNA/mixer circuit has an on-chip bandgap reference to stabilize the LNA gain to less than ± 0.5 dB over the –40° and +85° temperature range and to maintain the overall circuit operation as the power supply is lowered to 3 V. A power-down function is incorporated into the circuit by disabling the bandgap reference with a control voltage. The circuit is housed in a low-cost 16-lead surface mount plastic package. Simulation results at 900 MHz (two versions) and 1900 MHz for a single power supply of 5 V are shown below. As the supply voltage reduces to 3 V, the LNA's S_{21} is about 2.5 dB lower and its NF is about 0.3 dB higher. The mixer characteristics remain almost unchanged.

LNA @ 5 V and 27°C			
Frequency (MHz)	900	900	1900
I_{cc} (mA)	7.6	5.5	7.6
S_{11} (dB)	-19	-19	-8
S_{22} (dB)	-17	-16	-16
S_{21} (dB)	16.1	15.3	13.9
NF (dB)	2.1	2.2	3.4
Input $P_{-1\,dB}$ (dBm)	-16	-19.5	-16
Input IP_3 (dBm)	-5.6	-10.5	-7.0
Mixer @ 5 V and 27°C			
I_{cc} (mA)	5.5	4.6	5.5
RF S_{11} (dB)	-16	-16	-23
G_C (dB)	8.5	8.3	6.3
NF (dB)	10	10	10
Input $P_{-1\,dB}$ (dBm)	-10	< -10	-10
Input IP_3 (dBm)	4.0	3.0	0

V. Conclusion

A variety of high-performance integrated circuits appropriate for wireless communications has been demonstrated. High level of performance is achieved using the ISOSAT-II silicon bipolar process. In addition to transistor devices with excellent performance at microwave frequencies, incorporation of high-Q inductive and capacitive elements have allowed the circuits to be further optimized in the frequency band of interest. These techniques result in components with low noise, good power efficiency, and high level of integration.

References

[1] N. M. Nguyen and R. G. Meyer, "Si IC-Compatible Inductors and LC Passive Filters," *IEEE J. Solid-State Circuits*, vol. SC-25, no. 4, pp. 1028-1031, August 1990.

[2] E. A. Lee and D. G. Messerschmitt, *Digital Communication*, Kluwer Academic Publishers, Boston, 1988.

[3] J. Wholey, I. Kipnis, and C. Snapp "Silicon Bipolar Double Balanced Active Mixer MMICs for RF and Microwave Applications up to 6 GHz," in *IEEE MTT-S Digest of Technical Papers*, pp. 133-137, May 1989.

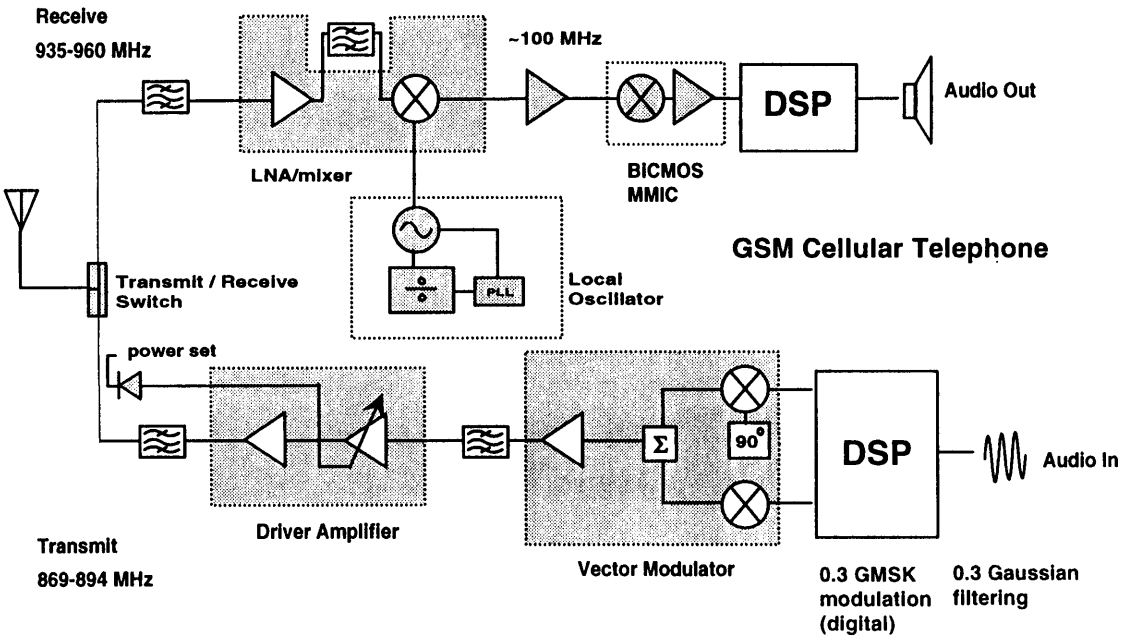


Figure 1 Typical Architecture of a Cellular Radio Handset

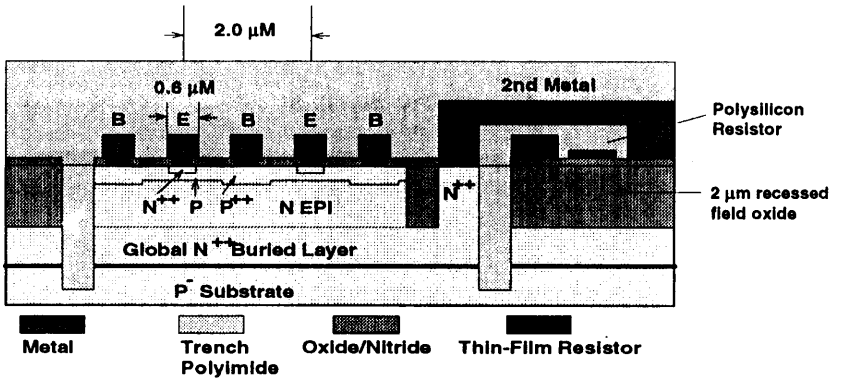


Figure 2 ISOSAT™ Process Silicon MMIC Structure

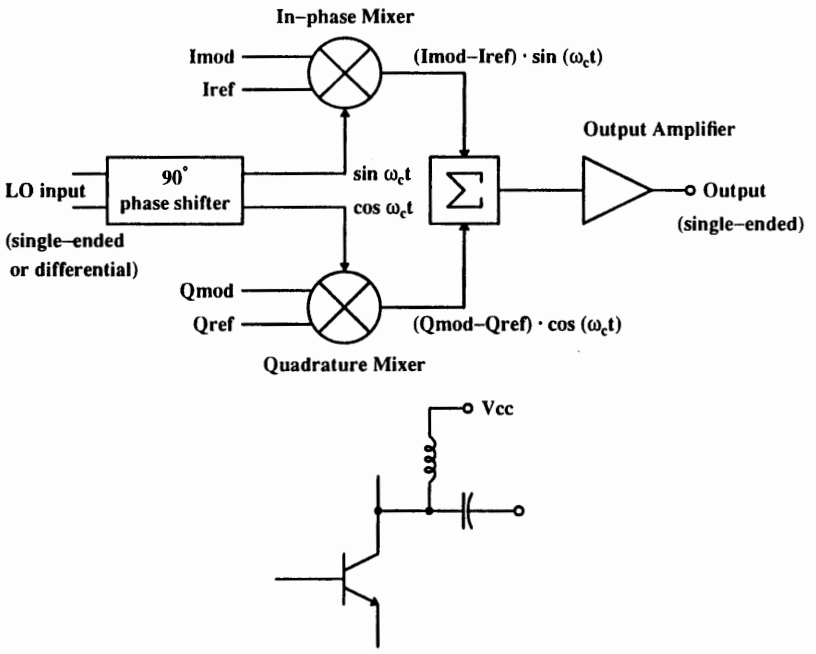
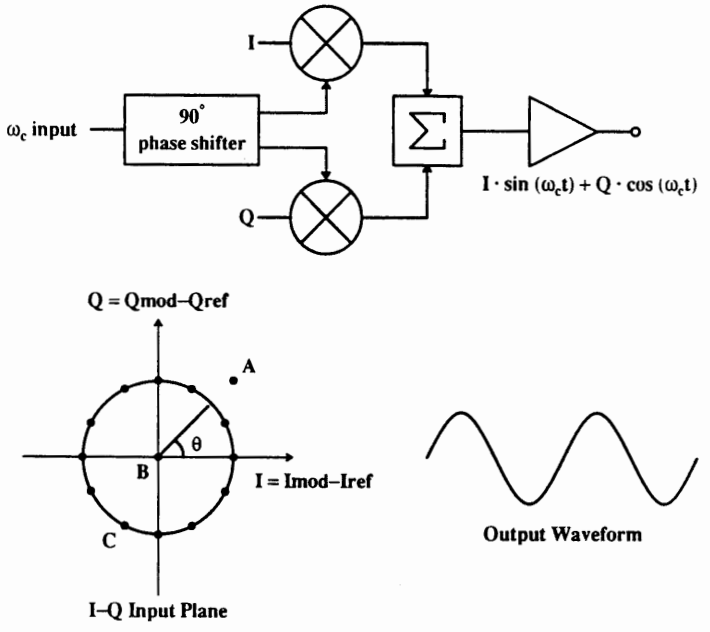


Figure 3: Functional Diagram and Simplified r.f. Output Stage of the Quadrature Modulator



	Ideal case	Measured case
Amplitude:	– $\sqrt{I^2 + Q^2}$	– Mag(S21)
Phase:	– $\tan^{-1}(Q/I)$	– Angle(S21)

Figure 4: Mapping Function of the Quadrature Modulator

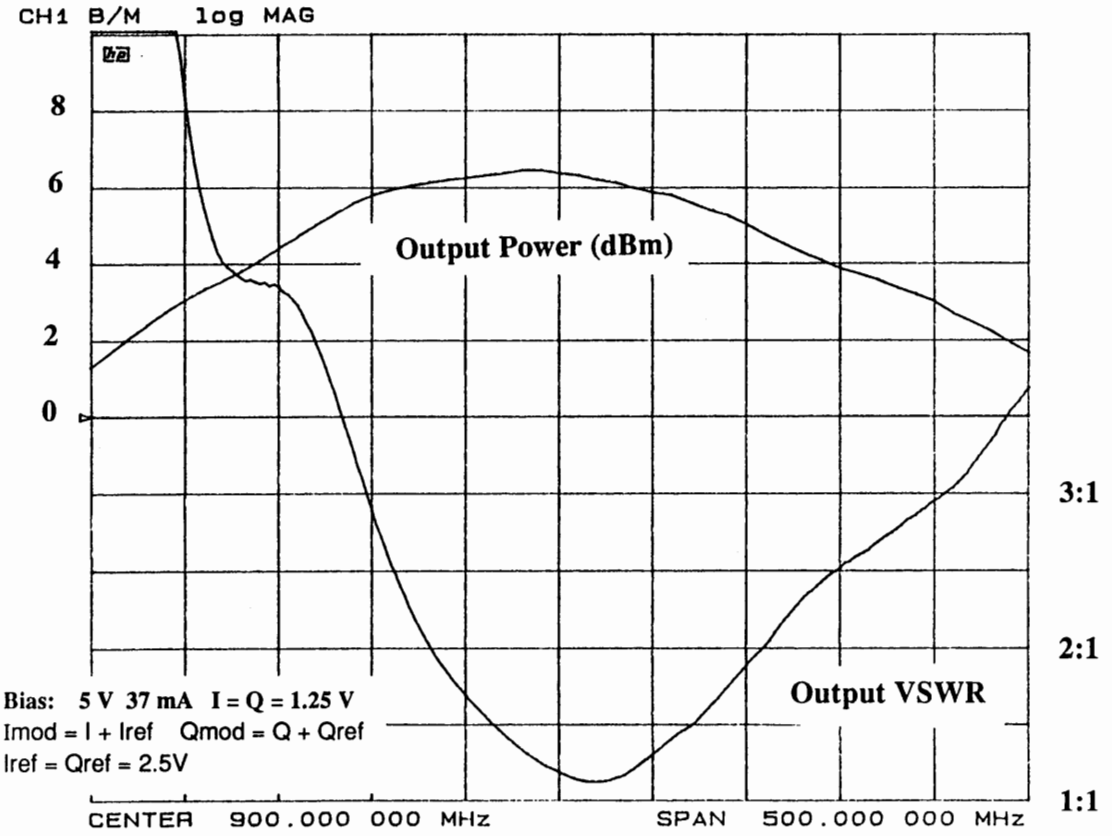


Figure 5: Output Power and Output VSWR vs Frequency

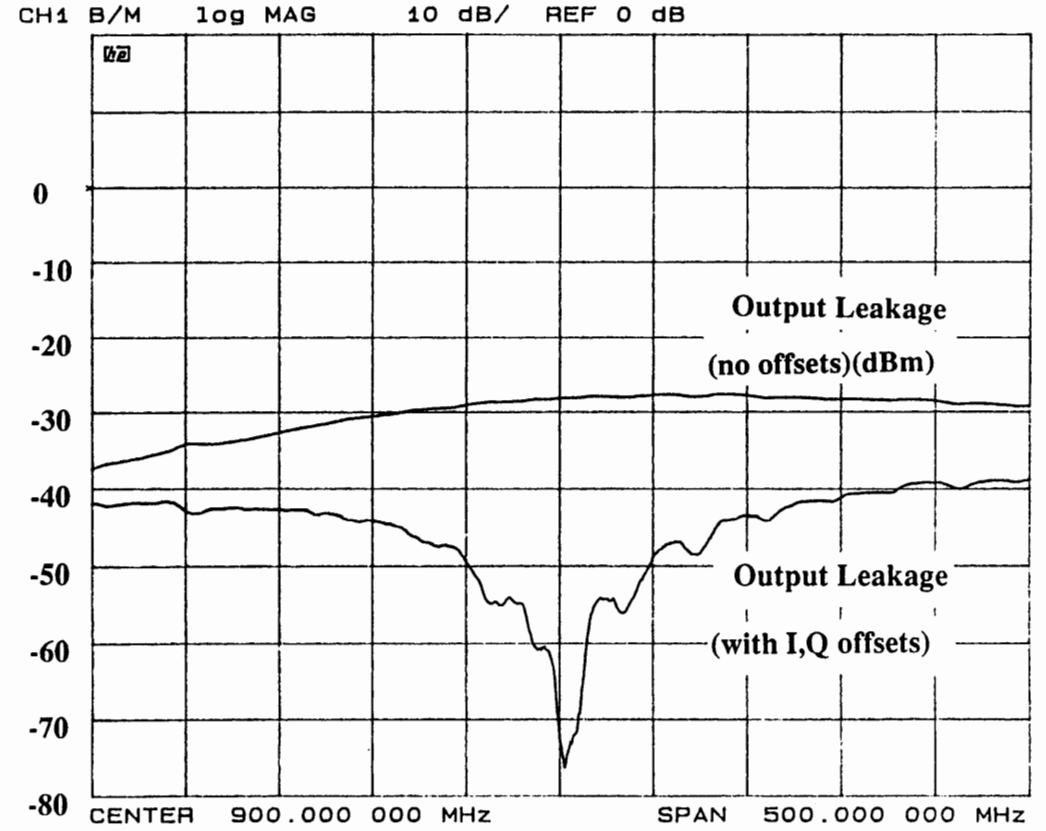


Figure 6: Output Leakage with and without Offsets

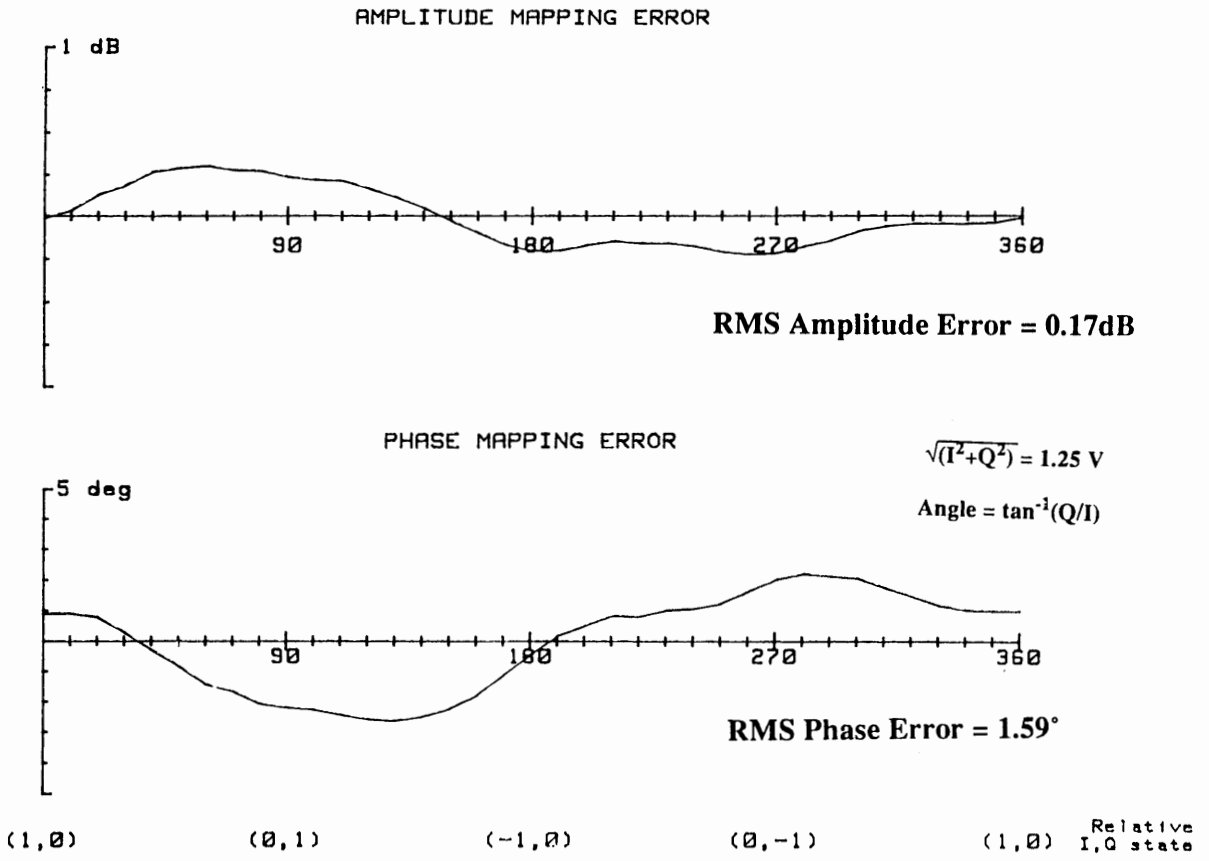


Figure 7: Amplitude and Phase Mapping Error vs IQ input angle

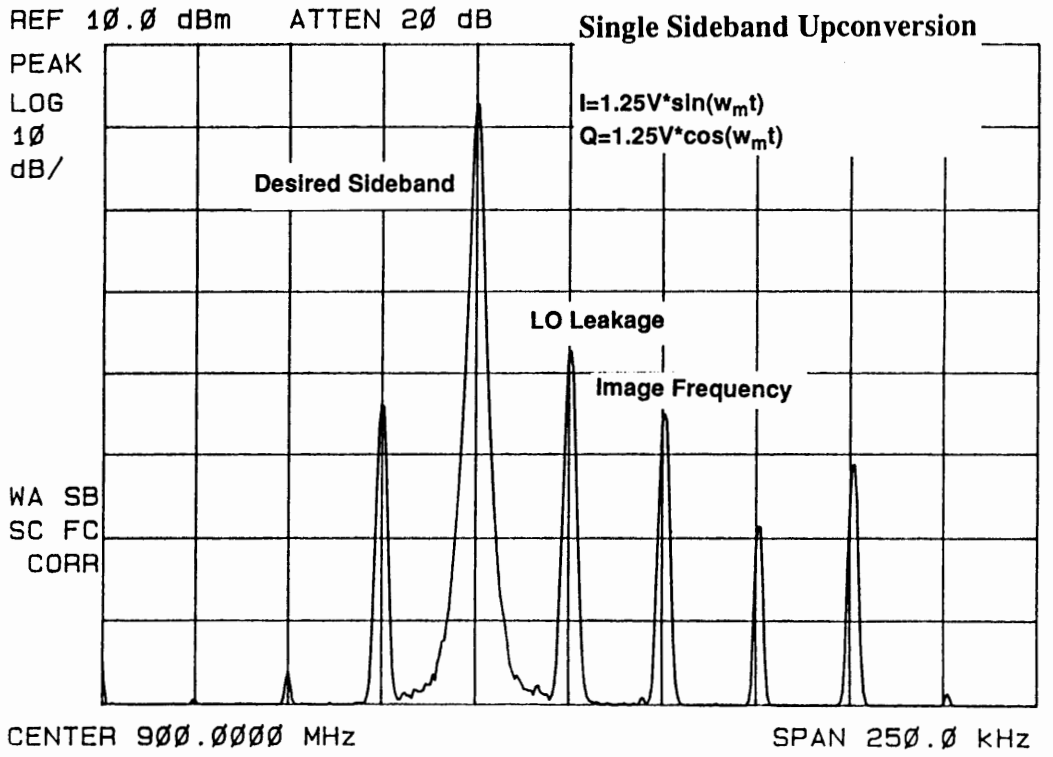


Figure 8: Single Sideband Upconversion, 25kHz quadrature inputs

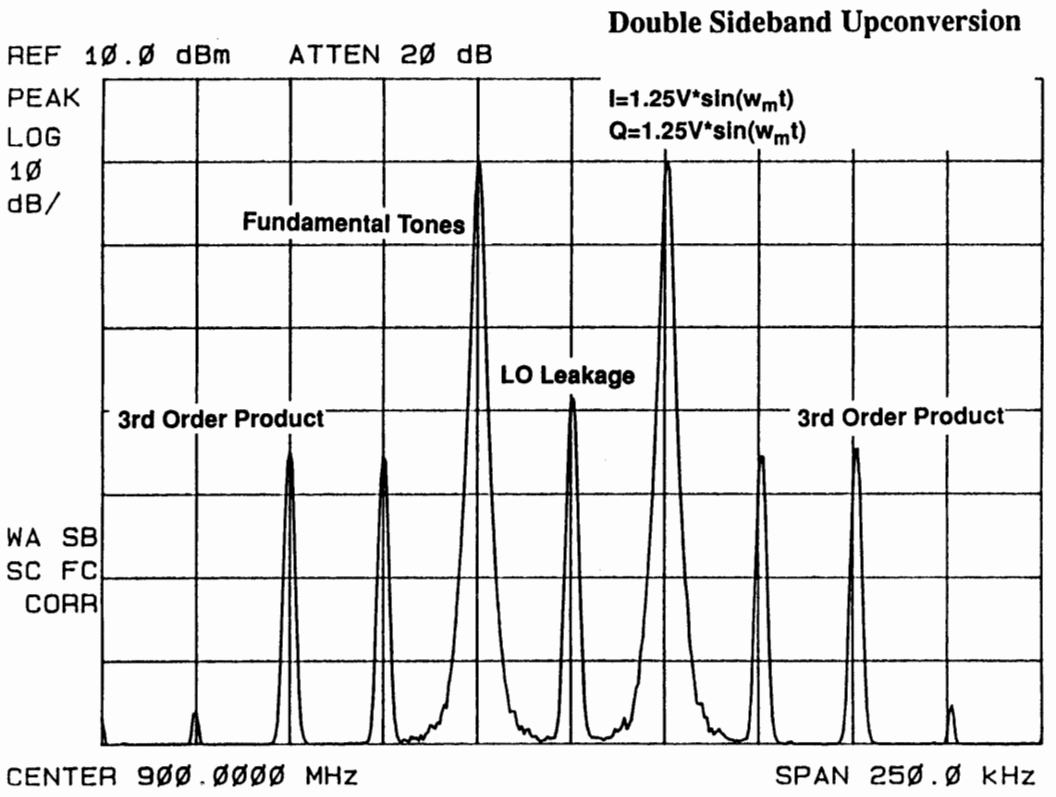


Figure 9: Double Sideband Upconversion, 25kHz in-phase inputs

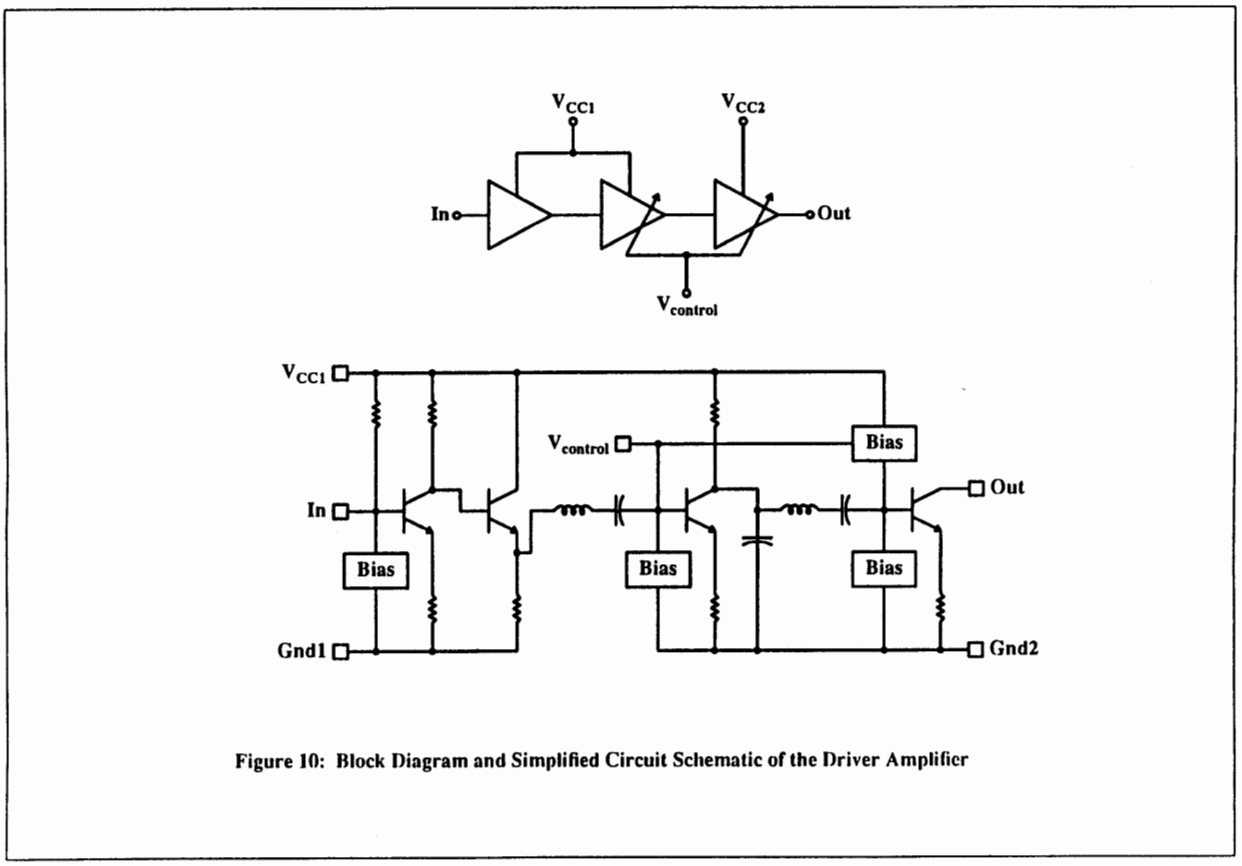


Figure 10: Block Diagram and Simplified Circuit Schematic of the Driver Amplifier

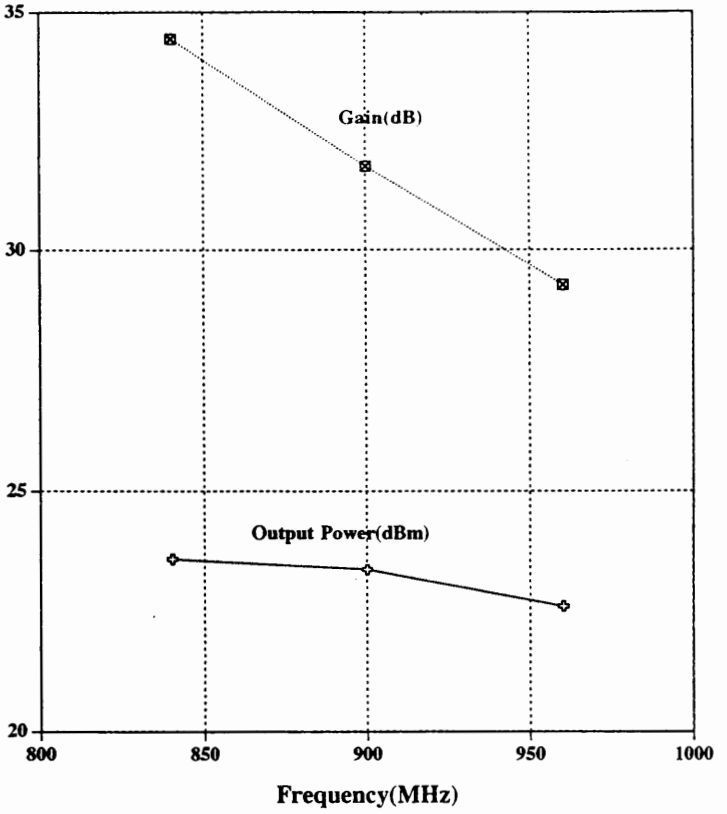


Figure 11 Output Power & Gain vs Frequency

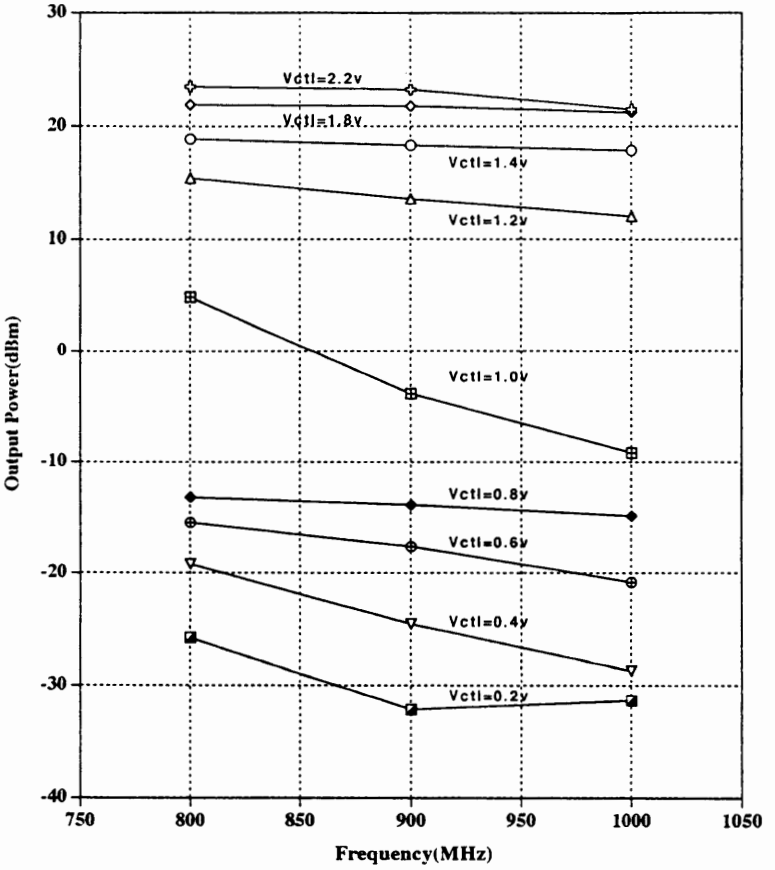


Figure 12 Output Power vs Frequency & Vcontrol

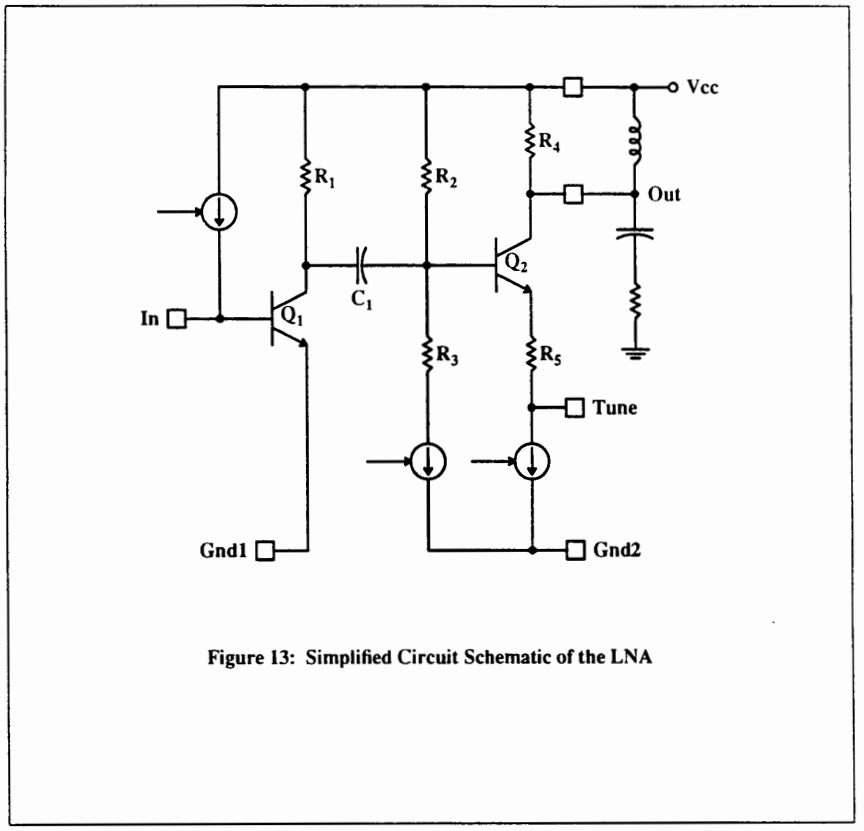


Figure 13: Simplified Circuit Schematic of the LNA

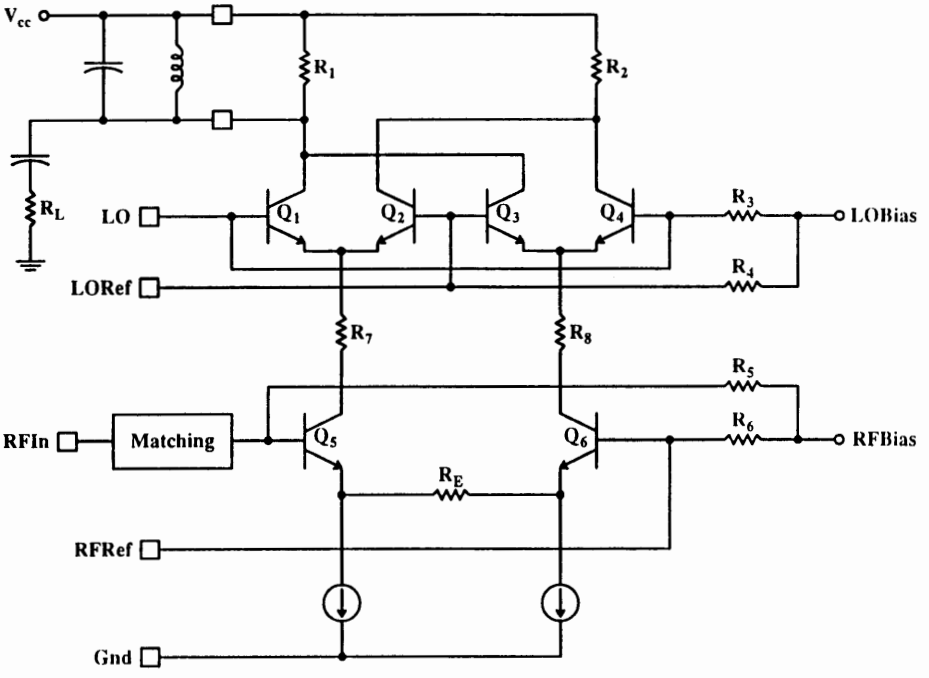


Figure 14: Simplified Schematic of the Double-Balanced Active Mixer

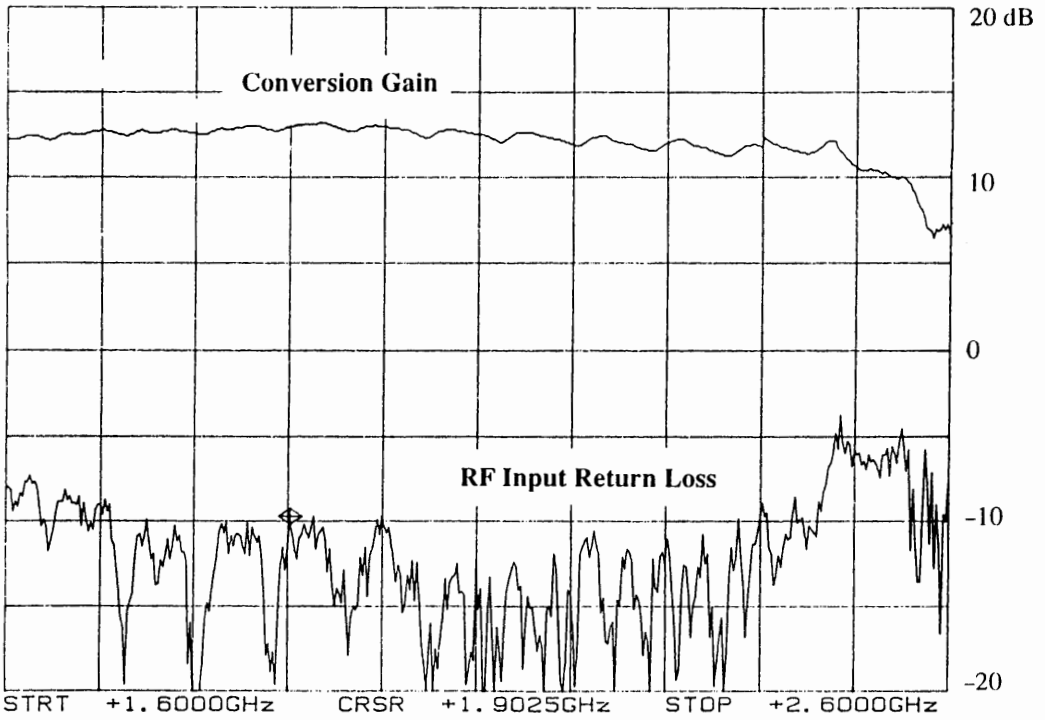


Figure 15: Conversion Gain and RF Input Return Loss vs RF Frequency

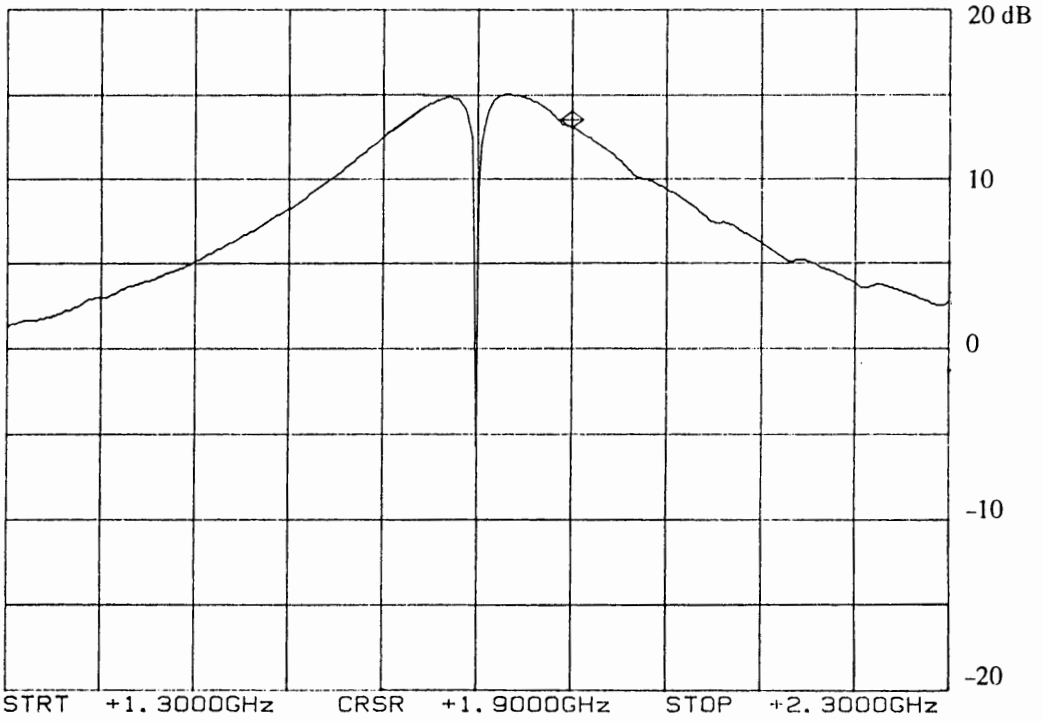


Figure 16: Conversion Gain vs RF Frequency for a fixed LO of 1800 MHz

A SILICON-BIPOLAR, MIXED-SIGNAL RFIC ARRAY FOR WIRELESS APPLICATIONS

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INTRODUCTION

Consumer markets such as the Cellular Telephone (AMPS, GSM, JDC and NADC), Global Positioning System (GPS), Cordless Telephone (DECT, CT-2 and PHP), Personal Communications Network (PCN) and Wireless LAN have passed their developmental stages and are poised for rapid expansion in the near future. All these markets require reliable, low-cost components that can be repeatably manufactured in large volumes. Early receivers and transmitters were constructed from discrete components and required significant labor costs for assembly and performance optimization. The current trend is toward lower cost, smaller size, less manual circuit tuning, lower power consumption and increased reliability through the use of Integrated Circuits which reduce component count. Several single function ICs are presently available such as low noise amplifiers, matched 50Ω gain blocks, prescalers and Gilbert cell mixers. The next step in size reduction is to incorporate these RF functions into a single, complex, multifunction, high density IC.

To address some of the varying needs of these consumer markets, Hewlett-Packard Co. has developed a mixed signal array Receiver-on-Chip (ROC) which is fabricated on a mature silicon bipolar IC process. This chip has been optimized to generate a variety of transmit/receive circuits utilizing frequency plans ranging from 800MHz to 2500MHz with supply voltages ranging from 3V to 5V. The low power consumption and small size make this an ideal technology for battery operated, hand-held applications. In today's competitive and rapidly changing market place, it is imperative that new product development cycles be minimized. Since the ROC array requires only three mask layers (metal 1, via, metal 2) for customization to a specific application, the fabrication time can be reduced from months to weeks. Furthermore, the close coupling of design and layout through parameterized standard cells greatly reduces the design time associated with complex RFICs. The chip is packaged in a low cost, industry standard 32 lead plastic quad flat pack and test costs are minimized through the use of automated test.

ISOSAT-II PROCESS

Hewlett-Packard Co.'s ISOSAT-II silicon bipolar IC process combines the advantages of proven military grade reliability with the stable, low cost manufacturability required for high volume consumer markets. Many features in the process, such as gold metallization, can meet or exceed the rigid and exacting requirements of a military Space grade qualification. Despite this high reliability level, ISOSAT-II is focused squarely on the delivery of high volume large scale integration (LSI) density ICs for consumer products.

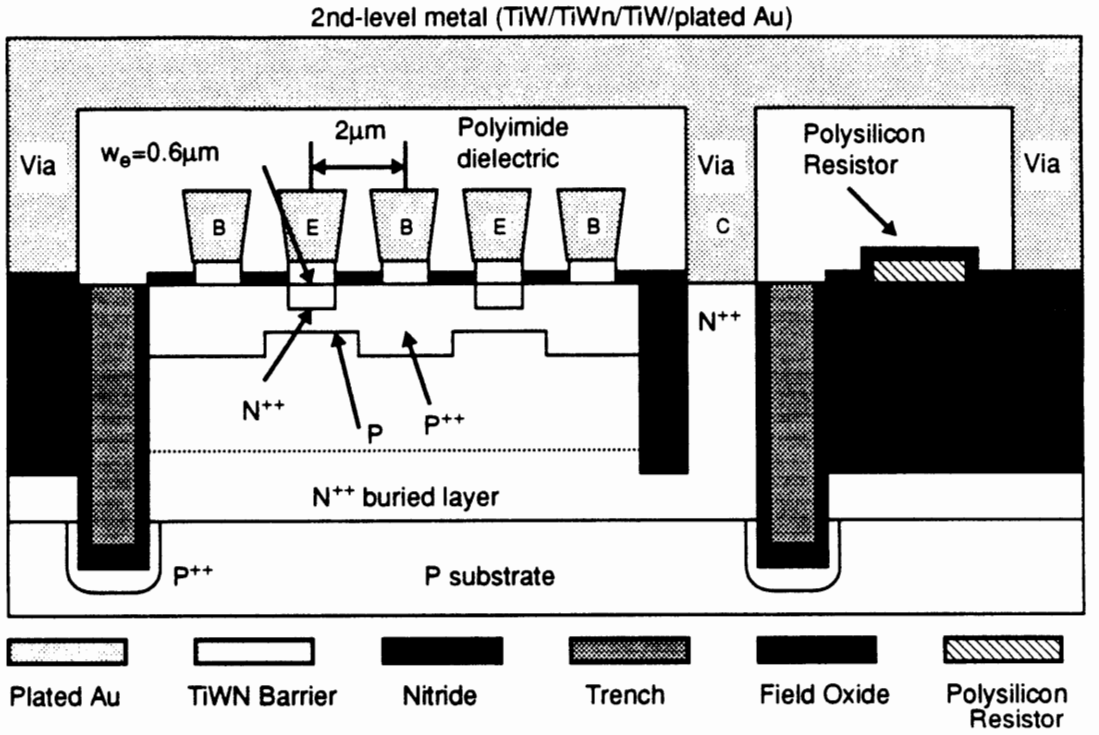


Figure 1: The ISOSAT-II silicon bipolar IC process which yields transistors with an f_t of 14GHz and an f_{max} of >20GHz

The ISOSAT-II process features an npn transistor with gold-metallized 0.6μm wide interdigitated emitters on a 2.0μm emitter to base pitch. An 8.0μm deep trench isolates the transistor from adjacent devices. These npns with f_t=14GHz and f_{max}>20GHz, can easily be scaled for low power consumption or high output power drives. Undoped polysilicon resistors are deposited on a 2.0μm thick field oxide which minimizes parasitic capacitance to the substrate for resistors and metal interconnects or bondpads. The thin-film

resistors are then implanted to produce either high or low sheet resistance values and a designer can select resistors ranging from a few Ohms to hundreds of kOhms. Two levels of metal interconnects are formed using gold metallization for low electromigration and a thick, low parasitic polyimide layer as the inter-metal dielectric. The combination of thick field oxide and low sheet resistance of gold metallization produces spiral inductors with performance comparable to those of GaAs processes up to 5GHz. A cross-section of the ISOSAT-II process is shown in Figure 1.

Other components such as Schottky diodes with f_c=100GHz, zener diodes, MIS capacitors and lateral pnp transistors allow designers additional flexibility in circuit design without adding significantly to the complexity or cost of the basic 10 mask process. Note that these diodes and the lateral pnps were not included on this mixed-signal array. The performance of passive elements in ISOSAT-II in the 800-2500MHz range is characterized by typical values of Q>10 for inductors up to 10nH and Q>25 for capacitors up to 20pF. These passive elements with high Q values and excellent repeatability allow ISOSAT-II designers to optimize circuits for significantly increased efficiencies within specific narrow bands.

Future process enhancements will include fully walled emitters and self align base contacts. The process will yield 0.4μm emitter widths with 0.8μm emitter to base pitch using conventional stepper lithography. Unlike many bipolar processes using polysilicon emitters, this process will produce completely inter-digitated devices with superior noise and power characteristics. Current development efforts are targeted toward achieving npn transistors with 30GHz f_t and 60GHz f_{max} without sacrificing the performance of passive elements or degrading the manufacturability of the current process.

ROC ARRAY

Wireless markets demand a variety of frequency plans, functionality and supply voltages. The ROC-01 mixed signal array was developed to be flexible enough to meet as many of these requirements as possible. It was originally developed for integrating receiver functions in L-band satellite systems such as GPS, GLONASS, Inmarsat and Iridium. The array can also be employed in applications such as 900MHz spread-spectrum transceivers and cellular telephones, 1900MHz European and Japanese cordless telephone systems, and 2500MHz wireless LANs. Array technology allows designers to produce chips to meet these diverse needs with relatively short development times. With the array approach, new RFIC development times are often reduced from several months to several weeks. The ROC-01 array combines high speed analog function blocks and ECL digital logic blocks to create a versatile mixed signal IC.

Cell Type	# on Chip	Max.Freq	Comments
LNA	1	2GHz	900 and 1600 MHz versions
RFAMP	1	2.5GHz	Reduces noise figure of mixers
MIXER	3	4GHz	Upconverter to 2 GHz
IFAMP	4	3GHz	Interfaces to 50-1000 Ω
VAR GAIN AMP	1	2GHz	30dB gain control range
OSCILLATOR	2	4GHz	Uses external resonator
DIG LOGIC	39	4GHz	Standard differential ECL gates
CMOS/TTL IN	4	500MHz	Can be AC-coupled
CMOS/TTL OUT	4	200MHz	Can drive 10pF at 50MHz
BANDGAP REF	5	N/A	Temp. comp. options for flat gain/current

Table 1: Major Parameterized-cells available on the ROC-01 array

The array is 1.8mm x 1.8mm (72mil x 72 mil) and has 32 bond pads. Within the body of the array are many parameterized layout cells placed in predetermined locations. Cells include mixers and amplifiers sufficient to produce three down or upconversion stages. Also included are various RF and IF amplifiers, bandgap voltage references, about 40 digital logic and buffer cells, and a negative resistance cell for creating an oscillator (see Figure 2 and Table 1).

CELL PARAMETERIZATION EXAMPLE

Parameterization of schematic and layout cells allows the designer to tailor the performance of the cell in fixed increments to trade off speed for power consumption in a digital cell or gain, linearity and noise figure versus power consumption in an analog cell. By merely changing the layout cell's parameter value, the wiring internal to the cell is automatically redrawn giving the mask designer a powerful tool for quickly creating a customized LSI layout. A corresponding parameter on the schematic cell multiplies resistors within the schematic by fixed increments to generate a new subcircuit for simulation. Figure 3 illustrates a parameterized mixer cell for the ROC-01 array in three different views. The designer usually interacts with the symbolic representation where discrete changes in the cell parameters are made by editing a list within the CAE system. These parameter changes then automatically update the schematic using the rules shown in the schematic view of Figure 3. Within the same CAE system the layout representation of the mixer cell is also automatically re-generated by the same list of parameters to ensure complete

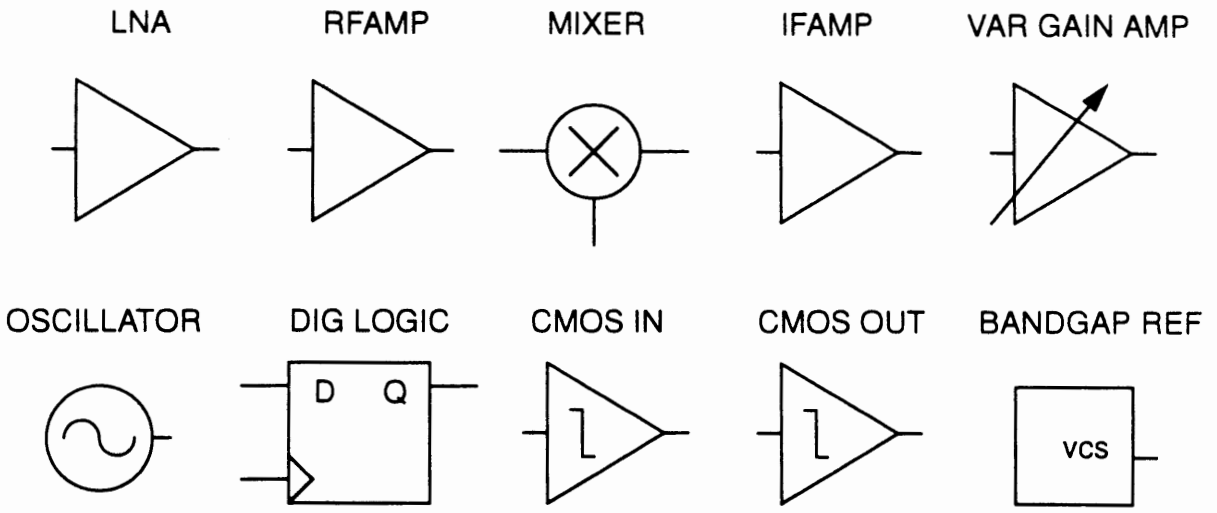
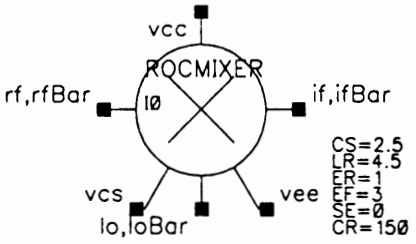


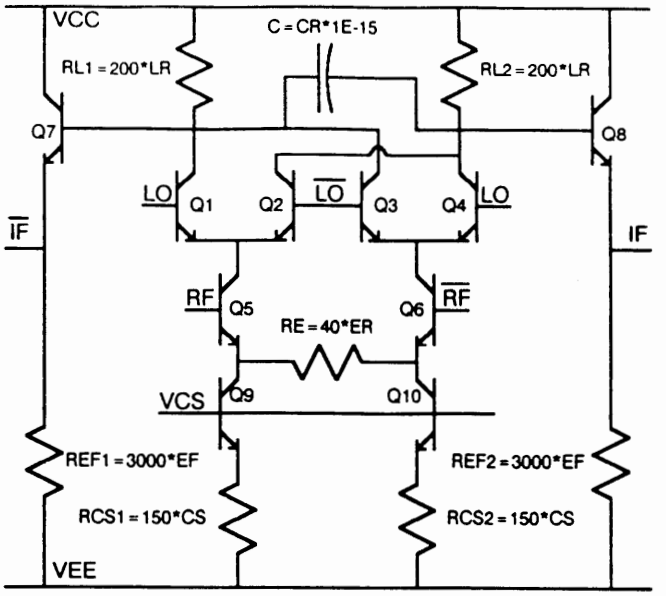
Figure 2: Cell types available on the ROC-01 Array

correspondence between design and layout. This ROC array design methodology is currently based on the Cadence Analog Artist software with significant extensions and modifications developed by Hewlett-Packard, Co. design engineers.

Table 2 summarizes a simple simulation example to illustrate the diversity of choices available within a given parameterized cell on the array. In this case the mixer cell of Figure 3 is simulated for different values of CS,LR,ER and EF with SE=1 (forces single-ended output and removes bias on unused output) and CR=0 (removes low -pass filtering capacitor completely). All simulations are performed with -10dBm of LO input power at VCC=5V and T=25°C. The RF, LO and IF ports are all resistively (wideband) matched to 50Ω. Different input/output impedances have also been used to advantage in ROC array designs. The supply current results in Table 2 include an LO buffer cell from the ROC array which is used to drive the LO quad of the Gilbert cell mixer.

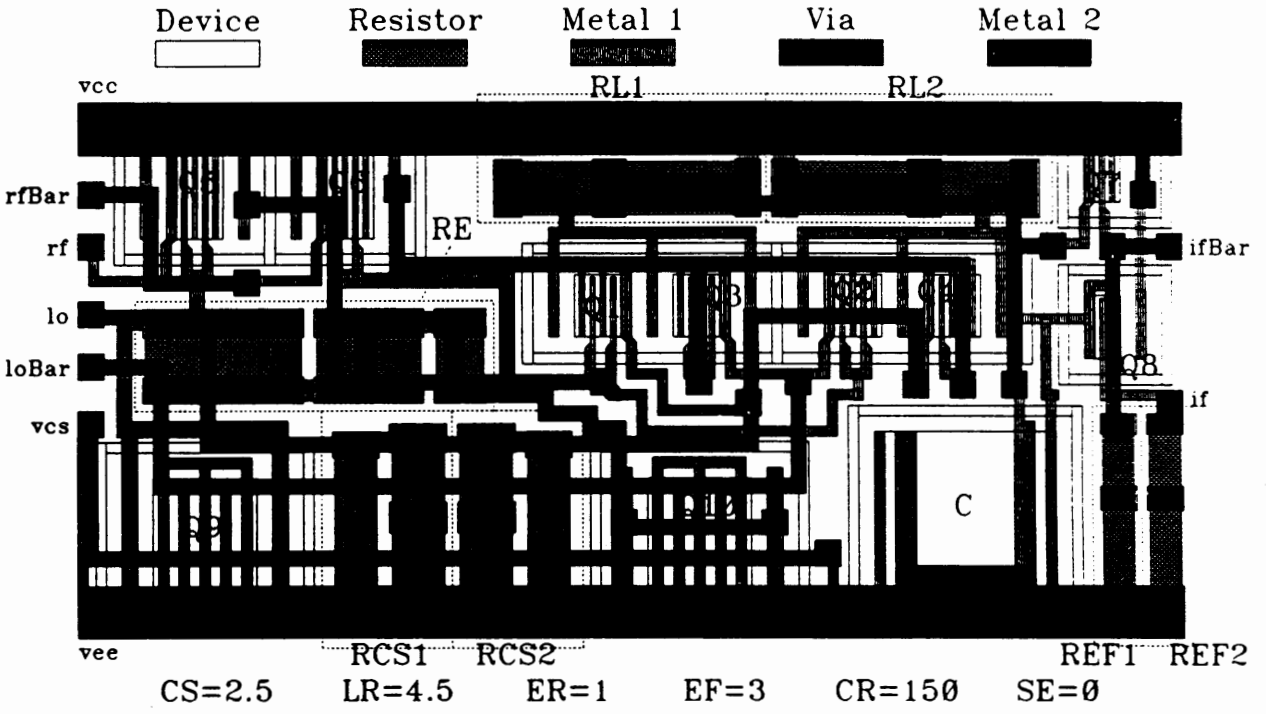
The first case in Table 2 shows the cell as might be used for a handheld satellite receiver downconverter with emphasis on low current and high conversion gain. In the second and third rows of Table 2, a more "general-purpose" downconverter arrangement is compared for operation in both the 900 and 2500 MHz spread-spectrum bands. The additional supply current for the 2500MHz case is used for more LO drive. Note that for downconverters with very low IF frequencies (especially second downconverters), the parameter CR is often set to 100-400 so that the undesired RF+LO product is low-pass filtered to significantly improve the linearity of the output stage. The final row of Table 2 illustrates an upconverter realized with the same ROC array parameterized cell. In this





(a) Symbolic Level

(b) Schematic Level



(c) Layout Level

Figure 3: Three views of a parameterized cell showing corresponding parameters of the symbol, schematic and layout views.

CS	LR	ER	EF	Icc (mA)	P1dB (dBm)	Gain (dB)	Test Conditions
4.5	6	0	1.5	2.8	-17	10.5	RF=1575MHz, LO=1400MHz
2.5	3.5	2.5	0.4	6.9	-8	3.2	RF=2450MHz, LO=2200MHz
2.5	3.5	2.5	0.4	6.4	-7	6.5	RF=900MHz, LO=1000MHz
1	1	2.5	.25	12.4	-9	-3.5	RF=100MHz, LO=1000MHz

Table 2: Parameterized cell example demonstrating the changes in the performance of a Gilbert cell mixer as parameter values are varied.

case the conversion gain is not very meaningful and in most cases, a higher impedance low frequency RF input would be preferable. The P_{1dB} of Table 2 in this case is for each of the two LO-RF and LO+RF output tones generated by the upconverter.

ROC ARRAY EXAMPLES

Several successful designs have already been implemented on the ROC array. Two design examples shown in Figures 4 and 5 will be discussed here to demonstrate the level of complexity that can be integrated onto the array.

The first application example is the RGP-03 product which has successfully been designed into production GPS receivers by Navstar, Ltd. This design incorporates two stages of downconversion and most of the components needed for a phase-locked loop onto the ROC array. (see Figure 4). The first LNA, which is the dominant component in determining the overall system noise figure, is intentionally left external to the IC to allow the end user maximum flexibility and choice. The chip operates off a nominal power supply voltage of 5V. However, through the use of temperature compensated bandgap references, the power supply can vary from 4.5V to 5.5V over a temperature range of -50°C to +100°C with little variation in overall gain (see Figure 6). An excellent correlation between measured and simulated results is also observed. Both down converters consist of an input amplifier followed by a Gilbert cell mixer with an emitter follower output. The two converters are separately optimized using the parameters discussed in the previous section to provide low noise and reasonable linearity to the first stage and high gain for minimum current in the second stage. Both converters are nominally matched at the input and output to 50Ω. The first stage provides15dB of conversion gain with a 13dB noise figure. Isolation between ports is very good with an LO to IF leakage of typically less than -50dBm. An on-chip negative-resistance cell is combined with an external varactor/resonator to generate the first LO frequency of 1280MHz. That LO signal is then

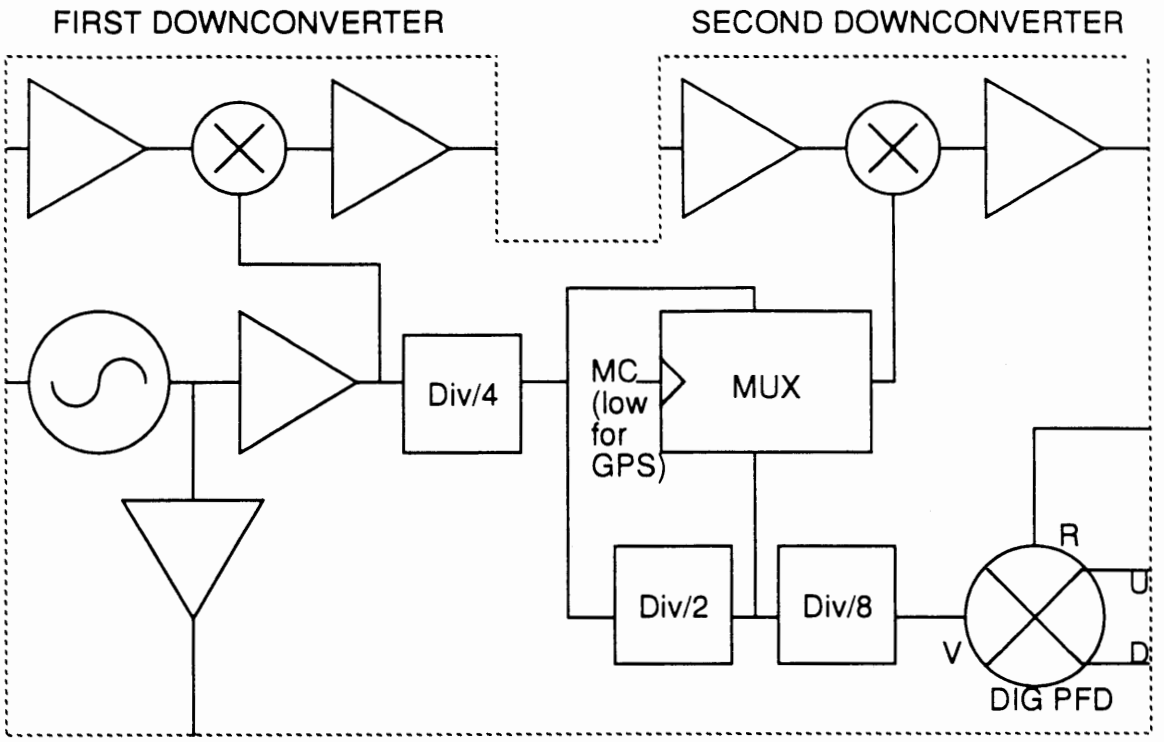


FIGURE 4: Block diagram of the RGP-03 GPS receiver IC with dual downconversion.

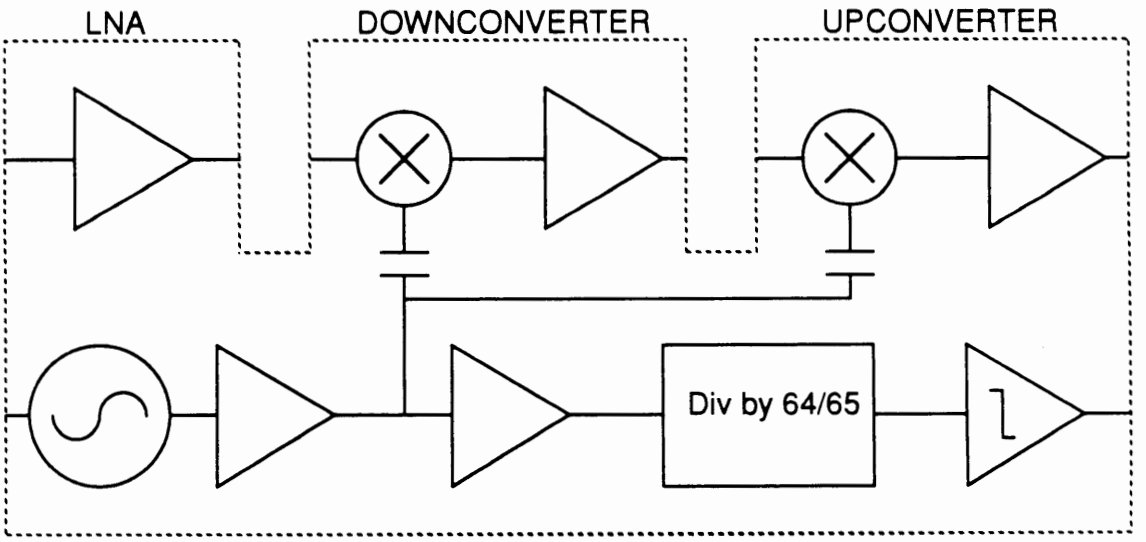


FIGURE 5: Block diagram of an R&D prototype 900MHz tranceiver IC.

divided to provide the second LO of 320MHz. The second LO is further divided to 20MHz as an input to a digital phase frequency detector which provides a differential offset voltage to an external loop filter which is proportional to the amount of phase offset (see transfer curve in Figure 7). Key characteristics of the RGP-03 are summarized in Table 3. Note also that the second LO drive can be user configured to either 1/4 or 1/8 of the first LO as shown in Figure 4. This RFIC is not narrow-band tuned and with some creativity in frequency planning, it can be used for many applications within the 800-2500MHz range.

Another design which has been successfully prototyped is a 900MHz spread spectrum tranceiver IC. The downconverter of Figure 5 used a 10nH on-chip ISOSAT-II inductor to improve the noise performance at 900MHz by 4dB for a given current draw and linearity. The upconverter had a P_{1dB} of nearly 0dBm per tone at 900MHz with broadband output matching straight into 50Ω. The input impedance of the upconverter is intentionally high to allow operation as a BPSK modulator. The divide by 64/65 prescaler provided a TTL compatible output for input frequencies up to approximately 1.6 GHz.

Parameter	Measured Value
First Stage Conversion Gain (RF to IF1)	15 dB
Second Stage Conversion Gain (IF1 to IF2)	33 dB
Noise Figure of First Downconverter	13 dB
Third-Order Intercept Point of First Downconverter	+5 dBm
VSWR (in band) of all RF and IF Ports	< 2:1
Phase Frequency Detector Output	.2 V/rad
LO Leakage at IF1 Output	-50 dBm
LO/4 Leakage at IF1 Output	-70 dBm
LO/64 Leakage at IF2 Output	-60 dBm
Supply Current at Vcc=5V	60 mA

Table 3: Measured performance of the packaged RGP-03 GPS receiver IC for RF=1575MHz, LO=1280MHz and 50Ω impedances on all RF and IF ports.

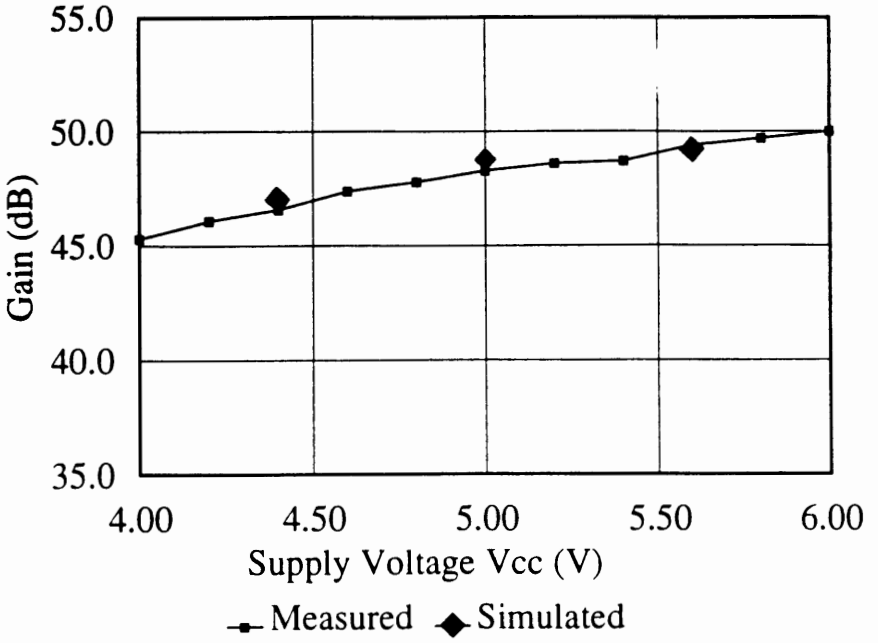


Figure 6a: Conversion gain of the RGP-03 versus supply voltage (VCC)

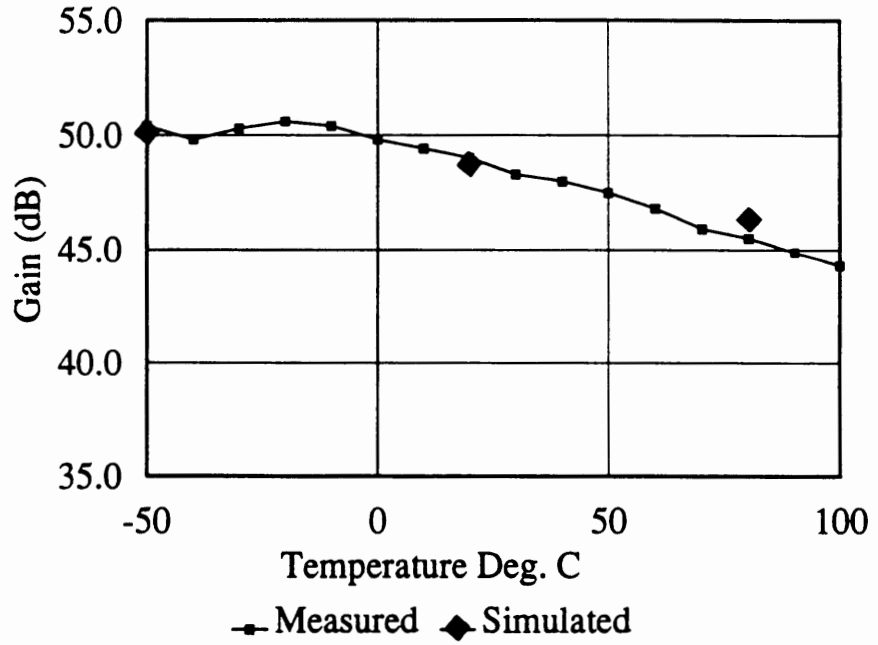


Figure 6b: Conversion gain of the RGP-03 versus temperature

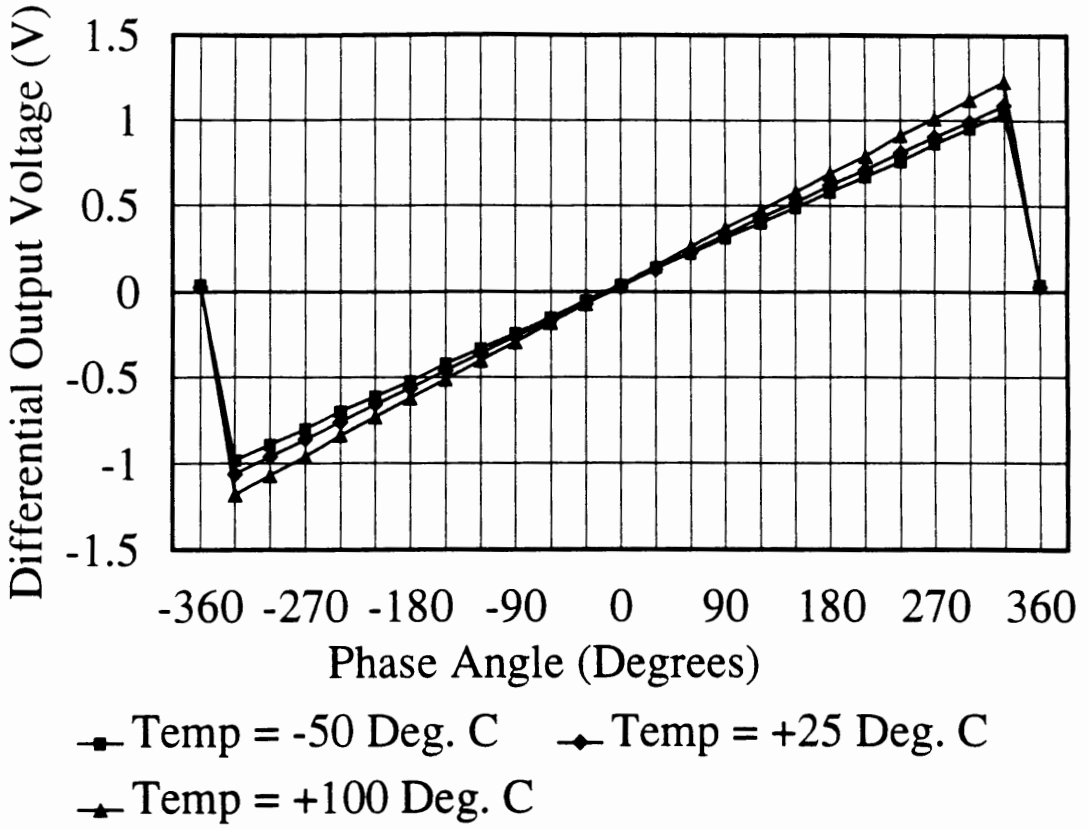


Figure 7: Transfer characteristics for the output of the phase-frequency detector on the RGP-03.

Wireless Applications for GaAs Technology

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Introduction

The applications of Gallium Arsenide to the wireless marketplace are now becoming too large to ignore. As the military markets are winding down, commercial opportunities are crying for attention. These opportunities are very different from the traditional military opportunities, with much greater cost and volume pressures, but with equivalent performance requirements. And there are hidden costs in the transition, as low volume, high skill production lines are replaced with the high volume, automated lines required for cost efficiencies.

In this paper we will discuss three different GaAs Integrated Circuits and some of their applications. The first is an IC which provides the transmitter and receiver front end for a half duplex transceiver. The second device is a power FET for a hand held cellular telephone. The third IC we will discuss is a C band low cost, low noise, low power gain block.

Half Duplex Transmitter / Receiver IC

The emergence of the 1.9 GHz PCN market has intensified the friendly rivalry between Silicon and GaAs MMIC designers. In reality, if the system is partitioned correctly there are sufficient opportunities for both technologies. Half duplex systems such as DECT, PHP, CT2 etc., can utilize a partition that plays well to the strengths of GaAs. This partition, shown in figure 1, includes the input low noise amplifier, the output power amplifier , and the SPDT switch between them, all on a GaAs MMIC.

The switching function would be difficult to realize with silicon IC technology. While 2 GHz low noise amplifiers are of course possible with silicon technology, the improved noise figure performance of GaAs provides the designer with a little more margin. And finally, at low bias voltages (3-5 volts) the efficiencies of a GaAs based power amplifier exceed that which can be obtained using silicon devices. In order to compete with silicon in price the GaAs MMIC die size will have to be minimized. As

much as possible, the large passive components should be realized off chip. To further reduce cost plastic surface mount packaging is essential.

The MMIC was fabricated using Hewlett Packard's MMICB process. The process features MESFETs with .5 um gate lengths and an Ft of approximately 25 GHz. This MESFET uses an MBE active layer with a low temperature buffer. Proton isolation is used to separate active regions. Passive components available to the designer include: silicon nitride thin film capacitors (.43 pF/sq. um), n-layer bulk resistors (340 ohms/sq.), and tantalum nitride thin film resistors (22 ohms/sq.). The process features true two level metal interconnects. The second level metal is plated to 2 um to reduce resistive loses in transmission lines and spiral inductors. While backside via holes are also available in this process, they were not used in this design in order to reduce die cost. All ground connections are made with bond wires.

The schematic of the low noise amplifier portion of the chip is shown in figure 2. The input match is realized by using the package's lead inductance. The output requires a shunt inductor and blocking capacitor to supply bias and transform the impedance to 50 ohms. A tradeoff exists between supply current and ease of match. At 2 GHz larger FETs (around 1 mm) require much simpler matching circuits due to the larger input capacitance. However, the supply current required to keep the FET in the high Gm region (40 to 50 mA) is excessive for many system requirements. Smaller FETs would require less current but would need 3 to 4 element matching circuits to transform their high input impedance to 50 ohms. Furthermore, a small device would impact the dynamic range of the system by limiting the amount of incident power. The LNA presented here represents a compromise utilizing a 500 um FET biased at 15 to 20 mA. At this bias, the LNA has a linear output power (P1dB) of greater than +10dBm, and an Output Third Order Intercept Point (IP3) greater than +20dBm. The current can be reduced for applications which do not require the high IP3 performance.

The schematic of the SPDT switch is shown in figure 3. Since this application is for a half duplex system, the receive chain is powered down when transmitting and the transmit side is powered down while receiving. The purpose of the switch therefore is to minimize the loading that the unpowered amplifier has on the other. Such a system allows the designer to tradeoff switch isolation for lower loss and higher linearity. To accomplish this the shunt stages typical to FET switches were removed. The linearity is increased because without these shunt FETs the switch can float on the RF signal. Therefore, a much larger signal level is required to override the gate bias, the principle cause of distortion. The capacitors included on chip tune out the package lead inductance.

Finally, the schematic of the power amplifier is shown in figure 4. Only the FET resides on chip and the input and output matching circuits were chosen to incorporate the package lead inductance.

Refer to the photograph of the die shown in figure 1. The LNA occupies the lower left hand corner of the chip. The SPDT switch occupies the right side of the chip. The 3 mm FET used in the power amplifier is found in the upper left hand corner. The chip size is 800 um by 900 um (31.5 mils X 35.5 mils). This device was designed for a 16 lead plastic package. Seven of the sixteen leads are connected to the die attach paddle, and thus to ground. This configuration minimizes the package's ground inductance and provides the thermal dissipation needed for the power amplifier. Packaged units were soldered to test circuit boards (figure 5) and each circuit function was tested separately. At 2 GHz the board's loss was measured at 0.5 dB. This loss is included in the measured responses that follow.

Figure 6 shows the response of the low noise amplifier. The amplifier is biased at 3 volts. The wide bandwidth allows the LNA to absorb large variations in process parameters as well as component values. Figure 7 shows the measured noise figure of the LNA. Again the response is flat from 1 to 3 GHz. And the LNA has an output one dB compression point (P1dB) of +10 dBm.

Figure 8 shows the measured response of the SPDT switch. Through Loss and Return Loss of both the on and off states are shown. An output third order intercept point (IP3) of 50 dBm was measured with -5 volts applied to the gate.

Finally, figure 9 shows the measured small signal response of the power amplifier. With a 5 volt supply the power amplifier produces an output P1dB of 26.5 dBm and a power added efficiency (PAE) of 40%. At 3 volts the output P1dB is 23.5 dBm and the PAE is 34%.

Table 1 is a summary of all the specifications for this T/R IC.

Cellular Telephone Power Amplifier Device

Modern cellular Telephony is currently undergoing a revolution. North America Europe and Japan are changing to digital transmission. Because of this transition, some new phones (NADC) must be able to move seamlessly from a digital environment to an analog environment, each of which has its own set of specifications. The current generation phones are very small, requiring great packing density of the circuitry. Because weight is an important feature, batteries must be small, and consequently the circuit must be very efficient. The phones range cannot suffer, however. This puts very

stringent requirements on that device which takes the bulk of the battery power, the power amplifier. To maximize talk time, the device must show better than 45% efficiency at 936 MHz, at 600mW in the analog mode. To minimize adjacent channel spillover, the device must exhibit a third order intercept point of 39dBm for the digital mode, all at a bias of 6V. Since this is a very high volume application, the average sale price must be very aggressive.

The device reported on here is a 10mm GaAs FET. The gate length is 0.9 micron. The epitaxial layer is grown using Hewlett Packard's proprietary vapor phase epi process, providing a very uniform structure. The transition from the semi insulating substrate to the semi conducting epi must be very sharp to support the efficiencies necessary. The device utilizes a wrap around ground, providing a very low impedance path to the bottom of the package. Table 2 contains a summary of the device performance.

Why use GaAs instead of Silicon? GaAs is generally more expensive than Silicon, at least at the current manufacturing volumes. The frequency is quite low for traditional GaAs, but Silicon has inherent limitations. Because the gain is lower, a Silicon power amplifier may require three stages (compared to two for a GaAs power amplifier with the same gain), adversely affecting the efficiency of the power amplifier. In Silicon devices the collector is at the bottom of the chip, so the output and thermal ground are the same node. This complicates the circuit board layout. GaAs FETs have both the signal and thermal grounds at the source, which is connected directly to amplifier ground. This means that a negative supply is required.

Packaging is critical to the performance and cost of this device. The package must present low thermal and electrical impedance at the common node, low losses at the signal terminals, and be inexpensive. Shown in figure 10 is an example of a low cost, high performance transistor package suitable for a multi watt power transistor. This proprietary package consists of a ceramic puck with a hole in the middle, brazed to a metal lead frame. The FET to thus die attached directly to the lead frame. This package concept can be used to build a hermetic device for high reliability applications.

The requirements for this amplifier are not trivial. The combination of linearity and efficiency is especially challenging. To achieve this performance, the device must exhibit a linear Gm Vs Vgs relationship down to about 15% of Idss. This puts severe requirements on the material, forcing the transition from the semi insulating bulk to the semiconducting channel to be tremendously sharp. Figure 11 shows an example of a device exhibiting the critical DC characteristics. At the required current, the Gm must still be close to the value at saturation.

The FET must be able to handle the power at all portions of the cycle. Saturated performance must be more than 3 dBm higher than the nominal output power. In practice, this means the saturated output power must be +31.5 dBm (in production) for a +28 dBm amplifier. A consequence of the linear operation requirements of the radio system, this is essentially an out of band emission specification.

To maximize the efficiency of a power device, one must match the output for maximum power transfer, short circuit all the even harmonics, and open circuit the odd harmonics. Unfortunately, this scheme causes the harmonics to mix with the fundamental, causing excessive intermodulation. For high linearity, the wave form must be as close to a sine wave as possible. This means that the harmonics must be power matched as well, so that the energy is not available to mix with the fundamental. Due to the out of band emission requirements, these harmonics cannot be present at the antenna. A diplexer can be used to terminate the harmonics separately. This results in a rather less than optimally efficient amplifier (65% PAE is a typical specification for analog systems), but the compromise is necessary to achieve the required linearity. Figure 12 shows the circuit schematic. Figure 13 is a photograph of the device. Figure 14 illustrates the two tone response of one of these FETs.

C Band Low Cost, Low Power LNA

There are numerous commercial bands from 1.5 to 8 GHz, some mature, many emerging. These bands include 1.5 GHz (GPS), 1.9 GHz (PCN), 2.1 GHz (MMDS), 2.4 GHz & 5.7 GHz (ISM), 3.7 to 4.2 GHz (Satellite/TVRO), C-Band (Aviation), and the full 1.5 to 8 GHz band (Instrumentation). A MMIC LNA has been designed to help those system designers involved at these frequencies. It includes integrated bias and impedance matching, eliminating most of the 10 to 15 components required to implement a comparable discrete design. A low cost surface mount package is utilized to maintain performance without significant degradation. This MMIC is a functional marriage of military technology (PHEMT) and a commercial application (low manufacturing cost / high yield).

This MMIC uses state-of-the-art 0.15u gate PHEMT devices, self-biasing current sources, source follower interstage, resistive feedback, and on-chip matching to make a unique low noise amplifier. The die area is small (0.40 mm sq.) and is compatible with surface mount packages. DC power requirements are low, consuming only 15mA from a single +7V supply.

This monolithic low noise MMIC amplifier employs Hewlett-Packard's advanced PHEMT (Pseudomorphic High Electron Mobility Transistor) process, which yields 0.25 dB noise figure at 4.0 GHz. The devices are built using MBE (Molecular Beam Epitaxy) material growth techniques. The gates are defined using electron-beam lithography. Typical lengths range from 0.12 to 0.17 microns. A mushroom shaped gate is used in order to reduce gate parasitic resistance by increasing the gate's cross sectional area.

Figure 15 presents a schematic of the PHEMT MMIC LNA, and a photograph of the device assembled into a surface mount package. The MMIC LNA consists of two primary FET gain stages, one source follower stage, three current sources, two feedback networks, and two source capacitors. Each 12 dB gain stage consists of a PHEMT FET biased at 25% of Idss with the use of a current source. The source follower also consists of FET at 25% of Idss bias with a current source. The use of active current sources on each stage allows for a robust design tolerant of natural variation in the fabrication process. The source follower provides impedance transformation for an internal feedback point. This interstage-to-input resistive feedback is used to improve stability and VSWR, with minimum degradation of the noise figure. A second capacitor and resistor network provide feedback on the last stage to improve the output match, stability, and gain flatness. Source capacitors allow for a single DC supply, and provide high pass filtering. The die size is small, approximately 0.59 mm (23 mils) by 0.68mm (27 mils).

Figure 16 illustrates typical performance, derived from more than 200 parts. In a 50Ω system, typical gain is 21 dB, noise figure is 1.9 dB, input VSWR is 3.0:1, output VSWR is 2.0:1, and output power at one dB compression is greater than 7 dBm. A simple external input match (series inductance of .1 to 2 nH) produces the minimum noise figure of 1.5dB, gain greater than 22 dB, and VSWR below 1.5:1. If output power is not critical, a 5 volt supply can be used with minimum degradation of the other specifications. As all stages share current, the MMIC consumes typically only 15mA, 1/3 less than any published, comparable devices. Table 3 shows measured performance for this MMIC. This MMIC LNA compares favorably in noise figure, gain, low current, match, wide bandwidth, and price with any advertised or published products presently available.

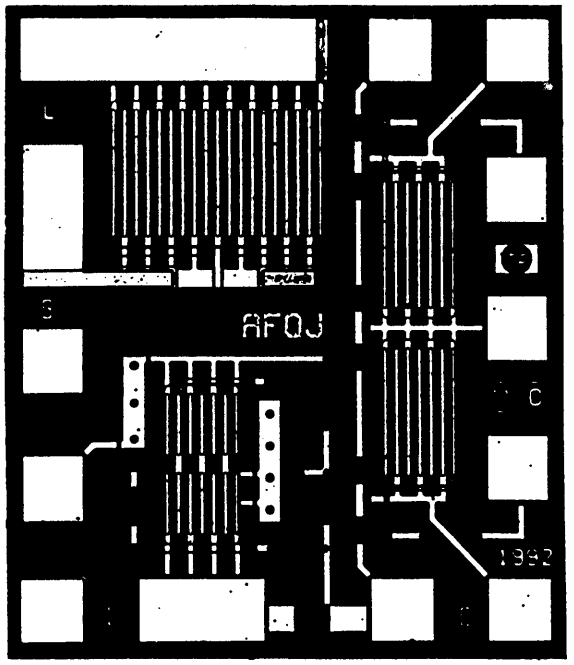


Figure 1: T/R Chip Photograph

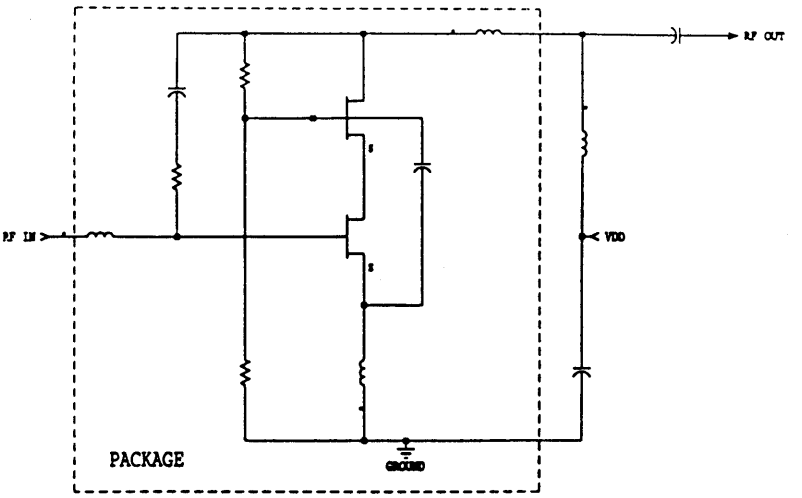


Figure 2: Low Noise Amplifier Section

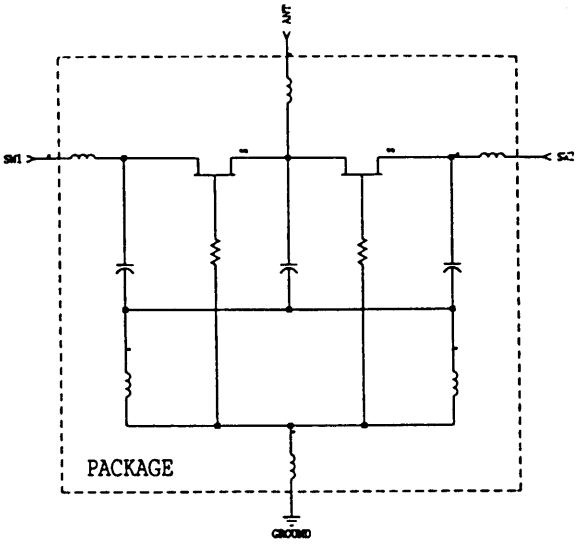


Figure 3: Switch Section

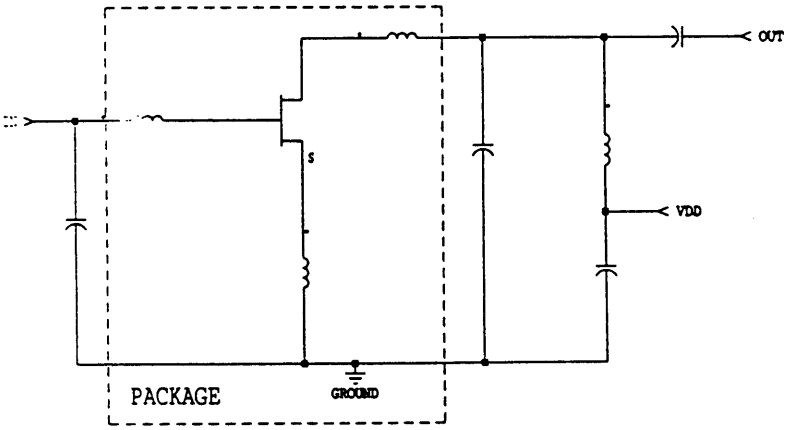


Figure 4: Power Amplifier with Off Chip Matching

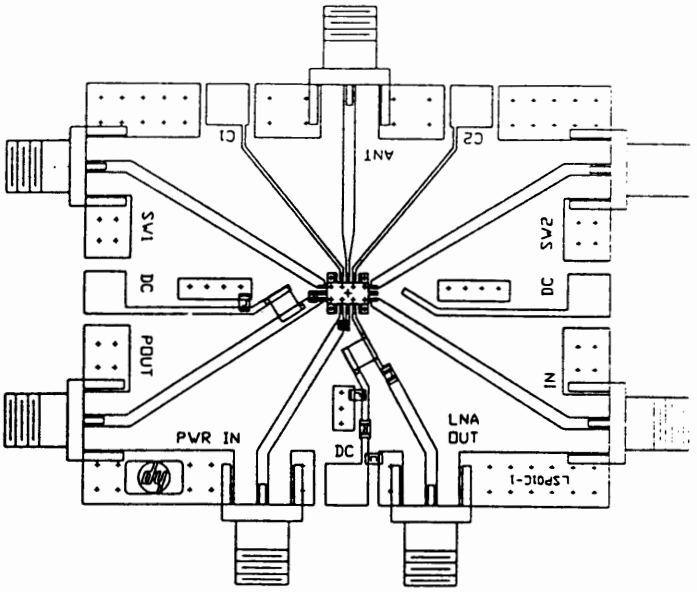


Figure 5: Test Board

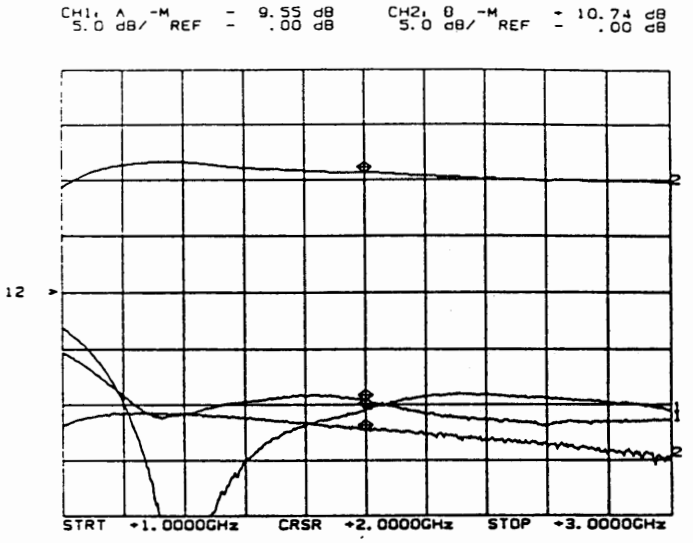


Figure 6: Gain, Isolation, and Return Loss of LNA

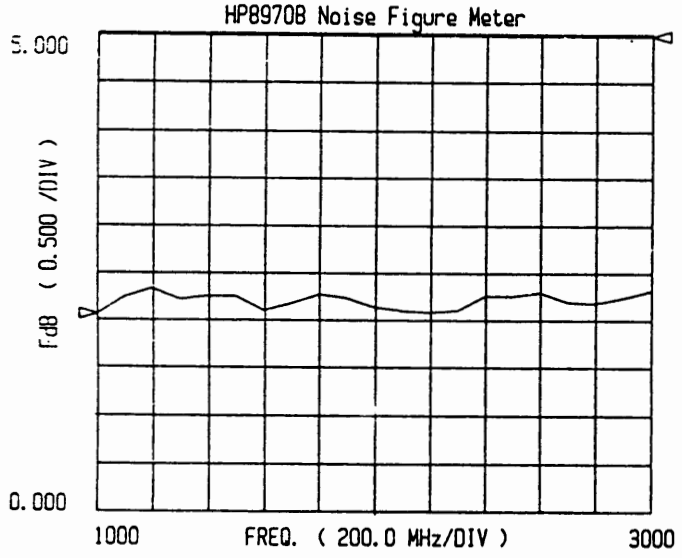


Figure 7: Noise Figure of LNA

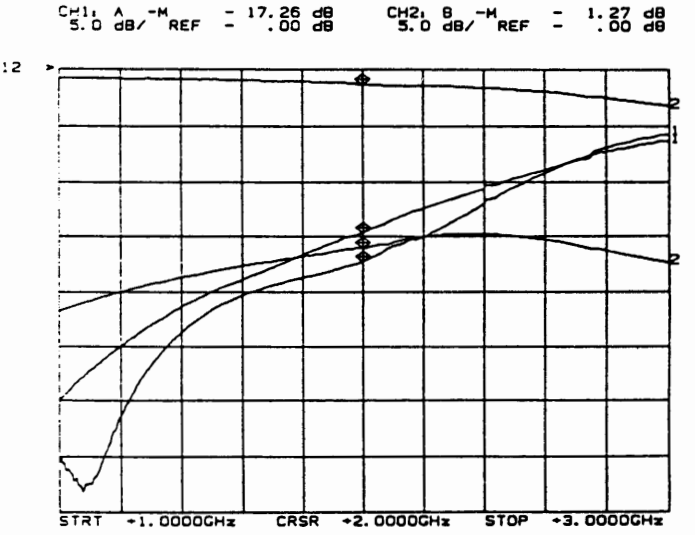


Figure 8: Gain, Isolation, and Return Loss of Switch

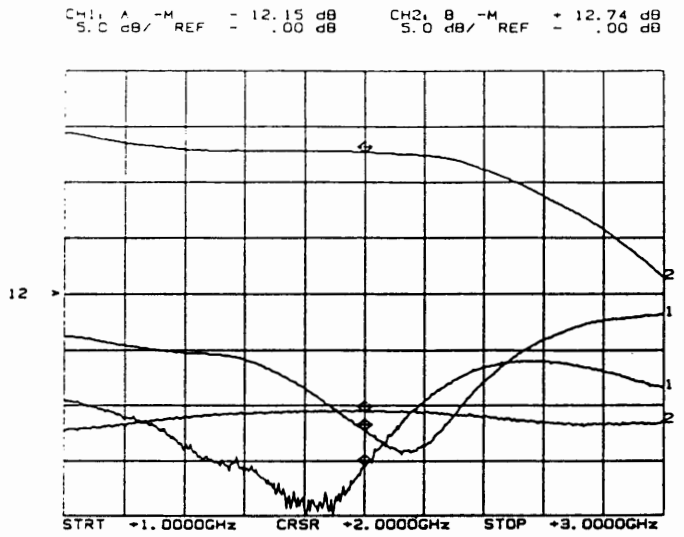


Figure 9: Small Signal Response of Power Amplifier

Table 1 Half Duplex T/R IC

	Parameter	Specification
	Frequency	1 to 2 GHz
LNA	Noise Figure	2.0dB
	Gain	12dB
	Return Loss	14dB
	P1dB	10dBm
	Power Supply	5V/20mA
Switch	Insertion Loss	1.3dB
	Return Loss	15dB
	Isolation	18dB
	IP3	50dBm
	Power Supply	-5V
PA	Gain	13dB
	P1dB	26dBm
	PAE	40%

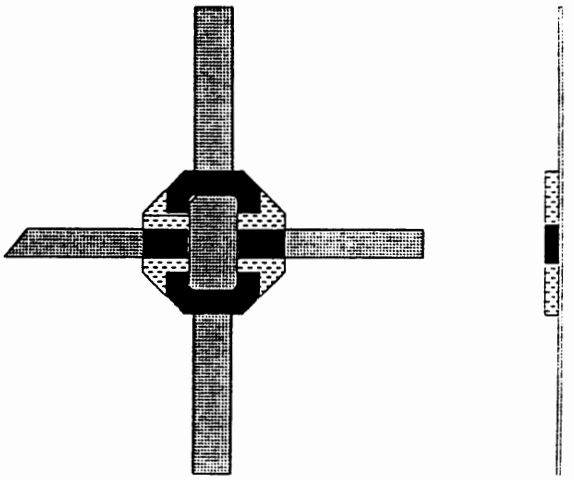


Figure 10: Cellular Power FET Package

Table 2 Cellular Telephone Power FET

Parameter	Specification
Frequency	830 to 842 MHz
Gain	14dB
Analog PAE	45%
Pout	+28dBm
IMD 3	-26dBc
IMD 5	-36dBc
IMD 7	-40dBc
Power Supply	6V

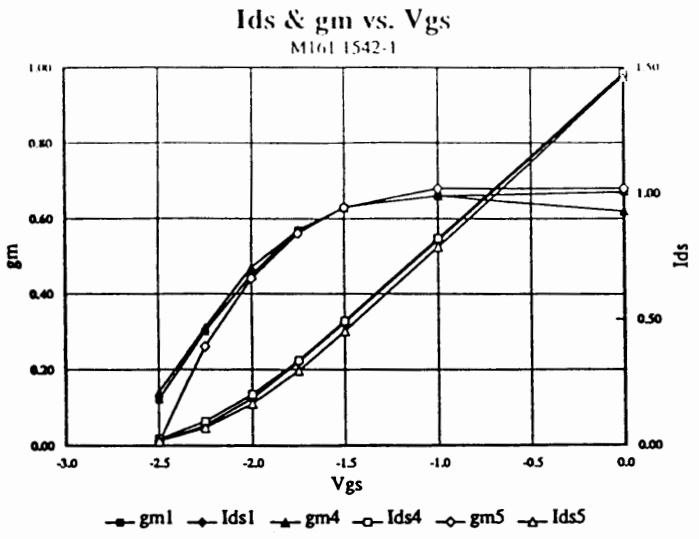


Figure 11: Gm & Ids vs Vgs for Cellular Power FET

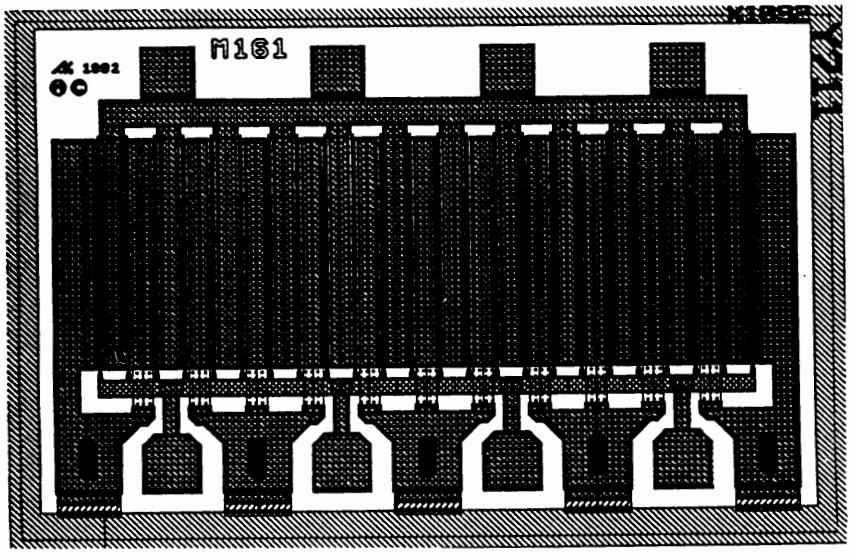


Figure 13: Cellular Power FET

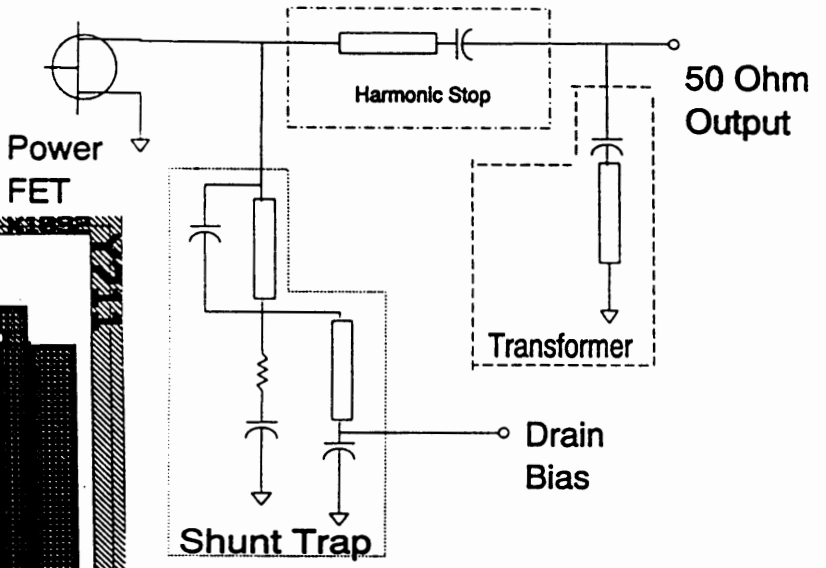


Figure 12: Diplexed Output Circuit

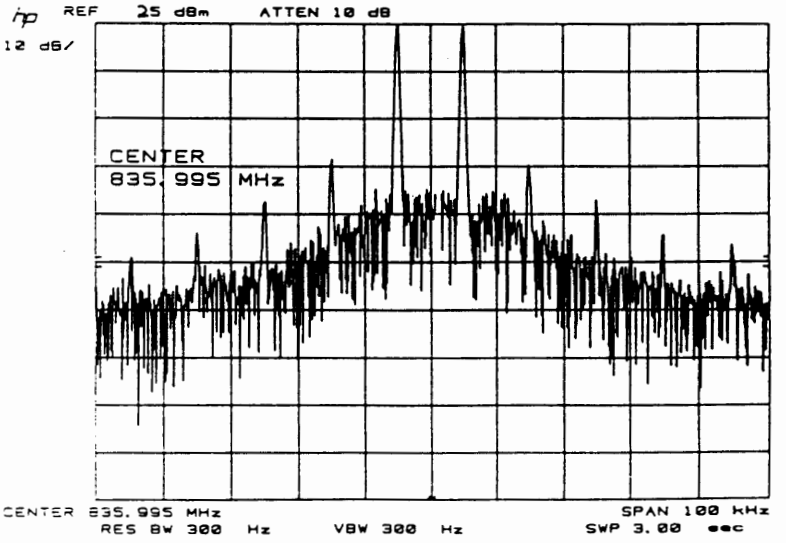
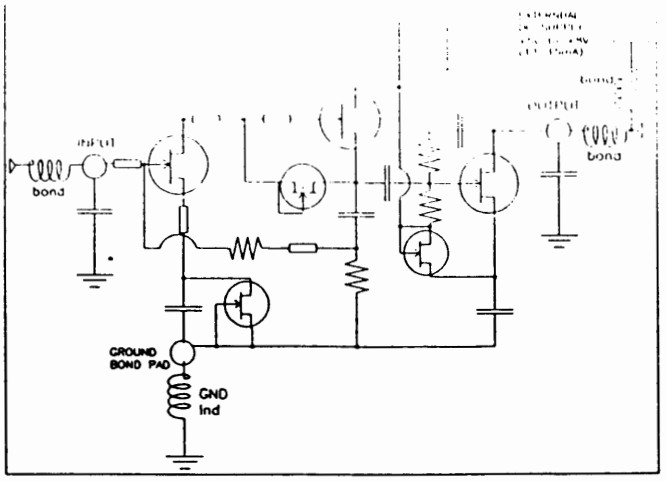
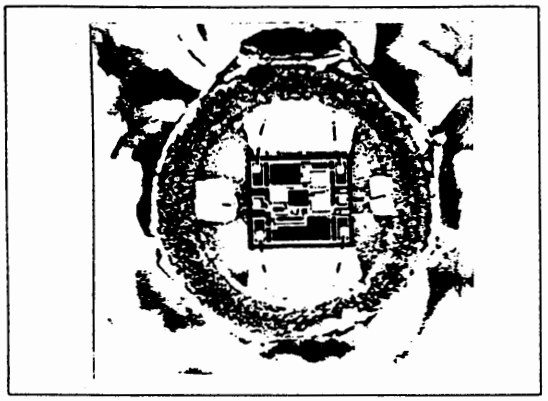


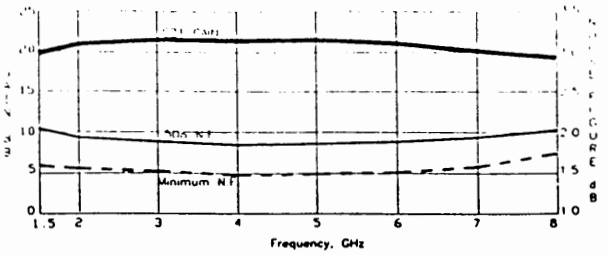
Figure 14: Intermod Performance of Cellular Power FET



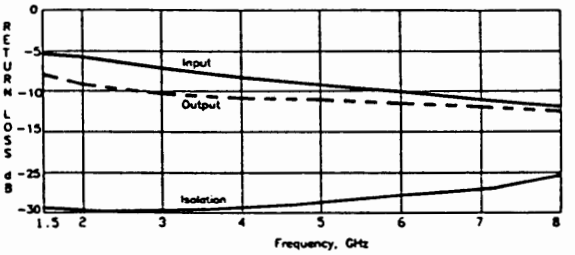
The Hewlett-Packard PHEMT MMIC 3 stage LNA schematic.



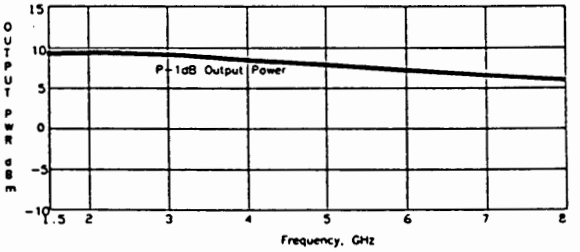
The MMIC LNA Chip in a standard 70 mil surface mount package.



Measured gain and noise figure of the MMIC LNA. Minimum noise figure is obtained for narrow bands with the addition of a .1-2 nH input series inductance.



Measured typical input return loss, output return loss, and isolation of the MMIC LNA. All data measured in a 50 Ohm system. An input match (series inductance) typically improves the input return loss by 10 dB.



Measured typical power output of the MMIC LNA at one dB compression. Vds is +7.0 V for power measurements.

Figure 15: PHEMT MMIC LNA

Figure 16: PHEMT LNA Performance

Electrical Specifications, Ta=25 C

Symbol	Parameters and Test Conditions: Vd=7.0V, Zo=50		Units	Min.	Typ.	Max.
Gp	Power Gain (|S21|^2)	f=1.5 GHz	dB	20.0	19.0	
		f=4.0 GHz	dB		22.0	
		f=6.0 GHz	dB		18.0	
		f=8.0 GHz	dB		15.0	
NF	50 Ohm Noise Figure	f=1.5 GHz	dB		2.1	2.1
		f=4.0 GHz	dB		1.9	
		f=6.0 GHz	dB		2.0	
		f=8.0 GHz	dB		2.1	
P1dB	Output Power @1dB Gain Comp.	f=4.0 GHz	dBm		8.0	
IL	Input Return Loss	f=1.5 GHz	dB		-5.0	-5.0
		f=4.0 GHz	dB		-7.5	
		f=6.0 GHz	dB		-10	
		f=8.0 GHz	dB		-10	
OL	Output Return Loss	f=1.5 GHz	dB		-7.0	-9.5
		f=4.0 GHz	dB		-12	
		f=6.0 GHz	dB		-16	
		f=8.0 GHz	dB		-20	
Id	Device Current		mA		15.0	20.0

Table 3: LNA MMIC

LOW COST, HIGH PERFORMANCE RECEIVER FOR WIRELESS APPLICATIONS

By Brian M. Kirk
Applications Engineer: California Eastern Labs

Introduction: With the increase in commercial applications of microwave and radio frequency (RF) equipment, designers have placed a greater demand on consistent performance and low price. The receiver front end described in this paper utilizes low-cost, off-the-shelf technology from NEC/California Eastern Labs to produce a circuit which can be used in many commercial designs.

The starting point for this circuit was the uPC2721GR MMIC down converter. This device includes a mixer with an internal local oscillator (LO) and an intermediate frequency (IF) buffer amplifier on a single MMIC chip. The internal LO is tuned using an external varactor diode. The uPC2721GR also allows the option of using an external oscillator.

In order to achieve an improved noise figure for the circuit, a low noise amplifier (LNA) was added at the RF input to the down converter. The LNA was designed using a discrete low noise GaAs MESFET (NE76038) with a matching structure made using discrete components. The NE76038 is fabricated using ion implantation techniques to improve RF and DC performance, and features a recessed 0.3 micron gate and triple epitaxial technology. Typical noise figures of 1.8 dB can be obtained at 12 GHz, with 7.5 dB associated gain, even in the low cost plastic "38" package. The device is also available in ceramic packages and in chip form.

A low-pass filter was placed after the down-converter to reduce the LO and RF power at the output, and an MMIC buffer amplifier (uPC2710T) was included at the end of the chain to increase the overall system gain. The uPC2710T features 33 dB typical gain up to 1500 MHz in an inexpensive six-pin minimold plastic package. A block diagram of the entire system is shown in Figure 1.

Both the MMIC parts used in this design are manufactured using the NESAT III MMIC process developed by NEC. The process features include:

* a low-energy, boron-ion base implant which reduces base transit times
* a 0.6-um emitter line width which results in low base resistance and low parasitic capacitances.
* an arsenic ion-implanted buried layer and thin epitaxial layer to reduce collector resistance.
* arsenic ion-implanted poly-silicon resistors on a thick SiO_2 layer to reduce parasitic capacitances of the on-chip resistors.
* PtSi/Ti/Pt/Au metalization and reactive ion etching to permit reliable production of 1-um electrode lines and gaps.
* a silicon nitride passivation layer for scratch and contamination protection.

These process features result in reliable and reproducible silicon MMIC's with cutoff frequencies (f_T) approaching 20 GHz.

Target Specifications: The design goal for this circuit was to produce a low-noise, high-gain receiver front-end. Operating frequency was to be 1800 MHz at the RF input, with a 1700 MHz LO resulting in a 100 MHz IF at the output. A further design goal was that the active parts used should be low cost: less than $10 (based on 10K piece quantities). The design specs were as follows:

Parameter	LN Amp*	Mixer	Filter	IF Amp*	Overall
Gain (dB)	14	20	-6	32	60
Noise Fig (dB)	1	11	6	3.5	2.5
Sat Power (dBm)	2	5	-	13	13
Inp Ret Loss (dB)	10	-	15	6	10
Out Ret Loss (dB)	8	-	15	12	12
Cost ($ @ 10K pc)**	$2.10	$2.00	-	$1.70	$5.70

* LNA specs at 1800 MHz, IF Amp specs at 100 MHz
** Cost of active parts only

Design Approach: Since the MMIC portions of this circuit are fixed in their performance, the design focused on the low noise amplifier. The NE76038 GaAs FET was chosen for its low noise figure, high reliability and low cost. The device was modeled using CAD (Touchstone) and the matching structure was optimized for a 100 MHz bandwidth centered at 1800 MHz. Discrete tuning elements were used with the goal of minimizing noise figure, while maintaining reasonable gain and return loss. The predicted circuit performance was 1.02 dB noise figure with 15.7 dB gain at 1800 MHz. Input and output return loss were predicted to be -9.9 dB and -8.3 dB respectively.

A test circuit for the low noise amplifier was assembled and tested separately from the other components of the receiver. This was done so that the tuning elements could be optimized for minimum noise figure. The test circuit layout with the initial and final values of the tuning elements is shown in Figure 2. 1800 MHz test results obtained from the final circuit were:

Small Signal Gain:15.2 dB Noise Figure: 0.6 dB
Input Return Loss: 5.2 dB Output Return Loss: 3.5 dB

The next stage of the design was to test the low noise amplifier breadboard with the other components of the system. To accomplish this, separate test fixtures were built for each of the components in the chain. Test results on circuits for the downconverter and the IF buffer amplifier were:

Down-Converter: uPC2721GR
RF=1800 MHz, LO=1700 MHz
IF= 100 MHz
Conversion Gain: 19.5 dB

IF Amp: uPC2710T
Small Signal Gain: 33.5 dB
Input Return Loss: 9.8 dB
Output Return Loss: 14.0 dB

The low pass filter test circuit was adjusted to reduce the LO and RF power level at the output to 10 dB below the IF signal level. At this time it became apparent that even though the filter had been designed to be somewhat lossy, the oscillator power being reflected back into the mixer of the uPC2721GR was causing an unacceptable level of spurious signals. A 3 dB pad was inserted between the filter and the mixer of the uPC2721GR, and this minimized the spur problem. The small signal gain of this line-up was 59.8 dB - close enough to the design goal to go to a final layout.

Final Layout: The final circuit layout is shown in Figure 3. The pad between the mixer and the filter was increased to 6 dB in the final design to further improve the spur performance at the output. The circuit was etched on Duroid 5880 substrate. Outside dimensions are 1.8 by 1.25 inches. The gain and noise figure performance of the final circuit versus input frequency are shown in Figure 4. In addition, the following data was taken:

Input Return Loss (1800 MHz): 6.0 dB
Output Return Loss (100 MHz): 14.2 dB
Power (1 dB compressed gain): 11.2 dBm

Conclusion: The drive to reduce costs for commercial RF and microwave products does not mean that performance must be sacrificed. Low-cost, off-the-shelf discrete and MMIC parts from NEC/California Eastern Labs can be used to provide reliable circuits which deliver top shelf performance for commercial applications.

Acknowledgements: Many thanks to Huy Tran for his efforts in the fabrication, assembly, tuning and testing of the circuits described in this article.

For further information please contact Brian M. Kirk, Applications Engineer at California Eastern Labs, (408) 988-3500.

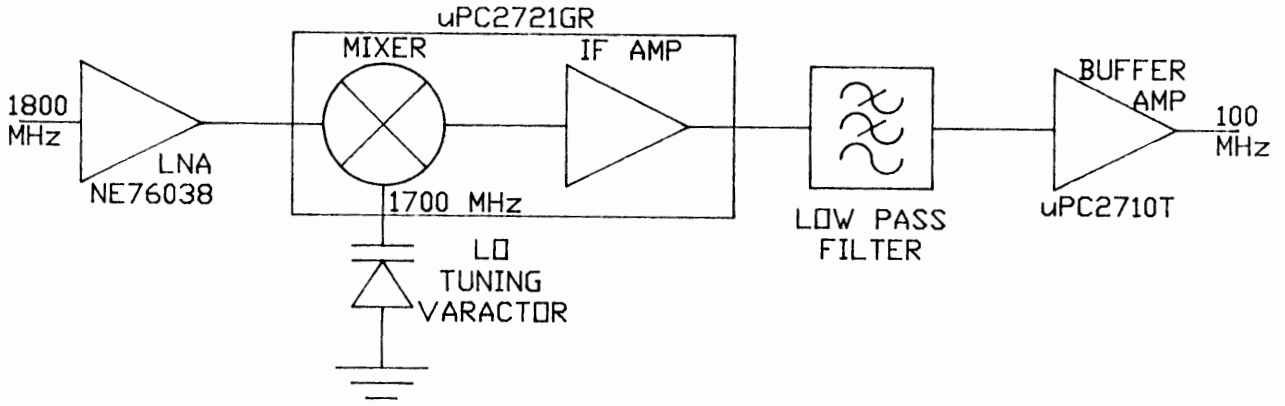


Figure 1: Block Diagram

PART LIST:

1	100 pF CHIP CAPACITOR
2	0.9 pF CHIP CAPACITOR
3	L1: ø 0.095, ø 0.020, 2T (INCH)
4	NE76031
5	20 pF CHIP CAPACITOR
6	L2: 0.6 nH MICROSTRIP LINE--- 0.1 LENGTH AND 0.01 WIDTH.
7	220 nH CHIP INDUCTOR
8	10000 pF CHIP CAPACITOR

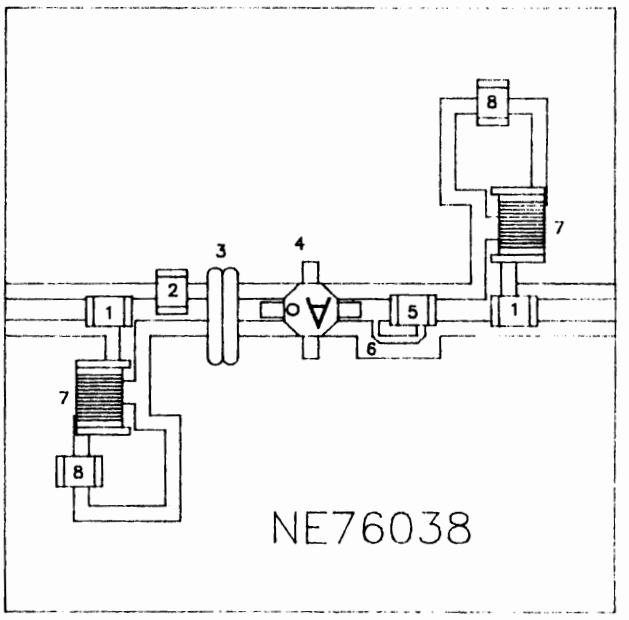


Figure 2: NE76038 LNA

PART LIST:

1	100 pF CHIP CAPACITOR
2	0.9 pF CHIP CAPACITOR
3	L1: ø0.095, ø0.020, 2T
4	NE76038
5	20 pF CHIP CAPACITOR
6	L2: 0.6 nH MICROSTRIP LINE-- 0.100 LENGTH AND 0.010 WIDTH
7	220 nH CHIP INDUCTOR
8	10000 pF CHIP CAPACITOR
9	22 pF CHIP CAPACITOR
10	UPC2721
11	0.5 pF CHIP CAPACITOR
12	2 pF CHIP CAPACITOR
13	47000 Ohm CHIP RESISTOR
14	SV166 VARACTOR DIODE
15	50 Ohm CHIP RESISTOR
16	270 Ohm CHIP RESISTOR
17	L3: ø2.0mm, ø0.3mm, 10T
18	1000 pF CHIP CAPACITOR
19	220 Ohm CHIP RESISTOR
20	50 Ohm CHIP RESISTOR
21	33 Ohm CHIP RESISTOR
22	14 pF CHIP CAPACITOR
23	L4: ø4.0mm, ø0.4mm, 3T
24	19 pF CHIP CAPACITOR
25	UPC2710TE3 PACKAGE
26	1.0 uH CHIP INDUCTOR

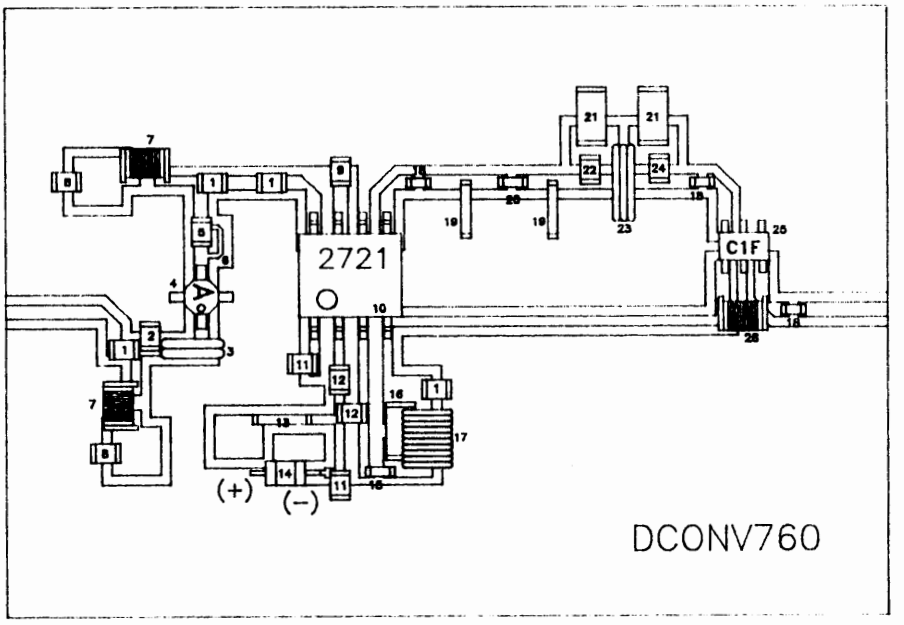


Figure 3: Overall Down-Converter Layout

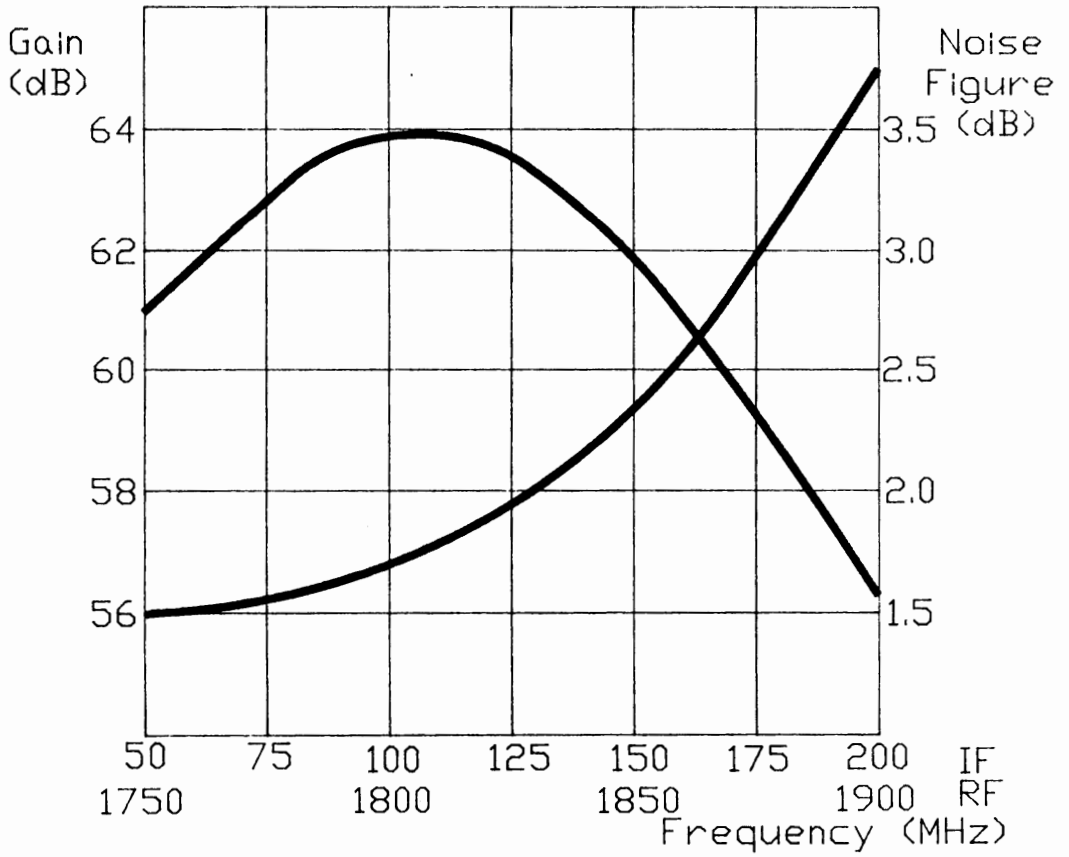


Figure 4: Gain & Noise Figure
(Local Oscillator: 1700 MHz)

Technologies for Cellular Communications

Session Chairperson: Keith Kaczmarek, *NEXTEL Communications, Inc. (Fleet Call) (Lafayette, CA)*

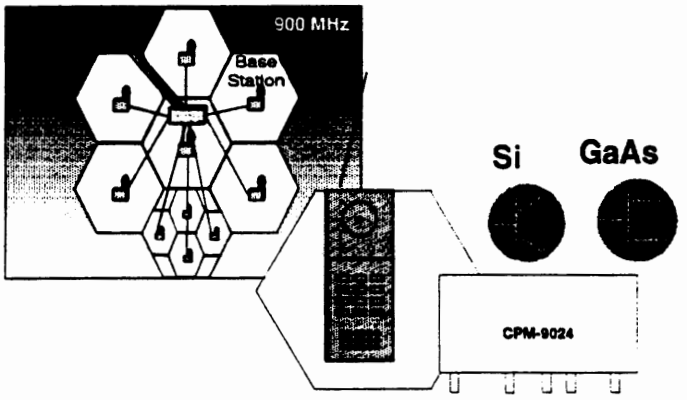
**Paper presented by Eric Botherel, Alcatel Radiotelephone (Colombes, France)*

Power Products for Cellular Telephone Handsets

William Mueller
Hewlett Packard Communications Components Division

HEWLETT PACKARD

Power Products for Cellular Telephone Handsets



A comparison of silicon and gallium arsenide power devices.

Figure 1. Power Products for Cellular Telephone Handsets.

This paper compares Gallium Arsenide Field Effect Transistor and Silicon Bipolar Junction Transistor options for the output device in 900 MHz cellular telephone handsets.

Cellular Handset Block Diagram

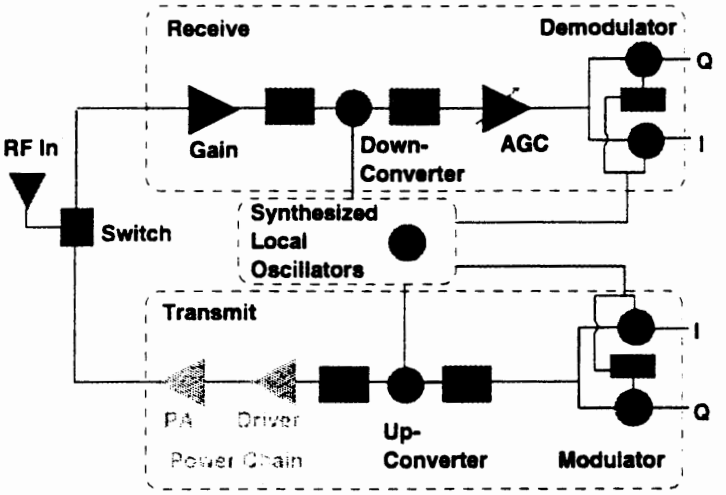


Figure 2. Cellular Handset Block Diagram

The block diagram shows a generalized architecture for a cellular handset. The products we are concerned with in this paper are the Power Amplifier and its' Driver. They are represented by the last two "triangles" in the transmit chain. The task of the power chain is to increase the magnitude of the modulated signal to the desired level for broadcast. The architecture shown is generalized, and many variations are possible, especially in the area of the modulator and up-converter.

Cellular Handset Power Requirements

AMPS	ADC	JDC	GSM
Analog	Digital (π/4DPQSK)	Digital (π/4DPQSK)	Digital (0.3 GMSK)
824-849 MHz 0.6W no IM spec	824-849 MHz 0.6W IM3<-26 IM5<-35 IM7<-40	810-826 MHz 1477-1489 MHz 1501-1513 MHz 0.6W linearity equivalent to ADC	890-915 MHz 3.5W peak (577μsec 10%) no IM spec

Figure 3. Cellular Handset Power Requirements.

Cellular can be divided into three major segments, with differing requirements for the handset power transistor.

North American Cellular consists of both an installed analog system (AMPS) and a developing digital system ADC (American Digital Cellular). At present the digital portion contains many factions, including NAMPS, CDMA users, ETDMA users, and others. North American cellular systems use a handset broadcast frequency range of 824 to 849 MHz.

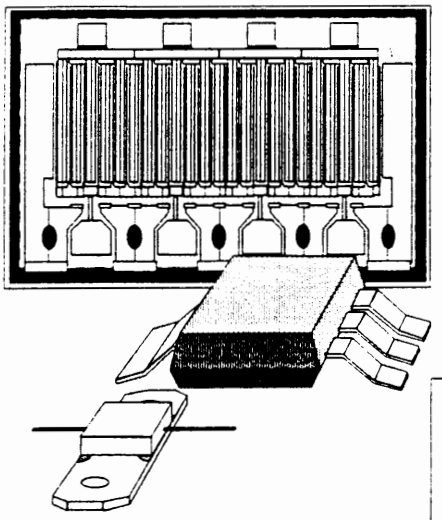
AMPS requires +28 dBm (0.63 Watts) of CW output power, but places no linearity or intermodulation constraints on the power amplifier. The output transistor is usually expected to provide a power added efficiency in the 45% range.

ADC in general uses π/4QPSK modulation, and has a linearity requirement that translates into an intermodulation specification on the output part of -26 dBC on the third order products, -35 dBC on the fifth order products, and -40 dBC on the seventh order products, all relative to two +25 dBm output signals. System operation is essentially pulsed.

JDC (Japan Digital Cellular) is the new Japanese digital system. **JDC** uses π/4QPSK modulation. Handset broadcast frequencies are 810 to 826 MHz for the 800 MHz system, and 1477 -1489 MHz and 1501 - 1513 MHz for the 1500 MHz system (metropolitan Tokyo and Osaka; also called **MCA** or Multi-Channel Access). The linearity and power requirements are essentially the same as for **ADC** use. In general, the same power transistors can be used to meet both **JDC** and **ADC** requirements.

GSM (Group Speciale Mobile) is the new European system, replacing many previous non-compatible analog systems that were similar to **AMPS**, NMT, etc. **GSM** uses 0.3 GMSK modulation. The output requirement is for 3.5 watts of peak output power with a 577 μsec, 10% duty cycle pulse. This system does not have the linearity requirement of **ADC** or **JDC**. **GSM** uses a handset broadcast frequency range of 890 to 915 MHz.

GaAs Device Performance



7.2 mm gate width
0.7 nominal gate length

die size: 41 x 29 mils

material optimized for linearity:
low gm, medium breakdown,
low current density

	Pout	Gp	IM3	IM5	IM7	Vds	Vgs	Id
ADC:	2x+25	10dB	-27	-35	-43	6V	-2 V	210 mA

Figure 4. GaAs Device Performance

One technology option for the output transistor is a Gallium Arsenide MESFET. GaAs is touted for superior mobility, operation at low voltages, and high linearity. Let's examine the performance offered by a typical device.

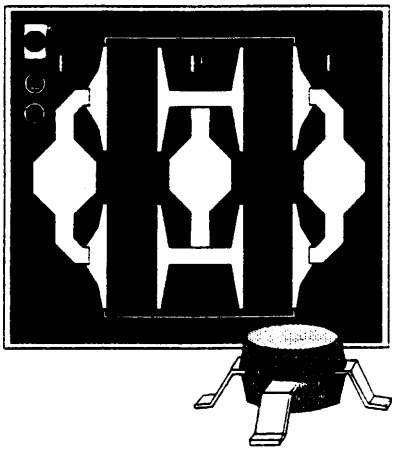
Gate length: 0.7 μm nominal
Gate width: 7.2 mm
The device has been optimized for linearity by targeting for low g_m, medium breakdown voltages, and low current density. These features derive both from the processing and the physical layout (finger length, spacing).

Packaging is a major concern, as source inductance from package parasitics significantly degrades performance. The desired package is something like a SOT-223: plastic, surface mount, low cost. However the SOT-223 package has very large parasitic inductances, and gives an unrealistically poor view of the GaAs FET performance. Additionally, it can limit the power dissipation of the assembled device due to poor heat conduction. The GaAs FETs measured for this paper were mounted in a 100 mil flange package which, in addition to having minimal source inductance, also provides excellent heat sinking. Although this package is too costly for commercial applications, it allowed us to examine the capabilities of the die unencumbered by package limitations. We felt this approach to be valid, as present market use is commonly in hybrid power modules which may make use of low parasitic carriers rather than packages.

Typical performance capability of one cell in 100 mil flange:

Pout [dBm]	Gain [dB]	IM3 [dBC]	IM5 [dBC]	IM7 [dBC]	Vds [V]	Ids [mA]	ηadd [%]
2x+25	14	27	35	43	6	210	48

Silicon Bipolar Power Transistor



Silicon power cell:

19 x 24 mils
3.4 micron E-E pitch
160 fingers
40 microns long

ft =10 GHz
fmax = 23 GHz

	Pout	Gp	IM3	IM5	IM7	Vce	Ic
ADC:	2x+25	10dB	-27	-37	-43	6V	270 mA

Figure 5. Silicon Bipolar Power Transistor

A second option for the output transistor is a Silicon bipolar junction transistor (BJT). Silicon is touted for low cost and repeatability. High frequency silicon cells are less common than GaAs devices, but can perform nearly as well. A typical silicon power cell has the following features.

3.4 micron emitter to emitter pitch
160 fingers each 40 microns long
The device is optimized for high f_t through material and diffusion, and laid out for best thermal distribution - note the four active areas to distribute the power dissipation.

The silicon die is smaller than the GaAs FET shown previously, and is used as a building block. A single cell can work as a driver device; producing an output power of several hundred milliwatts. For pulsed operation a single cell can be mounted in an 85 mil plastic surface mount package with low parasitic inductance. For higher power output, three cells are combined in parallel on a low parasitic ceramic carrier. Data in this paper is most often for the three-cell carrier configuration.

Typical performance capability of 3 cells on a carrier:

Pout [dBm]	Gain [dB]	IM3 [dBC]	IM5 [dBC]	IM7 [dBC]	Vds [V]	Ids [mA]	ηadd [%]
2x+25	10	27	37	43	6	270	35

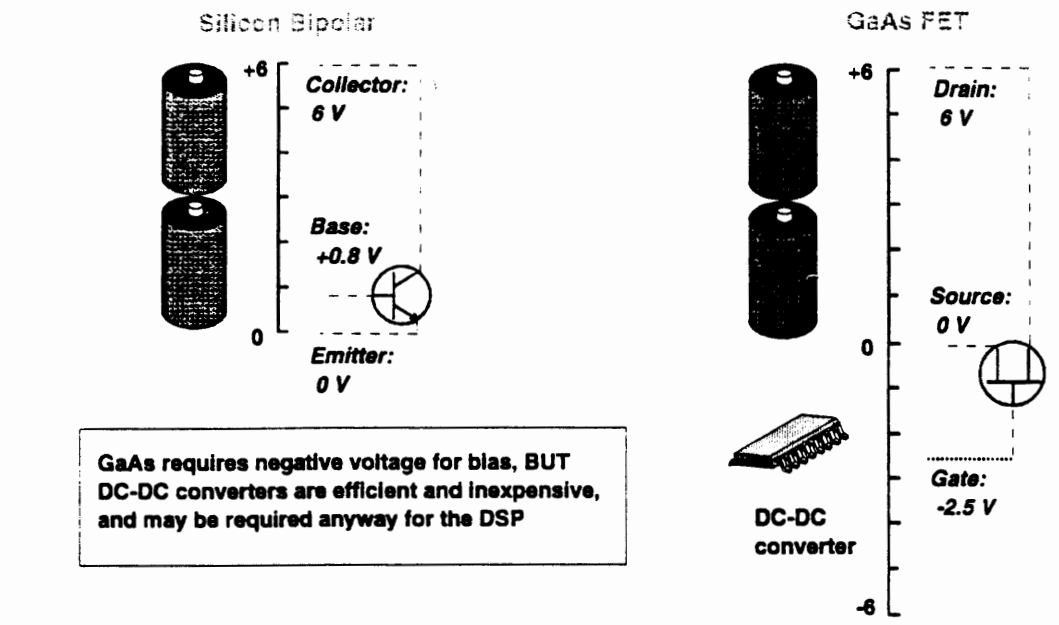


Figure 6. Operating Voltage

Cellular handsets run from batteries. Present phones have 6 V available, with a trend to lower voltage (3V) in the future. The output transistor must be able to operate from this kind of voltage source.

GaAs has the reputation for being the better power provider at low Vds values. Significant power can be obtained with Vds as low as 1 to 2 volts. However for a depletion mode GaAs FET, the gate must be at a lower potential than the source for operation. This adds the need for a negative power supply rail, typically on the order of -2 V. The availability of highly efficient, inexpensive DC-DC converters keeps the need for a second supply line from being a problem in most cases.

Silicon reputedly requires a high Vce for power. This is somewhat misleading: most Si transistors on the market have not been optimized for operation at low voltages. With proper targeting, good gain and power can be obtained at voltages in the 3 to 5 V range, and no negative supply is needed.

Both technologies can work now from a 6 volt battery; both can be target to work in the future from a 3 volt supply. If the need for a DC-DC converter is discounted, there is no clear "low voltage advantage" to either technology.

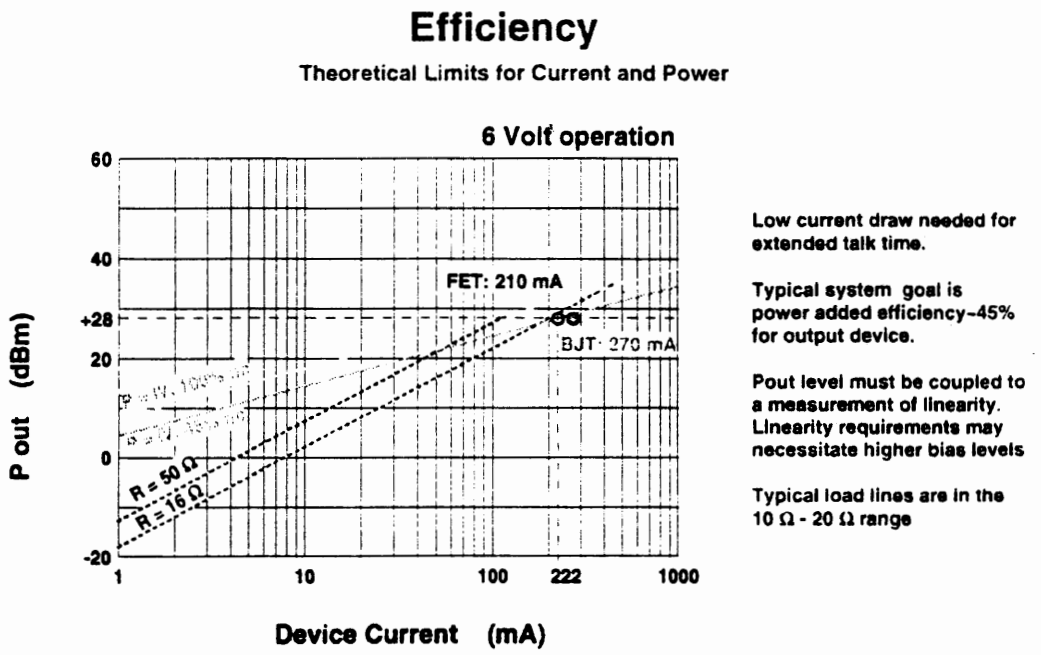


Figure 7. Efficiency: Theoretical Limits for Current and Power

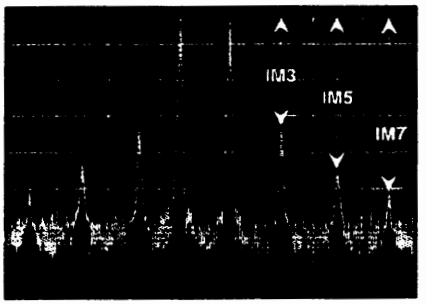
One of the primary selling features of handsets is talk time. This translates into a need for the lowest achievable current draw from the power stage, which is the "current hog" of the phone. With the assumption that the voltage is fixed by the battery selection, efficiency become the measuring stock for device performance.

However power is the product of voltage and current. So when the voltage is fixed by battery selection and the power is fixed by radio specification, a minimum current results from P = IV. It is unrealistic to expect 100 % efficiency, so it is also informative to look at curves for Pout vs. Device Current for an expected efficiency of 45% (a typical target for the cellular handset output device).

Load line also effects efficiency, since $P = I^2 R$. The design of the output match must set R low enough that the desired efficiency can be reached. For most devices, the output load line will be between 10 and 20 ohms. The FET circuit used a 16 Ω load line; the bipolar circuit used a 12 Ω load line.

From these curves we can see that the target current draw is in the low 200's of mA for the required +28 dBm of output power.

Load Line



Loadline = 16 Ω
Harmonics (2nd and 3rd) terminated in 16 Ω

Pout	IM3	IM5	IM7	Vds	Vgs	Id
2x+25	-27	-35	-43	6V	-2 V	210 mA

Loadline = 16 Ω
Harmonics (2nd and 3rd) reflected

Pout	IM3	IM5	IM7	Vds	Vgs	Id
2x+25	-24	-35	-38	6V	-2 V	240 mA

Output Power depends on linearity, which is a function of loadline at the fundamental and harmonics

Figure 8 Load Line

Linearity isn't as simple as just the bias. The load line must be set to allow the output voltage to swing without "clipping" or distorting. The loadline is set by some resistance, derived from voltage swing for desired power, modified by some reactance, set by the device parasitics (typically output capacitance and bond wire lengths). As parasitics are similar for GaAs and Si, the load lines (i.e. the output impedance to match to) are also similar, so neither technology has a significant advantage in impedance matching requirements.

Termination of the harmonic will additionally effect efficiency and intermodulation levels. If the harmonics are reflected, efficiency will be maximized. If the harmonics are terminated, lowest distortion will result. It turns out that from a system point of view optimum performance is in the "harmonics terminated" case. The attached data compares the same device in a circuit which reflects the harmonics with one that terminates them. The termination selected was 16 Ω, the same load line presented at the fundamental. This circuit technique works with both Si and GaAs.

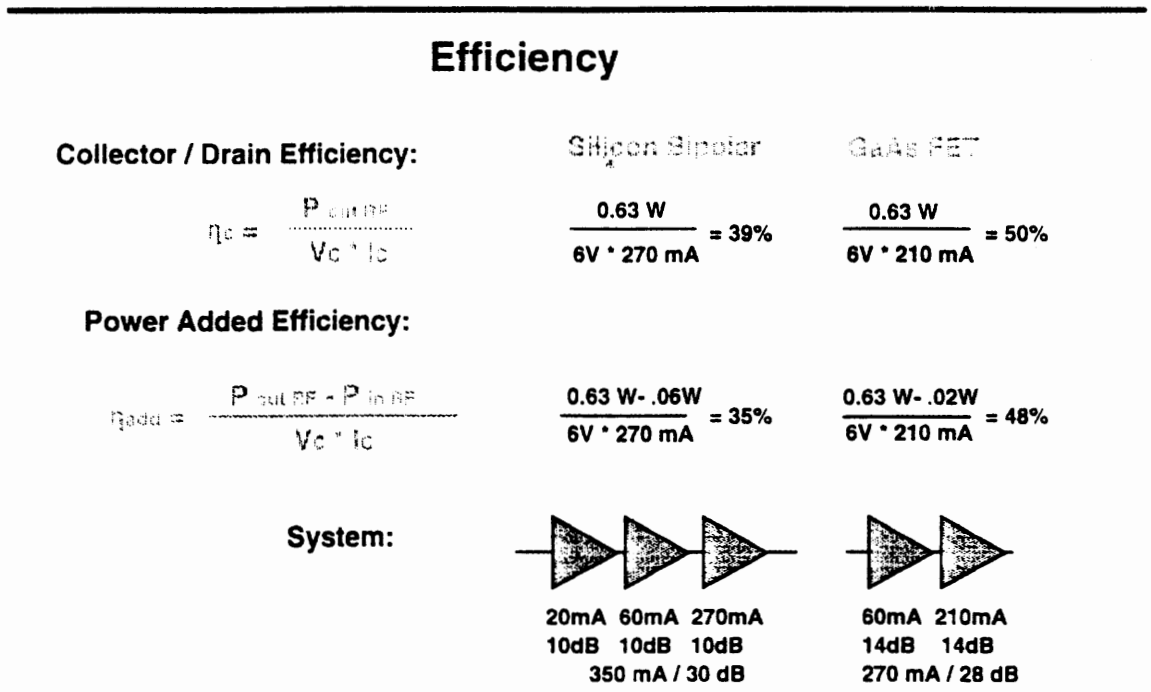


Figure 9. Efficiency

Efficiency should be evaluated using ηadd (power added efficiency) in preference to ηc (collector - or drain - efficiency) as ηadd takes into account the reduction in current that will result with the use of a high gain driver stage. Efficiency is tied to some output power level, which for digital phones is a function of the linearity needed. For a quotation of efficiency to be meaningful, the linearity as well as the power level must be clearly specified. The goal of the designer is to expend minimum current to get sufficiently low intermodulation distortion at the necessary output level and still maintain reasonable gain.

Collector / drain efficiencies are similar for Si and GaAs; however the present higher gain of GaAs gives this technology an edge in power added efficiency.

Bias point.

Biasing enters the picture to set the linearity associated with the output power. Very high efficiencies (>65%) are possible for self biased or "Class C" amplifiers, however these amplifiers have poor dynamic range and high distortion. Class C amplifiers can meet the requirements of analog AMPS, but not of any of the digital cellular schemes. Linear performance is achieved by biasing the device fully on (class A - no current shift with applied RF), but class A has a theoretical maximal efficiency of 50 % and realistic performance in the 30% range. Most handsets actually allow the current to pull somewhat with drive (Class AB operation). In this mode it is important to select a quiescent (no drive) bias point that results in the lowest intermodulation. Often there is a distinct "nulling" phenomena that occurs with class AB bias. Typical efficiencies in handsets are in the 45% range.

Si obtains a class AB bias by applying a slight positive voltage across the emitter base. GaAs requires a partial (but not full) pinching off of the gate. Thus GaAs needs more complicated circuitry in that a negative supply voltage must be provided. The alternative of a source resistor to allow the Gate to be more negative is usually impractical in a power stage because of the high dissipation requirement that results from the significant amount of current flowing. A bypassed source resistor also provides more parasitic source inductance than does a grounded source configuration.

Thus Si has a slight edge over GaAs in ease of use for biasing.

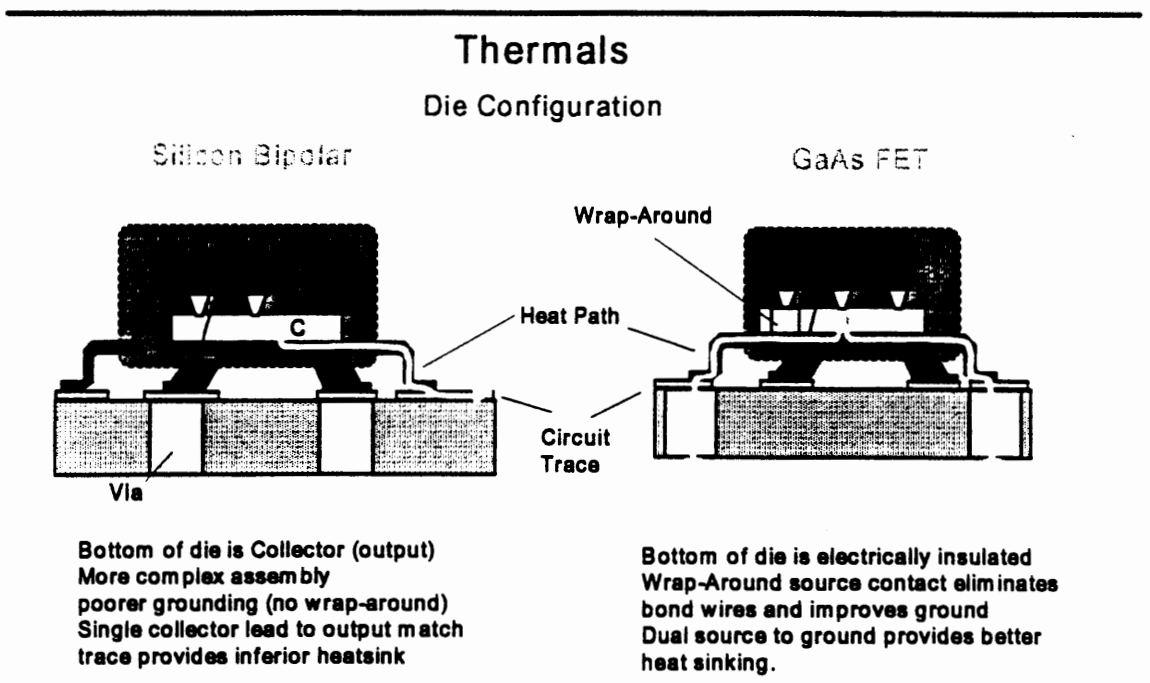


Figure 10. Thermals (Die Configuration)

The reliability of semiconductor devices ultimately reduces to the junction (or channel) temperatures at which they operate. From a purely theoretical point of view, GaAs usually allows channel temperatures as high as 175 ^{o} C, whereas Si allows junction temperatures up to 200 ^{o} C. This apparent edge to Si is largely negated by packaging: most cellular output devices are placed in plastic packages to keep costs low, and the plastic typically reduces maximum operating temperature for either technology to 150 ^{o} C.

GaAs has a layout advantage over Si for heat sinking. The backside of a GaAs FET is electrically isolated from the FET, and so may be die attached to the "common" or ground metalization of the device package. Common leads provide the best heat sinking for several reasons. First, most high frequency packages used multiple ground leads to keep parasitic inductance small. This also provides multiple heat flow paths for improved thermal conductivity. Second, common leads attach to the ground plane, which is typically the largest heat mass and thus the best heatsink in the system.

In contrast, the backside of a Si BJT is the collector, or output terminal. The collector must attach to the output circuit, a much poorer heatsink than the ground plane as its' shape (both electrical and mechanical) is determined by loadline requirements.

Thus GaAs has an advantage in thermal performance. However, proper design for current density typically keeps MTTFs for both devices in excess of 10^6 hours. (MTTF or Mean Time To Failure is the time at which 50% of the devices have failed in a reliability test, and is an accepted reliability measure of a non-repairable device such as a semiconductor.) Thus reliability is not an issue for either technology. The fact that digital cellular effectively uses pulsed operation also removes much of the thermal load from handset parts.

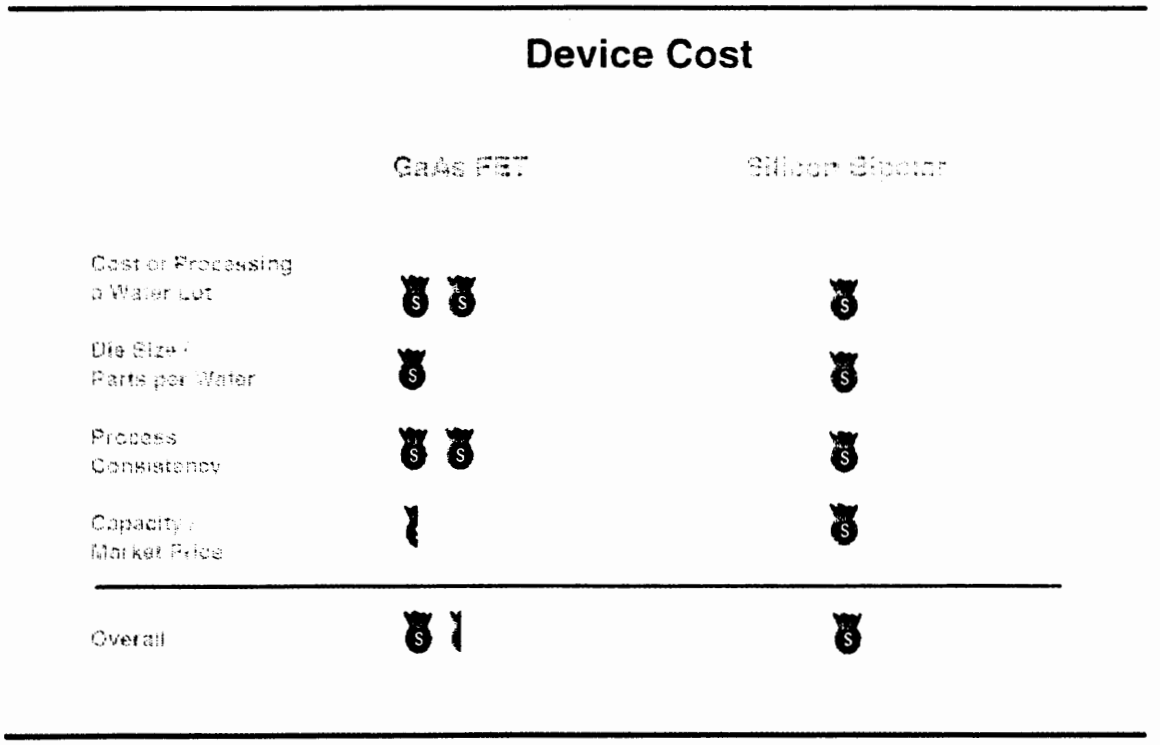


Figure 11. Device Cost

Cellular telephones are consumer products. This puts extreme price pressure on all components. The output device probably needs to sell for <$5 at present, with this number decreasing in the future.

Silicon is less expensive to process, sometimes only costing 1/2 as much as Gallium Arsenide. Silicon and GaAs can achieve roughly equivalent power densities, so number of chips/wafer should be similar (assuming the same size wafer). Silicon material is typically more consistent than GaAs, and the process more mature, so the expectation is that silicon based products will be more repeatable, have narrower distributions of performance and hence higher yields. The repeatability also leads to better modeling and improved simulation for design, which may translate into fewer design iterations and faster time-to-market.

However, it's a tough market place, and at present there are an overabundance of GaAs FABs all seeking to defray costs by manufacturing something. Consequently, the market price of GaAs products may not necessarily reflect the manufacturing costs. If GaAs manufacturers are actually operating at a loss, then the present situation may prove unstable and not be indicative of long term pricing. None-the-less, although silicon should perhaps have a big plus in lower cost, in fact it may not in today's market place.

Summary

1. Silicon power devices cost less to produce than GaAs power devices. The materials costs are lower, and the yields typically higher due to better product consistency. This advantage is at present largely negated by the current glut of GaAs fab capacity.

1. The gain of GaAs FETs is presently higher than that of Si BJTs. This results in fewer stages of amplification (simpler / smaller design) and lower system current drain (longer talk time).

2. The semi-insulating nature of the GaAs substrate and the physical layout of a depletion mode MESFET allow for die attach on the common lead. This results in both better heatsinking (lower operating temperatures) and lower common lead inductance (improved gain).

Figure 12 Summary

Examining the two technologies, we see that on most issues both silicon and GaAs can provide equally acceptable solutions.

Silicon's greatest strengths are its consistency and lower manufacturing costs. At present these may not be meaningful because of the over-abundance of GaAs suppliers and their willingness to take business at small margins. It remains to be seen if this situation is stable.

GaAs's greatest strengths are higher gain and a superior physical configuration. The gain advantage may disappear with future generations of bipolars. A advantage of a superior configuration is likely to exist for some time.

Cellular and PCS TDMA Transmitter Testing with a Spectrum Analyzer

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ABSTRACT: New technology has provided spectrum analyzers with specialized measurement capabilities for testing time-division multiple-access (TDMA) carriers. Time-domain and time-gated functions, along with built-in and downloaded measurement routines, simplify testing of burst carriers for the new mobile-communication digital formats.

Practical spectrum analyzer measurement techniques are described for these tests: carrier power, carrier-off power, adjacent channel power, spurious emissions, burst timing, and frequency deviation. While most examples are for the North American Digital Cellular TDMA (IS-54) system, the information presented also applies to other formats such as GSM, DCS 1800, JDC, CT2, and DECT.

Introduction

The spectrum analyzer is recognized as a valuable tool for making RF performance measurements on analog mobile communication systems. It has found use for both in-channel and out-of-channel transmitter measurements. The spectrum analyzer can also be an extremely useful tool for measuring and troubleshooting the base and mobile stations of the new digital mobile communication systems that employ TDMA (Time Division Multiple Access) or TDD (Time Division Duplex). The TDMA and TDD systems have burst carriers rather than the continuous carriers of analog systems. This poses new challenges for test equipment. In the last few years new capability has been added to some spectrum analyzers to provide sophisticated measurements on burst carriers.

Spectrum Analyzer Requirements for Burst Carriers

New spectrum analyzer hardware is required for measurements made on burst carriers. Traditionally, the spectrum analyzer has been used primarily for making measurements in the frequency domain. But for communication systems using TDMA or TDD, time domain measurements are also important. Adding a fast digitizer allows zero-span measurements to be made with sweep times as fast as 20 µs. Delayed sweep trigger capability allows the displayed waveform to be expanded about an arbitrary point in time. Limit lines for time domain waveforms provide internal comparison between the waveform and a specified limit mask. An important development is time-gated spectrum analysis, which adds a gated-video capability to frequency domain measurements. This technique allows the transient spectral power to be excluded, revealing the spectrum due to modulation and noise.

The spectrum analyzer setup and computation for these digital burst carrier systems are more complex than for the analog systems. Built-in functions or application specific downloadable software allow these complex measurements to be made quickly and accurately by the user. One-button measurements can be provided that automatically measure the signal level, adjust the input attenuation and reference level of the spectrum analyzer, establish the spectrum analyzer settings, perform computations, and display graphical and numerical results. The measurement sets are similiar for the different digital cellular and

Carrier Off Power

The carrier off power is the transmitter power during that part of the frame when the carrier is off. A spectrum analyzer also makes this measurement in zero span. Very low levels are specified for the carrier off power to insure that one radio does not interfere with another. For improved sensitivity, a narrower spectrum analyzer resolution bandwidth is often chosen for this measurement than for the carrier power measurement. A video trigger is usually used. Fig. 3 shows a carrier off power measurement on a NADC-TDMA carrier.

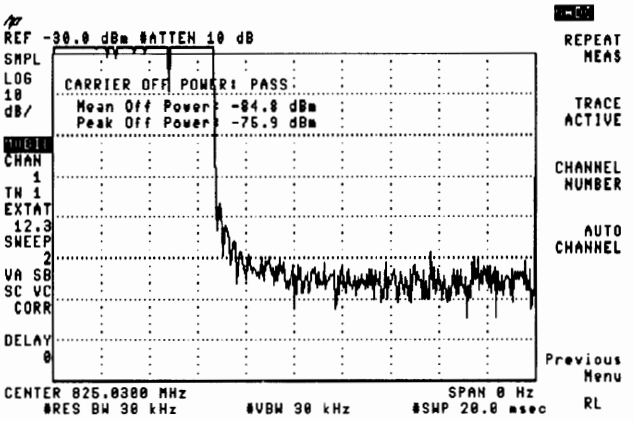


Fig. 3 Carrier off power measurement example for a burst NADC-TDMA carrier

Burst Timing Ramp-up and Ramp-down

The various standards define time domain masks; an example is given in Fig. 4. A minimum power must be maintained for the on part of the burst. To avoid interference it is important that the ramp-up and ramp-down times do not extend into adjacent time slots. The time domain masks do not specify a minimum limit for the ramp-up and ramp-down times. However, the faster these transitions, the greater will be the spectrum broadening (splatter) into the adjacent channels. The adjacent channel power limits allow very little spectrum broadening from ramping, so in practice nearly all of the allotted time is used for the ramp-up and ramp-down of the burst. The standards generally specify relative limits, but certain segments are sometimes specified at absolute power values.

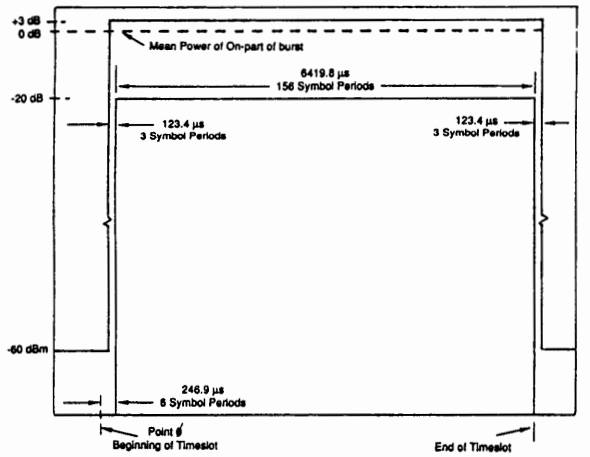


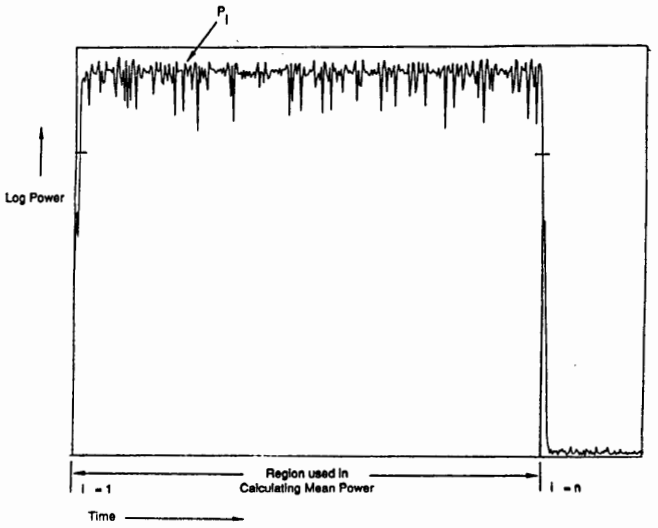
Fig. 4 Burst power mask for NADC as defined in EIA/TIA IS-55

Spectrum analyzers are high dynamic range instruments, but even they are challenged by the requirements for some TDMA systems. For example, the NADC-TDMA IS-55 standard specifies a -60 dBm off level, which for a 3 watt mobile requires a 95 dB measurement range. By the use of downloadable software routines, it is possible to get as much as 110 dB of on-screen calibrated dynamic range for this measurement, even from an analyzer that normally has an 80 dB log display.

PCS systems such as GSM (Groupe Speciale Mobile), DCS 1800 (Digital Communications System 1800 MHz), NADC-TDMA (North American Digital Cellular, IS-54), JDC (Japan Digital Cellular), CT2 (Cordless Telephone 2nd generation), PHP (Personal Handi-Phone) and DECT (Digital European Cordless Telecommunications). But, the standards for each of these have unique measurement methods, terminology, and limits. Separate software specifically tailored for each format offers convenience and confidence to the user. Additional confidence is provided when the manufacturer specifies the range and accuracy for each one button measurement.

Carrier Power

The carrier power is specified to be the mean power during the on part of the burst. With a spectrum analyzer, the measurement is made in zero-span (fixed tuned) mode with a log amplitude display. The analyzer's resolution bandwidth is set to be greater than the channel bandwidth, and the video bandwidth is set to be equal or greater than the resolution bandwidth. A video trigger is usually used, but an external trigger is also possible. The trace data is then averaged for the on part of the burst. For modulation formats with a significant amplitude variation, such as $\pi/4$ DQPSK (differential quadrature phase shift keying), it is important that a true power average be performed. Using the video average function or a reduced video bandwidth will provide averaging of the trace, but it will be the average of the log of the power. Obtaining the mean power requires that the trace data be anti-logged prior to averaging the data numerically (Fig. 1). An actual measurement of carrier power on a NADC-TDMA carrier is shown in Fig. 2.



$$P_{mean} = 10 \times \log\left[(1/n) \times \sum_{i=1}^{n} 10^{P_i/10}\right]$$

where:

P_{mean} = Mean carrier power during on part of burst (dBm)

P_i = Power level at sample point i of the waveform (dBm)

n = Number of sample points in the on-part of the burst

Fig. 1 Carrier power definition and equation

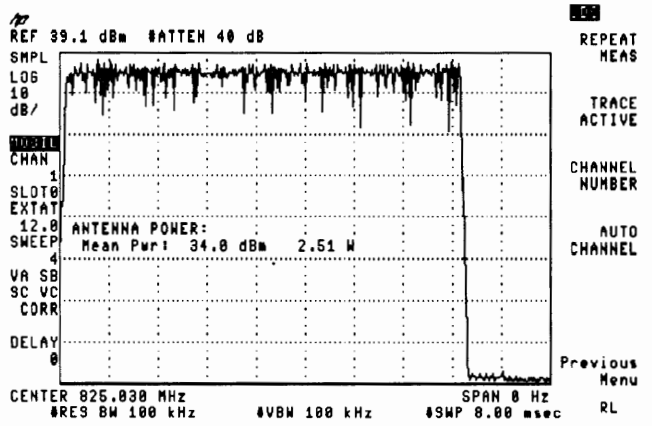


Fig. 2 Carrier power measurement example for a burst NADC-TDMA carrier

A fast digitizer and delayed sweep trigger capability are required to make these burst timing measurements. An external trigger signal is needed to trigger the delayed sweep. One way to obtain this trigger is to use a burst carrier trigger device that envelope detects the rising edge of the RF burst and converts it into a TTL signal. Fig. 5 shows a power versus time measurement over the entire burst and Fig. 6 shows a measurement for the ramp-up part of a burst.

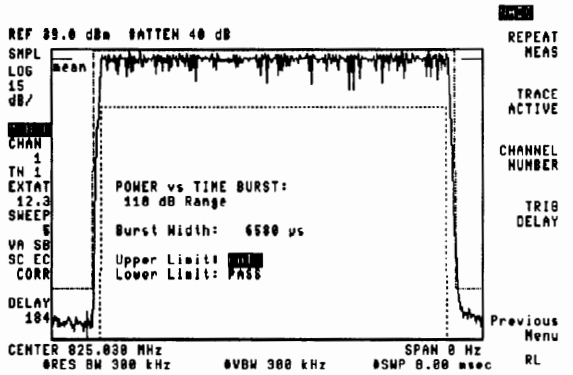


Fig. 5 Burst measurement example for a NADC-TDMA carrier

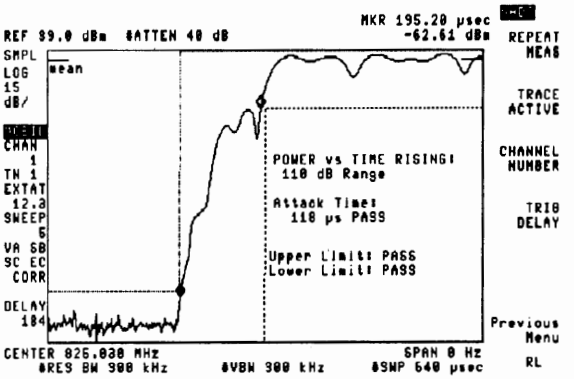
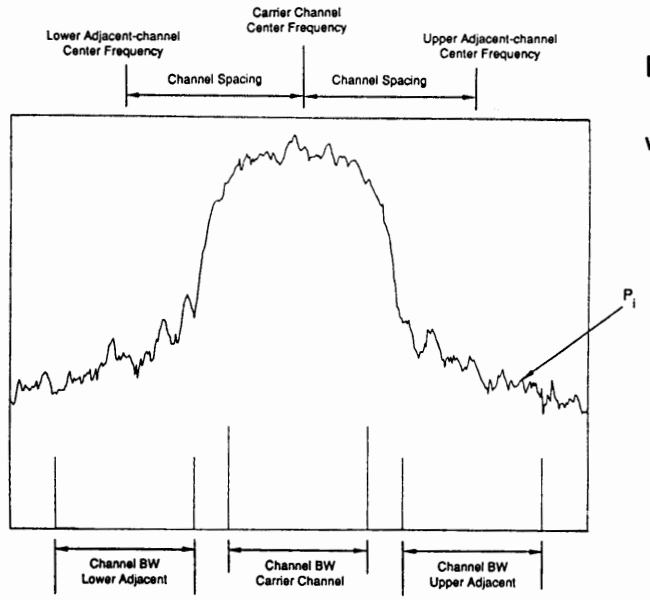


Fig. 6 Ramp-up measurement example for a NADC-TDMA carrier

Adjacent Channel Power (ACP)

Adjacent channel power is a measure of the amount of leakage power that is present in the adjacent channels. It is usually specified as a ratio to the total carrier power, but sometimes it is specified as an absolute power. It is measured with a spectrum analyzer using an integration method. For analog or continuous (non-burst) digital carriers, the measurement is made by obtaining a frequency domain trace of the spectrum using a sample detector. The analyzer's resolution bandwidth is set to be much narrower than the channel bandwidth. The video bandwidth should be at least ten times the resolution bandwidth to give power detection. The leakage power contained in the adjacent channel is computed with the power integration equation (Fig. 7). This equation averages the power contained in the all the trace elements within the adjacent channel integration bandwidth (sometimes called the specified bandwidth); and it applies a scaling factor based upon the ratio of the power (noise) bandwidth to the integration bandwidth.



$$P = (B_s/B_n) \times (1/n) \times \sum_{i=1}^{n} P_i$$

where:

- P = RMS-like power in the specified integration bandwidth (watts)
- P_i = Power level at sample point i of the spectrum (watts)
- B_s = Specified integration bandwidth for adjacent channel (Hz)
- B_n = Effective noise bandwidth of spectrum analyzer (Hz)
- B_n = 1.13 x BW_{3dB} (for 4-pole synchronously tuned RBW filter)
- n = Number of sample points in the specified bandwidth

Fig. 7 ACP definition and power integration equation

The ACP measurement is much more complex for burst carriers. To acquire a frequency domain spectrum trace without "drop-outs" requires the use of a peak detector rather than a sample detector. In addition, the sweep time must be slow enough so that at least one burst will occur for each trace element point. For example, the NADC and JDC systems have one burst every 20 ms, which, with a 400 point trace, requires an 8 second sweep.

The spectrum of a burst carrier also contains a transient component due to the burst ramping, in addition to the usual modulation and noise component. The correct integration equation for the ramping component is different than the equation for the modulation and noise component. The modulation and noise result is calculated with the power integration equation, whereas the transient component result is calculated with an impulsive noise power integration equation.

A very effective and practical way to separate the spectrum due to modulation and noise from the total spectrum, which also contains the transient spectrum, is with time-gated spectrum analysis (Fig. 8). This gated-video approach requires an external trigger signal. The gated-video is typically set so that the gate is on during the 50% to 90% part of the burst. If the gate is turned on too early, the IF filters will not have settled sufficiently and a residual transient will affect the spectrum. With correctly set gating, the resulting spectrum is the same as would be obtained if the transmitter had a continuous carrier. The adjacent channel power due to modulation can then be calculated by using the power integration equation. The adjacent channel power due to transients can be obtained by using the impulsive noise integration equation on the difference between the total spectrum and the modulation and noise spectrum. A total is sometimes calculated by adding the ACP due to modulation to the ACP due to transients. This total results from adding two peak powers with different time characteristics, so it should not be considered an RMS adjacent channel power (Fig 9).

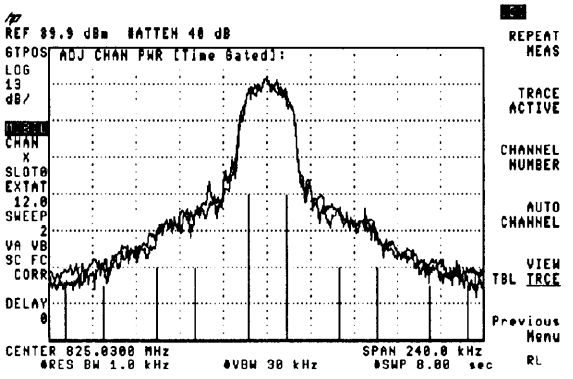


Fig. 8 ACP measurement example for a JDC-TDMA carrier showing separation of modulation spectrum from total spectrum by using time-gated spectrum analysis

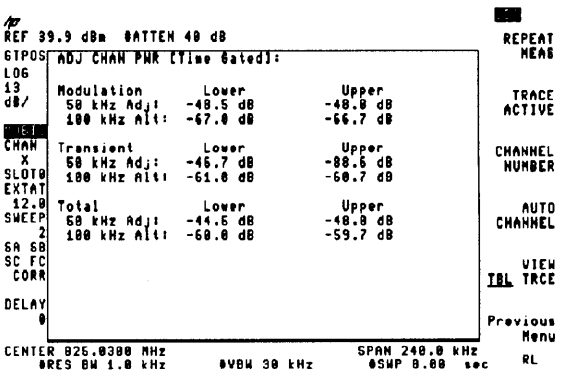


Fig. 9 ACP numerical results example for a JDC-TDMA carrier

The method of measurement for ACP varies in many details for the different digital mobile communication systems. Some systems specify only lower and upper adjacent channels, others specify additional channels (sometimes called alternate channels). A rectangular integration bandwidth is usually specified or assumed, but IS-55 and IS-56 specify the application of a Nyquist square-root-raised cosine filter prior to performing the integration. For the new digital cellular phone and cordless phones the ACP limits in the adjacent channel are rather loose, so the phase noise performance of the spectrum analyzer is not an important issue. However, spectrum analyzer dynamic range needs to be considered for measurements in the alternate channels. With downloadable software, the on-screen calibrated dynamic range can be extended beyond the capability of the unaided spectrum analyzer. The display in Fig 8 shows a dynamic range of over 100 dB (the log scale is 13 dB per division).

Spurious Emissions

Both in-band and out-of-band spurious emissions, including intermodulation spurious, are measured in much the same way for TDMA and TDD systems as for analog mobile communication systems. However, there is an important point that is often overlooked. The normal spectrum analyzer auto sweep-time will ensure that continuous spurious signals have the correct amplitude, but burst spurious may be under-represented or even missed. A spur search for burst spurious signals requires a slower sweep time as given by:

$$ST \geq PRI \times Span/RBW$$

where:

ST = Sweep Time of spectrum analyzer (sec)
PRI = Pulse Repetition Interval of burst (sec)
Span = Frequency span of spectrum analyzer (Hz)
RBW = Resolution Bandwidth of spectrum analyzer (Hz)

For example, NADC and JDC have PRI= 20 ms. Then for RBW = 1 MHz, the sweep time must be at least 20 s/GHz.

Modulation Accuracy

By using a hardware analog FM demodulator circuit in conjunction with an external trigger signal, it is possible to obtain traces of the frequency deviation versus time for a burst FM carrier. The trace data can then be used to compute the peak frequency deviation and mean frequency error (Fig 10). This technique is useful on burst BPSK modulated carriers, such as those used in the CT2 system. The modulation and frequency analysis for $\pi/4$ DQPSK and GMSK modulations requires DSP (digital signal processing) techniques. This capability could be provided in a spectrum analyzer through the use of DSP processing hardware and downloadable software.

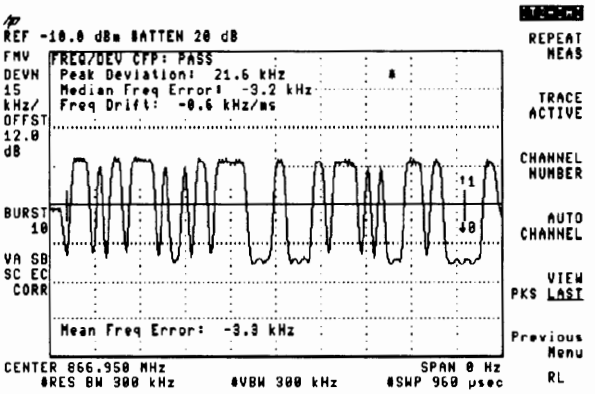


Fig. 10 FM deviation measurement example for a burst CT2 TDD carrier

Conclusion

Spectrum analyzers with the right hardware features are especially well suited for measuring the burst carriers of the new digital TDMA or TDD mobile communication systems. Fast digitized sweeps, delayed sweep trigger, and time-gated spectrum analysis (gated-video) are available on the Hewlett-Packard HP 8591 and HP 8560E families of portable spectrum analyzers. In addition there are a number of mobile communication downloadable software products for use on the HP 8591 spectrum analyzer family. Downloadable measurement personalities are currently available for the GSM, DCS 1800 (PCN), NADC, JDC, and CT2 formats. These offer automated one-button measurements that follow the method of measurements, terminology, and limits of the applicable standards document. Powerful measurement solutions are provide by the combination of a full-function general purpose spectrum analyzer and downloadable software tailored for specific mobile communication systems. With the current hardware and downloadable software, most digital transmitter parametric measurements can be made with a spectrum analyzer. It is expected that additional measurements for digital mobile communication systems will be added to spectrum analyzers in the future. While this paper has dealt with measurements on TDMA systems, with appropriate downlaodable software, spectrum analyzers could also provide a similiar set of useful measurements for CDMA systems.

References

1. J. Gorin, "Make Adjacent-Channel Power Measurements," *Microwaves & RF*, May 1992, pp 137-143

2. H. Chen, "Time-Selective Spectrum Analysis (TSSA): A powerful tool for analyzing TDMA communication signals," Hewlett-Packard RF & Microwave Measurement Symposium, Signal Analysis Division, 1992.

3. EIA/TIA IS-54 "Cellular System Dual Mode Mobile Station - Base Station Compatibility Standard," Telecommunication Industry Association, Apr 1992.

4. EIA/TIA IS-55 "Recommended Minimum Performance Standards for 800 MHz Dual Mode Mobile Stations," Telecommunication Industry Association, Dec 1991.

5. EIA/TIA IS-56 "Recommended Minimum Performance Standards for 800 MHz Base Stations Supporting Dual Mode Mobile Stations", Telecommunication Industry Association, Mar 1991.

6. RCR STD-27A "Japan Digital Cellular Telecommunication System Standard," Research and Development Center for Radio Systems, Japan, Jan 1992.

7. MPT 1375 "Common Air Interface Specification," Department of Trade and Industry, London, May 1989.

8. I-ETS 300 131 "Radio Equipment and Systems (RES); Common air interface specification to be used for interworking between cordless telephone apparatus in the frequency band 864,1 MHz to 868,1 MHz, including public access services." European Telecommunications Standard Institute, France, Apr 1991.

ERROR FREE MOBILE DATA COMMUNICATIONS: PRINCIPLES AND PROTOCOLS

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Abstract - The potential growth of wireless data communications over digital cellular and cell digital packet data presents new challenges to those engineers who are or will be involved in design and development of such systems. This paper describes protocols for error-free data transmission over communications links in these cellular systems. Efficient ARQ-based protocols are introduced to achieve high transmission throughput in multipath fading environments that these cellular channels encounter. In order to further reduce severe multipath fading and signal shadowing effects and to achieve robust data transmission auxiliary error protection techniques such as forward error correction (FEC) and diversity reception together with ARQ scheme must be employed. These schemes are incorporated into radio link protocols so called ARQ/FEC/DIV RLPs which are designed to support reliable data transmission across a radio link having a cellular frame architecture. These protocols can be used , for example, to provide error-free facsimile signal transmission and async data services in mobile radio environments.[1] The throughput performance of ARQ/FEC/DIV protocols as a function of fading parameters for different communication channels are investigated.

[1] Async Data and Group 3 Fax services are currently being standardized by EIA/TIA.

I INTRODUCTION

Error control is an area of increasing importance in data communications. The problem of providing reliable data communications over a mobile radio channel using error control techniques has received considerable attention recently [1 – 9], [20 – 30]. There are two main classes of channel coding techniques which are commonly used to improve the performance of a mobile communications system: ARQ schemes and forward error correction schemes (FEC). Error detection combined with retransmission on request, known as automatic RQ (ARQ) is a basic channel coding technique which have been used over three decades as a means of obtaining reliability in digital data transmission primarily for wireline channels [10 – 19], [31 – 35]. However, mobile digital communications systems are generally affected by noise and channel impairments such as multipath fading and Doppler effects as well as interference that degrade the reliability of the received information. In order to reduce severe multipath fading and signal shadowing effects and to achieve robust data transmission auxiliary error protection techniques such as forward error correction (FEC) and diversity reception together with ARQ scheme has been proposed. When FEC is used in conjunction with an ARQ protocol, it is called hybrid error control or *hybrid ARQ*. Hybrid ARQ schemes potentially offer better performance if appropriate ARQ and FEC schemes are properly combined. Either block or convolutional codes may be used for FEC. There has been a large number of variations on the basic ARQ theme which are detailed in [13] and references therein. These schemes are incorporated into radio link protocols so called ARQ/FEC/DIV RLPs which are designed to support reliable data transmission across a radio link having a cellular frame architecture. These protocols can be used , for example, to provide error-free facsimile signal transmission and async data services in mobile radio environments. The throughput performance of ARQ/FEC/DIV protocols as a function of fading parameters for different communication channels are investigated.

Figure 1 shows a reference model of the Interim Standard (IS-54) data channel set-up for a digital cellular system [22]. The terminal (TE2) is assumed to generate a stream of user's (raw) data in data blocks format. The mobile modem (MT2) is responsible for providing a reliable, connection-oriented, data delivery service by encoding the incoming data stream with a proposed FEC and to maintain a bookkeeping service on data blocks delivered across U_m interface by using a proposed ARQ scheme. A diversity technique must be used to further improve the perform-

ance of the system across the link. EIA/TIA[2] standard committee has formed a task force which is currently investigating appropriate radio link protocols for mobile data services [38]. There are two types of Fax/Data services: *transparent* and *nontransparent*. In a transparent service the fax quality or data bit error rate is affected by the condition of the channel. Data throughput and fax transmit time in this case is constant. However, in a nontransparent service both data error rate and quality of fax remains the same under different channel conditions. But transmit delay for fax and throughput for data services are affected by the level of channel impairments. This group is planning to develop parformance metrics which can be used to quantify the degree of improvement gained by using RLPs for various mobile data services and applications [22].

This paper is organized as follows. In section II an overview of ARQ protocols is given. Section III provide an insight into the FEC schemes. Hybrid ARQ schemes are presented in section IV. Section V discusses the use of diversity reception for cellular channels. Throughput performance of RLPs are outlined in section VI. Finally, the conclusions are given in section VII.

II ARQ PROTOCOLS

ARQ schemes are widely used in data communications systems for error control because they are simple and provide high system reliability [13]. For example, they are used extensively in packet-switched data networks and computer communications networks where they are mostly combined with adaptive routing techniques. In such a network if a packet hit a bad or noisy link, then this packet can be repeated and most likely it will be routed on a good link. An error control strategy is characterized by its complexity, the undetected bit error probability, and the throughput. There are three main protocols used in ARQ schemes: stop-and-wait (SW), the go-back-N (GBN), and selective repeat (SR). The SW protocols are easy to implement which is their main advantage. However, these protocols are inherently inefficient due to the idle time spent waiting for the receiver to acknowledge each transmission. The GBN schemes are more efficient since codewords are transmitted continuously one after another. These protocols have been studied previously [3,4,13,15,16]. The results show that at low error rates their performance is satisfactory particularly when the round-trip delay is small. However, for situations where the error rates are high and/or round-trip delays are large (for example, in satellite communications) their performance may deteriorate very rapidly. The

[2] EIA/TIA stands for Electronics Industries Association/ Telecommunications Industry Association.

most efficient of the ARQ protocols are the SR schemes. The transmitter in an SR scheme repeats only those blocks which are in error. There is an overhead due to the retransmissions of the blocks which is traded for higher reliability. The degree of overhead will vary greatly depending on how noisy the channel is. This scheme can be implemented only with large buffers at the receiver which make them less attractive for most of the communications applications. In order to enhance protocol efficiency there are numerous modifications of these three basic schemes which have appeared in the technical literature [12 – 17].

Most of the work in the area of ARQ error control has been done using block codes [31 – 32]. However, convolutional codes have a number of features that make them attractive for use in systems with repeat request. A number of ARQ schemes with convolutional codes have been proposed. Sequential decoding of convolutional codes appears to be the most promising method of ARQ error control [16, 34 – 35]. Drukarev et al. [16] analyzed two sequential decoding algorithms for memoryless channels with noiseless feedback. It was shown that the memory requirement for these algorithms when ARQ error control is used are less stringent than those for FEC error control. FEC error control is discussed next.

III FORWARD ERROR CONTROL

Forward error control (FEC) strategies are used in data transmission systems to achieve higher throughputs. In an FEC error-control system, an error correcting code (block or convolutional) is used for correcting transmission errors. Since no retransmission is required in an FEC error-control system, no feedback channel is needed. The overhead with an FEC scheme is always fixed and the throughput of the system is constant and is equal to the rate of the code used by the system. Compare this with bit-oriented protocols like SDLC and HDLC [17] in which the size of the data blocks (frames) are variable , therefore, the overhead due to cyclic redundancy check (CRC) varies from less than one percent in lengthy frames, to as much as 10 percent with relatively short frames [18]. The main drawback of FEC scheme is that it is not easy to obtain high system reliability with a moderate code length. Furthermore, the error probability of FEC systems is higher than those of ARQ systems. This is mainly due to the error-detecting capabilities of a code which exceeds its error-correcting capabilities in ARQ systems [16]. This is true when block codes and convolutional codes with Viterbi decoding is used. However, by using sequential decoding it is possible to achieve both lower error probability and higher throughput in FEC systems. Because of these reasons ARQ schemes are often preferred to FEC schemes.

There are certain applications when there is no return channel, necessary for ARQ operations, for example in data storage systems, or when the time involved in retransmission adds an intolerable delay to error correction then FEC is the only viable solution. This is why FEC (in the form of Trellis coding [36]) has been included as an integral part of the CCITT's new dial-up high-speed modem specifications. Trellis coded modulation allows more data to be transmitted over a channel with limited bandwidth. The block error rate performance of a TCM modualtor used in a high speed modem is shown in Fig. 2 [19]. As it is seen from this figure the performance improvement of TCM is 3 dB more than with a QAM scheme. Unfortunately Trellis coding alone is not very effective against deep fades and interference bursts. It is mostly used for voice grade channels with Gaussian noise in which the overwhelming majority of errors usually affect only a single bit. It is also difficult to use Trellis for very high-speed applications ($\geq$ 20*Mbps*). This is mainly due to the difficulty of implementing decoders and demodulators at such speeds. An appropriate coding strategy for these applications is to use low-redundancy block codes with simpler modulations or concatenated with Trellis codes.

More recently, FEC has been used to improve the performance of mobile radio communications systems [21, 25, 27 – 30]. For example, TCM and multiple TCM (MTCM) has been used and demonstrated improved performance at data rates of practical interest [29]. In [30] a combined TCM and type-I hybrid ARQ (HARQ) protocol is used to enhance system performance over slowly fading channels. It is shown that the TCM-HARQ and MTCM-HARQ protocols provide excellent reliability performance at the expense of some reduction in throughput at nominal signal-to-noise ratio over such channels. One disadvantage of an FEC system is that decoding FEC is normally more complex than encoding and it is mostly often done by the Viterbi algorithm [11]. With convolutional codes if the decoder makes a mistake in the history of the data stream (due to either fading or burst interference) error will propagate making these codes less attractive for error control in wireless data communications. Besides, the decoder of convolutional codes must know the boundaries of each sub block. Figure 3 illustrates the features of two commonly used FEC codes in practice [18]. It is seen that user data typically suffers a longer delay in block coding than with convolutional schemes. The error detection and correction capabilities of these schemes are different. As the figure indicates block coding seems to be the best technique for handling long error bursts.

IV HYBRID ARQ ERROR CONTROL

The most important advantage of ARQ is that the quality of the received data is predictable; the greatest disadvantage is that throughput depends on the channel condition. However, in a system employing FEC data is delivered with a constant throughput and a quality depending on the noise characteristics of the channel. From the above statement it is obvious that one should use a combination of FEC and ARQ , known as *hybrid ARQ* , in order to take advantage of the fact that these two schemes behave in a complementary fashion. The combined scheme can fundamentally change system performance provided that they are matched to the channel conditions and user requirements. In other words, FEC increases the system throughput by reducing the frequency of retransmission and correcting the error patterns which occur frequently. However, when a less-frequent error pattern occurs and is detected, the receiver requests a retransmission rather than passing the unreliably decoded message to the user. This increases the system reliability. Therefore, by properly combining FEC and ARQ the overall system throughput will be higher than that of a system with ARQ alone and the reliability will be higher than that of a pure FEC system. Hybrid ARQ schemes can be classified into two categories, namely *type-I* and *type-II* schemes [33]. These schemes are discussed next.

Type 1 ARQ is the one commonly used in practice. It is best suited for communications systems in which a fairly constant level of noise and interference is anticipated on the channel. In a type-I hybrid ARQ the data and error correcting parity bits are encoded with an FEC code. The bits added by the error correction code are called error correction parity bits to distinguish them from the error detection parity bits [14]. In this system channel errors are corrected and FEC decoder outputs an estimate of data and the error detection parity bits. The error detection decoder accepts the data if it is error free. However, if an error is detected a request for retransmission is sent to the source by the ARQ protocol.

Type I FEC/ARQ has a major disadvantage when used to control errors in less noisy or perfect channels. That is when the channel bit error rate is low the transmission is smooth and no (or little) error correction is needed. As a result the extra parity-check bits included in each transmission is wasted and, therefore, reduces the throughput. One the other hand, when the channel is very noisy, the designed error correcting capability may become inadequate. Therefore, for a channel with a nonstationary bit error rate it is desirable to have an adaptive hybrid ARQ scheme. This has led to the design of type-II ARQ. The most common form of type-II ARQ is ARQ/FEC scheme in which the system behaves like a pure ARQ when the channel

is in good condition. The data in this scheme is sent without FEC and only error detection parity-bits is attached to it. If data is delivered with no error, then a new block of data (if any) is sent. If an error is detected, source will send an error correcting code along with the error detecting code, to recover the erroneous data. If these codes are received correctly the receiver will use them to correct errors and the process ends. If the receiver detects errors in these codes, it will still try to recover data and if succeeds the process is terminated. Otherwise, the data or code are retransmitted and the process begins again until the data is properly delivered.

V DIVERSITY TECHNIQUES

As mentioned earlier (fast) multipath fading severely degrades the performance of a mobile data transmission system. One of the most effective techniques to cope with this problem is the use of diversity reception. Various diversity techniques have been proposed for digital mobile radio systems. This includes *Branch Construction Methods, Combining Methods*. Branch diversity can be constructed using the following methods [39]:

- Space Diversity
- Angle Diversity
- Polarization Diversity
- Frequency Diversity
- Time Diversity

Among these techniques space diversity is the one which is widely used. This comprises a single transmitting antenna and a number of receiving antennas. By adjusting the spacing between receiving antennas it is possible to uncorrelate signals received from each branch. Similar techniques are applied to angle and polarization diversity. For frequency and time diversity the required frequency and time spacing are determined from the characteristics of the time-delay spread and the maximum Doppler frequency. An advantage of these techniques is that only one receiving antenna is required to implement them. Combining methods are classified into three different categories:

- Maximal-Ratio Combining
- Equal-Gain Combining
- Selection Method

Maximal-ratio combining achieves the best performance improvement compared with the other methods, but it is the most difficult one to implement. Selection method is more suitable for mobile radio application due to its simple implementation. One attractive way to implement this technique is by switching diversity branches periodically. Performance improvements achieved by diversity techniques has been extensively researched (refer to [39]). These techniques combined with ARQ and FEC error control are used to design radio links for digital mobile radio systems.

In the next section an overview of some of the most recent work on throughput performance for different radio link protocols are presented and their performance are compared.

VI THROUGHPUT PERFORMANCE

The throughput of an RLP scheme depends on several parameters [9]:

- block length of data and acknowledgement
- signal-to-noise-ratio of forward and reverse channels
- signalling rates
- FEC code rate
- ARQ strategy
- environment of mobile terminal
- velocity of mobile terminal
- type of diversity

The throughput performance of a plain (also called type-0) ARQ is heavily dependent on the channel conditions (see Fig. 4). As the Figure indicates the throughput of the system decreases drastically when the bit error rate of the channel approaches some moderate values (between 10^{-3} and 10^{-2}) The other major disadvantage of using type-0 ARQ is its vulnerability to periodic (but not bursty) interferences. For mobile communications where channel is subject to short bursts of interference ARQ type 0 proves to be an effective error control mechanism. A throughput comparison of hybrid ARQ is shown in Fig. 5. It is noticed that a type-I hybrid ARQ system has lower throughput than its corresponding ARQ system when the channel error rate is low. However, when the channel error rate is

high type-I hybrid ARQ has a higher throughput as compared to a pure ARQ system. This is mainly due to the error-correction capability which reduces the retransmission frequency.

There has been numerous publications on throughput performance of ARQ schemes combined with FEC and diversity which has appeared in the literature over the past few years. Some of these research results pertaining to throughput of RLPs are discussed next.

Jalali et al. [1] studied the performance of data protocols for their proposed in-building CT2Plus wireless system. Their result on performance comparison of different R-S codes, GBN ARQ for a Time Division Duplex (TDD) system is shown in Fig. 6. A buffer at the receiver is used to queue the user data during poor channel conditions, therefore, preventing data from being lost. A higher throughput is obtained by emptying the buffer via using fast code rates in this system. A frequency non-selective Rayleigh fading channel using Jake's model [37] was used to evaluate the performance. The simulations results show that a coding gain of 2.8 dB was achieved at 80% throughput by FEC of 2/3 rate using (63,48;3) and (63,44;3) R-S codes. This gain reduces to 2.0 dB when no antenna diversity is used. This indicates that the use of diversity improves the performance of a radio link. For a Frequency Division Duplex (FDD) system performance reported in [1] show similar results. This study recommends the use of type-I hybrid ARQ schemes with the Reed-Solomon code (63,44;3) and the GB7 ARQ protocol for the proposed CT2Plus system.

A similar study for fax transmission over a Rayleigh fading channel for Japanese Digital Cellular (JDC) system was performed by Ito et al. [2]. A buffer at the receiver is used to keep track of the sequence number of the incorrect received data frames. These frames are repeated until they are received with no error. Differentially coherent QPSK with post detection selection diversity reception was used in the simulations experiments. As shown in Figure 7 the throughput efficiency of the WORM-ARQ protocol is 4 times of that of Rej-based HDLC protocol. Benelli proposed a new GBN protocol and its performance for a mobile communications channel was studied [3]. In this protocol also a buffer at the receiver was proposed. The results reported in this paper show that by introducing a memory at the receiver the throughput of an ARQ may be kept to acceptable values even for poor channel conditions where FEC techniques become unreliable.

An application of frequency diversity (in the form frequency hoppin) combined with FEC is discussed in a paper by Parviz Yegani and C. McGillem. This paper pro-

poses a Frequency-Hopped, M-ary, Frequency-Shift-Keyed (FH-MFSK), Spread-Spectrum Communication System operating over the Factory Radio Channel [40]. The performance of the system for Rayleigh, Rician, and logNormal multipath fading for factory environments was investigated. The statistics of these channels, based on recent channel modeling studies [41], were used to evaluate the performance of the FH-MFSK system. Frequency hopping spread spectrum (FH-SS) which has a longer chip interval offers some advantages over DS-SS for mobile users in heavy multipath channels. There are cases where the rms delay spread of the channel is small and the signal components are not resolvable for reasonable chip durations. For example, in a typical factory environment with an rms delay of about 200 ns using FH-MFSK offers promise of reducing the serious fading that occurs in the channel. The FH-MFSK system block diagram is shown in Fig. 8. In the transmitter data modulation (MFSK) and frequency hopping modulation (FH) have been implemented in a two-step modulation process. MFSK modulation provides the multiple-access capability to the system while the FH modulation protects the system against multipath losses. The MFSK modulator produces an M-ary signal based on the simultaneous dictates of the PN code and the data. In this system FEC is introduced by a simple repeat code where each data symbol is transmitted N times, every time via different MFSK tones. Since every single tone is hopped independently, the different replica of each symbol passing through the channel experience different transmission losses. The results reported show that with the proposed system a much higher throughput can be obtained under the specified conditions than is possible with previously proposed systems.

VII CONCLUSIONS

This paper presented protocols for error-free data transmission over radio communications links in digital cellular systems. Efficient ARQ-based protocols were introduced to achieve high transmission throughput in multipath fading environments that these cellular channels encounter. A combination of forward error correction and diversity reception with ARQ scheme was incorporated into the link protocol so called ARQ/FEC/DIV RLPs. Various RLPs have been designed and used to support reliable data transmission across a radio link having a cellular frame architecture. It was shown that these protocols are efficient and can support standard data services including facsimile signal transmission and async data services in mobile radio environments. Finally, the throughput performance of ARQ/FEC/DIV protocols

as a function of fading parameters for different communication channels was investigated.

REFERENCES

[1] A. Jalali et al., "Performance of data protocols for in-building wireless systems," ICUPC '92, pp. 407-411, Dallas, 1992.

[2] S. Ito et al., "Facsimile signal transmission using WORM-ARQ in TDMA cellular system," Proc. IEEE VTC '92, pp. 247-250, 1992.

[3] G. Benelli, "A go-back-N protocol for mobile communications," IEEE Trans. Veh. Technol., vol. 40, no. 4, pp. 714-720, Nov. 1991.

[4] J. C. Chaung, "Comparison of two ARQ protocols in a Rayleigh fading channel," IEEE Trans. Veh. Technol., vol. 39, no. 4, pp. 368-373, Nov. 1990.

[5] L. F. Chang and P. T. Porter, "Data services in a TDMA portable radio system," Proc. IEEE Globecom '90, pp. 480-484, 1990.

[6] N. R. Sollenberger et al., "Architecture and implementation of an efficient and robust TDMA frame structure for digital portable communications," Proc. IEEE VTC '89, pp. 169-174, 1989.

[7] S. Ito et al., "Facsimile signal transmission in digital mobile radio," Proc. IEEE VTC '88, pp. 83-88, 1988.

[8] Y. Furuya et al., "High speed digital mobile facsimile with effective error protection," Proc. IEEE VTC '87, pp. 32-37, 1987.

[9] E. Lutz, "Simulation of FEC/ARQ data transmission using stored land mobile satellite channels," Proc. IEEE VTC '86, pp. 109-115, 1986.

[10] D.-L. Lu an J.-F. Chang, "Analysis od ARQ protocols via signal flow graphs," IEEE Trans. Commun., vol. COM-37, no. 3, pp. 245-251, March 1989.

[11] N. Seshadri and C-E. W. Sundberg, "Generalized Viterbi algorithm for error detection with convolutional codes," Proc. IEEE Globecom '89, pp. 1534-1537, 1989.

[12] P. T. Brady, "Performance evaluation of multireject, selective reject, and other protocol enhancements," IEEE Trans. Commun., vol. COM-35, no. 6, pp. 659-666, June 1987.

[13] S. Lin et al., "Automatic-repeat-request error-control schemes," IEEE Commun. Magazine, vo. 22, no. 12, pp. 5-17, Dec. 1984.

[14] R. A. Comroe and D. J. Costello, JR., "ARQ schemes for data transmissions in mobile radio systems," IEEE J. Selected Area on Commun., vol. SAC-2, no. 4, pp. 472-481, July 1984.

[15] E. R. Berlekamp et al., "The Applicxation of Error Control to Communications," IEEE Communications Magazine, Vol. 25, No. 4, pp. 143-152, april 1987.

[16] A. Drukarev and D. J. Costello, "Hybrid ARQ error control using sequential decoding," IEEE Trans. Inform. Theory. IT-29, no. 4, pp. 521-535, July 1983.
[17] W. Bux et al., "Balanced HDLC procedures: A performance analysis," IEEE Trans. Commun., vol. COM-28, no. 11, pp. 1889-1898, Nov. 1980.
[18] E. E. Mier "The ABC's of FEC", Data Communications Magazine, pp. 64-70, May 1984.
[19] John Payton and Shahid Qureshi, "Trellis encoding: What it is and how it affects data transmission," Data Communications Magazine, pp. 143-152, May 1985.
[20] S. B. Wicker, "High-Reliability Data Transfer Over the Land Mobile Radio Channel Using Interleaved Hybrid-ARQ Error Control," IEEE Trans. Veh. Technol., vol. 39, no. 1, pp. 48-55, Feb. 1990.
[21] ----, "Reed-Solomom Error Control Coding for Rayleigh Fading Channels with Feedback," IEEE Trans. Veh. Technol., vol. 41, no. 2, pp. 124-133, May 1992.
[22] A. D. Sacuta, "Performance metrics for radio link protocols supporting async data type I and fax type I services," An Intrim Report by TR 45.3.4, July 1992.
[23] Li Fung Chang and N. R. Sollenberg, "Performance of a TDMA Portable Radio System Using a Block Code for Burst Synchronization and Error Detection," Proc. IEEE Globecom '89, pp. 1371-1376, 1989.
[24] A. M. Bigloo, Q. Wang and V. K. Bhargava , "A Robust Rate-Adaptive Hybrid ARQ Scheme and Frequency Hopping for Multiple-Access Communications Systems," Proc. IEEE Globecom '92, pp. 889-893, 1992.
[25] S. Periaylwar , "Multiple Trellis Coded for the Mobile Radio Channel," Proc. IEEE Globecom '92, pp. 894-898, Orlando, FL, Dec. 1992.
[26] L. F. Chang and S. Ariyavisitakul, "Performance of Convolutional Codes with Interleaving in the Interference Limited Rayleigh fading Channels," Proc. IEEE VTC '91, pp. 812-816, May 1991.
[27] G. Femenias and R. Agusti , "Switched Diversity Trellis Coded 8-DPSK for Mobile radio Applicxations," Proc. IEEE VTC '90, pp. 476-481, May 1990.
[28] N. Seshadri and C.-E. W. Sunberg, "Multi-level Block Coded Modulations for the Rayleigh Fading Channel," Proc. IEEE Globecom '91, pp. 47-50, Dec. 1991.
[29] D. Divsalar and M. K. Simon, "The Design of Trellis Coded MPSK for Fading channels: Set partitioning for Optimum Code Design," IEEE Trans. Commun., vol. COM-36, pp. 1013-1021, Sept. 1988.
[30] L. K. Rasmussen and S. B. Wicker, "A Performance Analysis of Trellis Coded Hybrid-ARQ Protocols in a Fading Environment," Proc. IEEE Globecom '92, pp. 899-904, Orlando, FL, Dec. 1992.
[31] R. J. Benice and A. H. Frey, "Comparing of error control techniques," IEEE Trans. Commun. Technol., vol. COM-12, pp. 146-154, 1964.
[32] ----, "An analysis of retransmission systems ," IEEE Trans. Commun. Technol., vol. COM-12, pp. 135-145, 1964.

[33] S. Lin and D. Costello, Jr., Error Control Coding: Fundamentals and Applications. Englewood Cliffs, NJ: Prentice-Hall, 1983.
[34] A. Drukarev, "Error control using sequential decoding with repeat request," Ph.D. dissertation , Illinois Institute of Technology, Chicago, IL, May 1981.
[35] A. Drukarev and D. J. Costello, Jr., "A comparison of blocks and convolutional codes in ARQ error control schemes," IEEE Trans. Commun., vol. COM-30, pp. 2449-2455, Nov. 1982.
[36] G. Ungerboeck, "Channel Coding with Multilevel Phase Signals," IEEE Inform. Theory, vol. 28, Jan. 1982, pp. 55-67.
[37] W. C. Jakes, Microwave Mobile Communications, Wiley, 1974.
[38] Draft Standard Document, TR45.3 Committee, Cellular Service Description, Async Data / Fax services.
[39] Kamilo Feher, Advanced Digital Communications, Prentice-Hall, 1987.
[40] Parviz Yegani and Clare D. McGillem, "FH-MFSK Multiple Access Communications System Performance in The Factory Environments," IEEE Trans. Veh. Technol., to appear.
[41] Parviz Yegani and Clare D. McGillem, IEEE Trans. Commun., vol. 39, No. 10, Oct. 1991, pp. 1445-1454.

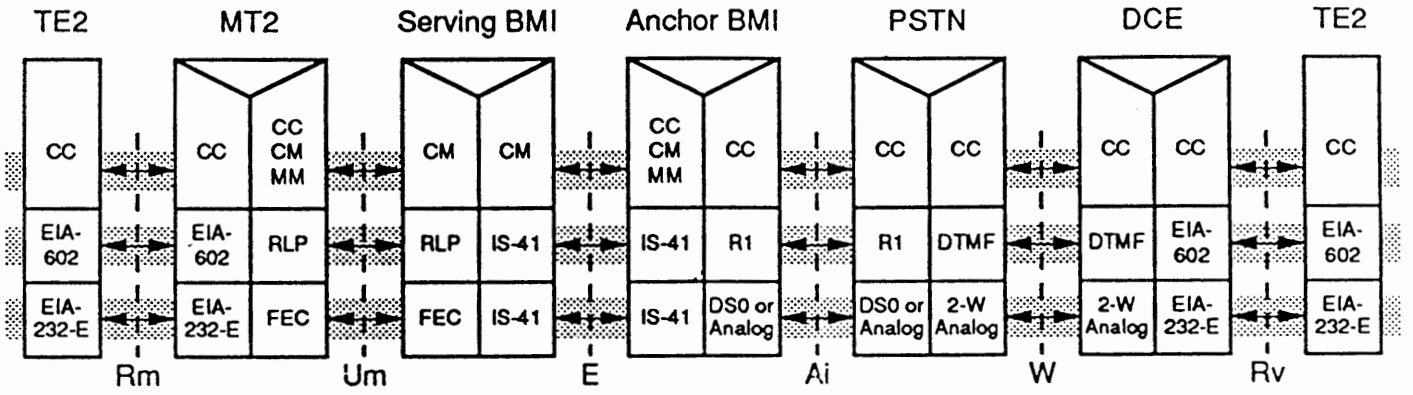


Figure 1. A reference model for a cellular network.

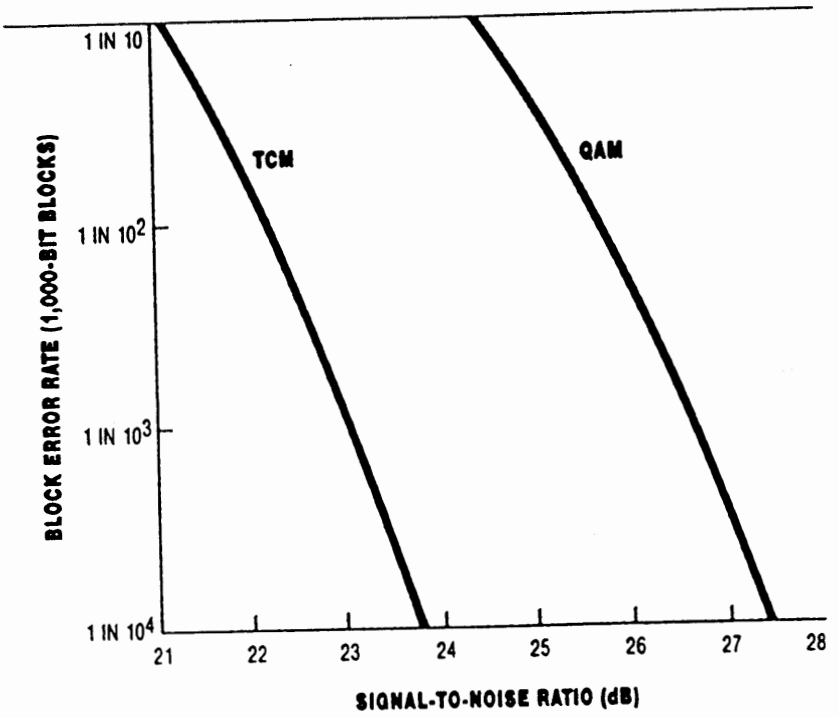


Figure 2. BER performance of TCM vs QAM.

Type	Maximum Data Rates Supported	Typical Code Rates	Typical Delays	Length of Error Bursts Corrected without Inter-leaving
Block (e.g. Reed-Solomon)	> 100 Mbps	$\frac{7}{8}$, $\frac{15}{16}$	2000 + bit durations	100 bits
Convolutional (e.g. Viterbi, Sequential)	Typically less than 50 Mbps	$\frac{1}{2}$, $\frac{3}{4}$, $\frac{7}{8}$	30 – 1000 bit durations	Typically less than 20 bits

Figure 3. Two commonly used FEC Schemes.

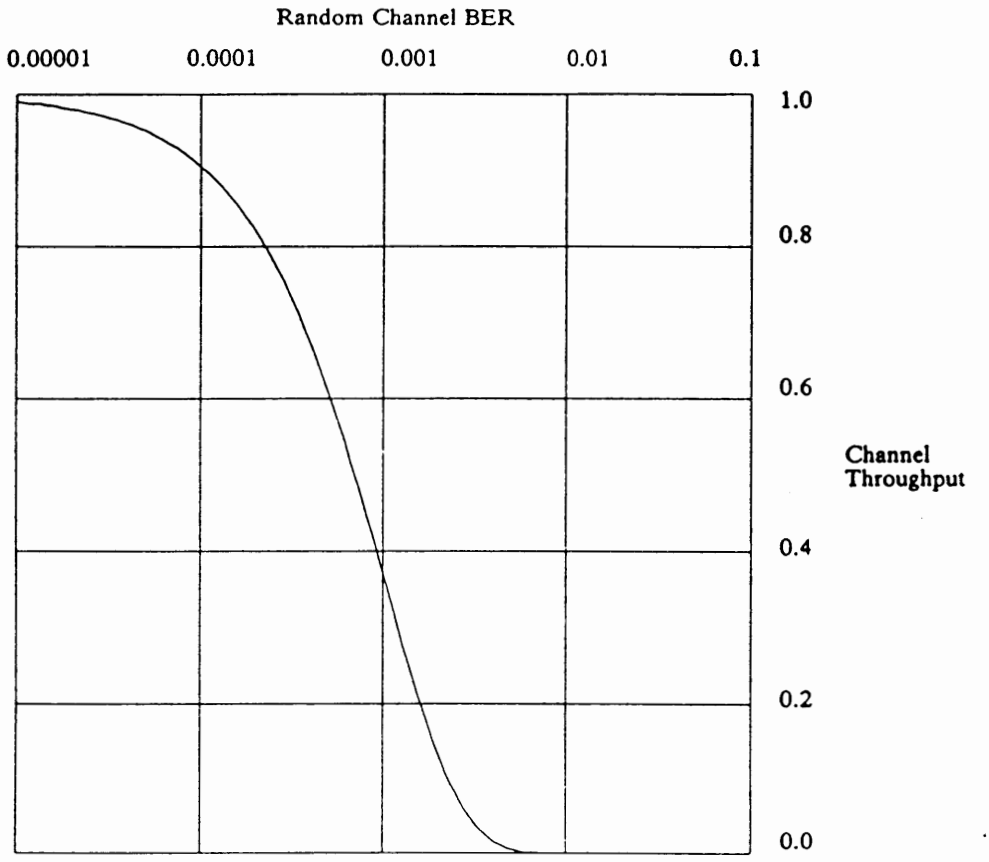


Figure 4. ARQ Throughput for 1000-Bit Blocks.

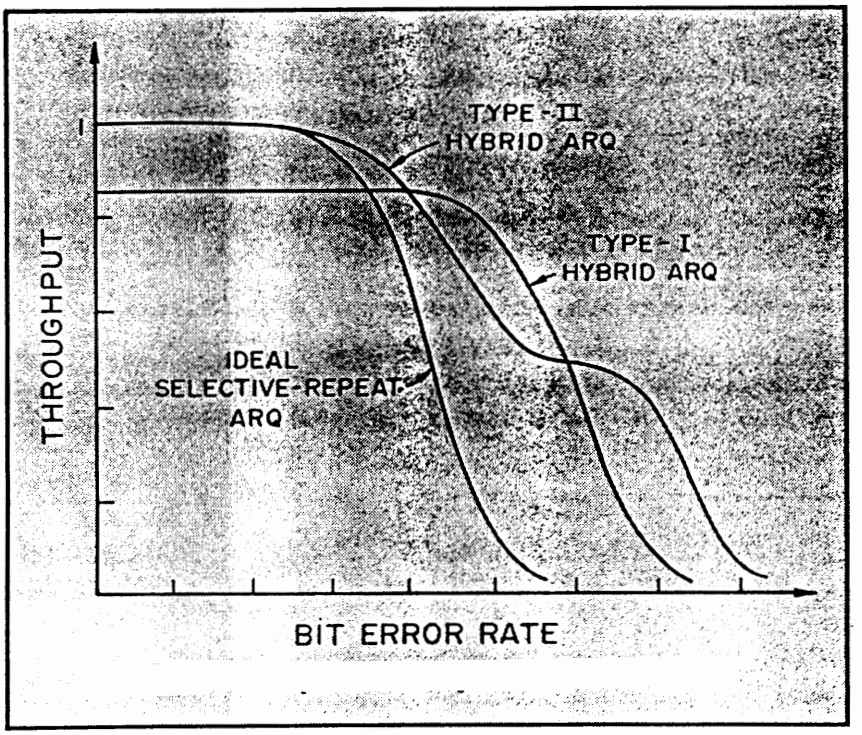


Figure 5. Comparison of hybrid ARQ schemes.

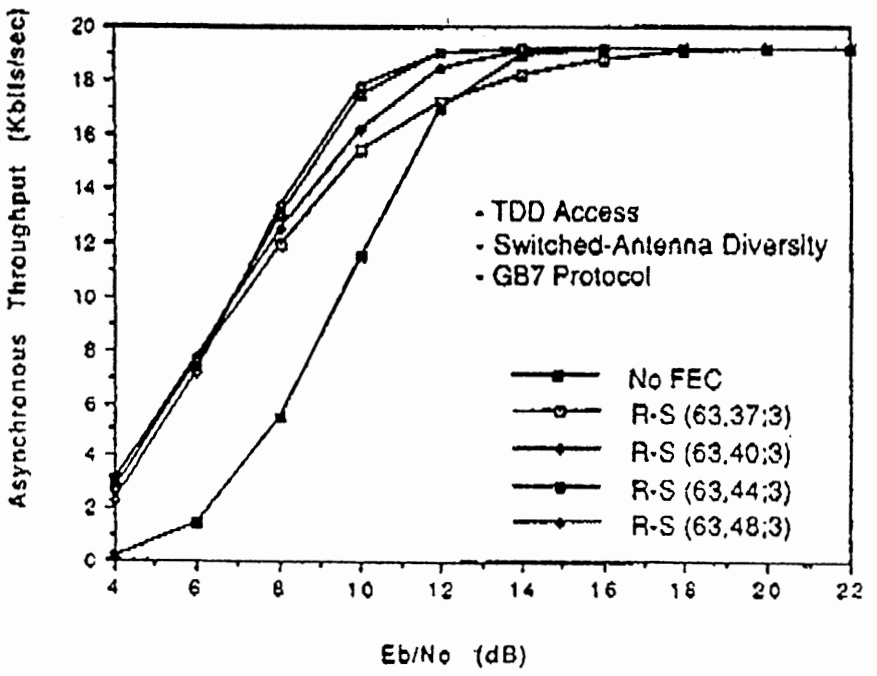
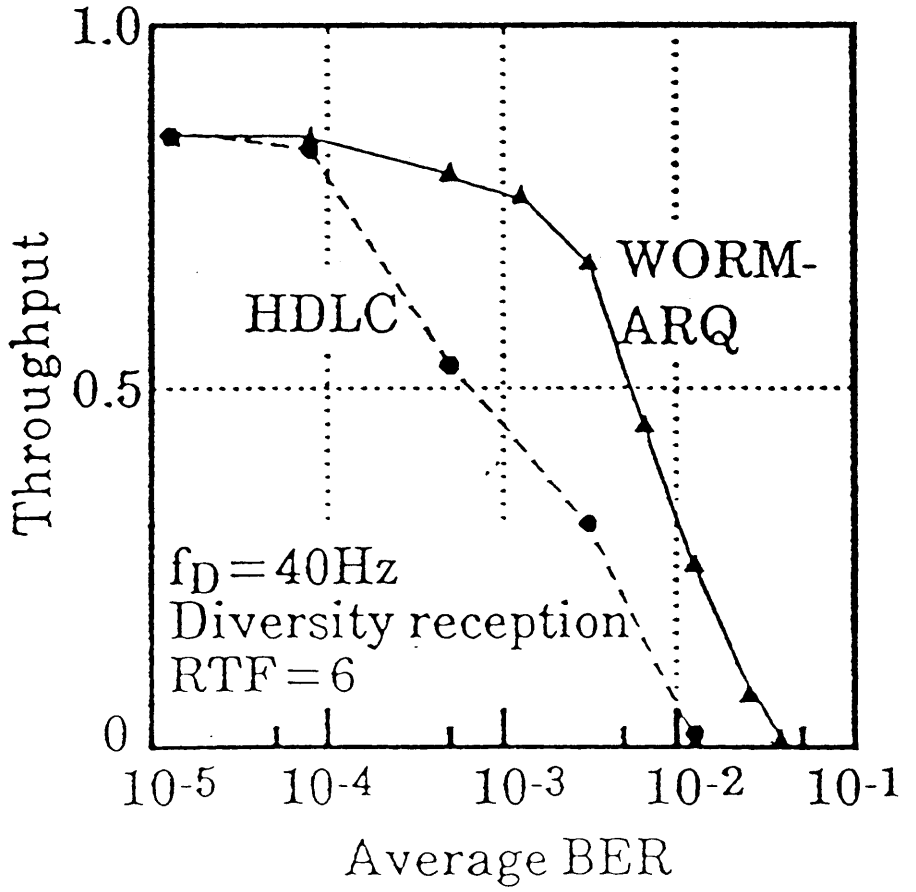


Figure 6. Comparison of different ARQ/FEC/DIV protocols.



f_D = Doppler Frequency

RTF = the number of frames transmitted during the round-trip delay

Figure 7. Throughput Comparison between WORM-ARQ and HDLC protocols.

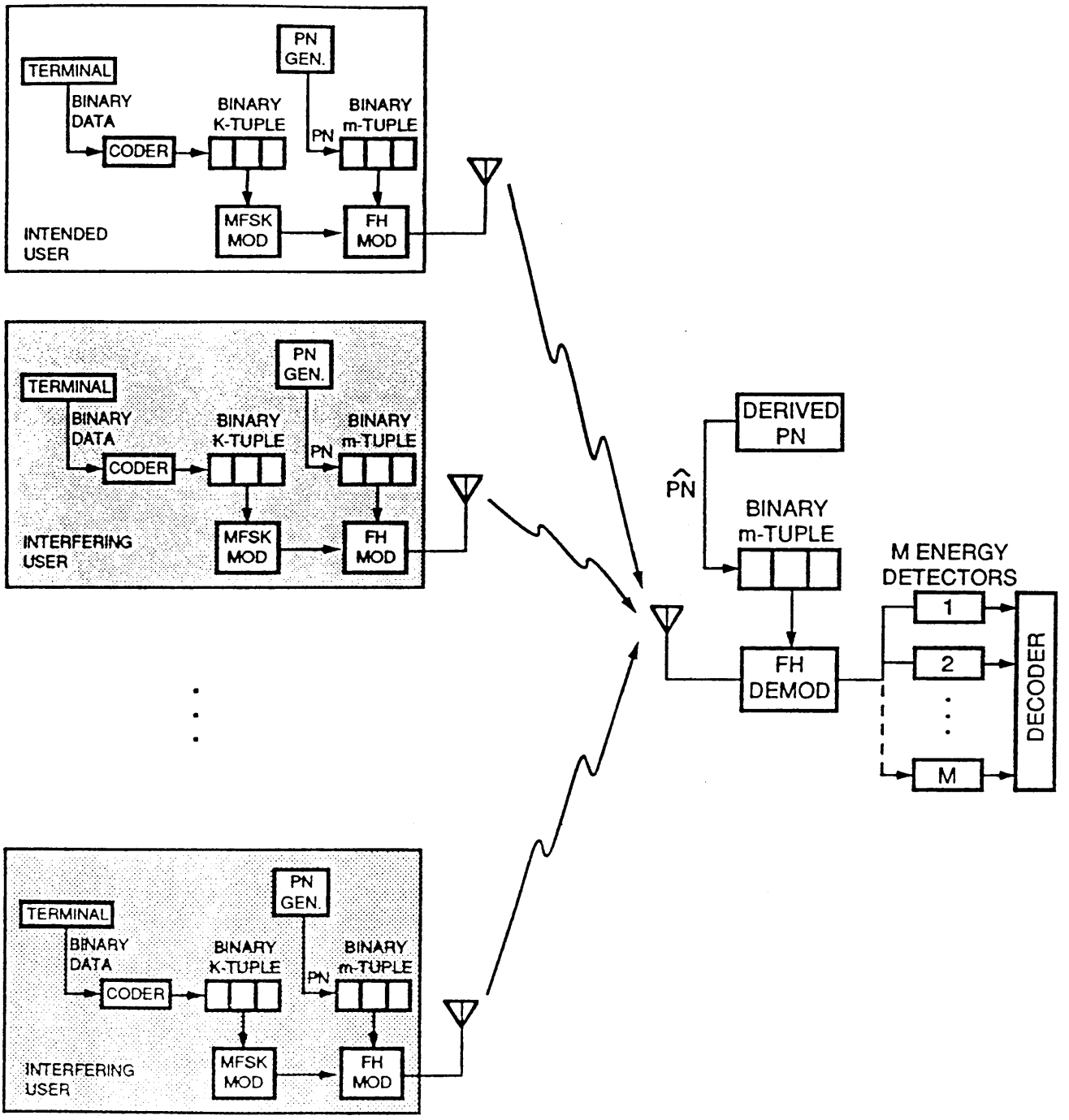


Figure 8. Block Diagram of the FH-MFSK system.

GaAs MESFET DIRECT QUADRATURE MODULATOR INTEGRATED CIRCUIT FOR WIRELESS COMMUNICATION SYSTEMS

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Abstract

An RF quadrature modulator integrated circuit utilizing GaAs MESFET process technology has been developed for wireless communication systems operating between 700 and 1000 MHz. The IC is packaged in a plastic SOIC package which makes it suitable for low cost, high volume consumer oriented products. The device consists of two input differential amplifiers, two limiting input LO amplifiers, two double balanced mixers, a hybrid phase splitter, a combining amplifier and an output RF amplifier which will drive a 50 Ω load at -3 dBm (typical). The device also contains a phase adjust pin to allow for optimum phase balance between the in-phase (I) and quadrature (Q) channels. The device is powered by a single +5 V supply. This modulator can be used for any type of vector based modulation.

Introduction

Current communication architectures that have been proposed and implemented for wireless communication systems utilize vector based modulation schemes. Inherent in these architectures are RF transmitter functions that require the baseband vector to be modulated onto an RF carrier. It is the conversion of this baseband vector to an RF transmit frequency via a GaAs MESFET integrated circuit that this device and paper addresses.

The baseband vector is a complex signal comprising an in-phase and quadrature component. These components are always 90° out of phase with respect to each other. It is the amplitude of each component which uniquely identifies each transmit vector. Given the fact that the phase of the transmit vector is changing with respect to time as information is sent, and the fact that the LO source has singular phase, it is necessary to modulate each component

independent of the other and then add the two signals to obtain the transmit vector at an upconverted RF frequency. In the process of mixing, it is necessary to first phase shift the quadrature channel LO by 90° so that there is phase matching with respect to the quadrature component. This function is implemented via a hybrid phase splitter and is included on the chip. No external components are necessary to implement this function. It is also desirable to reduce the amplitude of the carrier and the undesired image which is obtained in the process of upconverting. This too is accommodated within the device by virtue of its basic architecture. GaAs MESFET process technology is used to obtain a relatively high level of gain and to implement the hybrid phase splitter with a high degree of accuracy.

Device Architecture

The architecture of the device is shown in figure #1.

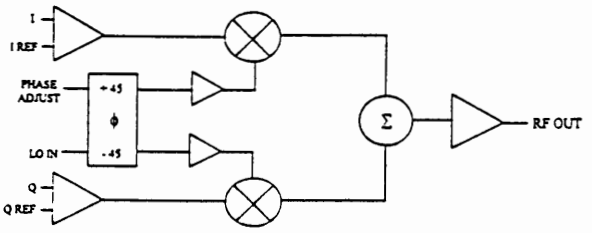

Figure # 1: Basic Quadrature Modulator Architecture

I, Q & LO Input Considerations and Resultant Performance

The I and Q inputs are differential inputs. They are loaded with approximately 3000 Ω. Typically these inputs are produced by baseband D/A converters and are DC coupled. They can be AC coupled as well, however. Because the device is a single power supply device, an artificial ground or reference has to be connected to the reference inputs. Since the input amplifiers are differential, their output is the difference between the two inputs. The driving source usually provides the reference voltage which is 2.5 V DC for this device. The input signal must be equal to the reference input for each amplifier (I=Q=2.5 V DC) for the mixer to be in its balanced state (no output) whereas an output is obtained for any non-zero sinusoidal inputs on either the I or Q channel. The maximum input condition for the I and Q channel is +5 V (2.5 V DC plus 2.5 V AC zero to peak).

DC offsets in the I and Q channel inputs can cause reduced carrier suppression. The offsets may originate in the digital signal source, D/A converters, the interconnects, or in the device itself. The design of the system must account for these errors when a high degree of carrier suppression is required. In testing, we have found that unadjusted I and Q inputs will provide about 25 dB of carrier suppression. Induced I and Q DC offsets on the order of 10 to 20 mV have produced carrier suppression levels of 40 dB.

The LO input is a low VSWR match to a 50 Ω line provided that an external terminating resistor of about 56 Ω is used. The DC component of the LO signal must be near zero volts so a coupling capacitor should be used if any DC is present in the LO driver. The devices LO limiting amplifiers normalize the LO signal being applied to the mixers. In order to maintain good normalization, the input signal should be at least -6 dBm. Optimal performance

will be achieved at a level of around 0 dBm. No more than +6 dBm of LO input power should be used. The RF output vs. LO drive level is displayed in figure #2.

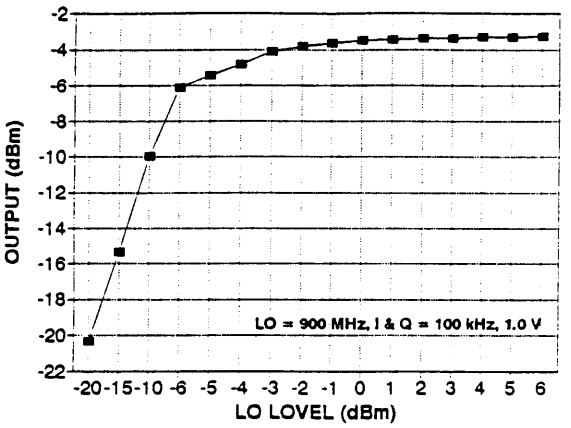

Figure #2: RF Output vs. LO Level

The device is optimized for use at frequencies of 700 MHz to 1 GHz. The unit may be used up to 1.2 GHz provided that a lower output RF amplitude can be tolerated. The curve of figure #3 shows the amplitude response of the unit vs. frequency. At frequencies below 700 MHz , the output RF amplitude remains constant but the internal phase and amplitude tracking errors between the I and Q channels become progressively worse. The curves of figure #4 and #5 show amplitude and phase error, respectively, vs. LO frequency.

Symmetry

Quadrature operation of the device requires that the phase balance between the I and Q channels be optimally 90°. By viewing figure #5, one can see that the phase error of the device is a function of LO frequency. This error can be compensated by using the "phase adjust" function of the device. This function has the net effect of moving the curve of figure #5 to the right horizontally. This movement causes the zero phase error point to cross at different frequencies. This is done by adding a DC voltage on the phase adjust pin. Typically, for no phase correction, the pin is left floating and is not used. To compensate for phase error, one should connect a 10 kΩ potentiometer to the pin and tie it to the +5 V source. The value of resistance and thus voltage drop can be varied until the optimum sideband suppression is obtained and thus phase matching is achieved. Once this level is obtained a fixed resistor can be used to avoid tuning requirements. Remember that phase error is also a function of frequency and does vary on a device by device basis so some level of phase error will have to be tolerated. Typically a level of 25 dB sideband suppression can be achieved at 900 MHz. A level of 40 dB can be achieved by using the phase adjust mechanism.

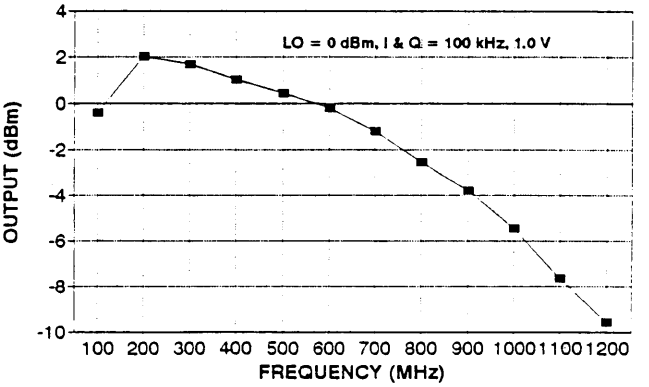

Figure # 3: RF Output vs. Frequency

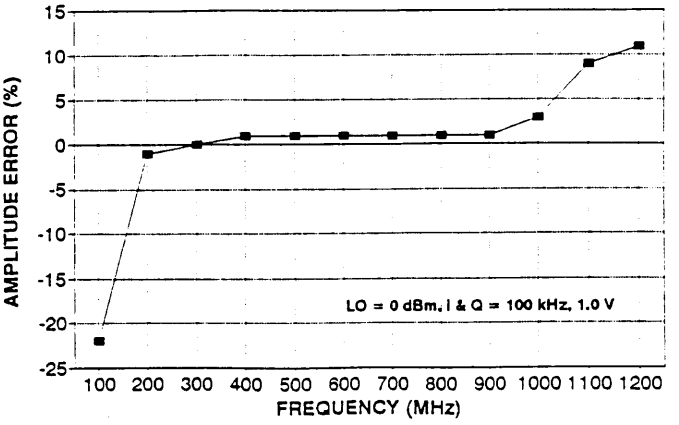

Figure #4: Amplitude Error vs. Freq.

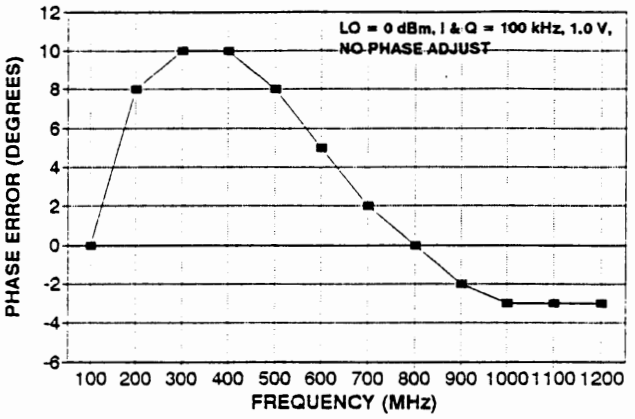

Figure #5: Phase Error vs. Frequency

RF Output

The output spectrum of the device is rich in harmonics, particularly the third harmonic. Thus, a low pass or band pass harmonic filter is generally used between the devices output and the final power amplifier stage (or antenna when the output level is sufficient). A plot of SSB output level vs. peak I & Q amplitude is shown in figure #6. This operation is all within the linear range. As you can see a peak output of +2.5 dBm is attainable. The output IM3 level varies with respect to SSB output level, but a level of -40 dB suppression is typical for this unit at -3 dBm RF output under two tone conditions at 900 MHz.

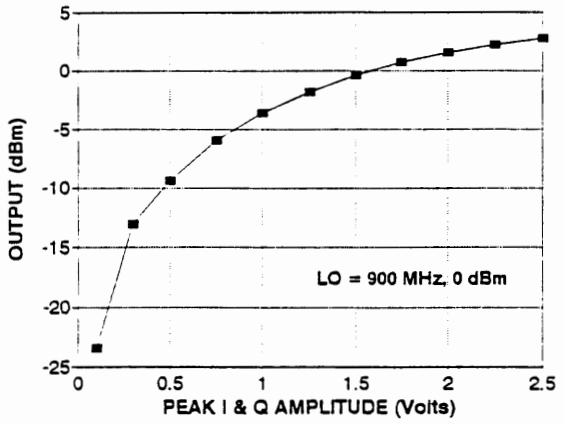

Figure #6: SSB Output vs. Peak Input

Power Management

The device typically consumes 28 mA of supply current, 35 mA maximum. This is satisfactory for the power budgets that have been established for most wireless applications. Given the fact that power should be conserved when possible, a power down function has been incorporated in the device. This is a pin that should be tied within 1 V of ground to be inactive and all the way to Vdd to be active. This pin is typically driven with an unloaded CMOS gate. When the power down function is enabled, the device typically consumes approximately 200 μA. This function is particularly useful for TDMA type applications where the transmitter duty cycle is less than 50%.

Connections

The device has been designed to be as integrated as possible. However, a minimal amount of external componentry is required. The LO input and RF output are UHF frequencies and need to be connected on the PCB with microstrip lines. Also, as much power supply bypassing as feasible is provided on the chip, however, it is preferable to have some bypassing externally. This is accomplished via a single 0.1 μF capacitor from Vdd to ground on the supply input pins.

Conclusion

An RF quadrature modulator has been successfully implemented in a GaAs MESFET process technology and packaged in a low cost plastic package.

This device operates from 700 MHz to 1000 MHz and is applicable to most wireless applications within that frequency range. The device will produce an output level of +2 dBm maximum and can maintain a high degree of phase accuracy. Sideband suppression, carrier suppression and IM3 performance (-40 dB or better with adjustments) has been shown to be excellent and well within the bounds of most system requirements. Further, a minimum amount of peripheral components is necessary to make this device operate and overall performance is significantly higher than an equivalent architecture implemented in bipolar silicon.

Acknowledgments

The author would like to thank Bill Pratt, the principal designer of this device, and Kellie Chong, whose persistence in test and evaluation made the contents of this paper possible.

SYSTEM ASPECTS & RF COMPONENT DESIGN FOR EUROPEAN MOBILE COMMUNICATION SYSTEMS

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ABSTRACT : This article offers a brief outline of radio interface specifications and functioning of various mobile communication systems recently standardised or still in process of standardisation in Europe. After a short introduction concerning the deployment of these systems, technical analysis based on typical values of their radio parameters is presented. Specifications of RF components and/or sub-assemblies for both Rx (receiver) and Tx (transmitter) chains are discussed. Only active circuits elements for both mobile subscriber (MS) and cell site (BS) equipments are considered. Comparison between radio parameters for various systems rather than detailed design calculations are stressed upon. Paragraph II gives details of frame structure for TDMA systems and Para III describes how specific system features are to be considered to determine the RF specifications. Details of system features and Rx and Tx parameters are given in Tables I, II and III respectively.

I.INTRODUCTION :

The field of mobile communications has been attracting lot of attention during last few years. In Europe, a variety of wireless systems have already been standardised by European Telecommunication Standards Institute (ETSI). Some others are approaching final standardisation. A relatively big set of radio communication systems, each suitable for a particular service application, are known to exist. Some of these are :

- **GSM :** Pan-European Cellular (Mobile) Communication System earlier known as "Group Special Mobile" is now called the - Global System for Mobile Communications. A more accurate name is GSM-900.

- **DCS-1800 :** It is the Digital Cellular Communication System operating at 1800 MHz. Adopted by the U.K Personal Communication Networks (PCN) operators, this is derived from GSM-900 with adaption of radio parameters to suit micro-cellular systems. At times it is simply called PCN.

- **DECT** : Digital European Cordless Telecommunication System has been standardised by ETSI for wireless office communications.

- **TFTS** : Terrestrial flight Telephone System is to be applied for ground to air communications for commercial telecommunications services in civilian aircrafts.

- **TETRA** : Trans European Trunked Radio System is in the process of standardisation by ETSI for Special/Private Mobile Radio (SMR/PMR) applications.

- **DSRR** : Digital Short Range Radio system has been standardised for voice and data transmission applications using low power radio transmission.

All these systems are suitable for full duplex digitised speech transmission and special provisions have been made in TETRA & DSRR for simplex and semi-duplex operation. Various services based on digital data transmission have also been designed in each of these systems. GSM-900, DCS-1800 and TFTS are deployable for multi-operator, wide area public networks. DECT is used mainly for special (private) network applications.

Two more systems namely European Radio Message Service (ERMES) and CT2 (second generation Cordless Telephone) have been standardised and widely deployed during the previous years. However these systems are not dicussed any further in this paper.

Different Technical Committees or Radio Equipment and Systems groups in ETSI carry out this standardisation work. Radio Interfaces of standardised systems are detailed in series 05 of ETSI recommendations. Recs. 05.04 and 05.05 for each specific system are of major importance for Rx and Tx designs. Parameter values in Table I, Table II and Table III, are based on information from the recommendations.

II. TDMA FRAME AND SLOT STRUCTURES

GSM-900 and DCS-1800

1 bit = 48/13 = 3.69 μs
1 time slot = 156.25 bits = 577 ms (including interburst guard time of 8.25 bits)
1 frame = 8 time slots
26 multiframe = 26 frames
51 multiframe = 51 frames

. Each active MS transmits traffic information duting one TS per frame in normal functioning.
. Traffic and associated signalling are transmitted modulo 26 -multiframe and 51 multiframe is used for dedicated and common channel signalling.
. Shorter bursts for random access are also used.

DECT :

1 bit = 1/1.152 μs
1 time slot = 480 bits (this includes an inter burst guard time equivelent to 60 bits)
1 frame = (12+12) time slots = 10 ms
1 multiframe = 16 frames

. A normal voice only MS transmits once every frame.
. Signalling information is carried in the header portion of each burst, both in forward and reverse links.
. Shorter bursts are also defined.

TFTS:

1 bit = 1/44.2 ms.
1 time slot = 208 bits = 4.706 ms.
1 frame = 17 time slots = 80 ms
1 Superframe = 20 frames = 1.6 ms.

. A total guard time of 5 bits is included in the time slot duration. An equivalent of 2.5 bits is provided at each end of the burst.
. Each active voice channel occupies four out of 17 time slots in a frame.
. Shorter time slots have been defined for specific functions.

TETRA :

1 bit = 1/36 ms
1 time slot = 510 bits = 14.167 ms
1 frame = 4 time slots = 56.66 ms
1 multiframe = 18 frames = 1.02 ms
1 hyperframe = 12 multiframes = 12.24 ms.

. Interslot guard time is included in the above time slot duration. Its exact position in the burst is to be determined.
. Shorter time slots (or sub slots) are also defined.
. Numbering of time slots on reverse link is derived from forward link numbering with a shift.

III.1 TIME DIVISION MULTIPLE ACCESS (TDMA), CONSTANT ENVELOPE MODULATION and POWER AMPLIFIER DESIGN

Table I shows that all the considered systems, except DSRR, use TDMA. Also most of these (four out of six) use constant envelope modulation of GMSK type. The two remaining systems namely TFTS and TETRA intend to use pi/4 shifted differential quadrature phase shift keying (pi/4 - DQPSK). This is designed to minimize the modulated signal form factor.

Such modulations (GSMK and pi/4 - DQSPK) facilitate the use of linearised power amplifiers for Tx signal amplification : Intermodulation noise and spectral distortion specifications for GSM, DCS and TFTS being very stringent , the power amplifiers need to be operated with a certain (sometimes high) back-off. This back-off is minimised if signal form factor is reduced.

However, Transmitter attack and Tx release time for GSM/DCS are rather fast and not so easily achievable without use of good linear amplifiers.

Moreover, once the initial switching transient at Tx output is absorbed, the power level for GSM/DCS Tx has to stay within +/- 1 dB of the normal transmit power. Similar constraints for DECT, DSRR are also applicable. The respective values are listed in Table II.

III.2 TRANSMITTED CARRIER STABILITY, POWER IN ADJACENT CHANNELS & PILOT SOURCE SELECTION.

Most of the digital radio systems require that both timing signals and carrier frequencies be derived from one common pilot source. Its stability has to be calculated for worst case condition which can be different for different systems.

A typical DECT network shall use one carrier per base station where as GSM, DCS and TFTS will require multi-carrier BS's. In such a case accurate receive-transmit timing for different carriers (rather than the carrier frequency stability itself) imposes the worst case requirement on pilot source.

In this context, it is really interesting to analyse the influence of doppler shift experienced by the radio signal in different systems. In DECT/DSRR indoor networks the relative Rx/Tx velocity is rather small (typically 3 Km/h). Whereas in TFTS high relative Rx/Tx velocities can induce a doppler shift of a few KHz on radio signal. Such a carrier shift coupled with any initial carrier inacurracy could mean that the signal energy in the adjacent channel is increased much beyond acceptable limits. Signals in GSM-900 and DCS-1800 networks shall experience doppler shifts in range of a few hundred hertz in worst case.

Table II presents the figures on Tx output carrier stability of the BS. Generally an MS adjusts the frequency of its transmitted carrier in synchronisation with the received BS carrier. For example, a DECT-BS carrier can stay within +/- 50 Khz of an absolute reference and a MS has to stay within +/- 50 KHz w.r.t the recovered carrier or w.r.t an absolute reference.

Since TETRA should permit a co-ordinated use of available radio channels between different systems in trunked mode, good carrier stability and low adjacent channel power (-60 dBc) are prime requirements. Also, disturbance to existing analog PMR/SMR networks have to be kept to a minimum.

Some other considerations for pilot source accuracy are detailed in coming paragraphs.

III.3 FREQUENCY HOPPING, DUPLEX METHOD and SPEED of Rx-Tx SYNTHESIZER

GSM/DCS implement slow frequency hopping (SFH) to improve radio link performance.In such a case, each MS should have the capacity to operate (Rx & Tx) on a different radio channel every TDMA frame. Moreover MS reception and Transmission use two frequencies 45 MHz apart.

In addition the MS is supposed to perform measurements on set-up channels of surrounding BS per TDMA frame. Hence its synthesizer has to be tuned to at least three different frequencies per frame of 4.6 ms. Synthesizer settling speeds of about 500 μs are usually considered. The frequency accuracy to which the synthesizer has to settle is very stringent in view of a total 50 Hz carrier frequency error on the transmitted burst. Total range of frequencies over which a synthesizer may have to place its 200 KHz mode channel is 70 Mhz for GSM-900 and about 200 Mhz for DCS 1800.

A typical DECT network would employ only one radio channel per BS. Also Rx and Tx during a call are performed on one same frequency in TDD mode. However for radio control functions both MS and BS may be required to switch operation to other radio channels for interference calculations. Any receiver trying to perform its normal reception and interference calculation in two consecutive time slots may require to shift frequency of its local oscillator in less than the 60 bit guard period provided after each time slot. However, the DECT standard does accommodate much higher carrier frequency error than the GSM or DCS. Ref Table II and Table III.

III.4 Tx-Rx SYNCHRONISATION, INTER-SLOT GAURD PERIOD and RECEIVER SETTLING TIME

As seen from Table I, DSRR & DECT would experience small Tx-Rx separation in comparison to the one for GSM-900, TFTS and TETRA. DCS-1800 falls in some intermediate range. Moreover, greater the Tx-Rx separation greater is the multipath time dispersion in a Rayleigh channel like for GSM 900/DCS 1800 and TETRA. Signal in TFTS shall be affected by proportionately smaller multipath time dispersion as TFTS channel behaves similar to a land mobile communication channel only during aircraft take off and landing.

MS generally is synchronised to BS timing in GSM / DCS, TFTS & TETRA. Once the MS burst transmission is time aligned to compensate for the radio propagation delay due to large BS-MS separation, MS maintains its timing within +/- 1 bit with respect to BS timing. By taking into account different parameters like Tx attack time, MS-BS timing mis-alignment, multipath timing dispersion on the received signal it can be concluded that only a small part of the total interburst guard period is available for receiver settling (e.g less than 10 μs for GSM 900).

Moreover, a BS receiver for any of the GSM, DCS, TETRA or TFTS may receive two consecutive signal bursts with wide amplitude differences. Such a situation is more probable in a system implementing slow frequency hopping without a perfect MS power control in a GSM/DCS network. Total received signal dynamic range of about 90dB has to be considered for an Rx design based on the worst case values.

DECT networks would mostly operate without any MS-BS time alignment. An interburst guard period of about 50 μs is useful to accomodate all the timing inaccuracies and the small cell time delay dispersion too.

III.5 DISCONTINUOUS TRANSMISSION (DTx), Tx POWER CONTROL and SYNTHESIZER FREQUENCY PULLING :

In call, dynamic transmit power control is applied in large cell systems like GSM / DCS, TFTS and TETRA. Transmitting just the required amount of power helps to reduce radio interference and the MS can save on battery consumption. In addition possibility of speech interpolation based discontinuous transmission is also available in most of the systems. The BS Tx must be designed to ensure the required carrier frequency stability (< 100 Hz for DCS) for all power levels. This carrier stability might be slightly affected by the variation in power supply current.

Burst to burst Tx power (over 30 dB dynamic range) and frequency changes have to be considered for the design of frequency hopping transmitters for GSM & DCS. TETRA & TFTS have to accomodate even larger power variations and DECT does not implement dynamic power control. A typical GSM/DCS MS has to implement rather slow (Tx active during one burst per frame) power variations i.e +/- 2 dB from one frame to next.

III.6 Tx SPURIOUS EMISSIONS & Rx SPURIOUS REJECTION FOR CO-SITING OF DIFFERENT SYSTEMS :

Three out of the six systems discussed above operate in the frequency range 1670 to 1900 MHz. A separation (in operating frequency) between co-sited networks of these systems has to be respected to avoid mutual interference.This is determined on the basis of interference calculations.

Important Tx prameters for these calculations are :
- transmitted power at frequencies offset from the wanted signal.
- intermodulation products created by a multi channel BS (especially in case of GSM/DCS and TFTS) after the transmitter output.

N.B suitable margins to account for the multiplicity of channels on a given BS site have to be considered on top of single Tx specs. of spurious emissions and intermodulation product generation.

Important Rx parameters for those calculations are :
- Rx sensitivity with respect to thermal noise, co-channel interference adjacent channel interference and in band and out of band signals.
- Rx desensitisation performance. The receiver ability to detect a weak wanted signal in presence of a very strong unwanted signal (offset in frequency w.r.t wanted channel) is considered here.

Receiver selectivity in terms of image frequency rejection and local oscillator noise directly influence this performance. Reverse mixing due to local oscillator re-injection has to be controlled too. A typical GSM-900 receiver may need -150 dBc/Hz of phase noise at 600 KHz from the wanted carrier frequency.

IV. CONCLUSION: The above system description and analysis shows that inter-dependence between various apparently different looking parameters. A comparison between parameters values for GSM-900 and DECT shows that components for wide area applications in public mobile networks are required to meet much more stringent specifications than those used in private networks for on-site and indoor applications. Cositing and coexistence of various systems can impose specific requirements for RF equipment design.

V. REFERENCES: 1. ETSI-SMG Recs. of Series 05. GSM and DCS Radio Interface.

2. ETSI-RES3. DECT Common Interface Part 2. Physical Layer.

3. ETSI-RES7. Digital Short Range Radio (DSRR). Interim Standard.

4. E. Fernandez et el. Le TFTS Alcatel 9810. Un Système European de Communication Sol-Air. Commutation et Transmission.

TABLE I SYSTEM CHARACTERISTICS

	GSM 900	DCS 1800	DECT	TFTS	TETRA	DSRR
FREQUENCY BAND in MHz REVERSE LINK (MS Tx) FORWARD LINK (BS Tx)	 865 - 890 910 - 935	 1710 - 1785 1805 - 1880	Both MS & BS 1881.792 to 1897.344	 1800 - 1805 1670 - 1675	 450 Mhz Range	 933 - 935 888 - 890 See Note 1
MULTIPLE ACCESS SCHEME	TDMA	TDMA	TDMA	TDMA	TDMA	FDMA
FRAME TO FRAME FREQ. HOP.	YES	YES	POSSIBLE	?	POSSIBLE	NO
DUPLEXING TECHNIQUE	FDD	FDD	TDD	FDD	FDD	FDD
DUPLEX SEPARATION	45 MHz	45 MHz	5 m Sec.	130 MHz	N. AV	45 MHz
RADIO CHANNEL SPACING	200 KHz	200 KHz	1728 KHz	30.30 KHz	25 KHz	25 KHz
TOTAL NO. OF RADIO CHANNELS	124	373	10	164	N. AV.	79
RADIO CHANNEL BIT RATE	270.83 Kb/S	270.83 Kb/S	1152 Kb/S	44.2 Kb/S	36 Kb/S	See Note (2)
MAX. No. OF CALLS PER R.F CHANNEL	8	8	12	4	4	1
MODULATION	GMSK	GMSK	GFSK	pi / 4 - DQPSK	pi / 4 - DQPSK	GMSK
B.W x SYMBOL DURATION	0.3	0.3	0.5			0.25 and 0.45 See Note(3)
MAX Tx-Rx DISTANCE	35 KM	8 KM	100 M	280 KM	40 KM	5 KM

(1) Both single frequency and double frequency of functioning is possible in DSRR. Channels from these two frequency bands are used in case of double frequency operation.
(2) Depends upon used channel coding and it is different for speach or data transmission.
(3) BT = 0.25 is used for 16 Kb/s speech transmission and BT = 0.45 for data transmission at 4 kb/s.

TABLE II :Tx CHARACTERISTICS

	GSM 900	DCS-1800	DECT	TFTS	TETRA	DSRR
MAXIMUM OUTPUT POWER (dBm)						
BS	55	43	24	46	N. Av.	36
MS	43	30	24	40	40	36
Tx POWER vs TIME IN A BURST (dB)	+/- 1	+/- 1	+/- 1	+/- 1	N. Av.	+/- 1.5
Tx ATTACK TIME (µs or ms)	10 (18)	10 (18)	< 10	6 (10)	N. Av.	25 ms
Tx RELEASE TIME (µs or ms) **See NOTE (1) Below.**	10 (18)	10 (18)	< 10	6 (10)	N. Av	5 to 25 ms
TRANSMITTED CARRIER FREQUENCY ACCURACY (Hz or KHz)	50 Hz	50 Hz	+/- 50 KHz	80 Hz	N. Av.	2.5 KHz
Tx POWER IN ADJ. CHANNEL (dBc)	- 50	- 50	- 60	- 50	- 60	- 50
INTRA BTS Tx INTERMODULATION ATTENUATION at 400 KHz (dB)	70	70	54	N. Av.	N. Av.	40 to 70
MAXIMUM Tx DUTY CYCLE (percent)						
BS	100	100	50	100	100	100
MS	12.5	12.5	50	25	25	100

N.AV = not available
N. AP = not applicable

NOTES (1). The figures in brackets include the transient duration.
(2) Different bandwidths for power measurements are specified in different cases.
(3) This table gives a subset of all the parameters specified in the Recs.

TABLE III :Rx CHARACTERISTICS

	GSM 900	DCS-1800	DECT	TFTS	TETRA	DSRR
Rx SENSIVITY (in dBm)						
BS	- 104	- 104	- 83	- 122	- 106	> - 100
MS	- 102	- 100	- 83	- 112 (see note 1)	- 104	
Rx NOISE BANDWIDTH (KHz)	200	200	800	30	20	10 or 18
Rx SELECTIVITY BETWEEN ADJACENT CHANNELS (dB)	- 9 see note 2	- 9 see note 2	- 18 see note 2	N.AV	N.AV	- 50
DIVERSITY RECEPTION (BS)	USEFUL	POSSIBLE	RECOMMENDED	USEFUL	USEFUL	N.AP
MAXIMUM Rx DUTY CYCLE (in %)						
BS	100	100	100	100	100	100
MS	25	25	16 or 100	50	25	100
Rx TIMING SYNC. ACCURACY						
MS	+/- 1 bit	+/- 1 bit	+/- 2 bits	N.AV	N.AV	N.AP
BS	REFERENCE	REFERENCE	REFERENCE			

N.AV = not available
N.AP = not applicable
Note (1) = Power level expressed in dBW/m² on the anntenna
Note (2) = this expresses carrier/interference ratio for good system operation
Note (3) Different bandwidths for power measurements are specified in different cases.
Note (4) This table gives a subset of all the parameters specified in the Recs.

VSAT, GPS, and DBS Technologies

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VSAT Performance Fits Market Niche Applications

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Historic VSAT Applications

When satellite communications systems were first developed antennas were very large. This large size or aperture was required to get enough gain to be useful in satellite communications. High earth terminal receive gain was necessary due to the low transmit power or EIRP from the satellite transponders. High earth terminal transmit gain was necessary due to the relative insensitivity (high noise figure) of the satellite transponders. As transponders became more powerful and more sensitive, smaller earth stations became possible. Thus, Very Small Aperture Terminals or "VSATs" were born.

The first satellite communications systems tended to simply be functional replacements for other terrestrial communications media. For a while multi-channel telephony was the bulk of the traffic being carried. Data communications were very limited, not because the satellite links were inadequate, but rather because computers did not have much communication capability. Most data communication was still teleprinter traffic at 75 or 100 baud using Baudot code.

It was in this environment that the first VSATs were developed. Because governments tended to tightly regulate interconnection to the public switched network these VSAT systems tended to be private. Essentially they became private telephone network bypass systems installed for users who had large enough long distance telephone bills to justify their development and installation.

There were, of course, some notable exceptions to the norm in these initial satellite systems. One of the most significant was the system developed by Equatorial, now a part of GTE Spacenet. A system was developed which took advantage of the inherent broadcast nature of satellite communications to send the same low-rate digital information to several thousand stations simultaneously. Such a system was ideal for the distribution of stock market data and news feeds to multiple affiliates. The Equatorial system design was contrary to what many in the industry believed to be the most economical. Spread spectrum techniques were used and it required higher transponder power and bandwidth than would normally be expected. Satellite capacity was sacrificed to push earth terminal prices lower and lower. Since the system served hundreds of thousands of terminals the economics proved successful.

Evolution of Systems Requirements

Things began to change as the FCC broke up the Bell system. Competition after the break-up in the U.S. meant that standards needed to be published for the

interconnection of telephone equipment. These standards were just what satellite communications systems needed for full connection. The standards permitted manufacturers to develop systems which interfaced to telephone switches (including PBXs) just like existing long distance lines. With these improved interfaces satellite communications systems expanded in usefulness. Since PBXs could be interfaced directly, VSATs could eliminate "the last mile" of connectivity which was historically contracted from the local phone company. This meant that satellite communications systems were beneficial both for wide bandwidth applications (trunked multi-channel systems such as between telephone Dial Central Offices) or for thin route applications (such as between PBXs at remote company locations). The thin route requirement was ideal for VSAT applications because the lower data rates could be handled easily by VSAT terminals.

Satellite communications voice requirements continue to evolve. High bandwidth point-to-point multi-channel voice systems are often better served by fiber optic systems today. In cases where it is difficult or impossible to install a fiber infrastructure, satellite systems continue to have substantial advantages. Satellite communication also often proves its effectiveness in handling thin route traffic where the installation of a dedicated fiber is not justified and in multi-point applications where the broadcast nature of satellite signals is optimal. Both thin route and multi-channel requirements continue to expand.

Early VSAT systems could do a pretty good job of transmitting data while the computers of the era had very limited communications capabilities. Even similar mainframe computers were often not designed to communicate among themselves effectively. When PCs became popular, communications requirements increased dramatically. Not only did users want their PCs interconnected but they wanted them to communicate with their mainframes . Several different approaches were developed for solving this problem. Many were attempted with satellite communications. One of the most common difficulties encountered was protocol incompatibility. While one computer might be able to send and receive data, it might not be able to understand data passed from a dissimilar machine. The solution had a tremendous impact on satellite communications.

Today almost all computers can communicate using the X.25 packet communications protocol. Thus, regardless of the size or type of the computer, X.25 is often a reasonable choice for a standardized communications interface. Satellite communications systems have been designed to make use of this feature. VSAT systems, using X.25 as the access protocol, can pass data between widely diverse computer systems on an international basis. While VSATs could pass data long before computers were ready for it, X.25 brings a relatively easy-to-use standard interface to both. The future holds even higher data rates with variations of existing and future protocols to meet expanding user requirements.

VSAT RF Link Requirements

To see why a particular type of earth terminal is suitable for a specific service application it is important to consider the characteristics of the signals. One can then determine the quality of service which could be provided with a specific earth terminal. This permits a system designer to define overall system requirements and thus the specification requirements for the individual equipment. Satellite systems engineers consider these requirements in terms of the "satellite link equation".

The basic satellite link equation for determining downlink performance is:

$$EIRP_{reqd} = P_L + L_i - G/T_{ET} + k + 10\log(R_s) + E_b/N_o + M \quad \textit{(Equation 1)}$$

Where:

$EIRP_{reqd}$	= Required EIRP (or satellite Effective Isotropic Radiated Power)
P_L	= Downlink Path Loss
L_i	= Implementation Losses
G/T_{ET}	= Earth Terminal "Figure of Merit" (receive Gain divided by Noise Temperature)
k	= Boltzmann's constant
R_s	= transmitted Symbol Rate (data rate with coding, etc.)
E_b/N_o	= Required MODEM energy per bit divided by Noise density
M	= Link Margin (for rain attenuation, etc.)

We can consider an example of a Ku-Band VSAT system by inserting appropriate values and calculating the results over a nominal range. For this example we will use the following:

P_L	= 206 dB
L_i	= 2 dB
T_{ET}	= 160 K Earth Terminal Noise Temperature
k	= -228.6 dBw/Hz/K
E_b/N_o	= 8.5 dB (for BPSK, rate 1/2 k=7 coded, BER $1x10^{-5}$)
M	= 8 dB Link Margin

Table 1 below provides the results of this analysis. There are definitely other factors which affect link performance as well, such as transponder loading and intermodulation distortion, etc., but if the system remains within nominal linear range Equation 1 provides a reasonable prediction. It shows the required satellite EIRP at various data rates (from 2.4 to 256 KBPS) with different earth terminal antenna gain values (from 28 to 45 dB) to satisfy the desired link performance. The table illustrates that changes in any of these different values result in a change in the required EIRP value.

By considering Table 1 it is relatively easy to see that a larger antenna aperture (and the resulting increase in gain) can be directly applied to reduce the required transponder EIRP. In most cases, this reduced EIRP translates into reduced space segment charges. If a small increase in EIRP results in a drastic reduction in total earth terminal cost, however, it may be worth consideration. For example, in an application with 10,000 earth terminals a modest decrease in each earth terminal's cost becomes very significant. This could easily offset a significant increase in space segment costs, as long as the capacity is available.

	EIRP dBW								
R_s KBPS	2.4	4.8	9.6	19.2	38.4	56	76.8	153.6	256
G_{ET}									
28	23.74	26.75	29.76	32.77	35.78	37.42	38.79	41.81	44.02
29	22.74	25.75	28.76	31.77	34.78	36.42	37.79	40.81	43.02
30	21.74	24.75	27.76	30.77	33.78	35.42	36.79	39.81	42.02
31	20.74	23.75	26.76	29.77	32.78	34.42	35.79	38.81	41.02
32	19.74	22.75	25.76	28.77	31.78	33.42	34.79	37.81	40.02
33	18.74	21.75	24.76	27.77	30.78	32.42	33.79	36.81	39.02
34	17.74	20.75	23.76	26.77	29.78	31.42	32.79	35.81	38.02
35	16.74	19.75	22.76	25.77	28.78	30.42	31.79	34.81	37.02
36	15.74	18.75	21.76	24.77	27.78	29.42	30.79	33.81	36.02
37	14.74	17.75	20.76	23.77	26.78	28.42	29.79	32.81	35.02
38	13.74	16.75	19.76	22.77	25.78	27.42	28.79	31.81	34.02
39	12.74	15.75	18.76	21.77	24.78	26.42	27.79	30.81	33.02
40	11.74	14.75	17.76	20.77	23.78	25.42	26.79	29.81	32.02
41	10.74	13.75	16.76	19.77	22.78	24.42	25.79	28.81	31.02
42	9.74	12.75	15.76	18.77	21.78	23.42	24.79	27.81	30.02
43	8.74	11.75	14.76	17.77	20.78	22.42	23.79	26.81	29.02
44	7.74	10.75	13.76	16.77	19.78	21.42	22.79	25.81	28.02
45	6.74	9.75	12.76	15.77	18.78	20.42	21.79	24.81	27.02

Table 1 Ku-Band Downlink Analysis Example

If we assume the values used to be appropriate, Table 1 lets us consider the effects of equipment changes on overall system performance. Consider the use of a transponder on a satellite like GTE Spacenet's GStar 1. Such a transponder has a total EIRP of about 42 dBW, depending upon where the receive earth station is located. Since this value is greater than all those in Table 1, with small exceptions, one might assume any of the analyzed configurations could be used. This power, however, is the total available over the full transponder bandwidth. If any other signals are to be transmitted by the same transponder (which is usually the case with such narrow signals) their power usage must also be considered.

The situation is similar on the uplink side of the equation. There the satellite G/T becomes the limiting factor in absolute signal levels. This G/T value is constrained not only by the physical design of the satellite transponder components but also by such factors as antenna pattern, adjacent signal interference, and radiated earth noise.

Table 1 illustrates the downlink performance expected from a typical Ku-Band link. Similar analysis needs to be performed for the uplink side of each communications link as well. VSATs make use of the property that a relatively large antenna can be used as a hub to transmit to small antennas at the remote terminals. The large hub antenna is able to transmit a stronger signal to the remote sites and is able to provide acceptable BER performance on receive links from the small transmit antennas.

Equation 1, presented above, can also be used to determine uplink performance if the appropriate values are used. In the uplink case the EIRP becomes the earth terminal EIRP instead of the satellite EIRP and the G/T becomes the transponder G/T instead of the earth terminal G/T. Appropriate values for our Ku-Band example are:

P_L	= 207.5 dB (Uplink path loss)
L_i	= 2 dB
G/T_{SAT}	= 0 dB/K (varies greatly depending upon satellite, gain, etc.)
k	= -228.6 dBw/Hz/K
E_b/N_o	= 8.5 dB (for BPSK, rate 1/2 k=7 coded, BER $1x10^{-5}$)
M	= 8 dB Link Margin

Table 2 illustrates the Transmit Power, in dBW, required for the desired BER at the satellite, which is then translated to the receive earth terminal. For this analysis to be valid the receive earth terminal has a sufficiently high G/T that the E_b/N_o received at the satellite is essentially the same as at the receive terminal. This is the general case of a VSAT hub terminal. Table 2 illustrates that changing the transmit terminal antenna gain, power, and data rate are all directly related.

	Xmtr Pwr dBW								
R_s KBPS	2.4	4.8	9.6	19.2	38.4	56	76.8	153.6	256
G_{ET}									
26	5.20	8.21	11.22	14.23	17.24	18.88	20.25	23.26	25.48
27	4.20	7.21	10.22	13.23	16.24	17.88	19.25	22.26	24.48
28	3.20	6.21	9.22	12.23	15.24	16.88	18.25	21.26	23.48
29	2.20	5.21	8.22	11.23	14.24	15.88	17.25	20.26	22.48
30	1.20	4.21	7.22	10.23	13.24	14.88	16.25	19.26	21.48
31	0.20	3.21	6.22	9.23	12.24	13.88	15.25	18.26	20.48
32	-0.80	2.21	5.22	8.23	11.24	12.88	14.25	17.26	19.48
33	-1.80	1.21	4.22	7.23	10.24	11.88	13.25	16.26	18.48
34	-2.80	0.21	3.22	6.23	9.24	10.88	12.25	15.26	17.48
35	-3.80	-0.79	2.22	5.23	8.24	9.88	11.25	14.26	16.48
36	-4.80	-1.79	1.22	4.23	7.24	8.88	10.25	13.26	15.48
37	-5.80	-2.79	0.22	3.23	6.24	7.88	9.25	12.26	14.48
38	-6.80	-3.79	-0.78	2.23	5.24	6.88	8.25	11.26	13.48
39	-7.80	-4.79	-1.78	1.23	4.24	5.88	7.25	10.26	12.48
40	-8.80	-5.79	-2.78	0.23	3.24	4.88	6.25	9.26	11.48
41	-9.80	-6.79	-3.78	-0.77	2.24	3.88	5.25	8.26	10.48
42	-10.80	-7.79	-4.78	-1.77	1.24	2.88	4.25	7.26	9.48
43	-11.80	-8.79	-5.78	-2.77	0.24	1.88	3.25	6.26	8.48
44	-12.80	-9.79	-6.78	-3.77	-0.76	0.88	2.25	5.26	7.48
45	-13.80	-10.79	-7.78	-4.77	-1.76	-0.12	1.25	4.26	6.48

Table 2 Ku-Band Uplink Analysis Example

Two of the factors which can be considered here are the effects of antenna gain and required transmit EIRP. An increase in antenna gain, resulting from the use of a larger antenna aperture, results in a lower required transmitter power. If installation space is not a problem a larger antenna reflector may be much less costly than a larger earth terminal High Power Amplifier. The VSAT system designer can trade-off such considerations in the design of the overall system.

Transceiver Characteristics

From the range of VSAT systems requirements, we observe that there are distinctly different types of systems. Our analysis of the link equations shows that the low rate systems can operate with relatively small antennas and moderate High Power Amplifiers. High rate systems require larger antennas and substantial High Power Amplifiers. Clearly, a VSAT built for the most stringent (high rate) requirements will exceed the requirements of a low rate system. If the costs of each were about the same there would be little need to worry about building one system which meets all requirements. In fact, the costs vary greatly depending upon the capabilities of the individual subsystems. This means that a prudent system designer can significantly enhance cost-effectiveness by using subsystems which meet the minimum requirements with desired margin for system expansion. This may seem fairly obvious, but it is not always the way current systems are designed.

Many of the subsystems of a VSAT need not change from one requirement to another. For example, Low Noise Amplifiers are moderately low in cost and can serve both high rate and low rate requirements equally well. Antennas are limited by the laws of physics so one must select an antenna of adequate aperture to produce the desired gain. Probably the most expensive single elements of VSATs, which can change greatly based upon system requirements, are the High Power Amplifiers and the transmitter and receiver, or transceiver.

As can be seen in Table 2 above, selection of an appropriate antenna/HPA trade can have a substantial effect. A change in antenna aperture by 1/2 provides a gain change of 6 dB, and a corresponding 6 dB HPA power requirement change. HPAs are among the most costly subsystems in a VSAT terminal so this is often an excellent trade. Due to this fact it is usually beneficial to design a VSAT system with a separate HPA so appropriate units can be installed in each VSAT to meet requirements. Too large an HPA results in undue expense. Too small causes unsatisfactory link performance.

There are other transceiver characteristics which have more subtle effects. The next most costly element in a VSAT transceiver, after the HPA, is the synthesizer. The performance-limiting specification of any VSAT synthesizer is its phase noise. High synthesizer phase noise results in poor BER performance which is especially pronounced on low rate digital signals. Different approaches can be taken to reduce this cost impact. If the synthesizer can be designed with larger step sizes its phase noise is easier to reduce-- this limits channel spacing however. In some systems it is possible to use a higher symbol rate with FEC and/or Time Division Multiple Access (TDMA) transmission to achieve the same user data rates with less phase noise effects. Similarly the system designer can consider different modulation formats which are less susceptible to the phase noise. The bottom line is: there is no single best answer. From a conceptual standpoint the easiest answer is to use the synthesizer

with the lowest possible phase noise. From a practical standpoint, however, this can result in undue cost increases.

Another more subtle effect is Intermodulation Distortion or IMD. This often becomes a concern when more than one carrier is transmitted simultaneously. Solutions include improved transmitter design or the use of a single carrier with some type of TDMA. The cost impact of improvements in transmitter design to reduce IMD are sometimes difficult to assess. If each transmitter must be hand-tuned in production to reduce IMD its cost would be much higher than one which produces acceptable performance in automated production. The upconvertor and HPA power levels are often major considerations for the desired IMD performance. Building in extra power margin for improved IMD performance can sometimes cause an unacceptable increase in costs.

Market Niche VSAT Examples

Having examined the "top level" factors in VSAT performance one can consider some typical examples of VSAT operation. While these examples will not be considered in minute detail, they illustrate the differences in requirements between various applications. VSAT performance can be adjusted to provide a cost-effective system solution in each case. While in each case there are obvious trade-offs in antenna aperture and EIRP, it is interesting to note that VSAT transceiver performance can also be considered in cost for performance trades.

Multi-Channel Telephony Example. Multi-Channel Telephony is one of the most demanding of VSAT applications. Telephony requires substantial communications throughput-- typically 32 KBPS full-period, full-duplex, for each toll-quality voice channel. "Bursty" transmission characteristics which may be acceptable with data traffic are not acceptable for voice. This means that sustained communications throughput must be maintained during the entire call. There are basically two ways to achieve this-- either transmit continuously during the call (using Frequency Division Multiplex, for example) or burst (with TDMA, for example) at such a high symbol rate that an effective 32 KBPS continuous rate is maintained. In the later case, if the symbol rate is 128 KBPS the transmitter would have to be on the air for more than 1/4 the time. The obvious trade-off there is that a higher symbol rate requires higher EIRP on both the uplink and downlink. In such a TDMA case, for example, a 4 times increase in symbol rate (a 6 dB increase) would require a 6 dB increase in EIRP for the same BER performance. In practice, TDMA systems usually use the same frequency for multiple stations so if a particular station is capable of transmitting 4 carriers, for example, and 4 such stations must be accommodated the symbol rate must be at least 16 times the basic channel data rate. A 16 times symbol rate increase (24 dB) would require a 24 dB EIRP increase. Considering Table 2, one can see that this soon becomes a substantial amount of transmitter power.

If FDMA is used the VSAT terminal can transmit continuously for each channel. In multi-channel telephony this means that the VSAT would have to transmit a separate signal for each channel continuously. Multiple simultaneous signals through the same transmitter require better IMD performance than a single signal but this may be advantageous in utilizing the total EIRP over a wider bandwidth.

The effect that multi-channel telephony service has on the VSAT transceiver is significant. There are at least three major performance requirements for this application:

1) Moderately high power HPA. Due to the relatively high user data rate (whether with a single signal or multiple) a moderately high EIRP is required. Since we are discussing a "VSAT" application relatively small antenna aperture is considered to be inherent.

2) Synthesizer phase noise must be relatively low if FMDA is used. High synthesizer phase noise could cause interference with adjacent carriers as well as causing demodulator BER problems.

3) IMD performance must be high if FDMA is used. Multiple simultaneous carriers on the uplink increase susceptibility to noise and resultant reductions in BER on the transmitted carriers.

Multi-channel telephony is one of the most demanding VSAT applications. Transceiver performance must be among the best and thus costs tend to be among the highest in any VSAT application. One of the only optimizations which can be used is the trade-off of antenna aperture to HPA power level.

Point-of-Sale Data Terminal Example. Point-of-Sale Data Terminals have become one of the largest VSAT applications. Currently there are probably more VSATs used for this application than any other. In this application "bursty" data is perfectly acceptable but since it tends to use operator-controlled transactions the response through the network or latency must be on the order of a few seconds at most. This implies that some type of TDMA or packet access may offer optimal use of the communications resources. Data rates tend to be relatively low (19.2 KBPS or so) because only a few bytes of information need be transferred in each transaction. One of the factors which makes these systems practical, however, is often the ability to transmit large blocks of computer data in "off-peak" periods. Typical applications make use of the network for credit verification during the business day and backhaul inventory control at night. This means that low data rates may be needed for the transaction processing but a dynamicaily higher data rate capability may be advantageous.

One of the overpowering factors in this application is that each network tends to have a large number of remote sites-- sometimes several thousand. This means that cost

of each remote terminal is a significant factor! Thus, steps taken to reduce the terminal cost even slightly can have a very big effect on overall cost-effectiveness. This can translate into things like designing the system for the relatively low data rates needed for the transaction processing and simply using whatever capability results in the backhaul function. Since there is such a large number of terminals it may also be prudent to use a moderately inexpensive control mechanism and have less than optimum space segment usage while absolutely minimizing the costs of each remote terminal.

This application offers some opportunities in cost reduction over other VSAT applications. The performance requirements placed on the VSAT transceviers include:

1) Reduced HPA output power. Since relatively low data rates are required, a lower EIRP from each terminal is necessary. This can mean smaller antennas and/or reduced HPA power requirements. Since HPA costs are among the largest factors in VSAT transceiver design, a reduction in HPA power levels is often prudent.

2) Synthesizer phase noise should be relatively low. Since fairly low data rates are used synthesizer phase noise should be considered to improve BER. Also since the rate is so low, however, FEC coding or other steps could be taken to improve BER for the same power level at the expense of bandwidth. The coding trade-off could be considered to reduce costs.

3) IMD performance is not as critical. This application almost always requires a single carrier on the uplink so IMD susceptibility is usually negligible. A system designer can make use of this fact in specifying transceiver performance to reduce costs.

Point-of-Sale data terminals are a very widespread VSAT application. With several trade-offs available a prudent system designer can relax some specifications and tighten others to minimize system costs while still meeting performance requirements.

SCADA Terminal Example. Supervisory Control and Data Acquisition, or SCADA, is an interesting VSAT application. SCADA systems require relatively small blocks of digital data to be passed between a central control site and many remote locations. For many years this application suffered from the early VSAT data transmission problems-- the VSATs could pass the data but the computers weren't ready to communicate. Progress in data communications protocols and microprocessor systems have now positioned SCADA to become a very popular VSAT application in the next few years.

The principal requirements in SCADA systems are to pass relative low rate data of a "bursty" nature. This implies the use of some sort of TDMA or packet transmission

protocol. Communications takes place between computers so latency is not as big a problem as with point-of-sale terminals. There are, however, some critical SCADA applications where response needs to be very short. These include things like remotely responding to a pipeline failure or powerline fault. A good compromise for these situations is some sort of prioritization scheme which could dynamically shorten latency when required. This is usually a matter of concern to the control system rather than for the communications system engineer.

Also, since SCADA applications tend to be very remote it may be advantageous to permit operation with low input power. Some SCADA systems have even been implemented with solar power supplies to permit unattended, excessively remote installations, away from conventional power supplies. Since data rates tend to be low and thus EIRP can be low, a low input power requirement is realistic for SCADA.

This application again offers some opportunities in cost reduction over other VSAT applications. The performance requirements placed on the VSAT transceviers in SCADA service include:

1) Reduced HPA output power. Since relatively low data rates are required, a lower EIRP from each terminal is necessary. This can mean smaller antennas and/or reduced HPA power requirements. Since HPA costs are among the largest factors in VSAT transceiver design, and since a lower input power requirement is also often desired, a reduction in HPA power levels is often prudent.

2) Synthesizer phase noise should be relatively low. Since fairly low data rates are used synthesizer phase noise should be considered to improve BER. Also since the rate is so low, however, FEC coding or other steps could be taken to improve BER for the same power level at the expense of bandwidth. The coding trade-off could be considered to reduce costs.

3) IMD performance is not as critical. This application always requires a single carrier on the uplink so IMD susceptibility is negligible. A system designer can make use of this fact in specifying transceiver performance to reduce costs.

SCADA terminals are a very rapidly growing VSAT application. With the many trade-offs available, a prudent system designer can optimize earth terminal design for SCADA and achieve substantial cost reductions while still meeting all operational requirements.

Summary

We have seen that VSAT systems continue to evolve as satellite transponder performance increases and as users increase their needs for VSAT services. User equipment (like PBXs and networked computer systems) now have a greater capability to make use of VSAT-delivered communications than ever before. Current VSAT systems are exceptionally flexible and capable of meeting dynamically changing market needs with sometimes minor and other times more substantial modifications.

We have also seen the quantitative effects illustrated with the satellite link equation. Analysis of the individual communications links permits the VSAT system designer to consider several alternatives to maximize performance for a given cost or minimize cost for a specified service quality. Since VSAT systems can have several thousand terminals, careful consideration of cost-reducing strategies are usually warranted. It's no longer enough simply to buy the "latest and greatest" VSATs and install them consistently. Attention must be paid to the minimum subsystem requirements necessary to provide the desired level of service. HPA power levels are but one example-- bigger isn't always better.

Some VSAT systems will consistently place a heavy burden on maximum subsystem performance-- like the multi-channel telephony example. The available industry performance limits will continue to be the ultimate limits of service quality offered by those systems. Even there, intelligent trade-offs can be made to minimize costs while meeting performance requirements. Other applications exist which can benefit greatly by designs optimized not for performance but for price. When several thousand earth stations are being installed in a single VSAT system every dollar saved becomes significant. The prudent VSAT system engineer considers this fact and examines the desired level of service carefully when specifying VSAT subsystem requirements.

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ENVIRONMENTAL EFFECTS ON MOBILE SATELLITE COMMUNICATIONS

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In recent years there has been much effort devoted to making land mobile communications possible using low Earth orbiting satellite systems. Satellite communications with the mobile terminal can suffer from the unpredictability of the propagation environment. In this environment, a received signal undergoes extreme variations in amplitude due to multipath fading and shadowing. Multipath signals can combine destructively to attenuate the received signal below usable levels resulting in outage times. Another effect of multipath is time delay spread, that is, multipath signals arrive in time intervals that cause a definite overlapping of symbols. This leads to intersymbol interference that in turn limits the symbol transmission rate.

Satellite communications is also limited by interference from other transmitters. Outage times occur when the sum of interfering signal powers exceeds the instantaneous signal power. In the absence of interference, outage times occur when shadowing decreases the signal-to-noise ratio below the minimum ratio required by the receiver. This suggest the need for a link margin that can be excessive to cope with multipath fading and shadowing. Unfortunately, a link margin is influenced by many factors including the type of terrain, the height and density of the vegetation, and the distribution of trees and man made structures.

Any satellite mobile communication system transmitting narrow-band signals can overcome the effects of multipath and shadowing by using a mixture of schemes. Among these schemes are adaptive equalization, adaptive symbol rate, and error-control. However, much greater resistance to multipath and interference is possible with spread spectrum wide-band signals. The most popular scheme appears to be direct-sequence code division multiple access (CDMA).

Multipath

Regardless of the radio transmission scheme, the power radiated from a satellite antenna will spread over a particular service area. It is desired that the spreading signal travel from satellite to receiver along a direct propagation path. However, as the signal spreads over the service area it will reflect off objects in the environment. This creates reflection signals that may return to the receiver along indirect propagation paths as illustrated in Figure 1. Notice that some of these paths are longer than others and with each reflection there is a corresponding loss of signal energy. Therefore, each reflection signal arrives delayed from the others and with a different power.

When two or more of these signals combine at the receiver, the amplitude of the resultant signal may increase or decrease. This of course, depends upon the phase and amplitude relationship of the arriving signals. Their phase relationship will depend upon the distance of each path measured in wavelengths. If the two distances differ by an integral number of wavelengths, the phase of the two signals will be in alignment, and the resultant signal will be the sum of the two signals. Should the two distances differ by an odd number of half wavelengths, the two signals will be 180 degrees out of phase and the resultant signal will be the difference between these signals. Since the location of a mobile radio is not constant, the phase relationship between the different path signals will vary with receiver location and hence the envelope of the resultant signal will vary. For this reason, the mobile radio experiences fades in signal strength that varies in depth and duration depending upon the mobile's speed and operating frequency.

Multipath also occurs when a radio wave traverses a medium with physical scatters. This medium includes tree foliage, ground vegetation, and rocky slopes. Because the tree foliage presents a discontinuous reflecting surface, a single traversing signal diffuses into a multitude of closely spaced signal paths. Upon reception, the diffused signals combine to create a resultant signal. This resultant signal undergoes amplitude and phase variations described by the Rayleigh and uniform distributions, respectively.

Since the antenna of a mobile radio is close to the ground, multipath signals resolve into three components. One is a specular component (often the ground reflection) which is coherent with the incident signal (line of sight) and the other is a noncoherent (diffuse) component that fluctuates in amplitude. The term specular refers to a nonfading signal, which usually arrives Doppler shifted from the transmitted frequency. Specular reflections arise when the incident signal bounces off the smooth surface of buildings or the ground. Should a strong specular path and many weaker path signals combine at the receiver, the resultant signal produces amplitude variations that follow a Rice-Nakagami distribution.

The destructive combining of multipath signals creates a communication's channel with a range of channel frequencies that undergo attenuation. This range of channel frequencies is commonly called the "coherence bandwidth." A channel exhibiting flat frequency fading has a coherence bandwidth that is greater in comparison to the bandwidth of the transmitted signal. In a flat fading channel any two identical signals transmitted on separate frequencies (within the coherence bandwidth) will arrive with their envelopes fading in unison. As the frequency separation increases, their envelopes will no longer fade in unison. Such a channel is exhibiting frequency selective fading, because the channel has a coherence bandwidth that is smaller in comparison to the bandwidth of the transmitted signal. As a result, the signal is amplitude and phase distorted, by what appears in the frequency domain to be a notch in the bandwidth of the received signal.

Mathematically the coherence bandwidth is inversely proportional to the differential delay time between the multiple signals that reach the receiver. For example, a transmitted signal traveling at 1 ns/ft along multipaths that differ by 200 feet in length will arrive 200 ns apart, causing a fading bandwidth of approximately 5 MHz. If these multipath signals destructively combine to produce a very deep fade, the mobile is likely to experience a communication outage. This is not unusual as the mobile radio often passes through random fades of varying depths. These depths vary by 10 to 40 dB below the mean level with successive minima occurring every half wavelength.

Frequency selective fading or time delay spread occurs when the difference in propagation delay on the different paths is similar to or greater than the symbol duration. If the difference is very much smaller than the symbol duration, then the multipath channel resembles a flat frequency fading channel. When multipath signals arrive in intervals comparable to the symbol duration each symbol will overlap with preceding and following symbols. In a digital system, particularly one attempting to operate at a high symbol rate, the overlapping of symbols creates intersymbol interference (ISI). A transmitted signal traveling at 1 ns/ft along multiple paths that differ by 1000 feet in length will arrive 1 us apart. If the symbol rate is 125 kilosymbols per second, the symbol duration is 8 usec. As a result, the average symbol overlap is 12.5 percent, which may be an unacceptable level of ISI. The overall effect of the energy contributed by overlapping symbols are greater bit errors. Intersymbol interference can produce error bursts even if the signal-to-noise ratio is high. Designers can lessen ISI by reducing the symbol rate or by employing adaptive equalization.

Path Losses

The direct path is one in which the propagation path is free of obstacles that might absorb or reflect the incident signal's energy before it reaches the receiving antenna. As the signal travels from transmitter to receiver it will undergo path attenuation due to free-space loss and transmission losses. The distance dependent free-space loss is given by

$$Lp = 10 * \log [(Y)^2 / (4*PI*d)^2] \text{ dB}$$

Where d is the distance in meters between terminal and satellite and Y is the wavelength in meters.

For a one wavelength separation between isotropic antennas, the free space loss is 22 dB and it increases by 6 dB each time the distance doubles. Consider the 42,162 km distance a radio wave travels to or from a geostationary satellite. If the system employs a 1.6 GHz operating frequency, the free space loss is almost 190 dB, which is enormous amount of signal loss. Overcoming this loss usually requires higher power transmitters, which places a considerable strain on satellite energy resources. Also, the round trip distance creates long propagation delays (approx. 0.5 sec.) that limits voice transmission quality. On the other hand, low Earth orbiting satellites are closer (765 km), which greatly reduces the free space loss to the mobile terminal. This allows for higher signal levels, lower propagation delays (0.003 second), and lower cost, which is appealing for future satellite mobile applications.

For satellite communications at frequencies above 8 GHz, transmission losses due to rainfall and atmospheric moisture become major concerns in the link design. This is because rain and atmospheric losses increase significantly at higher frequencies and at lower elevation angles. A uniquely troublesome path-loss occurs when the propagation path is partially obstructed by tree foliage, large buildings, or tall vegetation. Within this short obstructing path distance, the signal may undergo considerable attenuation. This path attenuation is highly dependent upon the frequency and upon the absorption properties of the obstacle. For instance, the average amounts of attenuation a 900 MHz signal undergoes when traversing 4 meters of roadside trees is 2.9 dB. That is, the signal lost about half its power. We can predict the average attenuation due to foliage by [1]

$$L = [0.187 * f^{0.284} * d^{0.588}] \text{ dB.}$$

Where f is frequency in MHz and d is the length of foliage traversed by the signal in meters. Undoubtedly, variations in shadowing loss will arise because of changes in the physical surroundings. Unfortunately, these variations may require a link margin for a given service (voice, data, fax, etc.) to be excessive to cope with the shadowing losses of a particular service area (urban, rural, mountainous, etc.).

The result of increasing shadow loss, rain attenuation, or flat frequency fading is equivalent to decreasing the instantaneous signal-to-noise ratio. As the losses become significant, detection errors occur in clusters commonly called burst errors. In this case, burst errors occur when the symbol rate is too high for the instantaneous signal-to-noise ratio. As a result, an outage occurs because the energy per symbol is too low. Note that the bit error rate is not always equal to the symbol error rate this depends on the number of modulation levels. One way to increase the energy per symbol is to raise the transmitter power. However, this may not be possible for a hand-held radio due to its limited battery power. On the other hand, raising the up-link transmission power of a fixed base station is not a problem. It is a practical way to reduce outage times due to rainfall [2].

Also, one can raise the energy per symbol by lowering the symbol rate. Since the energy per symbol is equal to the received signal power divided by the symbol rate, we can double the energy per symbol simply by halving the symbol rate. This suggest the possibility of adaptive symbol rate schemes that operate at higher data rates when the signal-to-noise ratio is high, and at lower data rates when the signal-to-noise ratio is low. Another way to overcome shadowing losses is to employ simple error control techniques that cope with short fade durations. Often satellite systems offering packet data communications overcome the occasional shadow outage by using error detection followed by retransmission.

CDMA

To resist multipath fading and allow users to communicate simultaneously over a single channel, designers are considering spread spectrum schemes. The favored scheme uses code division multiple access (CDMA) with direct spread modulation bandwidths ranging from 1 to 20 MHz. Direct spread modulation multiplies the data sequence by a pseudo random bit sequence that spreads the information far beyond the information bandwidth. By employing unique pseudo random bit sequences many CDMA users are able to transmit on the same frequency simultaneously and each user receives its information by recognizing its unique sequence pattern.

The CDMA receiver is able synchronize to one of the multiple signal paths. As long as the remaining signal paths are delayed by more than the chip duration from the synchronization path. The despreading process will greatly attenuate the remaining signal paths. To illustrate, consider a CDMA system using a chip rate of 5 Mchips/s, the chip duration is 200 ns, and therefore multipaths that differ by 200 feet or less creates overlapping chips. This would normally result in loss of synchronization unless the chip rate is increased until the differential path delay is one or more chip lengths. The remaining multipath signals are treated as uncorrelated interference signals whose signal power is reduced by the process gain of the system.

Recent urban propagation studies report fade bandwidths of 3 to 15 MHz [3,4], those CDMA systems employing spread bandwidths that are less than the reported fade bandwidths may also expect synchronization problems during deep fades. In this case, the synchronization path is likely to drop to power levels comparable to that of the multipath signals, giving rise to Rayleigh fading. As a result, the despreading scheme decrease the total signal power considerably, creating loss of synchronization leading to an outage time.

Mobile satellite systems are developing in many directions. Besides CDMA schemes, there are the traditional radio transmission schemes. Among these schemes are frequency division multiple access (FDMA), time division multiple access (TDMA), and hybrids of these schemes. Gains in the art of low cost satellite design allow system planners to move away from expensive large geostationary satellites toward medium-sized multiple low Earth orbiting satellite systems.

DERIVATION OF THE RICE-NAKAGAMI DISTRIBUTION

What follows is the derivation of the Rice-Nakagami multipath envelope distribution. We assume the transmitted signal is unmodulated this will simply the analysis. The direct path component is represented by

$$E_i(t) = A \cos[(wc + wd)t]$$

and the specular path component by

$$E_s(t) = B * \cos[(wc + wd)t + @]$$

Where wc is the angular carrier frequency, wd is the angular doppler frequency shift, and @ is some arbitrary phase.

Using the trigonometric identity

$$\cos(W + Z) = \cos W * \cos Z - \sin W * \sin Z$$

We can define X(t) and Y(t) as the sum of the in-phase and quadrature phase components of the direct and specular signal, respectively. Hence

$$X(t) = A * \cos(wd * t) + B * \cos(wd * t + @)$$

and

$$Y(t) = A * \sin(wd * t) + B * \sin(wd * t + @)$$

then

$$m(t) = X(t) * \cos(wc * t) - Y(t) * \sin(wc * t)$$

Likewise, the diffused in-phase and quadrature signal components can be represented by

$$I(t) = \text{SUM} \{ A_k * \cos(wd * t + P_k) \} \text{ for } k=1 \text{ to } N$$

and

$$Q(t) = \text{SUM} \{ A_k * \sin(wd * t + P_k) \} \text{ for } k=1 \text{ to } N$$

By the central limit theorem the I(t) and Q(t) components are approximately independent Gaussian random variables, with the approximation becoming more accurate as the N gets large.

$$S(t) = I(t) * \cos(wc * t) - Q(t) * \sin(wc * t)$$

Where P_k are fixed random phases uniformly distributed from 0 to 2*pi and S(t) is Gaussian, and the envelope

$$R = [\ I(t)^2 + Q(t)^2\ ]^{0.5}$$

has a Rayleigh distribution,

$$p_R(r) = (r / var) * \exp [- r^2 / (2 * var)]$$

Define new parameters (drop the time variable)

$$x = X + I \quad \text{and} \quad y = Y + Q$$

Therefore

$$r^2 = x^2 + y^2$$

$$z = \tan_{-1} (y / x)$$

Since I and Q are Gaussian, zero mean with variance var = Q^2, and uncorrelated, x and y are Guassian and independent. Thus,

$$p(x,y) = \frac{1}{2 \text{ pi var}} \exp \frac{- [(x - X)^2 + (y - Y)^2]}{2 \text{ var}}$$

At baseband doppler is zeroed, therefore X is the length of the fixed coherent vector and Y is zero. From the Jacobian technique of transformation of variables, the joint probability density of the envelope and phase is given by

$$p_{x,y}(x,y) \Longleftrightarrow p(r,z) = r * p_{x,y}(r * \cos z, r * \sin z)$$

$$p(r,z) = \frac{r}{2 \pi var} \exp \frac{-[(r*\cos z - X)^2 + (r*\sin z)^2]}{2\,var}$$

Simplify using the trigonometric identity $[(\sin z)^2 + (\cos z)^2 = 1]$

$$p(r,z) = r / (2 * pi * var) * \exp \{ [-(r^2 + X^2) + (2 * r * X \cos z)] / (2 * var) \}.$$

$$p(r,z) = \frac{r}{2 \pi var} \exp \frac{-(r^2 + X^2 + Y^2) + (2*r*X*\cos z)}{2\,var}$$

The probability density of the envelope is found by integrating out the phase variable

$$p(r) = \int p(r,z)\, dz$$

$$p(r) = \frac{r}{var} \exp \frac{-(r^2 + X^2)}{2\,var} * \frac{1}{2\pi} \int \exp [(r * X / var) * \cos z]\, dz$$

We can express the integral by means of a Bessel function;

$$I_0(k) = 1 / (2 * pi) \int \exp (k * \cos z)\, dz$$

$$= 1 / (2 * pi) \int \exp (r * X / var) * \cos z\, dz.$$

Where $I_0(k)$ is the modified Bessel of order zero. At last we get the Rice-Nakagami density, which describes the summation of a strong specular signal and weaker multipath signals

$$p(r) = (r / var) * \exp [-(r^2 + X^2) / 2 * var] * I_0 (r * X / var)$$

for $r >= 0$ and $0 =< z <= 2 * pi$.

We can include the contribution of additive white Gaussian noise (AWGN) to the quadrature Gaussian terms of the diffuse component together with the specular and direct component to form

$$p(r) = \frac{r}{V_n^2 + E_{rms}^2} \exp\left(\frac{-(r^2 + E_s^2)}{2(V_n^2 + E_{rms}^2)}\right) I_o\left[\frac{E_s * r}{V_n^2 + E_{rms}^2}\right]$$

Where r is the instantaneous peak envelope voltage, Vn^2 is the variance (average power) of the AWGN, $(E_s^2)/2$ is the average power in the specular signal, and E_{rms}^2 is the average power in the in-phase or quadrature components of the diffuse multipath. The total average received signal power is $[E_{rms}^2 + (E_s^2) / 2]$.

The probability that the envelope of the received signal exceeds a defined value, s, is given by

$$P(r >= s) = \int_s^{\infty} p(r)\, dr$$

If the dominate signal level $(E_s^2)/2$ drops to power levels comparable to that of the multipath signals, then Rayleigh fading occurs.

References

1. CCIR report 236-5, "Influence of Terrain Irregularities and Vegetation on Tropospheric Propagation," Vol. V, 1982.

2. N. Lay, K. Dessoucky, "A Communication Protocol for Mobile Satellite Systems Affected by Rain Attenuation," IEEE J. Select. Areas Commun., Vol. 10, No. 6, August 1992.

3. L. Milstein, D. Schilling, R. Pickholtz, et al., "On the Feasibility of a CDMA Overlay for Personal Communications Networks," IEEE J. Select. Areas Commun., Vol. 10, No. 4, May 1992.

4. D. Schilling, L. Milstein, R. Pickholtz, et al., "Field Test Experiments Using Broadband Code Division Multiple Access," IEEE Commun, Mag., pp 86-93, Nov. 1991.

Recommended Reading

1. C. Loo, "Digital Transmission Through a Land Mobile Satellite Channel," IEEE Trans. Commun., Vol. 38, No. 5, May 1990.

2. CCIR report 236-6 "Ionospheric Effects Upon Earth-Space Propagation," Vol. VI, 1986.

3. P. J. Crepeau, "Uncoded and Coded Performance of MFSK and DPSK in Nakagami Fading Channels," IEEE Trans. Commun., Vol. 40, No. 3, May 1992.

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A New Variable Rate Vocoder for Wireless Communication and Voice Storage Applications

by

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Introduction

Since the invention of the telephone more than a century ago engineers have sought to increase the number of voice channels that can be transmitted over bandwidth-limited electronic media. This includes both "wired" and "wireless" transmission systems. Recently, this quest has also led designers to find more efficient methods for storing voice signals for applications such as voice mail systems.

A key aspect of efficient digital voice transmission or storage is the use of a suitable voice digitizing system that reduces the data rate required to send or store voice signals. Voice encoding systems can be either simple, low cost techniques which usually require higher encoding data rates. Alternatively, more sophisticated, higher cost, low data rate approaches may be used. This paper presents a new voice encoding algorithm that provides telephone quality voice encoding at low data rates. This system combines the latest in digital signal processing (DSP) algorithms, modern VLSI technology, and a unique feature: dynamically variable data rate determination.

This paper describes the motivations for the use of digital voice encoding along with the tradeoffs and considerations associated with the selection of an appropriate coding system. Example applications are presented which demonstrate the value of variable rate voice coding systems. Finally, a single-IC implementation of such a variable rate coding algorithm is described. This device is commercially available and is designed to provide high quality speech coding to applications requiring low cost and low power consumption, such as digital cellular and cordless phones, VSAT systems, voice storage systems, and "voice over data" modem systems.

Background

Since the 1960's, the Bell system has been slowly switching over to digital technology for the efficient transmission of wireline voice communications. Only in the past few years has this conversion of digital voice transmission been applied to commercial wireless communication systems. The transmission of

digitized voice signals over RF channels began with military systems. Then came satellite-based telephone systems, VSAT's and, more recently, digital cellular telephony and similar services. This extensive switchover is not yet completed, but all these systems are benefited by the inherent advantages of transmission of digital signals. These advantages include:

1.) The use of sophisticated channel multiplexing techniques (e.g., TDMA, FDMA, packet switching, spread spectrum technology);

2.) The ability to control the transmission-induced noise levels, as well as the volume of the transmitted speech through the use of digital equipment such as regenerative repeaters and forward error correction (FEC) technology;

3.) The ability to provide security on the voice channel through the use of digital encryption technology;

4.) In some cases, digitized voice transmission will actually require less channel bandwidth than the transmission of analog voice information;

5.) The ability to buffer and store voice information using digital storage techniques (e.g., hard disks);

6.) Maximal use of advanced digital signal processing (DSP) techniques combined with low cost VLSI digital integrated circuit technology.

To take maximum advantage of these characteristics of digital transmission technology, an appropriate voice coding system must be selected for a given system. Many different voice coding systems exist and provide selective features and performance to meet the requirements of any specific application. To determine the right choice for voice coding, several factors must be considered as described below.

What is "Speech Encoding"?

Speech encoding is the conversion of analog speech signals to a digital format. The goal of speech encoding is to encode and decode speech signals so that the original voice message is accurately reconstructed.

A typical "telephone quality" analog speech signal is limited to a bandwidth ranging from about 300 Hz to about 3400 Hz. For simplicity, the desired bandwidth is filtered to range from near D.C. (0 Hz) to 4 kHz. To transmit higher fidelity audio signals, such as music, higher bandwidths are required and different encoding systems are used. However, we will limit our interest to the encoding of standard speech signals with no more than a 4 kHz bandwidth.

Given a 4 kHz signal bandwidth, sampling theory states that we must sample the signal at a rate of at least twice our "bandwidth of interest"; that is, at least 8,000 samples per second. If we use a simple linear digitizing approach to our 8,000

sample per second signal, 12 bits are required to encode each sample to provide a full 72 dB dynamic range, which is considered adequate for normal speech signals. However, the result is a digitized transmission rate of: (8,000 samples/second x 12 bits/sample) = 96,000 bps! Assuming a transmission bandwidth efficiency of about 1 bps per Hertz of bandwidth, we see that the digitized speech would require 96 kHz of bandwidth to transmit only 4 kHz of information. This 24:1 increase in bandwidth expansion is not very efficient.

Types of Speech Encoders

So far, we have only described a basic speech "digitization" system. However, even simple speech "compression" techniques provide a much greater efficiency in our speech encoding system. A very simple compression system is called "companding". Companding takes advantage of the fact that, although the human ear can hear a wide dynamic range of signal levels, the "instantaneous" dynamic range is limited by the loudest signal input to the ear at that moment. A companding voice encoding system encodes each speech sample into a value with a limited dynamic range. However, the compander also provides a value, similar to a gain value, that determines where, within the full encoding dynamic range, that particular sample lies. Using such techniques, the required data rate for telephone quality speech signals is reduced to 64 Kbps (from 96 Kbps). Two commonly used companding techniques are called "mu-Law" and "A-Law" systems, used by the North American Bell System and the European telephone systems, respectively.

Companding is just one (simple) approach to speech encoding. Other commonly used waveform coding techniques include "adaptive delta pulse code modulation" (ADPCM), "continuously variable slope delta modulation" (CVSD), and sub-band coders. These types of waveform encoders provide good quality speech to data rates as low as 24 Kbps and can encode intelligible speech to as low as 16 Kbps.

Figure 1 shows the "universe" of speech encoding techniques. This figure illustrates the set of all signal encoders, speech encoders or otherwise, and the subset of speech specific encoders. The set of all speech encoders is further divided into "waveform encoders" and "vocoders".

Waveform coders are actually sophisticated Analog-to-Digital Converter (ADC) systems. Our previous example of the compander approach is one type of waveform coder. Waveform coders do not assume that the signal being encoded is a speech signal, but can be any type of analog signal. As a result, waveform coders are typically better at encoding non-voice signals, such as tones or music. Waveform coders also typically require simple architectures and short processing delay times. The generally simple architectures of waveform coders typically result in lower cost implementations.

However, even though waveform coders provide these advantages, the data rate required to encode speech signals to achieve good quality is typically quite a bit higher than for the alternative encoding approach, i.e., vocoding.

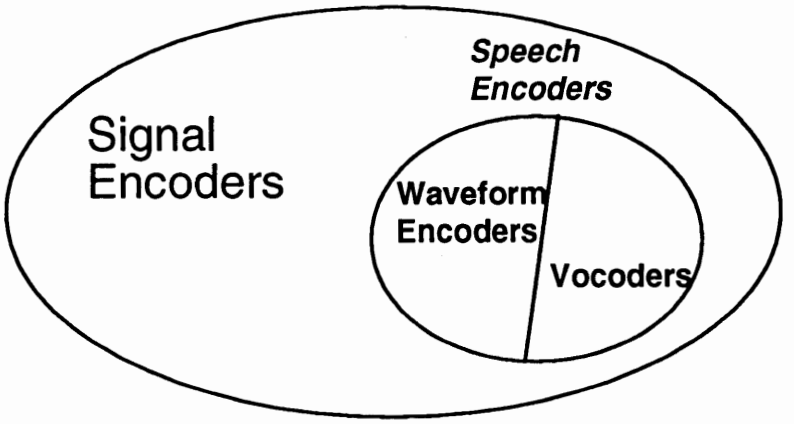

Figure 1: The Universe of Signal and Speech Encoders

Like waveform coders, vocoders convert speech signals from analog to compressed digital format and back to analog speech. However, vocoders are optimized to operate with speech signals. Vocoders assume that the signal being encoded is a human speech signal and attempt to electronically model the human speech mechanism. Because vocoding makes such assumptions about the encoded signal, the resulting data rate is typically quite a bit lower for similar quality when compared to a waveform coder system. The data rate reduction using vocoder technology can be as high as a factor of four or more when compared to a similar quality waveform coder.

Because vocoders are generally more sophisticated in their approach to speech encoding, more powerful processing is required, which results in typically more expensive implementations and longer throughput processing delays. Also, vocoders do not, in general, encode non-speech signals with the same quality as a waveform encoder. Some commonly used vocoder algorithms include "linear predictive coding" (LPC), "residual excited LPC" (RELP), "vector sum excited LPC" (VSELP), and "codebook excited LPC" (CELP). Figure 2 illustrates a general comparison of data rate and speech quality for vocoder and waveform coding technology.

Selecting a Speech Encoding Technology

Given the diverse capabilities and limitations of both waveform coders and vocoders, how do designers go about selecting the right solution for their systems? There are a number of characteristics and parameters that should be included in this decision process, including:

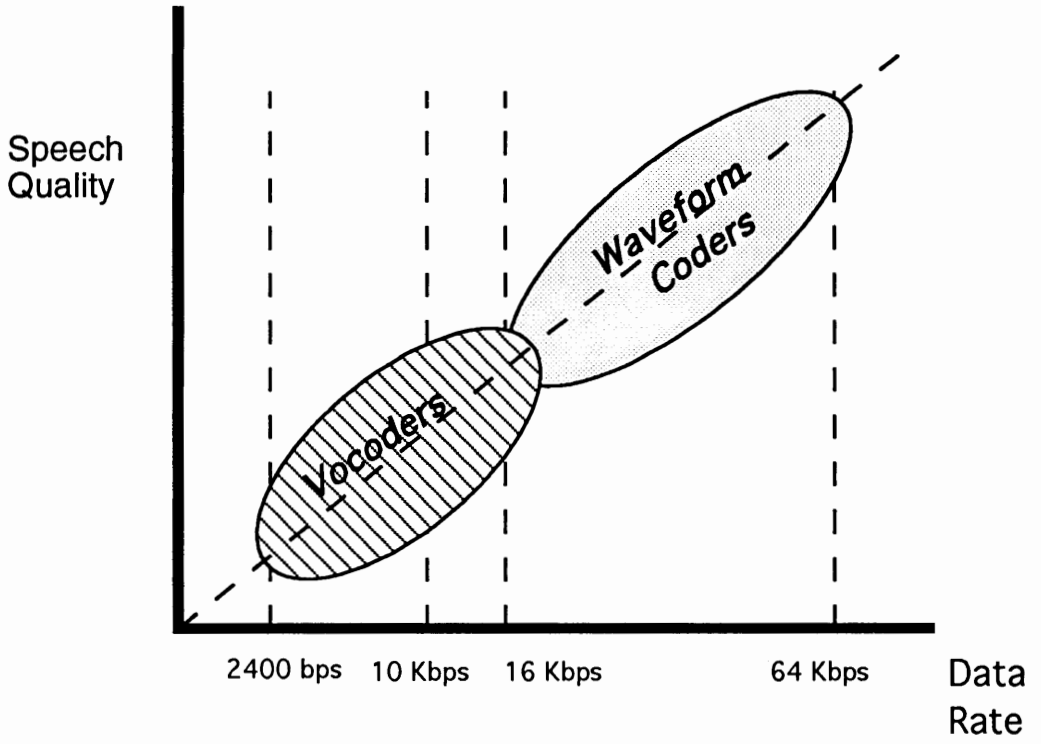

Figure 2: Speech Quality vs. Data Rate for Waveform Coders and Vocoders

1.) *Speech Quality:* Speech quality is measured in several ways, usually with subjective testing which compares the encoder being tested to some standard comparison system. "Speech quality" includes consideration of the ability of the encoding system to provide good speaker recognition, intelligibility of words, and general acceptability. Speech quality may vary for a given system between male and female voices, different languages or dialects, and performance in the presence of more complex audio signals such as multiple speakers or in the presence of background noise, such as street noise.

2.) *Encoded Data Rate:* The data rate compression factor is an important aspect of voice coding system selection. Differing system requirements dictate different level of compression. Increased speech quality with decreased encoding data rates are the two major conflicting system requirements in many systems.

3.) *Processing Delay:* The amount of time (measured in milliseconds) required for encoding and subsequent decoding of the voice signal can be an important design criteria, especially in systems where real-time two-way communications are required. In other systems, such as voice mail or broadcast voice transmission, minimizing the throughput delay is not as critical to the system overall performance. One-way processing delays of less than about 100 msec. are usually acceptable for two-way communications.

4.) *Ability to Process "Non-Voice" Signals:* Today's telephone system is required to process more than just speech signals. The use of telephones and similar systems for transmission of data, tone signaling, and faxes requires voice coding functions in such systems to either process these non-voice signals or at least to detect their presence and provide an alternative transmission routing.

5.) *Cost/Size/Power Requirements:* In a practical world, the voice coding system must meet the tangible constraints of cost, size, and power requirements. The complexity of the processing required for a particular voice coding scheme determines the computing power requirements (usually referred to in terms of millions of instructions per second (MIPS)). More complex processing usually results in higher cost, size, and power consumption. Fortunately, the evolution in increasingly powerful DSP processors with lower cost, size, and power continues at a fast rate. As a result, very complex voice coding systems which were not practical even a few years ago are now available and cost effective.

Of all these contributing factors to the selection of a voice coding system, the most important are typically 1.) speech quality, 2.) data rate compression ratio, and 3.) cost. The particular order of importance depends on the requirements of the specific system.

When the combined requirements of good voice quality and data rates below 10 Kbps are necessary, vocoder technology is the most appropriate choice for voice coding. Modern vocoders are available in single-chip VLSI-based DSP implementations. Some of these require less than 0.5 Watts of power to operate and provide near-toll quality speech encoding at data rates of 8 Kbps or less. The price of such vocoders is still typically twice as high as the price of a comparable quality waveform coder, but the data compression ratio is also better by about a factor of about three.

Variable Rate Vocoding

If vocoder technology is appropriate for a particular system design, it is important to select a vocoder which gives maximum performance at a minimal cost. Given that the voice compression ratio is an important selection criteria, a vocoder technology which minimizes the compressed speech rate while maintaining high quality is very useful. As previously mentioned, a "vocoder" is able to compress voice with high quality results because it attempts to model the human speech tract. Therefore, the extra "knowledge" the vocoder has about human speech generation provides greater efficiency.

One characteristic of human speech is that it is not a continuous process (at least not for most people!) There are pauses between words and sentences, as well as pauses for breathing and for listening to another speaker (in the case of two-way conversations). Obviously, during such periods of silence or near-silence the data rate required to accurately portray the speech signal is not as high as during

active talking periods. A vocoder that can recognize these periods and reduce the encoded data rate during these times will provide greater average data rate compression efficiencies.

Simple techniques for reducing the data rate during periods of silence involve actually stopping the transmission of encoded voice during these periods. While this technique does result in a lower average data rate for encoding, the abrupt transitions from fully encoded speech to complete silence can be very disruptive to the listener. Because such systems cannot perfectly predict the end of speech segments or the start of new segments, the beginning of new speech segments are often truncated or clipped. Also, it is quite unnatural for a listener to hear complete silence between segments of speech. In an uncompressed voice transmission system, some level of background sounds are constantly being heard even when the speaker has stopped talking. To attempt to offset this, some voice coding systems inject artificially generated "comfort noise" at the receiver when actual voice is not being encoded. However, the mismatch of the levels and characteristics of the actual background sounds (during speech) and the artificial comfort noise does not create a natural effect on the listener's ear.

A more sophisticated method for taking advantage of these periods is one that automatically adjusts the coding rate of the vocoder at a frequent rate. The coding rate is optimized for a particular short period of time. A new algorithm called "QUALCOMM Codebook Excited LPC" (QCELP) provides this type of intelligent vocoding. This algorithm, developed by QUALCOMM Incorporated of San Diego, California, is an enhanced version of the basic CELP vocoding approach.

The QCELP encoder partitions uncoded speech into frames which are 20 msec in duration. The QCELP algorithm performs a variable coding rate determination process and decides whether to encode each frame at one of several data rates, ranging from a low of 800 bps to a high of 9600 bps. During periods of silence, the QCELP encoder operates at a rate of only 800 bps. This very low data rate is useful for transmission of actual encoded background noise. Also, certain long-term voice parameters are continually updated when operating at this low rate. When speech resumes, the vocoder selects a higher rate for vocoding. The selected data rate is determined by the speech energy in each frame. As embodied in the QUALCOMM Q4400 single-chip QCELP vocoder device, the QCELP algorithm selects from one of three possible encoding rates for each frame. The sets of available rates are user selectable to be either 800/4000/8000 bps or 800/4800/9600 bps.

Using the QCELP algorithm, the average encoded rate for typical "constant talk" speech encoding is about 7,000 bps while maintaining near toll quality speech. Even greater efficiency is achieved when the vocoder is used in a two-way "full duplex" conversation mode, such as during a telephone call. In this case, during the period of time when the local party is listening to the remote speaker, the voice encoder is using only the lowest, 800 bps, coding rate. During such two-way conversations, the average transmitted voice coding rate is about 3.5 Kbps while still maintaining near toll quality.

An interesting aspect of the QCELP algorithm is its ability to automatically adjust thresholds to "filter out" undesired background noise when performing speech encoding. This is due to the fact that the speech energy measurement thresholds used to determine the encoder data rate are automatically adjusted over time. In the presence of high background noise levels, such as when using a cellular phone in the presence of high levels of "street noise", the QCELP encoder automatically shifts the rate determination thresholds to a higher level. Therefore, the high background noise is encoded at lower coding rates. The effect to the listener is an attenuation in the levels of the background noise without reducing the quality or volume of the encoded speech.

As shown in Figure 3, the QCELP algorithm provides good speech quality at a low data rate. This makes the QCELP algorithm suitable for a range of practical applications.

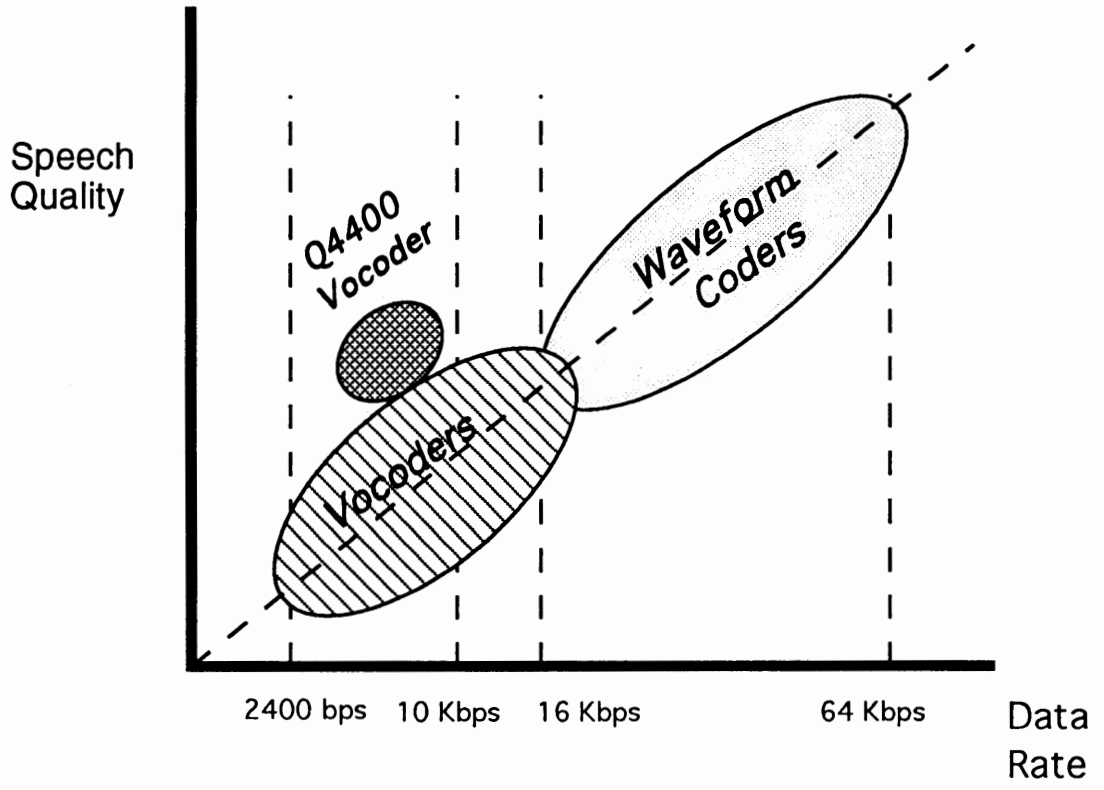

Figure 3: Q4400 Speech Quality and Data Rate Performance

The QCELP algorithm is currently under evaluation for standardization for use with the spread spectrum (CDMA) cellular phone system for the United States. Because of special inherent properties of spread spectrum communications, the decreased coding rate required for high quality cellular phone communication provide by QCELP directly increases the total call capacity of the cellular network. However, the special advantages of variable rate speech encoding are useful in a number of other system applications such as those listed in the following section.

Applications of Variable Rate Vocoding

VSAT and other SatCom Systems

A typical VSAT terminal might provide a 64 Kbps transmission data rate. If this channel is used for voice communications, a single 64 Kbps PCM voice signal may be transmitted from this station. If this same VSAT terminal uses a QCELP vocoder operating at a fixed rate of 8,000 bps it is easy to see that as many as eight voice circuits can be provided over this same channel. However, since most voice terminals are used for two-way telephone-like conversations (i.e., essentially half-duplex), the average data rate from the QCELP vocoder operating in variable-rate mode might be less than 3.5 Kbps. Even if one user is talking constantly and, therefore, requires the full data rate for vocoding, other users will probably not require full rate at any given moment. Therefore, a statistical multiplexing technique can be used resulting in the ability to carry as many as 16 voice circuits or more over the same terminal that could only handle a single PCM-encoded voice channel!

Voice Storage Systems

Voice mail and similar systems have become increasingly popular. In most voice mail systems the recorded messages are first digitized and then stored on a digital magnetic storage medium, such as a hard disk. Of course, the limit on how many minutes or hours of voice messages can be stored is determined by the size (in megabytes) of the storage media as well as the data rate of the encoded speech. Using the QCELP vocoder in variable rate mode, near toll quality speech is encoded at about 7 Kbps. This means that, for a given size hard disk, as many as nine times as many hours of speech can be recorded using QCELP-vocoded speech when compared to standard 64 Kbps speech digitizing. And, since only a few vocoder channels are actually required for even a large voice mail system, the cost for the advanced capabilities of the QCELP vocoder is minimal to the overall system.

Spread Spectrum Systems

The QCELP vocoding technique was initially developed for use in the QUALCOMM CDMA (spread spectrum) cellular telephone system. In spread spectrum systems, the limit on performance and capacity is directly related to the total number of "bits per second" being transmitted by all users at a given moment. If each user in a spread spectrum two-way voice communications system transmits only the average 3.5 Kbps data rate when using the QCELP vocoder, the total system capacity (in terms of the number of simultaneous users) is more than *double* that of the same system using a fixed rate 8 Kbps vocoder.

"Voice Over Data" Systems

An exciting new market is developing for data transmission systems that simultaneously transmit voice signals. An example of such a system is a baud-

rate telephone modem like those found in personal computers. While uploading a file between modems, or perhaps while playing a multi-player modem game, a voice conversation can also be held between people at either end of the link. This is also useful for multi-media networks where computer information is conveyed via phone modem while a voice conversation is also being held. Videophones are examples of transmission of simultaneous voice and "data" (in this case, digitized video signals) over a telephone. In each of these cases, it is desirable that the data rate of the voice signal be minimized to allow the maximum amount of data to be transmitted. QCELP vocoding not only is very efficient in its overall data rate requirement, but also allows the channel to be used almost totally to transmit data when speech is not present. The QCELP vocoder has the ability to limit the maximum speech rate to "half-rate" (either 4000 or 4800 bps) for short periods of time to allow short data transmissions to occur without interruption or degradation in the voice quality.

The Q4400 Single-Chip QCELP Vocoder System

QUALCOMM has implemented a full-duplex QCELP vocoder in a single DSP-based integrated circuit -- the Q4400 Variable Rate Vocoder. The Q4400 implements both encoding and decoding of voice signals which have been previously digitized using a standard off-the-shelf mu-Law PCM codec device. The Q4400 uses a standard 8-bit microprocessor bus interface to output speech samples which have been encoded by the QCELP encoder and to input previously encoded speech samples to be decoded by the QCELP decoder (refer to Figure 4).

The Q4400 provides several additional functions and features that are commonly required when using a voice coding system as shown in the block diagram of Figure 5. These features include built-in diagnostics, loopback modes, mute selection, and single or dual tone generation. The Q4400 also implements a useful VOX function which acts as an echo suppression capability. This is particularly useful for operation with a speakerphone or "hands free" cellular phone.

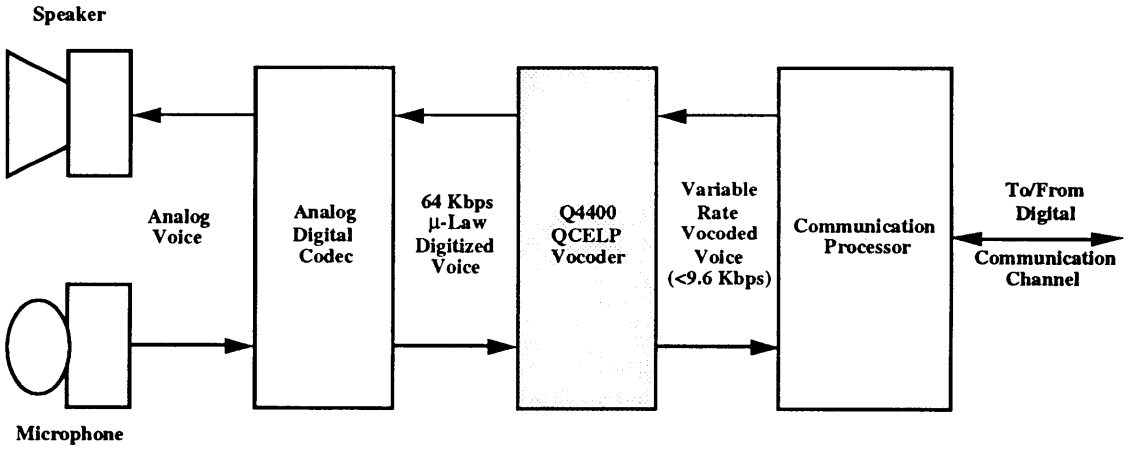

Figure 4: Q4400 Vocoder Typical Application

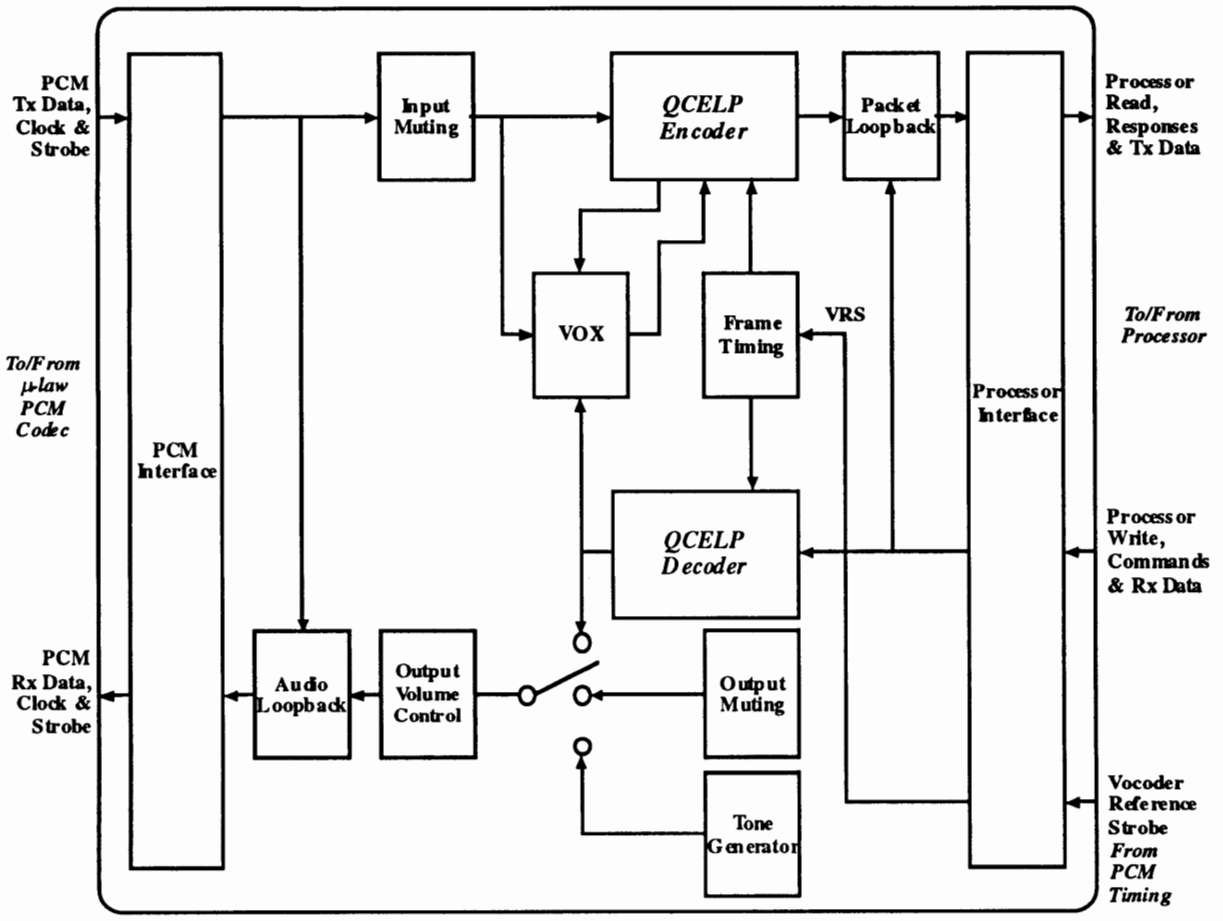

Figure 5: Q4400 Vocoder Functional Block Diagram

The encoding rate of the Q4400 is selectable to be a fixed rate of either 4000, 4800, 8000, or 9600 bps, or the automatically variable rate can be selected, using one of two data rate sets. The Q4400 decoder operates at a rate which is commanded to the decoder when a frame of data is transferred from the microprocessor controller.

The Q4400 is offered in a 100-pin PQFP package and requires less than 0.5 Watts of power from a single +5VDC supply. A 30 MHz clock signal or crystal controls the internal processing clock frequency.

Summary

As digital voice transmission and storage systems require greater speech compression rates while maintaining high speech quality, more "intelligent" vocoding algorithms must be developed. The QCELP algorithm is an excellent choice for systems that can take advantage of the unique ability to automatically determine the encoding data rate on a frequent basis. While maintaining speech

quality equivalent to a 9600 bps fixed rate vocoder, the QCELP algorithm encodes and decodes voice at an average data rate of less than 4 Kbps. The Q4400 single-chip vocoder implements the QCELP algorithm with user-selectable parameters and a variety of useful features. These attributes, along with the small size, low power requirement, and low cost of the Q4400, make this an ideal selection which meets the requirements for vocoding technology in many system applications.

Computer-Aided Engineering and PCN Components

Session Chairperson: Ray Pengelly, *Compact Software, Paterson, NJ*

SIMULATING DIGITAL RADIO PERFORMANCE USING THE HP MICROWAVE DESIGN SYSTEM

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(707) 577-2663.

Today we will be discussing ways to simulate digital radio performance using the HP High-Frequency Design System.

AGENDA

- Digital communications basics
- Important MDS capabilities
- A Case study: DQPSK Radio
  - -Transmitter performance
  - -Channel distortion and correction
  - -Receiver performance
- Summary

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First we will discuss the basics of digital communications systems, briefly discussing block diagrams, modulation formats, and common performance measurements. Next we will look at the features of the HP High-Frequency Design System that are especially important when analyzing digital systems. From there, we will discuss techniques to simulate transmitters, channel distortions, and receivers.

WHY THE MOVE TO DIGITAL COMMUNICATIONS

- Increased capacity for users
- More secure communications
- Additional services available
- Reduced fraud
- Common system across Europe

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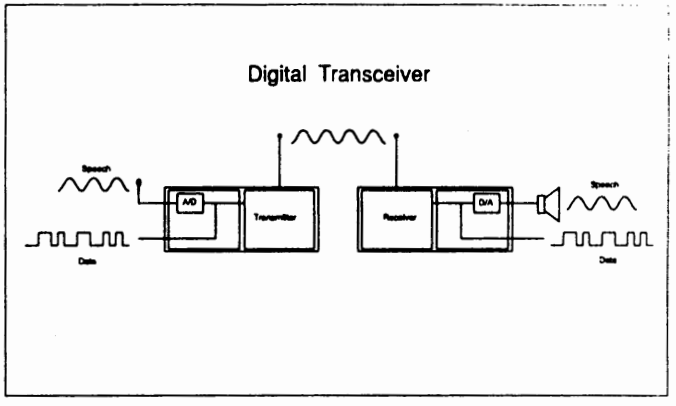
Digital modulation used in communication systems provide several benefits over analog. One of the primary benefits is the increase in capacity that can be gained by sending information in a digital format. Digital modulation also provides more secure communications than analog. With analog systems anyone with a frequency scanner can listen to a conversation. With digital systems the information is encoded and can have encryption added for even further security. Some digital modulation systems offer ISDN interconnect services. Any of the information available with an ISDN system would also be available over the communication link. So a user of a digital cellular phone would be able to transmit faxes, send/receive data files to/from his cellular phone, etc..

Another reason for the move to digital communications is to reduce the fraudulent use of cellular phones. Cellular service providers are losing millions of dollars every year to "pirated" cellular phones. These cellular phones are typically used by criminals. The calls are very hard to trace and provide good communications for the illegal operations.

Finally, a common cellular system is being implemented using digital modulation across Europe. Previously several different analog cellular systems were used by the different countries. This made it impossible for users to use their cellular phones as they crossed borders of countries. The new GSM digital cellular system will give users seamless phone coverage throughout Europe.

DIGITAL TRANSCEIVER



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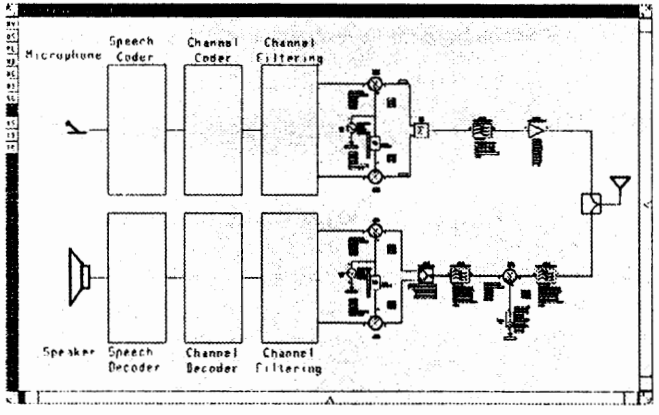
A digital transceiver transmits and receives voice on each end. However it converts the analog voice to data before modulating the carrier frequency. At a very basic level this can be done by using an analog to digital converter to digitize the voice, then send the data to the modulator of the transmitter. On the receiving end, the data is demodulated and run through a digital to analog converter to recover the original voice. Digital transceivers may also send and receive data directly between transmitters and receivers.

DIGITAL RADIO BLOCK DIAGRAM



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This is a generic digital radio block diagram. As can be seen the voice or audio is input to the microphone of the transmitter. The speech then goes through a speech coder. The primary purpose of the speech coder is to convert the audio into data and minimize the number of bits needed to represent the audio. The data then goes into a channel coder. The channel coder takes the voice data and adds additional data information that will be used by the receiver to recognize and reconstruct the transmitted signal. The channel coded data is then modulated onto an RF carrier, filtered (to reduce the bandwidth required to send the information) and pulsed out in "packets". On the receiving end, the pulsed carrier is received, filtered, and downconverted to an intermediate frequency (IF) which is again filtered and then demodulated. The data out of the demodulator is sent to the channel decoder to strip off channel coding information and then sent to the speech decoder to reconstruct the original speech.

CHANNEL FILTERING

- Needed to reduce occupied bandwidth of digital modulation
- Is applied to digital data stream before input to digital modulator
- Can cause intersymbol interference

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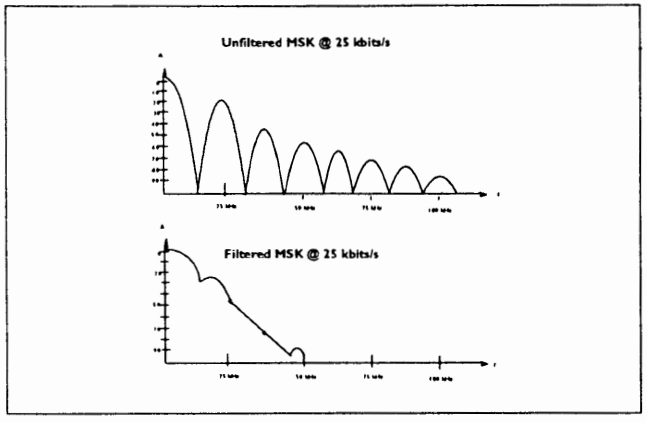
Once the digital information is channel coded, it is passed through a channel filter. Filtering allows more channels to be packed together, optimizing the use of airspace. The choice of the filter is very important, as it can easily introduce what is known as intersymbol interference. This interference degrades the performance of the radio by increasing the bit-error-rate (BER).

EFFECT OF FILTERING



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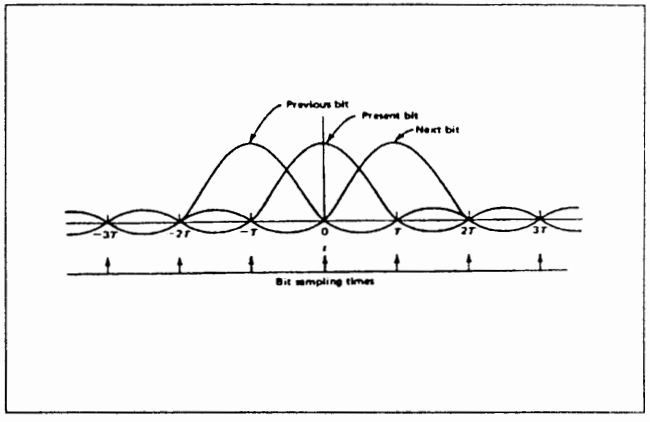
This slide graphically shows the effect of filtering the data. The top graph shows the single-sideband spectrum of a signal which has been MSK modulated by a 25 kbits/s data stream. Notice that although the modulation sidebands are -30 dB at a 30 kHz offset from the center frequency, the sidebands continue for many tens of kHz. The bottom graph is the same modulation and data rate, but the data stream has been filtered by a Gaussian low-pass filter (linear phase filter). Note the large improvement in modulation spectrum. Filtering allows digitally modulated signals to be used in cellular reuse patterns which do not interfere with each other.

NYQUIST FILTERING



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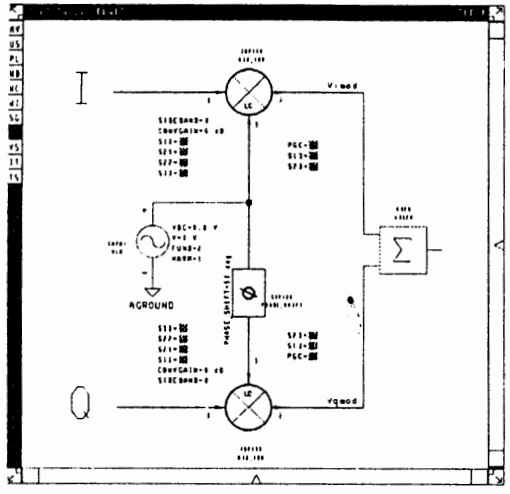
Shown here is an example of a perfectly filtered signal. Notice that this filter, as most, rings after a signal is applied. By carefully choosing the filter shape, the ringing crosses zero just as the next signal is sampled. If the filter's impulse response does not cross zero at the exact instant that the next signal is sampled, residuals from the previous bit will change the amplitude of the signal. This is intersymbol interference, one symbol interfering with another. Real filters will have significant ringing for as many as 5 to 10 cycles.

Digital radios are designed with filters that force the ringing to cross zero at the sampling point. This type of filter is known as a Nyquist filter. A commonly used implementation of a Nyquist filter is known as a raised-cosine filter. Typically, to make the radio symmetric, the filter is split into two square-root-raised-cosine filters, one applied to the transmitter and the other to the receiver.

MODULATION



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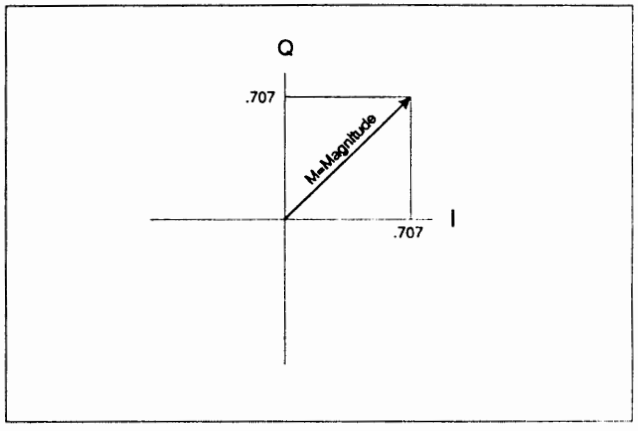
THE I/Q PLANE



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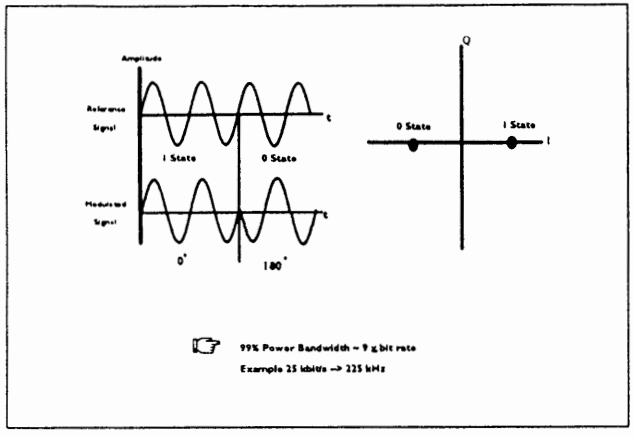
Once the voice information has been filtered, it is placed on a carrier through some type of modulation. Many modulation formats, such as amplitude-shift-key (ASK), frequency-shift-key (FSK), and phase-shift-key (PSK), are used in digital radios. Shown here is a basic I/Q modulator. The signal applied to the I channel controls the amplitude of the in-phase signal; the signal applied to the Q channel controls the magnitude of the quadrature signal.

A convenient way to look at modulation is to use the I/Q plane. This plane is a way to show both amplitude and phase information of the carrier. Digital modulation can use both phase and Amplitude to carry information. Let's look at a few basic types.

BPSK BI-PHASE SHIFT KEYING



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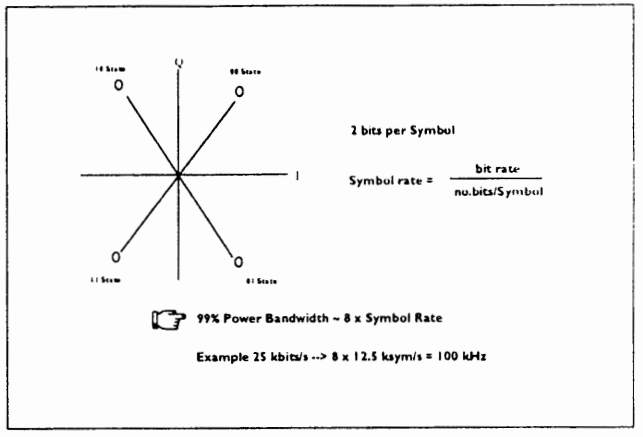
Bi-Phase Shift Keying is one of the simplest forms of digital modulation. For BPSK, the phase of the carrier is set to zero degrees when a binary one is applied to the modulator. When a binary zero is applied to the modulator, the carrier phase is set to 180 degrees. Displayed on the I/Q plane, BPSK appears as two points on the I axis which are 180 degrees apart. As can be seen from the amplitude graphs, the carrier flips its phase 180 degrees when a one to zero transition occurs. The relative simplicity of BPSK has some drawbacks, chiefly that it requires a large amount of bandwidth for a given data rate. As a rough rule of thumb, 99% of the power is a BPSK modulated carrier will occupy a bandwidth equal to 9 divided by one over the data rate period. For a 25 kbits/s data stream, BPSK would require 225 kHz of bandwidth. Clearly this bandwidth usage would eliminate the use of BPSK modulation for digital cellular applications. It is, however, used in satellite communications because of its high tolerance to noise.

QPSK QUADRATURE PHASE SHIFT KEYING



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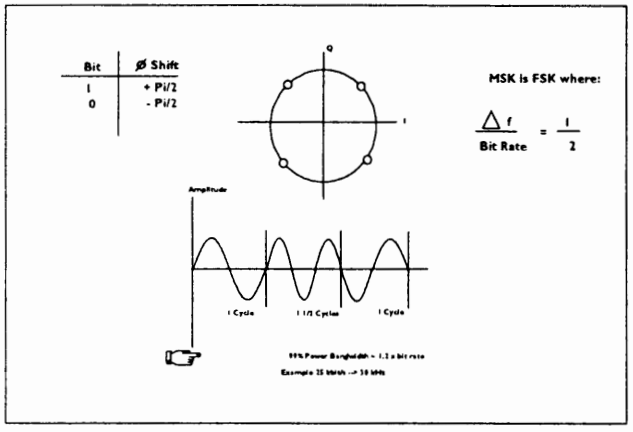
Quadrature Phase Shift Keying is a more complex digital modulation scheme which is derived from BPSK. Instead of having two phase states for the carrier, four phase states are used to represent the modulating digital data. On the I/Q plane, QPSK appears as four equally spaced points separated by 90 degrees. Since QPSK has four possible carrier phase states, it is possible to have each phase state represent two bits of data. This leads to a new term called the symbol rate. The symbol rate is defined as the bit rate divided by the number of bits per symbol. For QPSK there are two data bits for each symbol. Note that on the I/Q diagram each phase state is defined by two bits or one symbol. Because the symbol rate for QPSK is one-half the bit rate, more information can be carried in the same amount of bandwidth. As a rough rule of thumb, 99% of the power in a QPSK modulated carrier will occupy a bandwidth equal to 8 divided by one over the symbol rate. For a 25 kbits/s data stream, QPSK would require 100 kHz of bandwidth. This is much better performance than BPSK, but the reduced area between the modulation states means that bit errors are more likely for QPSK than BPSK for a given signal-to-noise ratio. The idea behind QPSK can be extended further to 16 states or even 64 Phase states. These modulation formats are far more efficient at the expense of the required signal-to-noise ratio to achieve the same bit-error-rate performance.

MSK MINIMUM SHIFT KEYING



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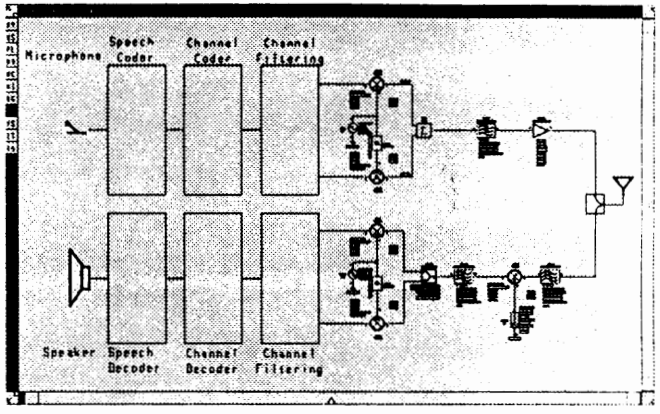
SUMMARY: THE DIGITAL RADIO



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Another possible digital modulation format is Frequency Shift Keying. Like BPSK, simple FSK involves shifting the carrier between two values, but uses frequency instead of phase. FSK is widely used for computer MODEMS and other digital transmission systems. For digital communications systems a popular modulation format is Minimum Shift Keying (MSK). MSK is a special form of FSK where the frequency shift is chosen to be exactly twice the data bit rate. It is called minimum shift keying because the frequency spacing between the two frequency states is the minimum spacing which allows the two frequency states to be orthogonal to each other. On the I/Q diagram, MSK appears to be a circle with a radius of one. Because the two frequency states are orthogonal, the frequency shift translates to either a +90 degree phase shift or a -90 degree phase shift (for either a one or zero data bit input to the modulator). Note on the amplitude versus time graph that MSK results in one cycle of the lower shift frequency and one and one-half cycles of the higher shift frequency. The main advantage of MSK is it's spectral efficiency. As a rough rule of thumb, 99% of the power in a MSK modulated carrier will occupy a bandwidth equal to 1.2 divided by one over the bit rate. For a 25 kbits/s data stream, MSK would require 30 kHz of bandwidth. This performance is far better than other modulation formats.

That ends the brief tour of a digital radio. In summary, a signal is received from a microphone, digitized, speech encoded, channel coded, filtered, and modulated. On the receiving end, the signal is demodulated, filtered, decoded, and delivered to the speaker.

AGENDA

- Digital communications basics
- Important MDS capabilities
- A Case study: DQPSK Radio
  - -Transmitter performance
  - -Channel distortion and correction
  - -Receiver performance
- Summary

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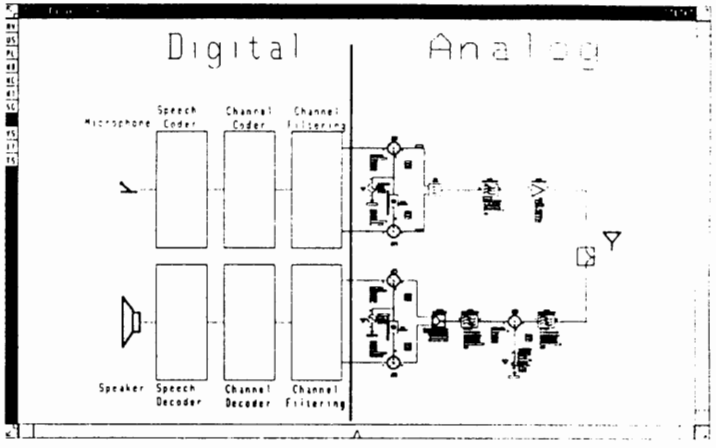
DIGITAL RADIO: DIGITAL vs. ANALOG



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Looking one more time at this block diagram, much of modern digital radios are implemented using Digital Signal Processing, or DSP, chips. The contribution of the HP High-Frequency Design System is in the analysis of the system from the output of the transmitter DSP to the input of the receiver DSP. Other simulation tools are available to analyze the DSPs.

So, the HP High-Frequency Design System takes the I and Q outputs, and analyzes the channel performance up to the I and Q inputs on the receiver.

MDS SYSTEM COMPONENTS

- Mixers, filters, amplifiers, splitters, couplers, etc.
- User defined components
- Circuit level descriptions
- AM, PM, FM, QAM, π/4 QPSK, IQ modulators, demodulators
- Pseudo-random bit sequence generators
- Unlimited input sources and output monitors
- Sources specified using measured data

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The system model library comprises a large number of building blocks that make system analysis easy. Predefined mixers, filters, amps, along with switches, couplers, isolators, and the like make building the circuit easy. For elements where HFDS has no direct equivalent, designers can easily build up custom devices using a variety of linear and nonlinear equation-based elements. These custom elements are built directly on the screen, without any programming. Also, circuit level descriptions can be freely intermixed with system models.

Special elements for digital modulation are also included, ranging from square-root raised-cosine filters to QAM modulators. To simulate real-world environments, there is no limit to the number of sources that can be included in the system. Sources can be specified at 12 different fundamental frequencies and any harmonic combination of those frequencies. A pseudo-random bit sequence generator is included to test long data streams.

ANALYSIS CAPABILITIES

- Simulate linear or nonlinear systems
- Calculate noise through nonlinear systems
- Sweep component values
- Determine component sensitivities
- Optimize for best system performance
- Run Monte-Carlo statistical analysis
- Estimate system yield

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Once a system is defined, a variety of analyses can be done. Systems can be analyzed in either a linear or a nonlinear fashion. Individual component values, such as amplifier TOI or mixer conversion gain can be swept. System sensitivity to component values can be calculated. Performance can be optimized using the random, gradient, or hybrid optimizer. Monte-Carlo runs can be used to analyze or estimate system yield.

DATA PRESENTATION

- Eye diagrams
- Constellation plots
- Bit Error Rate computations
- Transmitter Occupied Bandwidth
- Modulated output power computation
- AM to AM and AM to PM calculation
- Open post-processor for custom calculations

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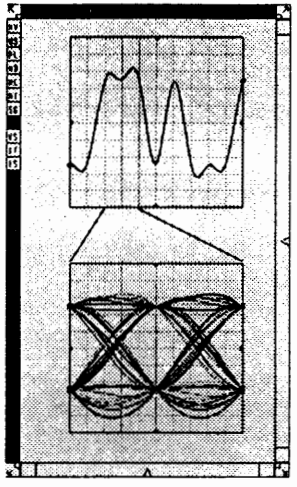
When analyzing digital radios, a variety of plots and calculations familiar to the digital system designer are available. Eye diagrams, constellation plots, and bit error rate curves are can all be displayed. Spectral regrowth, also called transmitter splatter, can be analyzed. Total modulated output power, AM-to-AM and AM-to-PM can be calculated. Using the built-in presentations functions, almost anything can be calculated.

EYE DIAGRAM



- Plot of I or Q versus time with bit intervals plotted on top of each other
- Clearly indicates sample points

"Open" eye is desired

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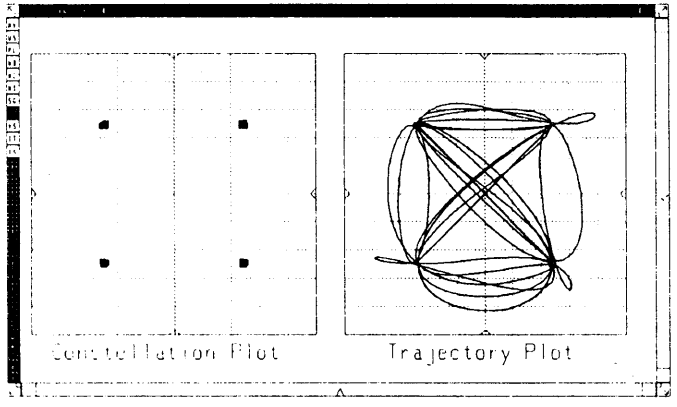
This slide shows an eye diagram and how it is created. It is actually a plot of the I or Q channel versus time, with successive bit intervals plotted on top of each other. Each 2-time sample interval is expanded and displayed.

CONSTELLATION PLOT



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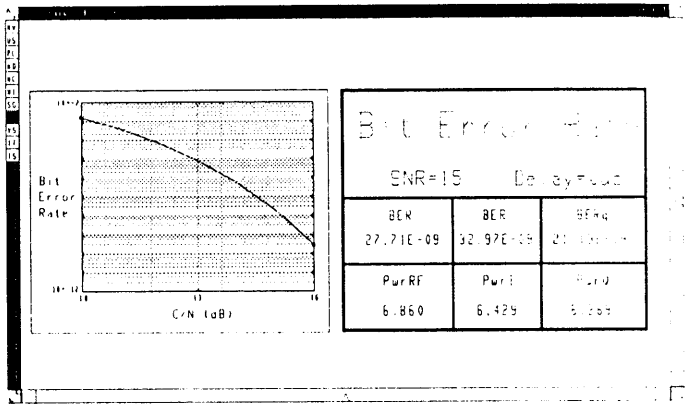
BIT ERROR RATE



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A constellation plot is just a plot in the I/Q plane. If the number of points displayed is equal to the number of time samples, a cluster of dots appear around each state. Ideal systems have all of the points aligned directly at the input data. The right plot is the same plot, however this time the trajectory of I versus Q is shown. This clearly illustrates how previous states affect the current state. Notice all of the different paths that are followed as the system traverses the -1,-1 to 1,1 state.

The ultimate test of radio performance is bit error rate. This is the single quantifiable measure of radio performance. Eye diagrams and constellation plots give insight into system performance, but the only real specification is how error-free are the bits at they are transmitted and received.

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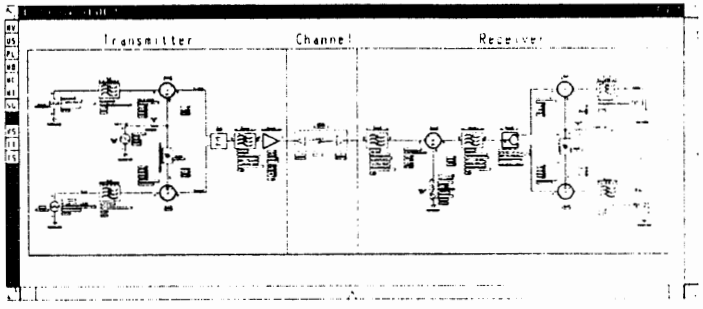
Now let's look at a specific radio and analyze how different errors in the design of the system affect system performance. The analysis is separated into transmitter, channel, and receiver tests.

THE RADIO



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For our example, we have chosen this radio, a DQPSK radio. Although the raised-cosine filtering is normally done by a DSP, here we have included it so that we can more closely analyze the system. The system is stimulated by two pulse train sources of definable length. Here we have made the length of the pulse sequence equal to eight, thus accounting for filter ringing effects for the previous eight bits. The I and Q data are filtered and modulated, amplified and filtered, distorted by the channel, amplified, filtered, down converted, demodulated, and finally filtered again. The output data is sampled at the two terminating resistors.

Note that no clock regeneration circuitry is shown. Most modern radios use DSP techniques to generate clock timing, so we are assuming that the clock recovery is not part of the analog circuitry and that is has been perfectly recovered by the DSP.

TRANSMITTER TESTS

- A perfect transmitter
- Quadrature errors
- Gain imbalance
- Output filtering
- Combined imperfections
- Transmitter occupied bandwidth

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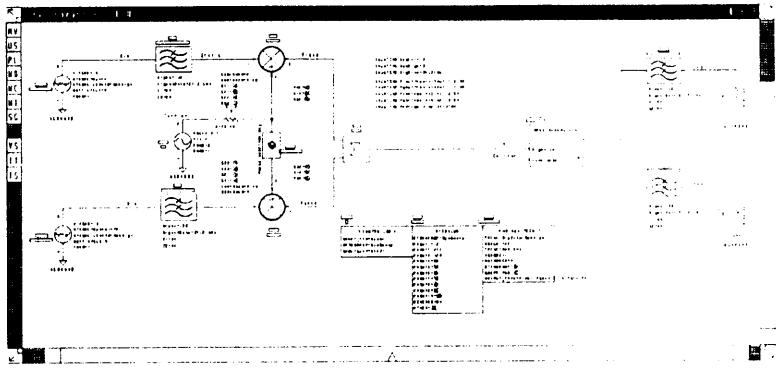
First we will examine the transmitter. For each set-up condition, the eye diagrams, constellation plot, and bit error rate will be shown. We start with a perfect transmitter, then sequentially introduce quadrature error, I/Q gain imbalance, output filters distortion, and output amplifier compression. Finally, the overall effects of this distortion are shown.

A PERFECT TRANSMITTER



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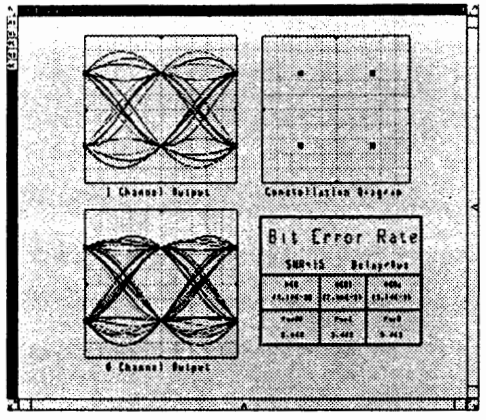
Here is a perfect transmitter. The filters are perfect raised cosine, the mixers are in perfect quadrature, the I/Q gain is balanced, and there is no output filtering or amplification.

PERFORMANCE:
THE PERFECT TRANSMITTER



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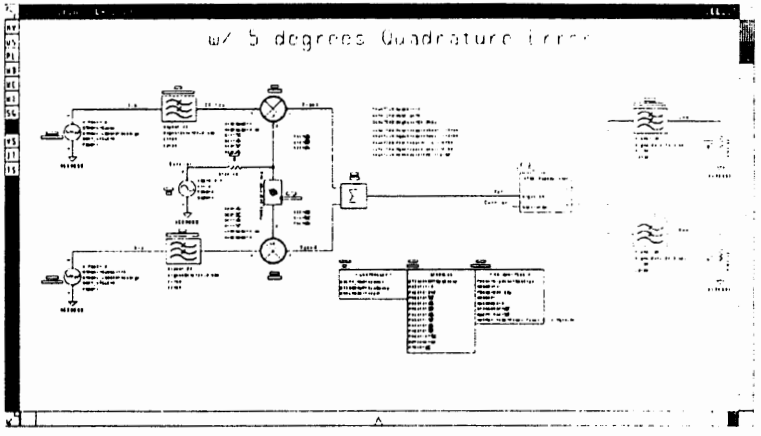
Here is the performance of the perfect transmitter. Notice that on the eye diagram the traces all cross at exactly the same point at the sampling instant. On the constellation plot, the input data and the output data lie on top of each other. The bit error rate for a 15 dB signal-to-noise ratio is at the theoretical minimum.

TRANSMITTER
QUADRATURE ERROR



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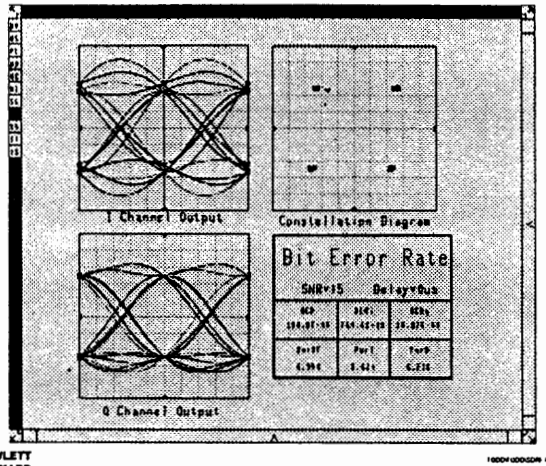
Now we take the perfect transmitter and introduce quadrature error. Note that the phase shift between the I and Q channel is now 85 degrees instead of 90 degrees.

PERFORMANCE: TRANSMITTER QUAD ERROR



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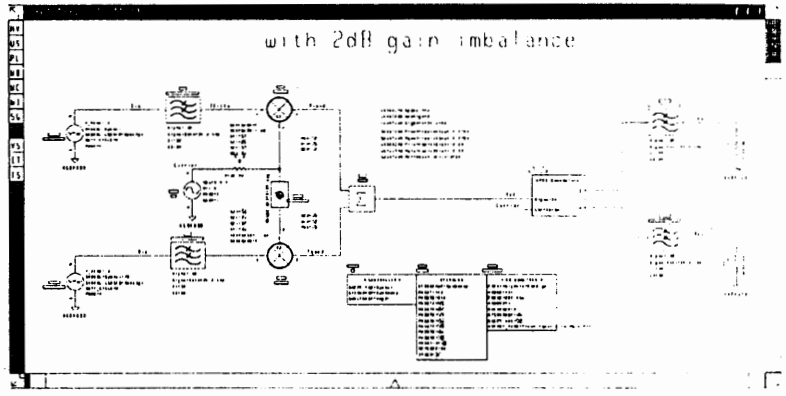
TRANSMITTER GAIN IMBALANCE



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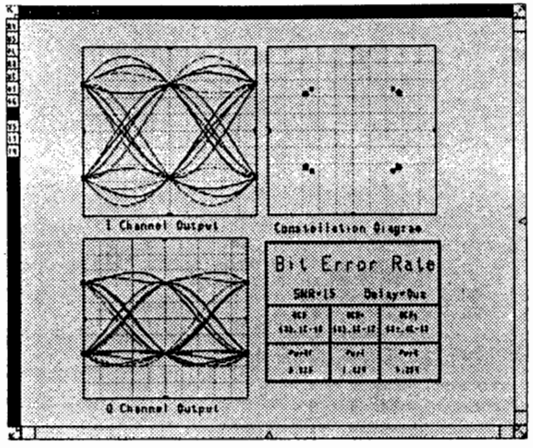
Notice now how the eye diagram has changed. The crossing is no longer as a single point. Also, the Q channel has dropped in amplitude as compared to the I channel. The quadrature error shows up most clearly on the constellation plot. The real effect, however, is seen in the bit error rate. Note that it has dropped in the I channel, but increased greatly in the Q channel. The overall RMS BER has increased from 21 x 10^{-9} to 188 x 10^{-9} an increase by a factor of nine.

This time we decrease the I channel gain by 1 dB and increase the Q channel gain by 1 dB

PERFORMANCE: TRANSMITTER GAIN IMBALANCE



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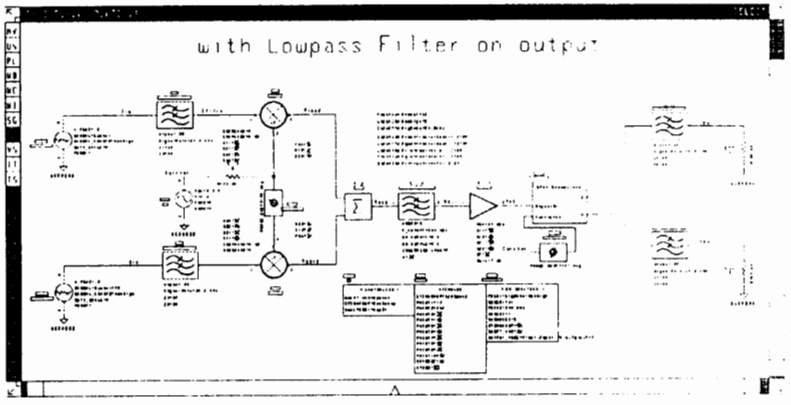
Again, the effects of the imperfect system are seen in the eye diagram and the constellation plot. The eye diagram clearly shows that the gain of the I channel is higher. This same effect is seen on the constellation diagram--the sample points are still nicely grouped, but they are shifted out and down. Interestingly, the BER of the I channel has dropped a lot, while the Q channel has increased. This indicates the great sensitivity of BER to signal-to-noise ratio--a 1 dB degradation of SNR degrades BER by a factor of 27.

TRANSMITTER OUTPUT FILTERING



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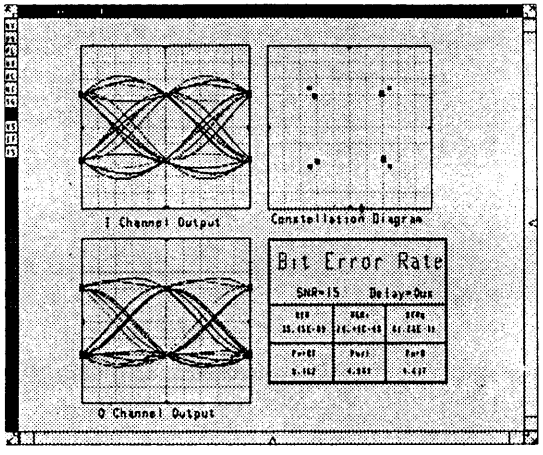
Now we will look at how a filter on the output of the transmitter effects system performance. Here we have placed a 5th order Chebychev lowpass filter that cuts off right at the edge of the transmit band. Note that a phase shift was added to the clock to account for the phase shift through the filter.

PERFORMANCE: TRANSMITTER OUTPUT FILTERING



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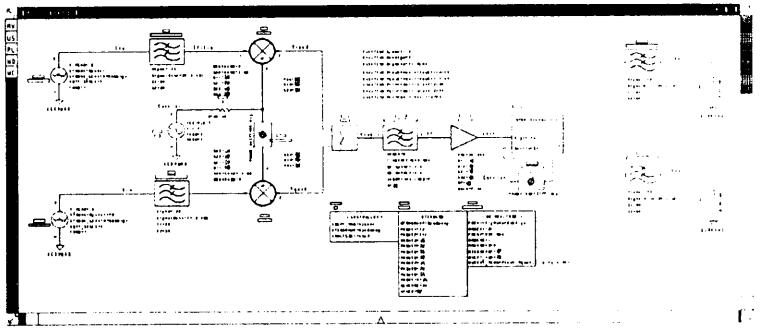
Looking at the eye diagrams, the effect of the output filtering is not immediately apparent--the eye shows just a little closure. The constellation diagram, however, shows clearly the effect of the filter--the filter has begun to roll off, decreasing the amplitude of the received signal. Because the roll off effects both channels, the SNR is equal for both channels, which drives the BER up by only a factor of two.

One effect that is not apparent from these diagrams is the phase shift, or delay, that is imposed on the signal. This delay has been compensated for by adjusting the phase of the clock as we saw on the previous slide. DSPs easily compensate for clock delay. Interestingly, the phase slope resulting from the filter is barely apparent. It is that phase slope that ever-so-slightly closes the eye.

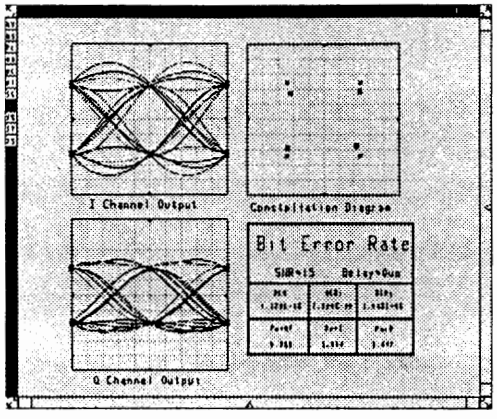
COMBINED TRANSMITTER IMPERFECTIONS



HEWLETT PACKARD

Pictured here is the radio with all three distortion mechanisms in place: quadrature error, gain imbalance, and output filtering.

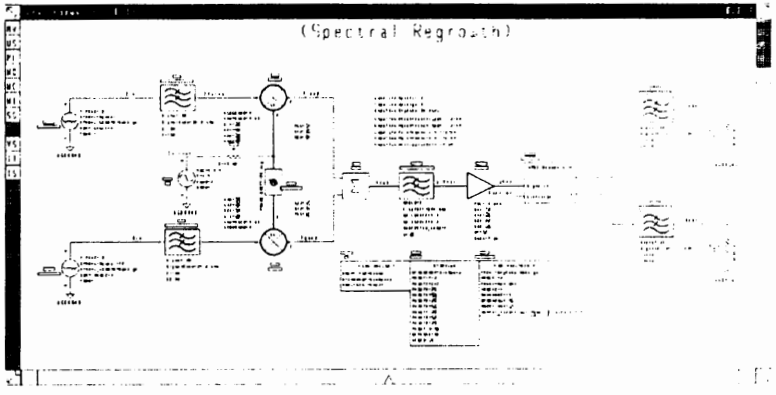
PERFORMANCE: COMBINED IMPERFECTIONS



HEWLETT PACKARD

Now let's look at the overall performance. The eye diagram shows the different amplitudes of the I and Q channels, and the eyes of each are partially closed. The constellation plot shows the overall distortion of the shifted quadrature and gain imbalance. Finally, the BER is 1.3 x 10^{-6}, a degradation by a factor of 60 from ideal--significantly worse than any of the individual contributors.

TRANSMITTER OCCUPIED BANDWIDTH



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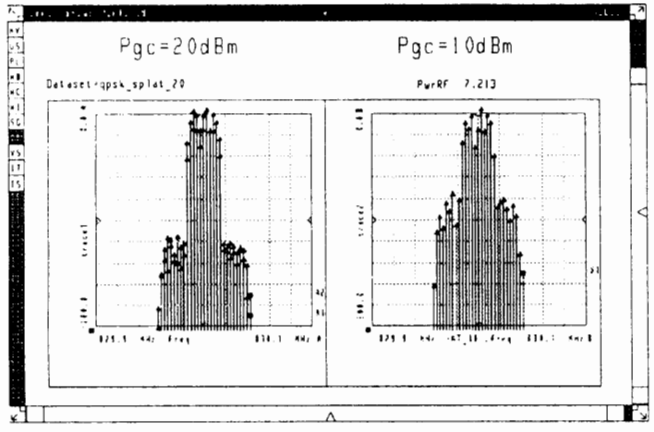
One final performance characteristic that we will examine is transmitter occupied bandwidth. Since communications systems try to pack as many channels together as possible, an important spec is how much bandwidth is used for a given channel. The Nyquist filter on the I and Q channels limits the bandwidth severely, but when the signal is passed through a nonlinear device, such as the output amplifier, intermodulation products give rise to sidebands outside the Nyquist filter limits. These products are known as transmitter splatter, the phenomenon is known as "spectral regrowth."

PERFORMANCE: TRANSMITTER BANDWIDTH



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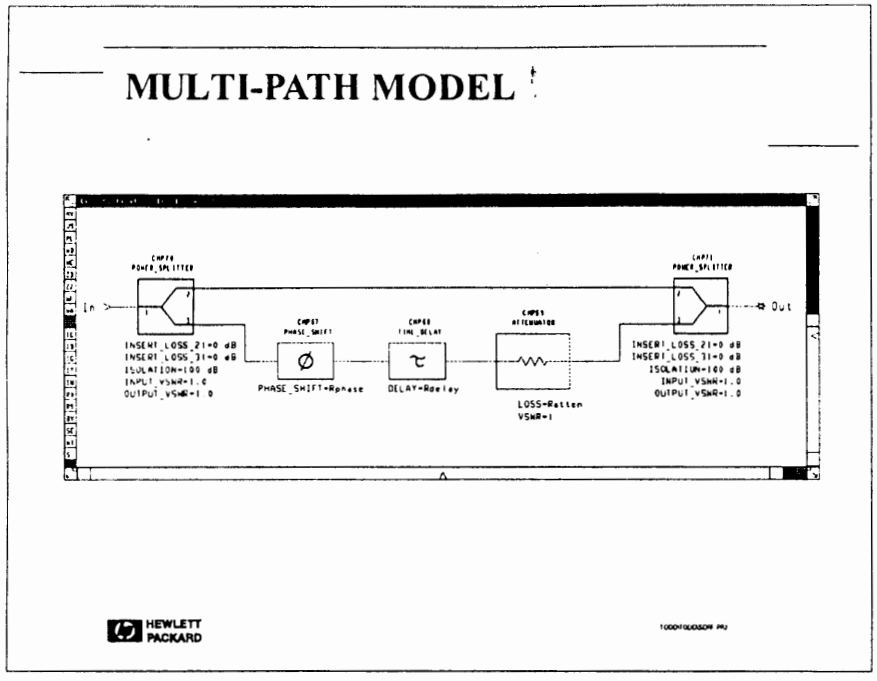
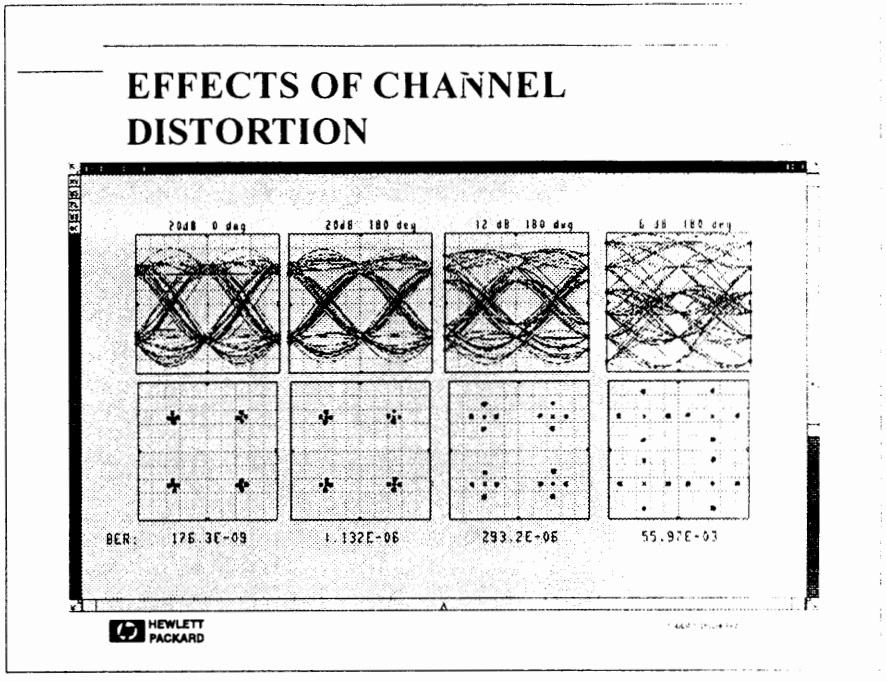
Here we see how the spectrum expands depending on the 1-dB compression level of the output amplifier. The two plots shown have an output signal level of 7 dBm. The plot on the left shows the output spectrum from an amplifier that has a 1-dB compression point at 20 dBm. The plot on the right shows the output spectrum from an amplifier that has a 1 dB-compression point at 10 dBm. Notice the spurious spectral lines have increased by about 20 dB. These plots help the designer to decide what compression characteristic the output amplifier must have to meet the occupied bandwidth specification.

AGENDA

- Digital communications basics
- Important MDS capabilities
- A Case study: DQPSK Radio
  - -Transmitter performance
  - -Channel distortion and correction
  - -Receiver performance
- Summary

HEWLETT PACKARD

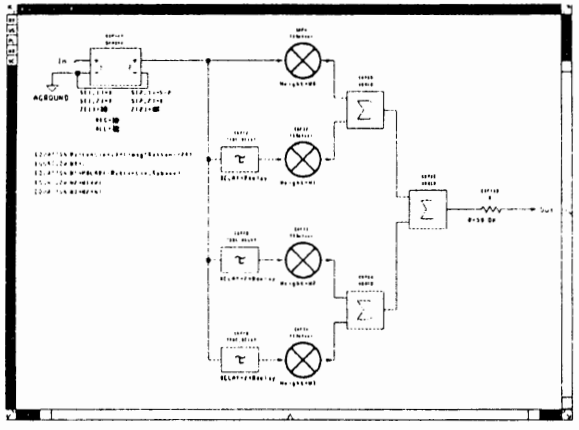




Now that we have looked at the transmitter, let's briefly look at how the transmit channel can add distortion to the signal. Probably the most common form of channel distortion is multi-path distortion. This diagram is a model of a transmitted signal as it follows a direct path and an indirect path from the transmitter to the receiver. The indirect path is formed as the signal reflects off of buildings, mountains, other cars, et cetera and arrives some time later at the receiver. Normally this reflected signal is attenuated from the direct path. The attenuation is modeled by the fixed attenuator. The delay can vary, but here is shown to be about one signal period. The incident phase is random; so here we will look at two cases, 0 and 180 degrees.

Shown here are the effects of varying degrees of interference. The leftmost picture shows an eye diagram, constellation plot, and the 15 dB C/N BER when the multi-path is attenuated 20 dB and there is no relative phase shift. The second column shows plots again with 20 dB attenuation, but this time 180 degrees of phase shift. Note that the relative phase has a dramatic effect on the BER, which is not immediately obvious from the eye diagram. Then we see the results with 12 dB and 6 dB attenuation. The eye closes a great deal. The constellation plot clearly shows the interfering signal as a set of points that are forming around the desired data points. If the phase were random, those points would form circles whose radius is equal to the magnitude of the multi path signal. These diagrams show the significant effect that multi-path has on digital radio performance.

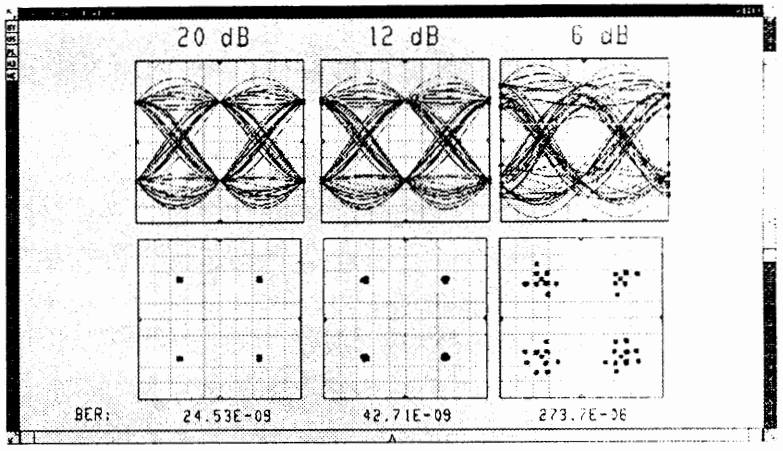
CHANNEL COMPENSATION: THE FIR FILTERS



HEWLETT PACKARD

Many digital systems are able to compensate for multi-path distortion using adaptive equalizers implemented as Finite-Impulse-Response (FIR) filters. Pictured here is a simple 4 stage filter that was designed to compensate for the specific multi-path distortion shown earlier. Although we will analyze them with fixed coefficients, modern systems are able to adjust the coefficients using training bursts and adaptive techniques.

PERFORMANCE: FIR COMPENSATION



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This slide clearly shows the benefit of using FIR filters. The filter coefficients were chosen to compensate for the multi-path distortion. Normally, the coefficients are dynamically adjusted to minimize BER. In this example, we assume knowledge of the multi-path attenuation and phase. All of these plots show dramatic improvement as compared to the performance without the FIR filter. With an interfering signal that is 20 dB down, the FIR filter is able to nearly perfectly correct for the distortion. The BER is almost at the theoretical minimum. It is less able to correct for the 12 dB, and even less the 6 dB. Nonetheless, the BER with the multi-path 6 dB has been improved by five orders of magnitude. Even better performance would be obtained by using more segments in the filter.

RECEIVER TESTS

- Quadrature, gain imbalance, filtering imperfections

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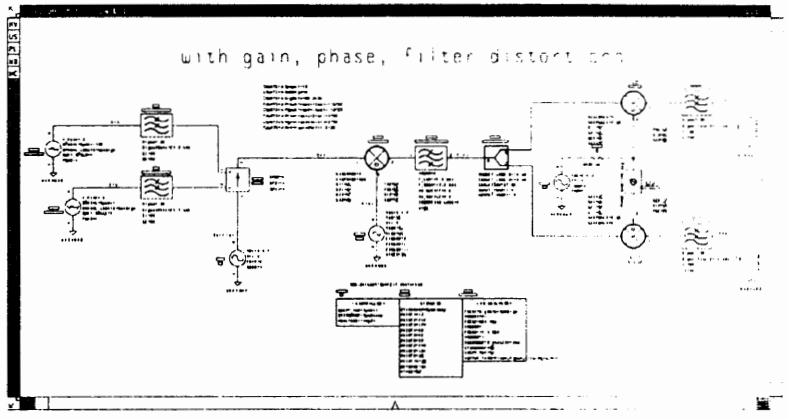
Finally, let's look at receiver performance. First we will look at the combined effects of quadrature error, gain imbalance, and filtering imperfections. The last test will be to look at the noise performance through the nonlinear portions of the receiver.

RECEIVER IMPERFECTIONS



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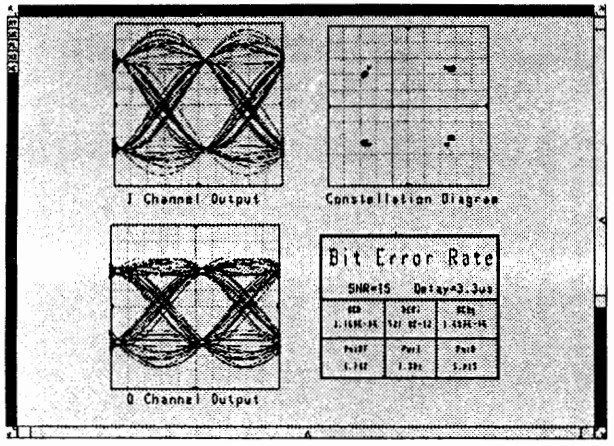
For the receiver we will look at the same distortions as in the transmitter, although we will look at them all together (to save time). The receiver is five degrees out of quadrature, the gain is imbalanced by 2 dB, and filters have been added on the input and the first IF.

PERFORMANCE: THE IMPERFECT RECEIVER



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Now let's look at the performance. Note that the eye diagram is not only distorted, it is shifted in time due to the filter delays, particularly the narrow first IF filter. The constellation plot and the bit error rates are degraded. Both used data points that were delayed by 3.3 us.

It is interesting that the I channel is nearly without distortion. The Q channel is attenuated, and the eye has collapsed significantly. The constellation plot shows the shift in quadrature and gain very clearly. The BER has degraded to 1.16×10^{-6}, 55 times worse than ideal.

SUMMARY

- Digital Radios
- MDS capabilites
- Transmitter tests
- Channel tests
- Receiver tests

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In summary, we have seen how the HP High-Frequency Design System is a complete tool for the system-level analysis of digital radios. It is able to calculate the key system performance specs for complete radios, including transmitters, channels, and receivers.

	CT-2	DCS-1800 (PCN)	DECT	Japan Digital Cordless Phone (JCT)
Geography	UK (Telepoint)	Europe	Europe	Japan
Service	1989	1992-1993	1992-1993	1991-1992
Frequency Range	864-868 MHz	1.7-1.9 GHz	1.88-1.9 GHz	1.9 GHz
Data Structure	TDD	TDMA	TDMA/TDD	TDMA/TDD
Channel per Frequency	1	8⇒16	12	4⇒8
Modulation	Two-level GFSK ±14.4-25.2 kHz deviation	0.3 GMSK	GFSK ±259-317 kHz deviation	π/4 DQPSK
Speech CODEC	ADPCM 32 Kbits/s	RELP-LTP 13 Kbits/s	ADPCM 32 Kbits/s	ADPCM 32 Kbits/s
Mobile Output Power	1 mW to 10 mW	250 mW to 2W	250 mW	10 mW
System Spectrum Allocation	4 MHz	75 MHz	20 MHz	20-25 MHz
Modulation Data Rate	72 Kbits/s	270.833 Kbits/s	1.152 Mbit/s	384 Kbits/s
Filter	0.5 Gaussian	0.3 Gaussian	0.5 Gaussian	√raised cosine
Channel Spacing	100 kHz	200 kHz	1.728 MHz	300 kHz
Number of Channels	40	3000 - 6000	132	
Estimated # of Subscribers year 2000				6.5-13 million
Source	MPT 1375 Common Air Interface (CAI)	prI-ETS 300 176 prETS 300 175-2	CI Spec Part 1 Rev 05.2c	

March 18, 1992

	GSM	NADC	JDC	CDMA
Geography	Europe	North America	Japan	U.S.
Service	1991	1991-1992	1991-1993	1992-1993?
Frequency Range	935-960 MHz 890-915 MHz	824-849 MHz 869-894 MHz	810-826 MHz 940-956 MHz 1429-1441 MHz 1447-1489 MHz 1453-1465 MHz 1501-1513 MHz	824-849 MHz 869-894 MHz
Data Structure	TDMA	TDMA	TDMA	CDMA
Channel per Frequency	8⇒16	3⇒6	3⇒6	118
Modulation	0.3 GMSK	π/4 DQPSK	π/4 DQPSK	BS/MS QPSK/OQPSK
Speech CODEC	RELP-LTP 13 Kbits/s	VSELP 8 Kbits/s	VSELP 8 Kbits/s	8550 bps
Mobile Output Power	3.7 mW to 20W	2.2 mW to 6W		2.2mW to 6W
System Spectrum Allocation	50 MHz	50 MHz	110 MHz	50 MHz
Modulation Data Rate	270.833 Kbits	48.6 Kbits	42 Kbits	1.2288 Mbits/s
Filter	0.3 Gaussian	√raised cosine	√raised cosine	
Channel Spacing	200 kHz	30 kHz	25 kHz	1.23 MHz
Number of Channels	124 frequency channels w/8 timeslots per channel (1000)	832 frequency channels w/3 users per channel (2496)	1600 frequency channels w/3 users per channel (4800)	10 channels 118 calls/channel
Estimated # of Subscribers year 2000	>20 million			
Source	GSM Standard	IS-54	RCR Spec	Qualcom

THE DESIGN OF LOW POWER CONSUMPTION RF CIRCUITS FOR DIGITAL EUROPEAN CORDLESS TELEPHONES USING MICROWAVE HARMONICA

by Raymond S. Pengelly
Vice President
Compact Software, Inc.
New Jersey, USA

Compact Software

Digital European Cordless Telephone

DCS 1800 System based on GSM 900

TDMA and FDMA combination

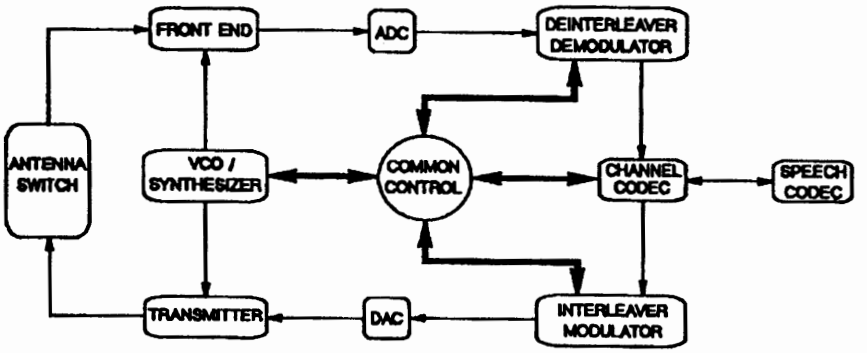
Mobile Station
Base Station
Mobile Switching Center

Using GaAs MMIC Technology

Designs for Low Current Consumption and High DC to RF Conversion Efficiency

Compact Software

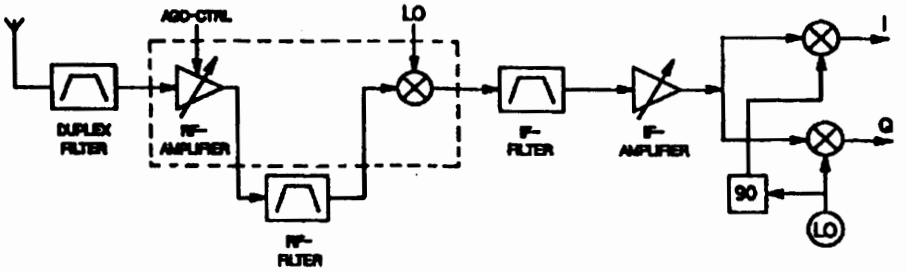
Digital European Cordless Telephone



Structure of DECT Mobile Station

Compact Software

Digital European Cordless Telephone



DECT Front End with GaAs MMIC Subsystem

Compact Software

Digital European Cordless Telephone

Subject:	SiBip- Technology	GaAs- Technology
Active Components	npn- Transistors	Depletion MESFETS Enhancem. MESFETS Schottky Diodes
Passive Components	Resistors (Capacitors)	Resistors Capacitors (Inductors) Lumped Elements
Maximum f_T	30 GHz	45 GHz
Minimum Noisefigure F	< 1 dB	< 3 dB
Suitability for analog	moderate	good
Suitability for digital	good	moderate
Reproducibility	good	bad
Production Efficiency	97 %	5 %
Production Costs	low	high

General Properties of Si BJT and GaAs Technologies

Compact Software

Digital European Cordless Telephone

Component	Frequency Range / GHz	Key Property	Possible Technology	Preferable Technology
LNA	1-3	low- noise	GaAs	GaAs
PRA	1-3	low- distortion	SiBip, GaAs	SiBip
HPA	1-3	power effic.	SiBip, GaAs-hybrid	SiBip hybrid
MPA	1-3	linearity	SiBip, GaAs	SiBip
VCO	2-6 (4-12)	stability, linear.	SiBip, GaAs	SiBip
PSC	2-6 (4-12)	low- power	SiBip, GaAs	SiBip
PSW	1-3	low- loss	GaAs	GaAs
RIM	1-3	uncritical	SiBip, GaAs	SiBip
TIM	1-3	low- sp. emiss.	SiBip, GaAs	SiBip
QDC	2-6 (4-12)	linearity	SiBip, GaAs	SiBip
QUC	2-6 (4-12)	gain/phase bal.	SiBip, GaAs	SiBip

Technologies for Specific RF Circuits for Mobile Communications

Compact Software

Simulation Requirements

Nonlinear Simulation needed for:

- ***System Gain***
- ***System Noise Figure***
- ***Compression***
- ***Dynamic Range***
- ***Third Order Intercept Point***
- ***Temperature Effects***
- ***Design Trade-Offs***

Digital European Cordless Telephone

Compact Software

Microwave Harmonica is a Harmonic Balance Simulator providing:

- * Efficient and Accurate Analysis
- * High Dynamic Range -- 140 dB
- * Optimization
- * Design Centering
- * Nonlinear Noise Analysis
- * Temperature Analysis

Microwave Harmonica uses a variety of nonlinear models as well as transistor libraries:

* Models need to be accurate particularly close to pinch-off and breakdown

* Models need to be consistent i.e.
  - Linear/Nonlinear
  - Spice syntax
  - Noise
  - Temperature Coefficients

Result of System Analysis

Stage	RF-Amplifier		Mixer		Front End	
F	4		12		23.30	
G_a	-5		15		SNR_o = 74.7	
$IP_{3,i}$	0		0 / 7		-4.3 / 1.8	
Stage	1	2	3	4	5	6
P_{out}	-26	-31	-34	-19	-29	-15
F	4		12		19.12	
G_a	0		10		SNR_o = 78.9	
$IP_{3,i}$	0		0 / 7		-4.8 / 0	
P_{out}	-26	-26	-29	-19	-29	-15
F	4		12		14.66	
G_a	5		10		SNR_o = 83	
$IP_{3,i}$	0		0 / 7		-9.8 / -5	
P_{out}	-26	-21	-24	-14	-24	-10
F	4		12		9.93	
G_a	12		10		SNR_o = 88.1	
$IP_{3,i}$	0		0 / 7		-16.8 / -12	
P_{out}	-26	-14	-17	-7	-17	-3

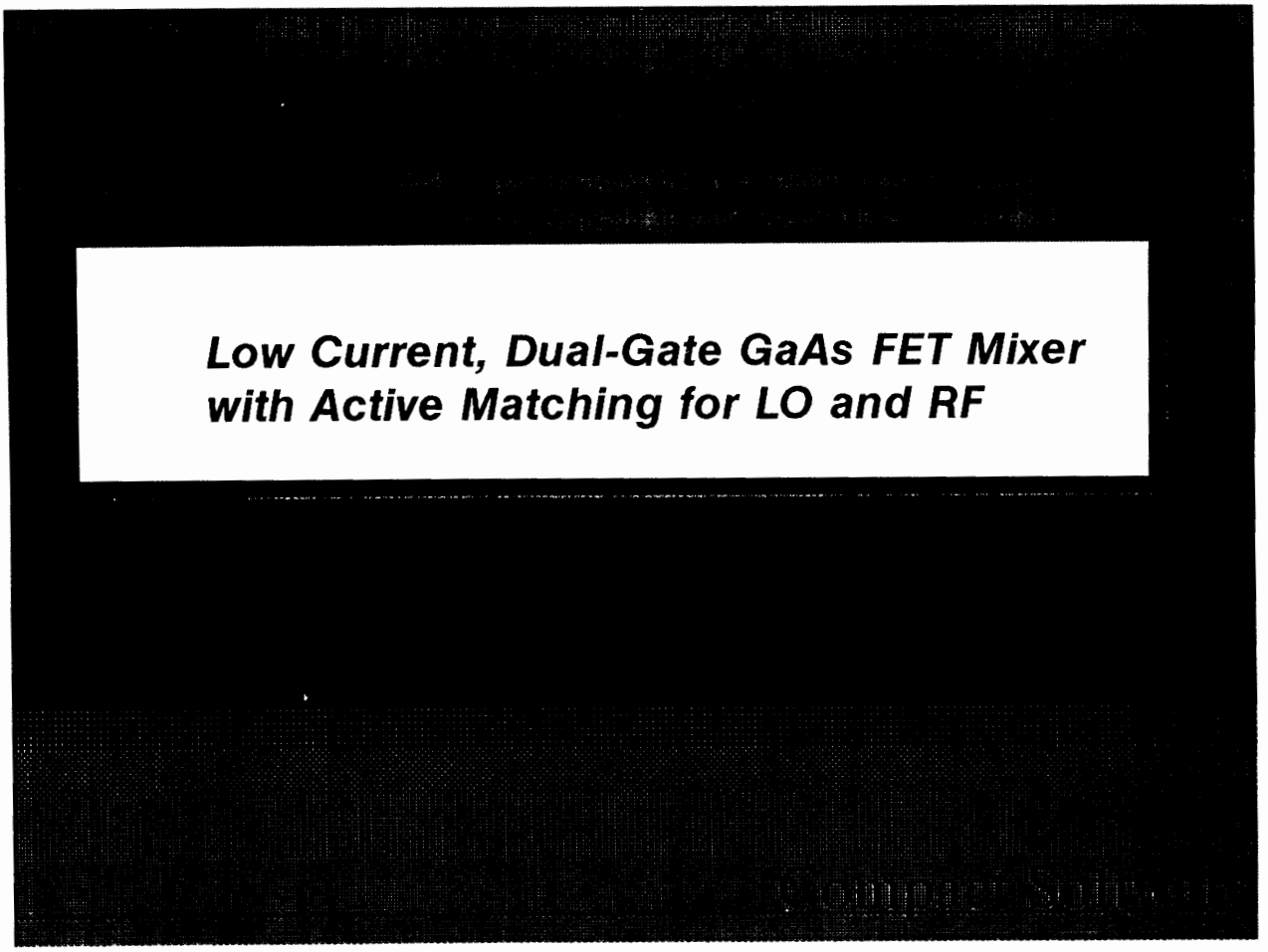
Digital European Cordless Telephone

Compact Software

Digital European Cordless Telephone

Mixer: RF-input impedance : 50 Ω
LO-input impedance : 50 Ω
IF-output impedance : 500 Ω
RF-frequency : 1805 - 1880 MHz
LO-frequency : 1935 - 2010 MHz
IF-frequency : 130 MHz
LO-input signal : > -10 dBm
Gain : 10 dB
Noise figure : ≤ 12 dB
$IP_{3,i}$: > 0 dBm

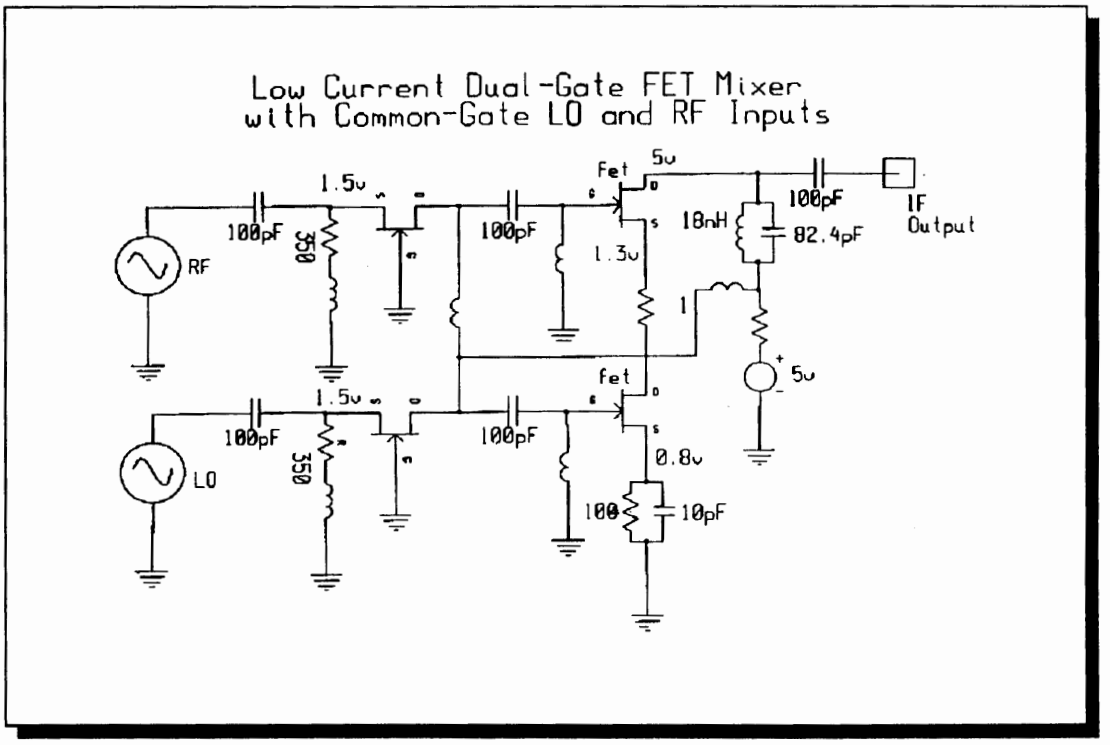
Compact Software



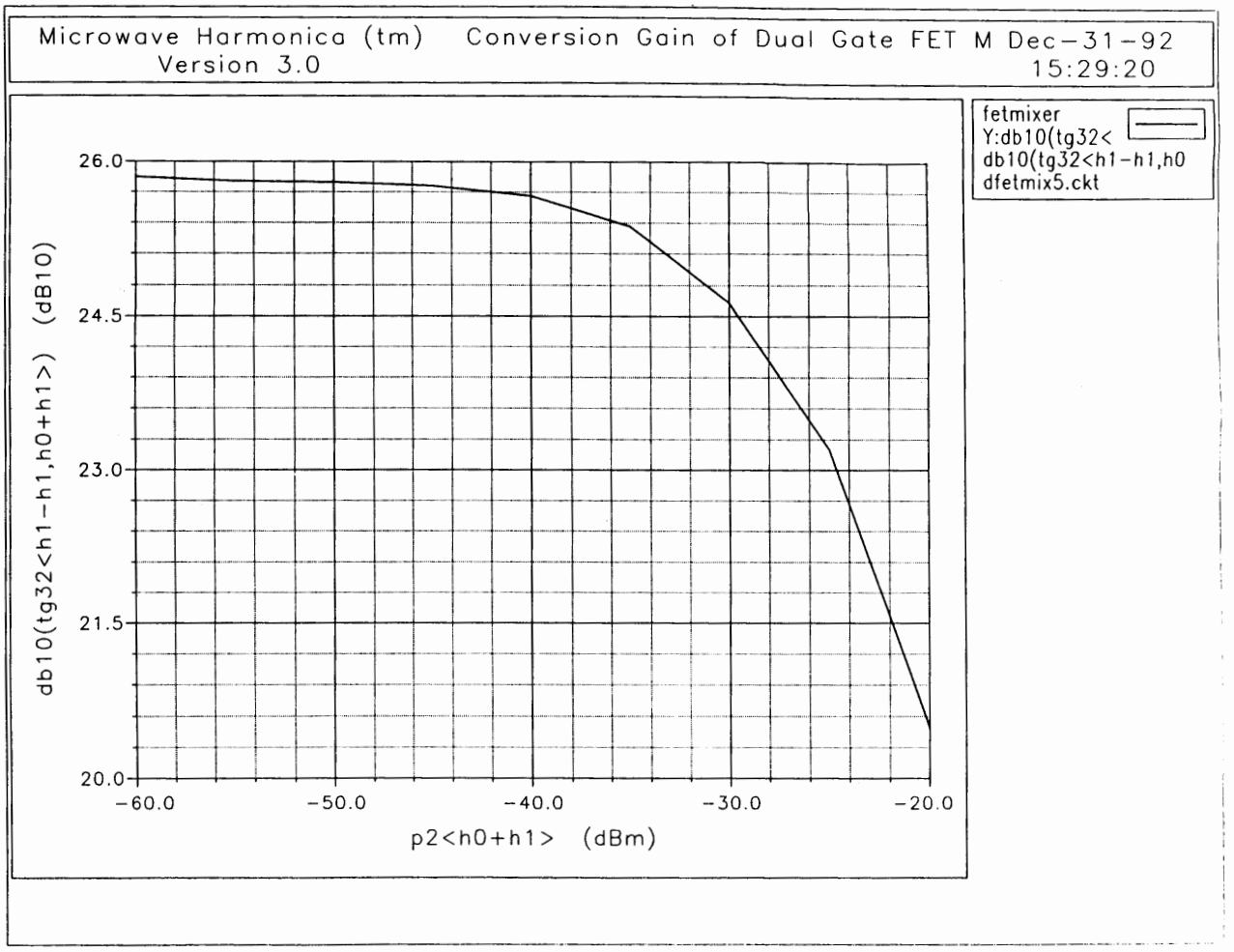
MIXER DESIGN

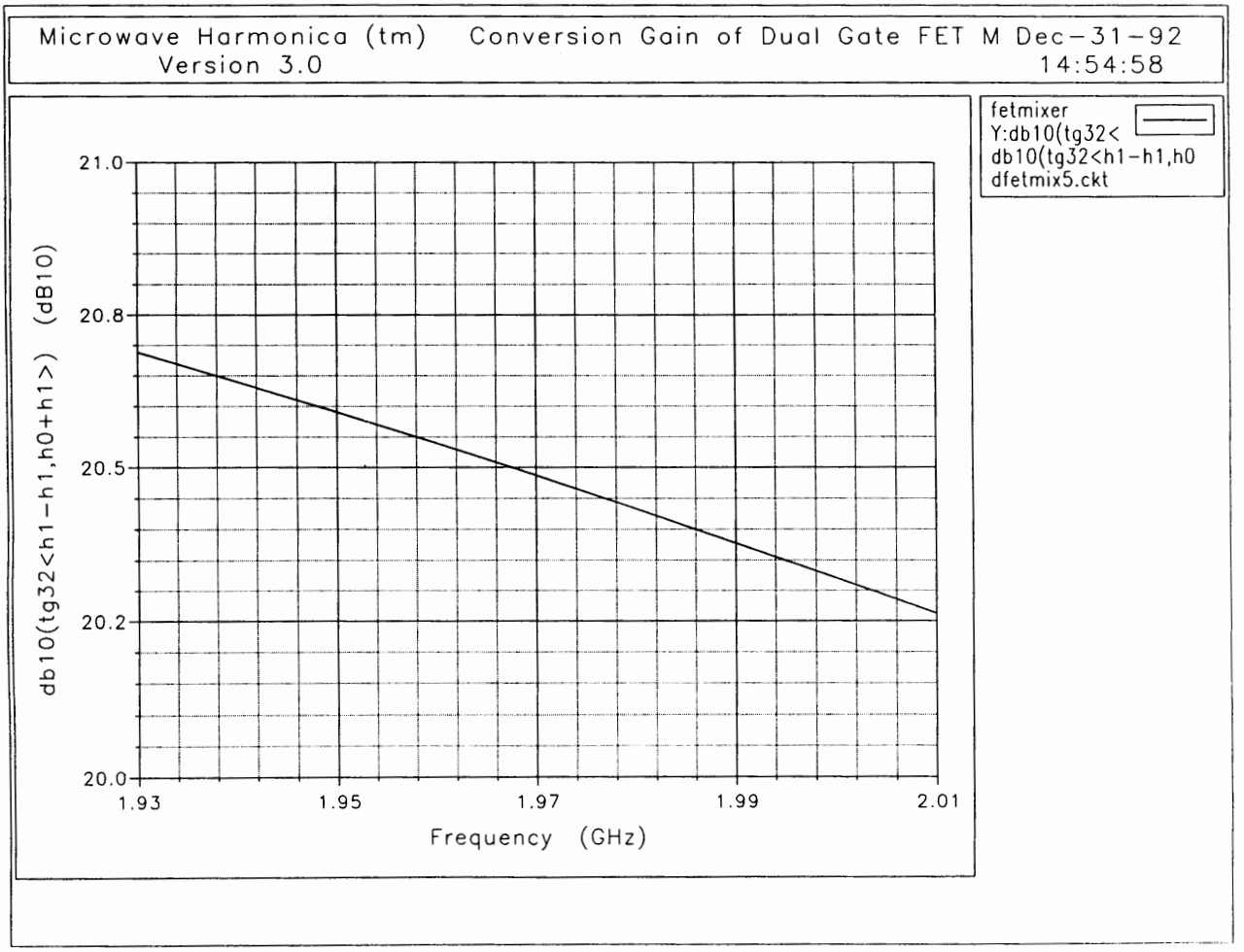
Operates from Single 3.5 volt Rail
Self-Biased
Low RF, LO and IF VSWRs
Low LO Power
Low Spurious Signal Leakage

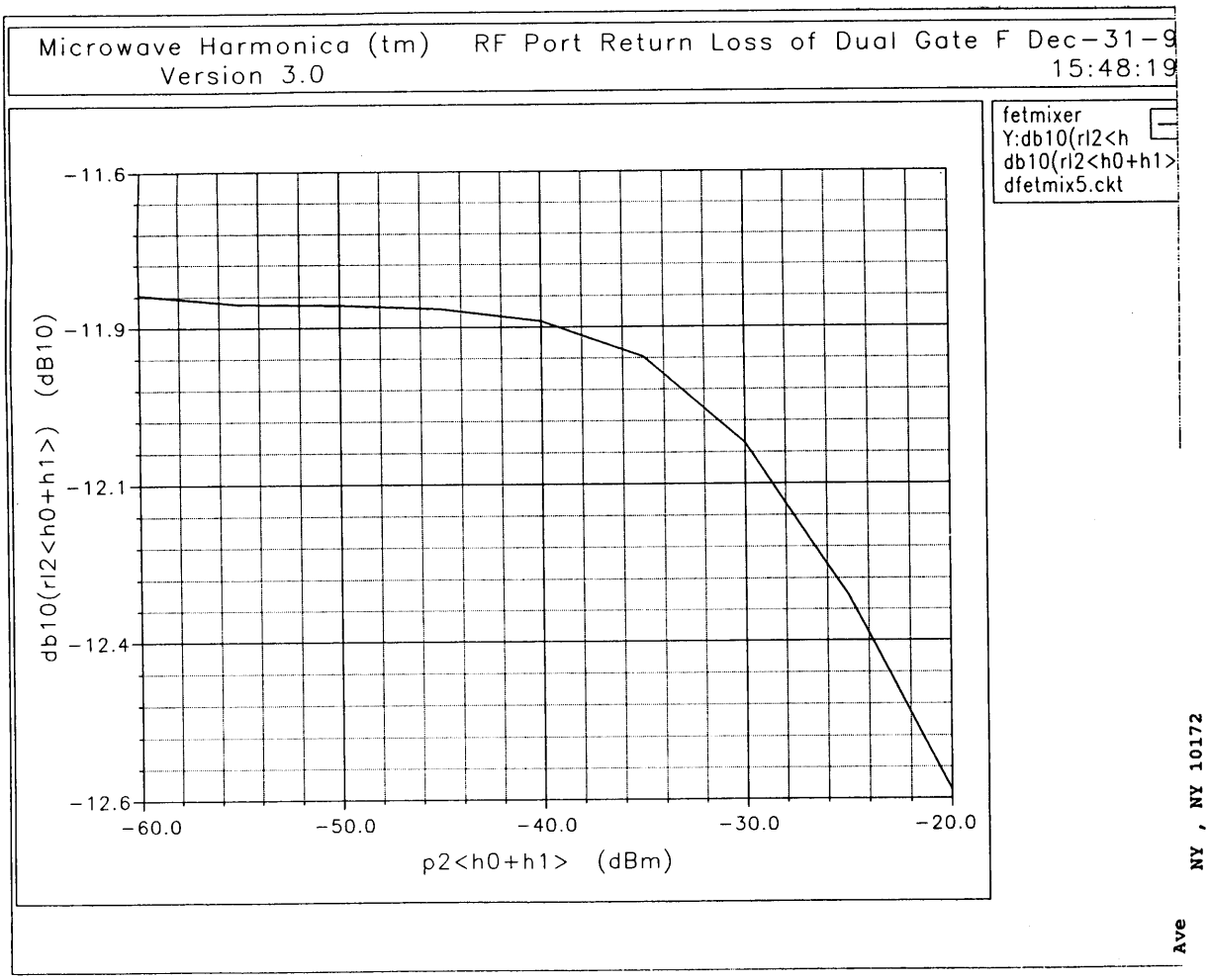
Two Common-Gate FETs and Dual-Gate FET
Materka Nonlinear Model used for FETs
Drain Current of Dual-gate FET is 8mA with an LO modulation of +/-2mA

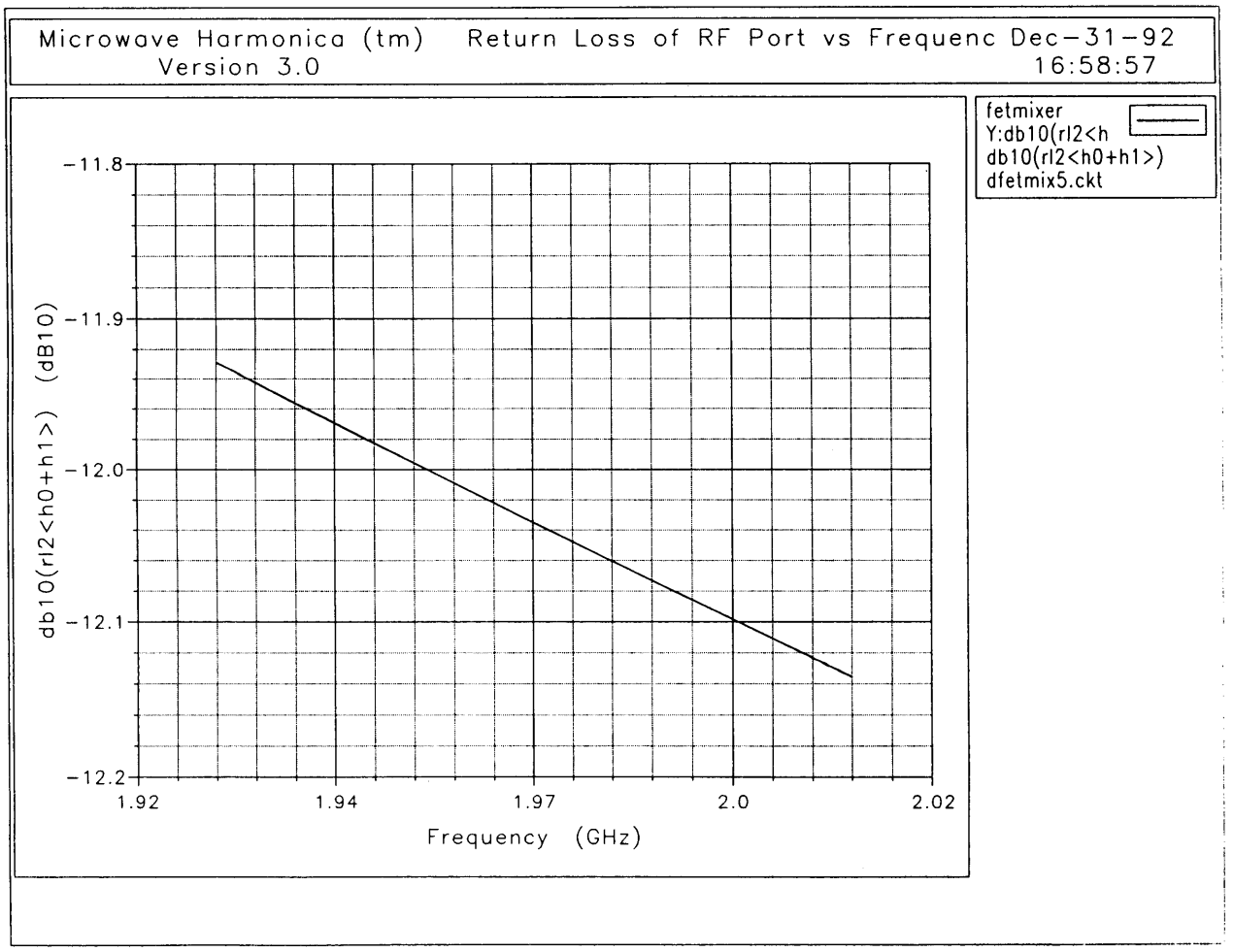


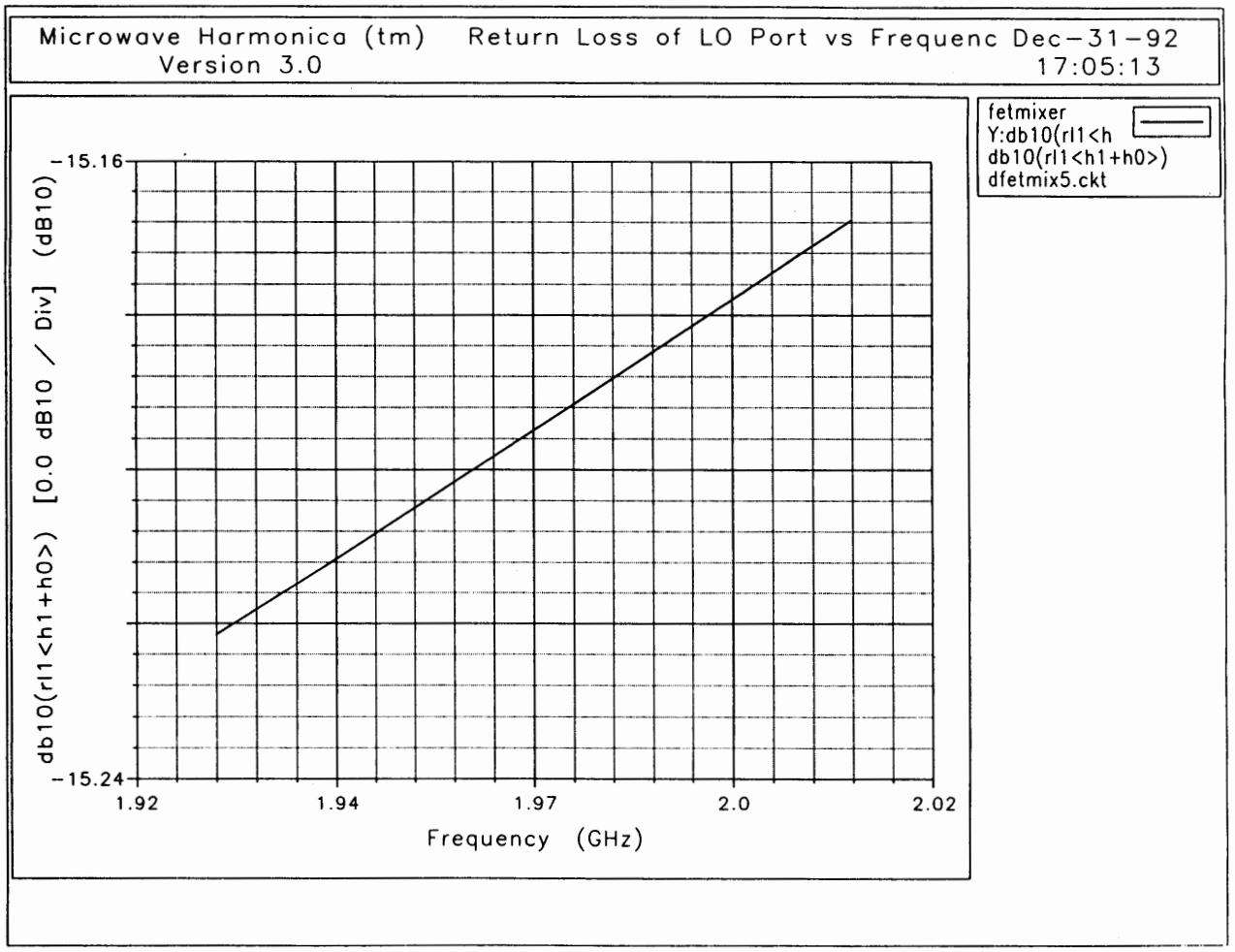
Digital European Cordless Telephone Compact Software

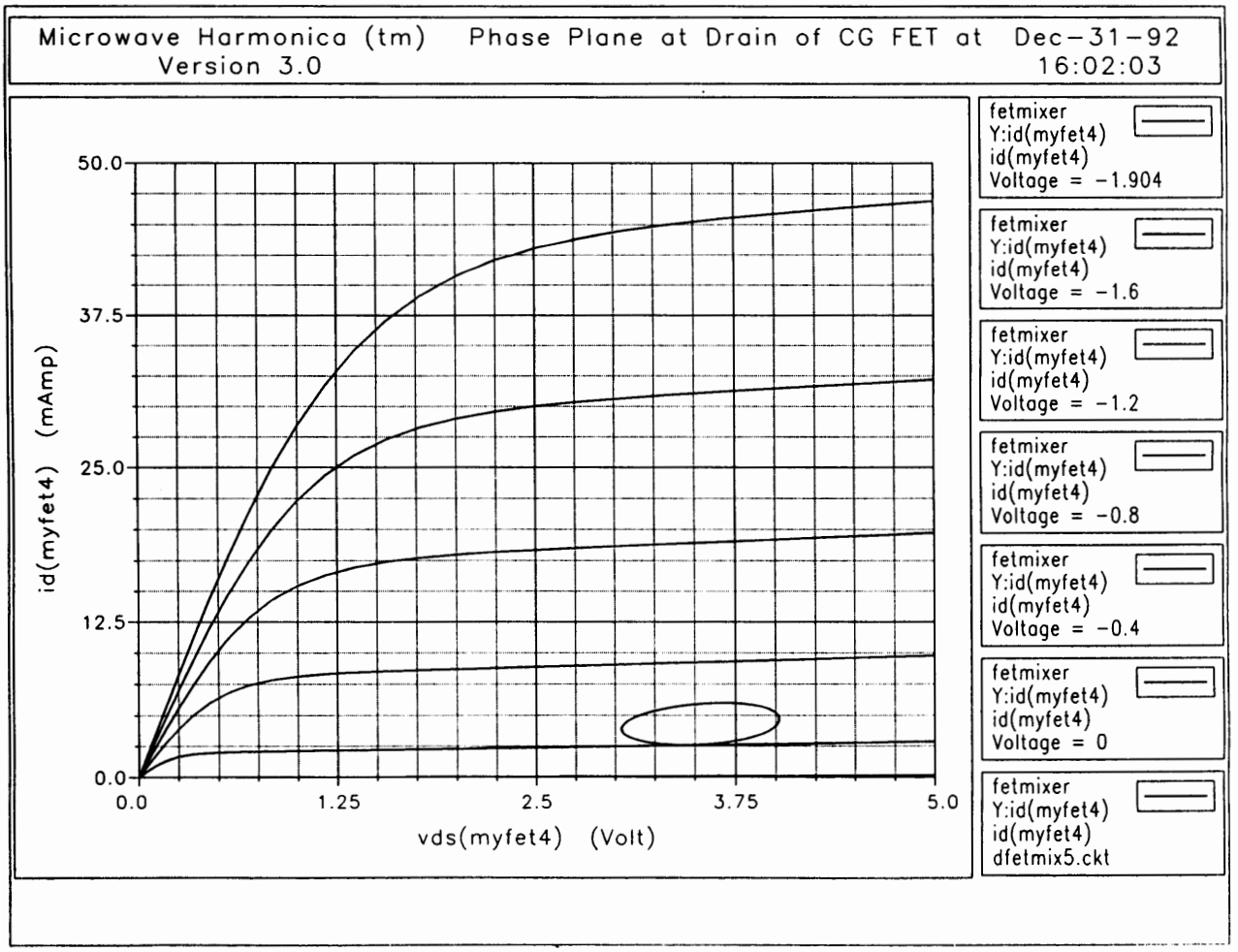

Microwave Harmonica (tm) Conversion Gain of Dual Gate FET M Dec-31-92
Version 3.0
15:29:20
fetmixer
Y:db10(tg32<
db10(tg32<h1-h1,h0
dfetmix5.ckt
26.0
24.5
23.0
21.5
20.0
db10(tg32<h1-h1,h0+h1>) (dB10)
-60.0
-50.0
-40.0
-30.0
-20.0
p2<h0+h1> (dBm)

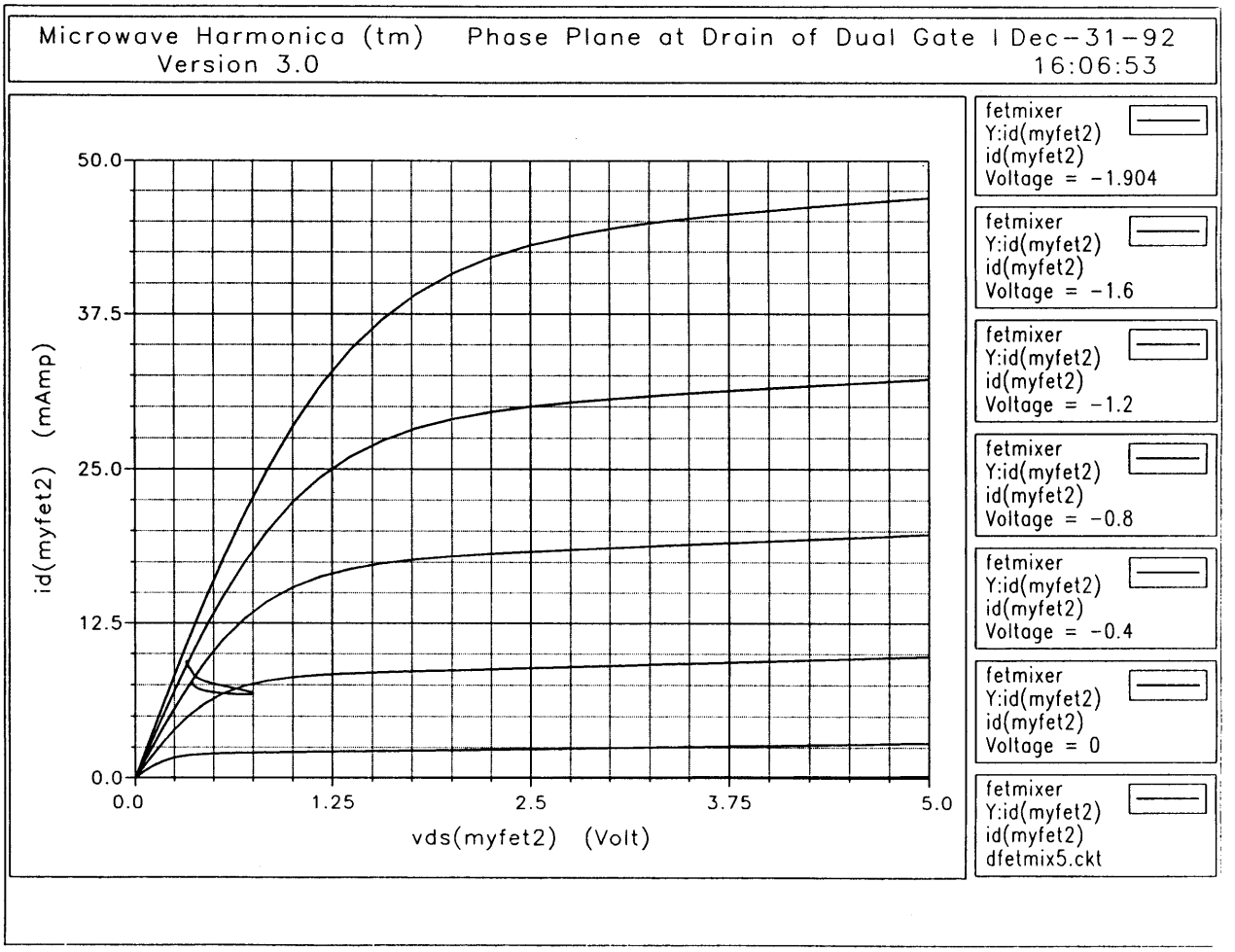

Microwave Harmonica (tm) Conversion Gain of Dual Gate FET M Dec-31-92
Version 3.0
14:54:58
fetmixer
Y:db10(tg32<
db10(tg32<h1-h1,h0
dfetmix5.ckt
21.0
20.8
20.5
20.2
20.0
db10(tg32<h1-h1,h0+h1>) (dB10)
1.93
1.95
1.97
1.99
2.01
Frequency (GHz)

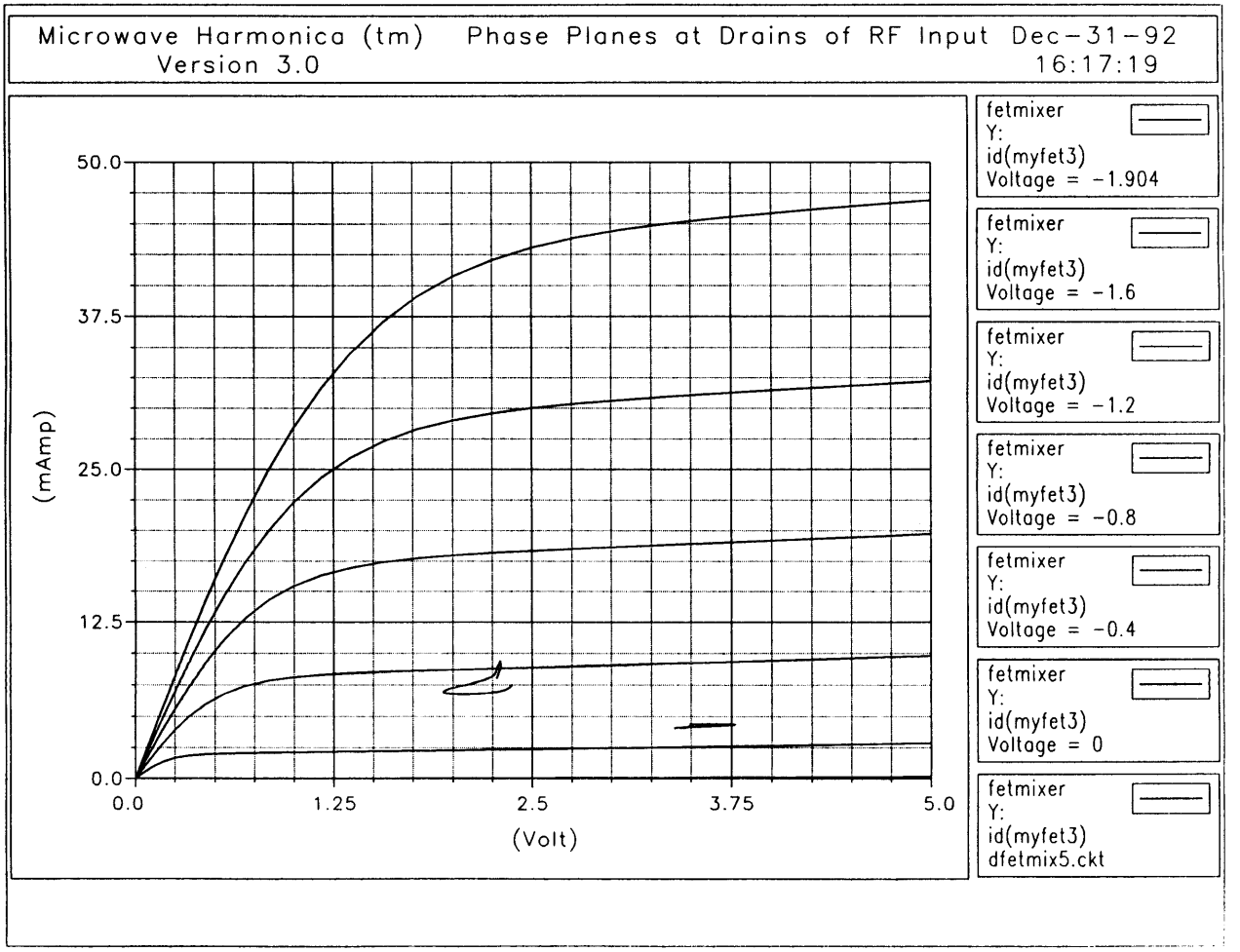

Microwave Harmonica (tm) RF Port Return Loss of Dual Gate F Dec-31-9
Version 3.0
15:48:19
fetmixer
Y:db10(rl2<h
db10(rl2<h0+h1>
dfetmixer5.ckt
-11.6
-11.9
-12.1
-12.4
-12.6
db10(rl2<h0+h1>) (dB10)
-60.0
-50.0
-40.0
-30.0
-20.0
p2<h0+h1> (dBm)
NY , NY 10172
Ave

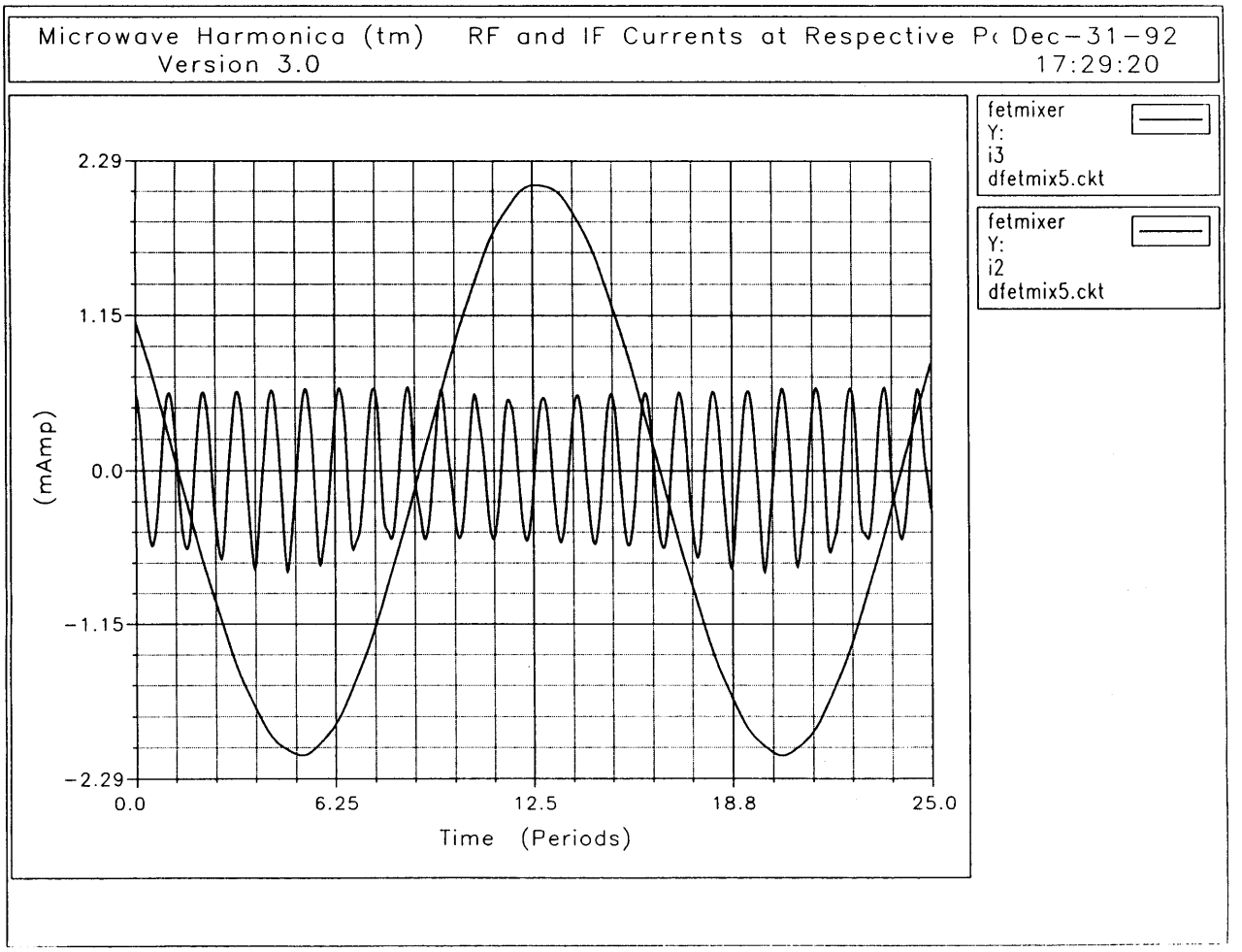

Microwave Harmonica (tm) Return Loss of RF Port vs Frequenc Dec-31-92
Version 3.0
16:58:57
fetmixer
Y:db10(rl2<h
db10(rl2<h0+h1>)
dfetmix5.ckt
-11.8
-11.9
-12.0
-12.1
-12.2
db10(rl2<h0+h1>) (dB10)
1.92
1.94
1.97
2.0
2.02
Frequency (GHz)

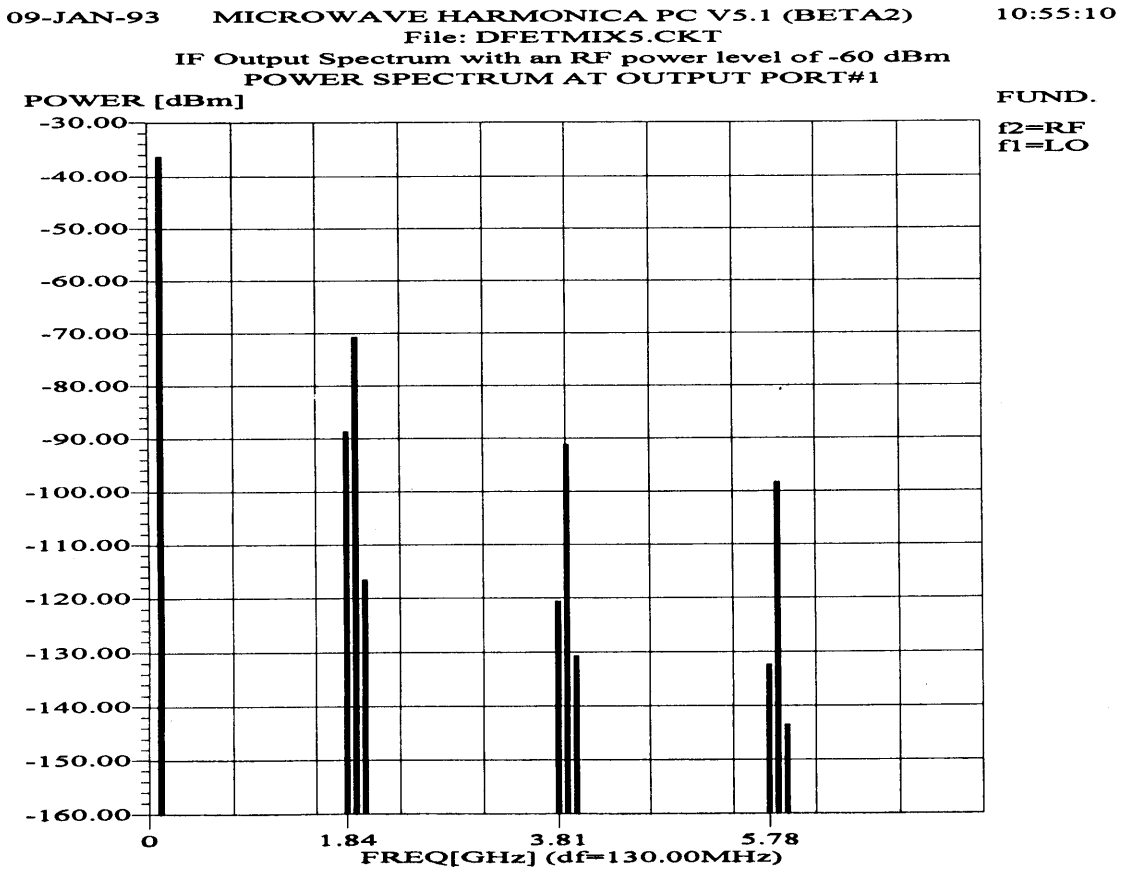

Microwave Harmonica (tm) Return Loss of LO Port vs Frequenc Dec-31-92
Version 3.0 17:05:13
fetmixer
Y:db10(rl1<h
db10(rl1<h1+h0>)
dfetmixer5.ckt
-15.16
-15.24
db10(rl1<h1+h0>) [0.0 dB10 / Div] (dB10)
1.92
1.94
1.97
2.0
2.02
Frequency (GHz)


Microwave Harmonica (tm) Phase Plane at Drain of CG FET at Dec-31-92
Version 3.0 16:02:03
fetmixer
Y:id(myfet4)
id(myfet4)
Voltage = -1.904
fetmixer
Y:id(myfet4)
id(myfet4)
Voltage = -1.6
fetmixer
Y:id(myfet4)
id(myfet4)
Voltage = -1.2
fetmixer
Y:id(myfet4)
id(myfet4)
Voltage = -0.8
fetmixer
Y:id(myfet4)
id(myfet4)
Voltage = -0.4
fetmixer
Y:id(myfet4)
id(myfet4)
Voltage = 0
fetmixer
Y:id(myfet4)
id(myfet4)
dfetmix5.ckt
50.0
37.5
25.0
12.5
0.0
id(myfet4) (mAmp)
0.0
1.25
2.5
3.75
5.0
vds(myfet4) (Volt)


Microwave Harmonica (tm) Phase Plane at Drain of Dual Gate I Dec-31-92
Version 3.0 16:06:53
50.0
37.5
25.0
12.5
0.0
id(myfet2) (mAmp)
0.0
1.25
2.5
3.75
5.0
vds(myfet2) (Volt)
fetmixer
Y:id(myfet2)
id(myfet2)
Voltage = -1.904
fetmixer
Y:id(myfet2)
id(myfet2)
Voltage = -1.6
fetmixer
Y:id(myfet2)
id(myfet2)
Voltage = -1.2
fetmixer
Y:id(myfet2)
id(myfet2)
Voltage = -0.8
fetmixer
Y:id(myfet2)
id(myfet2)
Voltage = -0.4
fetmixer
Y:id(myfet2)
id(myfet2)
Voltage = 0
fetmixer
Y:id(myfet2)
id(myfet2)
dfetmix5.ckt


Microwave Harmonica (tm) Phase Planes at Drains of RF Input Dec-31-92
Version 3.0 16:17:19
50.0
37.5
25.0
12.5
0.0
(mAmp)
0.0
1.25
2.5
3.75
5.0
(Volt)
fetmixer
Y:
id(myfet3)
Voltage = -1.904
fetmixer
Y:
id(myfet3)
Voltage = -1.6
fetmixer
Y:
id(myfet3)
Voltage = -1.2
fetmixer
Y:
id(myfet3)
Voltage = -0.8
fetmixer
Y:
id(myfet3)
Voltage = -0.4
fetmixer
Y:
id(myfet3)
Voltage = 0
fetmixer
Y:
id(myfet3)
dfetmix5.ckt


Microwave Harmonica (tm) RF and IF Currents at Respective P
Version 3.0
Dec-31-92
17:29:20
fetmixer
Y:
i3
dfetmix5.ckt
fetmixer
Y:
i2
dfetmix5.ckt
2.29
1.15
0.0
-1.15
-2.29
(mAmp)
0.0
6.25
12.5
18.8
25.0
Time (Periods)

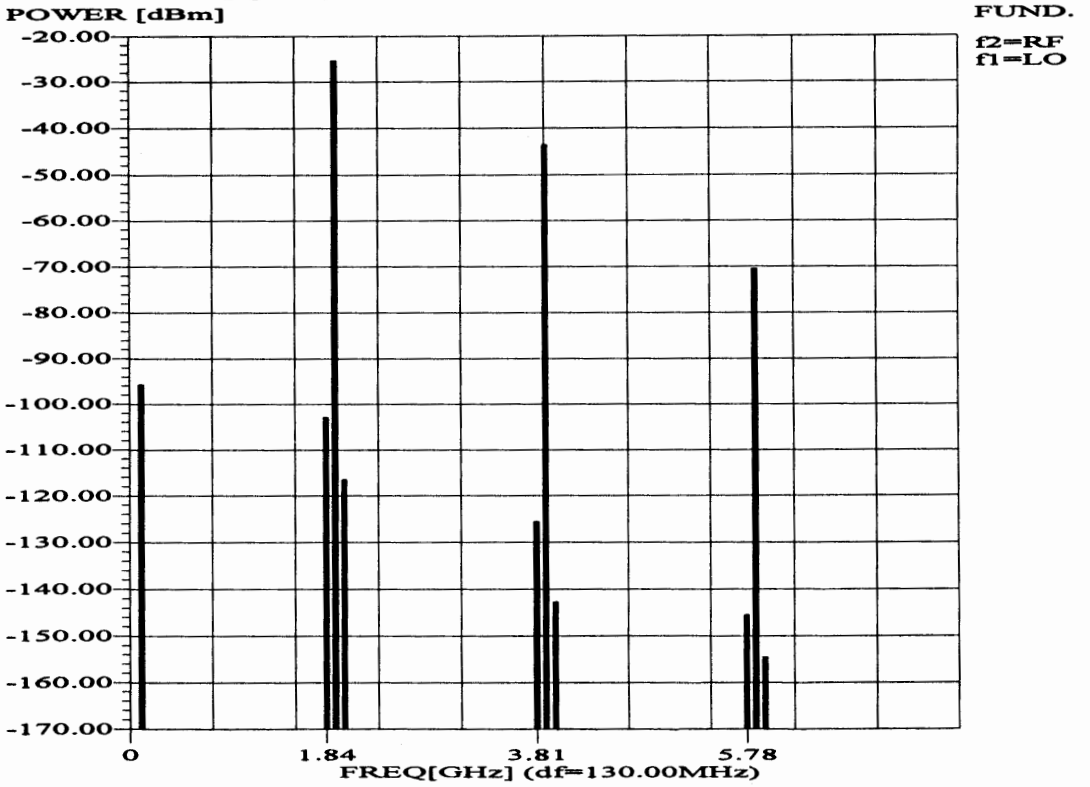

09-JAN-93 MICROWAVE HARMONICA PC V5.1 (BETA2) 10:55:10
File: DFETMIX5.CKT
IF Output Spectrum with an RF power level of -60 dBm
POWER SPECTRUM AT OUTPUT PORT#1
POWER [dBm]
FUND.
f2=RF
f1=LO
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
-100.00
-110.00
-120.00
-130.00
-140.00
-150.00
-160.00
0
1.84
3.81
5.78
FREQ[GHz] (df=130.00MHz)

09-JAN-93 MICROWAVE HARMONICA PC V5.1 (BETA2) 11:24:09

File: DFETMIX5.CKT

RF Signal coming out of LO Port of Mixer

POWER SPECTRUM AT SOURCE PORT#1

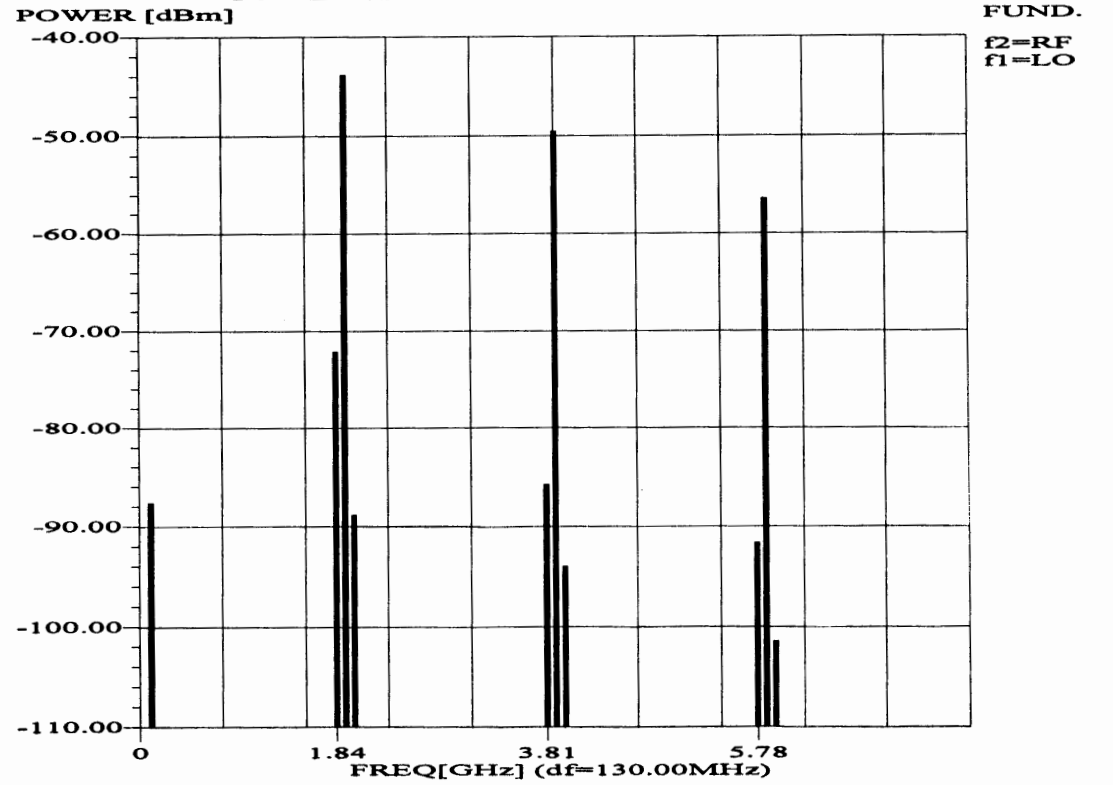


09-JAN-93 MICROWAVE HARMONICA PC V5.1 (BETA2) 11:26:47

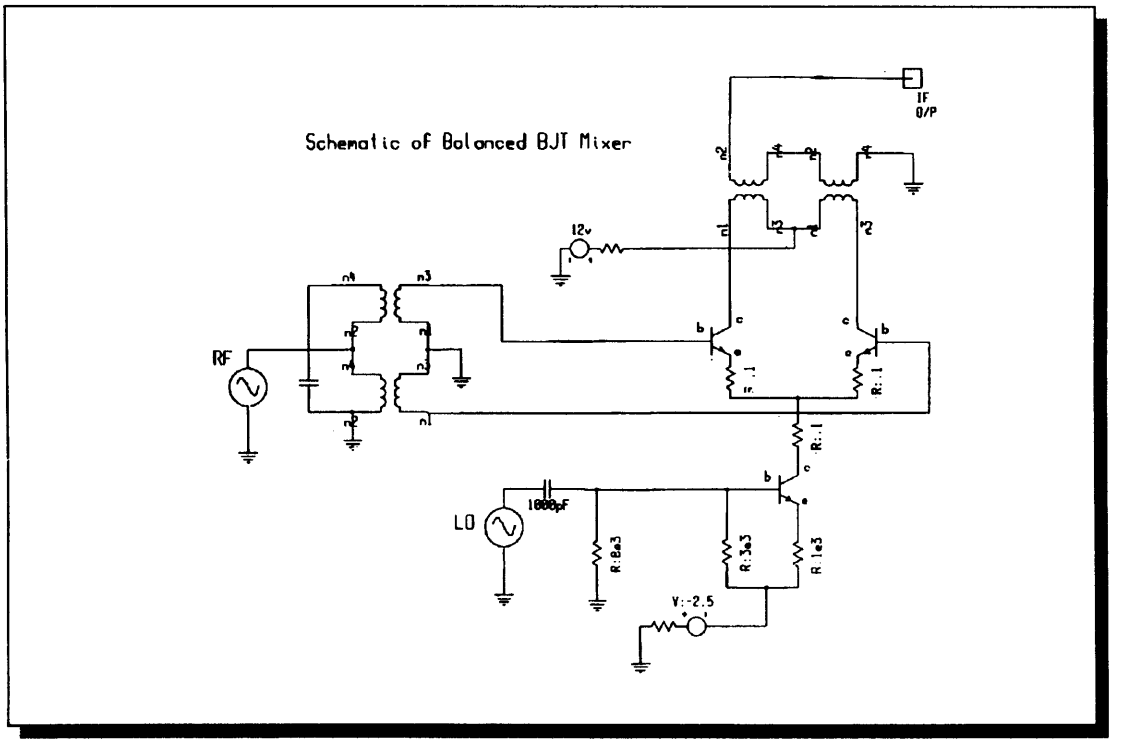
File: DFETMIX5.CKT

LO Signal coming out of RF Port of Mixer

POWER SPECTRUM AT SOURCE PORT#2



Low Current, Balanced Si BJT Mixer RF



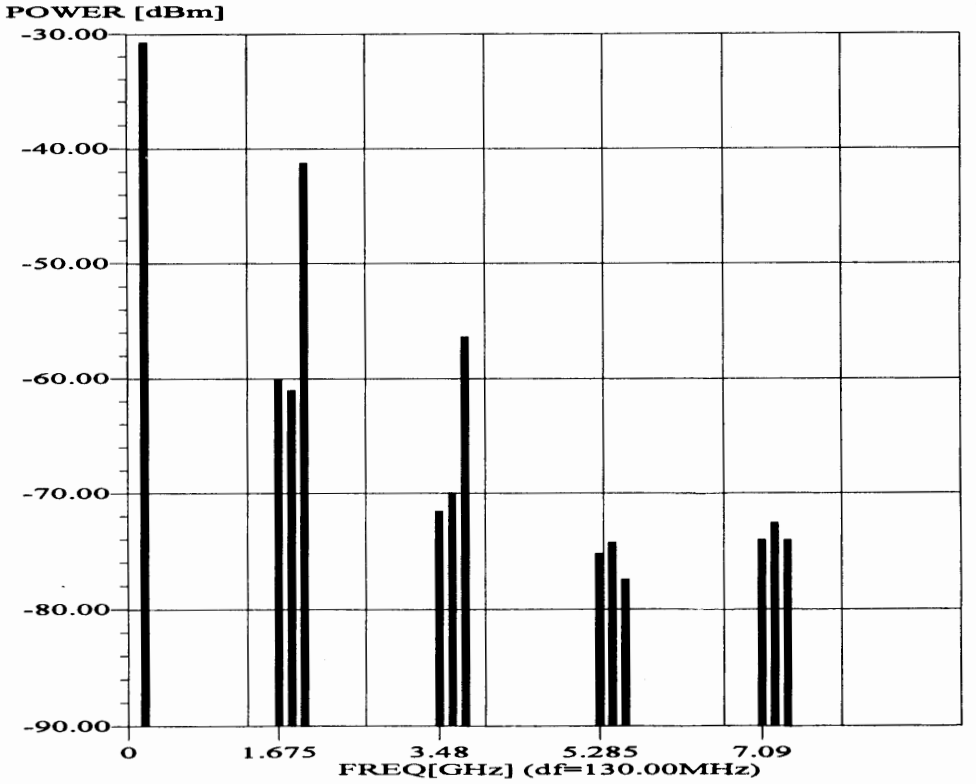
Digital European Cordless Telephone Compact Software

09-JAN-93 MICROWAVE HARMONICA PC V5.1 (BETA2) 15:27:44

File: MIXTEST.CKT

IF Output from Balanced BJT Mixer

POWER SPECTRUM AT OUTPUT PORT#1

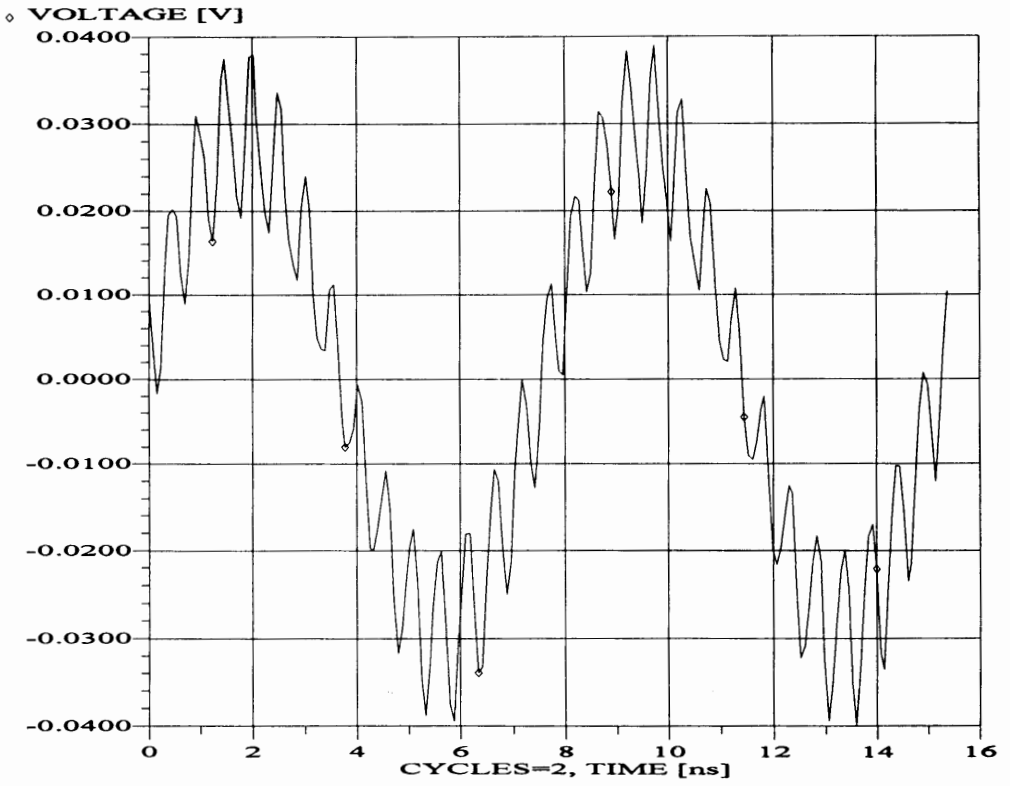


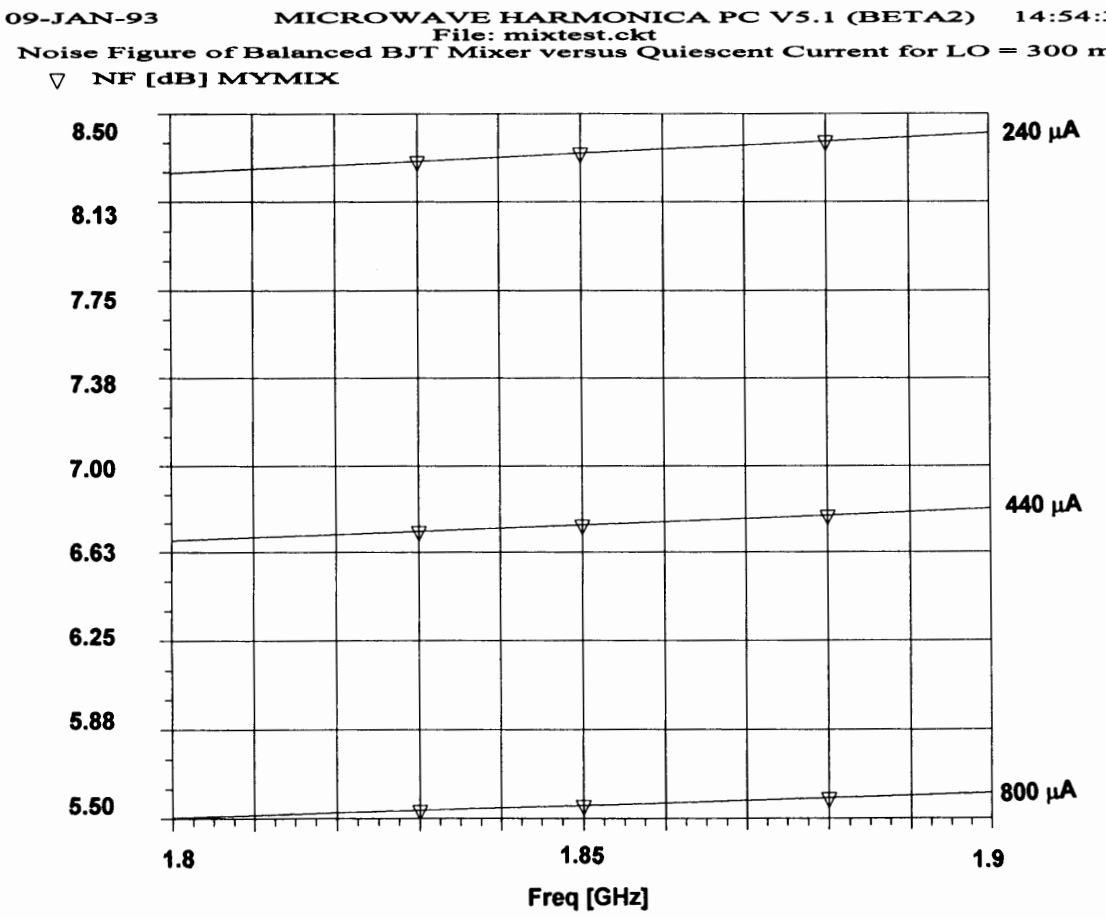
09-JAN-93 MICROWAVE HARMONICA PC V5.1 (BETA2) 15:26:46

File: MIXTEST.CKT

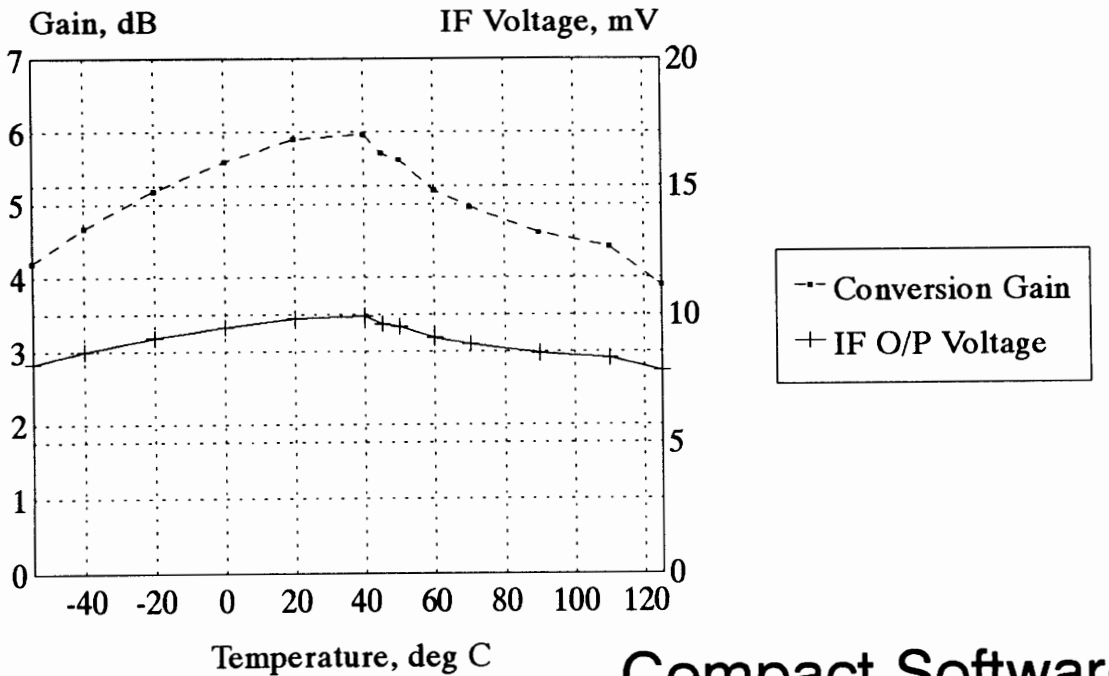
IF Output from Balanced BJT Mixer

VOLTAGE WAVEFORM AT OUTPUT PORT#1





Simulated Variations in Performance of Balanced BJT Mixer versus Temperature



Compact Software

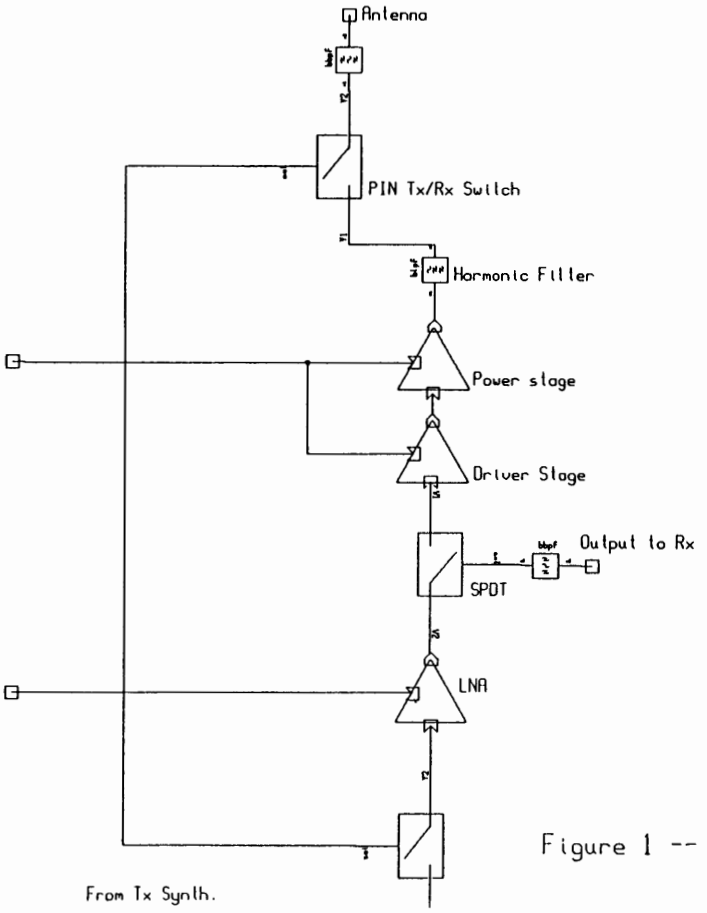


Figure 1 -- Module Architecture

Digital European Cordless Telephone

Typical GaAs Amplifier Performance Specifications
Low Noise Amplifier Application

Frequency range:	1880 MHz to 1900 MHz
Gain:	10 dB +/- 1 dB
Noise figure:	< 3 dB
Input two-tone 3rd order intercept point:	> -10 dBm
Quiescent current consumption:	< 10µA
Input and output impedances:	50 ohms
Power supply:	Single supply 3.3 to 4.5 volts
Operating temperature range:	-10°C to +50°C
Storage temperature range:	-50°C to +150°C

Compact Software

Digital European Cordless Telephone

Power Amplifier Application

Frequency range:	1880 MHz to 1900 MHz
Gain:	37 dB max.
Output power:	26 dBm max.
Quiescent current consumption:	< 10μA
Quiescent forward gain:	< -50 dB
Input and output impedances:	50 ohms
Power supply:	Single supply 3.3 to 4.5 volts
Operating temperature range:	-10°C to +50°C
Storage temperature range:	-50°C to +150°C

An input port is provided to allow the power amplifier to be turned completely off by a standard TTL logic level. The turn-off time must be less than 2 msec and the current consumption must be less than 10μA in this quiescent state. A logic input is also required to provide a ramp up/down within 6 to 8 milliseconds of a 20 dB gain increase/decrease.

Compact Software

GaAs MMIC LNA/ Driver/Power Amplifier and Switches

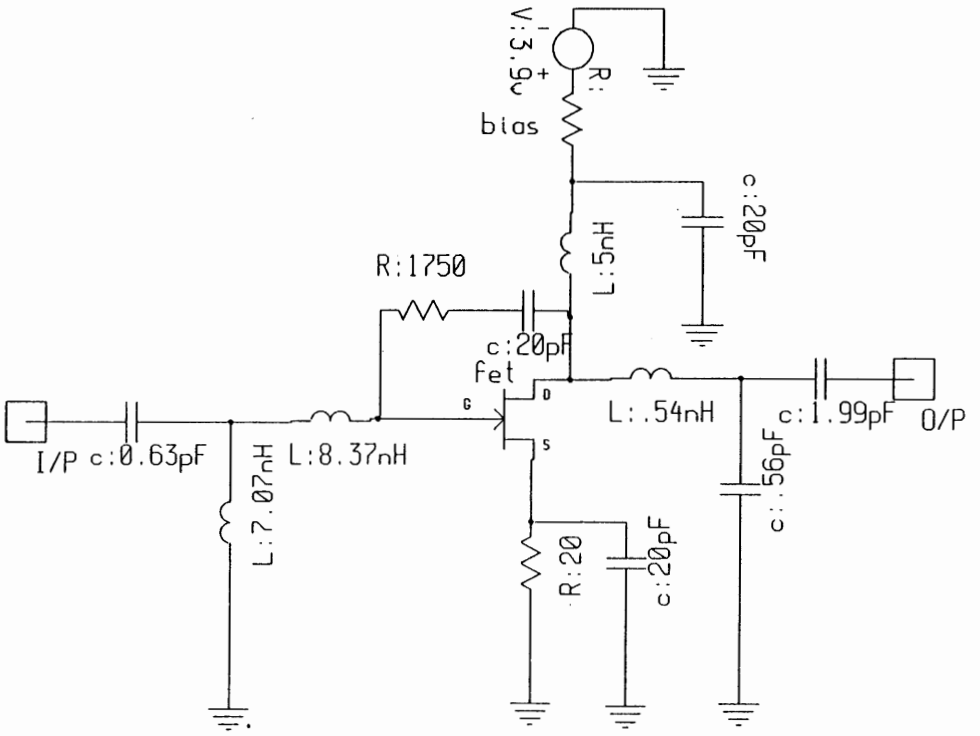
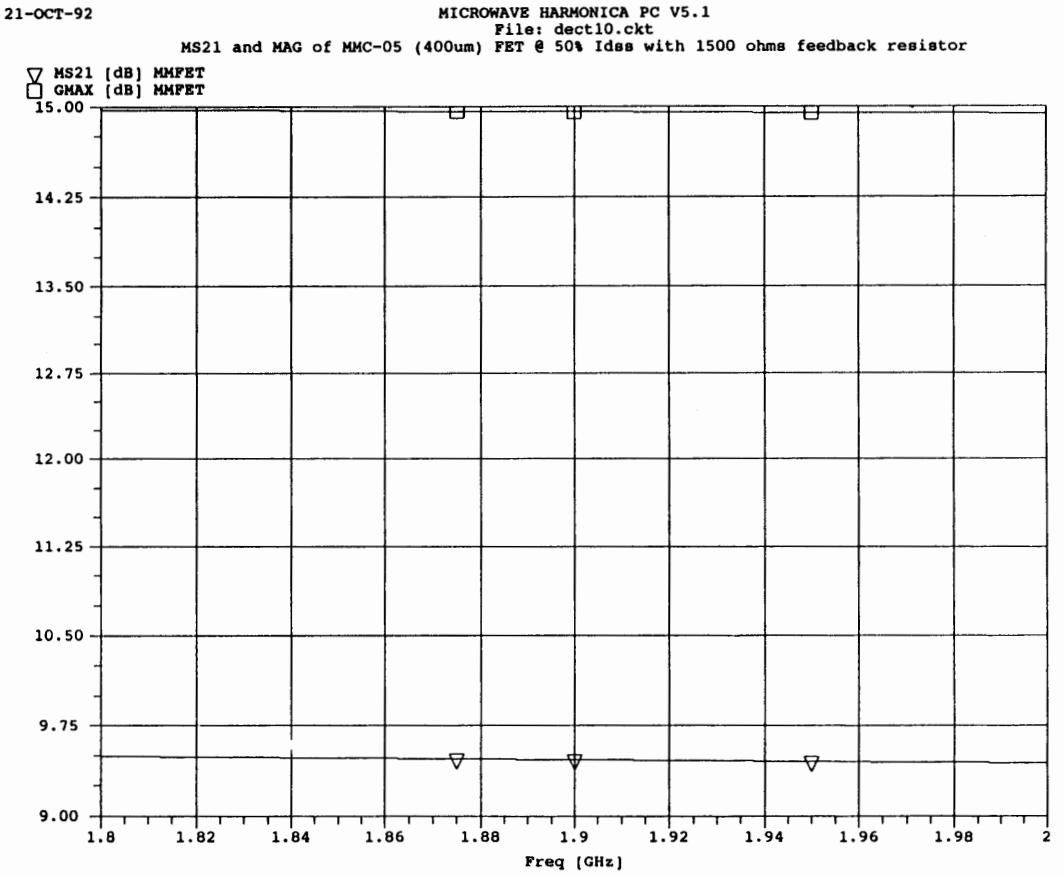
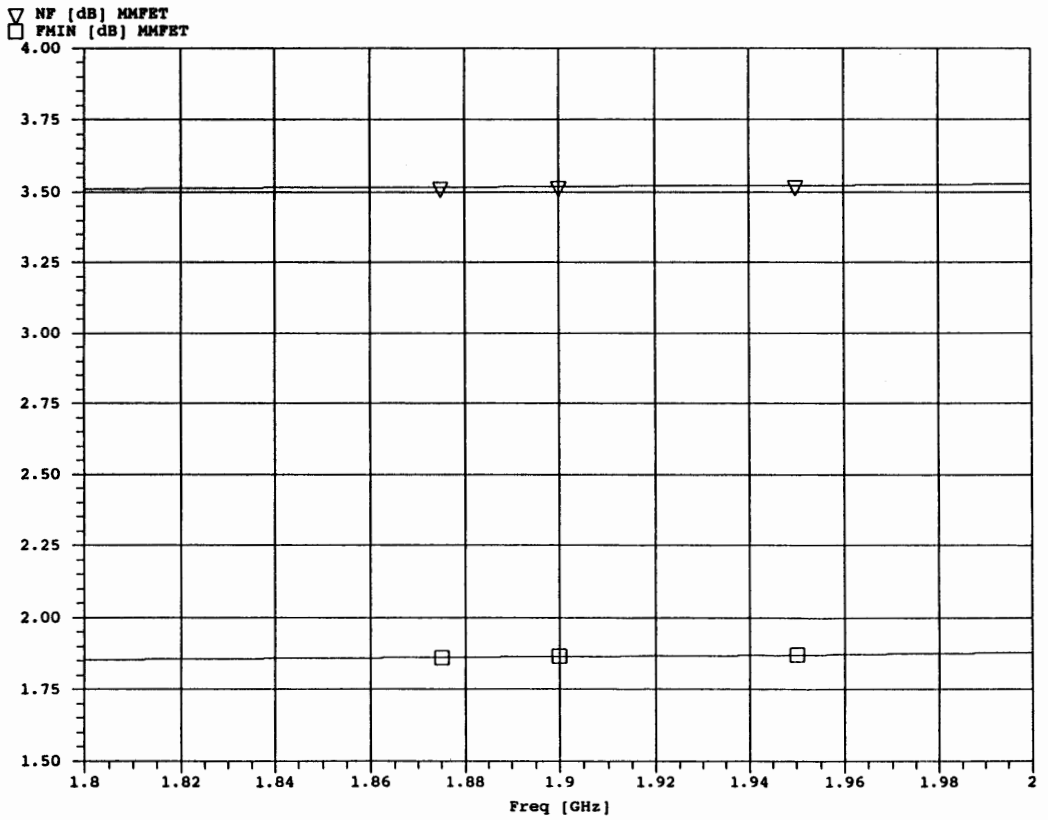


Figure 14 -- Self-Biased Driver Amplifier Stage



File: dect10.ckt

50 ohm an Minimum Noise Figure of MMC-05 (400um) FET (feedback stabilization)

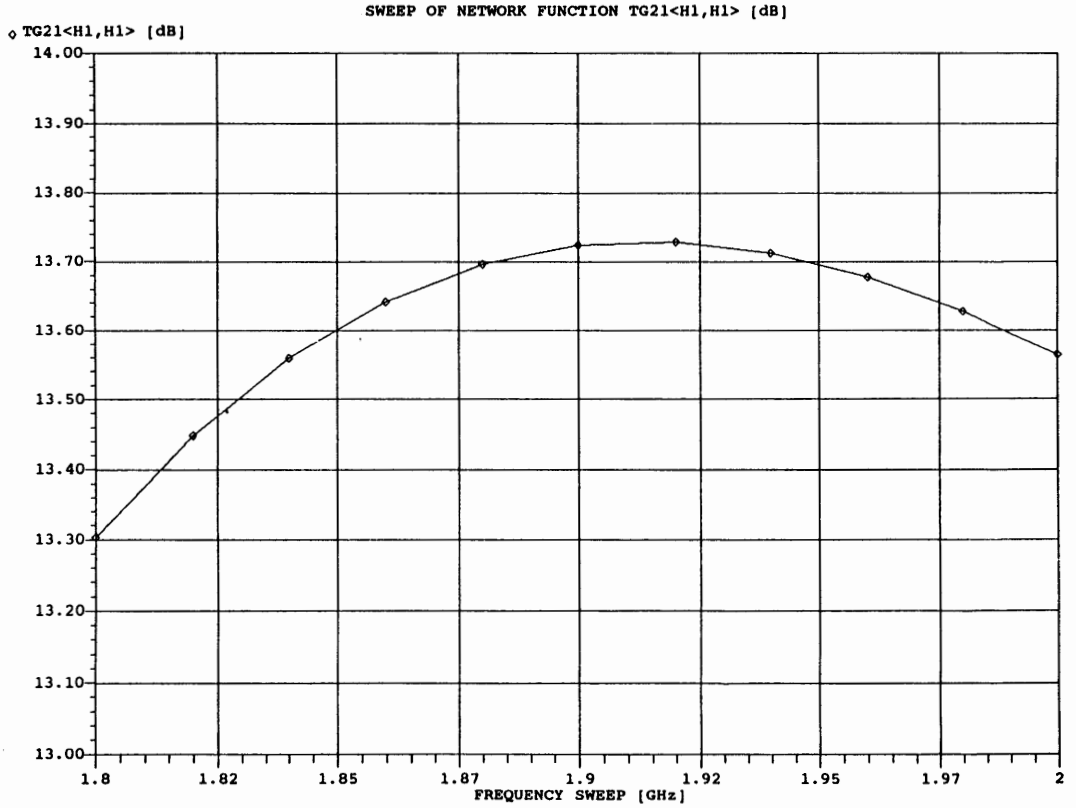


MICROWAVE HARMONICA PC V5.1

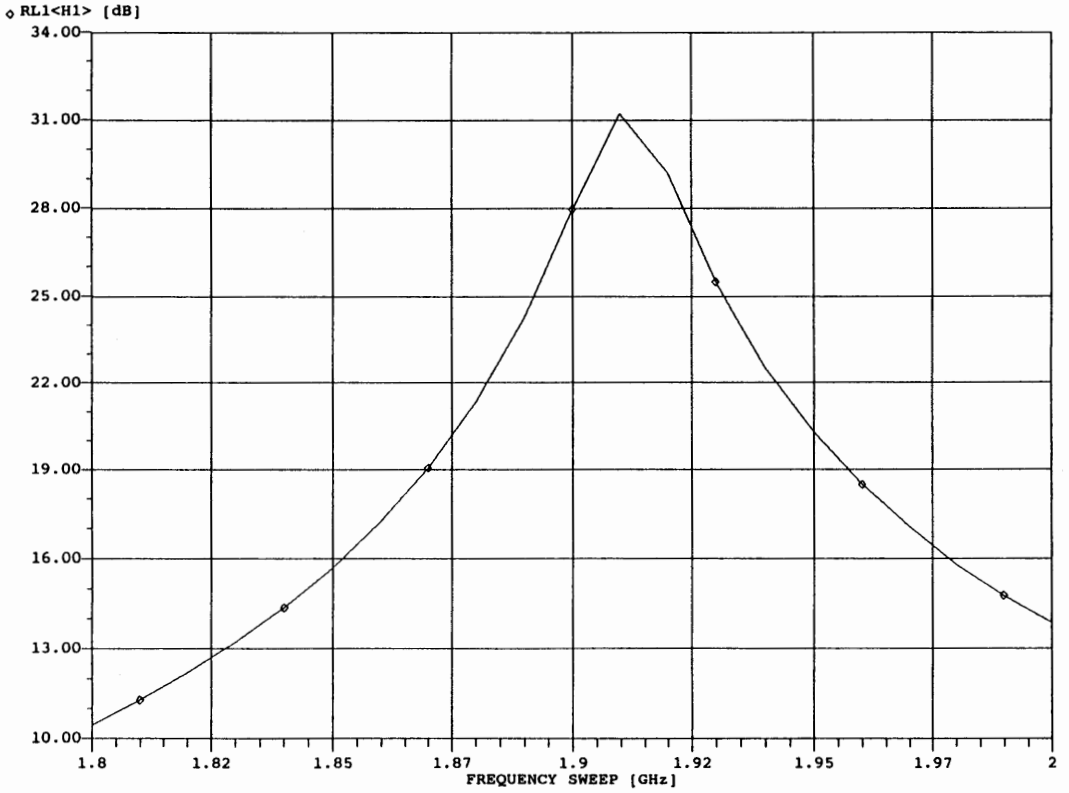
File: DECT17.CKT

Gain of Low-Noise Amplifier versus Freq. @ Pin = -10 dBm

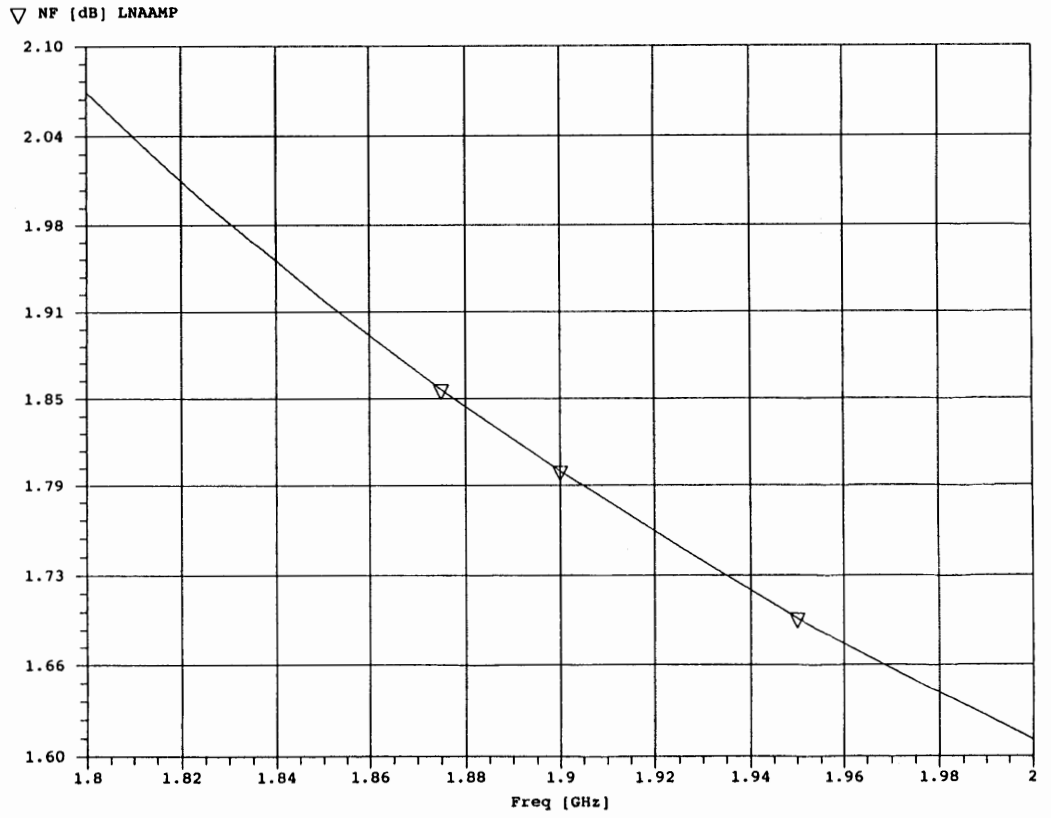
SWEEP OF NETWORK FUNCTION TG21<H1,H1> [dB]



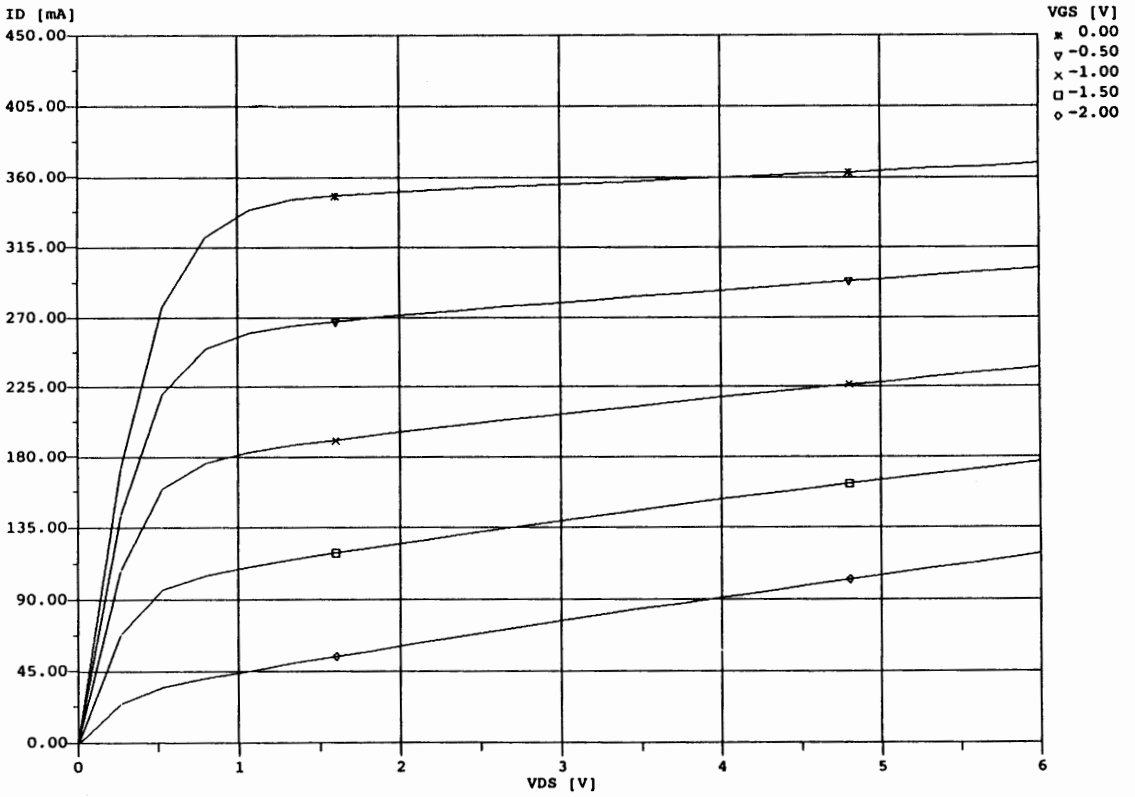
MICROWAVE HARMONICA PC V5.1
File: DECT17.CKT
I/P Return Loss of Low-Noise Amp. versus freq. at Pin=-10dBm
SWEEP OF NETWORK FUNCTION RL1<H1> [dB]



21-OCT-92 MICROWAVE HARMONICA PC V5.1 18:04:25
File: dect13
Noise Figure of Low-Noise Amplifier



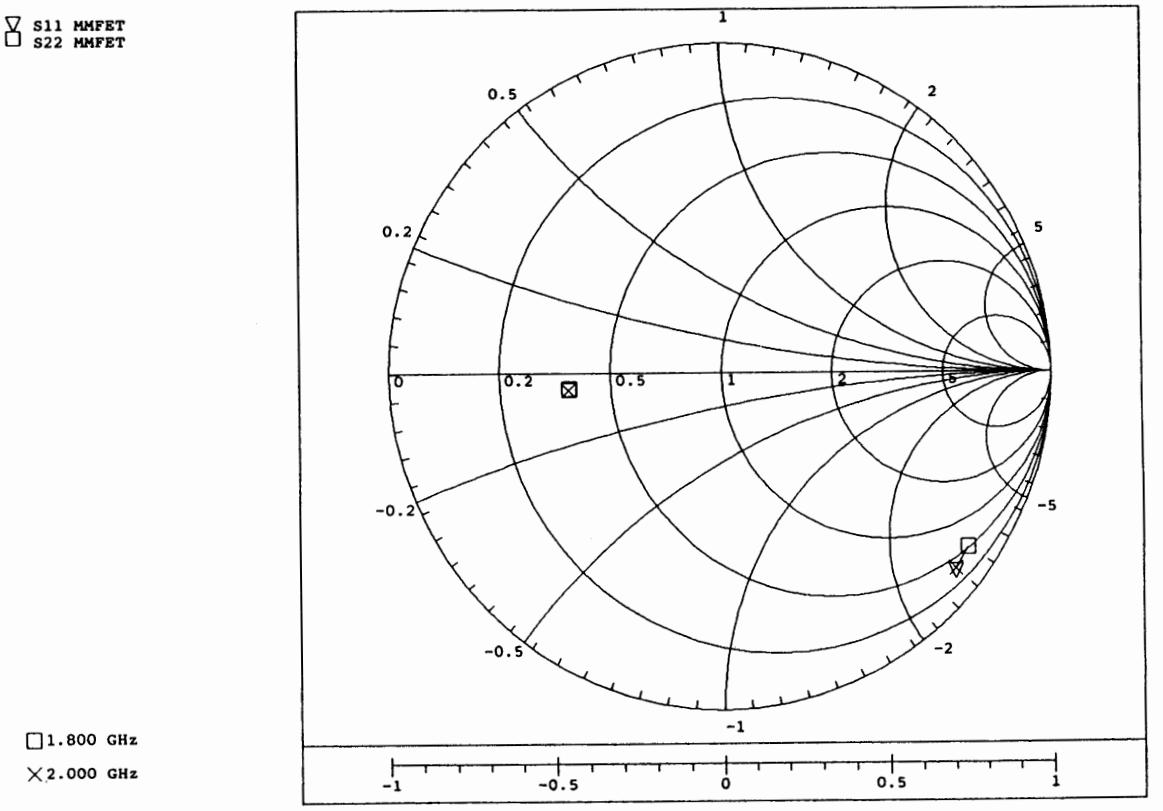
MICROWAVE HARMONICA PC V5.1
File: DECT01.CKT
I-V CHARACTERISTICS OF MMC-05 PROCESS POWER FET (1200um)
DC CHARACTERISTICS OF POFET1



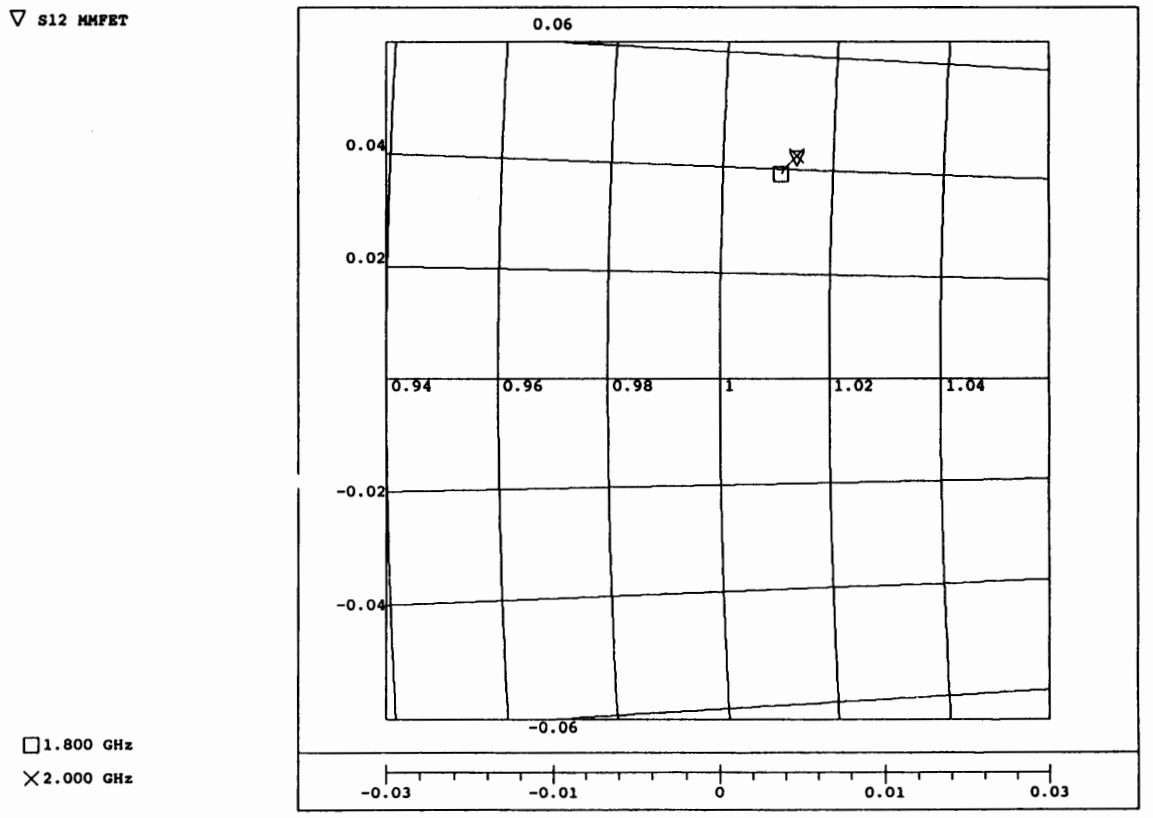
21-OCT-92

MICROWAVE HARMONICA PC V5.1
File: dect02.ckt
S11 and S22 of MMC-05 FET @ Vdd=3.9volts Vgs=-1volt; RF I/P power = 10dBm

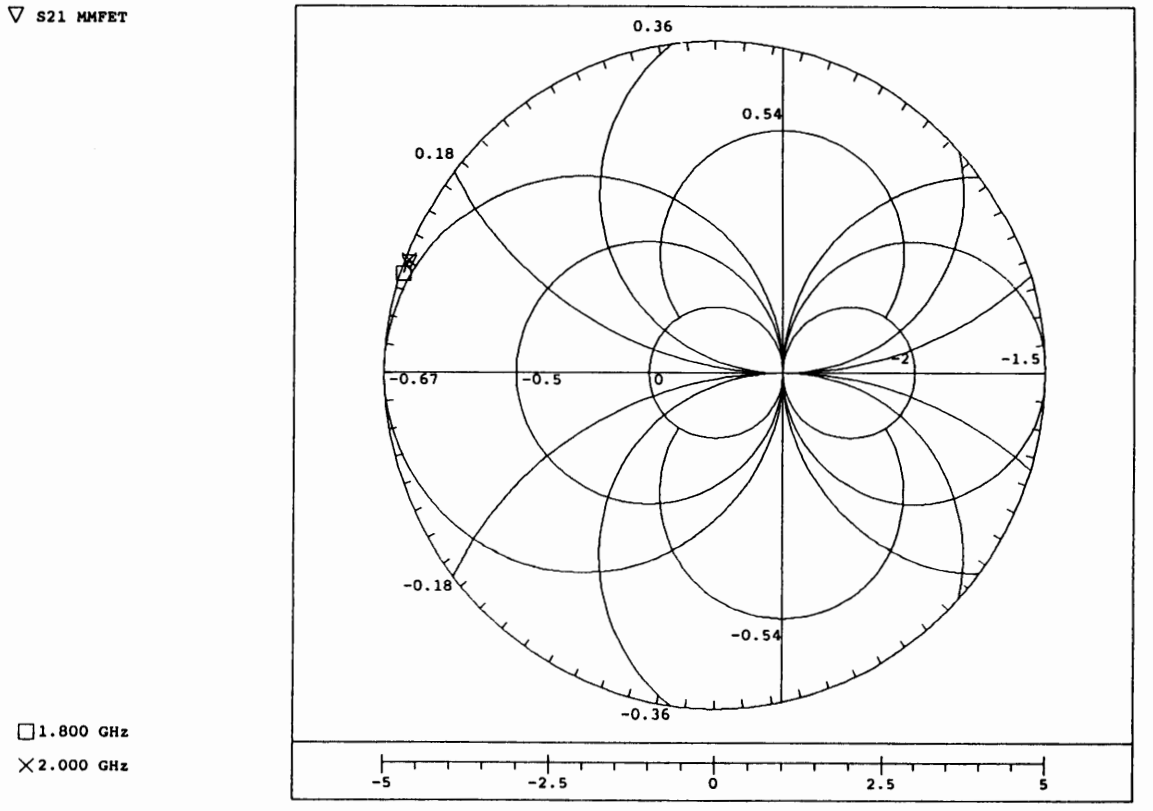
16:57:38



21-OCT-92 MICROWAVE HARMONICA PC V5.1 16:56:21
File: dect02.ckt
S12 of MMC-05 FET @ Vdd=3.9volts Vgs=-1volt; RF I/P power = 10dBm



21-OCT-92 MICROWAVE HARMONICA PC V5.1 16:58:51
File: dect02.ckt
S21 of MMC-05 FET @ Vdd=3.9volts Vgs=-1volt; RF I/P power = 10dBm



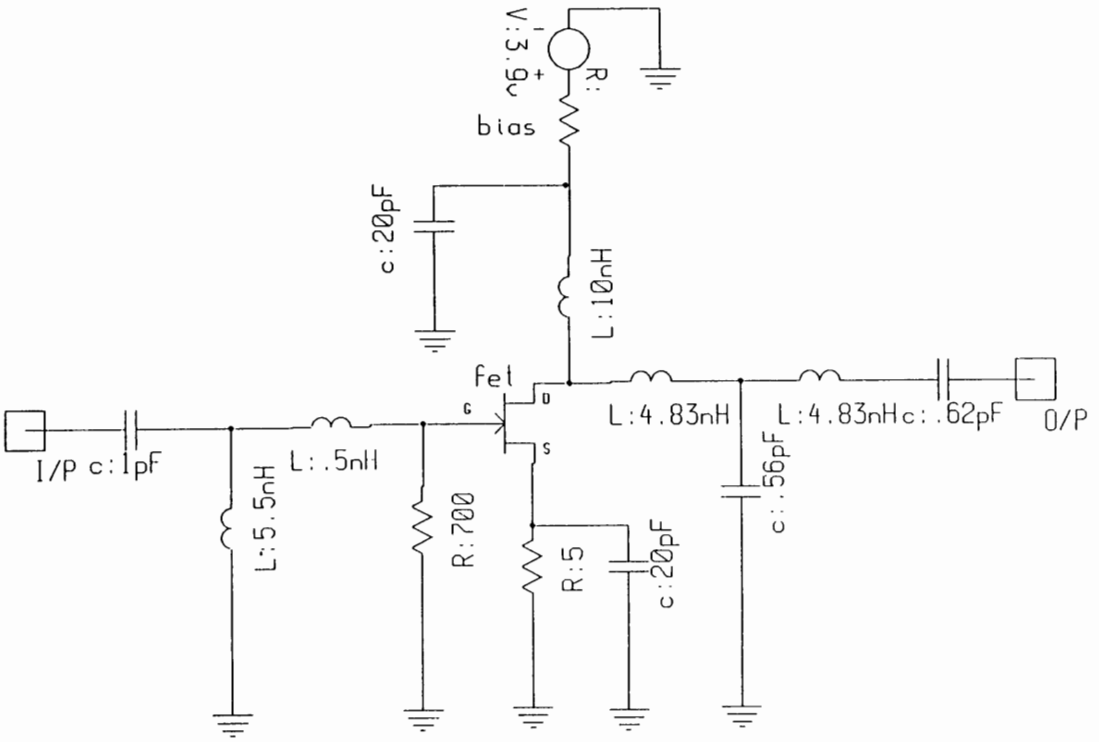
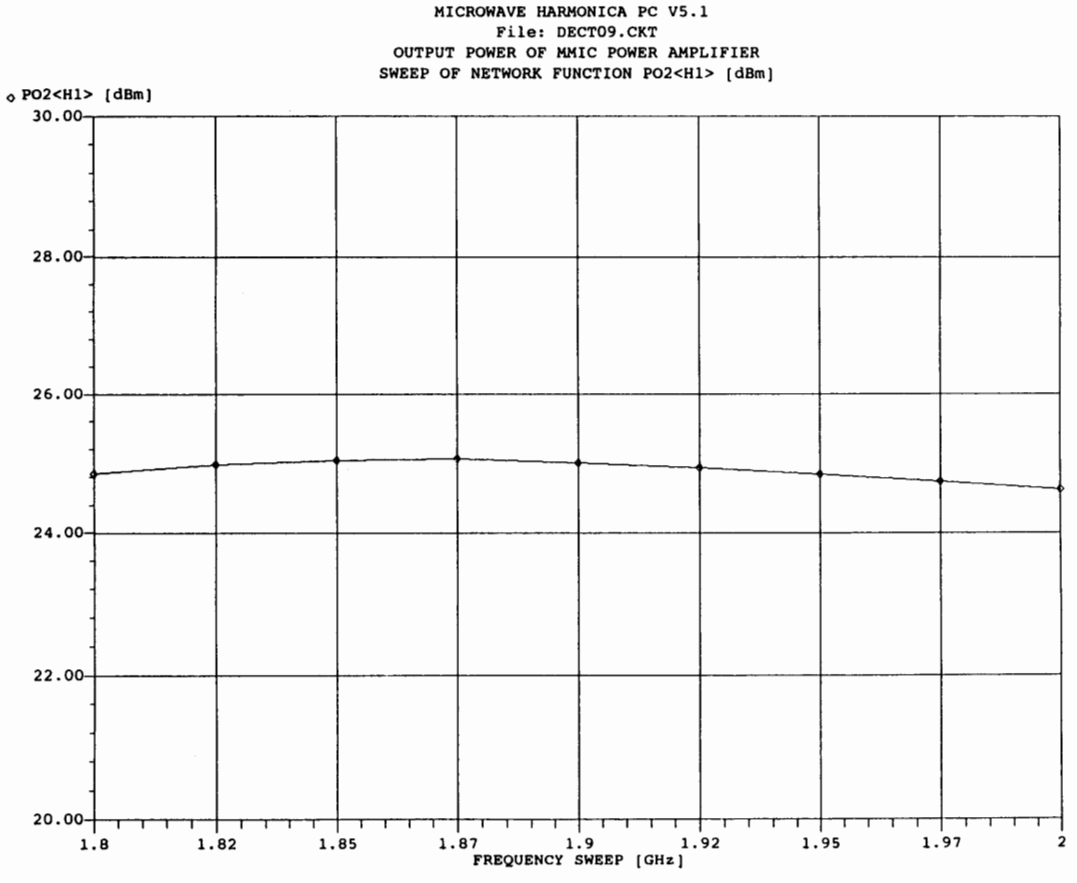
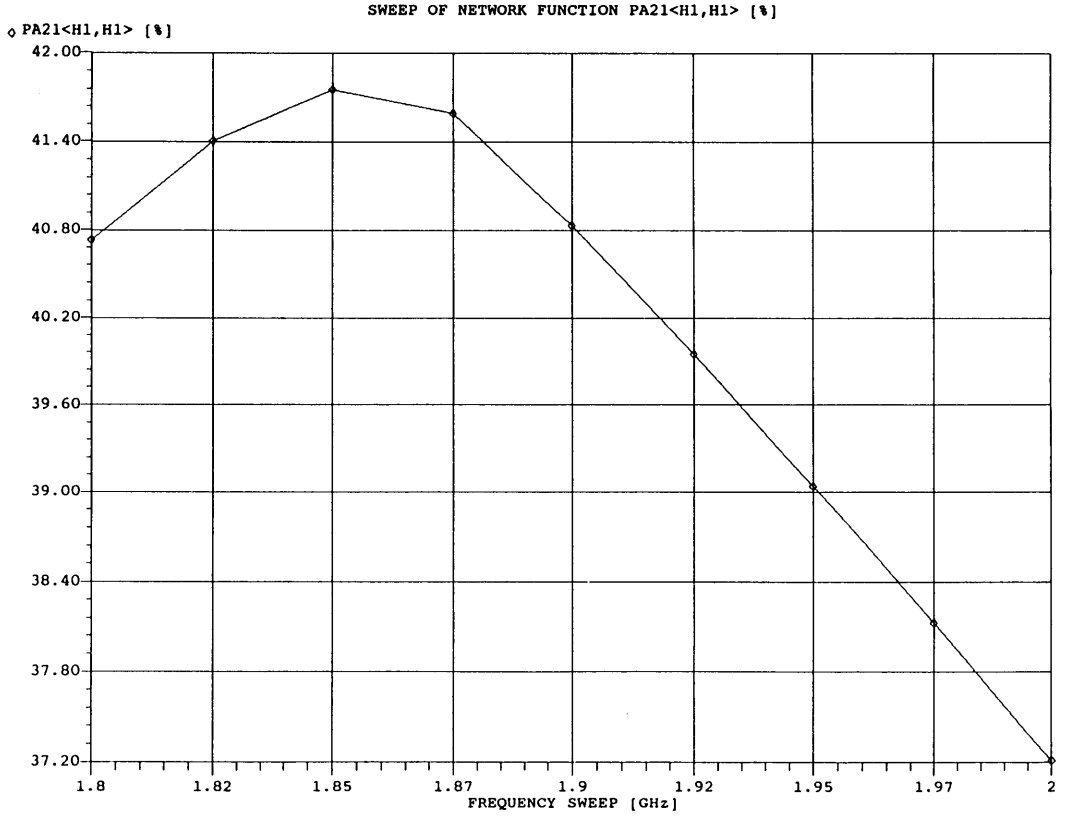


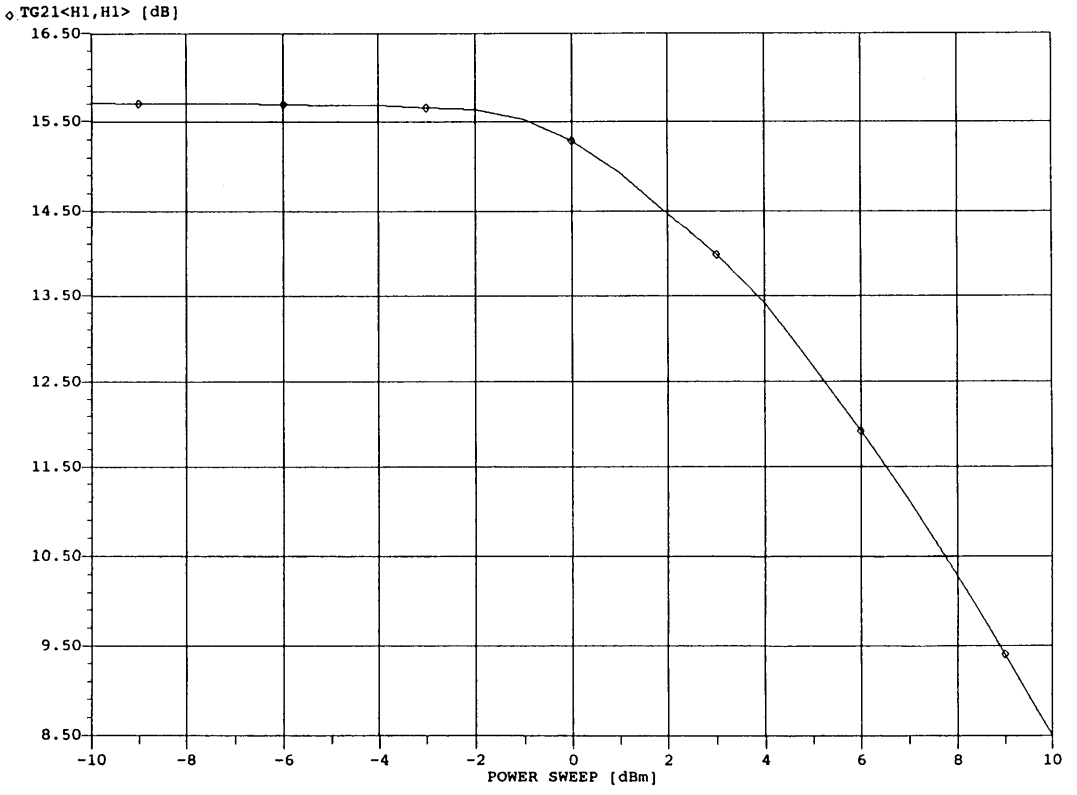
Figure 4 -- Self-Biased Power Amplifier Stage

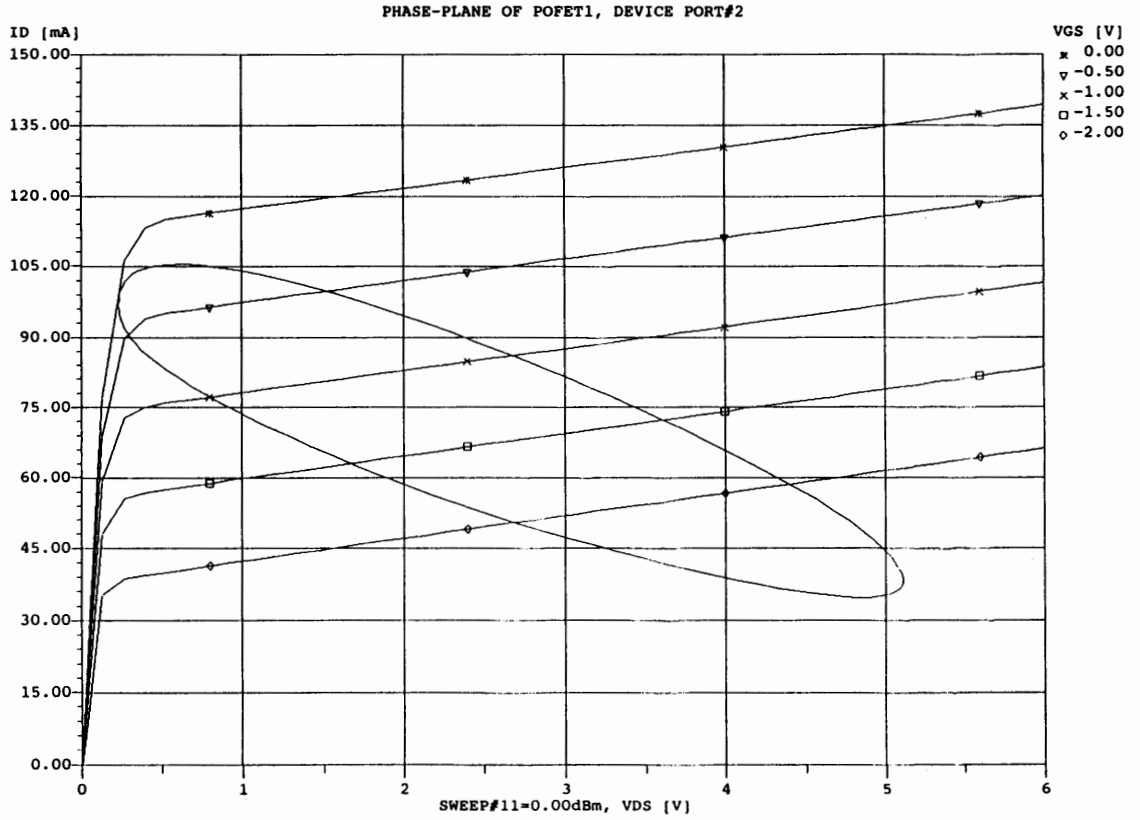


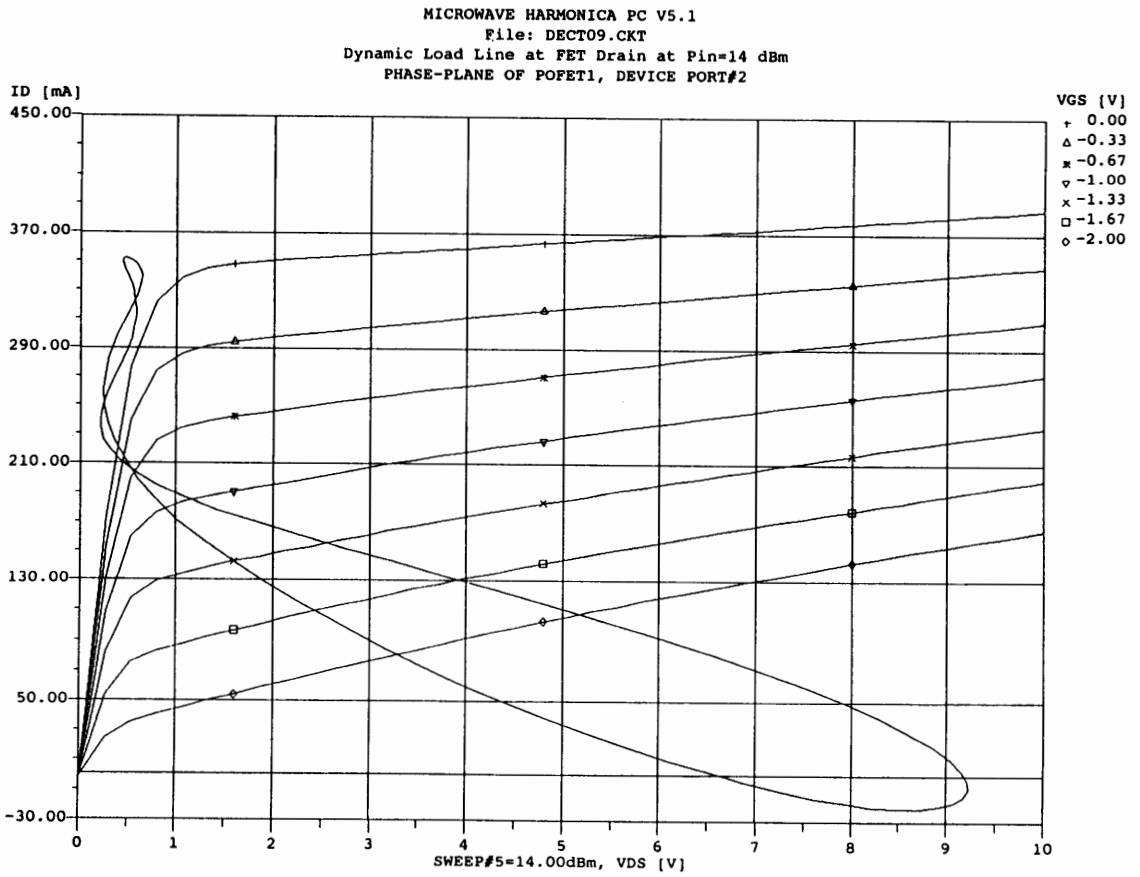
MICROWAVE HARMONICA PC V5.1
File: DECT09.CKT
Power-Added Efficiency of MMIC Power Amplifier
SWEEP OF NETWORK FUNCTION PA21<H1,H1> [%]



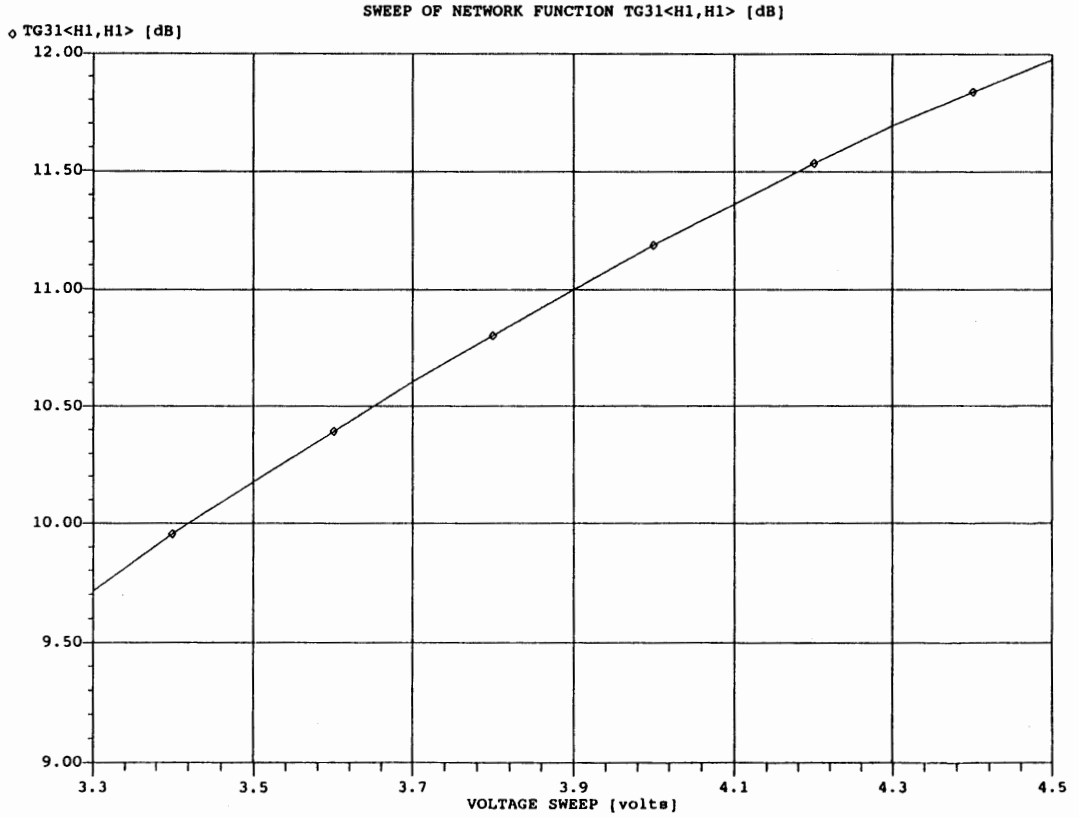
MICROWAVE HARMONICA PC V5.1
File: DECT16.CKT
Gain of Driver Amplifier versus Pin at F = 1.89 GHz
SWEEP OF NETWORK FUNCTION TG21<H1,H1> [dB]



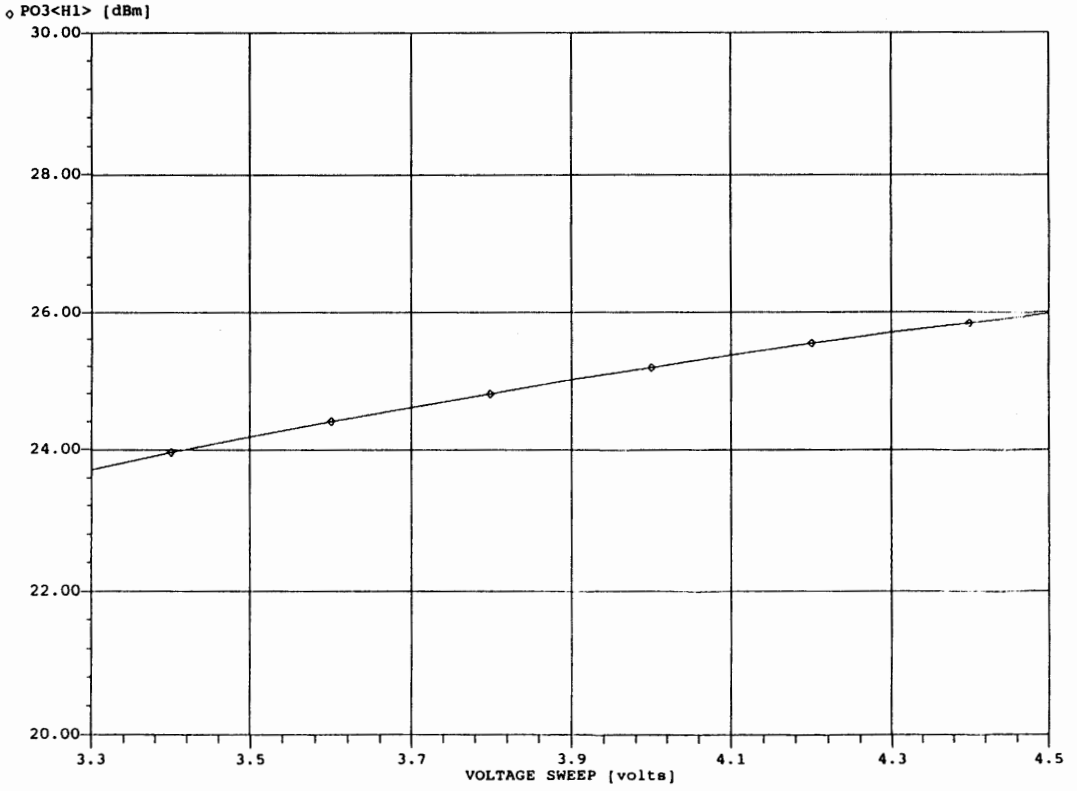

MICROWAVE HARMONICA PC V5.1
File: DECT16.CKT
Dynamic Load Line at Driver FET Drain @ Pin = 0 dBm
PHASE-PLANE OF POFET1, DEVICE PORT#2
ID [mA]
150.00
135.00
120.00
105.00
90.00
75.00
60.00
45.00
30.00
15.00
0.00
0
1
2
3
4
5
6
SWEEP#11=0.00dBm, VDS [V]
VGS [V]
0.00
-0.50
-1.00
-1.50
-2.00


MICROWAVE HARMONICA PC V5.1
File: DECT09.CKT
Dynamic Load Line at FET Drain at Pin=14 dBm
PHASE-PLANE OF POFET1, DEVICE PORT#2
ID [mA]
450.00
370.00
290.00
210.00
130.00
50.00
-30.00
0
1
2
3
4
5
6
7
8
9
10
SWEEP#5=14.00dBm, VDS [V]
VGS [V]
0.00
-0.33
-0.67
-1.00
-1.33
-1.67
-2.00

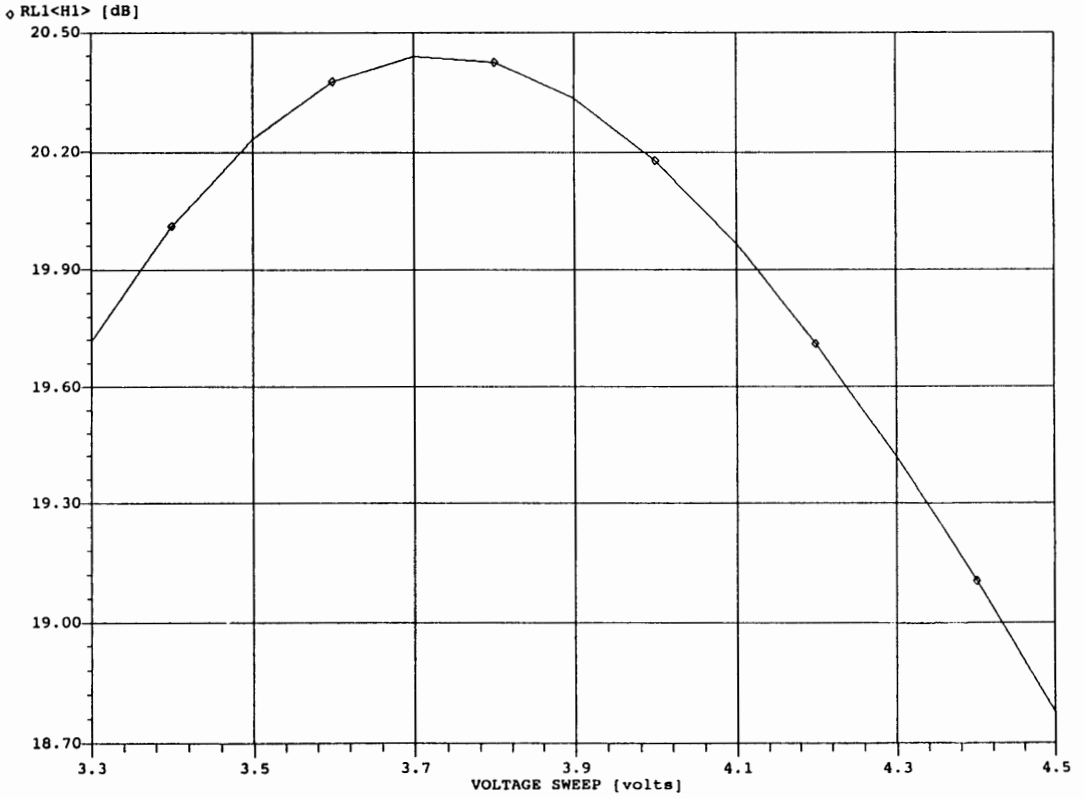
MICROWAVE HARMONICA PC V5.1
File: DECT09.CKT
Power Gain of Amplifier v. Power Supply Voltage @ Pin=14dBm
SWEEP OF NETWORK FUNCTION TG31<H1,H1> [dB]



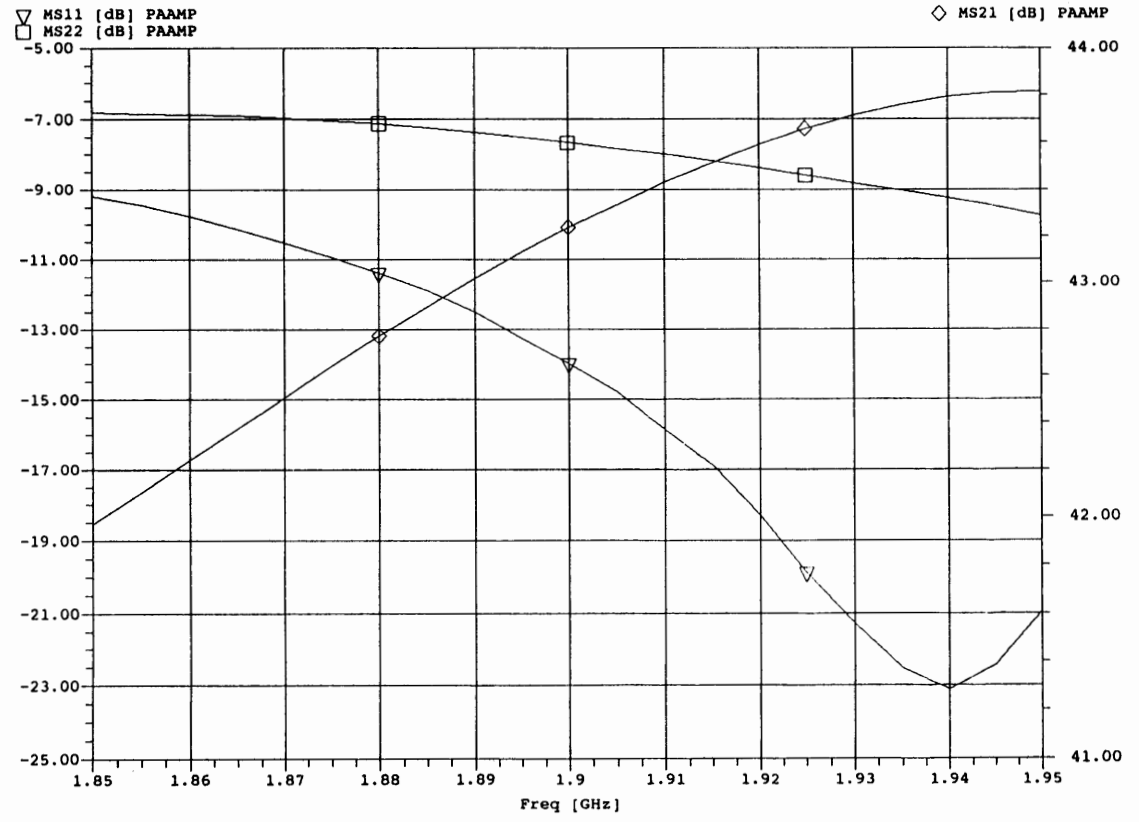
MICROWAVE HARMONICA PC V5.1
File: DECT09.CKT
Output Power versus Power Supply Voltage @ Pin=14 dBm
SWEEP OF NETWORK FUNCTION PO3<H1> [dBm]



MICROWAVE HARMONICA PC V5.1
File: DECT09.CKT
I/P Return Loss of Amp. v. Power Supply voltage @ Pin=12 dBm
SWEEP OF NETWORK FUNCTION RL1<H1> [dB]



21-OCT-92 MICROWAVE HARMONICA PC V5.1 18:08:46
File: dect20
Gain, S11 and S22 of LNA/PA with SPDT Switches

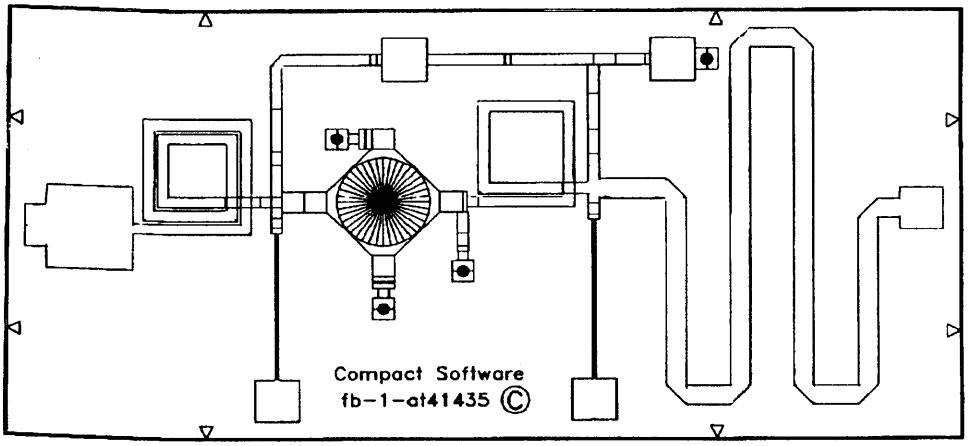


Integration of Simulation with Layout is MOST important even at the relatively low frequencies of present-day wireless communication circuits and subsystems.

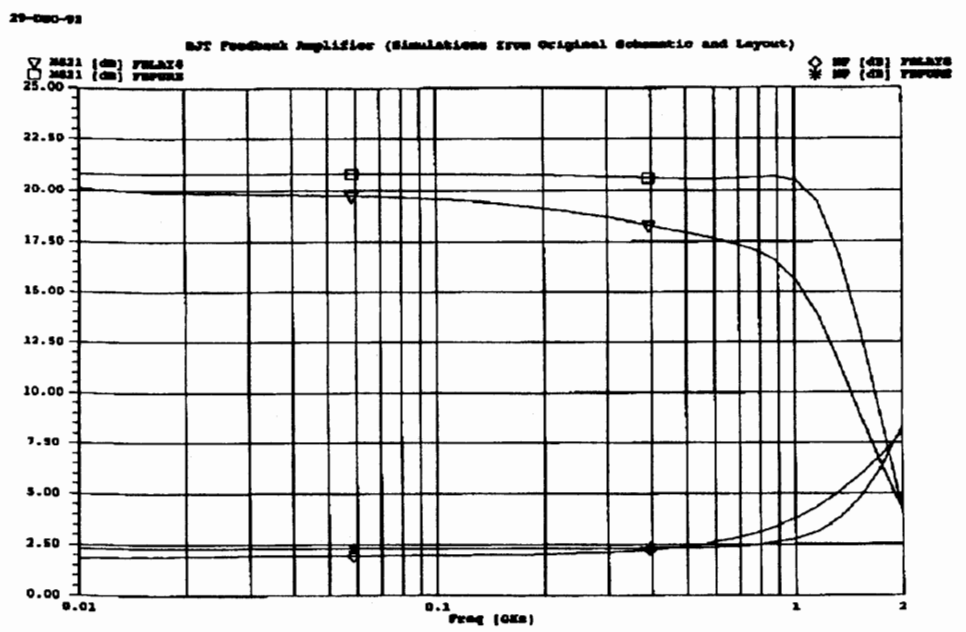
Vendors now supplying so-called Layout-Driven Simulation

EXAMPLE

Broadband BJT Feedback Amplifier with a frequency range of 10 MHz to 1 GHz has performance which is markedly changed by layout.



Layout of BJT Amplifier generated with Serenade



Simulated Performance of Amplifier from Lumped Circuit Only and from Layout

An Integrated Microwave Radio Transceiver For WLAN Applications

David Willliams
GEC Plessey Semiconductors

1. Introduction

The FCC regulations permit un-licensed operation of radio transmitting equipment in the 2.4 to 2.483 GHz band provided that the spectrum of the transmitted signal is spread in a prescribed manner.

This paper describes the design of a Frequency Hopping radio transceiver intended for use in a Wireless Local Area Network system.

2. Discussion

In any design for a frequency agile radio it is essential to minimise the number of oscillators whose frequency must change when the radio changes channel, since the radio will be required to be capable of transmitting or receiving data in the shortest time possible after a command to change frequency.

This requirement is particularly important where Frequency or Phase modulation schemes are used to impart Data on to the carrier signal. If the phase of the carrier signal was changing after a frequency hop any frequency modulated Data would remain corrupted until the rate of change of carrier phase fell below that respresenting a Data bit.

2a. Radio System Design

A schematic diagram of the basic Radio is shown in Figure 1. The design is fundamentally that of a Radio MODEM or Up/Down Converter.

The Frequency Synthesised Master Oscillator (MO) feeds both an up-converter mixer (For Transmit) and a down-converter mixer (For Receive). The Master Oscillator is designed to switch frequency in a short time (100

micro seconds) and is locked to the system reference oscillator (A Crystal Oscillator running at 10 MHz).

The Radio is designed to operate in the 2.4-2.483 GHz Industrial, Scientific & Medical Band and has a first Intermediate Frequency of 350 MHz. The MO therefore operates between 2.05 GHz and 2.133 GHz. The Radio channels are spaced 1 MHz apart.

A Major problem with Up/Down Converter systems is the fact that both the Transmit and Receive IFs are at the same frequency and steps must be taken to prevent leakage of the transmit signal into the Receiver IF chain. This design employs a frequency divider in the Transmitter IF system which is disabled when the Radio is configured to receive. The transmit IF signal is generated at 700 MHz with DATA being imposed by Frequency Modulation of the Voltage Controlled Oscillator (VCO) within the 700 MHz Phase Locked Loop (PLL).

A block schematic of the complete Phase Two (Non-Integrated) radio is shown in Figure 2.

2b. <u>The Receiver Section</u>

The Receiver is a classical double conversion superhetrodyne design. Signals entering the receiver via either antenna port are fed via a Band Defining Filter to the transmit/receive switch, then to a low-noise signal amplifier. A second band-pass filter is inserted after the amplifier to suppress noise generated at the image frequency (1.7 to 1.783 GHz) by this device. Signals are then fed to the first down-converter mixer together with Local Oscillator (LO) drive from the fast hopping synthesiser. Intermediate Frequency signals at 350 MHz are amplified and fed to a Surface Acoustic Wave Filter whose purpose is to restrict the IF band-width in order to maximise signal to noise ratio at this point. An Integrated circuit amplifier/mixer device (GPS SL6444) is used to down-convert the signals to the second IF of 38 MHz, further filtering is provided by a second SAW filter. The Frequency Modulated IF signal is de-modulated in an Integrated Circuit FM Receiver device (MOTOROLA MC 13055). This device provides a digital DATA output together with an analogue output which is used to monitor receiver signal strength. The LO drive for the second down-converter at 312

MHz is generated using a Frequency Synthesiser Integrated Circuit (GPS NJ8820) which is locked to the 10 MHz system reference oscillator.

2c. The Transmitter section

Serial digital DATA is taken from the DATA input and fed to a Low Pass Filter having a Gaussian transfer response, this has the effect of limiting the bandwidth occupied by the Frequency Modulated carrier and ensures that transmissions comply with the requirements of the FCC.

The "shaped" digital signal is used to Frequency Modulate the VCO within a Phase Locked Loop operating at 700 MHz. The Frequency Modulated signal is amplified before being fed to a high speed divide-by-two circuit which is gated on and off by the Transmit/Receive control. The divider output is in the form of a 350 MHz Frequency Modulated "square-wave". It is necessary to Low-Pass filter this signal before it is amplified and fed to the Up-Converter mixer. This is done to reduce the level of the harmonic energy within the signal at this point.

The Upper-Sided output signal from the Up-Converter is selected by the use of a Band-Pass filter at the output of the mixer. This filter provides adequate suppression of the carrier and un-wanted sideband signals from the mixer. The wanted signal is of low amplitude and it is necessary to amplify at this point to a level sufficiently large to drive the output amplifier.

The output power level may be selected to be either 10 mW or 100 mW by use of the "Power Set" control, this switches an attenuator in the output amplifier causing the output level to change.

The output signal from the transmitter is fed to the Transmit/Receive switch and band defining filter before reaching the antenna selector switch and Output/Input ports.

2d. Radio Performance

The Radio described in the previous section has been tested and its peformance is summarised in the table shown in Figure 3.

3. The Integrated Transceiver

The radio design has been developed further to a stage where the complete transceiver may be realised using only four integrated circuits.

A block schematic of the new radio is shown in Figure 4. It can be seen that integrated design makes use of the same basic architecture at the previous design but the various radio functions have been "absorbed" into Radio Frequency Application Specific Integrated Circuits (ASICs).

3a. The Microwave Front-End

This section of the Radio is realised as a Gallium Arsenide Mircowave Monolithic Integrated Circuit (GaAs. MiMIC) and comprises the following circuit functions:-

Antenna Selector (Diversity) Switch
Transmit/Receive Switch
Receiver Low Noise Amplifier
Down-Converter Mixer
IF Pre-amplifier
Up-Converter Mixer
Power Amplifier
Microwave VCO (for fast hopping synthesiser)

GEC Plessey Semiconductors has developed the design of this device with a GaAs foundry and has received first article devices which are being used in prototype integrated radios.

3b. The IF Receiver

The IF Receiver comprises:-

The first IF amplifier
The second down-converter
The RSSI circuitry
The second Local Oscillator
The frequency discriminator and DATA buffer

The IF receiver is fabricated using the GEC Plessey Semiconductors "HE" Advanced Silicon bipolar process and contains transistors having a transition frequency in excess of 14 GHz.

3c. The Triple Synthesiser

This device is fabricated using the GEC Plessey Semiconductors 1.0 micron CMOS process and comprises all the PLL components required to control the three frequency synthesisers in the radio.

3d. The Oscillator/Divider

The final RF ASIC contains the 700 MHz oscillator circuit together with the high speed, variable-modulus, pre-scaler which is used in conjunction with the microwave oscillator in the fast hopping synthesiser. This device is also fabricated using the "HE" bipolar process.

4. Radio Construction

The Phase two (non-integrated) radio contains approximately 40 Integrated Circuits and 200 various passive components and is fabricated on a multi-layer Printed Circuit card having an area 7.0 inches by 5.0 inches. The new integrated radio contains only 4 integrated circuits and 50 passive components and occupies a much-reduced area of 3.0 inches by 2.0 inches. The Phase two and Phase three radios are shown in Figures 5 and 6 respectively.

5. Conclusions

A radio transceiver has been designed and produced whose performance meets the requirments of a frequency agile transmission scheme for Local Area Network applications.

The spectral properties of the radio transmitter are compliant with the requirements of the FCC.

The Phase two radio designated DE6002 has been delivered to "BETA-Site" Customers.

A new fully, integrated radio designated DE6003 containing only four high-performance ASICs has been designed and is being developed.

The device will be commercially available early in 1993.

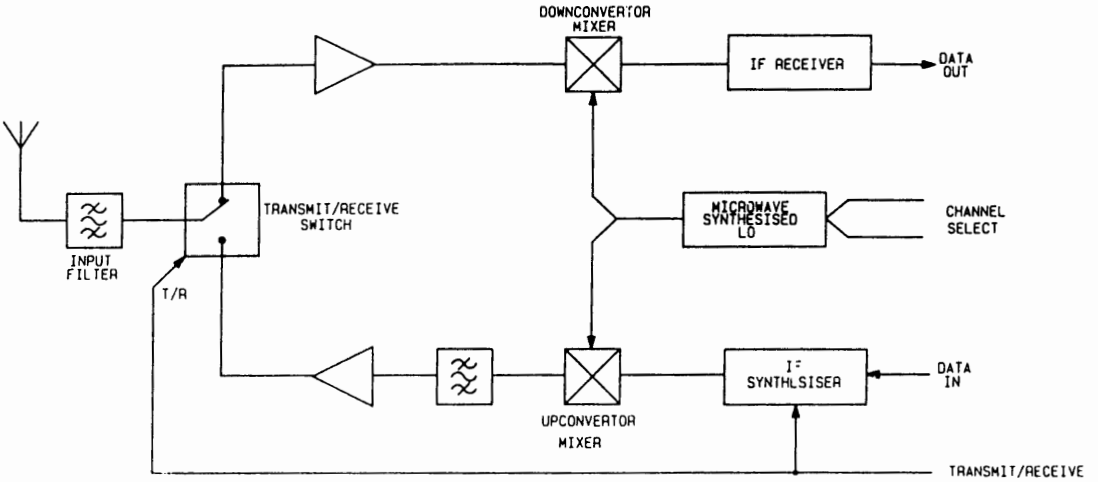


FIG. 1 UPCONVERTOR/DOWNCONVERTOR TRANSCEIVER SCHEME

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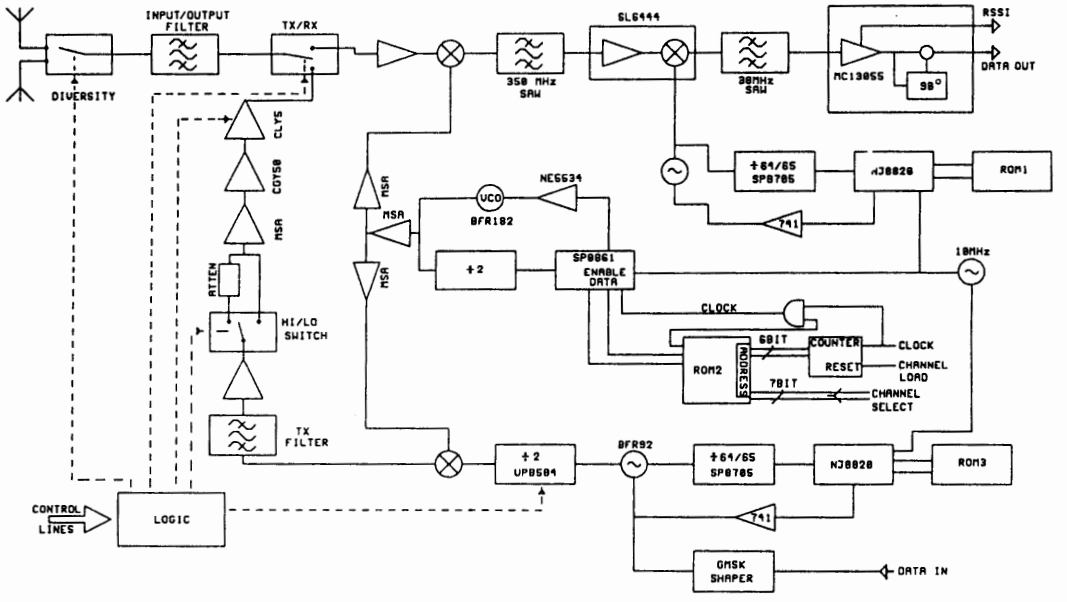

FIGURE 2 PHASE II Transceiver

* Radio System Performance

The performance of the Phase two radio is summaried below:-

a)	Radio Function	Digitally Controlled Transceiver.
b)	Operating Frequency	83 channels 1.0 MHz spacing. 2.4 - 2.483 GHz.
c)	Power Output	Two levels - Hi +20dBm Lo +10dBm
d)	Data Input	Serial 625 Kilo Bits Sec^{-1} 5 volt logic.
e)	Data Output	Serial 625 Kilo Bits Sec^{-1} 5 volt logic
f)	Receiver Sensitivity	-85dBm for 10^{-5} BER. (Bit Error Rate).
g)	Channel Change Time	100µS maximum.
h)	Transmit/Receive Change Time	4µS maximum

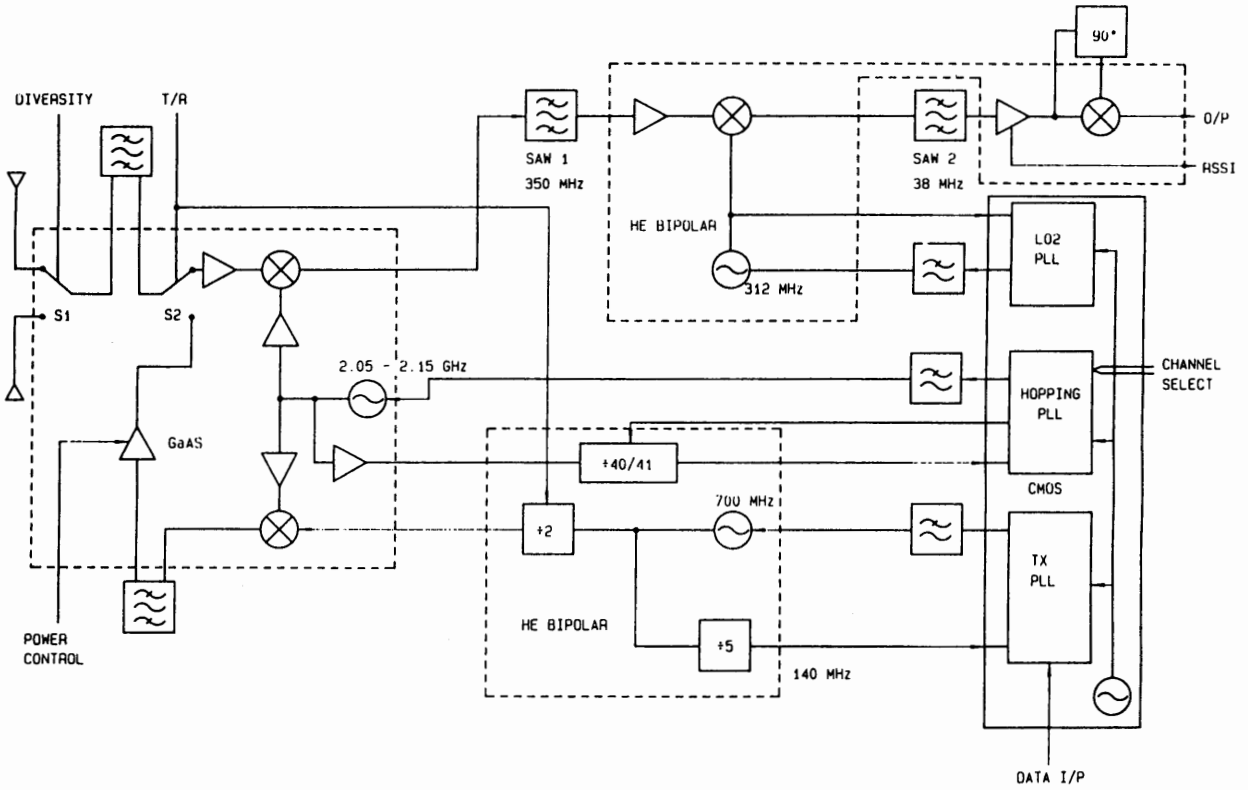

FIG. 4 PHASE III TRANSCEIVER

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ISSUE B

Planar Mixers For PCN Applications Utilizing GMIC Technology

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IC Design Center

M/A-Com Inc.

Abstract -- The investigation of planar mixers for use in communications applications will be discussed. These mixers were developed for use in a block converter or other similar applications where small size and weight are crucial system requirements. Two mixers which utilize separate design approaches are presented. The first approach is a lumped element [1] ratrace mixer which measures 0.150 X 0.120 inches. The second approach is a sub harmonically pumped mixer utilizing lumped element resonators and covering an area of 0.191 X 0.100 inches.

The Ratrace Mixer

This mixer consists of a ratrace coupler, a "beam lead tee" with its associated matching structure, and a low pass filter. The beam lead is the only external part to be assembled onto the GMIC circuit.

The ratrace coupler [2] is configured of three "pi" networks for the 90 degree sections and a "tee" network for the 270 degree section. The networks are transmission line equivalents for the appropriate sections. These equivalents are truly valid only at the exact center frequency, but still provide enough bandwidth for this application. The high pass "tee" was chosen for the 270 degree section to minimize the number of inductors (which are relatively lossy) in the realization of the network. The circuit schematic is shown in Figure 1. Simulated as well as actual performance of the coupler is shown in Figure 2.

The two isolated ports of the coupler are used for the RF and IF signals of the mixer [3]. The coupler isolation therefore provides the isolation between these two signals. The RF and IF signals are then passed through the remaining two ports of the coupler and are matched to the diodes with lumped element matching networks.

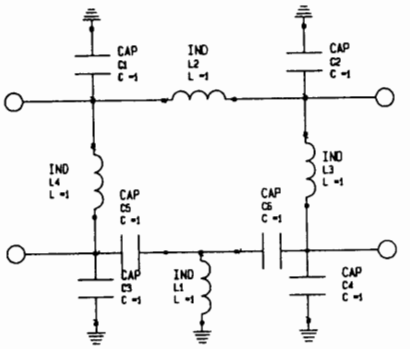

Figure 1. Lumped element equivalent for the ratrace coupler.

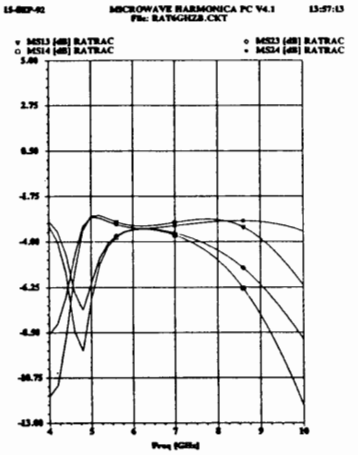

Figure 2a. Simulated coupling vs frequency for the ratrace coupler.

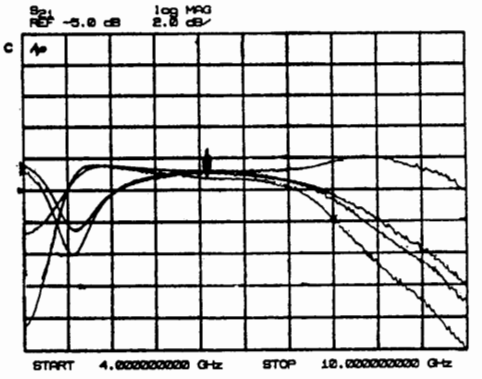

Figure 2b. Measured coupling vs frequency for the ratrace coupler.

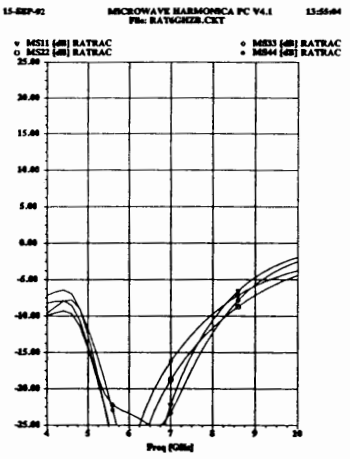

Figure 2c. Simulated return loss vs frequency for the ratrace coupler.

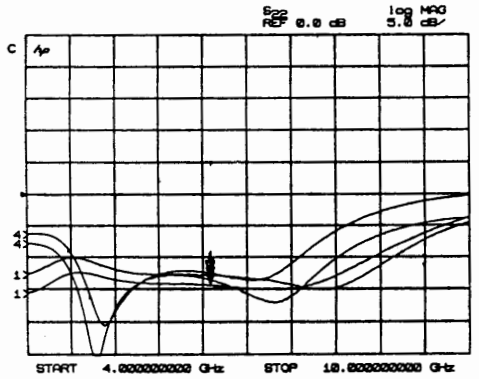

Figure 2d. Measured return loss vs frequency for the ratrace coupler.

The mixing products resulting from the two signals are passed through a three element filter to reject any unwanted signals which might be present. The simulated and measured performance of the mixer is shown in Figure 3. A schematic and a GMIC layout of the mixer are shown in Figure 4 and 5 respectively. A performance summary is presented in Table 1.

Frequency:	RF	5 - 8 GHz
	LO	5 - 8 GHz
	IF	750 - 950MHz
Conversion Loss		8 dB
Isolation:	RF-LO	18 dB
	RF-IF	45 dB
	LO-IF	45 dB

Table 1. Performance Summary.

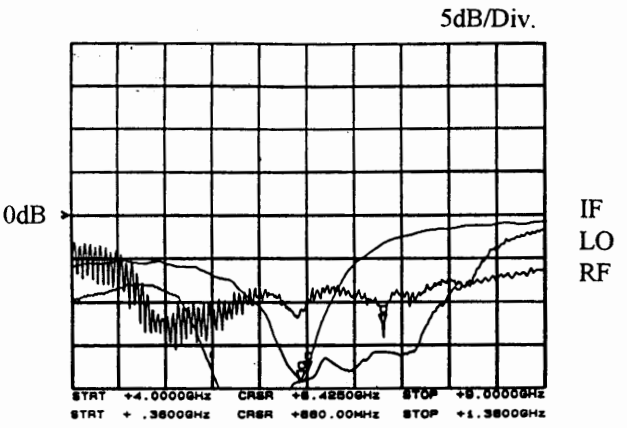

Figure 3a. Return loss of the ratrace mixer.

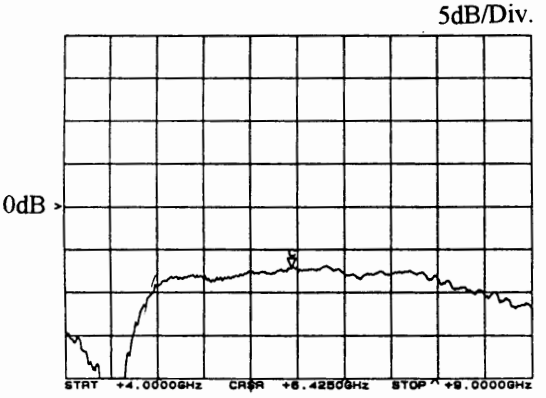

Figure 3b. Conversion loss of the ratrace mixer.

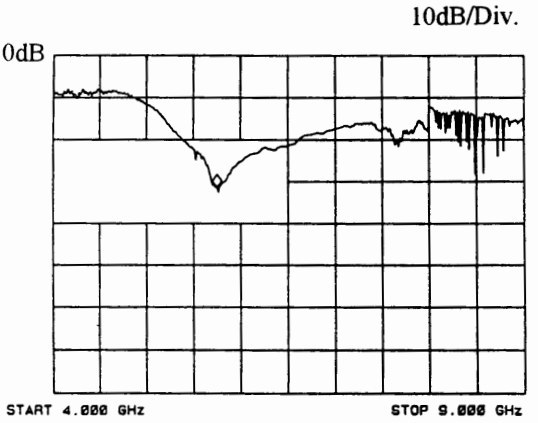

Figure 3c. Isolation of the ratrace mixer.

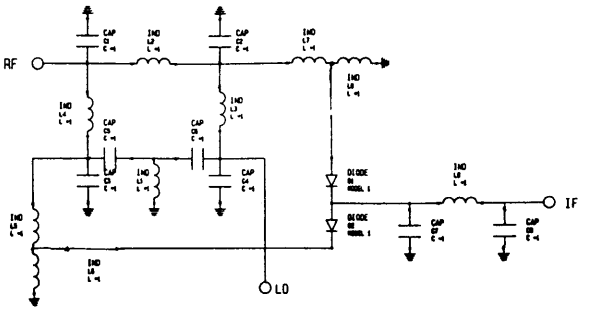

Figure 4. Schematic for the ratrace mixer.

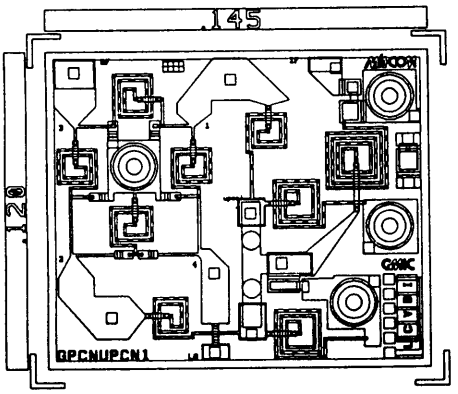

Figure 5. GMIC layout of the ratrace mixer.

Sub Harmonically Pumped Mixer

The sub harmonically pumped mixer was designed around an anti-parallel Schottky diode pair. Figure 6 shows the schematic for this mixer. Lumped element transformers provide matching from the diodes to the appropriate ports.

Shunt resonators are used on either side of the diode pair to provide AC ground for the LO and RF signals. The basic design approach is to deliver maximum RF and LO power to the diode pair with minimal leakage to the IF port. The power level of the LO signal typically needs to be about 10 dB greater than that of the RF signal. This insures that the diodes are driven by the LO signal and not the RF. At any given moment the LO signal is driving one of the two diodes in the pair to conduct while the other is being back biased at the same time. Since the LO signal is conducting for both the positive and negative halves of the wave form, the RF signal mixes with each half equally. The resulting IF signals are at the same frequency but are 180 degrees out of phase thereby canceling each other. The desired IF signal is a product of the RF signal mixing with twice the LO frequency.

The GMIC mask layout for the sub harmonically pumped mixer is shown in Figure 7. The measured performance of a fixtured mixer is shown in Figure 8. Return loss at the RF and IF ports are 8dB and 14dB respectively. The return loss of the LO port is 2.5 dB causing a large portion of the LO power to be reflected. The LO drive level has to be increased somewhat to compensate for this. The optimum power level required for the best conversion loss is +11 dBm. This is higher than originally expected, but can be explained by the poor return loss. The conversion loss of this mixer is 7.6 dB while the RF to IF isolation is 13 dB

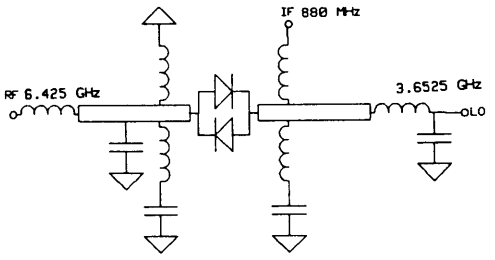

Figure 6. Sub harmonically pumped mixer schematic.

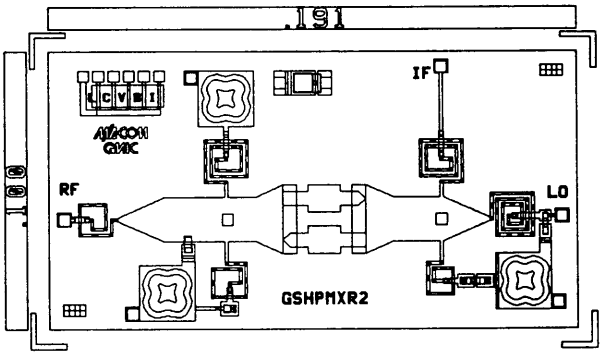

Figure 7. GMIC layout for the sub harmonically pumped mixer.

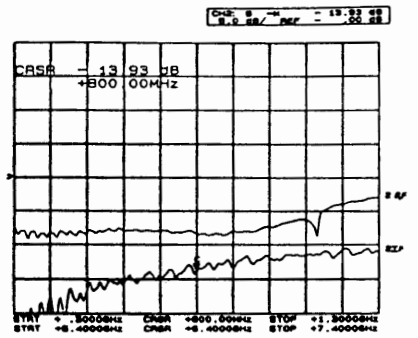

Figure 8. Return loss for the sub harmonically pumped mixer.

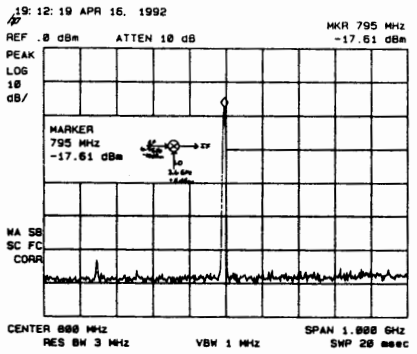

Figure 9. Conversion loss of the sub harmonically pumped mixer.

CONCLUSION

The mixers described in this paper are an example of the types of mixers which can be manufactured with the use of planar technology. This technology offers compact mixers at a very economical cost to the customer. Each of the two mixers has different performance characteristics and tradeoffs.

The ratrace mixer performance is consistent with the simulated results. It's 45% bandwidth makes it a useful circuit for a fairly wide range of applications. This circuit could also be designed and produced in other frequency ranges where the lumped element approach has advantages.

The sub harmonically pumped mixer also performs within the expected design parameters with the exception that the LO return loss resonates at a higher frequency than expected causing a poor return loss at the design frequency. This effect could be resolved with a mask revision to adjust the resonant frequency.

ACKNOWLEDGMENTS

The authors would like to thank all of the people involved in the design and fabrication of the mixers in this paper. Specifically, Scott Doyle and Renato Pantoja for their design expertise and assistance. Also, the GMIC processing and test groups for all their time and effort which they put into this work.

REFERENCES

[1] Joseph Staudinger and Warren Seely, "An Octave Bandwidth 90 Degree Coupler Topology Suitable For MMIC's", Microwave Journal, November 1990, pp. 117-130.

[2] Samuel J. Parisi, "A Lumped Element Rat Race Coupler", Applied Microwave, August/September 1989, pp. 84-93.

[3] Stephen A. Maas, "Microwave Mixers", pp. 264-266, Artech House Inc., 1986.

GMIC Interdigital Filters for Microwave Applications

by Holly A. LaFerrara
M/A-COM, Inc.

Abstract -- The design of interdigital filters utilizing Glass Microwave Integrated Circuitry is presented. The advantages and disadvantages of the interdigital structure are examined. Four interdigital filter designs are discussed, and comparisons are made between predicted results and measured data. Various applications for these filters are investigated. The issues of high-volume production and integration into larger modules are also addressed.

INTRODUCTION

As microwave applications such as cellular telephones, global positioning systems, and bar code readers develop there is more need for small, repeatable, low-cost microwave circuits than ever before. Filters are an essential component in each of these systems. Glass Microwave Integrated Circuits (GMIC) provide an excellent medium for the production of passive filters. The high yields for GMIC filters, along with the ability to combine discrete FETs, MMICs, or other GMIC circuits onto a single piece of substrate provide a path toward low-cost, high-volume production. The interdigital filters discussed in this paper were designed for use in a 6GHz frequency converter.

HIGH-VOLUME PRODUCTION

A GMIC wafer can contain a single circuit that has been stepped and repeated hundreds of times. This allows for mass production once a design is established. Also, several circuits that are intended to form one module can be masked on the same wafer. This allows for testing each component of the module as well as having parts handy to build and test an entire module at once. These filters were included on GMIC wafers containing other circuitry such as amplifiers and multipliers. By utilizing VAP (Volume Automated Processing) techniques and on-wafer testing, the filters can be both tested and tuned on wafer. This eliminates the losses incurred during fixturing and gives a better picture of the actual filter performance.

Filters done on GMIC are ideal candidates for integration into larger modules. It is possible to fabricate entire modules such as T/R modules on a single piece of substrate, because the filters can be attached to other components.

DESIGN ADVANTAGES/DISADVANTAGES

There are several common structures used in the design of microwave filters. For filters designed in microstrip, special care must be taken when choosing a design that gives both low loss and good stopband rejection. Several filter structures were examined, but many were simply too large for use in every location where a filter was needed. Others did not give results that were predictable enough to use in high-volume production. In the trade-off between performance and size, there are several advantages to using GMIC interdigital filters. Figures 1a through 1d show the GMIC CAD layouts of the four interdigital filters used in this

application.

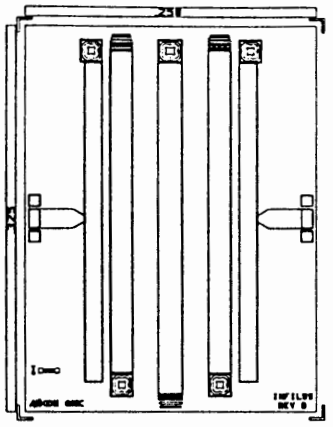

Figure 1a. Layout of GMIC interdigital filter for the transmit chain.

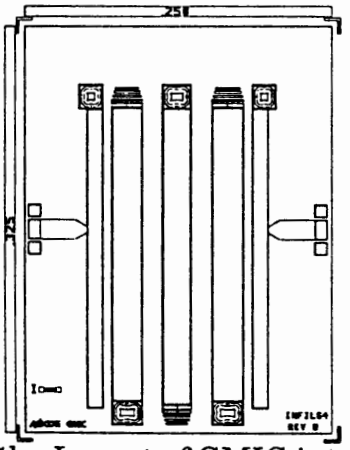

Figure 1b. Layout of GMIC interdigital filter for the receive chain.

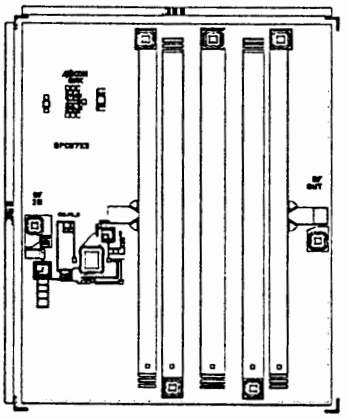

Figure 1c. Layout of GMIC multiplier/filter combination for transmit chain.

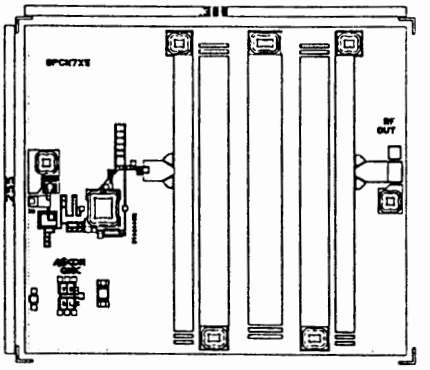

Figure 1d. Layout of GMIC multiplier/filter combination for receive chain

The interdigital structure is the most compact of all distributed filter designs. This makes the interdigital design an outstanding candidate for use in situations where space is at a premium. This design also possesses excellent rejection of the filter's second harmonic. Most filters will resonate at the second harmonic, but the interdigital structure does not resonate until the third harmonic. Thus, a second passband will still appear, but it will be very far out and spurious responses close to the fundamental frequency will be eliminated.

Another advantage of the interdigital design is the ability to vary the impedance of the structure by varying the location of the tap points on the input and output of the filter. By varying the tap point of either side or both sides of the filter, the need for an impedance transformer in a non-50 ohm system is eliminated.

The interdigital filter also possesses low insertion loss. The insertion loss tends to rise with

decreasing bandwidth; however, with careful modelling an optimal structure can be found having an insertion loss of 2.4 dB to 2.6 dB in a fixture. When on-wafer probing techniques are used, the interdigital filter will have losses of 1.7dB to 2 dB due to elimination of losses incurred during fixturing.

One disadvantage of interdigital filters is that they are thought to be lossy due to the effects of dispersion and coupling between lines. For designs having many resonators, loss can be a problem, but for designs with few resonators (here a three-resonator design was used) the insertion loss is comparable to that of other filter structures.

An apparent disadvantage lies in the grounding of alternate ends of the lines. In cases where the grounds are not well characterized, this could be a problem; however, with GMIC, the vias are well characterized and very repeatable. The via element can be modelled as a series resistor and inductor to ground, and can be included in a simulation to give a more accurate response than an ideal ground. This is especially important for filters needing very low loss, because the resistance of the via hole must be accounted for in order to have an accurate model.

Another disadvantage lies of the interdigital structure appears when trying to accurately predict the higher-order coupling effects between lines. Most CAD packages do not have accurate models for more than three coupled line sections. This presents a problem due to the fact that even a basic, three-resonator interdigital filter contains five coupled lines when you include the input and output coupling sections. Ideally, a full electromagnetic simulation should be done to thoroughly understand these effects; however, software availability and time constraints prevented a full-wave analysis. Sonnet[1] simulations were done on some of the crucial junctions, and then the rest of the frequency converter was structured so that there was minimal interference from other chips.

For these filter designs, the Super Compact[2] software package was used to analyze the structure. The Super Compact program contains a multiple-coupled line model which will analyze up to ten coupled line segments. This model proved to be accurate in its predictions of the filter performances.

DESIGN AND ANALYSIS

The initial design equations[3] for interdigital filters of narrow bandwidth are used in conjunction with mapping equations[4] to select a low-pass prototype filter. A low-pass-to-band-pass transformation[5] is then used to estimate the attenuation characteristics of the interdigital filter. The design equations are as follows:

$$\theta_1 = \pi/2 * (1-\pi/2)$$

$$J_{01}/Y_A = 1/\sqrt{(g_0\, g_1\, \omega_1')}\ ,$$

$$J_{k,k+1} = 1/((\omega 1')) * \sqrt{(g_k\, g_{k+1})} \quad k=1 \text{ to } n-1$$

$$J_{n,n+1}/Y_A = 1/\sqrt{g_n\, g_{n+1}\, \omega_1'}$$

$$N_{k,k+1} \Big|_{k=1 \text{to } n-1} = \sqrt{((J_{k,k+1}/Y_A)^2 + (\tan^2\theta_1)/4)}$$

$$M_1 = Y_A((J_{01}/Y_A)\sqrt{h} + 1)$$

$$M_n = Y_A((J_{n,n+1}/Y_A)\sqrt{h} + 1)$$

where h is a dimensionless admittance scale factor to be specified arbitrarily so as to give a convenient admittance level in the filter.

For this application, four three-resonator interdigital filter designs were selected. The three-resonator structure was chosen for its small size and low insertion loss characteristics. After the initial parameters were generated from the equations, the design was simulated using Super Compact PC. The resonator lengths, widths, and spacings were then optimized to obtain the desired performance. Figures 2, 3, 4, and 5 provide comparisons between the simulated and measured data for the four interdigital filters that were designed.

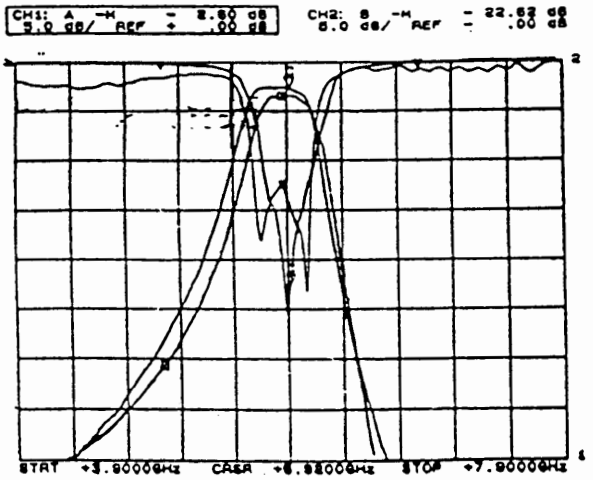

Figure 2. Comparison between simulated and measured data for GMIC interdigital filter at f=5.9 GHz.

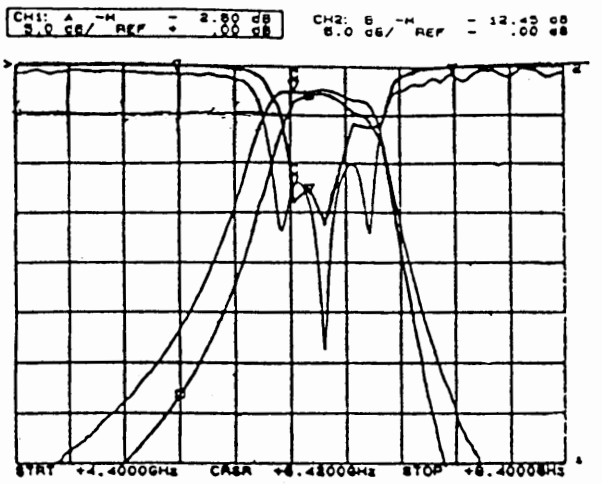

Figure 3. Comparison between simulated and measured data for GMIC interdigital filter at f=6.4 GHz.

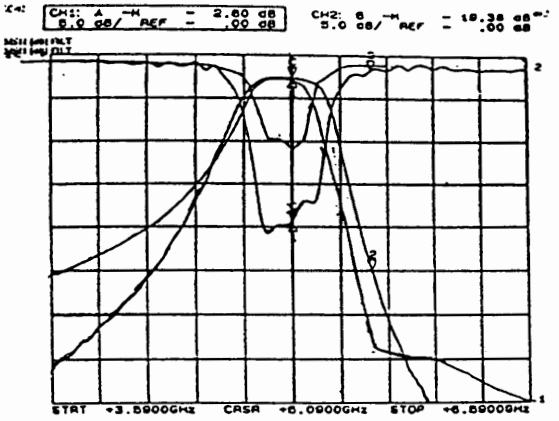

Figure 4. Comparison between simulated and measured data for GMIC interdigital filter at f=5 GHz.

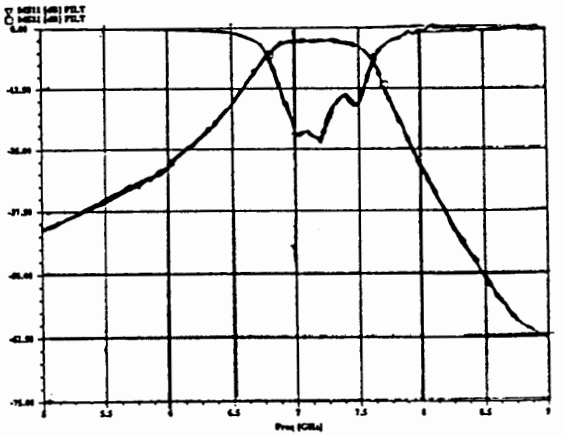

Figure 5. Predicted data for GMIC interdigital filter at f=7.3 GHz.

Excellent results were achieved for these filters. The measured data corresponds well to the software's predictions, and the insertion loss is approximately 2.6dB in a fixture. The filter passband can easily be shifted to achieve better high side or low side rejection. The structure can also be tuned to a slightly lower insertion loss of 2.4dB by adjusting the length of the middle resonator if a lower loss filter is needed.

CONCLUSION

GMIC interdigital filters are excellent for applications where highly reliable, predictable, and small filters are needed. Through careful modelling of the coupled-line structure, an optimal design may be obtained. With the addition of on-wafer probing capability, these filters are excellent candidates for high-volume production using VAP techniques.

ACKNOWLEDGEMENT

The author wishes to thank Paul Schwab, Tim Murphy, and Scott Doyle for their guidance and advice. Thanks also go to Bill Foley and Rick Gibson for help with fixturing and testing these designs.

REFERENCES

[1] Sonnet Software, Inc., Liverpool, NY, Sonnet is a registered trademark.
[2] Compact Software, Patterson, NJ, Super Compact is a registered trademark.
[3] G.L.Matthei, L.Young, and E.M.T.Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures, p. 617.* New York: McGraw-Hill, 1964.
[4] G.L.Matthei, L.Young, and E.M.T.Jones, *pp. 617-627.*
[5] G.L.Matthei, L.Young, and E.M.T.Jones, *pp. 617-627.*

Dual-Use Technologies

Session Chairperson: David Sprague, *The Strategy Group (Martinez, CA)*

**Paper presented by Ratan Bhatia.*

An Evolving Strategy for Dual-Use Microwave Instrumentation

John Minck
Stanford Park Division
Hewlett-Packard Co.

Presented at
Wireless Symposium
and Exibition

HEWLETT PACKARD

Outline

- The 1950-1990 microwave era
- The historical bias toward DOD
- The evolving impact on MW product strategies
- Some observations & examples for 1990-onward

Slide 2 HEWLETT PACKARD

Today I hope to offer a few comments and observations about the evolution of microwave instrumentation product strategies. Certainly, many if not most people would acknowledge that the "golden age" of MW systems and instrumentation occurred during the decades of the '50s to '90s.

The microwave business situation outlook today is partly the result of the DOD dominance through the last 40 years. And the big surge of the '80s further warped the balance. I'll try and emphasize what we will need to do to succeed in the decade of the '90s and onward.

The 1950-1990 Microwave Era

- The post-WWII decades
- Commmercial microwave systems technology lagged Aerospace
  — Communications, radar, navigation
- Influence of strategic weapons race (Korean/Vietnam conflicts)
- Commercial systems became somewhat dependent on DOD technologies and funding
- Instrumentation tended to lag system test needs

Slide 3 HEWLETT PACKARD

Looking backward doesn't help much with business, other than to realize how the "easy" microwave years owed a lot to the pervasive DOD funding windfalls of those years. Component technology, system capabilities, computer and communication breakthroughs pioneered by the military sector helped in the emerging commercial sectors.

While MW system technology drivers would come from both the DOD and commercial sector, DOD tended to dominate, if for no other other reason than its considerable funding power. Given that model, the instrument manufacturers usually found that product definitions which favored DOD requirements were virtually always successful.

At the same time, many of the instrument introductions tended to lag the system requirements, partly because the designers wanted to build the highest-performance they could manage. "Good enough" wasn't as likely to hit a product home run as the highest stability or agility.

The Evolving Impact on MW Product Strategy

- The "Ideal" MW instrument product strategy
- Full-feature sets
- All bells and whistles
- Inelastic demand (Aerospace Funding)
- High performance/high price

Slide 4

HEWLETT PACKARD

When there are legends of customers ready to take high-performance instruments off your hands at high prices, limited R&D resources push the decision-maker to favor a feature set which does it all. Wider frequency spans, more comprehensive modulation, higher stabilities and agilities, and more importantly, a horsepower race on accuracies all sold products.

The thinking prevailed that as long as a commercial customer, who only needs a subset of the full feature set, can get the capability with a higher-priced product, let's take those who can scrape up the money, and forget those who can't because the optimum return still looks good. I don't want to overdo the DOD argument, because there were many companies who targetted the commercial niche well. Bird power meters, IFR test sets, and others are just a few which come to mind.

Catagories of Instruments

DUAL-USE "Generic" Instruments	SINGLE-USE Application-Oriented
Vector Network Analyzers	Signal Generators
Oscilloscopes	Counters
Sweepers	Test Sets
Scalar Network Analyzers	Agile-Simulators
Spectrum Analyzers	"Personality" Spectrum Analyzers

Slide 5

HEWLETT PACKARD

It seems to me that an important distinction can be made between instrument types, which might be divided into two groups. Most "general purpose" instruments such as oscilloscopes, spectrum analyzers, power supplies, and others serve both commercial and DOD markets with little need for differentiation. In addition, component design tools, specifically vector network analyzers (VNAs), scalar network analyzers (SNAs), and the multi-band sweepers that drive them also have fitted into buying plans of both user sectors.

I'm begging the question a bit on instrument pricing. It is true that VNAs that cost $200,000 (without wheels), often were not cost justified by customers working on purely commercial components. But typically the component manufacturers were also working both sides of the user street, and were able to fill commercial and DOD needs.

It is in the RF and microwave-system test instruments that single-use was most noticed, and most confining. Conventional signal generators which tried to directly match radar and EW needs tended to outprice themselves for pure commercial. DOD-use instruments often had frequency ranges that split commercial bands like 3.9 to 4.4 GHz. Same story for DOD test sets. Recent additions to product lines such as fast-agile-simulators and vector modulation generators also directly focused on DOD applications, as revealed by their high prices.

Dual-Use Requirements for the Decade of the 90's

- Support Time-to-market initiatives
- Software re-configurable
- Hardware re-configurable (VXI, MMS)
- Real-life simulations
- Instrumentation strategies that lead system needs

Slide 6

HEWLETT PACKARD

In the '90s, business will divide into the nimble and the dead. Time-to-market is not just a catchy phrase rolling off our lips, but a new culture for design engineers. Fast-track design projects will dominate, and design engineers will need to bring real-life complex/impaired signal environments right down to the design bench to stress-test circuits and equalizers before they get to field testing environments.

Test equipment, as it is, will need to be highly-reconfigurable, both for hardware, and for software. VXI and MMS are vehicles which do some of this in hardware terms. Large, highly-capable signal systems such as agile simulators are the other example, which can reconfigure the entire signal environment instantly.

Finally, most marketing departments have gotten the message. No more technology horsepower races. Even DOD wants "just enough." And they are also buying "from-the-shelf" by directive.

Swords to Plowshares

- Turning modern DOD technologies to commercial success
- Cellular and PCN—agilities and spread spectrum
- Video and HDTV revolution—compression and coding
- Digital revolution continues—DSP
- MTBFs going up, BITE for digital circuitry

Slide 7

HEWLETT PACKARD

This conference and others are trying to figure out where we go from here? Not an easy task. There are intriguing success stories of military technology invading the commercial sector. These are just a couple of examples. We've all heard of the Pacific Rim making successes of US initial breakthroughs, and it is up to us to extend from those examples.

There are many non-intuitive things going to happen before 2000. When you can now buy a TV set which has not been tested in the conventional sense, because of sophisticated TQM and statistical quality control, you had better realize that test instrumentation can't be very far behind. The ideal instrument would be self testing. (Perhaps some traceable links to national standards will be allowed.)

As digital continues to invade the systems and the test instruments, abbreviated testing will be the norm. After all, you now buy complex computers in pieces, and assemble them at home. Digital interfaces make a BIG difference.

Impact on Instrumentation Strategies

- John Young statement to SIA
- Fast-track projects
- Simulation capabilities
- New paradigms

Slide 8 HEWLETT PACKARD

The simple message is that everyone needs to start writing on a clean sheet. Don't expect things to be the same, as they were under DOD cultures. Expect big discontinuities in testing strategies and test equipment

Is there any reasonable future for those of use with 40 years in instruments and measurements? Absolutely. I have appended a summary of some comments made recently by John Young just before his retirement as CEO of HP. John has an exciting vision. It is up to us to fill in the blanks.

Young at SIA

November 3, 1992

In his last public address prior to retiring as HP president and chief executive officer, John Young told a Semiconductor Industry Association (SIA) audience in San Jose, California, on October 28 that despite very real problems, the glory days are not gone: "Our industry's prospects can be even more exciting than its past."

Predicting that the Information Age will come during the lifetime of those in the room ("even for those of us who are retiring"), Young said three important technological trends are driving this change:

- The accelerating performance of technology — which has already made it possible to provide 50 to 75 percent more hardware performance every year — and the likelihood that by the end of this decade, software applications will be able to tap that potential. The cost of a computer cycle at the end of the decade will be about one-hundredth of what it is today, Young predicted. "Information technology will be as pervasive as electricity," he said.

- A trend under way toward development of an "information utility" as telecommunications and broadcasting move to digital technology and datacom, telecom and entertainment converge. Young sees ahead a network of networks stacked with services, intelligent directories, the Library of Congress on-line, the expertise of the world's best doctors, and far more.

- Information appliances. "The hundreds and thousands of new information appliances that tap into the utility will capitalize on U.S. strengths — sophisticated software solutions, multimedia, microprocessors and specialized ICs, and the willingness of count less entrepreneurs to exploit the almost infinite opportunities that will exist." This will offer opportunities for collaboration and "for bridging the distances and disciplines that divide us." Young sees the government's role as facilitator, not builder, with public funding focussed on research into architectures, switching and security. Public policy should smooth the way in such areas as standards, protection of intellectual property and the allocation of communication frequencies.

The High Performance Computing and Communications Initiative (HPPI), a government-backed network tying together the U.S. supercomputer centers, is a good start, Young believes. It addresses "grand challenges" for technical cooperation such as cancer, air pollution, energy conservation and superconductors.

Young was a founding member of the Computer Systems Policy Project (CSPP) made up of the heads of the largest U.S. computer companies. CSPP supports HCCI and believes further that the U.S. should aim for an expanded network with millions of nodes that would be widely accessible to the public. "Such a national information infrastructure would spur economic development — creating high value-added and high-paying jobs — in ways we can't even foresee," Young declared.

AFFORDABLE MMIC POWER AMPLIFIERS FOR 2.4 AND 5.8 GHz SPREAD-SPECTRUM APPLICATIONS

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ABSTRACT:

This paper describes the design and performance of fully integrated, low-cost MMIC power amplifiers for 2.4 and 5.8 GHz commercial Spread-Spectrum applications. Both MMIC amplifier designs deliver high gain and high-power in a modest chip area of only 3.0 x 1.7 mm with integrated bias networks, thereby providing an affordable solution to general purpose power amplifiers required in unlicensed commercial spread-spectrum transceivers. These PAs are optimized for +5V supply operation. The 2.4 GHz chip is discussed in greater detail, since same issues, tradeoffs and topology considerations apply to the 5.8 GHz amplifier.

INTRODUCTION:

In applications above L-band where Silicon devices are used, GaAs MMIC technology offers improved gain per stage and better multistage power added efficiency . In addition , MMIC technology also provides size reduction, improved reliability, lower parts count, lower cost and simpler component assembly. The amplifiers discussed here are designed to provide affordable solutions to the need for general purpose power amplifiers in unlicensed commercial spread-spectrum transceivers [1]. The FCC authorized frequency bands for Spread-Spectrum systems are 902 to 928 MHz, 2400 to 2483 MHz. and 5725 to 5850 MHz. The requirements for transmitter power output are +30 dBm EIRP with spread-spectrum modulation. With typical antenna gains in 0 to 3 dBi range , the maximum power output is in the + 27 to +30 dBm range. The two PAs described here are designed to provide greater than +27 dBm power output @ 1dB Gain Compression with +5 V drain supply.

CIRCUIT DESIGN:

Based on the requirements of an existing direct-sequence spread-spectrum system, the following minimum design goals were established for 2.4 and 5.8 GHz power amplifiers

Frequency Band	2.4 GHz +/-50 MHz	5.8 GHz +/-75MHz
Gain	25 dB	20 dB
Power Ouput @ 1dBGC.	+27 dBm	+27 dBm
Power Added Efficiency, ηadd.	20 %	20 %
Input VSWR, max.	2:1	2:1
Output Third Order Intercept Point	35 dBm	35 dBm
Operating Temperature Range	0 to +70 °C	0 to +70 °C

Based on these electrical specifications the circuit topology chosen includes 3-stages with lossy-reactive , lumped-element matching networks for high-gain, high power, high efficiency and small size. The power loading was based on +5 V drain operation . The FETs are biased in Class-AB mode for improved efficiency. Based on measured load-pull data on discrete FETs the optimum power loading is obtained by matching an equivalent source admittance of 47.6 ohms + j5.9 mS per mm of gate-width. The output power density @ 1dB gain compression is about 0.26 watts per mm. Accordingly, a 3mm FET device was chosen for the output stage. For the 2.4 GHz. PA , the stage 1 and stage 2 device sizes

were selected as 0.3 mm and 0.6 mm , whereas for the 5.8 GHz PA the stage 1 and 2 device sizes were 0.3 mm and 0.72 mm respectively. This choice was based on achieving high efficiency and ensuring that the first two stages are linear over the operating bandwidth and temperature range. The input, output and interstage matching network topologies were selected to provide optimum power match and flat gain. Other ccnsiderations were unconditional stability, minimum number of elements, bias application and realizability. Further, the output matching on final stage also included 2nd harmonic tuning to increase efficiency. Gate and drain bias networks included sufficient bypass and resistive loading to ensure stable operation. Both PAs are unconditionally stable. The circuit schematics of the two PA designs are shown in Figures 1 and 2.

The circuit analysis included both linear and non-linear simulations in Libra. The large-signal model used was the Curtice-Cubic FET. The model parameters were provided by the MMIC foundry. Modeled amplifier power and effciency were within 1 dB of measured levels.

FABRICATION:

The MMICs were fabricated at a commercial foundry. The active devices are supported by a standard 0.5 micron GaAs MESFET ion-implanted process. Gates are written in E-beam lithograpy and realized in a double recess. The process includes silicon nitride MIM capacitors, tantalum nitride and GaAs resistors, and low-loss transmission line elements. Low-inductive paths are provided through 50 micron diameter via holes. Typical DC parameters for a 1 mm device are Idss=320mA, Vp= -3.5V, Gm=135mS and Vb=15V. Chip area is conserved by distributing bypass MIM capacitors around via pads. This technique has been previously presented in [2].

MEASURED RESULTS:

The first-pass results on these MMICs have met all the design specifications. The photo of the MMICs is shown in Figures 3 and 4. The chip size of the 2.4 GHz MMIC is 3.0 x 1.7 x 0.1 mm and that of the 5.8 GHz. MMIC is 3.0 x 1.9 x 0.1 mm. The measured data is taken in a low-cost surface- mount package. The only external components required are two 0.1μF bypass capacitors for the positive and negative bias leads placed close to the chip to prevent any bias induced oscillations. The packaged chip assemblies are shown in Figures 5 and 6 . The measured gain and return loss for the 2.4 GHz MMIC is shown in Figure 7 and that for 5.8 GHz MMIC in Figure 8. Clearly, the 2.4 GHz PA has typical small-signal gain of 28 to 30 dB and less than -12 dB input return loss over a bandwidth in excess of the desired 2.4 to 2.483 GHz . The 5.8 GHz PA provides a typical gain of 23 dB and less than -12 dB of input return loss over a bandwidth in excess of the desired 5.725 to 5.850 GHz. Small-signal data is taken @ 25 ° C at a bias of +5 V, 422 mA quiescent current .

The measured output power and efficiency of the 2.4 GHz chip is displayed in Figures 9 through 12. Figure 9 shows the 1dB gain compression output power vs frequency for a 35% Idss bias. The 1dB gain compression power performance trade-off with operating point (drain bias and quiescent current) is illustrated in Figure 10. Similarly, the efficiency impact of operating point is shown in Figure 11. It can be seen that power output greater than 1 watt and associated power-added efficiency above 32% has been typically achieved from this MMIC. Power and efficiency at Vds=+5V are typically +28dBm and 25% respectively. Since the primary application of this chip is for direct sequence spread-spectrum modulated signals, Figure 12 has been included to illustrate the effect of operating point on spectral regrowth of the second (5th order) side-lobes. The power levels displayed are associated with a 3 dB degradation in the second (5th order side-lobes). Typical 3rd order output intercept point for the 2.4 GHz PA at 2.45GHz is about 36dBm at Vds=+5V.

Under similar bias conditions the 5.8 GHz PA delivers a minimum output power of 26 dBm with associated power-added efficiency of 18 % as shown in Figure 13 and 14. At appropriate bias levels, 1 watt power output and associated power added efficiencies above 20% are typically measured. The third-order intercept point at 5.85 GHz is typically 35 dBm at Vds=+5V.

CONCLUSIONS:

The design and performance results of 2.4 GHz and 5.8 GHz MMIC power amplifiers for spread-spectrum applications have been presented. These PAs provide a very compact, reliable, simple, stand-alone, and low-cost alternative to conventional hybrid and discrete power amplifiers. Power and efficiency performance is quite good for a fully integrated power MMIC. Both PAs provide useful gains in excess of 20 dB and P-1dB power output of 0.5 W, compatible with the typical requirements of unlicensed spread-spectrum systems. Further, these results were achieved on a first-pass with an overall design, fabrication and test cycle time of about 2.5 months.

REFERENCES:

[1] A. Ward, " Survey of Component Technologies for 900, 2400 and 5700 MHz Unlicensed Spread Spectrum Transceivers," RF Expo-West Proceedings, pp197-208, March 1992.

[2] T. Apel & S. Ludvik, " A Compact, High Gain, 2-20 GHz MMIC Amplifier," 1992 IEEE Journal of Solid State Circuits, Vol.27, No.10, pp. 1463-1469, Oct. 1992.

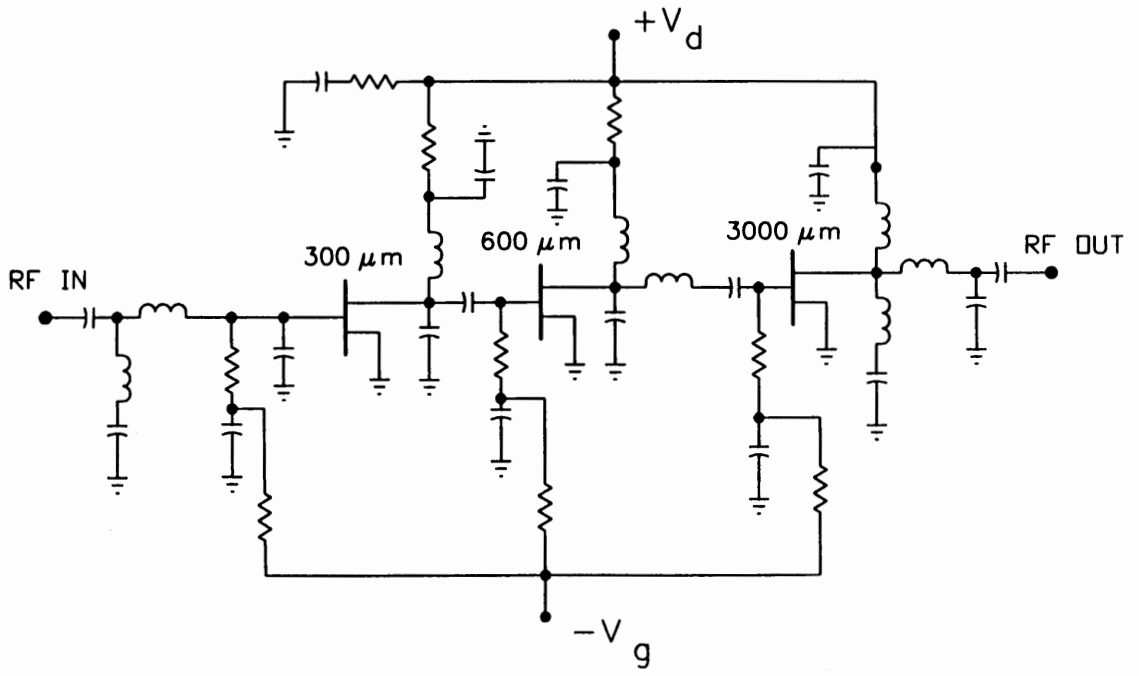

Figure 1. 2.4 GHz MMIC Schematic

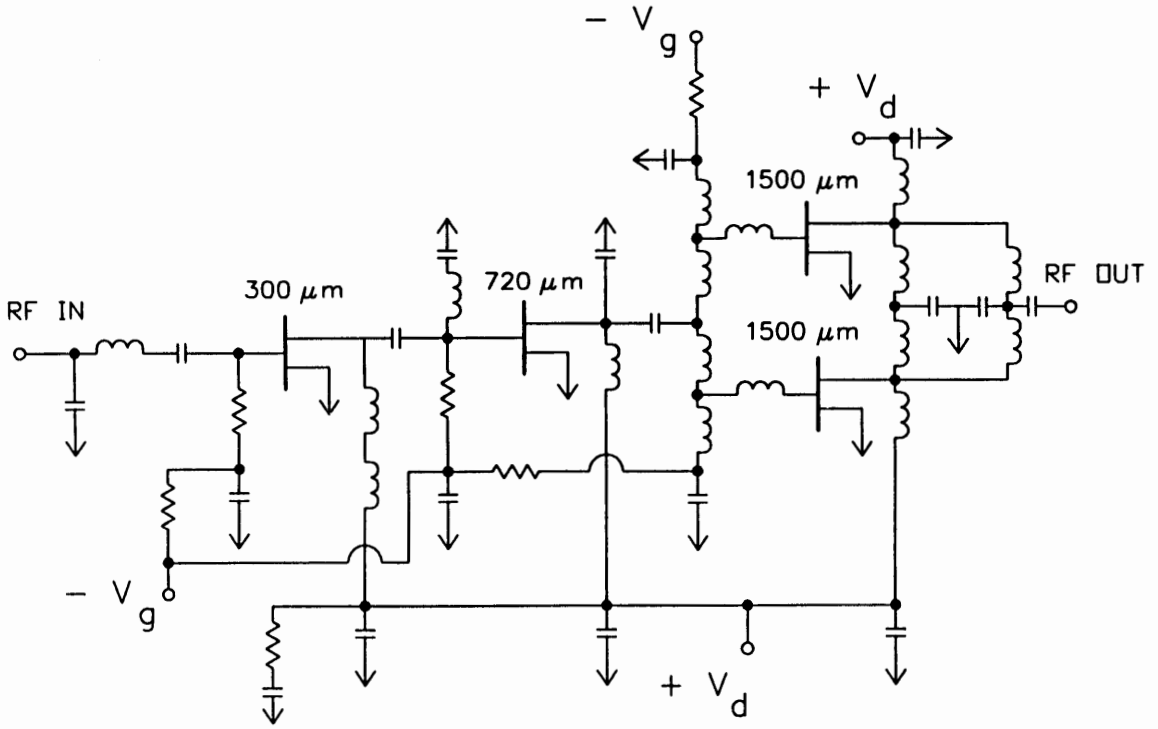

Figure 2. 5.8 GHz MMIC Schematic

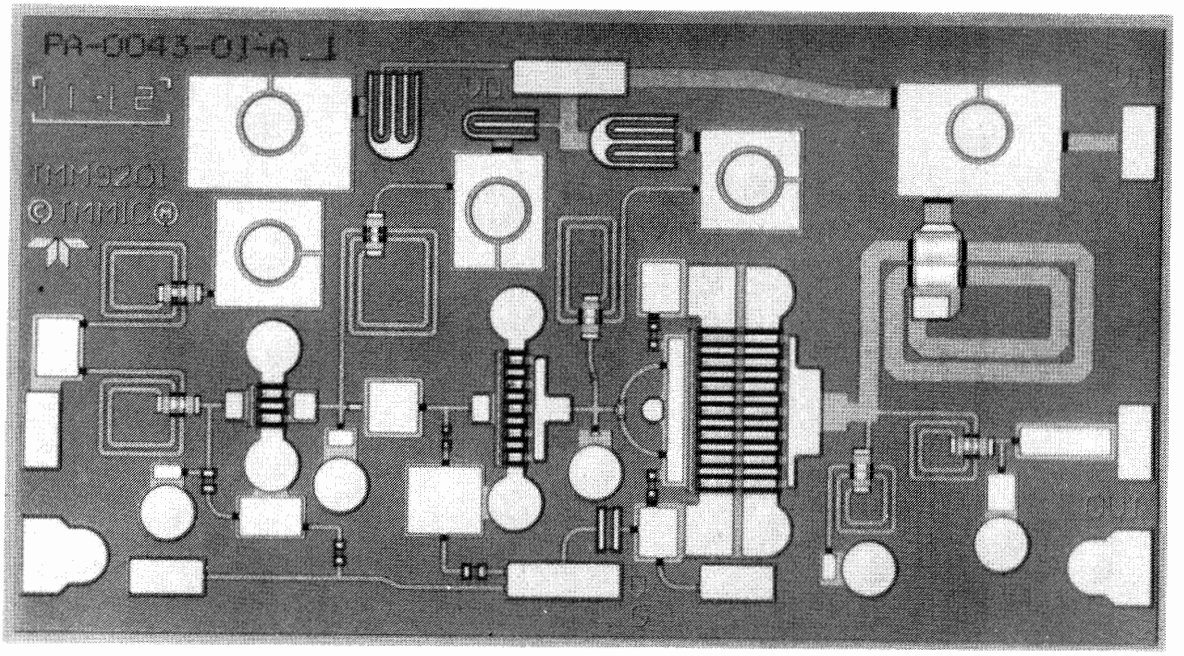

Figure 3. Photo of the 2.4 GHz MMIC PA

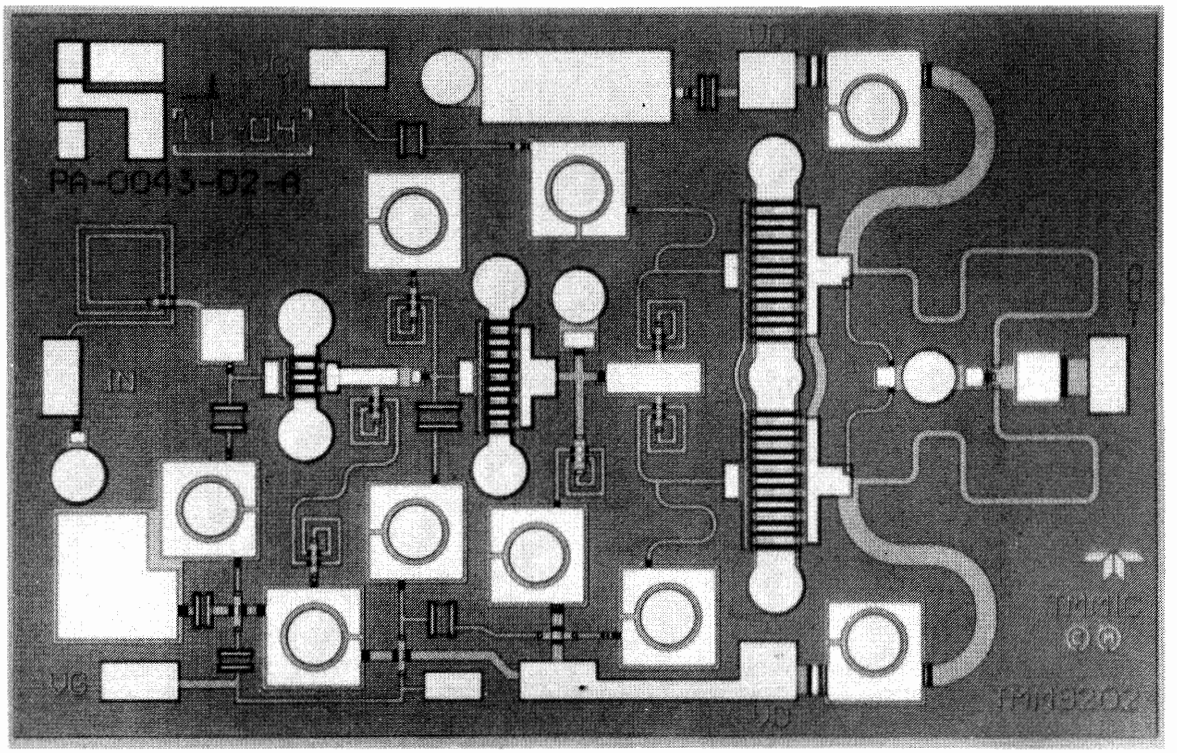

Figure 4. Photo of the 5.8 GHz MMIC PA

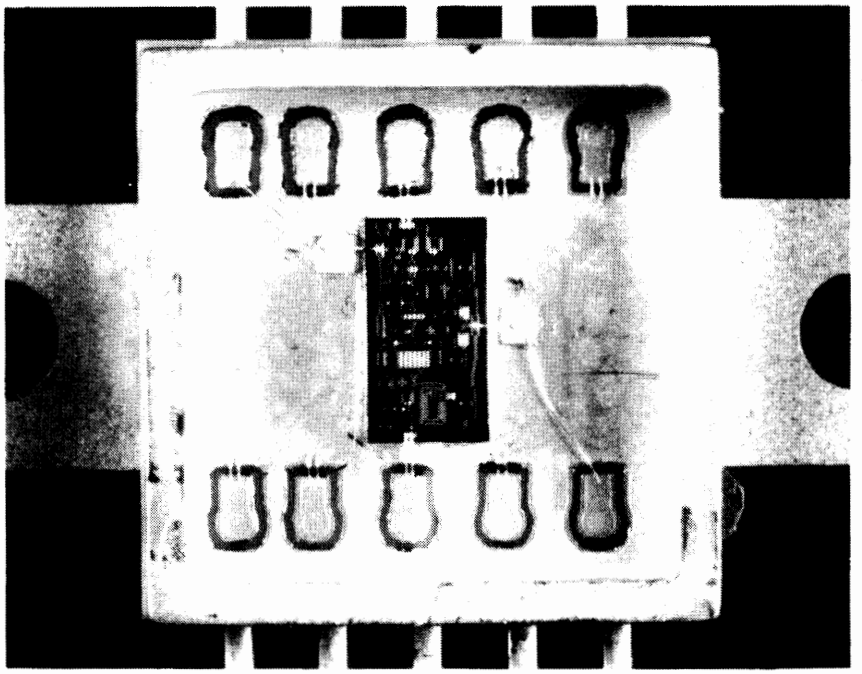

Figure 5. Photo of 2.4 GHz MMIC Assembly in Package

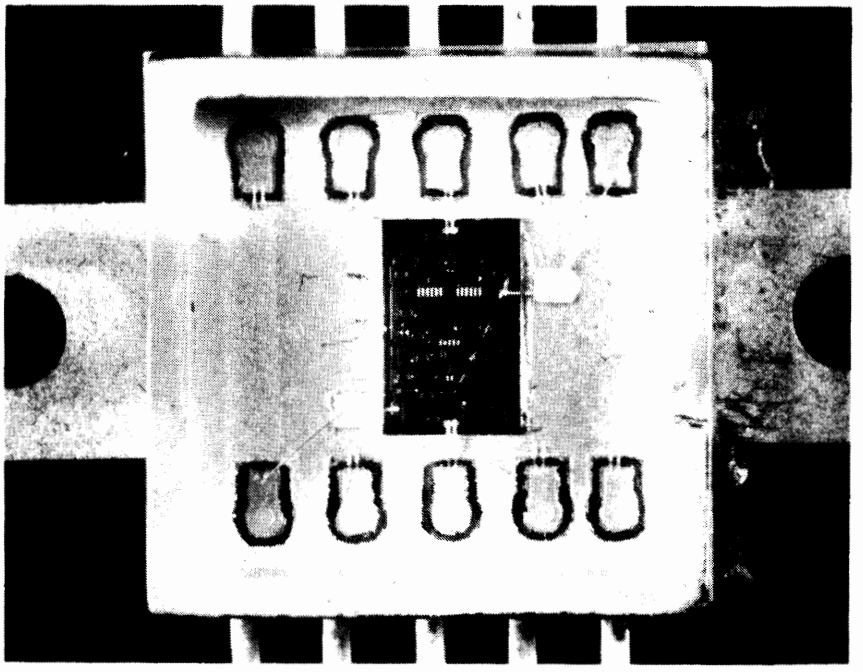

Figure 6. Photo of 5.8 GHz MMIC Assembly in Package

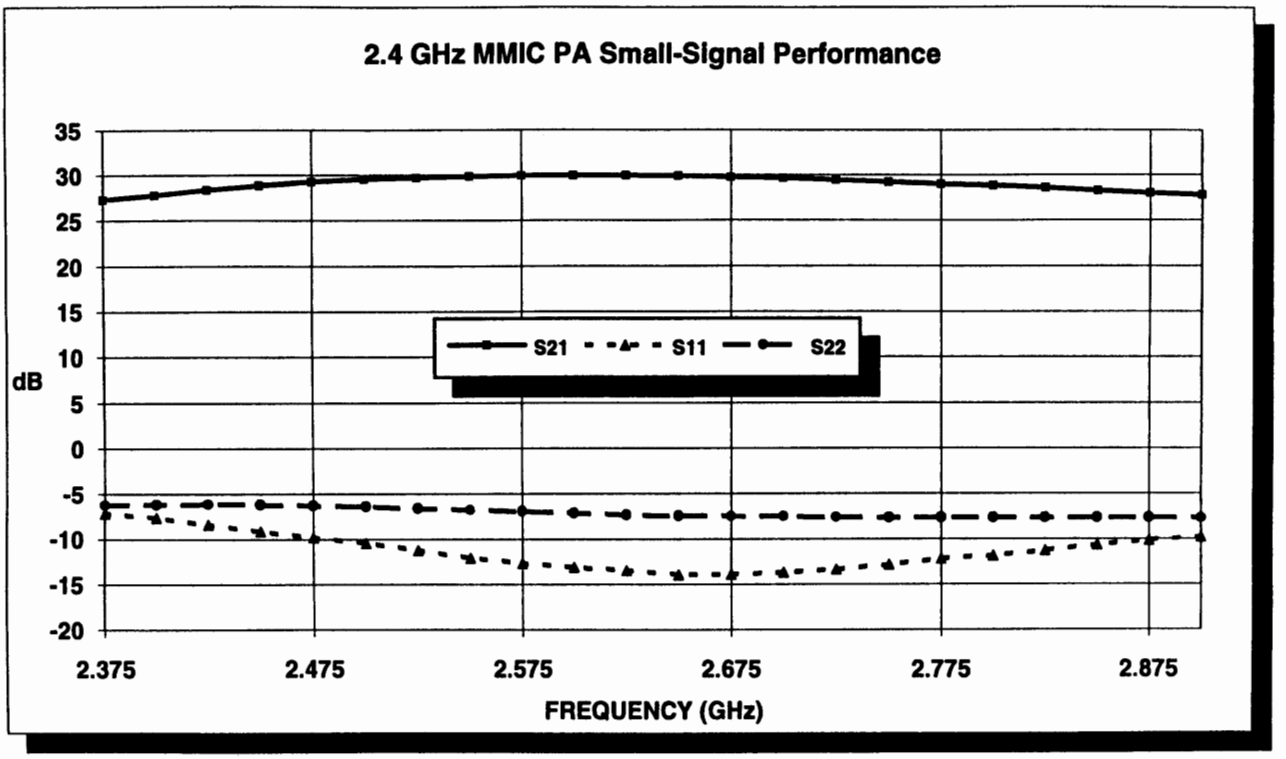

Figure 7. Measured Gain & Return Loss of 2.4 GHz PA

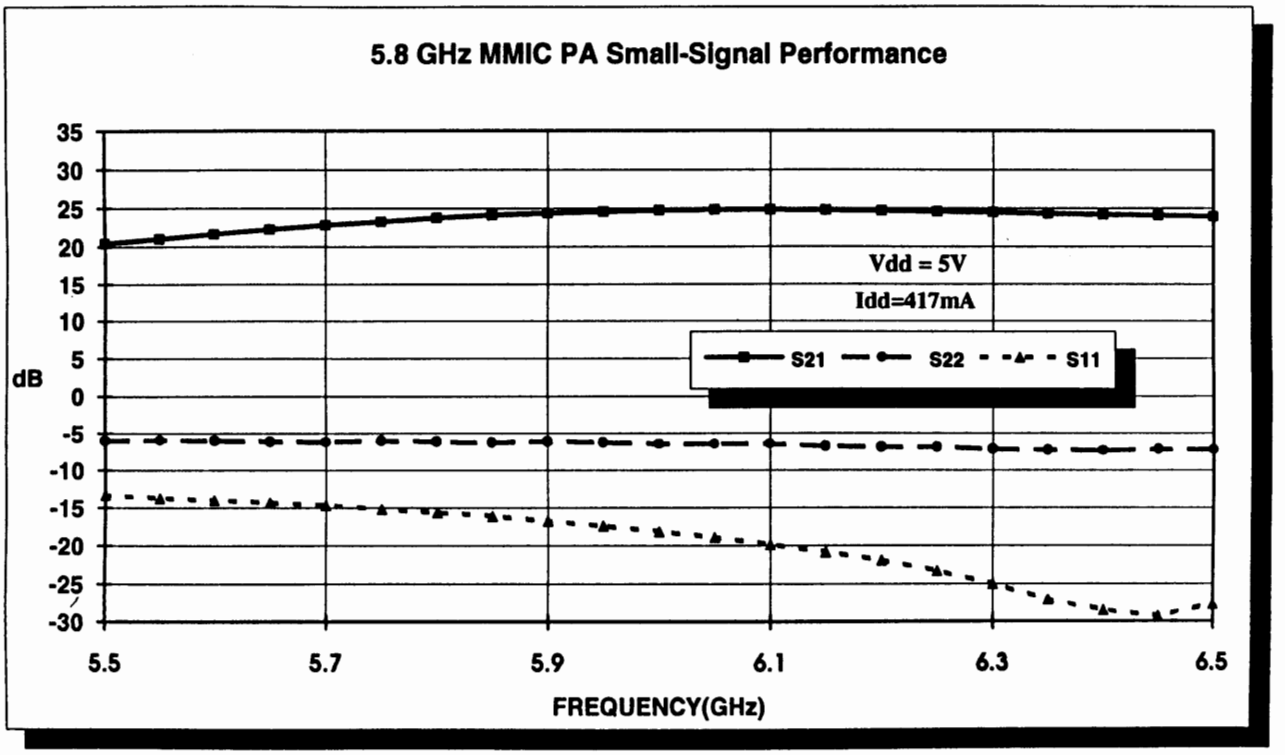

Figure 8. Measured Gain & Return Loss of 5.8 GHz PA

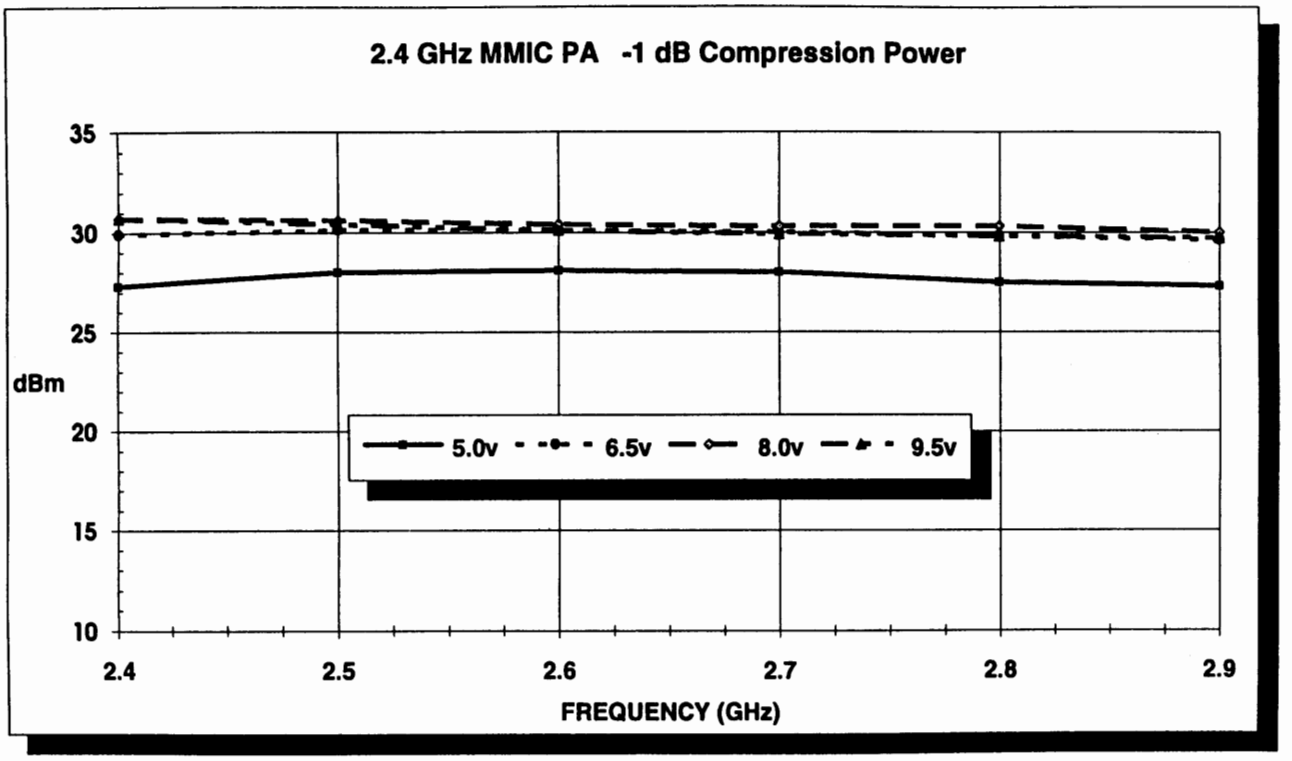

Figure 9. Measured Output Power Response of 2.4 GHz PA

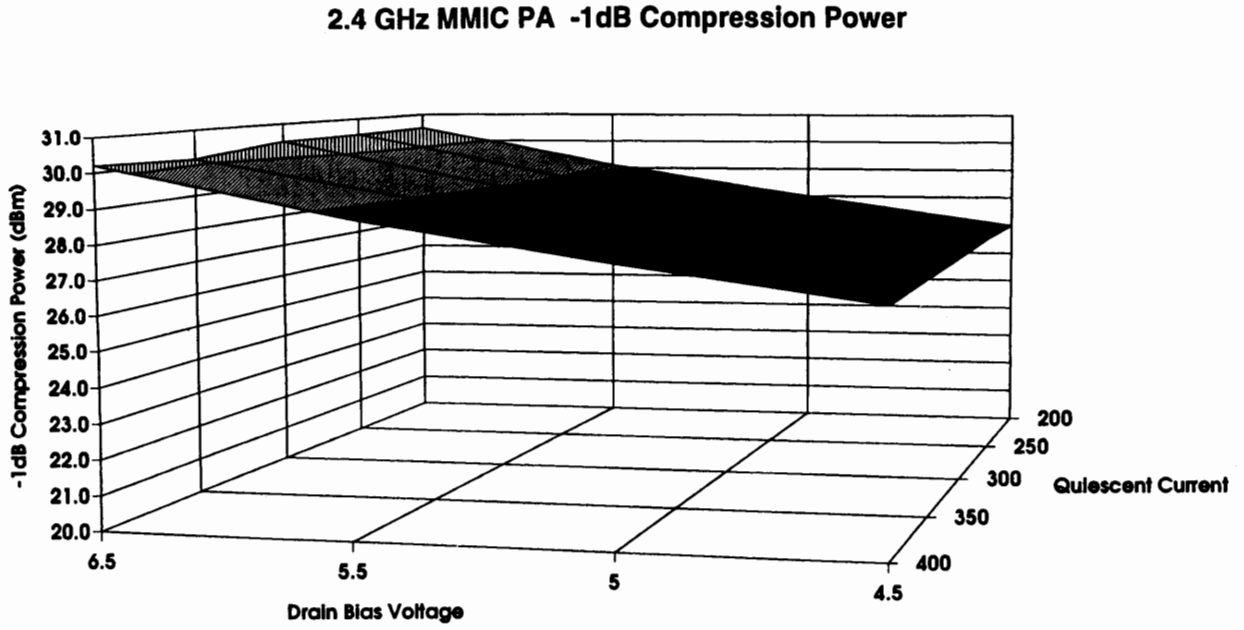

Figure 10. Measured Output Power Vs Drain Bias & Current of 2.4 GHz PA

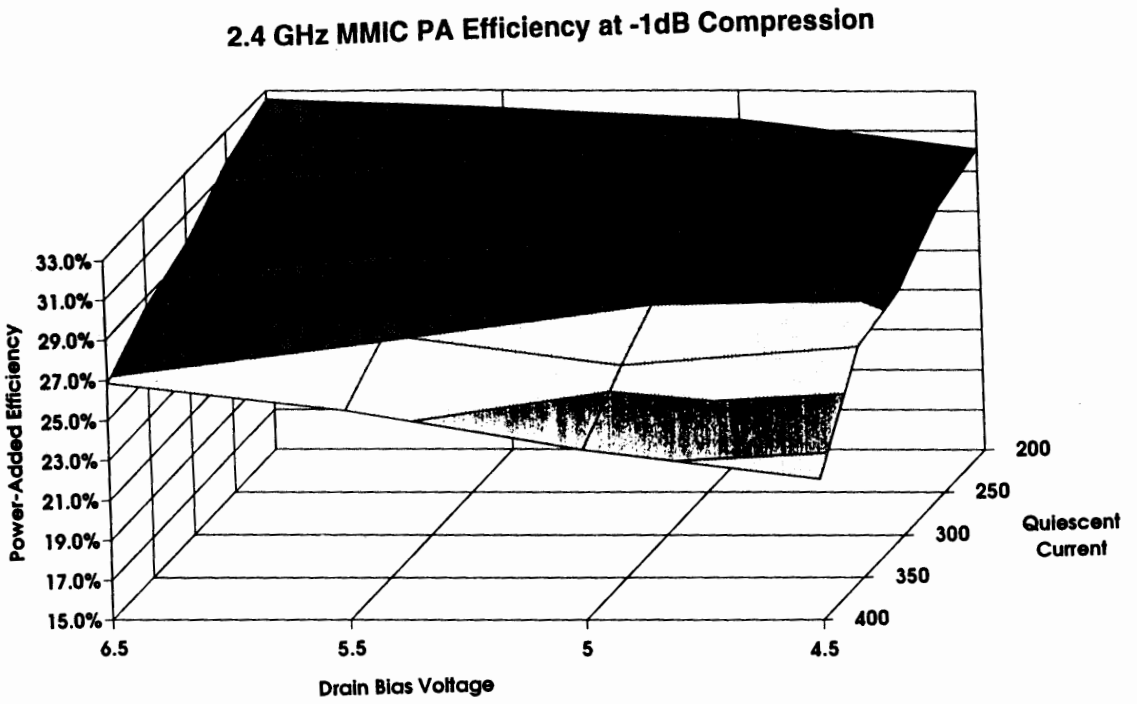

Figure 11. Measured Efficiency Vs Drain Bias & Current of 2.4 GHz PA

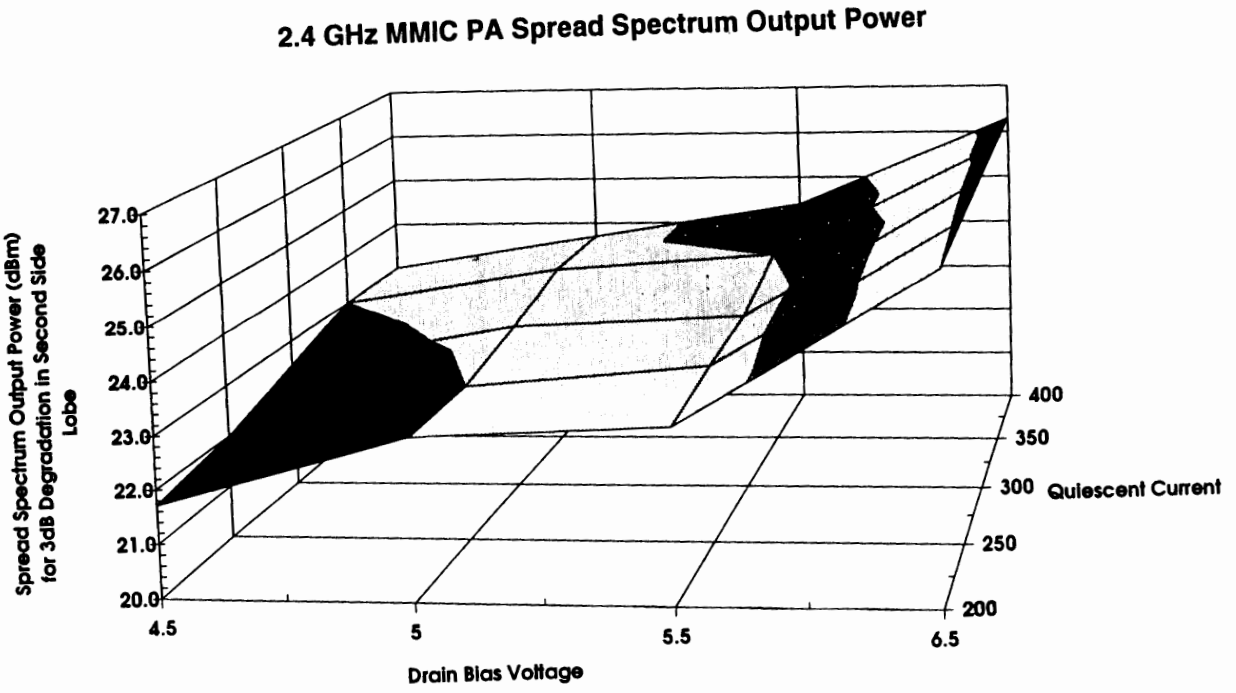

Figure 12. Spread Spectrum Output Power for 3dB Degradation in side-lobe Vs Drain Bias and Current of 2.4 GHz PA

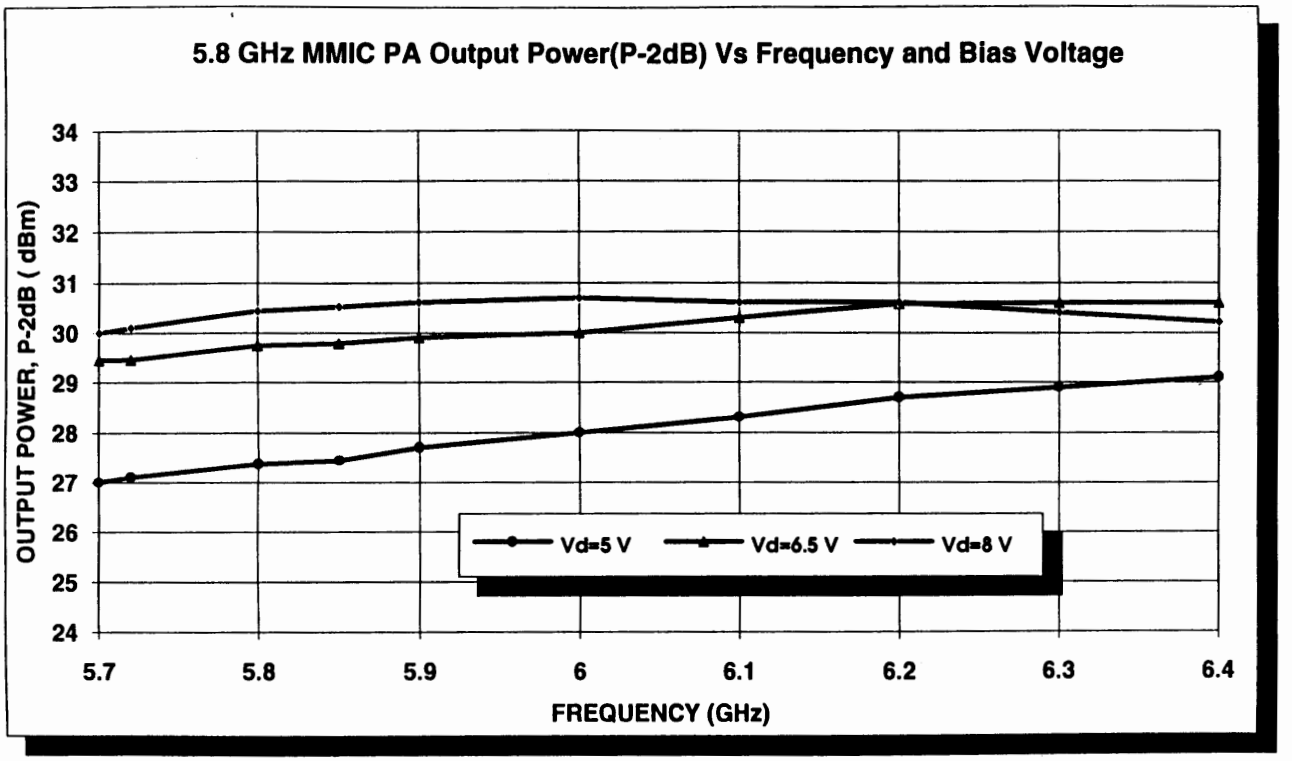

Figure 13. Measured Output Power Response of 5.8 GHz PA

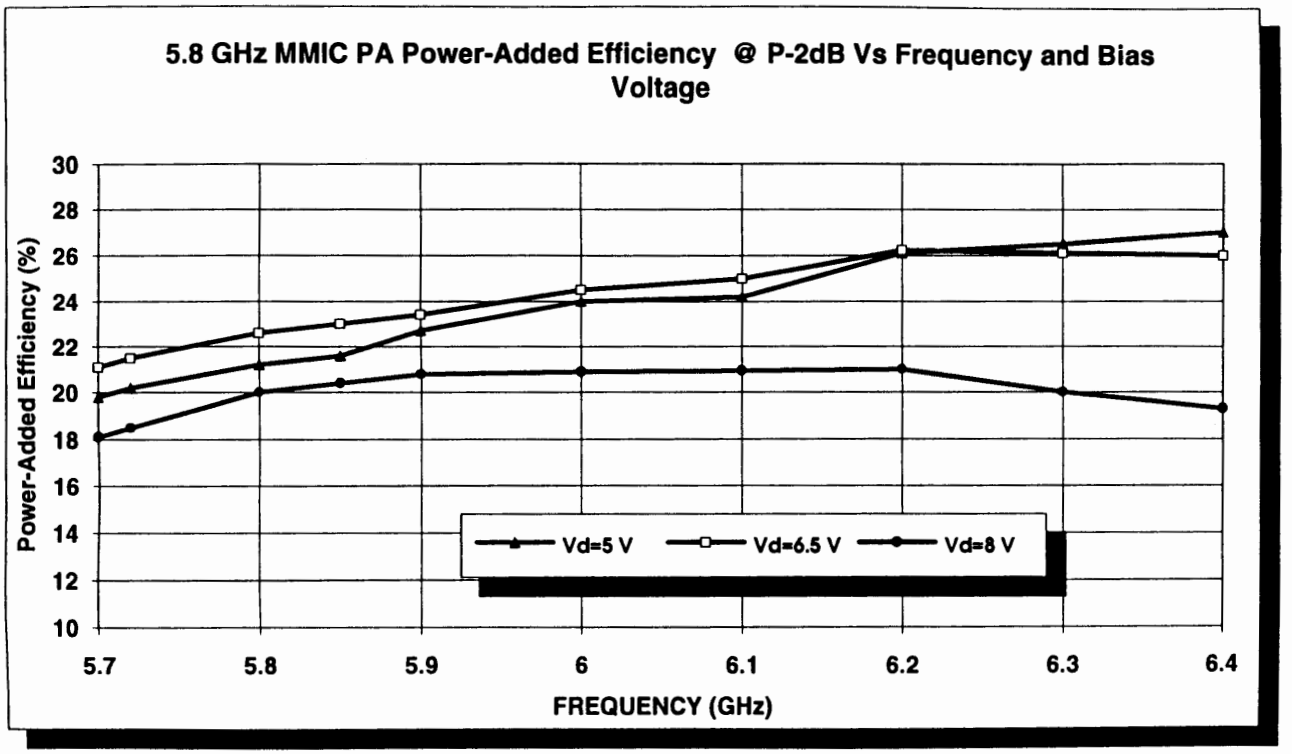

Figure 14. Measured Efficiency of the 5.8 GHz PA

Measurement Techniques for Wireless Systems

Session Chairperson: Ben Zarlingo, *Hewlett-Packard Co., Lake Stevens Instrument Division (Everett, WA)*

A Better Way to Design Tomorrow's Wireless Communications Systems Using RF Analyzers with Advanced DSP

Ben Zarlingo, Hewlett-Packard Co.

Abstract: Designing tomorrow's wireless communications equipment means working with burst and vector modulated signals. These signals are difficult to characterize using traditional instruments. This paper discusses real world measurements on these signals and systems, made with analyzers that combine traditional approaches and advanced DSP (Digital Signal Processing).

While the RF spectrum that we all must share is limited, the demands for use of this spectrum are growing exponentially. That situation, and the factors driving it are well known to everyone in the industry. It is a situation containing both good news and bad news for RF design engineers.

The good news is the expanded need for RF design expertise to develop these new systems. New systems to transmit more of the same information (such as voice and video) and new systems to transmit an ever-larger quantity of new information (mostly data of one type or another). In any event, more and more information is being sent in digital form, whether it is data or just voice. This increase in the use of digital techniques is often a result of the need to send more information in the same "space"--to make the most efficient use of the RF spectrum.

But of course this is where the bad news comes in. Designing tomorrow's digital wireless communications systems involves working with signals that are burst, transient (or non-repeating), and complex modulated. A far cry from the past, where the information was usually encoded as continuous AM or FM, and where high performance signal analysis could be done with tools such as spectrum analyzers, counters, power meters and so on.

On today's complex signals, performing even the simplest traditional measurements is a difficult challenge. The process of RF design involves nearly countless measurements of simple parameters such as frequency, power, distortion, noise, etc. But as engineers have discovered, making these measurements with speed and precision on complex modulated and/or time-varying signals is next to impossible.

Designers long to reach for traditional tools such as oscilloscopes and spectrum analyzers, and to make the traditional measurements that will give them the insight to be able to use accumulated judgment, experience and talent and established design techniques to quickly and efficiently design circuits and systems that meet stringent requirements.

But many measurement tools have not been able to keep up with these new signals. While today's digital oscilloscopes are excellent tools for viewing complex and time-varying signals, their 8-bit A/D converters do not have the resolution and accuracy to take over the functions traditionally performed by spectrum analyzers.

And swept spectrum analyzers offer high performance, but are designed for continuous signals. Any signal that is time-variant--that is, a signal that changes during a spectrum analyzer's sweep time--demands new tools and techniques.

For the designer, several approaches have emerged. Traditional tools have been enhanced. Some spectrum analyzers now have time-gated signal analysis capability, allowing them to measure certain time-variant signals which repeat consistently, and where an external trigger signal is available. However burst signals of short duration may limit the frequency resolution and dynamic range of these measurements, due to the need to use wide, fast-settling RBW filter settings.

New tools have been developed, such as modulation domain analyzers. These analyzers can measure the frequency behavior of rapidly time-varying signals by implementing very fast zero-dead-time counters. Their analysis is limited to frequency and phase, since they cannot measure amplitude or distortion, and cannot separate multiple signals from one another.

But what designers need are tools that give them traditional measurement functions and insight and allow them to make tests throughout the block diagram of communication systems--all frequencies, including baseband through IF and RF. Tools with the performance and broad capability that a spectrum analyzers offer in traditional RF design. Tests that correspond with those they have developed for simpler signals and systems.

Fortunately the digitizing and digital signal processing technologies that have created these complex and time-varying signals have also made new measurement solutions possible--both new tools and new measurements to go along with them. This paper will demonstrate several new or enhanced measurements that are useful in the design of digital wireless communications systems.

These measurements are made with the HP 89440A Vector Signal Analyzer. It covers the baseband-through-RF frequency range of DC to 1.8 GHz with broad measurement capability in the frequency, time and modulation domains. Key innovations of the analyzer include:

- An A/D subsystem with state-of-the art performance of up to 16 bits linearity and up to 22 bits resolution at 25.6 million samples/second
- A high performance digital signal processing subsystem using both proprietary and off-the-shelf elements to produce complex measurement results at up to 60 traces/second
- Advanced digital signal processing techniques including a universal AM/FM/PM demodulator, digital modulation analysis, correlation and coherence functions
- A flexible stimulus source covering the analyzer's entire frequency range with narrowband signals such as sinewaves, chirps, random noise and arbitrary waveforms.

Transient or Burst Signal Measurement

Designing systems using burst or time-varying signals is complicated by the difficulty of making simple, traditional signal quality measurements such as frequency, power, signal/noise, distortion, etc. Any signal which changes during the measurement time of a signal analyzer will prevent the user from obtaining reliable measurements. The same is true for transient signals of insufficient duration for a complete measurement or sweep.

An example of such a signal is shown in the time domain in figure 1a. It is composed of two alternating frequency bursts, with noise and harmonic distortion. Several spectrum measurements (made at slightly different times) of this signal are shown as figures 1b-1d. These spectra are not useful for making the signal quality measurements described above, since the actual spectra are obscured by the burst artifacts and the presence of two different signals at different times during the spectrum measurement.

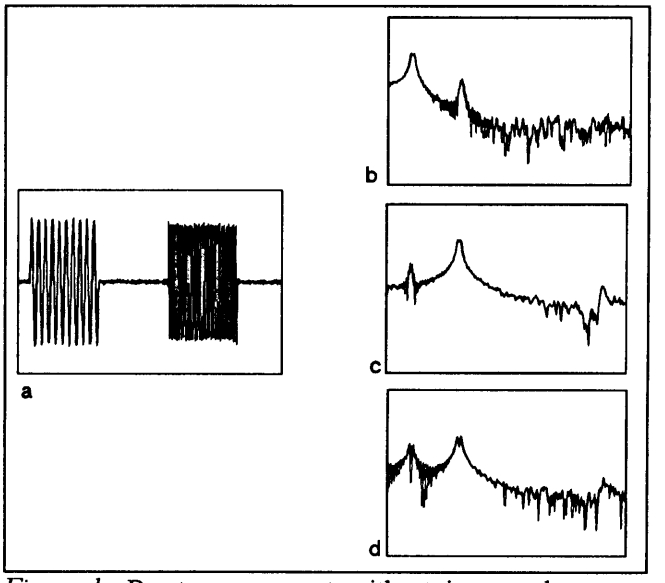

Figure 1: Burst measurements without time-gated spectrum analysis

When the signal is digitized with high resolution and accuracy, DSP techniques can be used to isolate the different components of the signal and perform spectrum analysis. This is shown in figures 2a-2c. In each figure the upper trace is the time domain signal and the lower trace is the spectrum measurement. The "gate" markers are shown on the upper trace as vertical bars, with the spectra (lower trace) corresponding to the part of the signal selected between the gate markers.

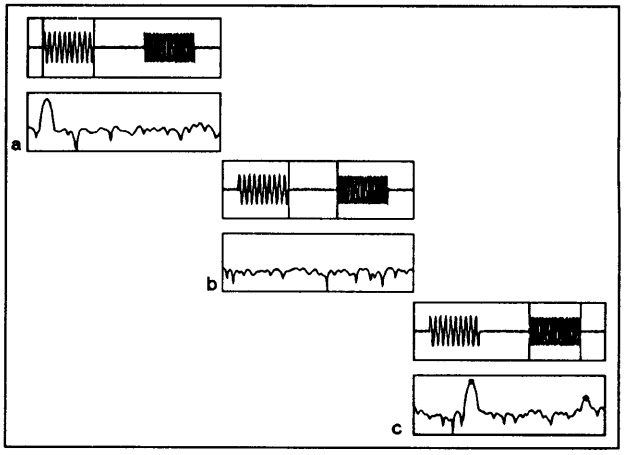

Figure 2: Burst measurements with time-gated spectrum analysis

Though they came from a challenging, time-variant signal, these spectra are as easy to interpret as similar

CW signals. Frequency, power, distortion and noise or signal/noise can be measured directly. The third, highest frequency, component of the signal can be tracked down as harmonic distortion on the higher frequency burst. The relative power of the signal bursts can be measured, along with on/off ratio and other parameters.

A measurement architecture with DSP operations performed on a digitized signal has other advantages for time-gated signal analysis:

- The signal to be tested need not repeat consistently, since the spectrum analysis can be performed from a stored single record.
- An external trigger signal is not required, since the signal to be measured can be selected from storage using gate markers.
- The IF filters used to perform spectrum analysis can be implemented digitally, providing better selectivity, shape factor and accuracy.
- The digital IF filters can be implemented with any arbitrary resolution bandwidth, allowing the user to select the best combination of gate width and frequency resolution, whether or not it fits the traditional 1-3-10 sequence.
- Additional dynamic range can be obtained when measuring repetitive signals by using time-domain averaging of the input signal. Noise and other components uncorrelated with the trigger will tend to average themselves out of the measurement, revealing lower level coherent spectral components.

This combination of benefits allows the designer to extract the maximum amount of information and insight from time-varying signals.

Transmitter Turn-On Analysis

Time-division multiple-access (TDMA) and other burst or frequency-agile communication schemes place special demands on many of the components of the transmission chain. For example, transmitters must turn on quickly and in a well-controlled fashion to avoid disturbing adjacent channels. In addition, their amplitude and frequency or phase must rapidly achieve stable (final) values so that these parameters may be used for modulation.

Time spent in turn-on is time lost for transmitting the data that is the fundamental purpose for the system, so designers must carefully optimize this behavior.

Traditional swept analyzers are good tools for measuring the frequency and power level of stable signals, but designers often must use other tools to characterize these rapidly changing characteristics of transmitters at turn on. Peak power meters and modulation domain analyzers are used to measure instantaneous power and frequency, respectively. However these tools give up some of the advantages that narrowband swept analyzers brought to such measurements. Specifically, broadband power meters do not have the wide dynamic range of spectrum analyzers and modulation domain analyzers do not have the frequency selectivity that allows one signal to be characterized among many others.

Here again the flexibility and power of advanced DSP can provide direct, intuitive measurements on dynamic signals combined with the benefits of traditional approaches used on simpler signals. Figure 3 is an example of a transmitter burst with amplitude and frequency variations at turn on. The lower trace is a spectrum analysis of the entire burst, indicating that there are probably multiple frequencies present in the burst. The amplitude variations can be roughly seen from the upper (time domain) trace.

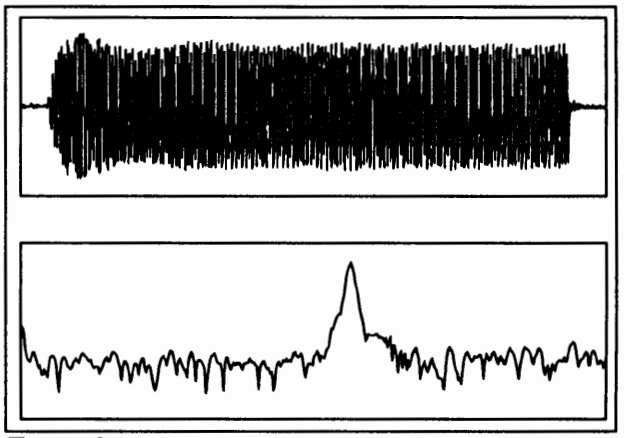

Figure 3: Transmitter turn-on and spectrum

If a trigger signal was available and if the signal consistently repeated itself, time gated spectrum analysis might be used to characterize the parameters of this signal. The advanced time gated spectrum analysis described in the example above could also be used, even if the signal was a transient or if no trigger was available.

But since any variation in amplitude, frequency or phase can be treated as modulation, we can use DSP to implement precision demodulation and display the desired characteristics of this burst directly. This is

shown in figure 4a as instantaneous amplitude and in figure 4b as instantaneous frequency. The measurement is made by selecting the desired center and span frequencies, along with the modulation type. If desired, an "auto-carrier" function can be implemented in the signal processing as well.

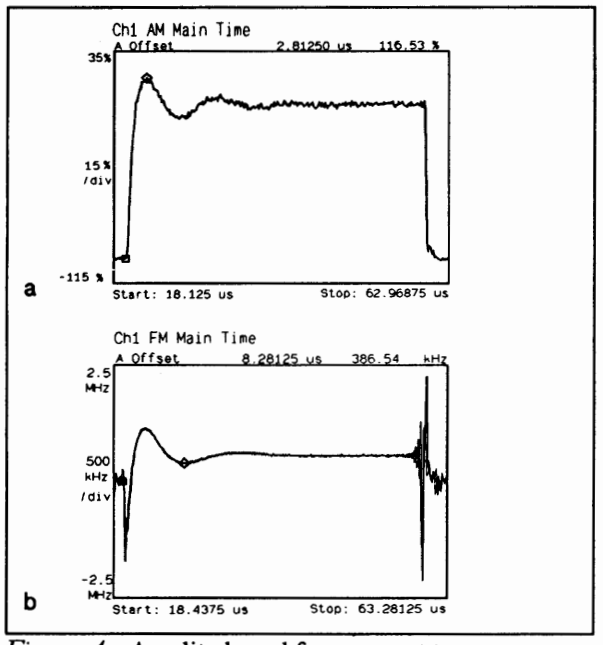

Figure 4: Amplitude and frequency at turn-on

For the designer this measurement technique offers several benefits:

- Direct display of the desired parameters--The amplitude demodulation result can be displayed as percent modulation, and the frequency variations displayed as deviation in Hz.
- No AM/FM/PM interaction--DSP technology allows the AM demodulator to be insensitive to PM, the PM demodulator to be insensitive to AM, and so on.
- Wide dynamic range and frequency selectivity--By using a narrowband analysis technique, the noise floor is kept low and no extraneous signals or adjacent channels interfere with the measurement.
- Real-time results for tuning--Modern DSP hardware allows this demodulation to be performed inside the instrument at a rate of tens of measurements/second rather than off-line in an external general purpose computer. Circuits can be adjusted and performance optimized in real time.
- Design with a single analyzer--Only one piece of measurement hardware is necessary to perform both general purpose signal analysis and precision demodulation.

Baseband-RF Coherence Measurement

Phase modulation techniques are increasing in number and variety, and are used more and more frequently in advanced communications systems. Whether a system uses phase modulation alone or in combination with other modulation, oscillator phase stability is a critical design parameter. Unfortunately it can also be a difficult parameter to measure, and the sources of phase noise or spurious sidebands can be very tough to track down. Both the sources and coupling mechanisms are many and varied.

Precision phase demodulation using DSP is an obvious tool to use to attack these measurement problems. It offers all the measurement benefits described in the example above. In addition, a signal processing function called coherence can be used with demodulation to great benefit in examining the relationship between baseband noise or discrete signals and troublesome phase noise or spurious sidebands at RF.

An example of this technique is shown schematically in figure 5.

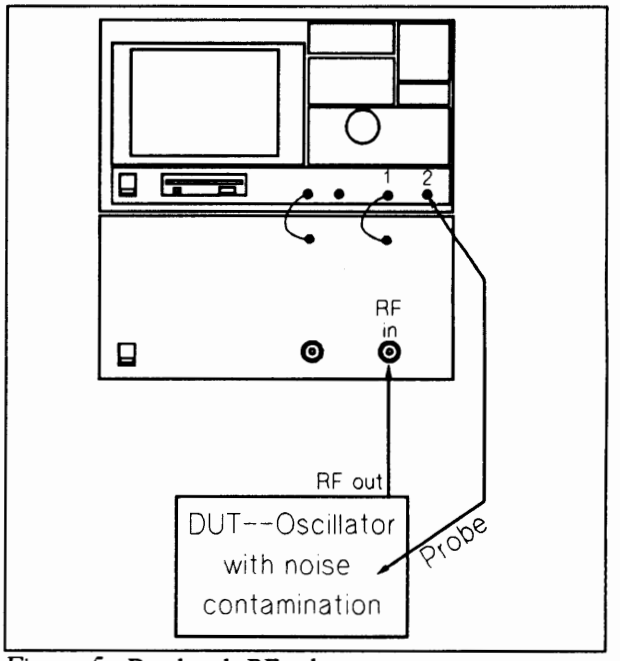

Figure 5: Baseband--RF coherence measurement

First, a direct RF spectrum measurement is made of the carrier with its close-in phase noise sidebands. This narrowband spectrum measurement is shown in figure 6, where the noise sidebands can be clearly seen.

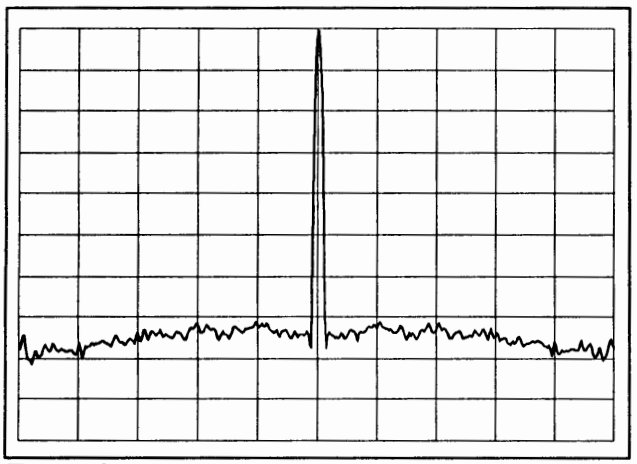

Figure 6: Narrowband spectrum with phase noise

Phase demodulation can be used on this RF carrier to recover and display the actual noise modulating signal in the time domain. This is the top trace in figures 7a and 7b.

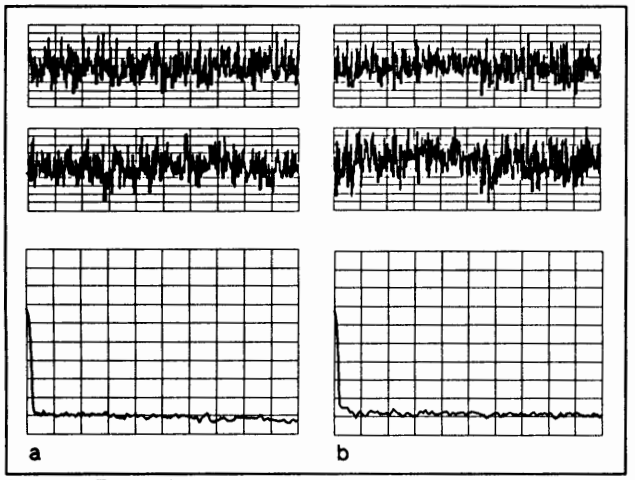

Figure 7: Phase demodulation in frequency and time

A second, baseband input channel of the vector signal analyzer can be used to probe various locations in the oscillator circuit to uncover noise sources which may be contaminating the RF carrier. This is shown schematically in figure 5. But in examining the resulting noise sources in both the time and frequency domains, the analysis problem is readily apparent: One source of noise often looks identical to another, whether examined in the time or frequency domains.

The bottom two traces in figures 7a and 7b represent time and frequency domain analysis of two different baseband noise sources. They are indistinguishable, and thus the source of the undesirable phase modulation (phase noise) remains unknown.

A powerful solution to this analysis problem is the DSP coherence function. Coherence is a measure of causality or the "relatedness" of two signals. It is a function of frequency, and is expressed as a value between zero and one. A value of zero indicates that two signals are unrelated, while a value of one indicates that two signals are exclusively related through a linear system.

We can use the coherence function in this example to compare the phase noise demodulated from the RF carrier with the noise sources which have been probed and measured directly at baseband. The results are shown in figures 8a and 8b.

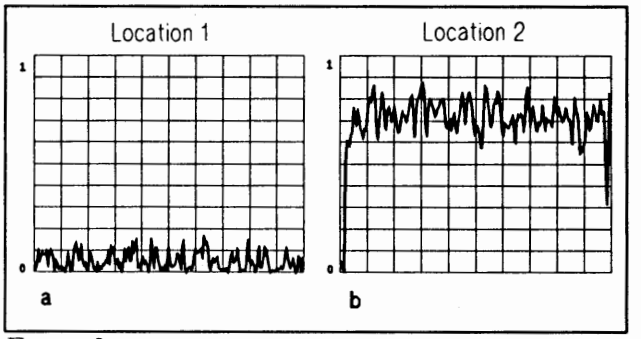

Figure 8: Baseband-RF coherence measured at two locations

The low coherence of figure 8a indicates that the baseband signal probed at that location is not responsible for the phase noise on the RF transmitter. The high coherence result in figure 8b shows that this signal is indeed the source of the phase noise, and that the baseband-to-RF coupling is broad and flat, with no obvious filtering characteristics.

This is a powerful and productive result for the RF designer. A principal source of phase noise can be discovered easily and attacked directly. In addition to the source of the phase noise, the strength and frequency response of the baseband-to-RF coupling function is revealed. This knowledge can help the designer better understand the phenomena and perhaps provide alternative solutions. If the noise source cannot be eliminated, the problem may still be fixed by defeating the newly-understood coupling mechanism through the use of filtering, active

cancellation, shielding, etc.

Digital Modulation Analysis

If sufficient processing power and signal memory is available, DSP algorithms can be written to extract information from, and perform tests on digitally modulated carriers. Engineers dealing with digital modulation can then have access to test techniques designed specifically for their systems.

The process begins with AM/FM/PM demodulation such as that described above. An example is shown in figure 9. This is a plot of a digitally modulated signal using the pi/4 DQPSK scheme, which is here phase demodulated and plotted in continuous phase vs. time.

Figure 9: Phase-demodulated pi/4 DQPSK

To perform digital demodulation the DSP engine must perform extra processes in parallel. After the time data is processed by a digital filter, algorithms must perform carrier and symbol lock functions. The timing and phase reference information is then provided to a DSP process performing demodulation to generate I and Q outputs. This parallel processing is shown schematically in figure 10.

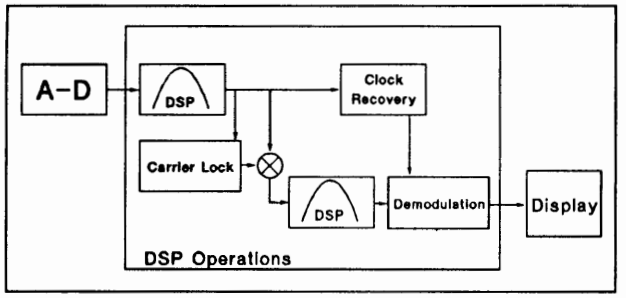

Figure 10: Digital modulation analysis with clock recovery, carrier lock

Results of these operations are displayed in two different formats in figures 11a and 11b, for a QPSK signal. Constellation diagrams allow the designer to isolate the signal at the instants when the data is valid, while vector diagrams permit examination of the signal trajectory between valid states.

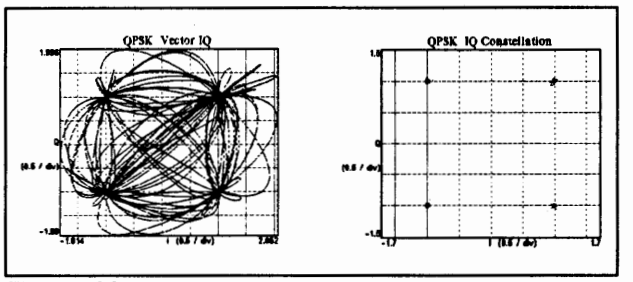

Figure 11: Vector and constellation diagrams

In addition to the graphs, measurement data can be presented in quantitative form such as Error Vector Magnitude.

Other DSP Measurement Benefits

DSP-based techniques such as this can provide a number of other measurements and measurement benefits. Several, beyond the scope of this paper include:

- True RMS detector and selectable band power measurements--Digital signal processing can be used to implement a bank of parallel filters with true RMS detection. This permits direct and accurate measurements of average power over arbitrary bandwidths.
- Direct phase noise measurements--Combining a precision phase demodulator with spectrum analysis using true RMS detection allows some phase noise measurements to be made in real time without external hardware or correction factors.
- PLL closed-loop frequency response--Comparing baseband stimulation of a PLL control loop with the phase-demodulated PLL output yields the amplitude and phase frequency response of the PLL in real time. This is a powerful design tool for tuning PLL response.
- Determining center frequency of modulated signals--This often-difficult task can be performed using techniques such as phase demodulation or computed frequency centroids.
- Correlation functions--DSP auto- and cross-correlation functions are a useful method for comparing different signals (or time-delayed versions of the same signal) to determine their similarity.

Applying the Modulation Domain to Wireless Communication Testing

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Introduction

Wireless RF communications is a dynamic worldwide market. Technologies are rapidly changing as cellular and cordless systems move from analog to digital transmission. New digital systems promise improved voice and data quality as well as more efficient use of the frequency spectrum. Time Division Multiple Access (TDMA) formats will solve capacity limitations that users and operators of cellular systems are currently experiencing in many of the large metropolitan areas.

These fast emerging digital modulation and accessing methods present tough new challenges for test equipment. New test equipment is required to bring designs to market quicker, and to perform manufacturing testing in a fast and efficient manner. This paper discusses recently introduced Modulation Domain Analysis techniques which have greatly simplified the analysis of dynamic frequency signals used in modern wireless communications systems.

Applying the Modulation Domain to Wireless Communication Testing.

The days of simple continuous wave transmission techniques are passing. Wireless communication system designers are utilizing various spread spectrum and time division accessing techniques to develop more reliable and efficient systems. These techniques make analysis of carrier frequency and modulation much more difficult. For example, in the case of a frequency hopping spread spectrum system, the carrier is switching frequencies hundreds or thousands of times each second. Designers need a method to characterize the frequency switching behavior of such a system.

The Modulation Domain provides a new way of looking at your signals. Figure 1 shows a three dimensional view of a dynamic signal. You are probably familiar with the time and frequency domains. The time domain is a view of voltage versus time (oscilloscope). The frequency domain shows amplitude versus frequency (spectrum analyzer). The modulation domain is the missing

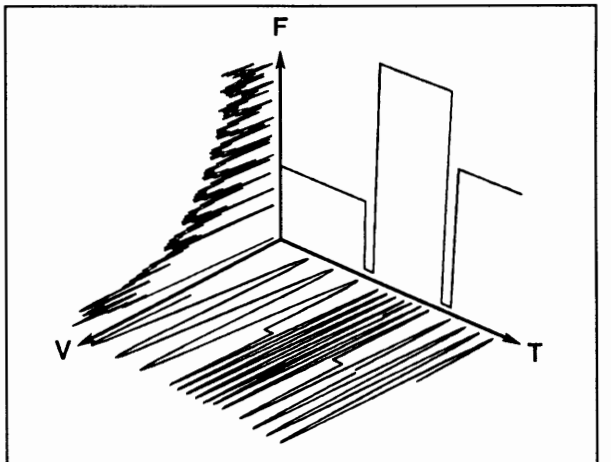


Figure 1. A three dimensional view showing a signal's time, frequency, and modulation domains.

third dimension - frequency versus time. The modulation domain reveals things that you have not been able to see before. Signal parameters that are not readily available in the time or frequency domains are now apparent. The Hewlett Packard HP 53310A and HP 5372A are the first instruments that let you see your signals in the modulation domain. All measurement results shown in this paper were taken with the HP 53310A Modulation Domain Analyzer.

The modulation domain analyzer can be thought of as a "frequency oscilloscope" when viewing a signal's frequency versus time. It also provides histograms showing the probability distribution of millions of continuous frequency measurements.

Lets examine how a modulation domain analyzer makes frequency versus time measurements. The measurement technology breakthrough is called continuous counting. A patented technique of reading high speed event and time counters on the fly without disturbing the counting process makes single-shot continuous frequency measurements possible. Figure 2 shows how continuous frequency samples are taken. Continuous event and time counters monitor zero threshold crossings of the input signal. The point-to-point frequency is equal to delta events divided by delta time. The time of each sample is known, so the input signal's frequency can be plotted as a function of time.

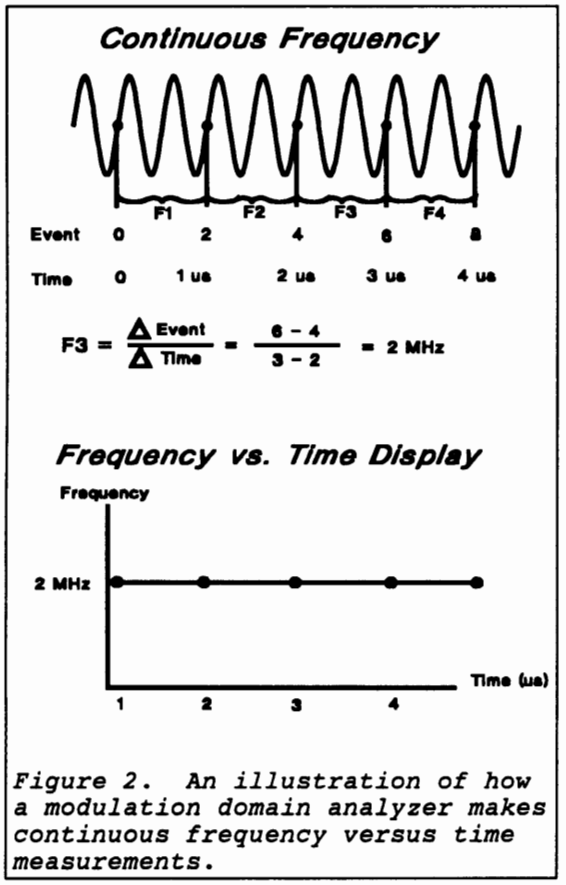


Figure 2. An illustration of how a modulation domain analyzer makes continuous frequency versus time measurements.

The modulation domain analyzer's frequency versus time and histogram displays are very useful in analyzing synthesizer settling time, turn-on/off frequency behavior, frequency hopping, and FSK center frequency and peak deviation. Now we will examine many of these measurements in detail.

Measuring Synthesizer Settling Time.

The synthesizer is a key part of the RF design effort for today's digital RF communication systems. The synthesizer is constantly switching frequencies in many systems for a variety of reasons including cell hand-offs, frequency division duplexing, or frequency hopping. Measuring synthesizer settling time is critical to design verification. Indirect measurement methods such as delay line discriminators, zero beat mixing, or spectrum analyzers in zero span have been used in the past. These indirect techniques are difficult to use and prone to a variety of errors. A fast and accurate method is needed to characterize synthesizer settling time.

Figure 3 is a time domain view of a frequency step. The step command edge is also shown. Settling time measurements must be time referenced to the step command edge. The modulation domain analyzer can measure the frequency continuously during the step to provide a direct view of synthesizer settling (figure 4). The measurement is triggered by, and time referenced to, the step command edge. The display is

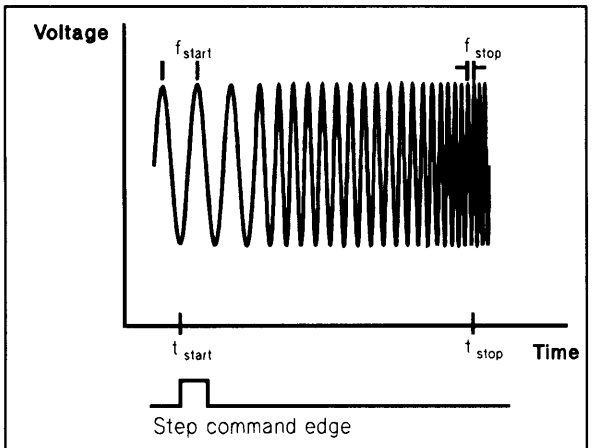


Figure 3. Time domain view of a frequency step.

zoomed-in on the final part of the settling transient for optimum resolution. The settling time is measured automatically by analyzing the trace. The user enters the target frequency and tolerance band using the horizontal frequency markers. The analyzer then automatically searches backwards in time from the right edge of the display to find the point where the trace last entered the "pass band". This time is indicated with the vertical time marker, and the settling time result is shown at the bottom of the display.

Another consideration for synthesizer performance is amplitude pulling. Amplitude pulling can occur as a result of power

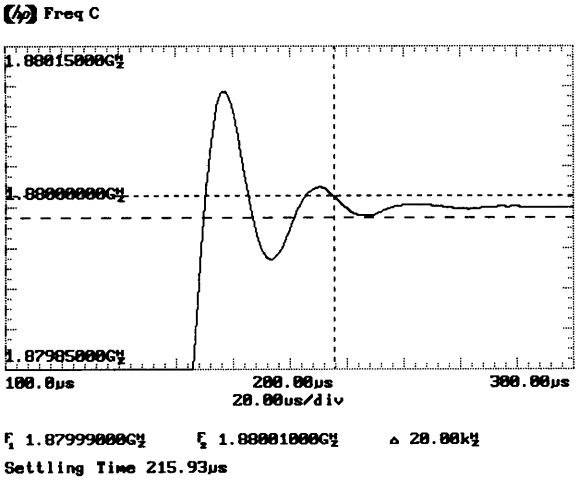


Figure 4. Synthesizer settling time measurement.

variations as the TDMA burst is turned on. The power ramp can cause a temporary shift in the synthesizer's frequency. The modulation domain analyzer makes it easy to analyze pulling effects (figure 5). You can quickly see how far off frequency it is pulled and how long it takes to relock.

Direct frequency versus time displays make it easy to measure synthesizer settling time and pulling. The automatic measurement of settling time speeds your analysis. Accuracy of better than 100 Hz is typically achieved at RF frequencies.

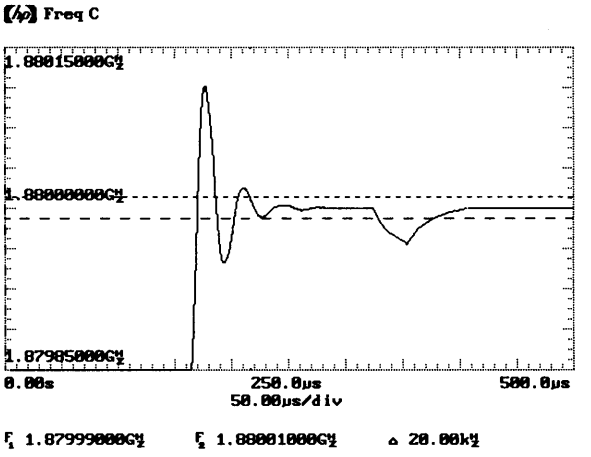


Figure 5. Synthesizer frequency pulling measurement.

Transmitter Turn-on and Turn-off Frequency Behavior

Manufacturers of RF communications systems must characterize transmitter turn-on and turn-off behavior to comply with various new international test standards (e.g. ETS 300 113 & 162). The intent of the new test standards is to assure that the device is not transmitting "out of channel" during power on/off. Many people are searching for an easy and reliable test method to comply with the new standards. The Modulation Domain Analyzer makes it easy to measure transmitter turn-on and turn-off transients.

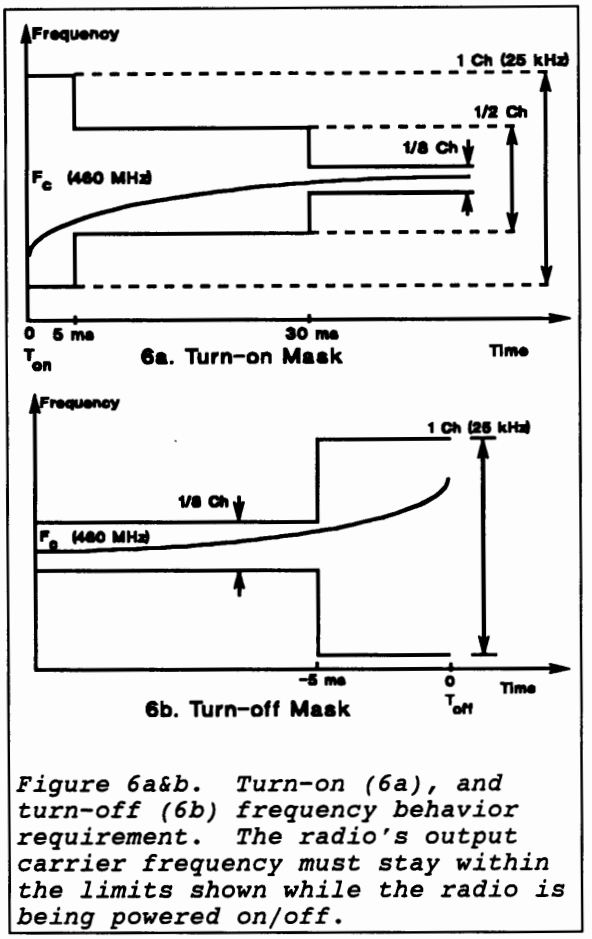


Figure 6a&b. Turn-on (6a), and turn-off (6b) frequency behavior requirement. The radio's output carrier frequency must stay within the limits shown while the radio is being powered on/off.

Figure 6a&b provide a quick graphical view of a typical set of transmitter turn-on and turn-off frequency behavior requirements. These requirements apply to a 460 MHz emergency services radio.

The modulation domain analyzer provides a direct frequency versus time view of the transmitter's frequency behavior during turn-on and turn-off. Accurate triggering is the key to turn-on/off frequency transient measurements. The preferred method is to trigger on the -30 dBc point. This is the point on the power ramp where the transmitter's output power is 30 dB below its average carrier power level. It is referred to as the T(on) or T(off) point. This is the preferred method because it assures that the frequency is being measured when it is important - when the transmitter is transmitting above -30 dBc. The modulation domain

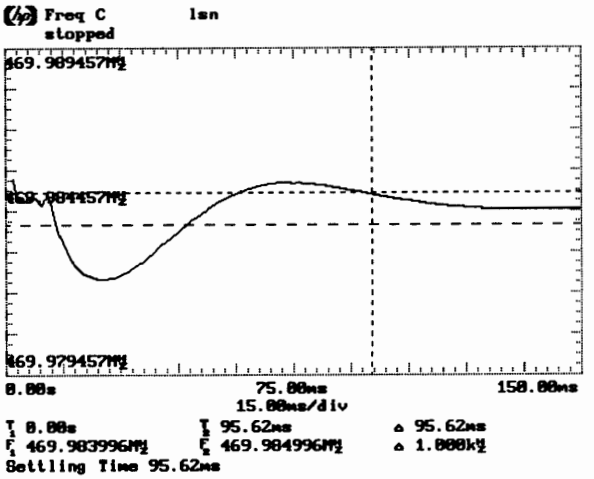


Figure 7a

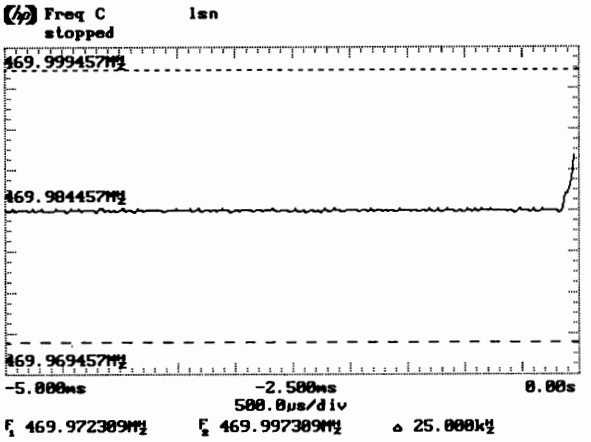


Figure 7b

Figure 7a&b. Turn-on (7a) and turn-off (7b) frequency behavior of a 460 MHz emergency services radio.

analyzer can be calibrated to trigger a measurement at the -30 dBc point. An alternate method is to trigger the measurement with an external sync pulse. This sync pulse should have a fixed timing relationship to the -30 dBc point.

Figure 7a shows a single shot measurement of a radio's frequency behavior during turn-on. The time zero trigger for this was the -30 dBc point on the power ramp up. The radio must settle to within the limits shown in figure 6a. The horizontal markers can be easily

positioned to define the target frequency and tolerance bands. This radio passes the 30 ms requirement. The 1 channel (25 kHz) and 1/2 channel (12.5 kHz) settling times are easily measured by changing the timebase setting.

Figure 7b shows a measurement of the radio's frequency behavior during turn-off. This measurement is made by looking at the pretrigger information. The trigger is the -30 dBc point on the power ramp down as the radio is keyed off. The markers show a peak frequency deviation of less than 7 kHz during the turn-off. This is well within the 1 channel (25 kHz) allowance for this radio.

Frequency Hopping Measurements

Many wireless communication systems employ frequency hopping. The GSM Pan-European Digital Cellular system can use a frequency hopping mode to overcome multipath fading problems. When frequency hopping is used, the carrier frequency is switched for each TDMA burst of the mobile (figure 8). The modulation domain analyzer can provide a direct view of the frequency hopping pattern in a single pass measurement (figure 9). Frequency and time markers can be used to verify the hopping sequence.

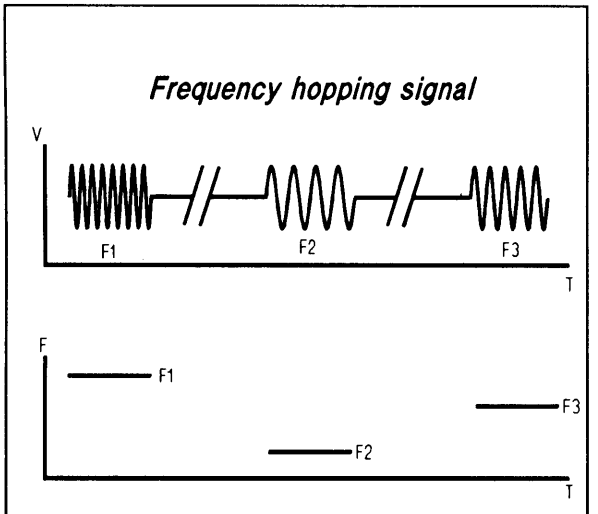


Figure 8. An illustration of a frequency hopping signal.

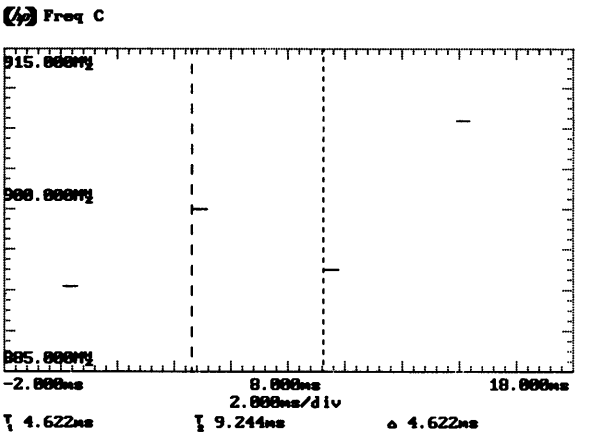


Figure 9. Frequency hopping measurement on a GSM transmitter.

FSK Center Frequency and Peak Deviation

Lets now look at modulation measurements on the RF carrier. Advanced cordless telephone systems such as CT2, CT3 and DECT require that carrier center frequency and peak deviation be measured in order to meet the regulatory standards. The TDMA bursting of the carrier makes this a very difficult measurement. Figure 10 provides a view of a typical TDMA carrier. The mobile only transmits in a given time slot. Center frequency and peak deviation of the filtered FSK modulation must be accurately measured in the presence of the on-

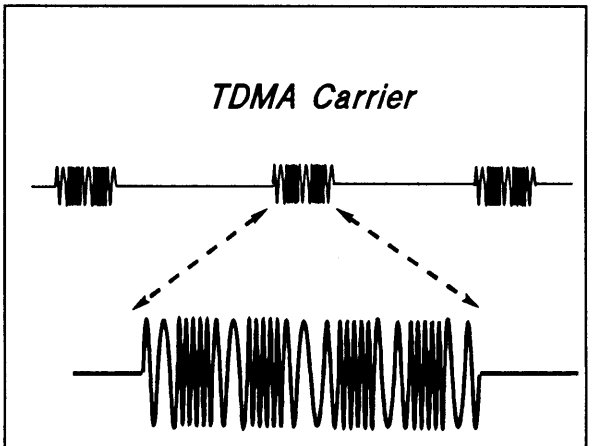


Figure 10. Illustration of a typical TDMA carrier.

off TDMA bursting. The modulation domain analyzer gives a direct view of the modulation on a TDMA carrier.

Figure 11 is an example of a frequency versus time display of the 0.5 GMSK modulation used on the new Digital European Cordless Telephone (DECT) system. You can quickly verify the bit pattern, bit rate, frequency deviation, and filtering profile on the RF signal.

The measurement data can also be displayed as a histogram (figure 12). The histogram display shows the probability distribution of thousands of fast frequency measurements on a DECT carrier. The filtered BFSK modulation peaks are revealed directly in the histogram. The center frequency is the midpoint of the deviation peaks. The modulation domain analyzer automatically calculates the center frequency and peak deviation from the histogram display. Measurement results are presented at the bottom of the display.

The modulation domain is well suited to measuring center frequency and deviation on TDMA carriers. The automatic measurements simplify bench use and make it easy to automate in a manufacturing test system. Automatic center frequency and peak deviation measurements make it easy to verify conformance to regulatory standards.

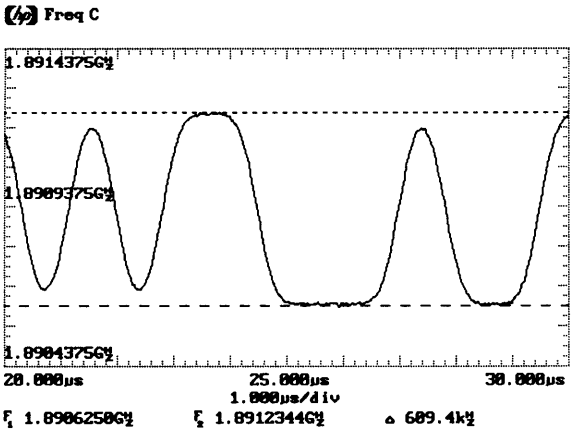


Figure 11. Frequency versus time measurement of 0.5 GFSK modulated DECT carrier.

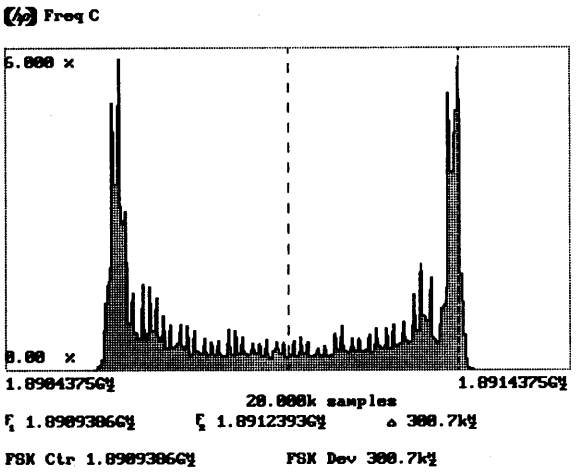


Figure 12. Center frequency and deviation are automatically calculated from the frequency histogram.

Jitter Measurements and RF Eye Diagrams

Let's now examine jitter measurements on the RF carrier. It is very common to measure jitter on a baseband signal using a digital oscilloscope. To do so, you trigger on a reference edge and repetitively trace the bit transition edge of interest. Infinite display persistence allows you to build up a history of bit transition positions. The width of the infinite persistence trace at the midpoint is the peak-to-peak jitter.

A key limitation of the digital oscilloscope method is that you must have a baseband signal available. Many people either do not have a convenient baseband signal available or would prefer to measure jitter directly on the RF carrier. A modulation domain analyzer can use the same method described above for a digital oscilloscope to provide an infinite persistence frequency versus time trace of a bit transition directly on the RF carrier.

Figure 13 shows an infinite persistence frequency versus times display of the first bit transition in a TDMA burst. The peak-to-peak jitter can now be measured directly on the modulated RF carrier.

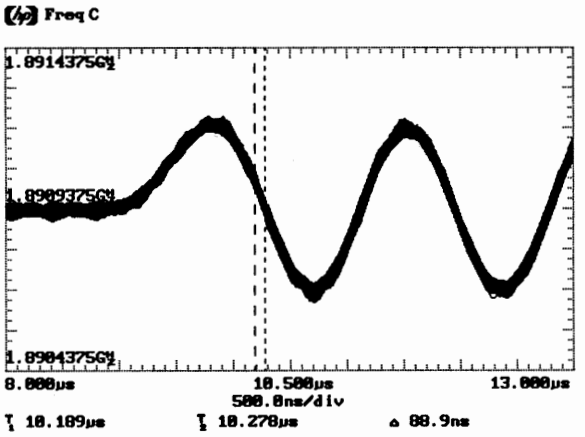


Figure 13. Peak-to-peak jitter measurement on the RF carrier.

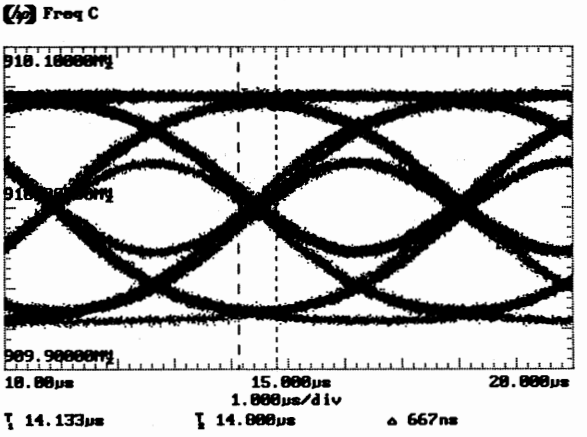


Figure 14. Frequency versus time eye diagram of a GSM carrier.

The modulation domain analyzer can also provide frequency versus time eye diagrams when measuring a carrier with live data. Figure 14 is an example of the unique eye pattern of a 0.3 GMSK modulated GSM signal. Frequency versus time eye diagrams provide a quick qualitative view of transmitter performance.

Eye patterns allow you to view the effects of bit jitter and inter-symbol interference directly on an RF carrier. The frequency versus time eye diagram can be compared to a conventional baseband eye diagram of an oscilloscope. Comparing the RF eye diagram with the baseband eye diagram allows you to quickly isolate problems with the RF chain.

Summary

We have seen that the modulation domain analyzer can provide many new measurements for wireless communications systems. It is a powerful new tool for design characterization and manufacturing test. Its ability to provide direct frequency versus time views provide insights not previously available. The automatic measurements of FSK center frequency and peak deviation on TDMA carries provide an easy way for engineers to automate their test systems.

MEASURING THE PEAK-TO-AVERAGE POWER OF DIGITALLY VECTOR MODULATED SIGNALS

Charles J. Meyer, Senior Applications Engineer, Boonton Electronics

Digital vector modulation has become the preferred method of modulation for wireless digital communication today. The need to have the capacity and robustness of a high speed digital communication channel with the versatility of a wireless transmission has resulted in considerable advancement of this area in recent years. However, system designers continue to be challenged by the high peak-to-average power ratios and large linear dynamic ranges that this type of modulation requires. The Boonton 4400 is an advanced Peak Power Meter that can be used to accurately measure these requirements.

Digital Vector Modulation

Digital vector modulation is being utilized in a wide variety of technologies such as digital cellular radio, high definition television (HDTV), satellite and microwave links, military communication, and numerous spread spectrum applications.

Digital vector modulation is a modulation scheme whereby a signal's phase and/or amplitude are altered to represent digital bit patterns called symbols. Specific phase/amplitude combinations are called symbol states and valid symbol states are defined on a vector map called an I-Q (in-phase - quadrature) diagram (Fig. 1).

Schemes which modulate only a signal's phase are often referred to as Phase-Shift Keying (PSK) modulations, whereas when amplitude and phase are both used to encode data it is usually referred to as Quadrature Amplitude Modulation (QAM).

Variations of these basic schemes continue to emerge. A variation of PSK called pi/4 differential quadrature phase-shift keying (pi/4-DQPSK), is used by the North American Digital Cellular (NADC) and Japanese Digital Cellular (JDC) formats, while another PSK variant called minimum shift keying (MSK) is used by the GSM European digital cellular format.

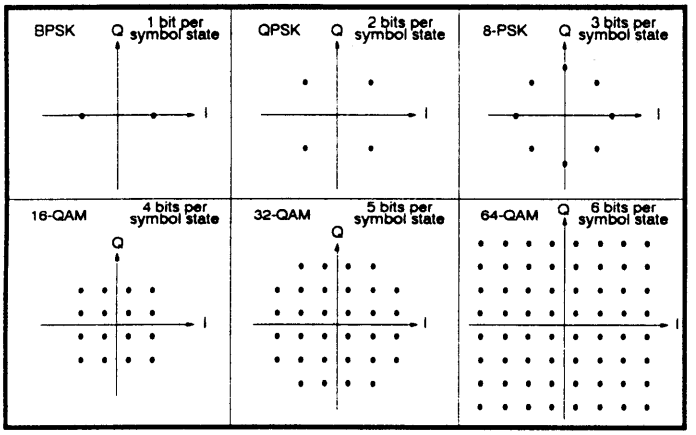


Figure 1 - Typical I-Q Diagrams

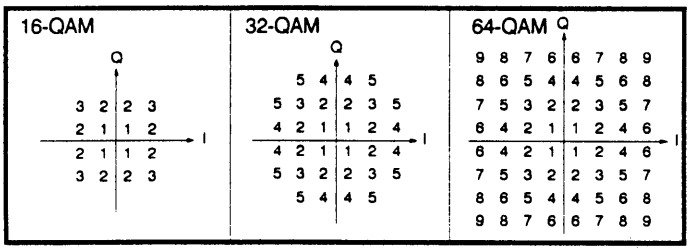


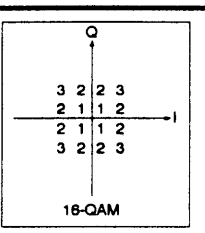
Figure 2 - Symbol Power Levels

Power Analysis of Digital Vector Modulation

The high peak (envelope) power of a digitally vector modulated signal is the result of three primary factors: the existence of multiple symbol power levels (caused by the multiple amplitude levels that exist in a QAM type scheme), compound ringing (caused by filtering of the baseband I&Q signals), and multiple carrier power addition (caused by the vectorial summation of the voltages of multiple carriers).

Digitally vector modulated schemes that modulate a signals amplitude (such as QAM), have multiple symbol power levels. Vectorial analysis of an I-Q diagram will reveal these levels (Fig. 2). Since each symbol power level represents multiple symbol states (and all of the data associated with those states), any system non-linearities that could alter one of the symbol power levels (such as AM/AM or AM/PM distortions) would also affect the system bit error rate (BER). An impairment of this type could easily generate BER's high enough to disable an entire system. PSK modulations have only one symbol power level, but they are still vulnerable to amplifier nonlinearity distortions (especially AM/PM).

Assuming that all of the symbol states are occupied equally over time, then it is possible to calculate the relative peak-to-average symbol power and dynamic range requirements of a complex signal (Tables 1 and 2)[1]. Discrete symbol power levels can be easily seen and measured on a QAM signal that employs little or no baseband filtering (Fig. 3).



Symbol Power Level Number	Power Vector Magnitude (a)	Number of occurrences (b)	Weighted Symbol Power (a)*(b)
1	1	4	4
2	5	8	40
3	9	4	36
		Total weighted symbol power :	80
		divided by total number of symbol states :	16
		Average symbol power magnitude :	5
		Peak symbol power magnitude :	9

Peak/Average Power Ratio = 9/5 = 1.80 = 2.55 dB

Dynamic Range = 9/1 = 9.54 dB

Table 1 - Calculation of Symbol Power for 16-QAM

Type of Vector Modulation	Number of Symbol Power Levels	Peak-to-Avg Symbol Power ratio	Peak-to-Avg Symbol Power dB	Dynamic Range ratio	Dynamic Range dB	Percent of Data in highest power level	Percent of Data above average power level
16-QAM	3	1.8:1	2.55	9:1	9.54	25.0 %	25 %
32-QAM	5	1.7:1	2.30	17:1	12.31	25.0 %	50 %
64-QAM	9	2.3:1	3.68	49:1	16.90	6.3 %	50 %
256-QAM	32	2.7:1	4.23	225:1	23.52	4.8 %*	45 %
256-SSQAM	30	1.9:1	2.85	157:1	21.96	25.0 %*	52 %

* Highest 1dB of power

Table 2 - Symbol Power requirements of various schemes

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Also published in abridged form in Microwaves & RF Magazine, January 1993

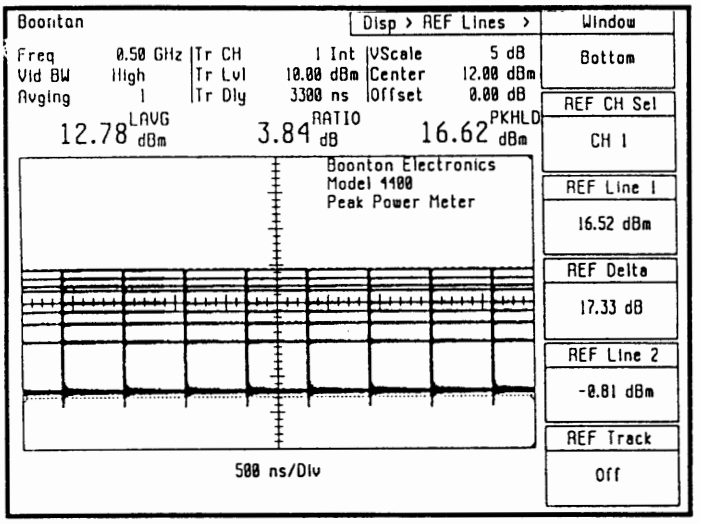


Figure 3 - Nine symbol power levels of a 64-QAM (unfiltered)

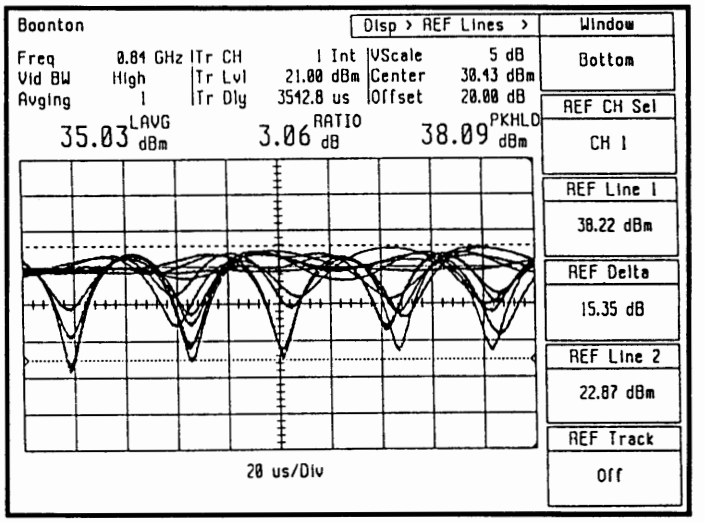


Figure 4 - Compound ringing caused by baseband filtering

Baseband filtering will introduce an additional peak power contribution in the form of compound ringing (Fig. 4). Digitally vector modulated signals require baseband filtering because they have a theoretically infinite bandwidth (as defined by the function (sin x)/x). To limit the occupied signal bandwidth, the I&Q modulator signals must be filtered so that the digitally driven modulator does not have to instantly transition to the next symbol state. A digitally produced symbol change causes an impulse response that has an infinite Fourier series. This series becomes truncated when it is convoluted with a bandwidth limiting filter. Whenever a Fourier series is truncated, ringing results (known as Gibbs phenomena)[2].

The amplitude of the ringing will vary from symbol to symbol because certain phase/amplitude changes will be more drastic than others. This is compounded by residual ring voltages that are still decaying from previous symbol changes. Although well designed baseband filters will keep this effect to a minimum, peak power transitions will occur in proportion to the square of the compounded ring voltage.

The effect of symbols transitioning across multiple power levels combined with the compound ringing from the baseband filters will produce a power spectrum that resembles white noise (Fig. 5). The highest (peak) power levels of this signal must be preserved within the linear region of an amplifier. Failure to do this has serious consequences since compression of the peak power could result in significant data loss as well as the generation of unacceptable intermodulation distortion products (IMD). Thus, QAM amplifiers are usually operated with average power levels of about 7 to 15 dB below their 1 dB compression points. PSK amplifiers usually require 3 to 7 dB of output "backoff" as well.

Accurate measurement of the peak power is necessary since only 3 dB of error equates to 50% linear error. This could be the difference between choosing either a 500 watt or a 1000 watt amplifier for the same system.

Multiple Carrier Transmissions

Transmitters that support multiple simultaneous carriers are further challenged due to the peak power effect that results from the vectorial addition of the voltage waveforms of each individual carrier. Each time that the number of carriers (with equal power) in a system are doubled, the average power level will increase by 3 dB, and the peak power level will increase by 6 dB (Table 3). In PSK and QAM schemes, the peak power will always be higher due to the peak power components of the individual carriers (symbol power and baseband filter ringing contributions).

In an example situation of 32 carriers, each being QPSK modulated and having an individual average power of 10 Watts with a peak-to-average power ratio of 3 dB, the combined average power would be 320 Watts (55 dBm), but the combined instantaneous peak power would reach to over 20,000 Watts (73 dBm) (Table 4). Assuming that the amplifier was rated for linear operation to 5 kW, all peak power occurrences greater than 5 kW would drive the amplifier toward saturation.

If we constructed a histogram of the power levels, totaling all random occurrences of peak power by level, we would see a statistical distribution with a diminishing number of occurrences as we approached the highest levels. If these were FM carriers, the number of peak power occurrences at and above the power amplifier's compression level would represent the amount of crosstalk and IMD being tolerated. But with a digital vector modulation scheme such as QPSK, this may also be representing instantaneous occurrences of symbol destruction on every carrier at the same time.

Assuming that the peak power occurrences are of a very small duration compared to the symbol rate and that the amplifier can quickly recover from these occurrences, the symbol information may be recoverable and the transient IMD

Number of Carriers (1W each)	Combined Average Power dBm	Combined Average Power Watts	Maximum Peak Power dBm	Maximum Peak Power Watts	Peak-to-Average Power dB	Peak-to-Average Power ratio
1	30	1	30	1	0	1:1
2	33	2	36	4	3	2:1
4	36	4	42	16	6	4:1
8	39	8	48	64	9	8:1
16	42	16	54	256	12	16:1
32	45	32	60	1024	15	32:1
64	48	64	66	4096	18	64:1
128	51	128	72	16.4 k	21	128:1

Table 3 - Peak-to-Average Power of Multiple FM Carriers

Number of Carriers (10W each)	Combined Average Power dBm	Combined Average Power Watts	Maximum Peak Power dBm	Maximum Peak Power Watts	Peak-to-Average Power dB	Peak-to-Average Power ratio
1	40	10	43	20	3	2:1
2	43	20	49	80	6	4:1
4	46	40	55	320	9	8:1
8	49	80	61	1280	12	16:1
16	52	160	67	5120	15	32:1
32	55	320	73	21 k	18	64:1
64	58	640	79	82 k	21	128:1
128	61	1280	85	328 k	24	256:1

Table 4 - Peak-to-Average Power of Multiple QPSK Carriers

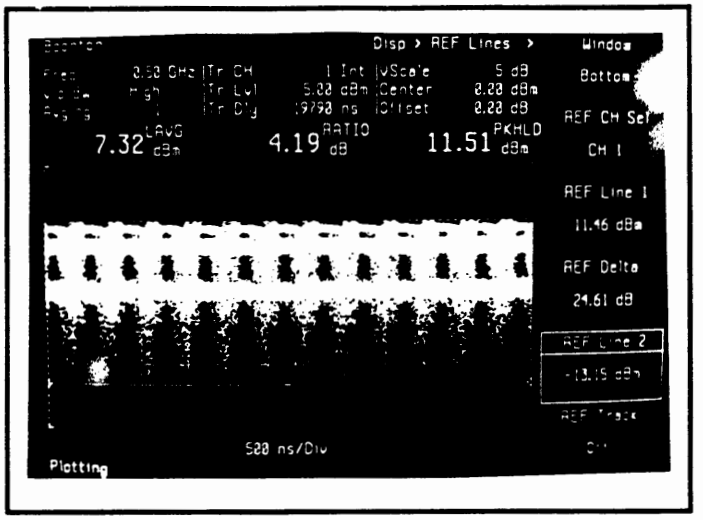


Figure 5 - The "white-noise" power spectrum of a QAM signal

may be able to be tolerated. Yet, if the peak power was known on a continuous basis (by monitoring), the amplifier loading could be regulated to allow for maximum linear output performance while protecting against saturation.

Power Domain

Successful implementation of a digitally vector modulated system requires an analysis of the peak and RMS average power response of a system. What is needed is a power domain analysis, or an ability to analyze instantaneous peak power occurrences as a function of time. Power domain analysis requires measuring scalar power as it occurs in the time domain.

This can be viewed in contrast to traditional scalar analyzers that measure scalar power in the frequency domain. This type of analysis was first defined by commercial and military requirements to analyze pulsed power transmitters. They needed to accurately measure specific pulsed power envelope parameters in the time domain. The peak power meter was developed to meet those needs.

Traditional instruments used for power measurement are not suitable for power-domain analysis. Spectrum analyzers, for example, have bandwidth and mixer limitations and lack the accurate power level measurement capability of a power meter. Conventional averaging power meters are also not suitable for this type of analysis since they are designed to average all instantaneous peak power occurrences. They can, however, provide true RMS average power information.

Thermocouple sensors thermally derive the measurement of true average power, while averaging diode sensors use long resistive-capacitive (R-C) time constants to provide an average voltage response proportional to the average RF power input level. Averaging diode sensors also cannot be used to measure the true RMS power of complex waveforms unless the peaks of the complex waveform exist completely within the square-law limits of the diodes[3].

Peak Power Meters

Power domain analysis of a digitally vector modulated signal requires a peak power meter with advanced features. The peak power sensor must be a fast, average-responding diode type, providing instantaneous voltage output proportional to instantaneous RF power input. This is to accurately follow the details of the power envelope of a signal and to capture all instantaneous power occurrences to the frequency limit of its video bandwidth.

Dynamic Range	Digitizing Bits	Percent Bit Resolution	Power Measurement Resolution
45 dB	8	0.391 %	0.176 dB
45 dB	10	0.098 %	0.044 dB
45 dB	12	0.024 %	0.011 dB
45 dB	14	0.006 %	0.003 dB
45 dB	16	0.002 %	0.001 dB

Table 5 - Power Measurement Resolution

The sensor's video bandwidth specification should be sufficient to capture all power transitions related to a symbol change. Any power transitions occurring above the limit of a sensor's video bandwidth will be averaged by the diode's video load. These sensors typically use diodes in a full-wave rectification method to insure accurate detection of both positive and negative voltage transitions.

The sensor diode's video output must be supported by a wide dynamic range amplifier such as a logarithmic amplifier. This is necessary to accurately track a signal through large peak-to-average power levels and to preserve the details of large power transitions. The amplifier's output must then be digitized at high speed with high resolution. High speed sample and hold circuits and flash type A/D converters are often used to perform this type of digitization.

The number of bits used to digitize the signal will determine the power measurement resolution. When the percent bit resolution is applied across the full dynamic range of the logarithmic amplifier, the quantization level resolution is established (Table 5). This resolution must be fine enough to discern the smallest power level of interest.

Video averaging is often used to interpolate the area between the quantization levels. This has an effect as if the number of bits of resolution could be increased and it is usually referred to as "averaging the signal". By averaging a PSK/QAM signal in this way, peak power information is lost. This is because the power envelope is not repetitious with time, but changing continuously from symbol to symbol. So signal averaging cannot be used.

The acquisition system must use very high speed sampling, or else use a technique such as random repetitive sampling to provide true statistically random sampling. The system should also acquire power data with or without a repetitive trigger event. This is important in situations where a symbol trigger is not available or with multiple carrier transmissions.

Finally, consideration also must be given to the processing system since acquisition speed (samples per second) does not take into account how effectively the processing system can utilize these samples. When significant mathematical processing is required, a weak processing system may be forced to ignore a significant percentage of the available samples because it will not have the time to process them.

Boonton 4400 Peak Power Meter

The Boonton 4400 is an advanced peak power meter designed to support extensive power domain analysis. It combines powerful signal acquisition and digital signal processing with a versatile set of user interface features. It can accurately analyze instantaneous peak power occurrences on either continuous or pulsed signals, whether repetitive or not, from 30 MHz to 40 GHz (depending on sensor) with NIST traceable accuracy.

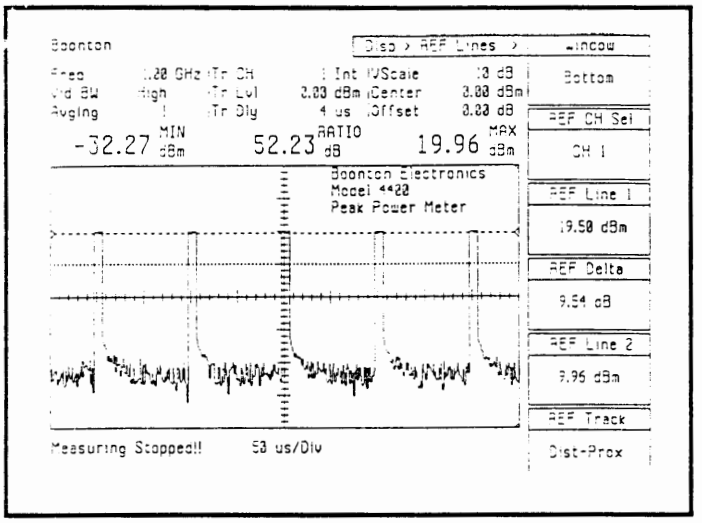


Figure 6 - The 4400 tracks power over a large dynamic range

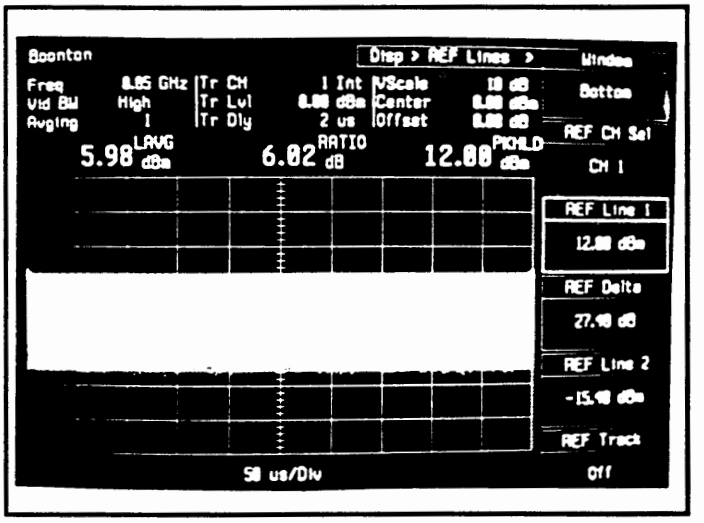


Figure 8 - Multiple carriers requiring 28dB of dynamic range

It's 56318 peak power sensor can accurately track all instantaneous power events up to 35 MHz (video bandwidth limit). Power occurrences (or white noise effects) that are faster than this, are averaged down to the video bandwidth limit. Pulse rise/fall time measurements are possible to less than 15ns. Diode response is tracked with a logarithmic amplifier having a dynamic range of over 47 dB (Fig. 6). The logamp's output is random-repetitively sampled by a 12-bit flash acquisition system digitizing at 1 Msamples/sec (1 MSample/s for timebase settings of 50us or faster, else .5 MSample/s).

A dedicated 32 bit floating point digital signal processor (DSP) continually process this data and execute all mathematically related analyses with negligible sample decimation. The DSP system can perform true integral RMS averaging on any portion of a waveform by simply positioning the area of concern between two time markers. These markers can be positioned to integrate an area within a pulse or across the whole screen (the DSP converts all data to linear values for RMS integration). The area between these markers also can be analyzed to indicate max/min power occurrences, long-term peak occurrence (peak-hold), long-term RMS average (LAVG), and peak-to-average power ratio (Fig. 7).

The DSP performs all trigger and measurement analysis directly on the acquired data (not on the displayed data), and it does not require that the operator have the display set in any particular way for proper operation. A dedicated video graphics processor continually processes the peak power data for display on an integral high resolution 256 color VGA compatible display. Both logarithmic and linear display modes are available for analysis. The screen display can be plotted or printed to a variety of supported devices.

Amplitude reference lines are provided to index absolute power levels on the VGA display. This feature, combined with display persistence, allows the large dynamic range requirements of a signal (or multiple signals) to be easily measured (Fig. 8).

On slower timebase settings (10 msec/div and slower), the DSP can process many more samples than can be displayed. In this situation, the DSP will over-sample to determine a pixel's value. The user can select whether the DSP will average a set of samples (normal mode) or select the highest value of the set (peaking-mode) to represent a pixel's value. With peaking-mode enabled, the DSP can peak-detect up to 5 million continuously acquired samples in one sweep.

Peak power data can also be continuously transferred to a host computer via the IEEE-488 GPIB port. This feature can be used to support extensive user analyses such as transmitter power histograms and peak power monitoring.

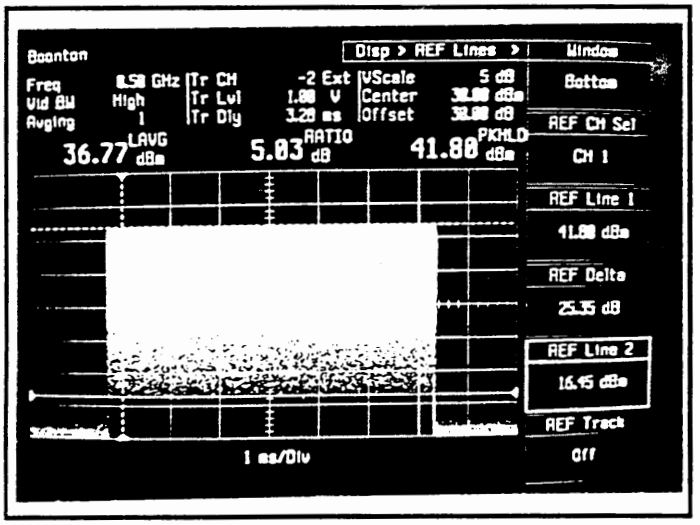
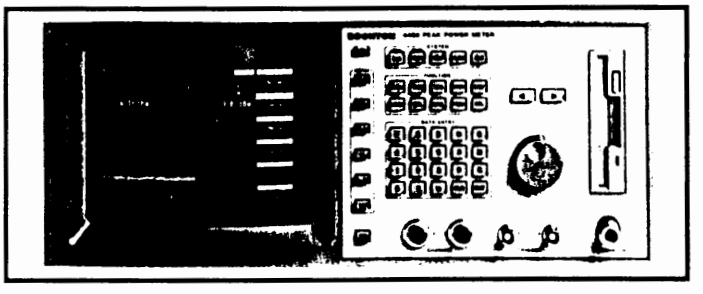


Figure 7 - RMS integration of area between time markers



Boonton 4400 Peak Power Meter

For more information contact Boonton Electronics, USA, at (201) 584-1077.

References

1 "Measuring Peak and Average Power of Digitally Modulated Advanced Television Systems", C.W.Rhodes & P.Crosby, IEEE Transactions on Broadcast Technology, December 1992

2 Digital Filters R.W.Hamming, Prentice-Hall, 1977

3 "Diode Sensors for the Measurement of True Power" R.E.Lafferty, Microwave Journal, November 1987

DELAY SPREAD MEASUREMENTS AND FEHER'S BOUND FOR DIGITAL PCS AND MOBILE CELLULAR SYSTEMS

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ABSTRACT

A simple and powerful technique and apparatus for delay spread measurements and analytical predictions is presented. Delay spread (τ) is one of the most critical practical radio propagation parameters in the design of US digital cellular standard, Japanese digital cellular and GSM European systems. Delay spread may also control the performance of several high data rate PCS/PCN systems.

The described measurement technique is suitable for laboratory and factory measurements, as well as for field measurements. A simple CW burst generator, spectrum analyzer and graphic plotter are configured to provide measurement accuracy within 5%. This accuracy is significantly higher than is required for most practical applications. We compare this measurement apparatus with considerable more sophisticated and unnecessarily complex test instrumentation. We highlight the advantages of the bursted RF method. Several field measurement results of indoor (up to 1 km), cellular (up to 10 km) and Public Land Mobile Radio (PLMR-up to 70 km) have been performed with the described method.

For analytical predictions of the maximal worst case delay spread bound τ_{max}, we introduce "Feher's delay spread bound" and compare it to numerous experimental data. We demonstrate that this simple bound "τ_{max}" requires only a knowledge of RF frequency and of transmit and receive (threshold) power. It is useful as a practical design tool for delay spread estimation of wireless systems.

Proceedings of the WIRELESS Symposium and Exhibition, San Jose, CA, Jan. 12-15, 1993.

1. DELAY SPREAD: THEORETICAL CONCEPTS AND TERMINOLOGY

The physical cause of delay spread is illustrated in Fig. 1. As an illustrative example we assume that at t = 0 one very short RF burst is transmitted from the base station located on the 70 m rooftop of a high-rise building. The "direct" LOS (line-of-sight) signal path has a length of d_0(m) and a propagation time (delay) of τ_0. The LOS path is obstructed by several buildings and has an obstruction caused signal attenuation of 60 dB. If d_0 = 1000 m = 1 km, then the free space LOS loss at 150 MHz, as shown in Fig. 2, is 101 dB. Thus, the total path loss of the direct signal path is 60 dB + 101 dB = 161 dB, see Table 1. The reflected multipath RF signals travel along of

$$d_1 + d_2, d_3 + d_4, \ldots, d_k + d_L$$

If the signal obstruction caused attenuation along these longer signal paths is not very large, e.g., assume 7 dB and 10 dB in Table 1, then the received reflected signals, having a considerably longer propagation delay than the LOS signal in the d_0 path, arrive to the mobile with received powers of comparable magnitude to the power of the LOS signal path. In this example, we assume that the signal received by the mobile, through the reflected delayed path $d_1 + d_2$, having a propagation delay of $\tau_1 + \tau_2$ is −119 dBm, that is, 2 dB higher than the obstructed LOS signal.

The reflected signal path $d_1 + d_2$, arriving at $\tau_1 + \tau_2$ has a delay, relative to the direct LOS signal of $\tau_A = \tau_1 + \tau_2 - \tau_0$. It is known as the first arrival delay (or delay spread). The second reflected signal, path $d_3 + d_4$, arrives at $\tau_3 + \tau_4$ and has a delay spread, relative to the d_0 direct signal path f $\tau_B = \tau_3 + \tau_4 - \tau_0$ and a received power of −138 dBm, that is, the received power of this delayed signal is 17 dB lower than the power of the direct path signal. In a real multipath environment a very large number, practically infinite, of delayed components are added. These components form a power delay profile.

2. DELAY SPREAD MEASUREMENTS

The impact of delay spread (τ) on the performance of mobile systems can be analytically evaluated, predicted by means of computer simulations and measured in the laboratory and/or in the field in a real multipath propagation environment. In this section laboratory and field measurement concepts are presented.

2.1 LABORATORY - DELAY SPREAD MEASUREMENT SET-UP

For laboratory delay spread measurements the delay model, profile, and/or amount of the delayed signal path and received levels are specified. System specifications are developed from field propagation experimental data and are based on overall cellular/mobile system network studies. A frequently used specification and model, illustrated in Fig. 3, is the radio and delay spread propagation model adopted by the TIA and EIA committees for the North American Digital Cellular (NADC) standard, known as TIA-IS 54. In this measurement set-up the transmitted modulated RF signal is fed to the direct path Rayleigh simulator, $R_0 e^{j\phi_0}$ and also to a delayed path Rayleigh simulator, having a simulated propagation delay of τ_1 [μs] and the same average power as the direct path. In Fig. 3 the second transmitter Tx2, transmits a modulated interfering signal, having the same center frequency as the main and delayed signal path. This interfering signal is simulating co-channel interference (CCI) C/I_c. It is passed through an independent Rayleigh simulator $R_i e^{j\phi_i}$ and a variable attenuator which sets the specified desired carrier power to CCI ratio, i.e. C/I_c. In these set-ups the individual Rayleigh fade simulators

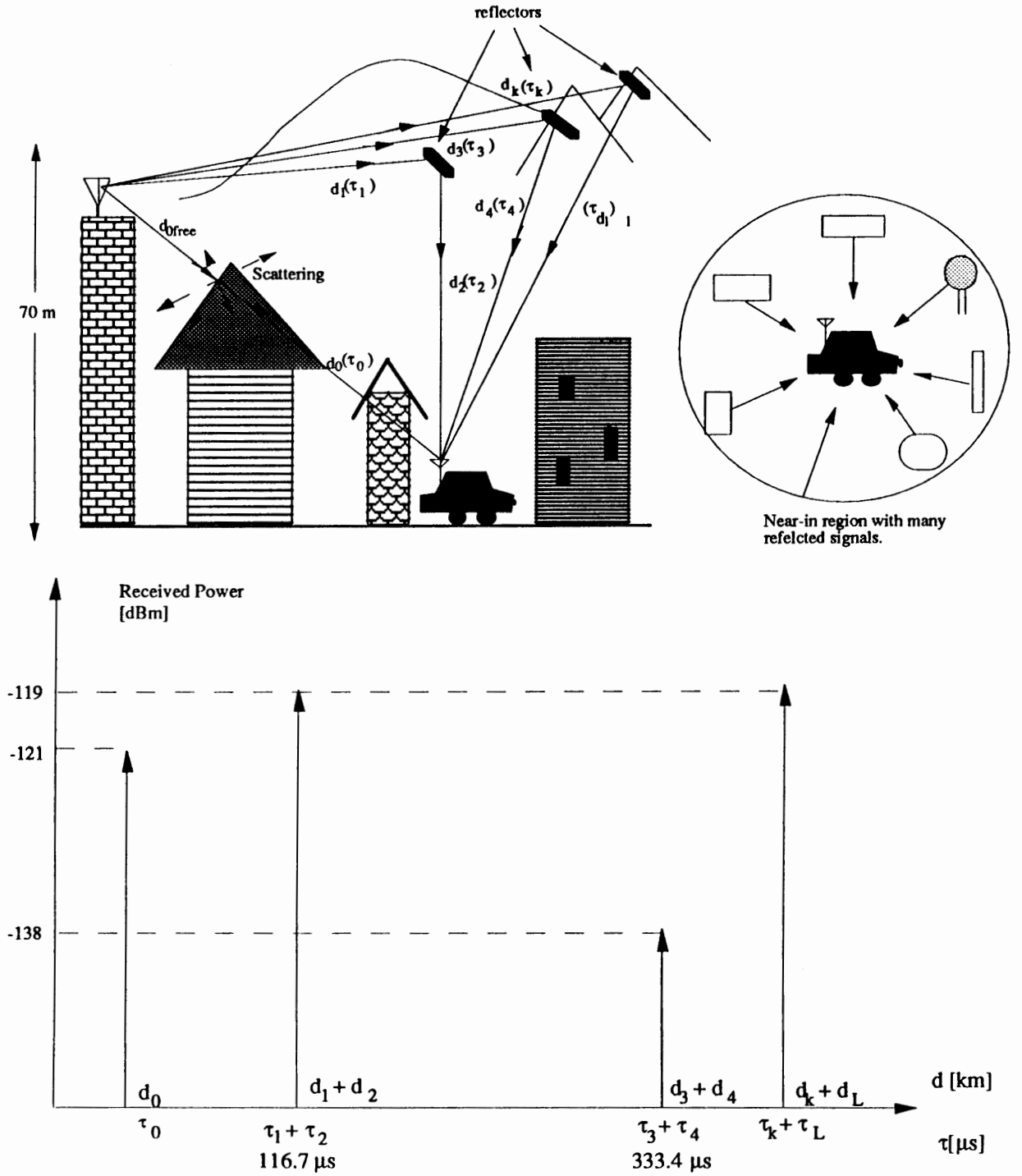


Fig. 1 Propagation environment of a land-mobile Line-of-Sight (LOS) and Non-Line-of-Sight (NLOS) radio system. The base station antenna in this illustrative example is at a height of 70 m. The direct LOS free space path "d_{0free}" is between the base antenna and the first building. Afterwards the direct d_0 path is attenuated. The distant mountains reflect the signals. The reflected delayed signals could be received at a comparable power level to the attenuated direct path signals. Ref. K. Feher [FE-B6].

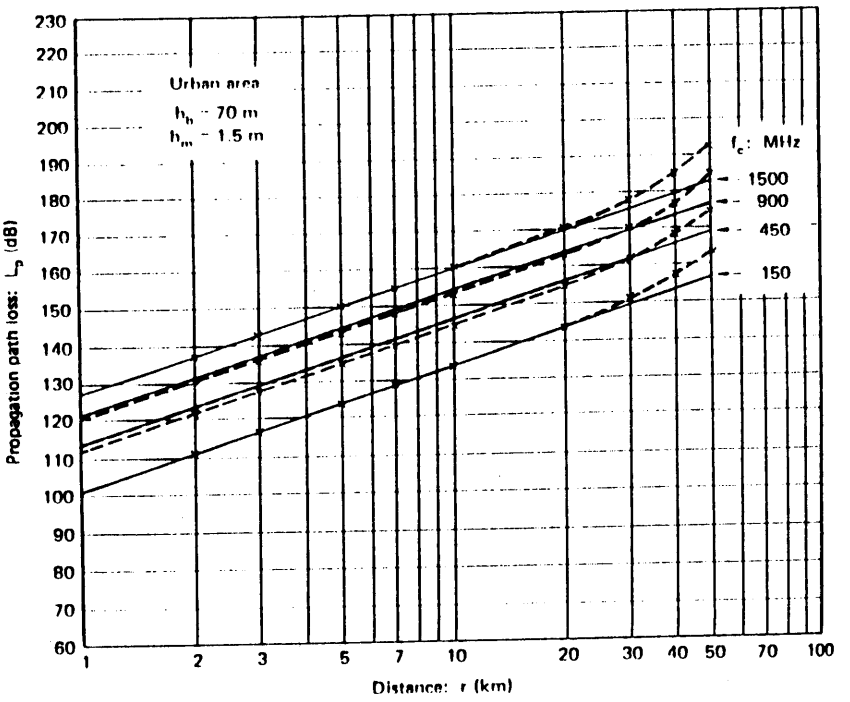
	Direct LOS Path "d_0"	1st Reflected Path "d_1+d_2"	2nd Reflected Path "d_3+d_4"
Total Propagation Distance	d_0=1km	d_1+d_2=36km	d_3+d_4=101km
Transmit Power P_T=10 Watt	40dBm	40dBm	40dBm
Propagation Path Loss (based on Fig. 2 at 150MHz)	101dB	152dB	168dB
Path loss due to buildings and other obstructions	60dB	7dB	10dB
Total path loss (L_T)	161dB	159dB	178dB
Received Power $P_R = P_T - L_T$ (dBm)	-121dBm	-119dBm	-138dBm
Total Propagation Delay	$\tau_0 = 3.3\mu s$	$\tau_1 + \tau_2 = 120\mu s$	$\tau_3 + \tau_4 = 336.7\mu s$
Delay Spread "τ" of Reflected Signal $\tau=(\tau_N+\tau_m)-\tau_0$	0 μs	116.7 μs	333.4 μs

Computation of $\tau_1 + \tau_2$ and $\tau_3 + \tau_4$:

$$\tau_1 + \tau_2 = \frac{d_1 + d_2}{c} = \frac{36 \times 10^3 m}{3 \times 10^8 m/s} = 120\ \mu s$$

$$\tau_3 + \tau_4 = \frac{d_3 + d_4}{c} = \frac{101 \times 10^3 m}{3 \times 10^8 m/s} = 336.7\ \mu s$$

Table 1 Delay spread "τ" and illustrative propagation loss values of a 3kHz narrowband 150MHz radio frequency Public Land Mobile Radio (PLMR) system. Values in this Table correspond to Fig. 1, Ref. [FE-B6].



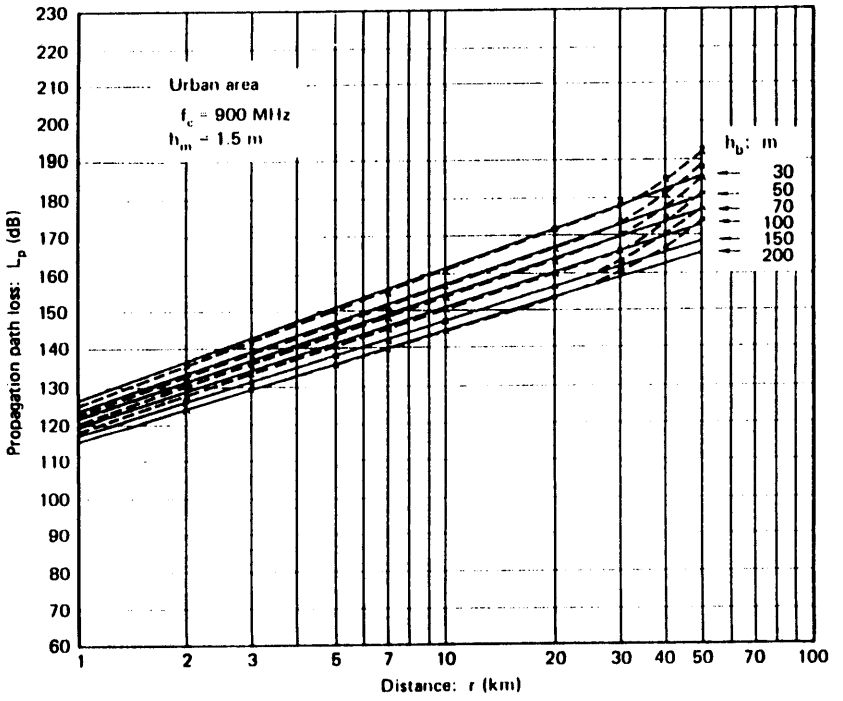


Fig. 2 Propagation path loss in urban area. Solid lines are obtained by empirical formula, dashed lines by Okumura's prediction method [FE-B5].

have adjustable Doppler frequencies. A considerably more complex laboratory delay spread simulator is illustrated in Fig. 4. In this simulator, adopted by the European GSM standardization committee, up to twelve delayed Rayleigh faded "taps" simulate the multipath Rayleigh delay spread environment.

2.2 DELAY SPREAD - FIELD MEASUREMENT APPARATUS

A simple and powerful delay spread field measurement concept and apparatus is shown in Fig. 5. In this set-up an RF oscillator (frequently designated as LO = local oscillator or CW = carrier wave generator) provides an unmodulated carrier wave to an "on-off" - RF switch. The amplified RF signal is illustrated at point **A** in the timing diagram. Note that the RF signal is turned "on-off" at a periodic rate, e.g., every 5 ms, and has a very short "on" duration, e.g., 100 ns. Practically a periodic RF impulse stream is generated and transmitted [DR-1]. The mobile receiver amplifies the received signal by a low-noise amplifier (LNA) and down converts it to a suitable intermediate frequency (IF), for example 140 MHz. The LNA and down converter could be part of a low-noise RF spectrum analyzer. By setting the RF-IF spectrum analyzer to a "zero IF" the spectrum analyzer envelope detects the received bursted carrier wave. The "resolution" bandwidth also known as "noise bandwidth" of the spectrum analyzer has to be sufficiently wide in order to preserve the "impulse nature" of the received signals. At the same time this bandwidth should not be to wide because the "noise floor" of the set-up increases with increased resolution bandwidth [FE-B4]. For a time resolution of approximately 5 μs a spectrum analyzer resolution (noise) bandwidth of about 300 kHz leads to acceptable measurement accuracy. To calibrate the time delay spread in the laboratory you may wish to add a calibrated delayed path "τ_{cal}" attenuated by 0 dB, 10 dB to 50 dB. This "pre-field" laboratory calibration assures that the set-up handles the amplitude dynamic range of interest and the required resolution accuracy of the time delay spread. The falling edge of the direct path corresponds to the τ=0 reference point.

More advanced delay spread field test sets have been developed by several engineers. The apparatus described by A. Zogg [ZO-1] utilizes a wideband RF signal obtained by an 8 bit length pseudo-random sequence ($2^8 - 1 = 255$ bits) having a 4.9 MHz clock rate. This baseband data stream modulates the RF carrier. The received modulated signal is coherently demodulated to the in-phase and quadrature signal components. The difference between the received multipath-delay spread signals and the reference signal is caused by propagation reflections "echoes". By obtaining the Fourier transforms and the inverse Fourier transforms the delay path/profile/spread characteristics are computed.

In summary, the simple set-up of Fig. 5 provides reasonable accurate measurements. The more advanced (and unfortunately more complex) set-up described by Zogg [ZO-1] requires considerably wider RF bandwidth. It leads to more data and somewhat increased field measurement accuracy.

3. DELAY SPREAD FIELD MEASUREMENT RESULTS

Delay spread has a tremendous impact on the performance of digital mobile radio systems and in particular on relatively high bit rate systems. If the rms delay spread τ exceeds about 10% of the bit duration, T_b then the BER performance degradation becomes significant. For a $\tau_{rms}/T_b = 0.25$, a high BER floor of about 3×10^{-2} has been observed. This severe impact of delay spread on the performance of digital cellular and PCS systems led to large scale global research and delay spread field measurement efforts. Hundreds of publications and reports contain delay spread field measurement data and analysis. Most IEEE conferences in mobile

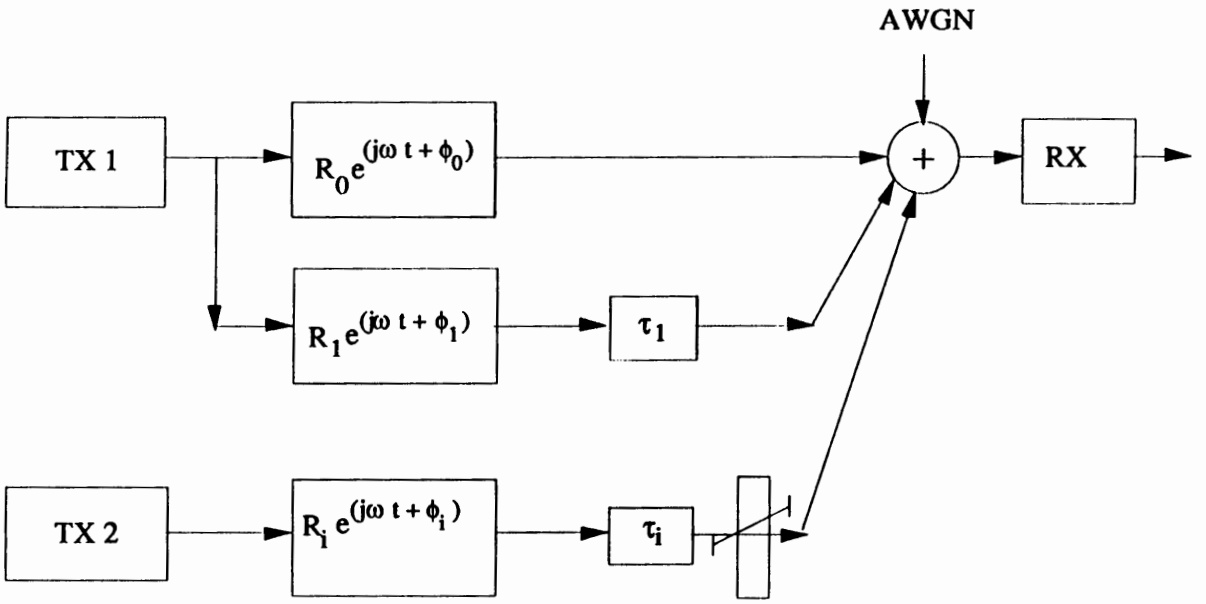


Fig. 3 Radio Propagation Simulator Model Specified by TIA and EIA committees for the North American Digital Cellular (NADC) standard. Co-channel interference comes from the adjacent cell transmitting at the same frequency. R_x is an independent Rayleigh fade simulator, with a given rms power gain. The specified rms delay τ_x is smaller than the symbol duration T_s, i.e., $\tau_x < T_s$ Ref. [FE-B6].

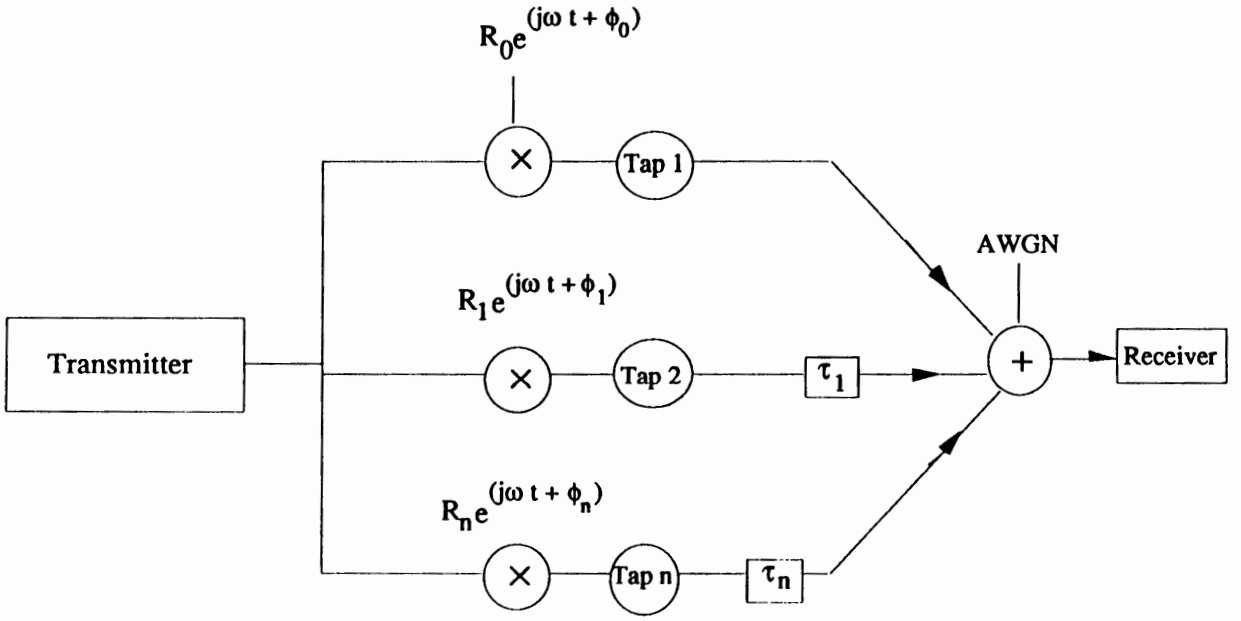


Fig. 4 Multi-tap Rayleigh/Rician fade simulator Conceptual-Implementation Diagram. In the GSM system specifications up to 12 taps have been specified. For the NADC (North American Digital Cellular) system, only two taps (worst case two taps) have been simulated. In this diagram, each tap represents a Rayleigh faded signal [FE-B6].

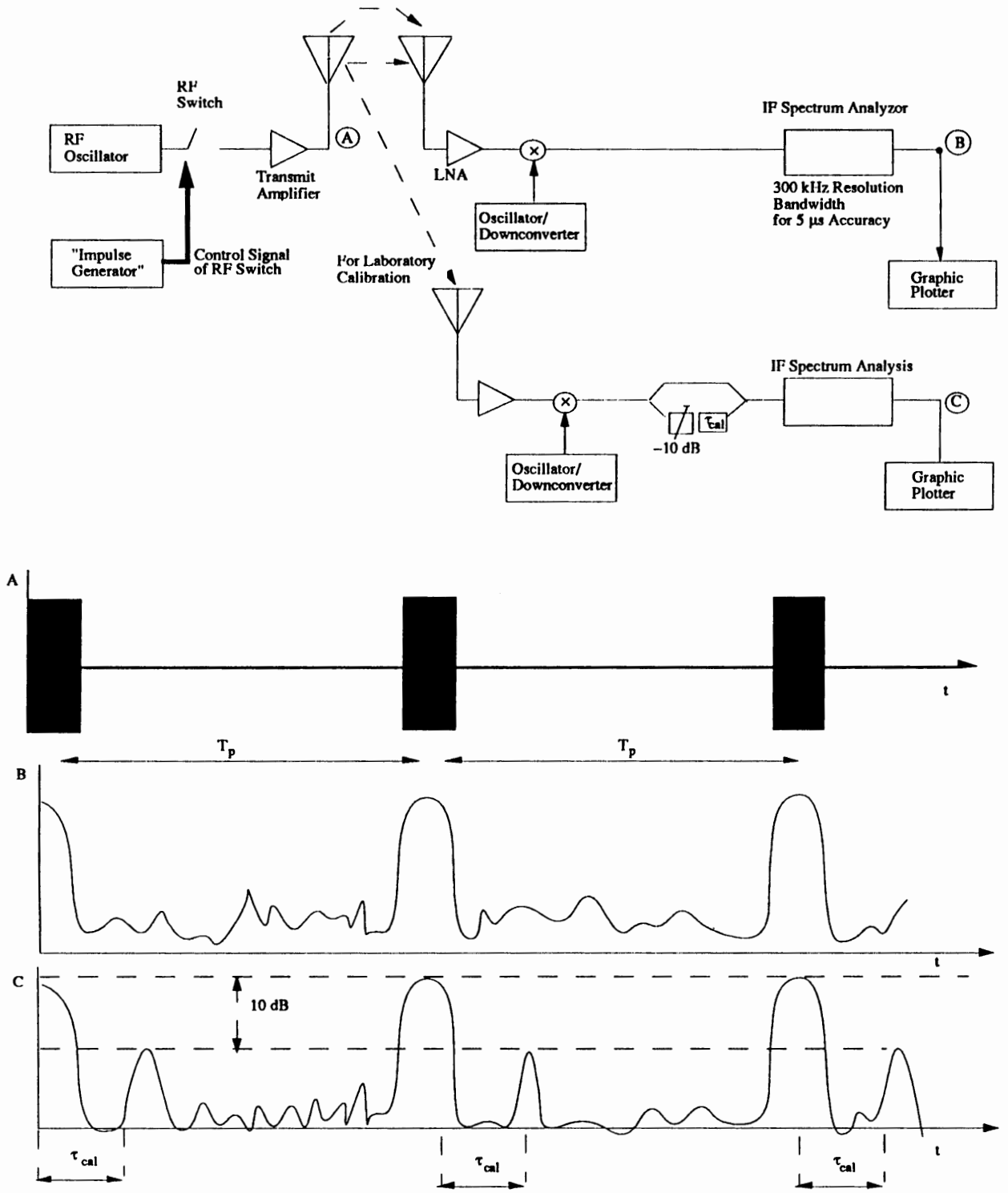


Fig. 5 Delay spread-measurement apparatus for simple field measurements. At point A, a wide-band short burst, having a repetition time of T_p is illustrated. At point B, a bandlimited pulse pattern with noise floor is measured. At point C, 10 dB attenuated and delayed signals are observed.

communications fields contain about 20 papers per conference proceedings and there are about 5 to 10 conferences per year in this area.

Instead of a comprehensive literature survey, which could require several hundred pages, we list illustrative delay spread measurement results for:

- cellular systems coverage up to 10 km: delay up to 100 μs
- land mobile radio coverage up to 70 km: delay up to 350 μs
- PCS indoor/outdoor coverage up to 30 m: delay up to 300 ns.

4. FEHER'S THEORETICAL DELAY SPREAD BOUND

A powerful and simple theoretical upper bound of worst case delay spread is introduced and derived in this section. Maximal delay spread, abbreviated as τ_{max}, is one of the most difficult measurement and estimation parameters. It can have a devastating effect on the BER (Bit-Error-Ratio) floor and overall mobile system performance.

This theoretical delay spread bound, introduced by Feher, leads to a simple estimation of "worst case" delay spread, based on knowledge of basic system parameters: transmit power (P_T), receive power at threshold (P_{Rmin}) and radio frequency (f_c). **It is an unexpected new discovery that, based on "Feher's bound-theoretical model", the environment, that is, surroundings, including urban or suburban, flat terrain, hills, or mountains, indoor short distance, e.g., up to 100m, or outdoor distance of up to many hundreds of km or even larger distances, have no impact on the delay spread bound, τ_{max}. Our theoretical limit applies to all mobile and all radio/wireless communications and broadcast systems applications.**

To derive the delay spread upper bound, we take a closer look at Fig. 1. In this "physical-engineering derivation" (contrary to sophisticated mathematical analysis and complex derivations of upper bounds), we assume that the "d_k" and "d_ℓ" signal paths having "τ_k" and "τ_ℓ" propagation delays are the longest line-of-sight (LOS) signal paths and that the reflection coefficient is 100%, that is, the total signal energy is reflected. Furthermore, we assume that the "direct" or shortest path is LOS for a short distance d_{ofree} and afterwards scattering and severe signal attenuation occurs in this direct path. For our upper bound derivation we assume that the delayed signal energy could have a significant impact on the system performance, e.g., BER = f(S/N) if the received power of the delayed path is at threshold level, that is,

$$P_{rmin} = P_{r\ threshold}$$

Thus, we have

$$d_{max} = r_{max} = d_k + d_\ell$$

and for LOS propagation, the path loss is given as the ratio of P_{Rmin}/P_T that is,

$$\frac{P_{Rmin}}{P_T} = G_T G_R \left(\frac{\lambda}{4\pi r_{max}}\right)^2$$

From this expression, we obtain

$$d_{max} = \left[\frac{P_T G_T G_R (\lambda/4\pi)^2}{P_{Rmin}}\right]^{1/2}$$

The delay spread bound of the propagation delay, that is, delay spread is given by

$$\tau_{max} = \frac{d_{max}}{c}$$

where P_T = transmit power, G_T and G_R represent the transmit and receive antenna gains and λ and c the wavelength (λ = c/f) and velocity of light respectively, f = radio carrier frequency.

Feher's maximal delay spread bound can be further simplified if omnidirectional unity gain ($G_T = G_R = 1$) transmit and receiver antennas are assumed. This simplified delay spread bound is

$$\tau_{max} = \frac{d_{max}}{c} = \left[\frac{P_T}{P_{R_{min}}}\right]^{1/2} \frac{\lambda}{4\pi} \frac{1}{c} = \left[\frac{P_T}{P_{R_{min}}}\right]^{1/2} \frac{c}{f} \frac{1}{4\pi c}$$

$$\tau_{max} = \frac{1}{4\pi} \frac{1}{f} \sqrt{\frac{P_T}{P_{R_{min}}}}$$

The following examples illustrate the simple and powerful estimation method offered by this bound:

Example 1: How much is Feher's delay spread bound τ_{max} of a 220 MHz Public Land Mobile Radio (PLMR) system if P_T = 1 Watt (+ 30 dBm) and P_{Rmin} = –90 dBm?

We use Feher's bound with unity gain omnidirectional antennas and the specified parameters:

$$\tau_{max} = \frac{1}{4\pi} \frac{1}{f} \sqrt{\frac{P_T}{P_{R_{min}}}}$$

For P_T = 1 Watt = 10^3 mW and P_{Rmin} = –90 dBm = 10^{-9} mW, we have $P_T/P_R = 10^{12}$, thus

$$\tau_{max} = \frac{1}{4\pi} \frac{1}{220 \cdot 10^6} \sqrt{10^{12}} = 361.7\ \mu s$$

Thus, the delay spread theoretical bound in this example is 362 μs.

Example 2: How much is Feher's delay spread bound for the European standard "DECT" system, having a transmit power of P_T = +24 dBm (250 mW) a receiver bandwidth of 1.1 MHz and a carrier frequency of f_c = 1.8 GHz. The receiver sensitivity is controlled by the receiver noise figure (F). This low cost system is designed for an F = 11 dB overall noise figure and requires a threshold (minimum) C/N of 23 dB.

To use the theoretical delay spread bound, first we have to compute P_{Rmin}. It is given by

$$P_{Rmin} = P_{R\ threshold} = kTBF + C/N$$

where

kT = −174 dBm/Hz

B = Receiver noise bandwidth

F = Noise figure of the receiver

C/N = required carrier-to-noise ratio in the receiver bandwidth

First we obtain the total noise N_T in the receiver

$$N_T = kTBF = -174\ dBm/Hz + 10\log 1.1 \cdot 10^6\ Hz + 11$$

$$= -174\ dBm/Hz + 60.041 + 11 = -103\ dBm$$

$$P_{Rmin} = N_T + C/N = -103\ dBm + 23\ dB = -80\ dBm\ (10^{-8}\ mW)$$

Thus,

$$\tau_{max} = \frac{1}{4\pi} \frac{1}{f} \sqrt{\frac{P_T}{P_{Rmin}}} = \frac{1}{4\pi \cdot 1.8 \cdot 10^9} \sqrt{\frac{250\ mW}{10^{-8}\ mW}}$$

$$\tau_{max} = 6.99\ \mu s$$

Note: the computed Feher's delay spread upper bound τ_{max} = 6.99 μs is about 20 times higher than typical indoor measurement results having a coverage of about 30 m. For systems having a coverage in the 1 km to 5 km range, a 7 μs delay spread is a typical measured result.

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Most of the material contained in this paper is based on and is closely related to the copyrighted material by Dr. K. Feher, Reference [FE-B6]. This material will appear in a forthcoming book and also in a journal/magazine publication.

REFERENCES

[FE-B1] K. Feher: "Digital Modulation Techniques in an Interference Environment," Encyclopedia on EMC, Vol. 9, Don White Consultants, Inc., Gainesville, Virginia, (1977-178 pages).

[FE-B2] K. Feher: "Digital Communications: Microwave Applications," Prentice Hall, Inc., Englewood Cliffs, New Jersey 07632 (1981-282 pages).

[FE-B3] K. Feher: "Digital Communications: Satellite/Earth Station Engineering," Prentice-Hall, Inc., Englewood Cliffs, New Jersey 07632 (1983-480 pages).

[FE-B4] K. Feher and Engineers of Hewlett-Packard: "Telecommunications Measurements, Analysis and Instrumentation," Prentice-Hall, Inc., Englewood Cliffs, New Jersey 07632 (1987-415 pages).

[FE-B5] K. Feher, Ed.: "Advanced Digital Communications: Systems and Signal Processing Techniques," Prentice-Hall, Inc., Englewood Cliffs, New Jersey 07632 (1987-710 pages).

[FE-B6] K. Feher: "Cellular Digital PCS-Mobile Radio Communications," a forthcoming book, copyright K. Feher, 1993.

[ZO-1] A. Zogg: "Multipath delay spread in a hilly region at 210 MHz," IEEE Transactions on Vehicular Technology, Vol. VT-36, No. 4, pp. 184-187, Nov. 1987.

Personal Communications Systems (PCS)

Session Chairperson: Randy Roberts,
Spread-Spectrum Scene (El Granada, CA)

**Paper presented by Henry Eisenson.*

GaAs MMICs FOR PCS APPLICATIONS

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Introduction

When personal communication services (PCS) were first proposed in 1989-1990, the objective was to develop a system that is more versatile and cheaper than the existing cellular mobile telephone (CMT) services.

The proposal was to divide existing CMT cells into hundreds of small cells and use a small, inexpensive handset that would work inside buildings and tunnels. The proposed frequency spectrum would be around 1.8 - 2.0 GHz in order to avoid serious background noise problems encountered by CMT services at between 800 - 900 MHz.

Although most of the original concept for PCS has been kept as the development moved forward, there might be a time in the future that PCS will encompass CMT services and become the ubiquitous single wireless phone for everyone, everywhere. People will carry phones with them and would be able to be reached at any time.

System Technology

Many competing systems are vying for dominance in the PCS market. It is not the scope of this paper to review every system proposed [1, 2]. In this paper, the discussion will be focused on the code division multiple access (CDMA) system proposed by Qualcomm and the DCS-1800, which is a Pan-European time division multiple access (TDMA) system. Key parameters for these systems are listed in Table I.

Table I

SYSTEM PARAMETERS

	Qualcomm	**DCS-1800**
Frequency Spectrum	1850 - 1900 MHz	1710 - 1880 MHz
Multiple Access	CDMA	TDMA
Duplexing	FDD	FDD
Channel Bandwidth	1.25 MHz	200.0 KHz
Traffic Channel on One RF Channel	32	8
Speech Rate	8.0 KB/S	13.0 KB/S
Modulation	QPSK	GMSK
Portable Transmit Power, Peak/Average	500 mW	1.0 W/125 mW

RF Systems for Portable Handsets

A generic block diagram of the RF system for portable handsets is provided in Figure 1 [2]. The present receiver and transmitter circuits are mostly homemade products made with discrete devices. This is because there are no cost effective, application specific MMICs available.

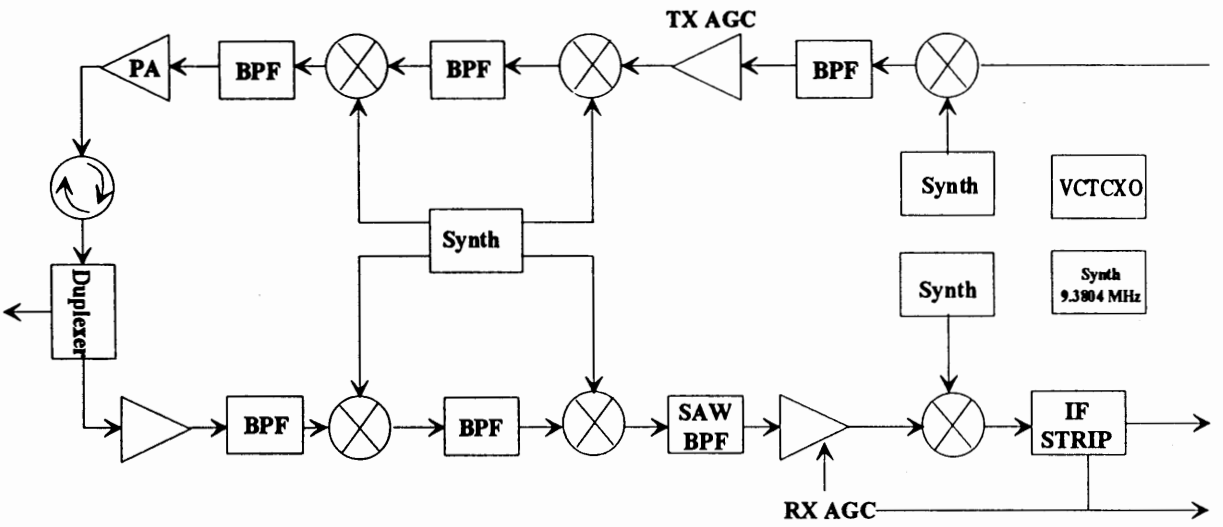


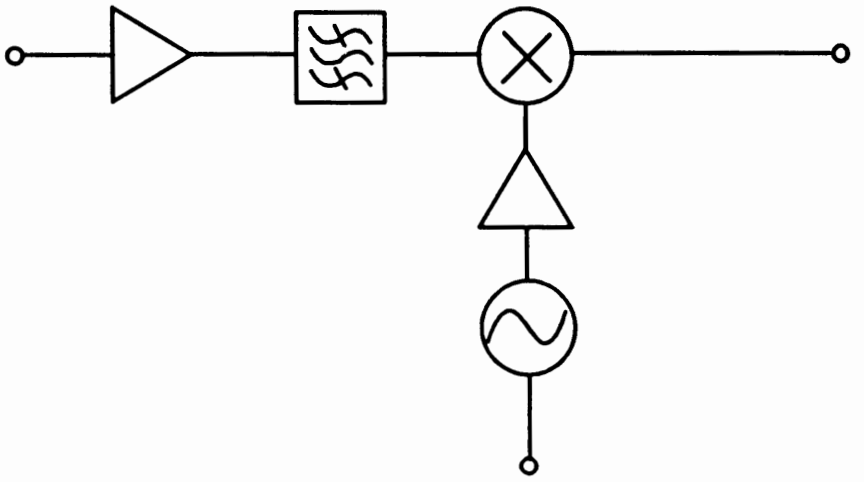
Figure 1. An RF System Block Diagram for Portable Handsets

GaAs MMICs for PCS Applications

Since 1989, cost effective GaAs MMICs for high volume production have become available for direct broadcast satellites (DBS), global position systems (GPS) and cable television systems [3]. GaAS MMICs are ideally suited for PCS applications because of the following performance advantages:

A. High Intercept Point
B. Low Noise Figure
C. Low Voltage operation
D. Low Current Consumption
E. High Power Added Efficiency

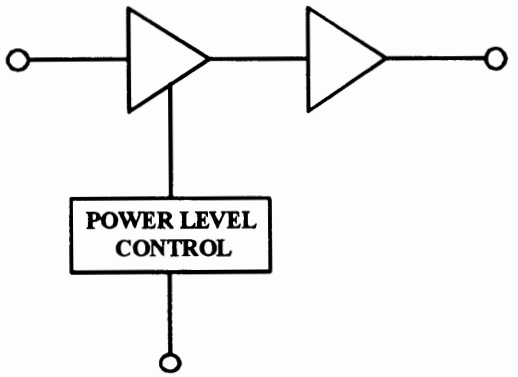
In Figures 2 through 4, block diagrams for GaAs MMICs currently under development for PCS are provided. The receiver circuit, as shown in Figure 2, will replace a low noise amplifier transistor, a mixer diode, a bulky image rejection filter, and also provide a local oscillator and a buffer drive to the mixer. All of these functions will be integrated on a single GaAs chip. It will use a tiny (0.4 mm) square plastic surface mount package. The power supply for the receiver MMIC is 3.0V and 13 mA, which is comparable to the best results achievable by using discrete devices.



RF Frequency	**1900 MHz**
IF Frequency	**150 MHz**
Conversion Gain	**20 dB**
Noise Figure	**2.5 dB**
Image Rejection	**15 dB**
Input Intercept Point	**-10 dBm**
Power Supply	**3 V, 13 mA**

Figure 2. Receiver MMIC Specification

The power amplifier MMIC, as shown in Figure 3, will use a 16 pin surface mount SOIC package and will operate with a 3.0V power supply. The linearity and power added efficiency of this MMIC is comparable to the much larger discrete hybrid power modules.



FREQUENCY	**1900MHz**
Output Power	**500mW**
Gain	**30dB**
Power Efficiency	**45%**
	(Spurs at -30dBc)
Power Supply	**3V**

Figure 3. Power Amplifier MMIC Specification

The transceiver circuit, as shown in Figure 4, will be customarily optimized for each application in order to maximize the benefits of the monolithic integration.

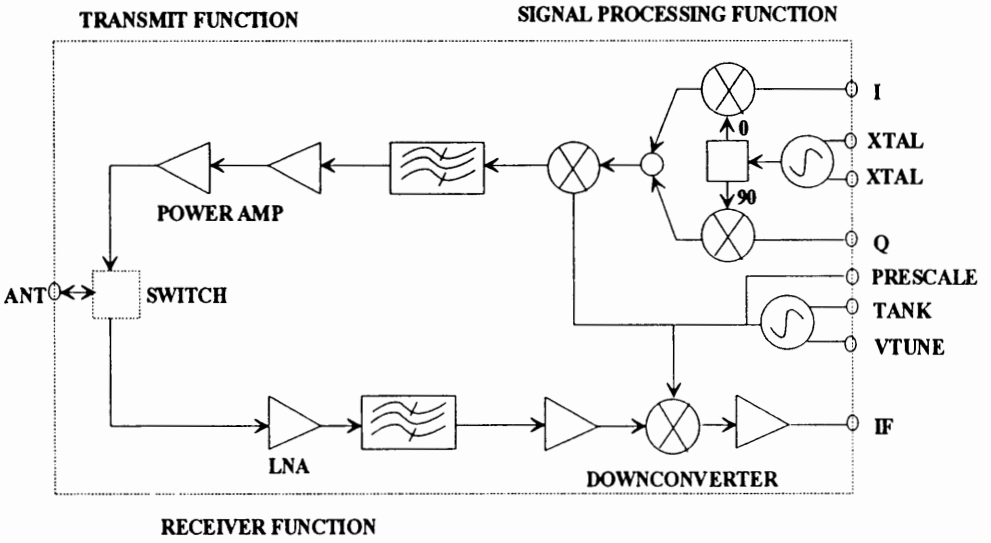


Figure 4. A Transceiver MMIC Architecture

These MMICs should prove very successful in the marketplace because they offer size and weight advantages when compared to discrete device solutions. Furthermore, the MMIC reduces the engineering development effort and simplifies the manufacturing process. Consequently, the quality and reliability of the final product is improved, while the cost of manufacturing is reduced.

Summary

GaAs MMICs for PCS applications should become available in 1993 and the market prospects for these products is bright.

References

1. D. Cox, "Wireless Network Access for Personal Communications," IEEE Commun. Mag., p. 96, Dec. 1992.

2. Qualcomm, "RF Vendor's Forum, CDMA and PCN," San Diego, Aug. 1992.

3. C. Huang, "MMICs Move Into New Marketplaces," Microwaves & RF, p. 134, Sept. 1992

A High-Efficiency GaAs MMIC Power Amplifier for 1.9 GHz PCS Applications

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Abstract

A high-efficiency 1.9 GHz GaAs MMIC power amplifier has been developed for emerging PCS applications. Operating at 3V of DC supply, the module achieves a typical RF output power of +27.5 dBm at 1890 MHz with an RF input power of 3 dBm and an overall DC-RF efficiency of 50%.

I. Introduction

Emerging PCS applications such as DECT (Digital European Cordless Telephone) and PHP (Personal Handy Phone) place stringent demands on RF component designers. Aggressive size and cost targets require highly integrated solutions. In addition, to maximize talk time, these next generation systems require high DC power efficiency at low supply voltage.

The RF power amplifier is a particularly challenging piece of the overall PCS system, since traditional silicon bipolar or BiCMOS approaches fall well short of the needed performance. We report here on a novel 2-stage power amplifier which sets new standards for DC power efficiency, accomplished through a GaAs MMIC (monolithic microwave integrated circuit) approach. The MMIC approach is ideal for consumer electronics because of its ability to be mass produced at a low cost.

II. Design Approach

The power amplifier was designed to meet the following objectives:

1. Low DC voltage, 3.0V nominal, 2.7V minimum.
2. +27 dBm output power and 50% efficiency
3. High gain, 30 dB goal, 25 dB minimum
4. Manufacturable low cost design
5. Ability to reconfigure to 2.4 GHz.

The performance criteria of objectives 1 through 3 dictated a relatively low pinch off, high f_t GaAs process. Additionally, the desired efficiency required that the output match be external to the chip as the Q of MMIC matching structures are relatively low. The ability to reconfigure the module to 2.4 GHz also required the input, output, and interstage matching to be external.

The functional schematic diagram, Figure 1, indicates the portion of the circuit which is included on the MMIC and the additional external components required. The MMIC itself uses 0.5 um gate length technology and has 2 stages of amplification with associated bias circuitry. The driver stage and the output stage are 600 um and 5000 um gate widths, respectively. The MMIC is 0.036 x 0.036 inches in area. The external L-C matching structures are a combination of standard 0603 surface-mount capacitors and printed transmission line inductors. The PCB used in the module is standard 0.031 inch thick FR-4 board.

The module, shown in Figure 2, is 0.810 x 0.515 x 0.160 inches in size. It requires a Vdd of +3V and negative bias of -1.2V and -1.5V for the driver stage and output stage respectively. The negative voltage can be generated by a simple switched capacitor design as the required negative current is less than 2 mA.

III. Measured Performance

The small signal gain, input, and output VSWR are shown in Figure 3. The output power vs. input power is shown in Figure 4. The measurements show that reasonable power is achieved even at 0 dBm but to achieve 50% efficiency it is necessary for the input power to be +3 dBm. Another important requirement is the ability to control the output power of the amplifier. This is accomplished by controlling the negative bias to the amplifier. Figure 5 shows the reduction in power and efficiency as a function of this control. In actual use it is not possible to create the -3.1V required to pinch off the device from a 3V battery. Therefore, external circuitry was developed that switches off the +3V Vdd line when the transmitter is not in use. This has been possible due to the graceful degradation in output power as Vdd is reduced. Figure 6 indicates that at 2.7V the module achieves 26 dBm and degrades to 23 dBm at 2.0V.

IV. Conclusion

A small, high-efficiency 1.9 GHz GaAs power amplifier has been demonstrated. The GaAs MMIC based design will meet the stringent demands of performance, size, and cost in the PCS market.

V. Acknowledgment

The author would like to acknowledge the technical contributions of Steve Cripps, Gary Lizama, and Fernando Aguilar.

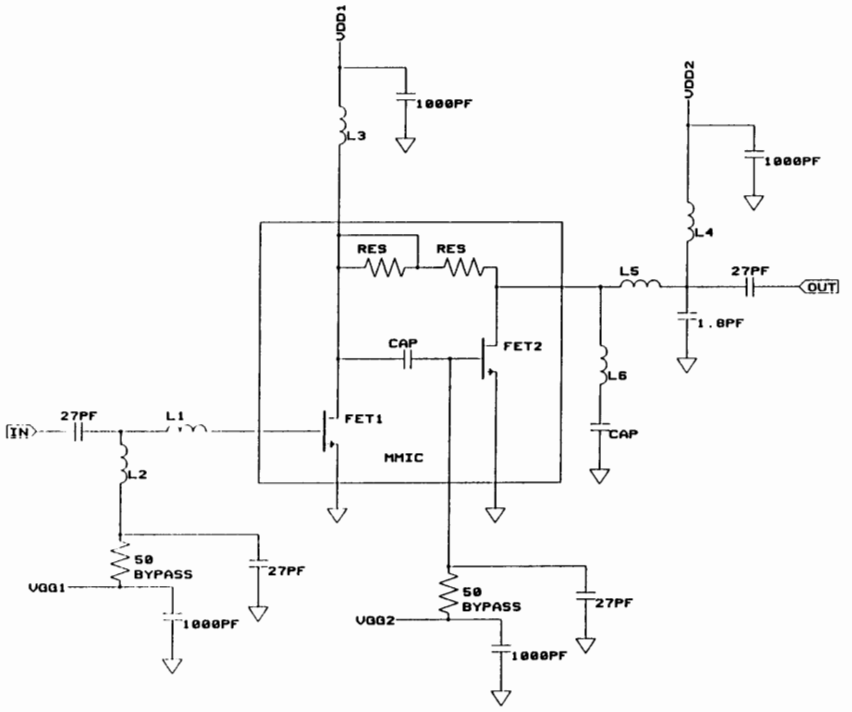

FIGURE 1. POWER AMPLIFIER MODULE SCHEMATIC

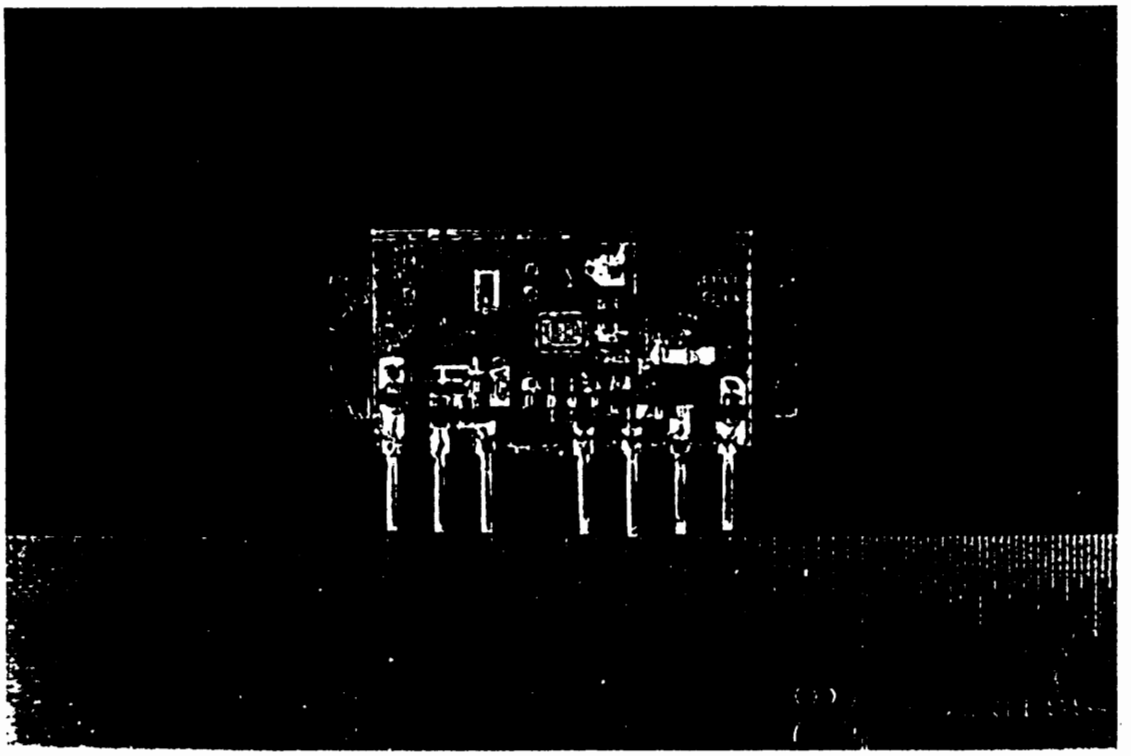

FIGURE 2. POWER AMPLIFIER MODULE

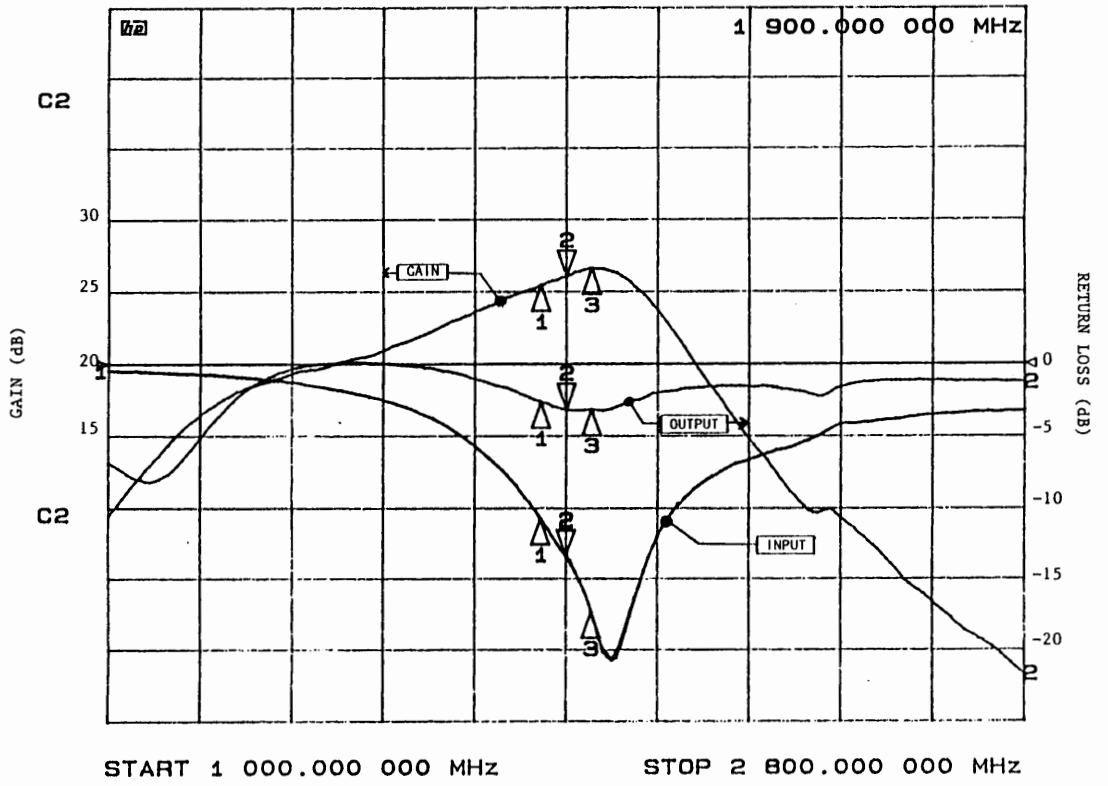

FIGURE 3. SMALL SIGNAL CHARACTERISTICS

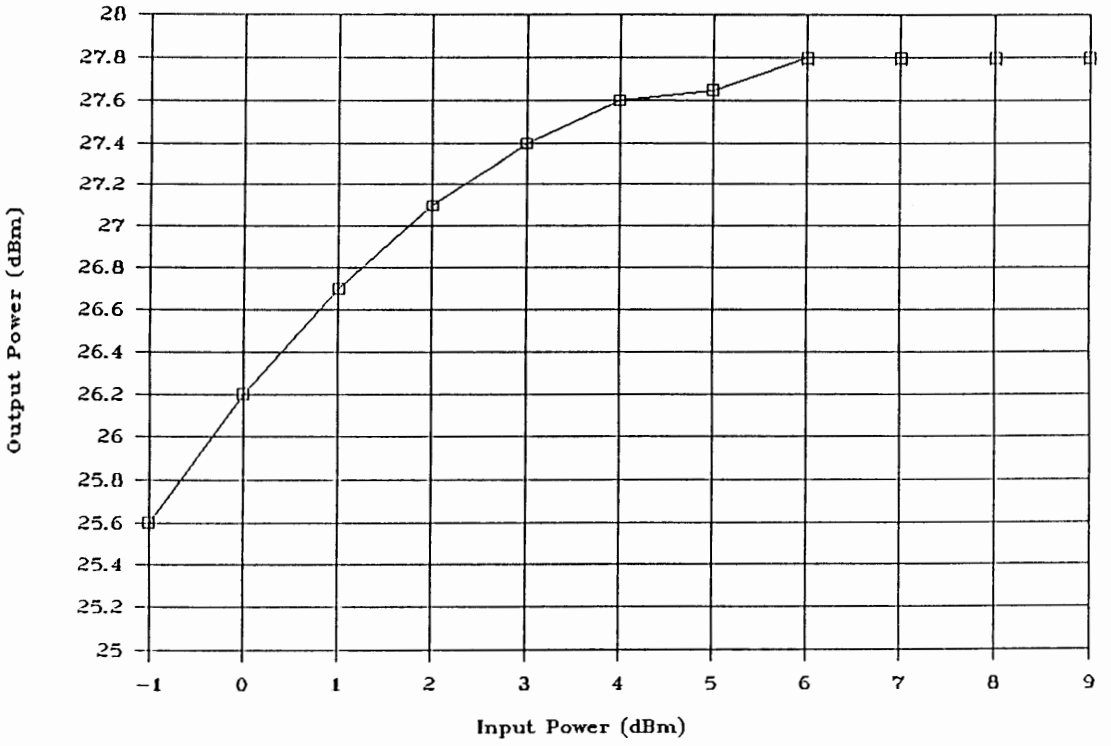

FIGURE 4. OUTPUT POWER vs. INPUT POWER

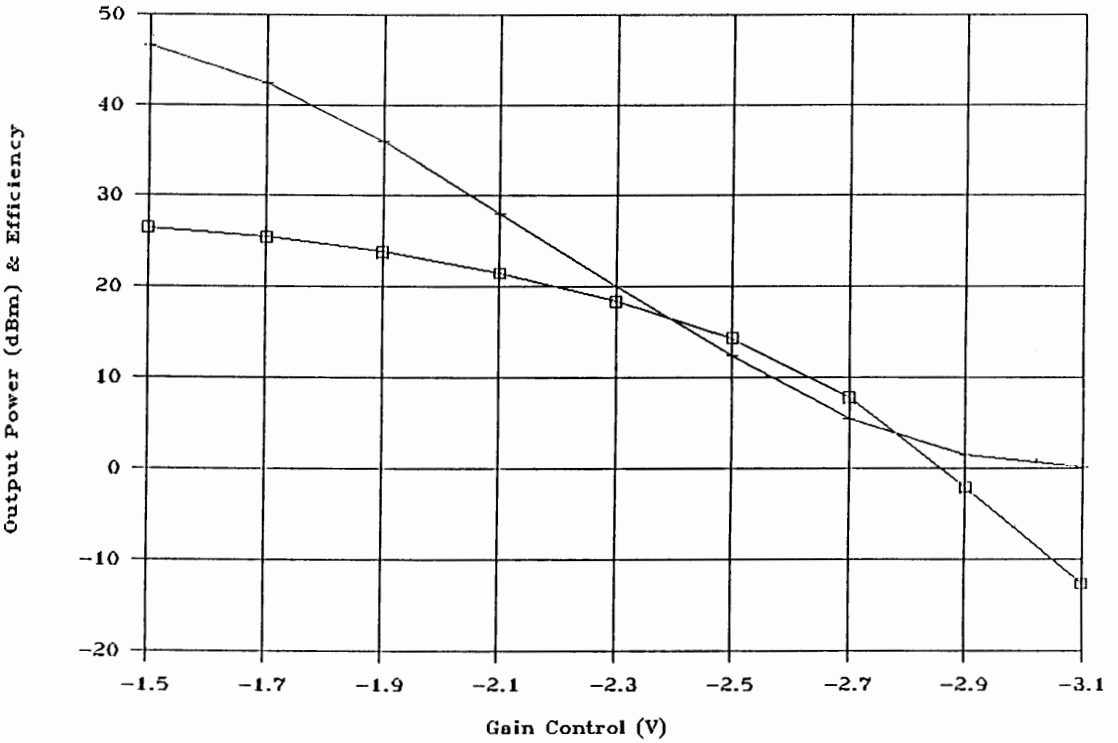

FIGURE 5. OUTPUT POWER EFFICIENCY vs. GAIN CONTROL

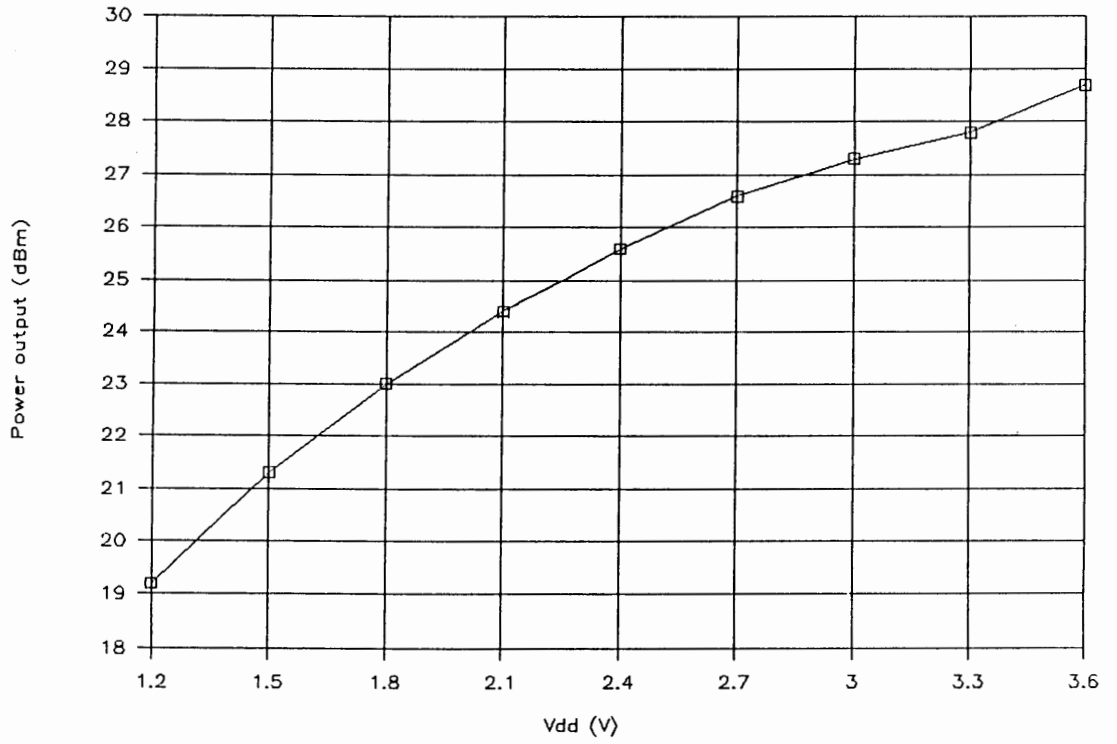

FIGURE 6. POWER OUTPUT vs. DRAIN VOLTAGE

LOW COST SIGNAL PROCESSING COMPONENTS FOR THE CELLULAR MARKET

by
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INTRODUCTION

In the last few years, the cellular telephone market, the market for global position systems, and the cordless telephone have expanded dramatically. While this new technology offers greater advantages for the users, it is very cost sensitive. Typical components for signal processing are mixers, power dividers, hybrid transformers, switches, various types of attenuators, phase shifters and even modulators. Construction of these components reveals instantly that there are a number of labor costs affecting the production price and, therefore, there is a critical need to find manufacturing methods to reduce these labor related costs. The traditional method of handling this has been to employ off-shore production facilities with low labor costs, but this is only a temporary fix as costs will increase there in the future as well. Synergy Microwave has successfully looked into changes in the physical design of the components with a goal to automate production in the USA, eliminate manual wiring and thereby reduce costs.

APPROACH

Radio Frequency (RF) components, commonly referred to as signal processing components, require ferrite cores and twisted (bifilar, trifilar and quadrafilar) wires for their construction, which makes it difficult for automated assembly. Since most of the ferrite cores are either in the form of a toroid or a balun, manual operation is required. This automatically means a labor intensive process. Figure 1 shows the traditional way of manufacturing an RF cellular mixer, which serves as an example of using toroidal transformers and Schottky quad rings. These toroids are usually hand-wound and secured in place prior to being connected to the diode ring. The following assembly steps are required:

1. By using epoxy or epoxy adhesive, the diode ring has to be secured to the mounting base of the assembly.

* **Patent pending**

2. The hand-wound transformers have to be placed in the appropriate locations and secured.
3. All connections have to be made with hand-wiring.
4. The assembly has to be cleaned with a combination of chemical treatment and forced air.
5. In order to obtain a sturdy and rugged design, either epoxy or potting compound is used.
6. Finally, the cover is either soldered or welded to the base assembly.

In reviewing this process, it becomes obvious that it is time-consuming and labor intensive.

Synergy Microwave has developed an innovative method* which drastically reduces the assembly time, improves and maintains constant performance. This new method of assembly is shown in Figure 2. The layout consists of an SMD printed/bonded diode ring which will become part of the assembly. Instead of using toroid or balun cores, ferrite rods (marked T1 and T2 in Figure 2) have been selected. By incorporating the winding on the cores as part of the assembly process (interconnection between the diodes and transformer), an economical way of assembling an array of these mixers at one time is achieved. Encapsulation and sealing are also done in one step. This manufacturing process incorporates repetition and consistency as key features since the tedious, awkward and expensive manufacturing process of winding wires around the toroid and baluns is streamlined. In these instances, the wire must be repeatedly looped in and out of central hole or holes. As the holes become much smaller, these windings become more difficult to achieve. It also becomes difficult to affix a toroidal transformer to the mounting base where there are insufficient flat edges. In the case of a balun structure, the windings are exposed on the flat surface. In the case of RF transformers the typical diameter of the central holes for a balun is approximately .020 inches and generally AWG36 to AWG30 sized wire is used. Unlike the toroid and balun cores, rods can more easily be placed and the windings can be handled more conveniently. The most effective method of attaching the rods to the surface is to provide a recess of the proper size on the mounting base, which is referred to as a base. Using the base as a substrate, Schottky diodes, either in ring or cross-over configuration, can be cost effectively mounted and the leads of the diodes will be brought out in the form of pads as interconnection to the transformers using either a bonding, welding or soldering technique. The ferrite rods are then firmly secured to the substrate as shown in Figure 2. The same basic design can be used for

various frequency ranges which require different numbers of turns or diodes with different characteristic performance.

The substrates are available in standard panel sizes either 8" x 8" for alumina or 24" x 24" for epoxy, fiberglass material or Teflon. Figure 3 shows such a panel assembly. Individual substrates are scribed so that each of the components can be separated easily by snapping. Diodes are assembled on the substrates while on the panel. The required amount of glue is dispensed into the recesses of the substrate and rods are placed into these recesses by a pick and place machine. After proper baking, at a specific temperature for a precise period of time, the panel is ready for further assembly. After winding the required number of turns of the twisted wires on the first ferrite rod, the transformer leads are connected to the diodes and package leads. This same procedure will be used for the second core. All the units on the substrate are assembled utilizing the above-described method. Therefore, the complete panel can be cleaned at one time and then it is ready for the next manufacturing operation. It is recommended that an inspection be conducted following each production step.

Special molds are used and hold the required quantity of encapsulating compound for each device. Molds in the form of an array are designed in such a way that -- with the exception of the package leads -- the rest of the assembled material is fully covered by the encapsulating material. This material is then baked at the appropriate temperature sufficiently long enough to achieve the proper consistency. Once the mold is removed, the individual components are then snapped apart. This process of manufacturing for RF components can be automated by using the above outlined procedure. The same basic procedure can be applied to different types of RF signal processing components using this new and innovative technique. Therefore, even modulators and other complex assemblies are available in smaller sizes. CELLULAR & PCN BAND MODULATORS CAN BE PRODUCED INEXPENSIVELY.

To highlight this new manufacturing method, we are now looking at two components, namely a double-balanced mixer and power divider. Depending on the number of required turns in the transformer, the design can be optimized for certain frequency ranges and bandwidth. To achieve the optimized design, parasitics are kept to a minimum. The advantages of this new approach by Synergy Microwave are best demonstrated by comparing measured data. Figure 4 shows the plot of conversion loss as a function of intermediate frequency (IF) for two fixed RF signals. These plots are the results of mixing fixed RF signals with a variable local oscillator (LO). Figure 5 shows the isolation

between the LO and RF ports and the LO and IF ports as a function of frequency. For the purpose of this discussion, the plots cover the cellular radio frequency band. In the case of a second example, we looked at an in-phase (zero degree) two-way power divider. The theoretical loss for such a two-way power divider is 3dB. Any loss in excess of 3 dB is called the insertion of the power divider. Typical parameters for the power dividers are insertion loss, amplitude and phase imbalance between the outputs, and isolation between the output ports when the input port is terminated in proper impedance (generally 50 Ω). To see the differences between various frequency ranges, two power dividers with different numbers of turns are compared.

Figures 6 and 7 describe the two-way power divider with two turns and whereas Figures 8 and 9 describe the power divider with three turns. The power divider with two turns has a better high frequency response whereas the one with three turns has better lower frequency response.

SUMMARY

As the cellular radio, global position systems (GPS) and cordless telephone markets require both high performance and low cost signal processing components, Synergy Microwave has successfully demonstrated a new and innovative manufacturing method which allows one to obtain and maintain high performance at greatly reduced costs. The process detailed herein is also subject to various patents pending for Synergy Microwave.

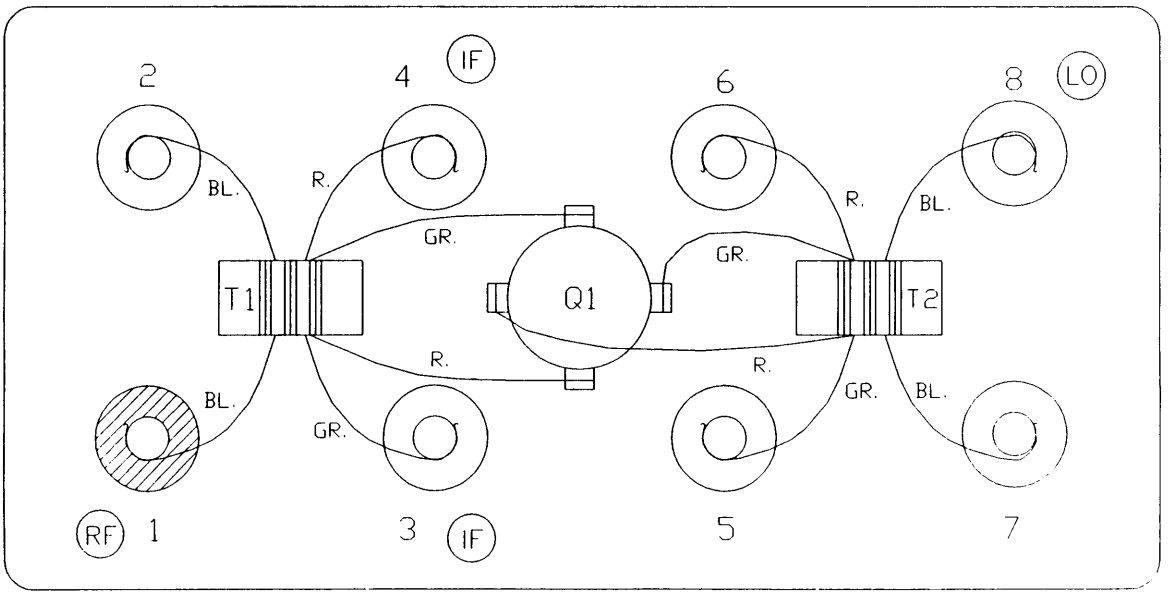


Fig.1 Typical assembly of a double balanced mixer using conventional technique.

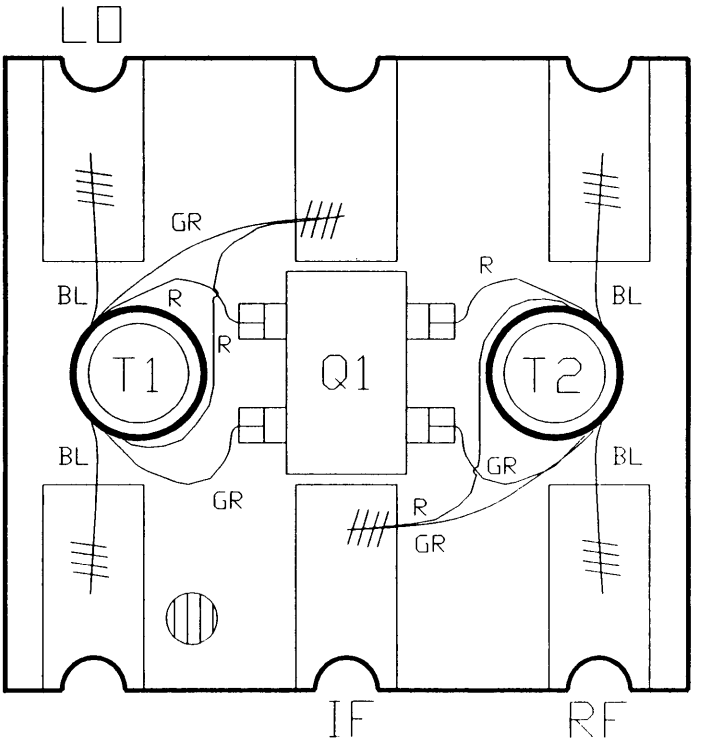


Fig.2 Typical assembly of a double balanced mixer using the new method.

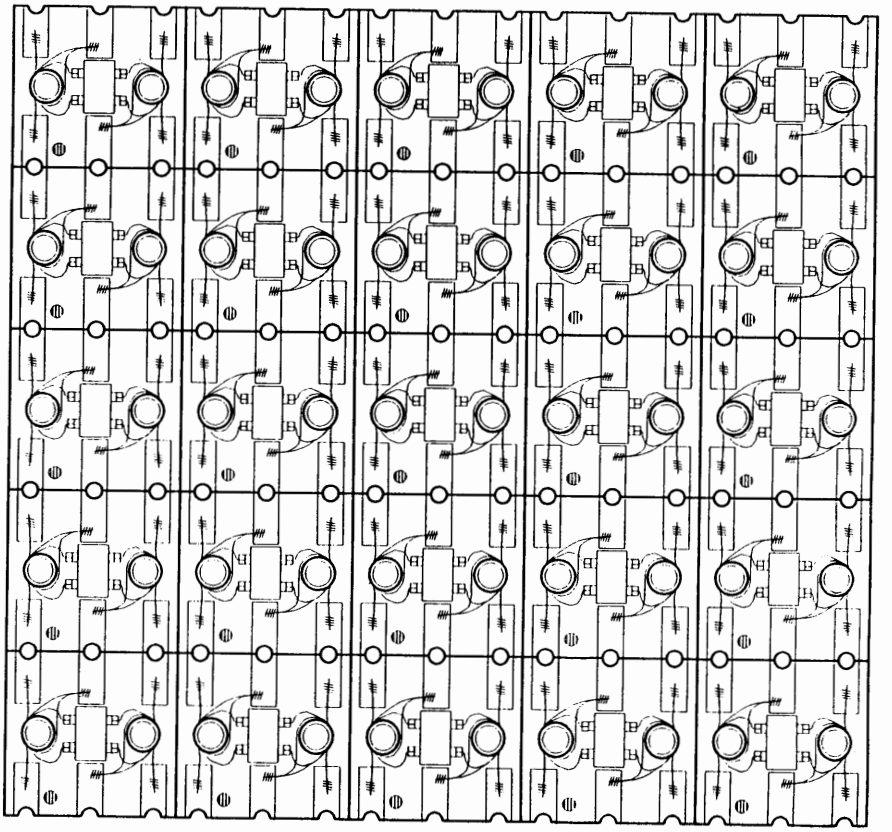


Fig.3 Panel Assembly

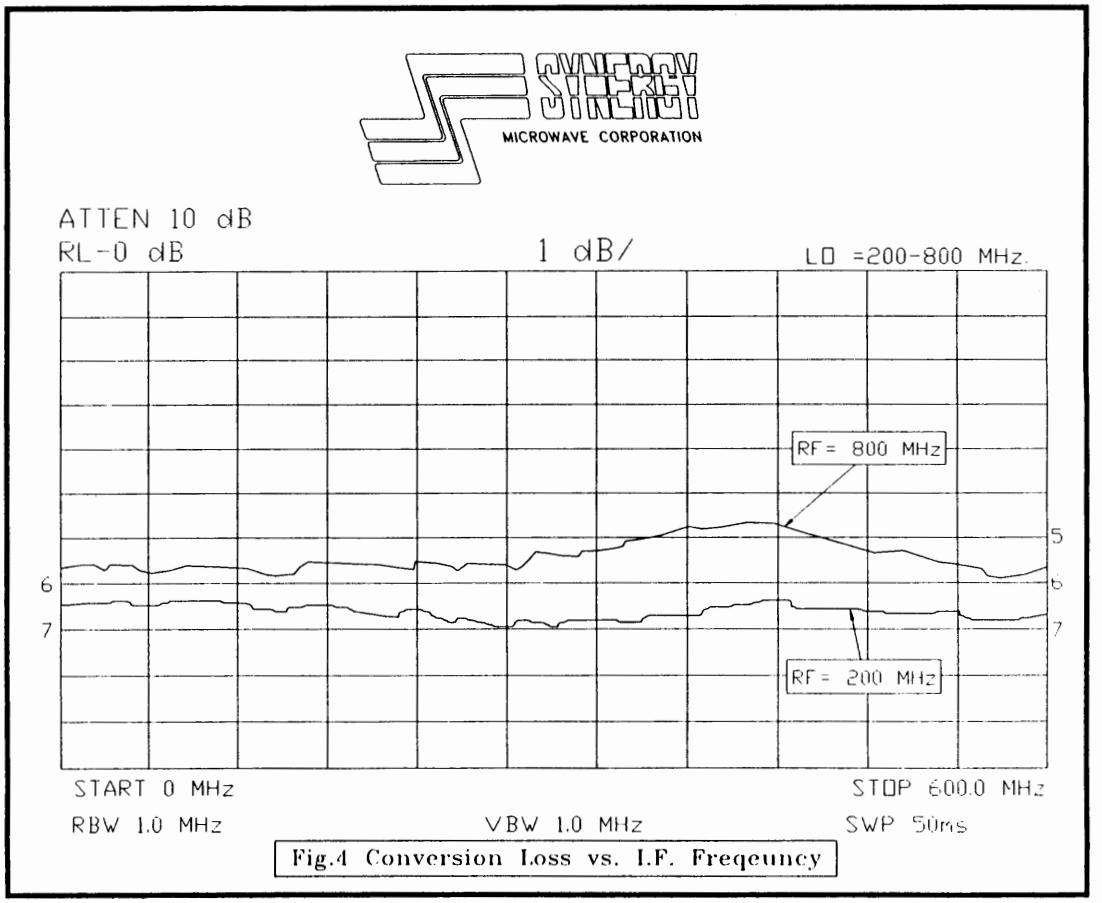


Fig.4 Conversion Loss vs. I.F. Freqeuncy

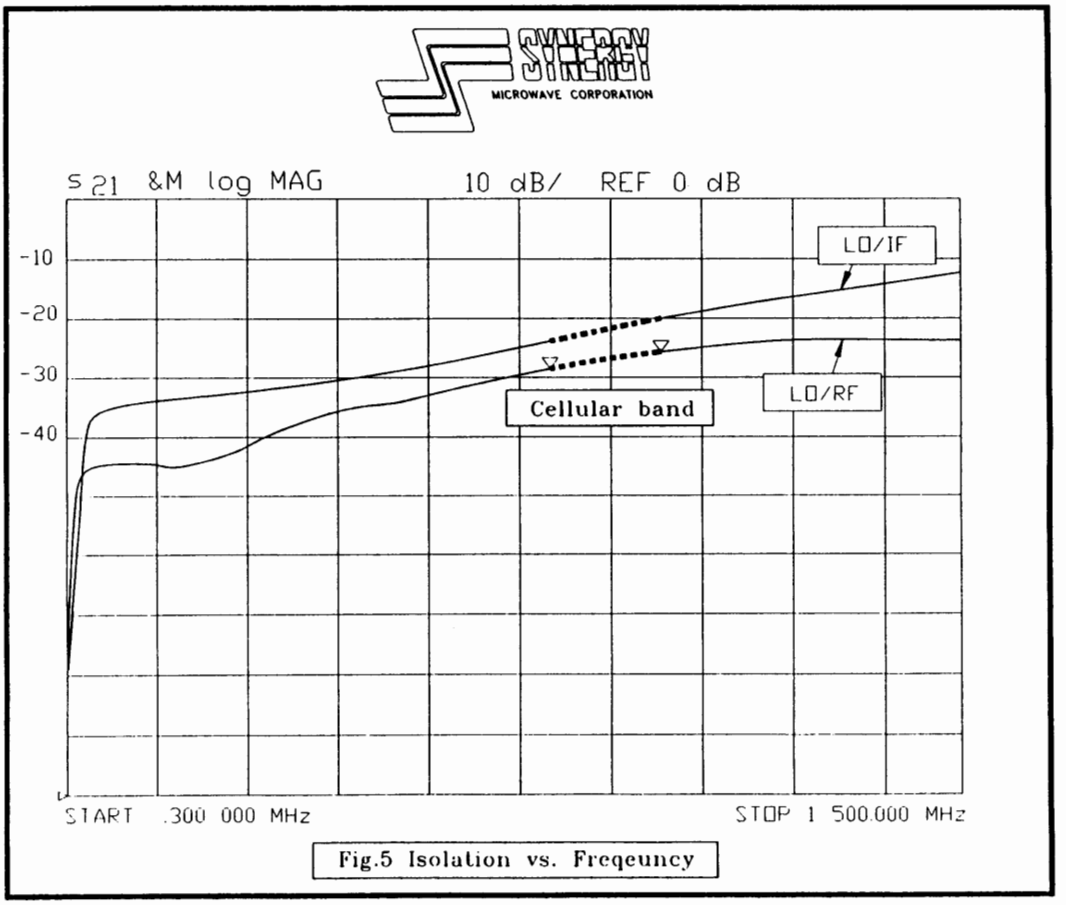


Fig.5 Isolation vs. Freqeuncy

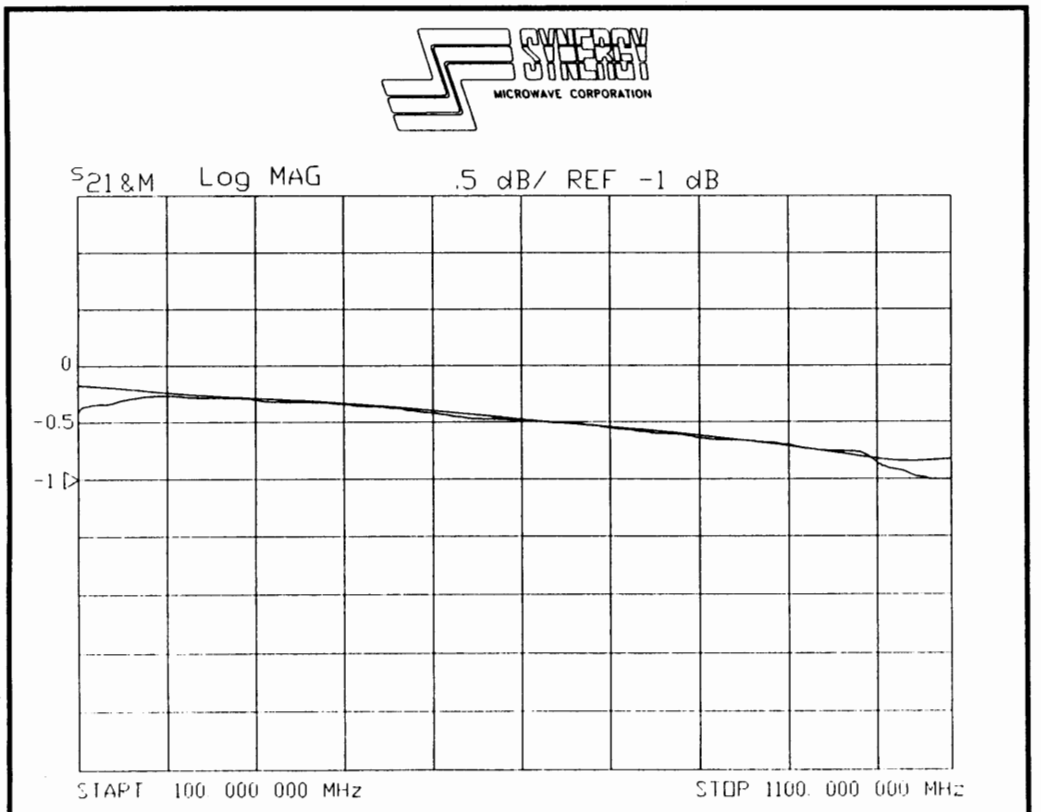


Fig.6 Insertion Loss vs. Freqeuncy for 2-way power divider with 2 turns.

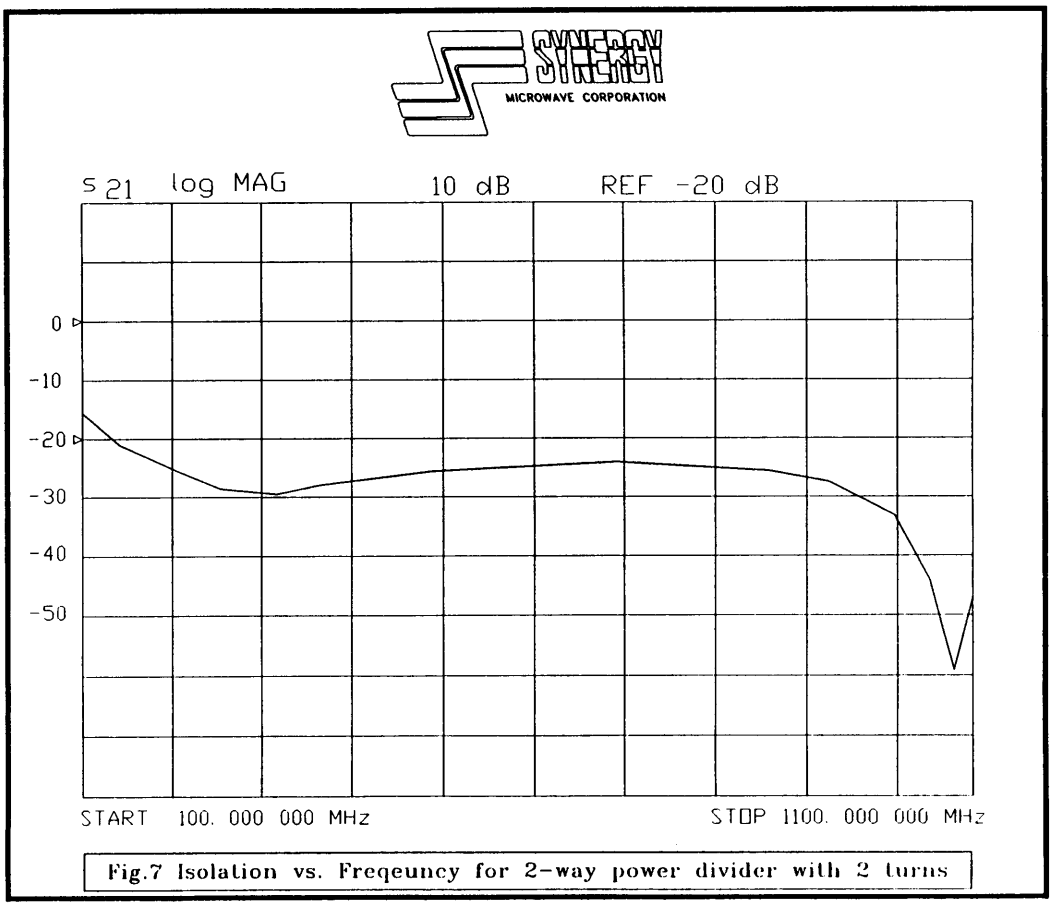


Fig.7 Isolation vs. Freqeuncy for 2-way power divider with 2 turns

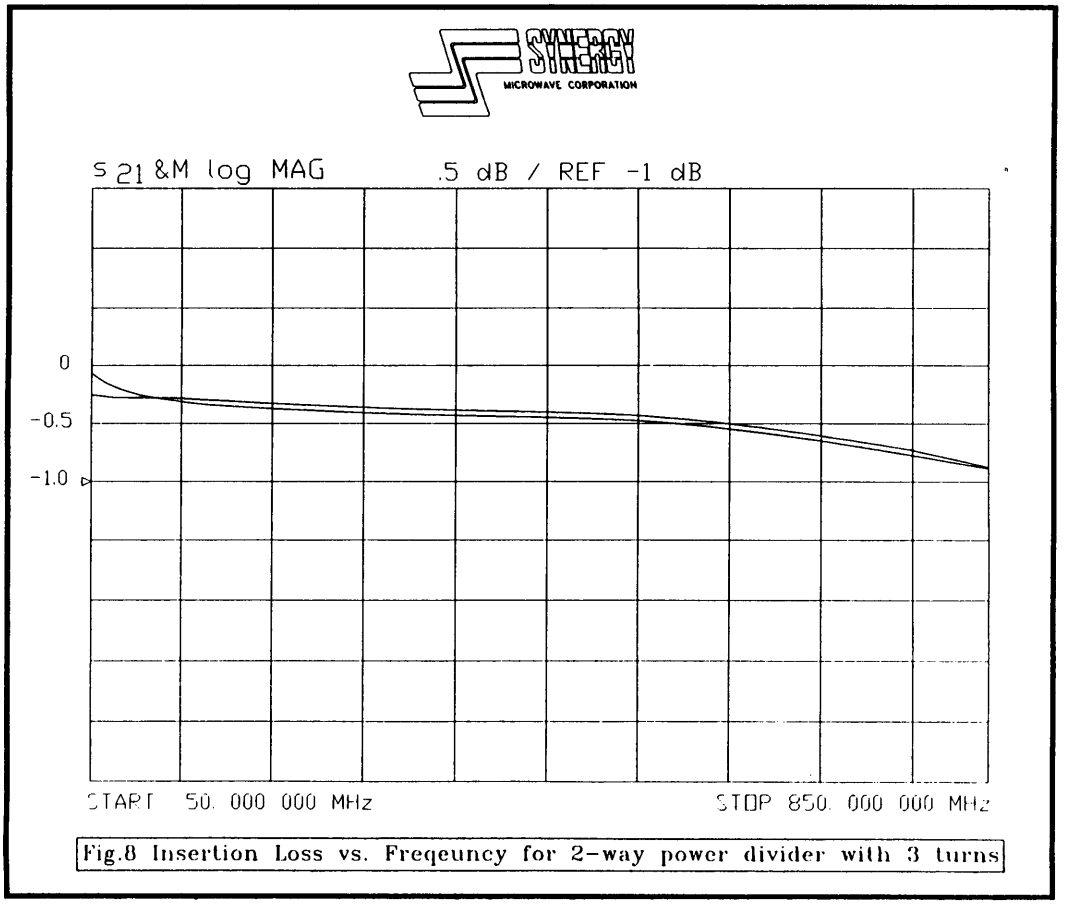


Fig.8 Insertion Loss vs. Freqeuncy for 2-way power divider with 3 turns

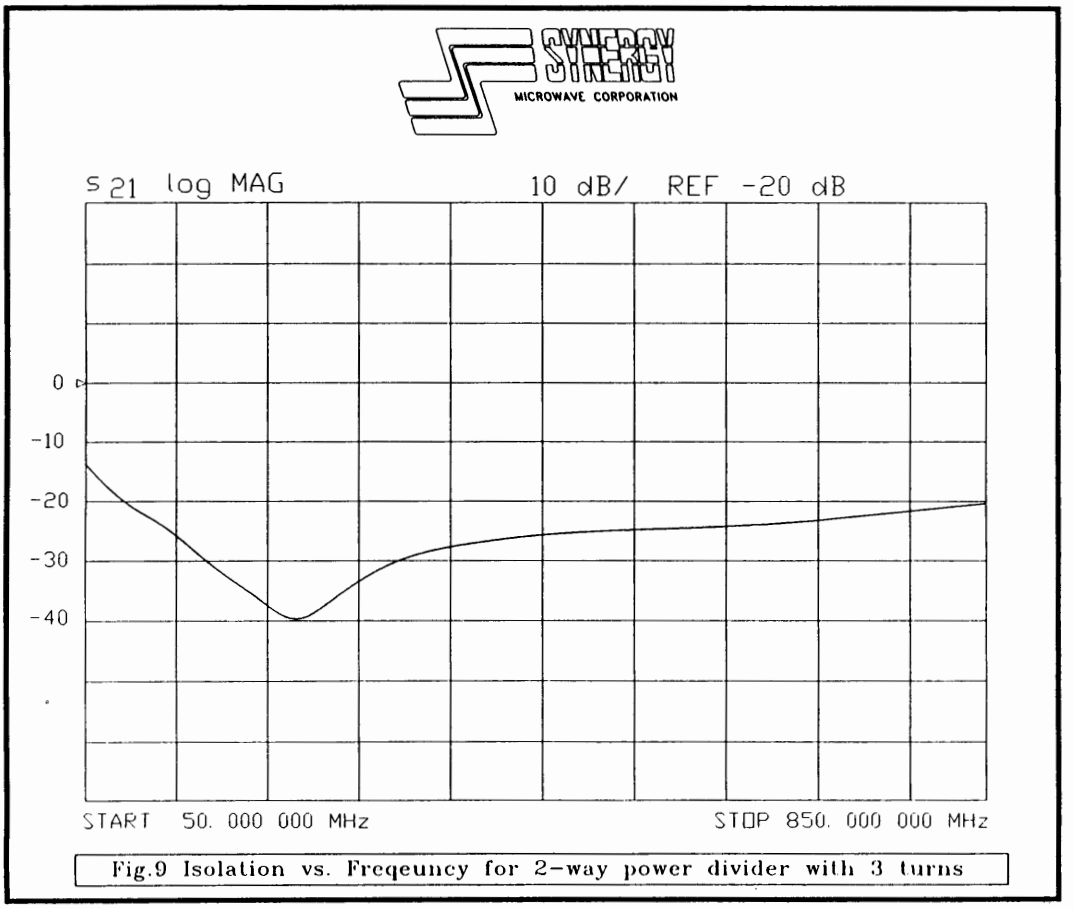


Fig.9 Isolation vs. Freqeuncy for 2-way power divider with 3 turns

FREQUENCY SYNTHESIZER STRATEGIES FOR WIRELESS

Bar-Giora Goldberg, MSEE
Henry Eisenson
Sciteq Electronics, Inc.
December, 1992

PURPOSE

This presentation was prepared to illustrate some of the challenges posed by emerging wireless/PCN/PCS industries (hereafter "wireless"), particularly as they apply to a key subsystem: the frequency synthesizer. Wireless creates a spectrum of opportunity and technical challenge, as well as risk, and since the frequency synthesizer is one of the most difficult developments in any analog system this document will seek to present some potential strategies for meeting those requirements.

Optimistically, the authors have written to two audiences. The first includes design and system engineers, who may be very competent at designing the RF systems of five years ago but with the advent of wireless are encountering new arrays of challenges based on economic, production engineering, and performance factors. The second target audience includes program managers and company executives, who may have limited technical knowledge yet must listen to the engineer's explanations as to why the strategies of yesterday simply don't work in this new technical and marketing environment.

DEFINITIONS

One of the problems facing many designers of systems and subsystems for the wireless businesses is a lack of structure. Operating bands, modulation schemes, protocols, power limitations, and – surprisingly – even applications, are all poorly defined. Firms developing systems and making investments in this new market, and particularly those who are aggressively working to establish a position early in the evolution of the industry, are very much at risk because of the lack of structure, protocols, spectrum allocations, and – of course – definitions. It is beyond the scope of this paper to attempt to generate such a set of data, however, so this statement is presented only as a warning to those investing money and engineering, and a plea to those involved in the establishment and standardization of protocols and definitions.

Regarding frequency synthesizers, for the purpose of this document historical definitions apply. Though they will not be listed in this paper, they correspond with those appearing in many publications.

INTRODUCTION

Radio systems are tuned by generating a frequency reference, and the quality of that reference determines the performance of the radio circuit. Accuracy is critical; both transmitters and receivers must be at the same frequency for communication to occur. When the energy of the signal appears only at the desired frequency, phase noise is considered perfect, and as that energy spreads to nearby frequency, phase noise is described as less perfect. A good reference generates no discrete uncommanded signals (spurs). Together, accuracy, phase noise and spurious signals define the performance of a reference.

By far, the best way to tune a radio or any RF system is with a crystal, and when multiple frequencies are necessary, multiple crystals and a switch can be used. Eventually, however, it becomes first impractical and then impossible to use complex arrays of crystals, as shown in Figure 1.

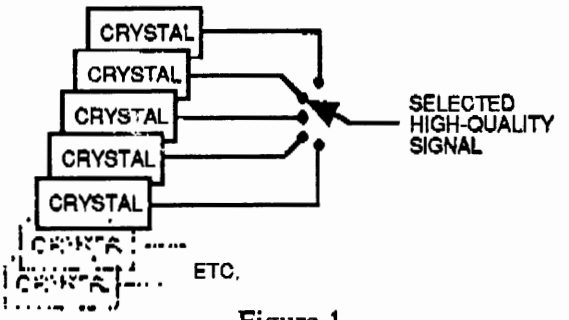


Figure 1

A "frequency synthesizer" is a device or circuit that synthesizes a new frequency based upon an original one (reference), retaining the stability, accuracy, and spectral purity of the reference though at a new point in the spectrum. It can generate one frequency (beyond that of the crystal reference) or multiple frequencies, as selected by a control mechanism (Figure 2).

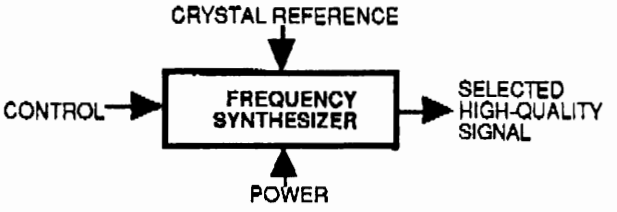


Figure 2

Like shoreline, spectrum is limited and precious, and the synthesizer (among other factors) determines how efficiently spectrum is used and how many channels can be compressed into any given operating band. Frequency synthesis is always a challenge, and the characteristics of the synthesizer have long defined the performance of the system that employs it.

Though there are as many synthesizer designs as there are designers, only three synthesizer techniques can be described as fundamental; all others are variations or combinations of one or more of them.

DIRECT-ANALOG

This (mix/filter/divide) is the oldest frequency synthesis method. The first time an engineer amplified a reference sufficiently to saturate a diode and used a filter to pick out a new frequency derived from the original, direct-analog was born. Today, many direct-analog techniques exist for multiplying, dividing, adding and subtracting an array of references, all locked to a common reference, to produce new frequencies.

This process supports very high spectral purity, since there is no correction circuit's "seeking" (that corrupts phase noise in a PLL), and careful planning can achieve frequency manipulation that avoids spurious signals. An important advantage of this technique is fast switching. The major drawback of direct-analog is the cost of the array of references required to cover the desired frequency range, plus the cost of one echelon of mix/filter/divide circuitry for each decade of resolution (step size) required.

Nevertheless, the finest synthesizer performance achieved by the industry employs direct-analog techniques, and appears in the Comstron FS-5000. Expensive, but there is no better method for generating a fast-switching, high spectral purity, broad bandwidth signal. Obviously, while this may be interesting to the designer of a simulator or radar system, the direct-analog approach is of little interest to a designer of wireless systems.

DDS

In one sense, the only true "synthesizer" is a DIRECT-DIGITAL SYNTHESIZER (DDS), since it literally constructs the waveform from the ground up (synthesizes the frequency) rather than combining or controlling existing oscillators.

A "vanilla" DDS appears in Figure 3, which also shows the signals generated by each circuit element.

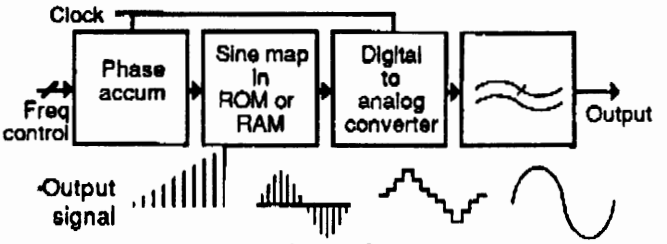


Figure 3

Though each of the blocks can be broken into many smaller ones (even down to the transistor level), the arrangement shown permits understanding of the means by which a DDS constructs a waveform.

The PHASE ACCUMULATOR correlates the clock with a control word, defining a "ramp" from 0° to 360° within some time period, and therefore the output frequency. A MEMORY maps the phase data in that ramp to a series of digital amplitude words, and a digital-to-analog converter DAC converts those digital data to an analog sinusoid (or any waveform stored in memory). That process must comply with sampled data rules, and therefore any frequency to be produced must be sampled *at least* twice each 360° (cycle), and the highest frequency that can be digitally generated is exactly one half the clock rate – though filter realities make the available output closer to 45%.

The DDS is also a supreme modulator. Digital shifting of frequency supports FM and toggling between two frequencies supports MSK/FSK; in fact, the DDS is a theoretically perfect FSK modulator. By placing an adder between the accumulator and the memory, the output can be shifted in time (phase), and a multiplier between the memory and the DAC permits scaling of the output, and therefore amplitude control. Both phase and amplitude modulation is therefore possible with a DDS, and with digital precision not possible with analog circuitry. Finally, SSB implemented using DDSs approaches theoretical perfection.

The advantages of the DDS include inexpensive high resolution (fine step size), fast switching speed, excellent phase noise, and while the signal is in the digital domain it can be manipulated/modulated with exceptional accuracy. The disadvantages include the fundamental limit of bandwidth (maximum frequency output is less than one half the clock rate, and logic has limits), and discrete spurious signals at a higher level than with other techniques. Nevertheless, in only twenty years the DDS has grown from an engineering novelty to a serious design tool.

There are many DDS products on the market today, and they're generally divided into two categories based upon a combination of price and performance. The "commodity DDS," typically in CMOS and from Analog Devices, Harris, Qualcomm, and Stanford Telecommunications, is characterized by low price, performance that is most often exploited as part of a much more complex synthesizer, and a high level of integration. Such DDS products often offer waveform manipulation capabilities, modulation, and other features sought by the wireless designer, but do not operate in the frequency ranges of most wireless systems.

High performance DDS products are often executed using very fast silicon or gallium arsenide logic so they can be clocked at a much higher rate than the commodity-level products. These DDS products cover a band much broader than that of the commodity DDSs. Expanded bandwidth requires higher clock rates, and therefore faster logic and more critical manufacturing and testing processes, hence higher prices. Even the fastest of the high performance DDSs operate only at about 400MHz, and that plus their relatively higher prices make the DDS unsuited to the needs of wireless systems.

While there are many specifications and architectures that differentiate one DDS from another, in general, a DDS can be characterized by a combination of bandwidth and spurious signals. By that simple standard, the state of today's DDS art will not meet the needs of wireless. The DDS should not be ignored by the wireless system designer, however, because as will be seen there are techniques by which the performance of the DDS can be translated to the frequency ranges of interest.

PLL

The PHASE LOCKED LOOP (PLL) is the single most commonly used synthesis technique, and is unquestionably the most flexible and adaptable. Perhaps more than ninety-nine percent of all synthesizers use one variant or another of the PLL. It appears in countless automobile radios and television sets, yet variants of the same architecture are used in exotic satellite transponders.

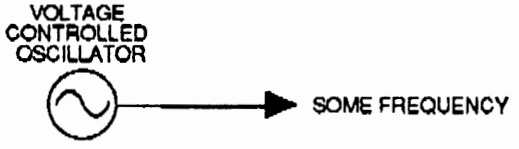


Figure 4

In Figure 4, a free-running oscillator generates a signal, the frequency of which varies (drifts) over time, according to circuit anomalies, temperature, etc.

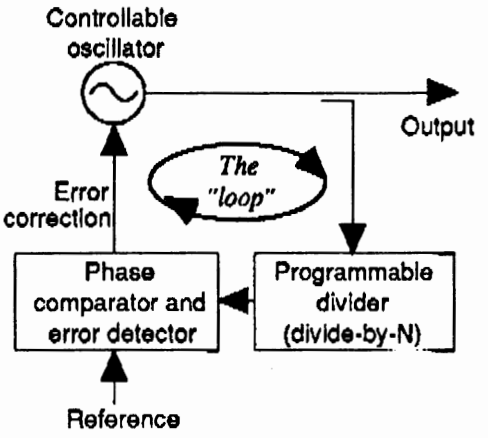


Figure 5

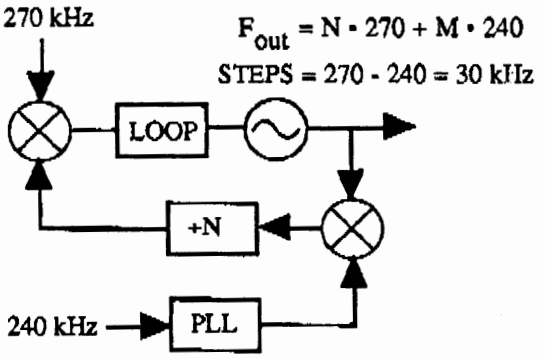
Figure 5 adds feedback and a phase detector, a correction mechanism that completes a loop to lock the output to some reference (thus "phase locked loop" or PLL), in accordance with some numeric ratio set by the frequency control command.

The PLL does not synthesize a waveform; rather, it controls the oscillator to the desired output frequency by dividing the output of the oscillator by some number, and then comparing the result with a reference. When errors are detected, they produce correction signals that return the oscillator to the correct operating frequency. For that reason, the system is always "seeking perfection," and the effectiveness of that seeking process determines the performance of the synthesizer. As that seeking occurs, the greater the deviation from the commanded frequency the worse the purity of the output signal. Such deviations are called "phase noise."

The advantages of PLL are low cost and excellent spurious suppression. The major disadvantage is that *both* fine steps *and* good phase noise can be achieved only in expensive implementations. In fact, the primary deficiency of PLL is that inverse relationship between step size and phase noise, because as step size decreases, division ratios in the system must increase, and the higher the division ratio the worse the phase noise within the loop bandwidth (close to the carrier). There is another drawback to PLL: switching speed. While the direct approach (DDS and direct analog) can be very fast, the PLL is slow because there is a certain electrical inertia involved before the system settles at a new frequency. The finer the required steps (the higher

the division ratio) the longer it takes a typical PLL design to reach a new commanded frequency.

Phase noise can be reduced by using two PLLs wherein a primary loop generates the required operating band but in coarse frequency steps, therefore with low division ratios and acceptable phase noise. A second loop, also doing coarse steps, is combined with the first to generate fine steps (a difference). See Figure 6.



TYPICAL TWO-LOOP SYNTHESIZER

Figure 6

Switching speed can be improved by generating a tuning signal to the VCO early in the change process. That's usually done by generating a digital change word, and converting it to an analog voltage applied to pre-tune the VCO. This approach can increase speed, but it also increases circuitry, cost, power dissipation, etc.

Another approach is to simply use two PLLs, with a switch to select between them. Assuming only that the system "knows" the next frequency, it can tune PLL-2 to that frequency while PLL-1 dwells at the prior frequency. When the time comes to change, a digital command switches to PLL-2. This obviously requires two PLLs, with twice the power, etc.

As can be seen, the PLL is a very useful technique, but a conventional single PLL cannot achieve aggressive combinations of fine steps, fast switching, and good phase noise.

COMBINATION DESIGNS

Many systems combine two or more of the basic techniques, and this approach is constantly being explored for wireless applications. To cover a limited band in fine steps, above the range of a DDS, the output of a DDS can be mixed with an LO and a filter used to select the desired sideband. In direct-analog systems, a PLL might be used to generate some of the required references. PLLs are often successfully combined with DDS to achieve fine frequency steps with reasonable phase noise. Ever more inventive combination designs appear every year, and some include elements of all three building blocks: PLL, DDS, and direct analog.

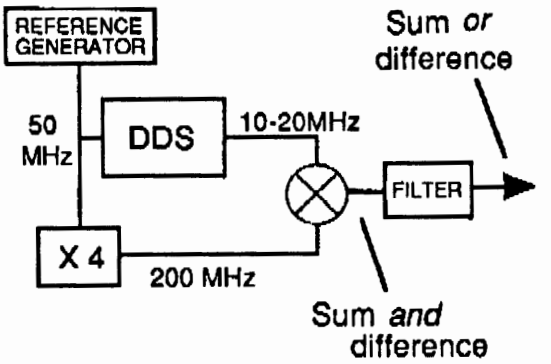
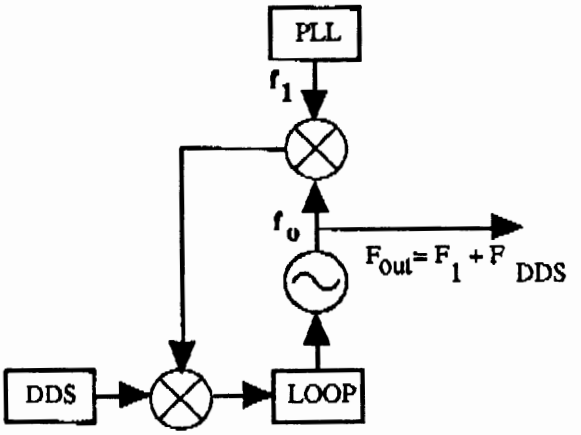


Figure 7

When a system concept dictates operation over a relatively narrow band but at a higher center frequency, a DDS can be upconverted to that range so as to exploit the DDS' fine steps, modulation capabilities, and fast switching. An example of such an architecture appears in Figure 7. In the example shown, 10 MHz of the DDS' output is translated or upconverted to the 200 MHz range. Obviously, the same architecture can be used to achieve a wide variety of goals, limited by DDS bandwidth and the physics of the filter.

It is sometimes useful to upconvert the DDS with a PLL, and, again, there are many ways to accomplish this. One mechanism (developed in 1984) uses a DDS as a reference to the phase detector of the PLL, though multiplication seriously degrades spurious performance.



TYPICAL DDS+PLL SYNTHESIZER

Figure 8

Another (also from that period) uses a DDS, a PLL, plus a combining loop. A typical DDS+PLL approach is shown in Figure 8. These techniques are useful, but involve cost and power compromises.

There are other interesting PLL mechanisms, which will be discussed as the needs of the emerging wireless market are analyzed.

GENERAL REQUIREMENTS OF WIRELESS SYSTEMS

The wireless industry will be filled with cell or base stations, of which each interacts wirelessly with dozens, hundreds, or even thousands of portable stations. The consumer purchases the wireless portable but the price of the cell/base radio is usually buried in service charges by the network owner. Also, because power, cost, and size are less important in immobile cell/base radios, this paper addresses only the requirements of portable systems.

It also considers only frequency-agile systems. The synthesizer for a typical wireless system (for instance a TDMA-based wireless PBX) will operate near 900 MHz with steps under 50 kHz, spectral purity that supports digital modulation, and power dissipation that ensures reasonable battery life. CDMA-based designs can trade frequency agility for complex coding circuitry, but TDMA, N-AMPS, AMPS, GSM, and most other cellular/PCS/PCN wireless systems require channel selection, hence agility.

Throughout wireless, once the basic function is accomplished price becomes paramount. Few engineers are experienced in designing products for the volumes involved in the wireless market. When millions of units will be made, savings of a few cents on each can have a profound effect upon the profitability of the enterprise. There is a spectrum of companies addressing every emerging opportunity in wireless, hence competition is fierce and will only grow tougher as the industry evolves. The relationship between price and performance, therefore, determines corporate success and failure.

Required performance is established by marketers who determine what the end user needs and wants, and what limits are acceptable. Once that information is collected and integrated, it is the engineer's task to achieve that performance at the lowest possible price. The most general assumption is that parts count will affect price, particularly when assembly effort is considered, and therefore the simplest (or more highly integrated) product will probably be lowest in cost and most competitive.

In wireless, reliability and durability are only barely behind price in relative importance. Historically, our industry has defined quality as either "military" or "commercial," and the assumption was that "military quality" produced the highest reliability. There are two reasons why production methodologies that define "military" quality won't work for wireless. Military quality standards require training programs, a wall full of diplomas, constant inspections, intensive testing, and reams of documentation. Like the ubiquitous pager, wireless products are measured only by the simplest standard of all; they must work nearly forever.

Generally, in the electronics industry, parts count and reliability are inversely related, and the more parts the more opportunities for manufacturing defects, so the simplest (or more highly integrated) product will be the most reliable.

Size is an issue because all wireless system developers are driven toward exceptional portability, and small size always complicates RF/analog design problems, involves higher levels of integration, and generally raises the cost of engineering the final product.

Some system architects have described requirements that include rapid settling. GSM (the European standard), for instance, establishes timing standards that dictate a fast switching solution. Designers of PBX and security systems have also asked for fast switching. A generic wireless synthesizer solution must, therefore, include the ability to switch at rapid rates. By extension, that seems to demand either multiple synthesizers with a selector and supporting software, or some implementation of a direct design.

"Wireless" implies exactly that, so not only is the communication by radio rather than coaxial cable, there are no extension cords and portable elements of the system run on batteries. Power consumption determines battery life, and one of the major engineering challenges of the wireless industry is efficiency of power utilization.

Marketing defines the needs of the end user and ensures that the product will have salable competitive advantages. The engineering group must develop a product that first attains those goals, but also costs little to make and works forever.

The needs of the wireless industry, in general, can best be met by simple, highly integrated, physically small, low-power designs. That is true in general,

and it is especially valid for the frequency synthesizer engine that drives the system.

FREQUENCY SYNTHESIS FOR WIRELESS

The frequency synthesizer subsystem of a wireless product does exactly the same job as a synthesizer does for any RF system. It is the system's tuning mechanism, and its performance determines the product's compliance with many marketing-driven requirements. Channel spacing determines step size, and in a PLL that establishes a mathematical relationship between operating band and division ratios that also dictates phase noise performance. Spurious signals can fool the system, lack of reliability can kill it, and excess cost makes everything else insignificant. This is valid for all RF systems and subsystems, including the synthesizer.

We've learned that the frequency synthesizer "menu" offers many alternatives from which the system designer can select, and we've also covered some of the needs of marketable wireless systems. Perhaps one valid method for identifying the best approach for wireless is to eliminate those techniques that will not work. The problem would be solved if a wireless portable end-user would pay for – and carry around – a Comstron FS-5000, or if the industry knew how to clock a cheap DDS at 2 GHz and still get good spurious suppression from the result. For reasons of cost, bandwidth, size, or spectral purity, therefore, pure-direct (analog or digital) synthesizers do not work for wireless.

What about a DDS upconverted using mix/filter circuitry – in other words, one of the "combination" designs? One advantage is the ability of the DDS to generate a modulated signal derived from digital manipulation of the waveform, and a second advantage is switching speed. At first glance, this approach looks inviting, but what are the disadvantages?

Make the estimate. Assume that the system demands 10 MHz bandwidth at a final operating frequency near 900 MHz. If reasonable filters are to be used, then there must be either two upconversions or substantial bandwidth in baseband. Two upconversions are expensive, since two good LOs must be generated and that greatly increases complexity.

For a single upconversion the required baseband coverage might be 50 MHz, which implies a clock rate for the logic near 110 MHz. Consider Figure 9, which illustrates the limitations imposed by filter issues.

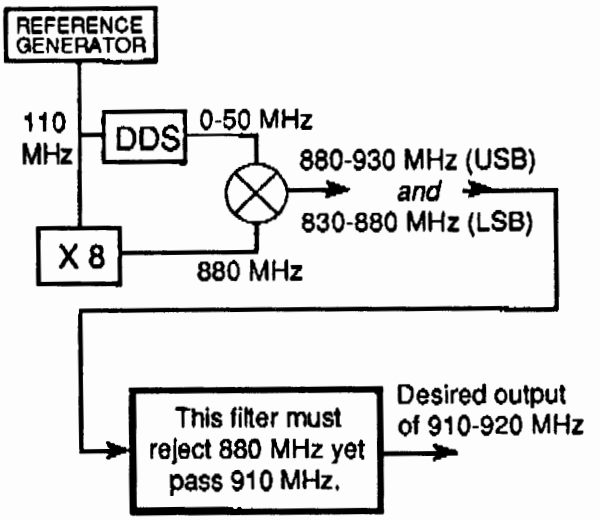


Figure 9

Depending upon the required suppression of the undesired sideband, the filter requirements shown are not impossible to meet. They are, however, difficult, very expensive, labor intensive, and impractical for inexpensive portable equipment.

Power is another issue that probably disqualifies the DDS. Even an advanced-technology, fractional-micron CMOS, fully integrated DDS will occupy a die of about 100 x 100 mils, and assuming a clock rate of 100 MHz the most optimistic dissipation estimate is 0.5W. Wireless portables will probably use a tenth of that for the entire design, hence the likely disqualification of DDSs using today's technology.

For these reasons, neither two conversions nor a 100 MHz DDS clock rate are practical. The designer must look beyond the direct approach. That leaves indirect, or PLL, which works for nearly all RF applications throughout the electronics industry.

In today's wireless, synthesizers are almost all PLL and use either one or two loops. Both have been implemented with very high levels of integration, and single chip PLL ASICs are available at $5 or less, with operation from 6-15 mA. These devices include all functions and require only an external VCO plus a few discrete devices for the loop filter.

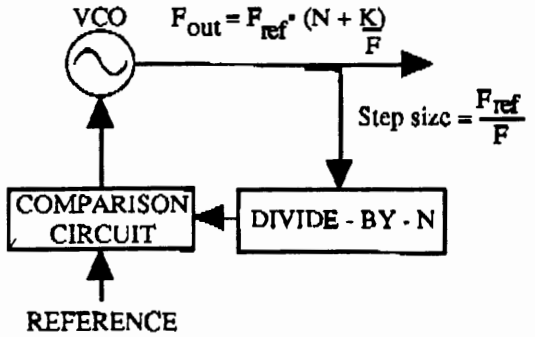
The single loop iteration of such a design is simple, economical, reliable, and small, but it does not meet the requirements of digital modulation techniques.

For many years, a broad variety of simple single loop synthesizers have used inexpensive PLL chips by Fujitsu, Plessey, Motorola, etc. to meet the requirement of early wireless, including FM/analog cellular. Close channel spacing of agile wireless requires fine tuning steps and therefore high division ratios, yet digital modulation demands phase noise better than conventional PLL architectures can achieve.

Designers have therefore used two loops to achieve the combination of phase noise and step size needed by digital modulation schemes, which means two synthesizers with two VCOs, etc., and all the baggage a double circuit implies. The two-loop solution therefore implies higher power, complexity, cost, and likelihood of failure – everything the successful wireless system designer was directed to avoid. Nevertheless, state of the PLL art for wireless has been two loops,which achieve the required phase noise. In some systems, the requirement is for two such assemblies with a switch, to support fast switching. That's four loops, with four VCOs and associated circuitry; it's expensive, large, power hungry, and in general is an array of compromises.

FRACTIONAL *N*

There's a relatively little-known derivative of PLL that can address many such requirements with only one loop; it's called fractional *n*. Though mysterious to many engineers, it is not a true innovation because some fractional designs have been used for years. Fractional *n* synthesis can best be understood by examining the conventional block diagram for a PLL, but with one twist. The divide-by-N circuit appears where it always has, but additional circuitry changes the *value* of N from an integer to some fraction. Consider the impact, as suggested by Figure 10.



Conventional PLL: N is an integer
Fractional: N can be a fraction

Figure 10

N is programmable, of course, to define the relationship between the output and the reference. Suppose the requirement is to operate at about 1 GHz in 30 kHz steps. In conventional PLL designs, the output (1000 MHz) is divided by 33,000 to reach a value that can be compared to the reference (30 kHz), and that division imposes a phase noise degradation of 20 log *N*, or 90 dB. That degradation can be cut by 20 dB with a good fractional design, and there are several ways to achieve the desired result. Fractional division can be used to *increase* the reference by an order of magnitude, or to *reduce* the division ratios, and in any case the effect is to reduce the division ratio for a given combination of output frequency and step size, thus improving phase noise.

Fractional at first appears to be an aspirin for all forms of PLL headaches, but that hasn't been the case. Conventional implementations of fractional require major increases in circuitry, and that implies increased power dissipation, parts count, complexity, labor costs, and therefore overall costs – again, all the things the designer was told to avoid.

Naturally, fractional division generates a new periodicity within the divide-by-N circuitry, and therefore introduces spurious signals. For the above example, if the reference goes from 30 to 300 kHz, for 30 kHz steps there will be 30kHz/60/90...etc. spurs in addition to the 300 kHz spurs. Those spurs are at the frequency of the new periodicity or its harmonics, but in either case they can produce a major degradation of spurious suppression. In a way, fractional has been largely ignored because those who have experimented with it consider the improvement in phase noise to be virtually a trade off for spurs.

Yet another problem with fractional is that the fractionality of conventional circuits is fixed, hence a given design has little flexibility and new applications imply new designs. For these and allied reasons, fractional *n* synthesis has been largely ignored. This situation is about to change, as market factors drive engineering to examine every alternative.

An important derivative of fractional is Sciteq's Arithmetically Locked Loop (ALL), which combines aggressive digital signal processing (DSP) with fractional to overcome all of the disadvantages outlined above. ALL is a simple – and patented – design that increases overall gate count (compared, for instance, to the Fujitsu or Plessey PLL chips) by about 3%, so complexity is not an obstacle. The effect of the new periodicity is minimized, hence spurious signal level is also not an obstacle. Finally,

spurious signal level is also not an obstacle. Finally, fractionality is programmable, making one design suitable to a spectrum of applications.

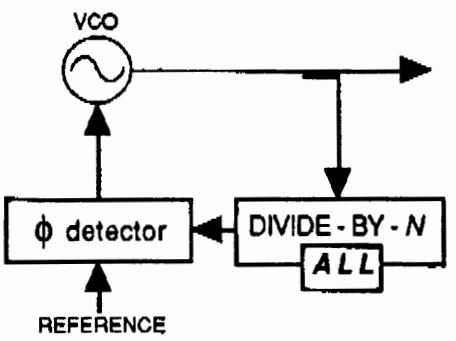


Figure 11

Adding ALL to a synthesizer design is simple, as implied by Figure 11. There is no change to the existing design except for I/Os in the divider circuit; the ALL block adds simple DSP that does the actual job of managing the division process and reducing the required ratios.

ALL APPLICATIONS IN WIRELESS

The ALL can operate over all wireless segments of the spectrum up to C-band. Comparisons are best made by examining any of the standard single-chip solutions (Fujitsu, National Semiconductor, Plessey, etc.) and adding about 3% in gate count and power **while reducing close-in phase noise by about 20 dB.**

That performance level support digital modulation scenarios with a single loop. Even close-in, phase noise is competitive with levels ordinarily achieved using two loop designs.

Frequency switching is far faster than conventional PLL designs, even without pretuning, since the reference frequency can be much higher for a given step size.

ALL has been in full production for two years, executed with discrete components to build modular synthesizer products. These designs have been very successful, and constitute one of Sciteq's most important product line. Potential users can today support system development using prototypes built with discrete devices, in the expectation that a fully integrated solution will be available during summer 1993.

Now that the U. S. Patent Office has allowed Sciteq's patent, a full-custom chip development contract has been let to a U. S. semiconductor firm. Because the design is based on existing hardware (that uses discrete devices), risk is viewed as low.

The new low-power Sciteq design has a 2.5 GHz front end, integrated dual modulus, integrated ALL, low spurious levels, and programmable fractionality. It is suitable to all wireless applications, as well as other systems where competitive posture requires new levels of cost-effectiveness. Projected cost of the new single-loop integrated synthesizer, designated the SCX-180, is under $10 in commercial quantities.

Some derivative of ALL will be used in many future cellular and other wireless products requiring agility, so Sciteq invites inquiries from system developers, who are invited to contact Sciteq in San Diego, at 619-292-0500.

A 2.4GHz Single Chip Transceiver

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Introduction

The Industrial, Scientific and Medical (ISM) frequency band includes the frequency range 2.4 - 2.5GHz. In the USA, unlicensed operation using spread spectrum modulation at transmitter powers of 1W is permitted over this band. This paper describes a transmit/receive front end for a 2.4GHz wireless communications transceiver, the entire circuit of which has been integrated onto a single GaAs Microwave Monolithic Integrated Circuit (MMIC). A photograph of the 3.3mm x 5.2mm chip, which is available in an SSOP28 style plastic package, is shown in figure 1. Low receive current of 30mA from a +5V supply and a standby current of less than 0.5mA, make this an ideal component for battery powered operation.

Transceiver Architecture

A block diagram of the complete transceiver is shown in figure 2. The circuit can be switched between receive, transmit and standby states. In receive mode, input signals are down converted to differential IF signals. Although designed specifically for the 2.4-2.5GHz band, RF signals between 1.9GHz and 2.6GHz could be utilised. The off chip filters can be selected to suit the band of interest.

In transmit mode, the IF input signal, either balanced or single ended, is between 200MHz and 500MHz. The IF input is up converted to a single ended signal at the RF frequency. The circuit has been designed to provide a constant output power for a wide range of IF signal levels. A switched attenuator has been included to allow a 10dB step in the output power level.

The frequency of the VCO, and hence the IF frequency, is selected by appropriate choice of an off-chip resonator. Local oscillator frequencies of between 1.4GHz and 2.7GHz are available. A diversity switch has also been included to allow antenna selection. DC supply to the chip is +5V and -5V, with complementary 0V/-5V switching. The -5V supply takes less then 0.5mA of current, regardless of transceiver operating mode. Typical current requirements from the +5V supply are 30mA in receive mode and 220mA in transmit mode. A standby state is also available and requires a current of less than 0.5mA.

In addition to the complete transceiver chip, all of the sub-circuits have been manufactured as individually measurable components. The design and measured performance of these subcircuits is described below. The circuits were realised on the standard GMMT F20 GaAs MMIC process.

Sub-Circuit Design and Measurements

LNA

The Low Noise Amplifier (LNA) is a two stage design with series inductive feedback to allow good noise figure performance with a well matched input[1]. A stacked bias arrangement is used to help reduce current consumption. Instead of biasing the drain of each FET at +5V and the source at 0V, the arrangement shown in figure 3 is used. This allows the +5V to be shared between the FETs and the current to be re-used.

The RF On Wafer (RFOW) measured s-parameters of a typical LNA are shown in figure 4. Gain is 17.5dB $\pm$0.5dB from 2 - 3GHz. The input match is better than 15dB and the output match is better than 13dB. Measured noise figure is 2.5dB at 2.4GHz. Total current consumption is 6mA from a +5V supply.

Switches

T/R and diversity switches all use simple series mounted FETs[2]. The FETs are biased at zero volts DC and the control signal is applied to the gates. One common design of Single Pole Double Throw (SPDT) switch is used throughout. The measured "on" case insertion loss is typically 0.7dB with an "off" case isolation of 20dB.

Mixers

A quad ring of zero biased FETs is used to realise a balanced conductance mixer[3]. When driven with differential inputs, excellent balance is achieved with a conversion loss of 6dB.

VCO

A Clapp type Voltage Controlled Oscillator (VCO) is used[4]. The oscillation frequency can be set between 1.4GHz and 2.7GHz by an external resonator. For operation with an IF of, say 250 MHz, the nominal LO frequency is 2.15GHz. An on chip inductor/capacitor combination was included on the sub-circuit, for use as an alternative to the off-chip coaxial resonator. This allows testing of the oscillator on wafer. Figure 5 shows the output power and tuning voltage versus oscillation frequency. Output power varies by less than $\pm$0.2dB across the tuning range.

VCO Balun

A common gate stage and a common source stage of amplification are used to provide an equal amplitude split with 180° phase difference[5]. The inputs of each stage are common and the two outputs are used to provide the differential drive to the balanced mixer. Figure 6 shows the RFOW measured s-parameters of a typical device and figure 7 shows the insertion phase between the input and each of the two outputs. A gain of 1dB at 2.1GHz and terminal matches of better than 20dB are achieved. The amplitude difference is only 0.15dB and the phase difference is 186°. Stacked bias has been used to allow operation with only 6mA of current from a +5V supply.

RF Balun

The RF balun is very similar to the LO balun but at a slightly higher frequency. The RFOW measured s-parameters are shown in figure 8 and the insertion phases in figure 9. A gain of 1dB with terminal matches of better than 20dB is achieved at 2.4GHz. Amplitude difference between the outputs is 0.45dB and the phase difference is 189°.

Buffer Amplifier

The buffer amplifier is used to provide a low level VCO output for phase locking of the LO. It must present minimal loading to the VCO, provide high isolation and be able to operate into any load from 50Ω to an open circuit. This has been achieved by using a small single finger FET, biased through a 50Ω resistor in the drain. Figure 10 shows the measured s-parameters of a typical amplifier. S11 is close to unity, which is indicative of the high input impedance presented to the VCO. The reverse isolation is more than 40dB at 2.4GHz and the output match is better than 14dB. An insertion loss through the buffer of 12.5dB ensures the required low level of output power is delivered. Current consumption of this component is only 1.5mA.

Differential Amplifier

With the chip in transmit mode, the IF input is into a differential amplifier[6,7]. A long-tailed pair at the input of the amplifier allows single ended or balanced input. Each of the differential outputs from this first stage is then amplified by identical common source stages of amplification. Active biasing is used throughout in order to minimise chip area. The differential input impedance to the circuit is 800Ω. When driven with differential signals from a source of the same impedance, the gain of the amplifier is 20dB over a frequency range of 200MHz to 500MHz.

Pre-amplifier

The output of the transmit mixer is amplified by the pre-amplifier prior to passing off chip, through the transmit filter and into the power amplifier. A low level of gain is required to balance the gain budget through the transmit chain. The input to the pre-amp is resistivity matched with reactive matching at the output. Figure 11 shows the measured s-parameters of a typical pre-amp. The amplifier exhibits a flat 5dB of gain from 2 - 3GHz. Input return loss is greater than 12dB and output return loss is greater than 17dB.

Power Amplifier

A two stage power amplifier is used to increase the level of the transmit signal[4]. Figure 12 shows the small signal s-parameters of the amplifier. The gain is 23dB at 2.4GHz with input and output return losses of greater than 13dB.

Switched Attenuator

A 10dB switched resistive attenuator[8] is positioned before the common T/R output, in the transmit path. This allows the output power level to be switched by 10dB. The small signal gain through the power amplifier, attenuator and T/R switch on the complete transceiver chip has been measured with the attenuator in both states. Figure 13 is a plot of this and the 10dB gain difference shows the accuracy of the switched attenuator. Because the attenuator is positioned after the power amplifier this gives an accurate 10dB step in output power level, regardless of amplifier compression.

Transceiver Measurements

Measurements have been made on the complete transceiver chip. These were made on an unpackaged device in a purpose built jig. A spectral plot of the buffer amplifier output is shown in figure 14. The output power level is -12dBm with a phase noise of -122dBc/Hz at 1MHz off carrier. This signal is used to drive the phased lock loop of the transmit/receive circuit.

Figure 15 shows the measured receiver conversion gain and double sideband noise figure versus IF frequency. This is for a fixed LO frequency of 2.035GHz with the IF varying from

50MHz to 500MHz. The slight roll off with increasing IF frequency is a result of on chip IF path losses and the off chip balun used to combine the differential IF signals developed by the chip.

The power transfer characteristic through the power amplifier, attenuator and T/R switch chain has been measured and is shown in figure 16. A 1dB compression point of +18.5dBm with a saturated output power capability of +21dBm is demonstrated. Figure 17 shows the gain versus IF frequency through the entire transmit chain from differential IF input to T/R common port output. This is also measured with the LO frequency fixed at 2.035GHz and shows a gain of 38dB $\pm$1dB for IF frequencies between 200MHz and 500MHz.

Conclusions

A single chip GaAs transceiver to cover the 2.4 - 2.48GHz ISM band has been described. Receive gain is 13dB with differential IF outputs and a double sideband noise figure of 4dB. Current consumption in receive mode is just 30mA from a +5V supply. A standby mode is available with a current consumption of less than 0.5mA. Transmit mode offers a constant output power level switchable by 10dB, for a large range of IF input levels. These features combine to give a component which is ideally suited to spread spectrum Wireless LAN applications.

Acknowledgements

Numerous staff at GEC-Marconi Materials Technology have helped with the development of this chip, the authors would like to thank all concerned and in particular: Arthur Bradley, Rod Conlon, Ian Davies, Alistair Frier, Mike Geen and Barry Roberts.

References

1. Murphy, M.T., "Applying the Series Feedback Technique to LNA Design", Microwave Journal, November 1989, pp 143 - 152.

2. Ayasli, Y., "Microwave Switching With GaAs FETs", Microwave Journal, November 1982, pp 61 - 74.

3. Boulouard, A., "Simple Analysis Method Simulates Switching Mixers", Microwaves & RF, June 1989, pp 103 - 107.

4. Vendelin, G.D., Pavio, A.M. and Rohde, U.L., "Microwave Circuit Design", John Wiley & Sons, Inc 1990.

5. Hiraoka, T.et al, "A Miniaturized Broad-Band MMIC Frequency Doubler", IEEE Transactions On Microwave Theory and Techniques, Vol 38 No 12, December 1990, pp 1932 - 1936.

6. Gray, P.R and Meyer, R.G. "Analysis and Design of Analog Integral Circuits", Second Edition, John Wiley & Sons, Inc 1984.

7. Robertson, I.D and Aghvami, A.H "Ultrawideband Biasing of MMIC Disturbed Amplifiers Using Improved Active Load", Electronics Letters Vol 27, No 21, 10th October 1991, pp 1907 - 1909

8. Clifton J.C and Arnold J., "Digitally Controlled GaAs MMIC Attenuator For Active Phase Arrays", Proceedings of the 22nd European Microwave Conference 1992, Vol 1, pp 231 - 235.

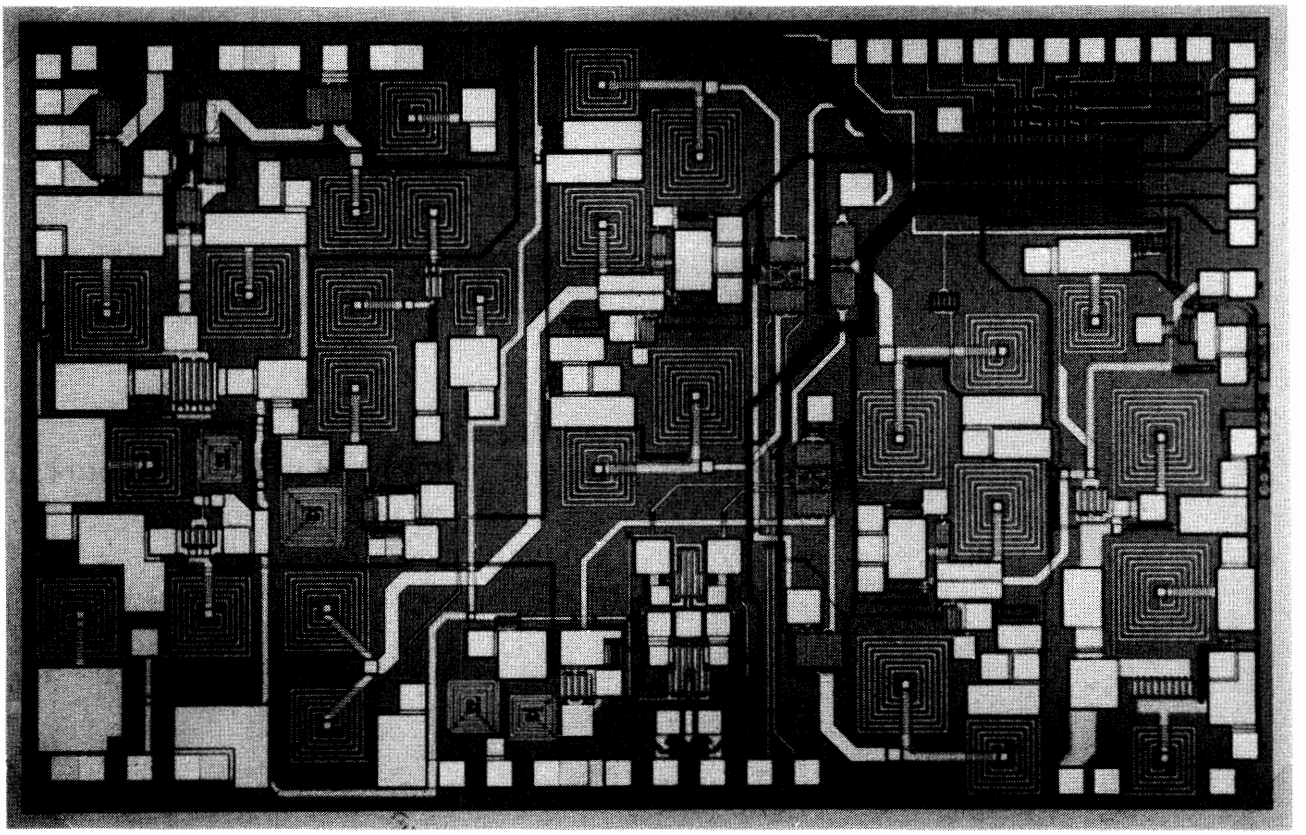


Figure 1 Photograph Of The Transceiver MMIC

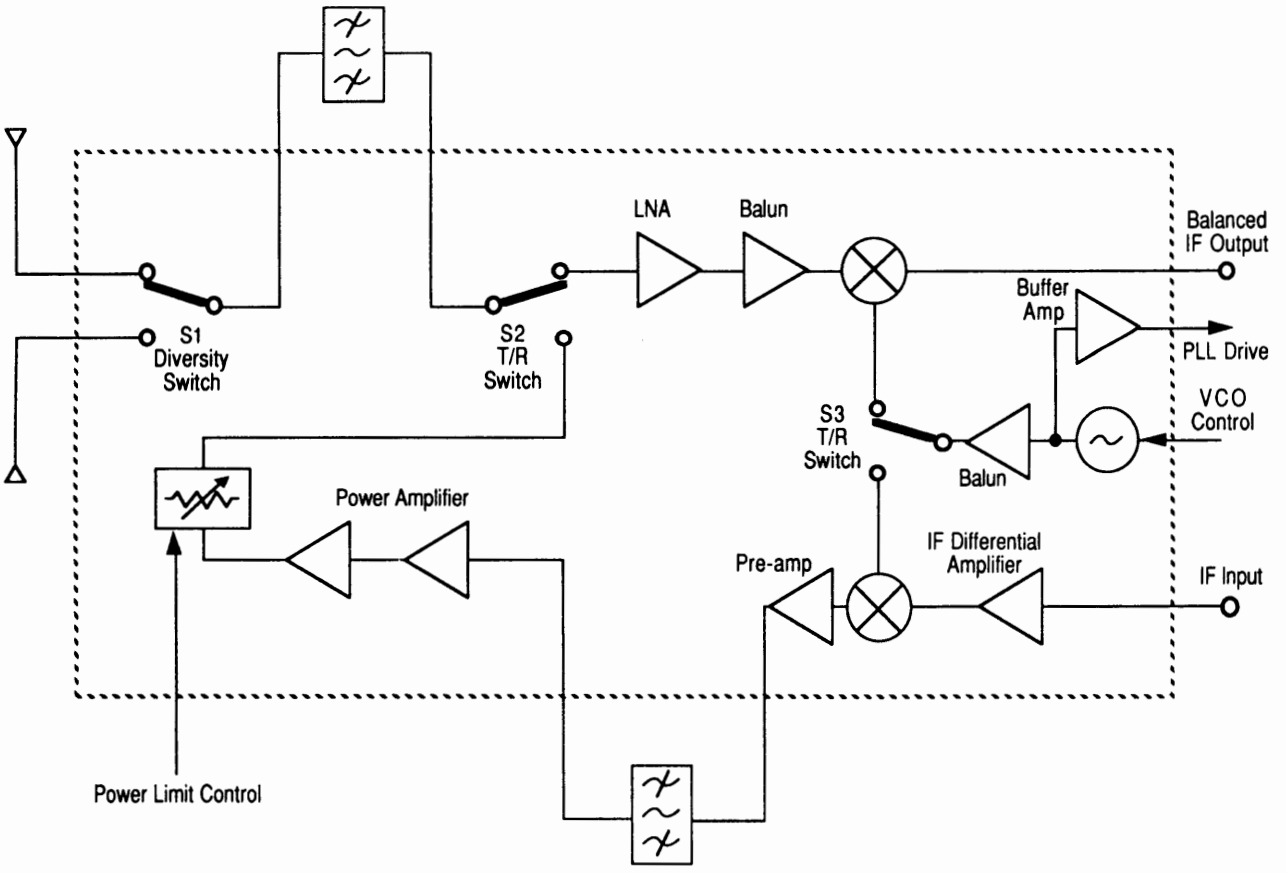


Figure 2 Block Diagram Of The Transceiver

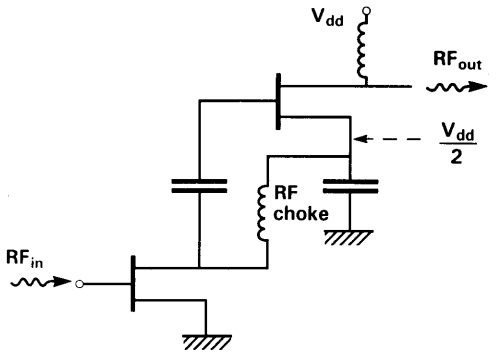


Figure 3 Stacked Biasing Arrangement

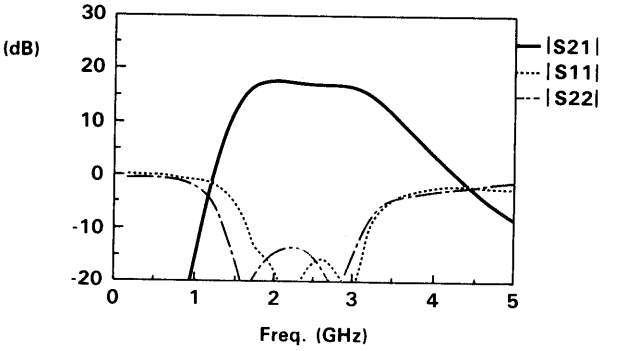


Figure 4 RFOW Measured Performance Of the LNA

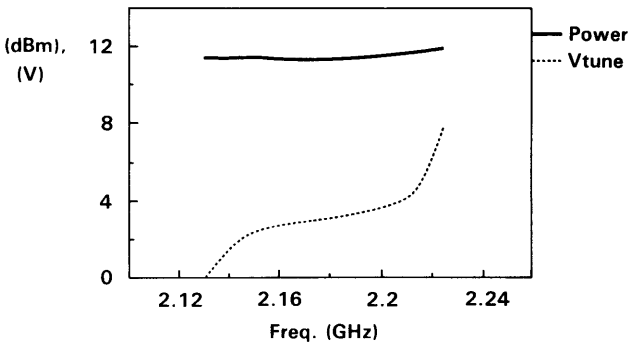


Figure 5 RFOW Measured Performance Of The VCO

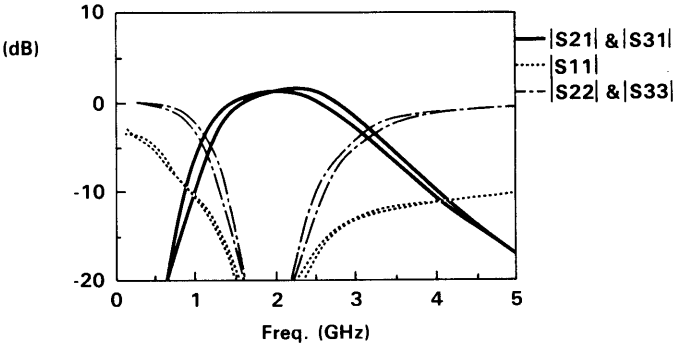


Figure 6 RFOW Measured Performance Of The VCO Balun

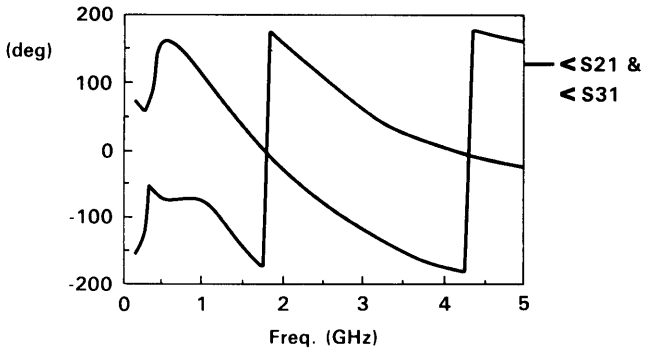


Figure 7 RFOW Measured Performance Of The VCO Balun

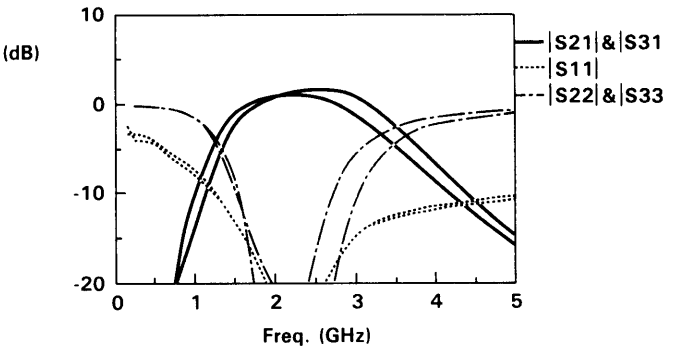


Figure 8 RFOW Measured Performance Of The RF Balun

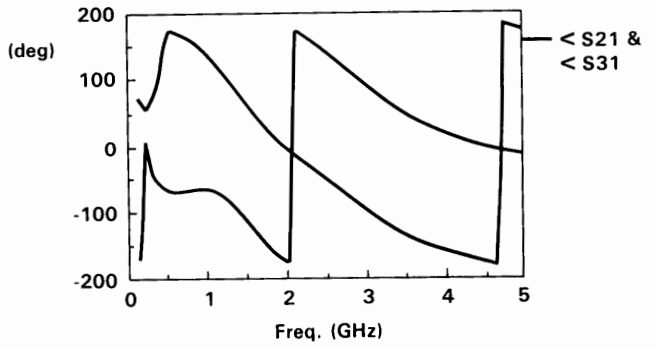


Figure 9 RFOW Measured Performance Of The RF Balun

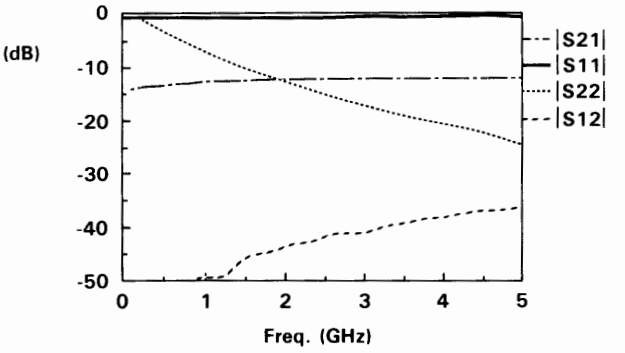


Figure 10 RFOW Measured Performance Of The Buffer Amplifier

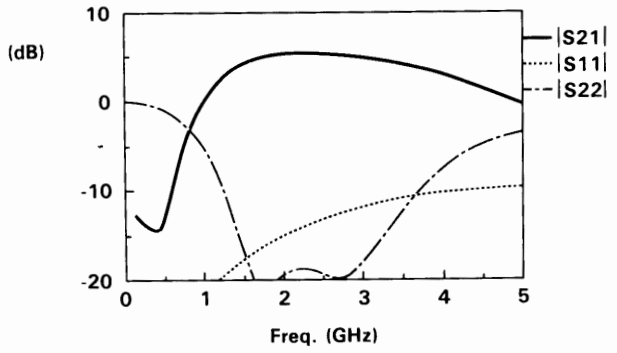


Figure 11 RFOW Measured Performance Of The Pre-Amplifier

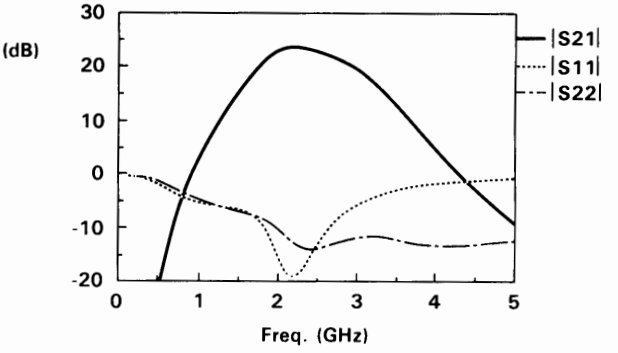


Figure 12 RFOW Measured s-parameters Of The Power Amplifier

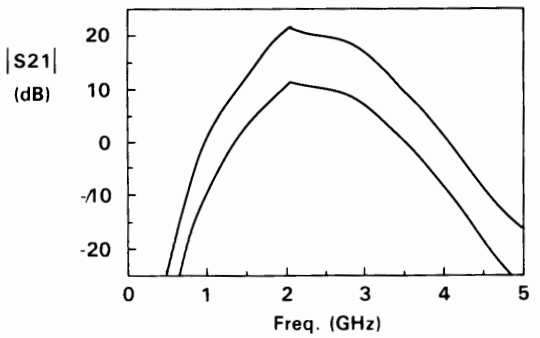


Figure 13 Measured Gain Through The Power Amplifier, Attenuator and T/R Switch Chain. Two States.

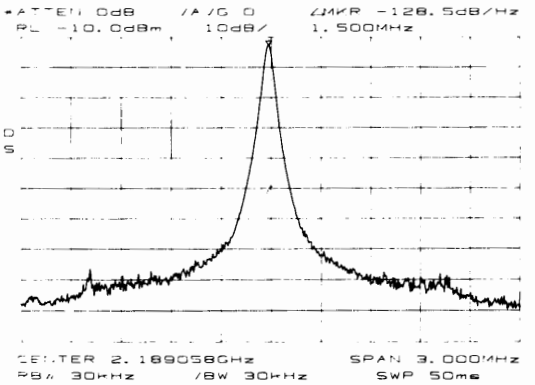


Figure 14 Spectral Output From The Buffer Amplifier

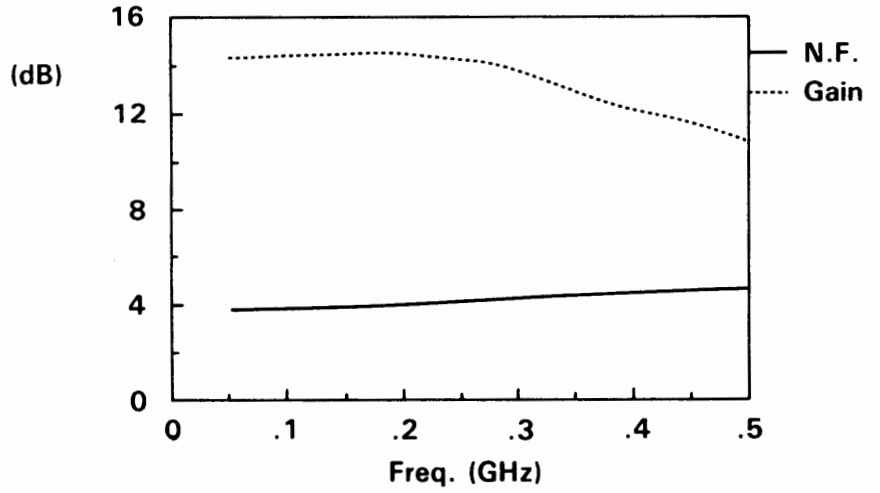


Figure 15 Measured Receive Gain And Noise Figure

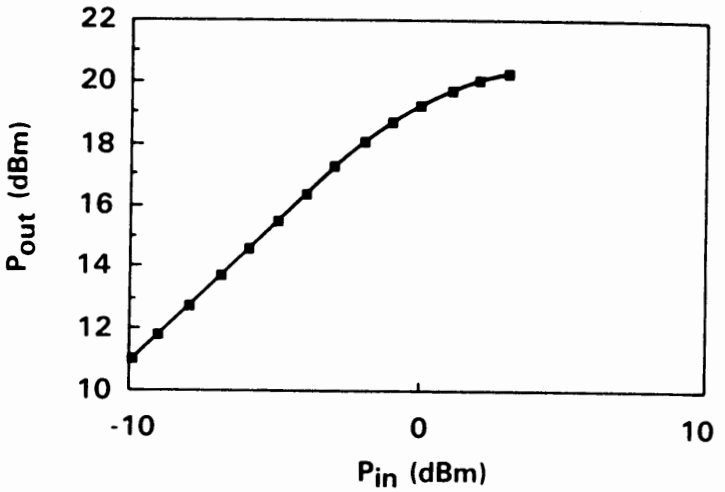


Figure 16 Measured Power Transfer Through The Power Amplifier, Attenuator And T/R Switch Chain

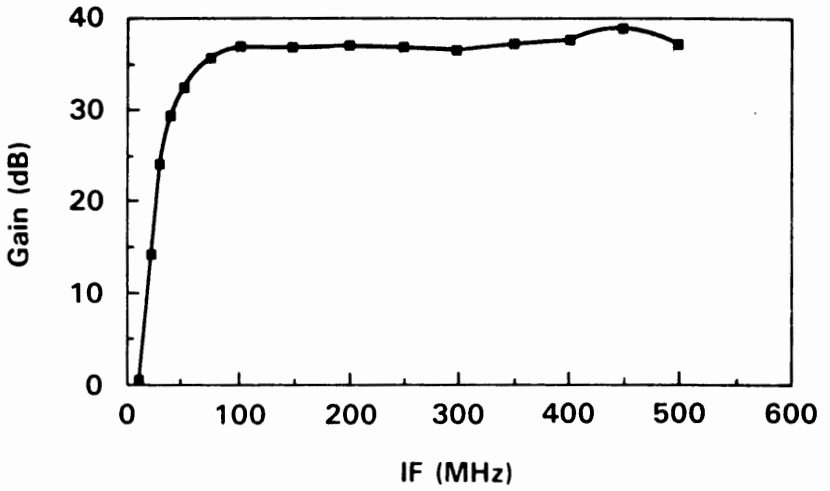


Figure 17 Transmit Up-Converter Gain Versus Intermediate Frequency

Wireless Data and Personal Communications

Session Chairperson: Jack Browne,
Microwaves & RF (Hasbrouck Heights, NJ)

Demodulating at 10.7MHz IF with the NE/SA605/625 AN1996

Author: Alvin K. Wong

INTRODUCTION

The need for high speed communications is increasing in the market place. To meet these needs, high performance receivers must demodulate at higher IF frequencies to accommodate for the wider deviations in FM systems.

The standard 455kHz IF frequency, which is easier to work with, and thus more forgiving in production, no longer satisfies the high speed communication market. The next higher standard IF frequency is 10.7MHz. This frequency offers more potential bandwidth than 455kHz, allowing for faster communications.

Since the wavelength at 10.7MHz is much smaller than 455kHz, the demand for a good RF layout and good RF techniques increases. These demands aid in preventing regeneration from occuring in the IF section of the receiver. This application note will discuss some of the RF techniques used to obtain a stable receiver and reveal the excellent performance achieved in the lab.

BACKGROUND

If a designer is working with the NE/SA605 for the first time, it is highly recommended that he/she reads AN1994 and AN1995.

These two application notes discuss the NE/SA605 in great detail and provide a good starting point in designing with the chip.

Before starting a design, it is also important to choose the correct part. Philips Semiconductors offers an extensive receiver line to meet the growing demands of the wireless market. Table 2 (see end of app note) displays the different types of receivers and their key features. With the aid of this chart, a designer will get a good idea for choosing a chip that best fits their design needs.

If low voltage receiver parts are required in a design, a designer can choose between a NE/SA606, SA607, SA608, or SA626. All of these low voltage receivers are designed to operate at 3V while still providing high performance to meet the specifications for cellular radio. All of these parts can operate with an IF frequency as high as 2MHz. However, the SA626 can operate with a standard IF frequency of 10.7MHz and also provide fast RSSI speed. Additionally the SA626 has a power down mode to conserve battery power.

A close look at Table 2 will also show that there are subtle differences between the 3V receivers. The main differences between the NE/SA606, SA607, and SA608 can be seen in the audio and RSSI output structure. Additionally the SA607 and SA608 provide a frequency check pin which can aid in locking in the desired received frequency over temperature.

OBJECTIVE

The objective of this application note is to show that the NE/SA605 can perform well at an IF frequency of 10.7MHz. Since most Philips Semiconductors receiver demo-boards are characterized at RF = 45MHz/IF = 455kHz, we decided to continue to characterize at this frequency. This way we could compare how much degradation (for different IFs) there was with a RF = 45MHz/IF = 455kHz vs RF = 45MHz/ IF = 10.7MHz. As we will discuss later, there was minimal degradation in performance.

We also tested at RF = 240MHz/IF = 10.7MHz. The 240MHz RF is sometimes referred to as the first IF for double conversion receivers. Testing the board at RF=83.16MHz (which is also a common first IF for analog cellular radio) and IF = 10.7MHz was not done because the conversion gain and noise figure does not change that much compared to 45MHz input. Therefore, we can probably expect the same type of performance at 83.16MHz.

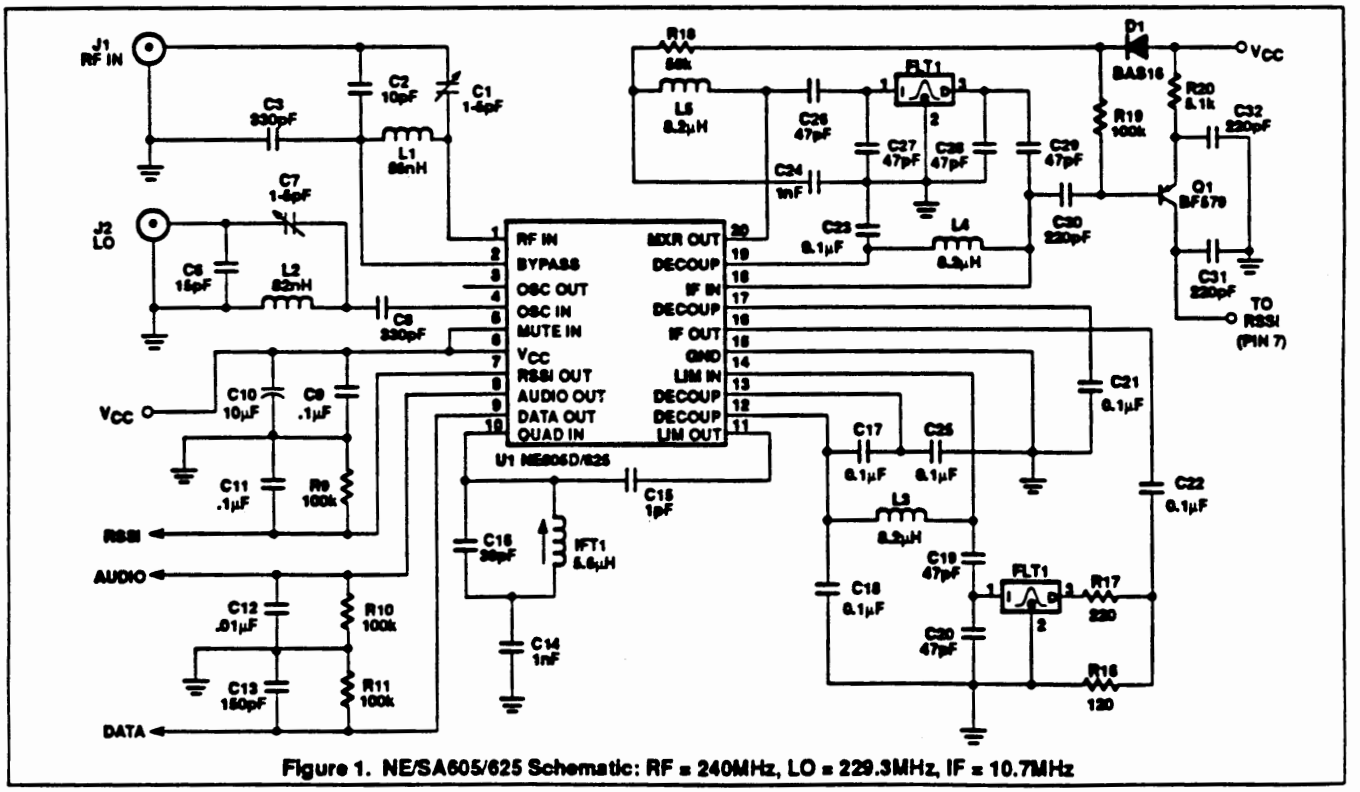


Figure 1. NE/SA605/625 Schematic: RF = 240MHz, LO = 229.3MHz, IF = 10.7MHz

Demodulating at 10.7MHz IF with the NE/SA605/625

AN1996

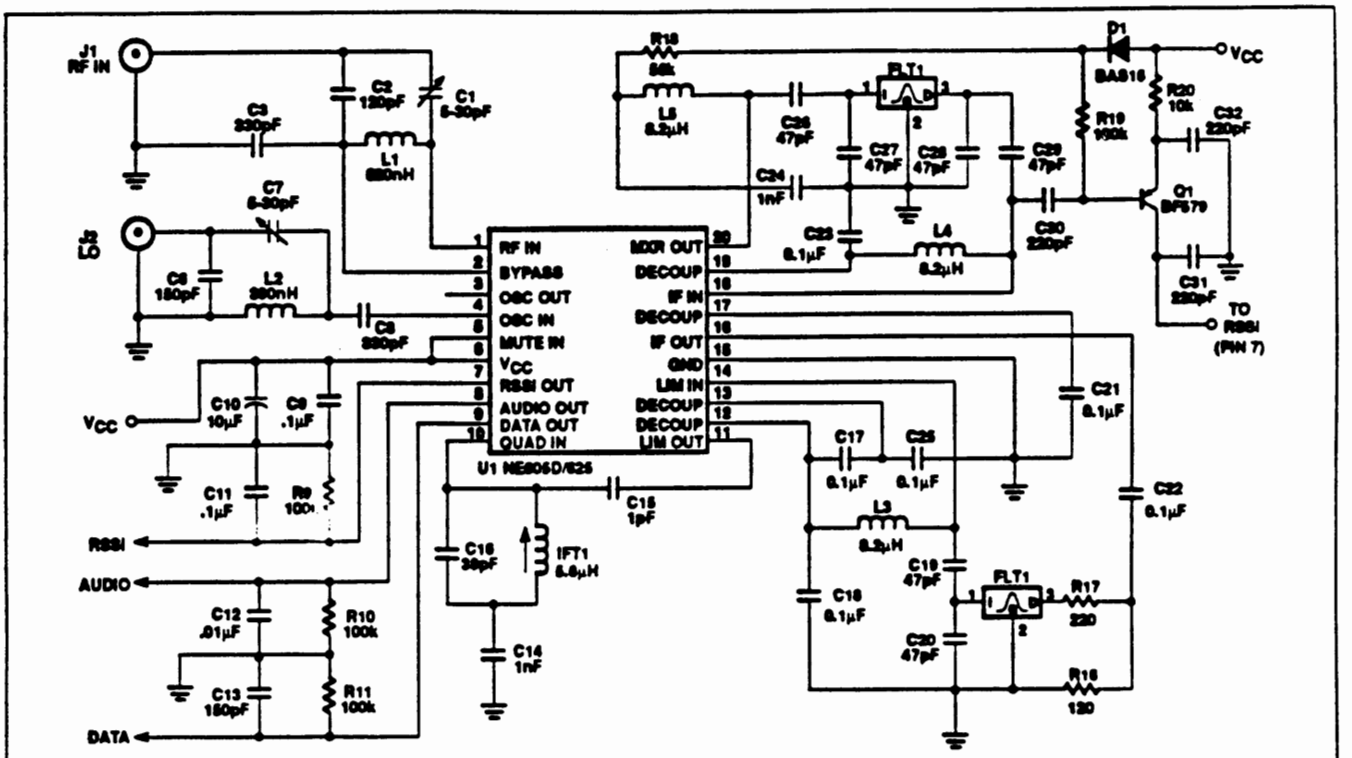


Figure 2. NE/SA605/625 Schematic: RF = 45MHz, LO = 55.7MHz, IF = 10.7MHz

The RF = 240MHz/IF = 10.7MHz demo-board is expected to perform less than the RF = 45MHz/IF = 10.7MHz demo-board because the mixer conversion gain decreases while the noise figure increases. These two parameters will decrease the performance of the receiver as the RF frequency increases.

With the new demands for fast RSSI time, Philips Semiconductors has also designed receiver chips with fast RSSI speed: The NE/SA624, NE/SA625 and SA626. The NE/SA625 can also be used in this layout because it is pin-for-pin compatible with the NE/SA605. The RSSI circuitry was the only change done for the NE/SA625, so performance will be similar to the NE/SA605. Performance graphs shown in this application note will reveal the similarities.

For systems requiring low voltage operation, IF=10.7MHz and fast RSSI speed, the SA626 will be the correct choice, however, this application note does not address the performance of the SA626 because the SA626 was not available at this writing.

Board Set-Up and Performance Graphs

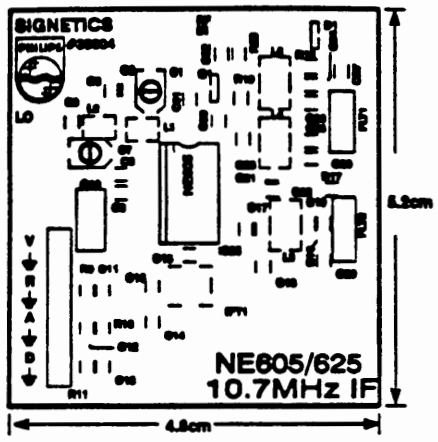
Figures 1 and 2 show the NE/SA605/625 schematics for the 240MHz and 45MHz boards, respectively. Listed below are the basic functions of each external components for both Figures 1 and 2.

SO Layout Schematic List

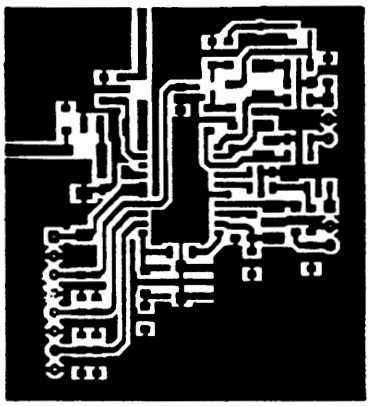
U1- NE/SA605 or NE/SA625
FLT1-10.7MHz ceramic filter Murata SFE10.7MA5-A (280kHz BW)
FLT2-10.7MHz ceramic filter Murata SFE10.7MA5-A (280kHz BW)

Note: If a designer wants to use different IF bandwidth filters than the ones used in this application note, the quad tank's S-curve may need to be adjusted to accommodate the new bandwidth.

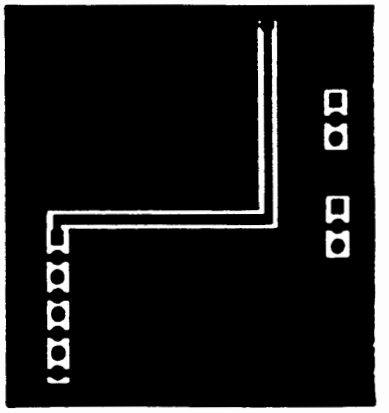
C1- Part of the tapped-C network to match the front-end mixer
C2- Part of the tapped-C network to match the front-end mixer
C3- Used as an AC short to Pin 2 and to provide a DC block for L1 which prevents the upsetting of the DC biasing on Pin 1
C6- part of the tapped-C network to match the LO input
C7- part of the tapped-C network to match the LO input
C8- DC blocking capacitor
C9- Supply Bypassing
C10- Supply bypassing (this value can be reduced if the NE/SA605/625 is used with a battery)
C11- used as a filter, cap value can be adjusted when higher RSSI speed is preferred over lower RSSI ripple
C12- used as a filter
C13- used as a filter
C14- used to AC ground the quad tank
C15- used to provide the 90° phase shift to the phase detector
C16- quad tank component to resonant at 10.7MHz with IFT1 and C15
C17- IF limiter decoupling capacitor
C18- DC block for L3 which prevents the upsetting of the DC biasing on Pin 14
C19- part of the tapped-C network for FLT2
C20- part of the tapped-C network for FLT2
C21- IF amp decoupling cap
C22- DC blocking cap
C23- IF amp decoupling cap and DC block for L3 which prevents the upsetting of the DC biasing on Pin 14
C24- provides DC block for L5 which prevents the upsetting of the DC biasing on Pin 20
C25- IF limiter decoupling capacitor
C26- part of the tapped-C network for FLT1
C27- part of the tapped-C network for FLT1
C28- part of the tapped-C network for FLT1
C29- part of the tapped-C network for FLT1
R9- used to convert the current into the RSSI voltage
R10- converts the audio current to a voltage
R11- converts the data current to a voltage
R16- used to kill some of the IF signal for stability purposes
R17- used in conjunction with R16 for a matching network for FLT2



TOP SILK SCREEN



TOP VIEW



BOTTOM VIEW

Figure 3. NE/SA605/625 SO Demo-Board Layouts (Not Actual Size)

L1 - part of the tapped-C network to match the front-end mixer
L2 - part of the tapped-C network to match the front-end mixer
L3- part of the tapped-C network to match the input of FLT2
L4- part of the tapped-C network to match the input of FLT1
L5- part of the tapped-C network to match the input of FLT1

RSSI Extender Circuit

R18-provides bias regulation, the gain will stay constant over varying V_{CC}
R19-for biasing, buffer RF DC voltage
R20-provides the DC bias, RSSI gain (when R20 increases, RSSI gain decreases
C30-DC blocking capacitor which connects the ceramic filter's output to the PNP transistor's input
C31-decoupling capacitor, and should be removed for measuring RSSI systems speed
C32-peak detector charge capacitor
D1- diode to stabilize the bias current
Q1- Philips BF579 PNP transistor
IFT1-part of the quad tank circuit

There are minor differences between Figures 1 and 2. The RF and LO tapped-C component values are changed to accommodate for the different RF and LO test frequencies (RF=240MHz and 45MHz and LO = 229.3MHz and 55.7MHz). The other difference is the value of R20. This resistor value was changed to optimize the RSSI curve's linearity (see RSSI extender section in this application note for further details).

The recommended NE/SA605/625 layout is shown in Figure 3. This layout can be integrated with other systems.

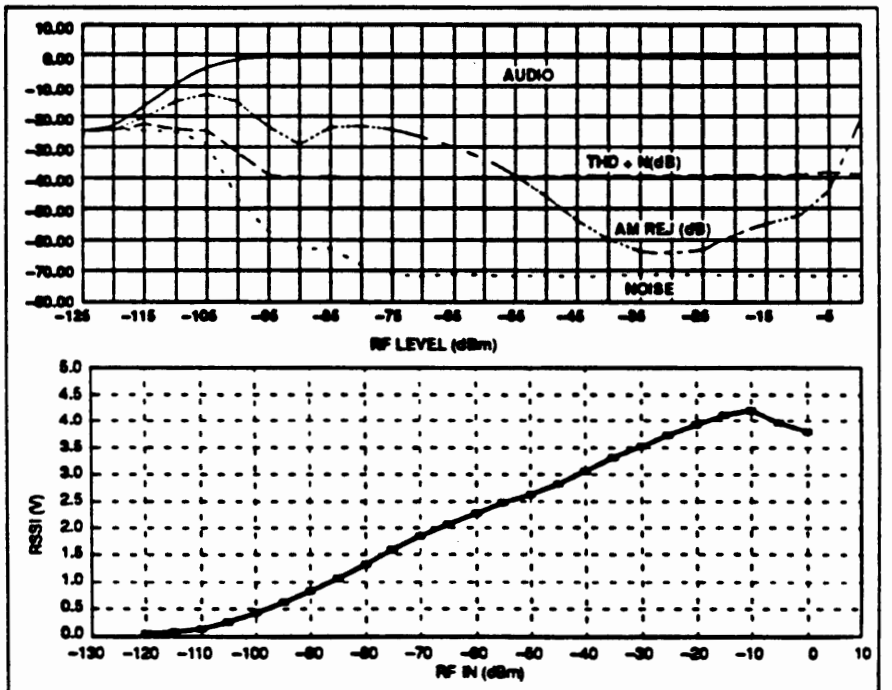


Figure 4. NE/SA625 SO Performance Graphs at 240MHz

Figures 4 through 7 show the performance graphs for the NE/SA605 & NE/SA625 at 240MHz and 45MHz RF inputs. There was no real noticeable difference in performance between a NE/SA605 or NE/SA625 except for AM rejection. The NE/SA605 appears to have a little better AM rejection, but from the end user's point of view, there is no difference between the receiver. All the other measurements were perfect, including SINAD.

RF Input

The NE/SA605/625 board is set up to receive an RF input of 240MHz (see Figure 1). This is achieved by implementing a tapped-C network. The deviation should be set to ±70kHz to achieve ***-110dBm to -112dBm for -12dB SINAD***. However, the deviation can be increased to ±100kHz, depending on the bandwidth of the IF filter and the Q of the quad tank.

Demodulating at 10.7MHz IF with the NE/SA605/625 AN1996

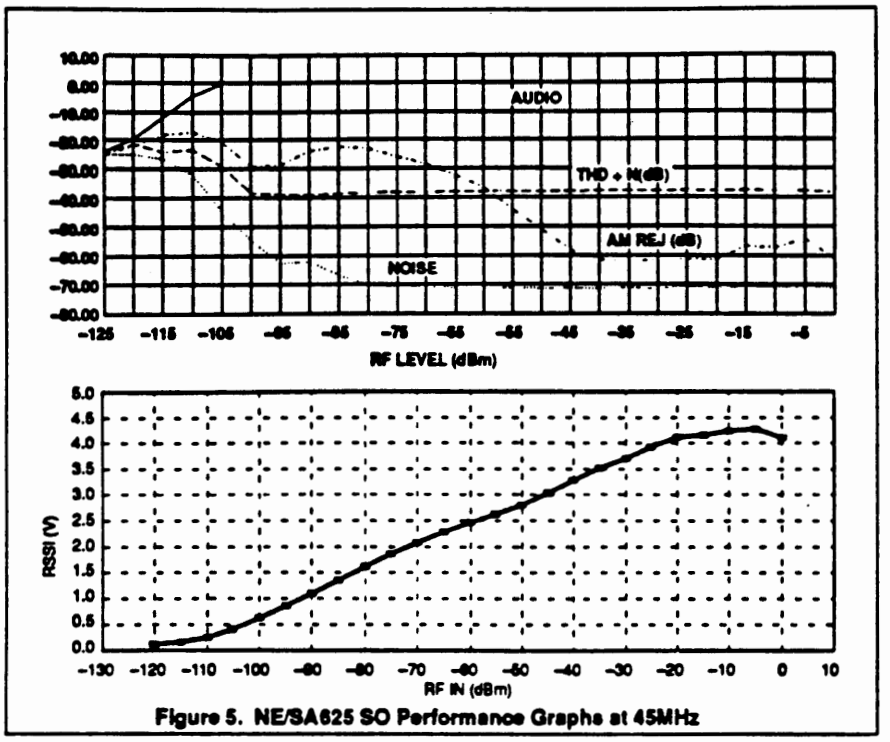


Figure 5. NE/SA625 SO Performance Graphs at 45MHz

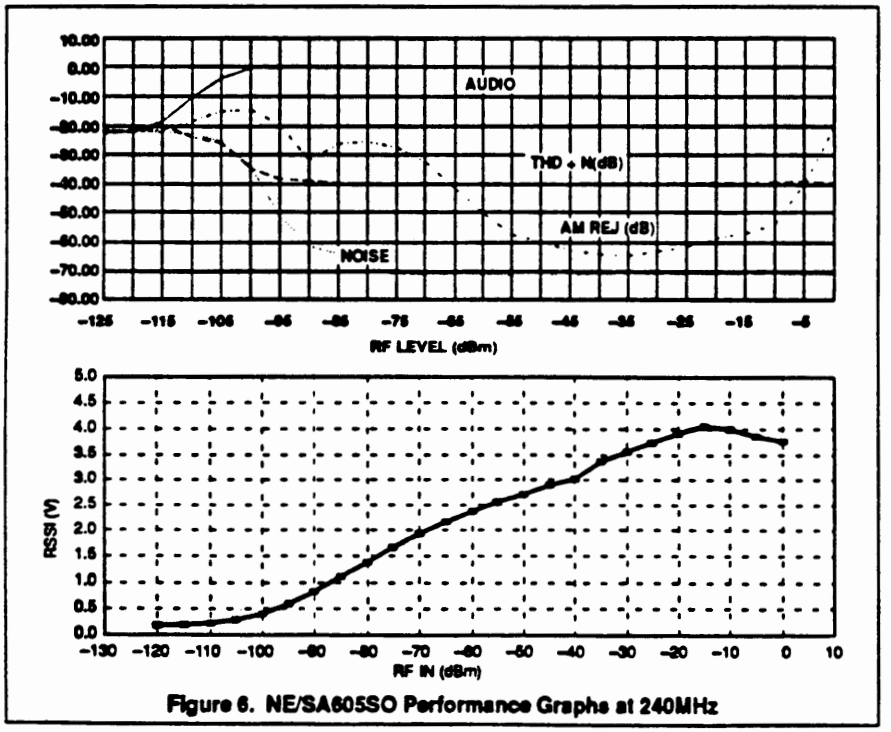


Figure 6. NE/SA605SO Performance Graphs at 240MHz

Because we wanted to test the board at 45MHz, we changed the values of the tapped-C network for the RF and LO ports (see Figure 2). We found that a ***-116dBm to -118dBm for -12dB SINAD*** could be achieved. With these results, we were pretty close to achieving performance similar to our standard 455kHz IF board.

A designer can also make similar RF and LO component changes if he/she needs to evaluate the board at a different RF frequency. ***It should be noted that if a designer purchases a stuffed NE/SA605/625 demo-board from Philips Semiconductors its set up will be for an RF input frequency of 240MHz.*** AN1994 will aid the designer in calculating the tapped-C values for other desired frequencies, while AN1995 will be of value for making S11 bench measurements. Just remember that the input impedance will differ for different RF frequencies.

LO Input

The LO frequency should be 229.3MHz for the RF = 240MHz demo-board and have a drive level of -10dBm to 0dBm (this also applies for the RF = 45MHz and LO = 55.7MHz). The drive level is important to achieve maximum conversion gain. The LO input also has a matched tapped-C network for efficiency purposes which makes for good RF practices.

If a designer wanted to change the matching network to inject a different LO frequency, he/she could follow the steps in AN1994 and assume that the input impedance is around 10kΩ for low frequency inputs. The main goal is to get maximum voltage transfer from the signal generator to the inductor.

An external oscillator circuit was used to provide greater flexibility in choosing different RF and LO frequencies; however, an on-board oscillator can be used with the NE/SA605/625. New high frequency fundamental crystals, now entering the market, can also be used for high LO frequency requirements. Most receiver systems, however, will use a synthesizer to drive the LO port.

10.7MHz Ceramic Filters

The input and output impedance of the 10.7MHz ceramic IF filters are 330Ω. The NE/SA605/625's input and output impedances are roughly 1.5KΩ. Therefore, a matching circuit had to be implemented to obtain maximum voltage transfer. Tapped-C networks were used to match the filters input and output impedance.

But in this case, we decided to go with non-tuning elements to reduce set-up time. Figure 8 shows the values chosen for the network.

Although our total deviation is 140kHz, we used 280kHz IF bandwidth filters to maximize for fast RSSI speed. The SINAD performance difference between using 180kHz BW filter versus 280kHz BS filter was insignificant.

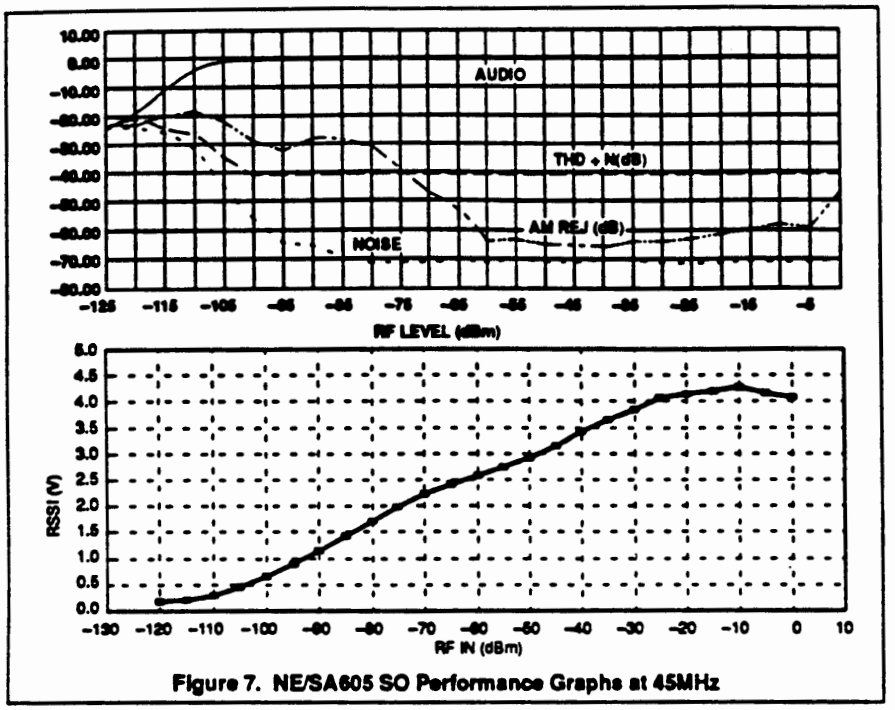


Figure 7. NE/SA605 SO Performance Graphs at 45MHz

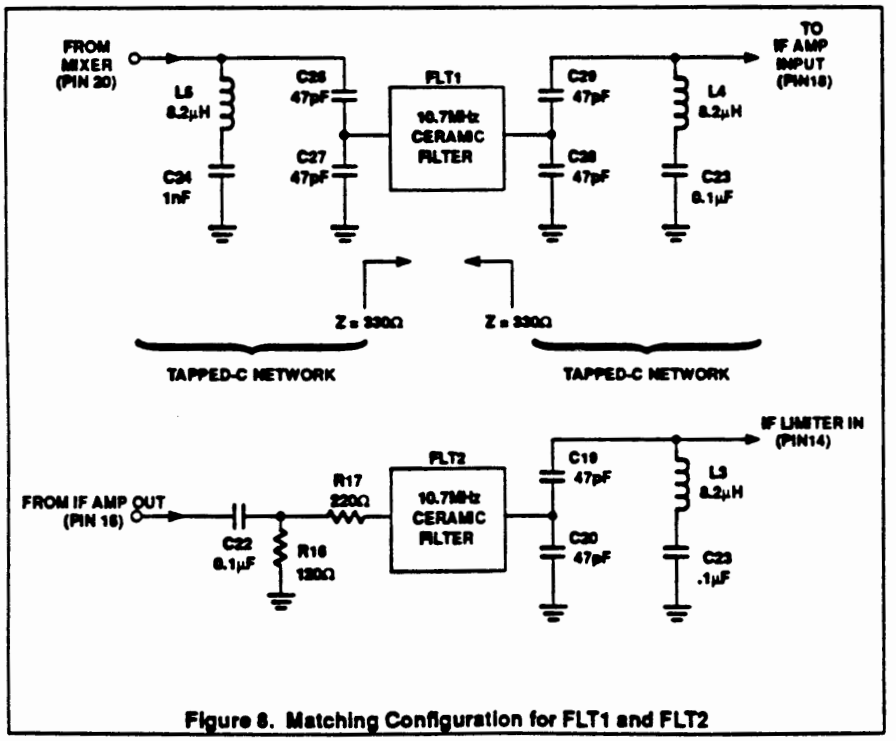


Figure 8. Matching Configuration for FLT1 and FLT2

Stabilizing the IF Section From Regeneration

Because the gain in the IF section is 100dB and the wavelength for 10.7MHz is small, the hardest design phase of this project was to stabilize the IF section.

The steps below show the methods used to obtain a stable layout.

1. The total IF section (IF amp and limiter) gain is 100dB which makes it difficult to stabilize the chip at 10.7MHz. Therefore, a 120Ω (R16 of Figure 1) resistor was used to kill some of the IF gain to obtain a stable system. (NOTE: Expect AM rejection performance to degrade as you decrease the IF gain externally.)
2. Since the tapped-C inductors for FLT1 and FLT2 are not shielded, it is important not to place them too close to one another. Magnetic coupling will occur and may increase the probability of regeneration.
3. It was also found that if the IF limiter bypass capacitors do not have the same physical ground, the stability worsens. Referring to Figure 1, the IF limiter bypass capacitors (C17, C25) are connected to assure a common ground.
4. The positioning of ground feedthroughs are vital. A designer should put feedthroughs near the IF bypass capacitors ground points. In addition, feedthroughs are needed underneath the chip. Other strategic locations are important for feedthroughs where insufficient grounding occurs.
5. Shielding should be used after the best possible stability is achieved. The NE/SA605/625 demo-board is stable, so shielding was not used. However, if put into a bigger system, shielding should be used to keep out unwanted RF frequencies. As a special note, if a good shield is used, it can increase the R16 resistor value such that there is less IF gain to kill to achieve stability. This means the RSSI dynamic range is improved. So if a designer does not want to implement the RSSI extender circuit, but is still concerned with SINAD and RSSI range, he/she can experiment with R16 and shielding because there is a correlation between them (see RSSI extender section in this application note for more information). In addition, AM rejection performance will improve due to the greater availability of the total IF gain.

The key to stabilizing the IF section is to kill the gain. This was done with a resistor (R16 in Figure 8) to ground. All the other methods mentioned above are secondary compared to this step. Lowering the value of this resistor reduces the gain and the increasing resistor value kills less gain. For our particular layout, 120Ω was chosen to obtain a stable board, but we were careful not to kill too much gain. One of the downfalls of killing too much gain is that the SINAD reading will become worse and the RSSI dynamic range is reduced.

Demodulating at 10.7MHz IF with the NE/SA605/625 AN1996

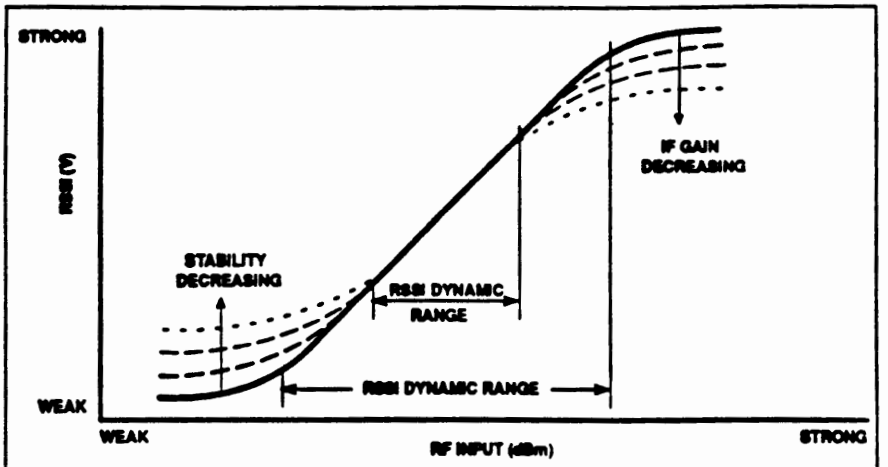
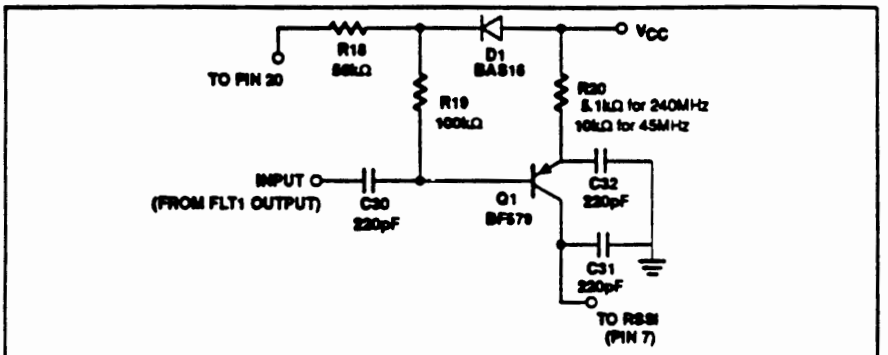


Figure 9. RSSI Dynamic Range



RSSI EXTENDER COMPONENT LIST AND EXPLANATION

R18–provides bias regulation, the gain will stay constant over varying V_{CC}

R19–for biasing, buffer RF DC voltage

R20–provides the DC bias, RSSI gain (when R20 increases, RSSI gain decreases

C30–DC blocking capacitor which connects the ceramic filter's output to the PNP transistor's input

C31–de-coupling capacitor

C32–peak detector charge capacitor

D1–diode to prevent improper current flow

Q1–Philips BF579 PNP transistor

Figure 10. External RSSI Extender Circuit

RSSI Dynamic Range

There are two main factors which determine the RSSI dynamic range. These two factors are 1.) how stable is the board, and 2.) how much gain is killed externally. If the board is unstable, a high RSSI voltage reading will occur at the bottom end of the curve. If too much gain is taken away, the upper half of the curve is flattened. Thus the dynamic range can be affected. Figure 9 shows how the linear range can be decreased under the conditions mentioned above.

It is important to choose the appropriate resistor to kill enough gain to get stability but not too much gain to affect the upper RSSI curve dynamic range. Because we had to kill some IF gain to achieve good board stability and good SINAD readings, our RSSI overall dynamic range was reduced on the upper end of the curve.

Because SINAD and the RSSI dynamic range are two important parameters for most of our customers, we decided to add an "RSSI extender" modification to the board to get the best of both worlds. Together with the RSSI external modification and the "stability resistor", we can now achieve excellent SINAD readings and maintain a wide RSSI dynamic range.

RSSI Extender Circuit

The RSSI extender circuit increases the upper dynamic range roughly about 20-30dB for the 240MHz demo-board. The NE/SA605/625 demo-board has 90-100dB of linear dynamic range when the RSSI modification is used.

Referring to Figure 10, one can see that one transistor is used with a few external components. The IF input signal to the PNP transistor is tapped after the ceramic filter to ensure a clean IF signal. The circuit then senses the strength of the signal and converts it to current, which is then summed together with the RSSI output of the chip.

The PNP transistor stage has to be biased as a class B amplifier. The circuit provides two functions. It is a DC amplifier and an RF detector. The gain of the RSSI extender can be controlled by R20 and R9 (Gain = R9/R20). Adjusting R20 is preferable because it controls the upper half of the RSSI curve, whereas adjusting R9 shifts the whole RSSI curve.

If a different RF frequency is supplied to the mixer input, it is important to set the external RSSI gain accordingly. When the RF input was changed from 240MHz to 45MHz, the conversion gain of the mixer increased. Therefore, the earlier gain settings for the RSSI extender was too much. A lower gain setting had to be implemented such that a smoother transition would occur.

Quad Tank

The quad tank is tuned for 10.7MHz ($F=1/2\pi\sqrt{LC}$). Figure 1 shows the values used (C14,C15, C16, IFT1) and Figure 11 shows the S-curve. The linear portion of the S-curve is roughly 200kHz. Therefore, it is a good circuit for a total deviation of 140kHz. It is possible to deviate at 200kHz, but this does not leave much room for part tolerances.

If more deviation is needed, a designer can lower the S-curve with a parallel resistor connected to the quadrature tank. A designer should play with different value resistors and plot the S-curve to pick the best value for the design. To key in on the resistor value with minimum effort, a designer can put a potentiometer in parallel with the quad tank and tune it for best distortion. Then the designer can use fixed value resistors that are close to the potentiometer's value.

Fixed quad tank component values can be used to eliminate tuning, but a designer must allow for part tolerances and temperature considerations. For better performance over temperature, a resonator/discriminator can be used. Thus, no tuning is required for the quad tank section, which will save on production costs.

Demodulating at 10.7MHz IF with the NE/SA605/625 AN1996

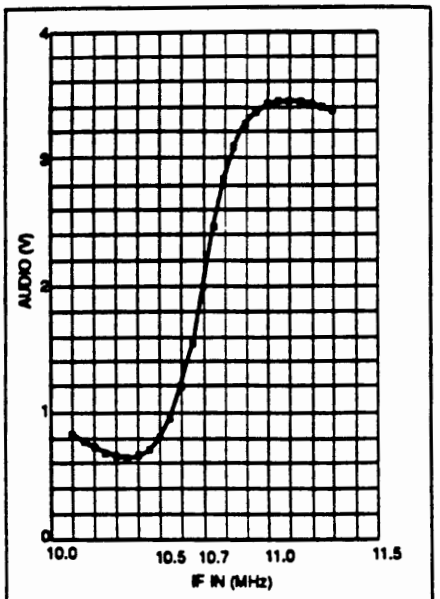


Figure 11. 10.7MHz Quad Tank S-Curve

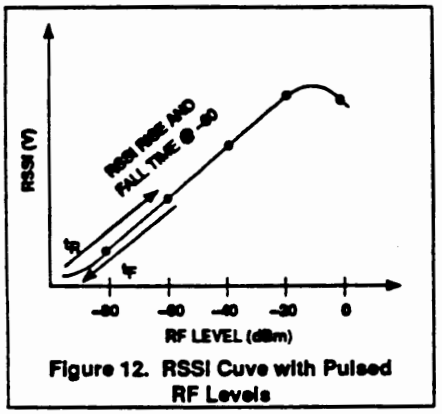


Figure 12. RSSI Cuve with Pulsed RF Levels

RSSI System Speed

The RSSI rise and fall times are important in applications that use pulsed RF in their design. The way we define the speed is how fast the RSSI voltage can travel up and down the RSSI curve. Figure 12 shows a representation of this. Five different pulsed RF levels were tested to get a good representation of the RSSI speed. One can predict that the stronger the pulsed signal, the higher the RSSI voltage and the longer it will take for the fall time to occur. Generally speaking, the rise time is determined by how long it takes to charge up an internal capacitor. The fall time depends on how long it takes to discharge this capacitor.

It is also important to understand that there are two types of RSSI speeds. The first type is the RSSI *chip* speed and the second is the RSSI *system* speed. The RSSI *chip* speed will be faster than the *system* speed. The bandwidth of the external filters and other external parts can slow down the RSSI system speed dramatically.

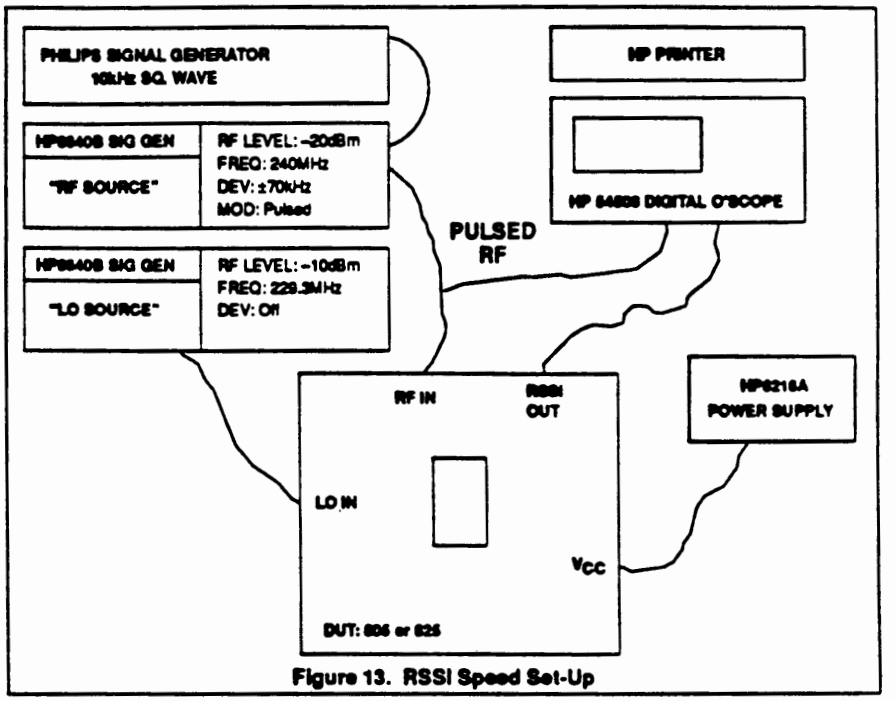


Figure 13. RSSI Speed Set-Up

Figure 13 shows the bench set up for the RSSI system speed measurements. The pulsed RF was set for 10kHz and and the RSSI output was monitored with a digital oscilloscope. Figure 14 shows how the rise and fall times were measured on the oscilloscope.

The modifications done on the NE/SA625 board are shown in Figure 15. The RSSI caps C11 and C31 were eliminated, and the RSSI resistor values were changed. We wanted to see how much time was saved by using a smaller RSSI resistor value.

The RSSI system speed for the 240MHz NE/SA625 demo board is shown in Figure 16. Again, the only modification was that the RSSI caps (C11 and C31) were taken out and the RSSI resistor value (R9) was varied. For different RF levels, the speed seems to vary slightly, but this is expected. The higher the RSSI voltage, the longer it will take to come back down the RSSI curve for the fall time.

Looking more closely at Figure 16, one can note that the 0dBm input level has a faster fall time than the -20dBm level. This occurs because of the limited dynamic range of the test equipment. The equipment does not have sufficient on/off range, so at 0dBm the 'off' mode is actually still on. Therefore, you don't get a true reading.

At 0dBm the RSSI voltage is lower than -20dBm. The reason why this happens is because the RSSI linearity range stops at -10dBm. When the RF input drive is too high (e.g., 0dBm), the mixer conversion gain decreases, which causes the RSSI voltage to drop.

QUESTION AND ANSWER SECTION

Q. What should the audio level at Pin 8 be?

A. The audio level is at 580mV$_{p-p}$ looking directly at the audio output pin and does not include a C-message filter. However, the audio output level will depend on two factors: the "Q" of the quadrature tank and the deviation used. The higher the quad tanks "Q", the larger the audio level. Additionally, the more deviation applied, the larger the audio output. But the audio output will be limited to a certain point.

Q. Am I required to use the 10µF supply capacitor?

A. No, a smaller value can be used. The 10µF capacitor is a suggested value for evaluation purposes. Most of the time a power supply is used to evaluate our demo boards. If the supply is noisy, it will degrade the receiver performance. We have found that a lower value capacitor can be used when the receiver is powered

Demodulating at 10.7MHz IF with the NE/SA605/625 — AN1996

by a battery. But it is probably safer to stay at a reasonable capacitor size.

Q. Can I use different IF filters for my required bandwidth specifications?

A. Yes, you can order different IF filters with different bandwidths. Some of the standard manufacturers have 180kHz, 230kHz, and 280kHz bandwidths for 10.7MHz ceramic filters. Just be sure that the quad tank "S-curve" is linear for your required bandwidth. The NE/SA605/625 demo-board has a 200kHz linearity for the quad tank. So ±70kHz deviation is perfect.

We have also found that even though the IF filter's bandwidth might be more than our requirements, it does not really degrade overall receiver performance. But to follow good engineering practices, a designer should order filters that are closest to their requirements. Going with wider bandwidth filters will give you better RSSI system speed.

Q. I want to use part of your demo board for my digital receiver project. Can you recommend a good 10.7MHz filter with accurate 10.7MHz center frequency which can provide minimum phase delay?

A. At the present time, I only know of one manufacturer that is working on a filter to meet digital receiver requirements. Murata has a surface mount 10.7MHz filter. The number is FX-6502 (SFECA 10.7). It was specifically designed for Japanese digital cordless phones. You can adapt these filters to our NE/SA605/625 demo board.

We also used these filters in our layout and got similar SINAD and RSSI system speed performance compared to the standard 10.7MHz filters (280kHz BW). I believe the difference between the filters will be apparent for digital demodulation schemes.

Q. If the system RSSI time is dependent on the external components used, like the IF filters, then what is the difference in using the NE/SA605 vs the NE/SA625?

A. The difference comes in the fall time for high IF frequencies. You are correct that for IFs like 455kHz, there is probably little delta difference because the filter's bandwidth prohibits the speed dramatically. However, for 10.7MHz IFs, there will be a difference in the fall time between the chips because the bandwidths are much wider. Therefore, the chips will play a role in the RSSI system speed. The chip difference in RSSI speed will depend on your overall system configuration.

Q. Why does the AM rejection performance look better on the NE/SA605, 455kHz IF board than the NE/SA605/625 10.7MHz IF demo-board?

A. For the 455kHz IF demo-board there is more IF gain available compared to the 10.7MHz IF board. Recall that for the 10.7MHz IF board, some of the IF gain was killed externally for stability reasons. Since the IF gain helps improve AM rejection performance, by killing IF gain, AM rejection is decreased.

Q. The NE/SA605/625 10.7MHz IF demo-board is made for the SO package. Can I use your SSOP package and expect the same level of performance?

A. We have not done a SSOP layout yet. But if the same techniques are used, I am sure the SSOP package will work. The SA626 demo-board will be done in SSOP, and probably be available in the future.

Q. I tried to duplicate your RSSI system reading measurements using your demo-board and I get slower times. What am I doing wrong?

A. The RSSI system speed measurements are very tricky. Make sure your cable lengths are not too long. I have found that when making microsecond measurements, lab set-up is of utmost importance. Also, make sure the RSSI caps (C11 and C31) are removed from the circuit.

Also be sure that the bandwidth of your IF filters is not slowing down the RSSI system speed (Cf: section on RSSI system speed).

Q. I am going to use your design in my NTT cordless digital phone. Can you recommend a 240.05MHz filter?

A. Murata SX-4896 (SAMAFC 240.05) is a filter you can use for your application.

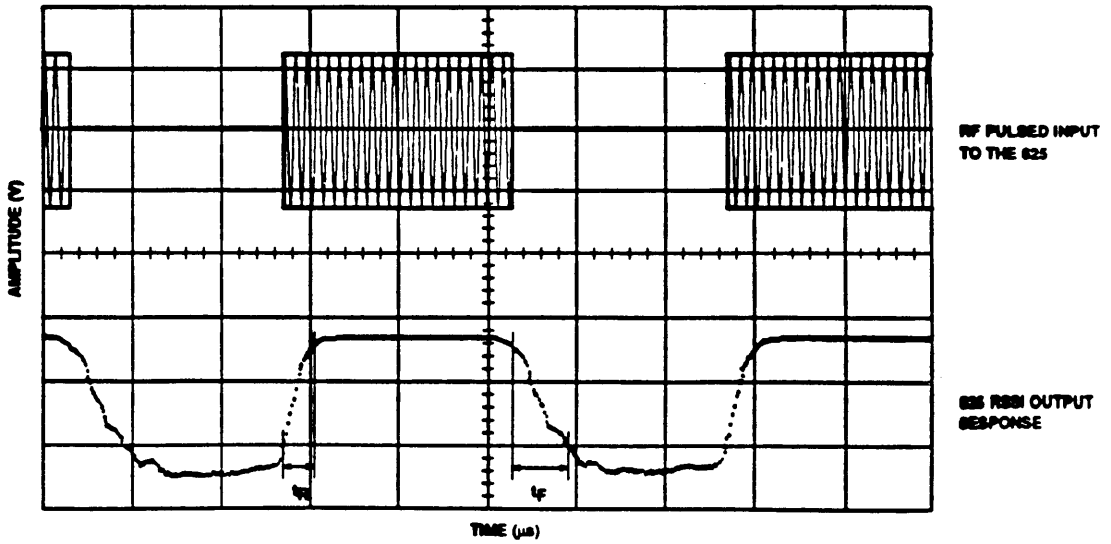


Figure 14. Oscilloscope Display of RSSI System Rise and Fall Time

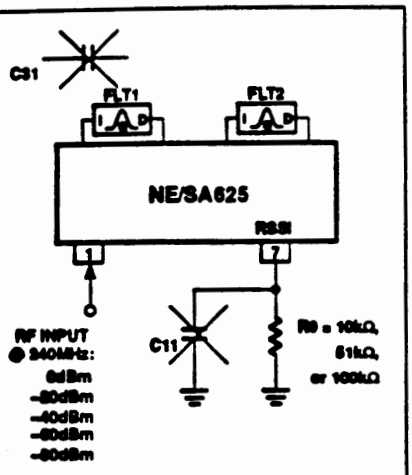


Figure 15. NE/SA625 RSSI Test Circuit Configuration

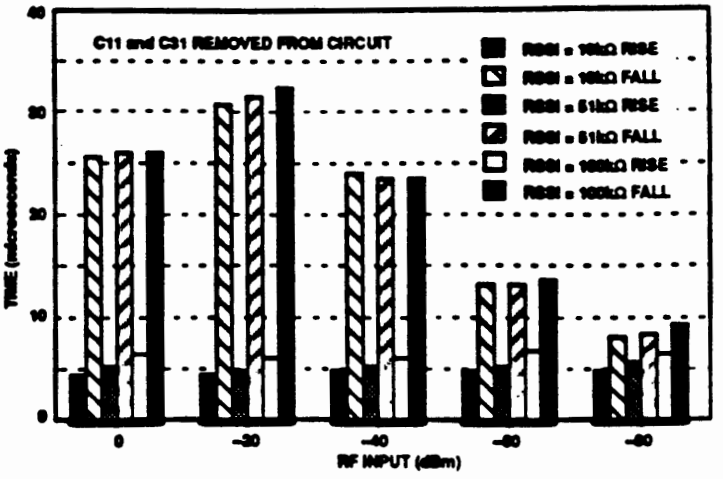


Figure 16. RSSI Systems Rise and Fall Time with Different RSSI Resistor Values

Table 1. FM/IF Family Overview

		NE602A/604A		NE605	NE606	SA607	SA608	NE624	NE625	SA626	NE627
V_{CC}		4.5–6V	4.5–6V	4.5–6V	2.7–7V	2.7–7V	2.7–7V	4.5-8.0V	4.5-8.0V	2.7–6.5V	4.5-8.0V
I_{CC}		2.4mA@6V	3.3mA @ 6V	5.7mA @ 6V	3.5mA @ 3V	3.5mA @ 3V	3.5mA @ 3V	3.4mA @ 6V	5.8mA @ 6V	6.5mA @ 3V	5.8mA @ 6V
Number of Pins		8	16	20	20	20	20	16	20	20	20
Packages NE: 0 to +70°C SA: –40 to +85°C N: Plastic DIP D: Plastic SO FE: Ceramic DIP DK: SSOP		NE602AN NE602AD NE602AFE SA602AN SA602AD SA602AFE	NE604AN NE604AD SA604AN SA604AD	NE605N NE605D NE605DK SA605N SA605D SA605DK	NE606N NE606D NE606DK SA606N SA606D SA606DK	SA607N SA607D SA607DK	SA608N SA608D SA608DK	NE624N NE624D SA624N SA624D	NE625N NE625D NE625DK SA625N SA625D SA625DK	SA626D SA626DK	NE627N NE627D NE627DK SA627N SA627D SA627DK
–12dB SINAD (RF = 45MHz), IF = 455kHz 1kHz Tone, 8kHz Dev.		–120dBm / .22uV		–120dBm / .22uV	–117dBm / .31uV	–117dBm / .31uV	–117dBm / .31uV	–120dBm / .22uV	–120dBm / .22uV	–112dBm / .64uV (RF = 240MHz) (IF = 10.7MHz) 1kHz Tone, +/–70kHz Dev.	–120dBm / .22uV
Process f_t		8GHz		8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz	8GHz
For lower cost version and less performance		612A & 614A		615	616	617	—	—	—	—	—
Features		– Audio & Data pins – IF BW of 25MHz – No external matching required for standard 455kHz IF filter		– Audio & Data pins – IF BW of 25MHz – No external matching required for standard 455kHz IF filter	– Low voltage – Internal RSSI and audio op amps – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Freq check pin – Low voltage – Internal RSSI and audio op amps – Unity gain RSSI output – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Freq check pin – Low voltage – Internal RSSI and audio op amps – Unity gain audio output – No external matching required for standard 455kHz IF filter – IF BW of 2MHz	– Fast RSSI Time – Pin-to-Pin compatible with 604A – No external matching required for standard 455kHz IF filter	– Fast RSSI Time – Pin-to-Pin compatible with 605 – No external matching required for standard 455kHz IF filter	– Power down mode – Low voltage – Fast RSSI Time – IF BW of 25MHz – Internal RSSI & audio op amps – No external matching required for standard 10.7MHz IF filter	– Fast RSSI Time – Freq check pin – IF BW of 25MHz – Internal RSSI & audio op amps – No external matching required for standard 455kHz IF filter
RSSI OUTPUT SECTION	Dynamic Range	90dB		90dB	90dB	90dB	90dB	90dB	90dB	90dB	90dB
	Accuracy	+/–1.5dB		+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB	+/–1.5dB
	455kHz IF Rise* Time	—	1.4us	—	—	—	—	1.1us	1.2us	—	1us
	455kHz IF Fall* Time	—	21.3us	—	—	—	—	1.3us	2.1us	—	1.7us
	10.7MHz IF Rise* Time	—	1.5us	—	—	—	—	1.2us	1.2us	1.2us	0.9us
	10.7MHz IF Fall* Time	—	19.4us	—	—	—	—	1.6us	2us	2us	1.4us

*NOTE: No IF filters in the circuit

Table 1. (cont.) FM/IF Family Overview

		NE602A/604A	NE605	NE606	SA607	SA608	NE624	NE625	SA626	NE627
MIXER	Max. Conversion Power Gain (RF = 45MHz; IF = 455kHz)	17dB	—	13dB	17dB	17dB	17dB	—	13dB	13dB	13dB	13dB
	3rd Order Intercept Point (Input) f1 = 45MHz f2 = 45.06MHz	-13dB	—	-106Bm	-9dBm	-8dBm	—	-106Bm	-116Bm f1 = 240.05 f2 = 240.35	-106Bm
	Noise Figure @45MHz	5dB	—	5dB	6.2dB	6.2dB	—	5dB	11dB @ 240MHz	5dB
	RF Input Resistance and Capacitance @45MHz	1.5k 3pF	—	4.7k 3.5pF	6k 3pF	6k 3pF	—	4.7k 3.5pF	4.7k 3.5pF @ 240MHz	4.7k 3.5pF
	Output Resistance	1.5k	—	1.5k	1.5k	1.5k	—	1.5k	330	1.5k
IF AMP	Input Impedance	—	1.6k	1.5k	1.5k	1.5k	1.6k	1.6k	330	1.5k
	Output Impedance	—	1.0k	330	330	330	1.0k	1.0k	330	1.0k
	Gain	—	40dB	44dB	44dB	44dB	40dB	40dB	44dB	40dB
	BW	—	41MHz	5.5MHz	5.5MHz	5.5MHz	41MHz	41MHz	40MHz	40MHz
LIMITER	Input Impedance	—	1.6k	1.5k	1.5k*	1.5k	1.6k	1.6k	330	1.5k
	Output* Impedance	—	330	330	330	330	330	330	330	330
	Gain	—	80dB	98dB	98dB	98dB	40dB	80dB	88dB	80dB
	BW	—	25MHz	4.5MHz	4.5MHz	4.5MHz	25MHz	25MHz	25MHz	25MHz
IF OUT	Total IF Gain	—	100dB	100dB	100dB	100dB	100dB	100dB	98dB (includes -6dB pad)	100dB
	Total IF BW	—	25MHz	2MHz	2MHz	2MHz	25MHz	25MHz	25MHz	25MHz

NOTE: *Not designed to drive a matched load

Windata Inc.

WIRELESS INFORMATION NETWORKS

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11/11/92

Agenda

- Wireless LANs - Why all the fuss?
- Market Opportunities
- Technology Options
- Standards, The FCC, and International
- Technology Trends

What is a Wireless LAN?

- Systems operating at >1 Mbps
- Broadcast packet communications
- Indoor / In-building applications
- 30-100 meter distance coverage
- Current technology focus is radio in unlicensed frequency bands

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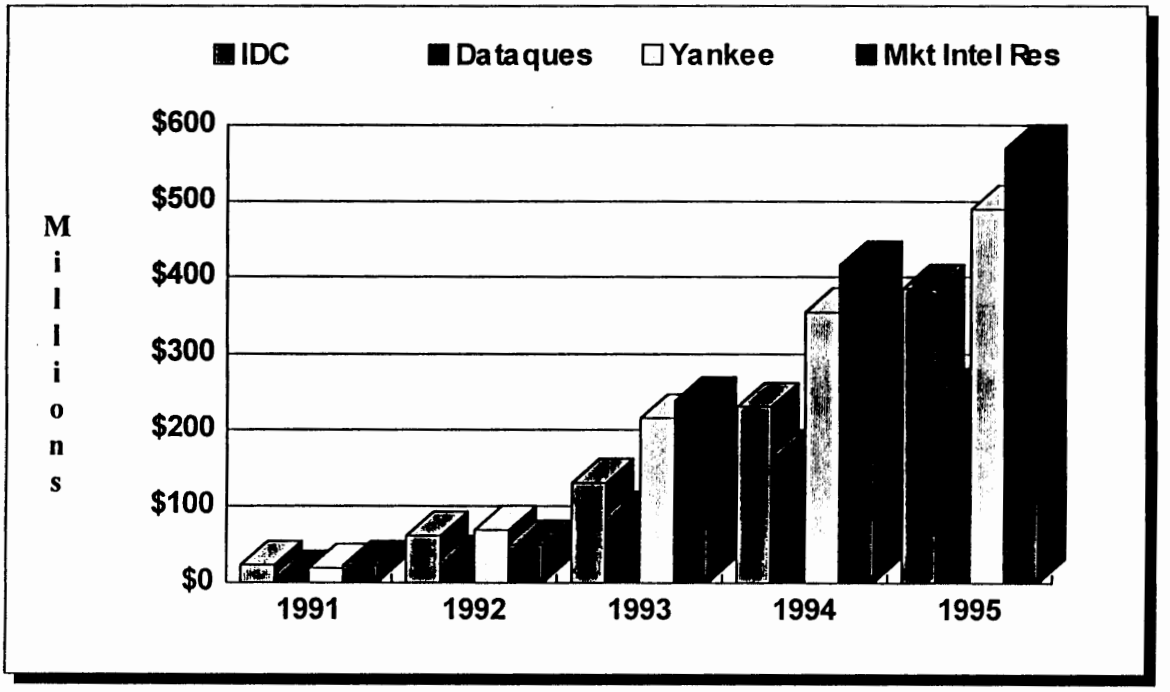
Why all the fuss?

- **The LAN connection of choice for portable computers**
- **Augmentation to existing wired LANs**
  - **Rapid deployment**
  - **Construction limitations**
  - **Aesthetics**
  - **Labor intensive adds and changes**
- **Wiring alternative for interbuilding links**

804-4

Wireless LAN Market Forecast



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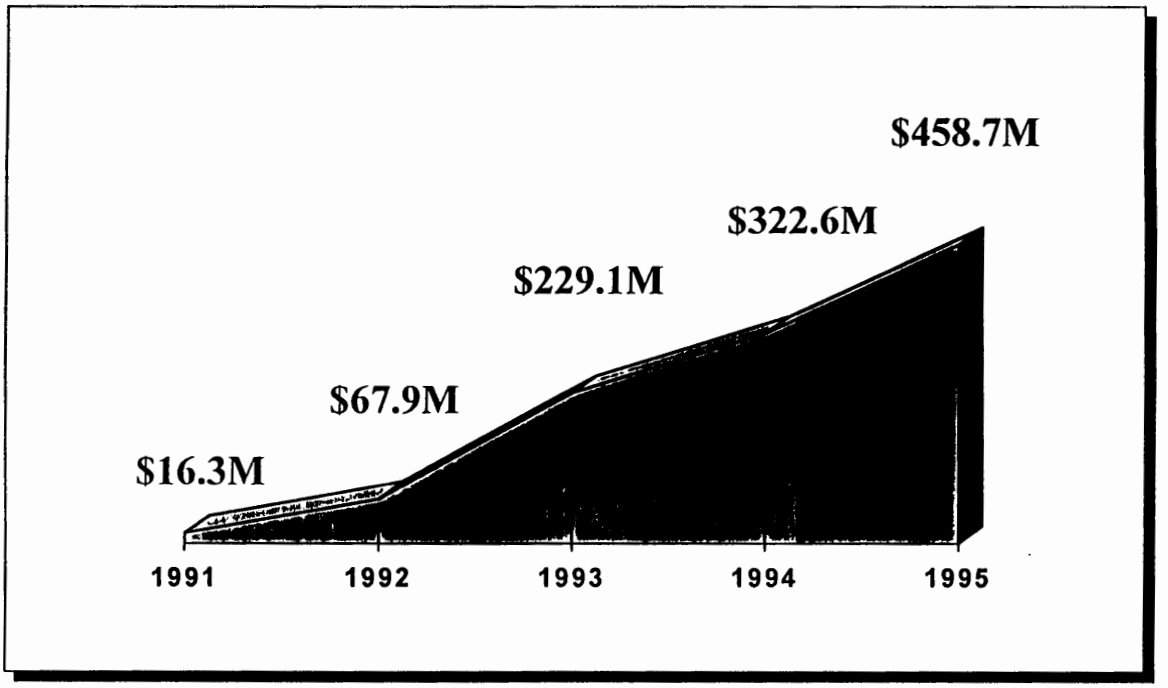
WLAN Market Size - $



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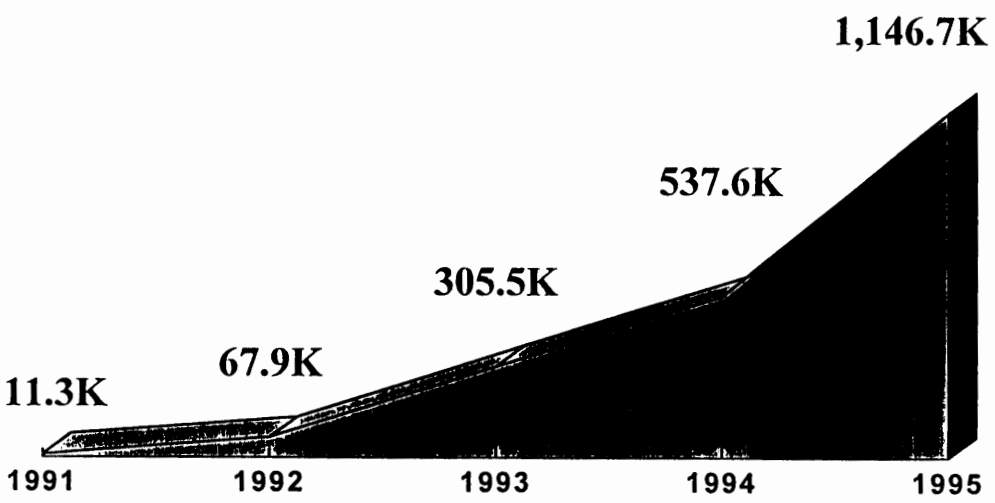
WLAN Market Size - Units



Market Segmentation

Wireless Data Network Market Segmentation

Attribute	In-Business	Outdoor/Mobile	Home
License?	no	maybe	equipment certified
Data Rate	LAN speeds	< 50 Kbps	< 1 mbps (ISDN?)
Distance	<100 meters	>> 100 meters	< 100 meters
Voice & Data	maybe	yes	yes
$/bit or $/sec	no	yes	no
Typical Application?	Your portable connected to the Corporate LAN	Your PDA in your car with digital voice (PCS)	High quality digital voice, message storage, LAN, and phone line/ cable connection for your in-house network

What are the market drivers?

- **Product cost**
  - > $1000 - rapid deployment/harsh environments
  - $500-1000 - wired LAN augmentation
  - <$500 - portables/general usage/why use wire?
- **Growth of networked portables**
- **Killer applications**
  - Enterprise network services for portables
  - Wireless classroom
  - Wireless business meeting

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Infrared Transmission

- **Infrared**

Point-to-point	10 Mbps, 1km, LOS
Focused Shared Beam	1 Mbps, 100 ft, reflected
Diffuse	1 Mbps, 20 ft, diffuse

- **Diffuse Infrared is the most promising infrared option**
- **Laser and High Power Infrared**

801-10

Radio Transmission

- **Four Radio choices:**
  - **Licensed (Motorola at 18 GHz)**
  - **Unlicensed Part 15(902-928, 2400-2485, 5700-5825 MHz)**
    Direct Sequence
    Frequency Hopped
  - **Low Power**
  - **New Part 15 Allocation(1910-1930 MHz)**

802.11

Windata's Solution

- **Spread Spectrum "radio" based family of products**
- **Offer family of products in three major categories:**

  Ethernet* and *token ring products that integrate transparently to enterprise structured wire at LAN speed and performance

  Inter-building wireless products

  Portable computing battery operated wireless LANs

All systems focused on high performance, easy connection to wired systems, and SNMP network management

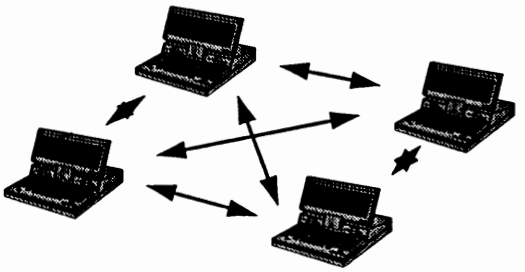
The Indoor Radio Problem

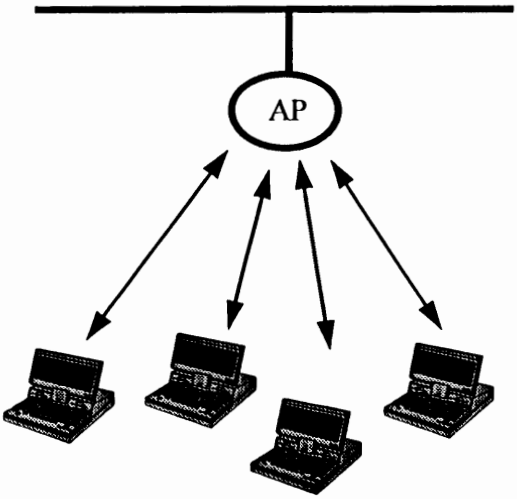
- **Multipath**
  Reflections
- **Outages**
  Difficult locations disrupting system operation
- **Propagation path changes**
  Doors closing, people moving, etc.

Surprisingly, signal power is not the major problem!

The Architectural Question

Is the system peer to peer or controller based?





Why a Hub or Access Point?

- Consistent with structured wire installations
- Doubles service area over peer to peer
- Solves near-far problem
- Simplifies and reduces cost of transceiver
- Provides focus for network management
- Provides logical interface point to wired LANs
- Provides wake-up capability for reduced power consumption

Reliable wireless data communications systems cannot be built without a hub or access point

The FCC & Standards

- **IEEE-802.11**
- **FCC and DATA-PCS**
- **The WINForum**
- **Motorola and 18 GHz licensing**

International Activities

- Europe is looking at 2.4 and 5.2 GHz (lower power than US)
- Japan at 2.4 GHz, 300 Mhz, but 30 milliwatts
- Many companies are building 2.4 GHz spread spectrum systems because of potential international opportunity
- Data-PCS band is a very appealing because it is a clear channel(?), capable of being a silicon radio, and without spread spectrum restrictions

804-17

A Low Current UHF Remote Control System using a SAW based superhet receiver

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ABSTRACT

This paper presents a new technical approach to a low current UHF remote control system. This system is universal with regard to modulation systems (AM or FM), different transmission coding and a wide range of data rates. After a description of the system's boundary conditions and the SAW (surface acoustic wave resonator) stabilized single stage transmitter, we are focusing on the receiver. The superheterodyne receiver is likewise SAW based with a very low average current consumption of approximately 1 mA. This outstanding feature is achieved by a standby concept in conjunction with a special circuit arrangement and an application specific Integrated Circuit.

The standby concept minimizes the current consumption of the receiver by utilizing the fact, that some functions are not permanently required. Therefore two receiver modes exist. First in the standby mode only those parts are turned on which are needed to detect the presence of a relevant signal, and if necessary to switch the receiver to the active mode. In this second mode the remaining components, which are needed for further signal processing, are enabled and current consumption is consequently increased.

The special circuit arrangement consists in the stacking of circuit stages for current reduction. This DC stacking appears on the one hand inside the tuner, which is realized using special discrete UHF transistors, and on the other hand in the cascading of the entire tuner with the remaining IF and baseband parts, which are covered by a single IC.

This monolithic IC in bipolar technology includes all necessary parts from IF signal processing to data output. In detail these are standby power control, IF amplifier, FM demodulator with adjustable discriminator bandwidth, logarithmic received signal strength indicator suited as an AM demodulator, high performance operational amplifier to realize a signal adapted baseband filter and a clamping comparator for additional noise suppression and data regeneration.

The performance of the described system is discussed by using measurement results of realized universal 433.92 MHz transmitter and receiver modules. A prospect of possible further developments will round off this presentation.

INTRODUCTION

In the present age of modern communication and increasing mobility we recognize a raising need for remote control systems. Reasons for using wireless systems are numerous and can not only be for comfort, versatility and flexibility but also for safety and cost savings. This is valid for various applications, as keyless entry systems for cars and buildings, alarm and security systems, domestic installation and wireless data transfer systems.

Recently in some areas low-power radio links are replacing infrared systems. Especially in the car market, which was the initial target for us, infrared systems experienced transmission problems due to dirt, ice and snow. Nowadays often the car's windows are additionally shaded to reduce excessive heating of the car interior. Unfortunately the shading attenuates the IR transmission of the remote control systems just as much as the emission from the sun.

RF systems operating in the UHF band are not restricted to the line-of-sight coverage of optical systems due to diffraction and reflection of radio waves at edges and conductive surfaces, as well as their capability to penetrate dielectric materials. This becomes apperent in an even illumination of space under complicated spatial circumstances as in buildings. Also the necessity to aim with the transmitter at the receiver is removed, because the commonly used small low gain aerials show an almost perfect omnidirectional radiation pattern. The range of the RF system can not be well defined because of the said propagation characteristic and due to additional polarization losses. These may vary from zero up to approximately 20 dB depending on the relative orientation of the transmitter and the receiver antennas.

As has been shown, IR as well as RF systems have advantages and drawbacks and therefore they are likely to co-exist. A more detailed comparison of the two systems can be found in [1].

SYSTEM CONTEMPLATIONS

To be able to appraise a system, one needs to know the boundary conditions and objectives, it is based upon. So every developer of a remote control system must be aware of his special requirements. The mere attempt to expound all possible requirements would be beyond the scope of this paper. Nevertheless we will not fail to mention some marked points, which seem to be relevant for most applications. Customers usually keep their eyes on range, safety in operation, current consumption, response time, size of the system's components and last but not least of course the price. Additionally the legal regulations in the particular country has to be considered.

From the boundary conditions technical attributes can be derived such as used frequency band, transmitter power, receiver sensitivity, modulation system, data rate and coding techniques. Most of these aspects depend on each other and some of them will be discussed in the subsequent explanations.

To get an overview let us first look at the block diagram (see figure 1). To simplify matters we consider an unidirectional transmission system. Therefore we need only one transmitter and a single receiver. Nevertheless most of the following considerations apply also to multidirectional systems.

Both transmitter and receiver can be subdivided into a digital and an analog section. The digital part of the transmitter encodes the information to a serial bit stream which can be modulated upon a RF carrier. This is done in the RF transmitter unit.

Vice versa in the receiver module the seriell data signal is recovered and the subsequent decoder makes the transmitted information available at its control outputs. The frequency of the radio link in our example is 433.92 MHz but any other frequency in the UHF range can be used after minor modifications of the RF part of the transmitter and the tuner of the receiver.

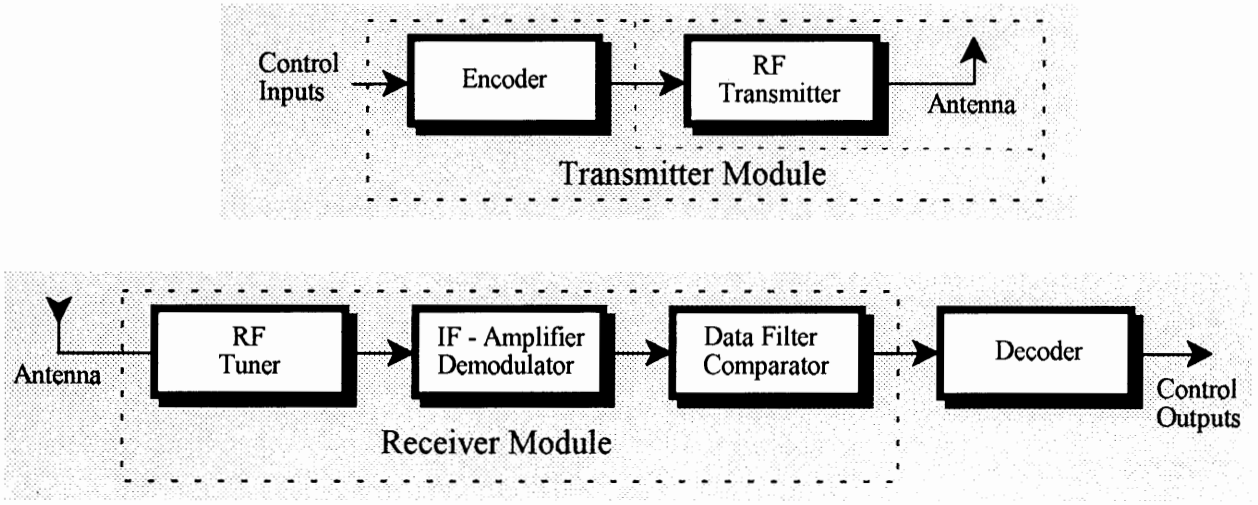


Figure 1: UHF - Remote Control System

The benefits of the UHF range become obvious by a study of the radio wave propagation versus frequency. For simplification we assume free space propagation and consider only the far field region. Referring to a transmission at a frequency f, respectively a wavelength λ, the received power P_R in a distance d from the transmitter, with output power P_T and an antenna gain G_T referred to an isotropic radiator, respectively G_R on the receiver side is according to reference [2]

$$P_R = P_T \cdot \frac{\lambda^2}{(4 \cdot \pi \cdot d)^2} \cdot G_T \cdot G_R \ . \qquad (1)$$

The logarithmic attenuation ratio L_0 for free space propagation is defined as

$$\frac{L_0}{dB} = -10 \cdot \log \frac{P_R}{P_T} = 32.5dB + 20 \cdot \log \frac{d}{km} +$$

$$+20 \cdot \log \frac{f}{MHz} - 10 \cdot \log G_T - 10 \cdot \log G_R \ . \qquad (2)$$

Taking the widespread demand for small size into account, a small loop antenna seems to be a good choice. The pattern of such an antenna is equal to that of a Hertzian dipole with a gain of $G = 1.5$. Supposing the transmitter, as well as the receiver antennas, are to be of that kind ($G_T = G_R = 1.5$), we obtain from equation (2)

$$\frac{L_0}{dB} = 29.0dB + 20 \cdot \log \frac{d}{km} + 20 \cdot \log \frac{f}{MHz} \ . \qquad (3)$$

Next the total radiated power P_T of such a small loop of w turns tuned with a parallel capacitor is deduced

analogically to that of an electrical Hertzian dipole [3]. Assuming a spherical coordinate system, electric and magnetic intensities are

$$H_\vartheta = H_{\max} \cdot \sin\vartheta = \frac{2 \cdot \pi \cdot w \cdot A}{\lambda} \cdot \frac{I}{2 \cdot \lambda} \cdot \frac{\sin\vartheta}{r} \cdot e^{-j \cdot \frac{2 \cdot \pi \cdot r}{\lambda}} \quad (4)$$

and

$$E_\varphi = E_{\max} \cdot \sin\vartheta = -\frac{\pi \cdot w \cdot A \cdot I}{\lambda^2} \cdot \frac{\sin\vartheta}{r} \cdot Z_0 \cdot e^{-j \cdot \frac{2 \cdot \pi \cdot r}{\lambda}} \quad (5)$$

related by the free-field characteristic impedance Z_0

$$E_\varphi = -Z_0 \cdot H_\vartheta \ . \quad (6)$$

The surface integral of the power density S yields the total radiated power P_T

$$P_T = \oiint S \cdot dO = \frac{1}{2} \cdot \oiint E_\varphi \cdot H_\upsilon \cdot dO = \frac{1}{2} \cdot \oiint \frac{E_\varphi^2}{Z_0} \cdot dO \ . \quad (7)$$

Substitution of the electric intensity (5) and solving the integral yields

$$P_T = \frac{E_{\max}^2}{Z_0} \cdot \int_0^\pi \sin^2\vartheta \cdot 2 \cdot \pi \cdot r \cdot \sin\vartheta \cdot r \cdot d\vartheta =$$

$$= 2 \cdot \pi \cdot r^2 \cdot \frac{E_{\max}^2}{Z_0} \cdot \int_0^\pi \sin^3\vartheta \cdot d\vartheta = \frac{8}{3} \cdot \pi \cdot r^2 \cdot \frac{E_{\max}^2}{Z_0} \quad (8)$$

with

$$E_{\max} = \frac{2 \cdot \pi \cdot w \cdot A}{\lambda} \cdot \frac{I}{2 \cdot \lambda} \cdot \frac{1}{r} \cdot Z_0 \cdot e^{-j \cdot \frac{2 \cdot \pi \cdot r}{\lambda}} \quad (9)$$

and

$$|E_{\max}| = \frac{\pi \cdot w \cdot A}{\lambda^2} \cdot \frac{I}{r} \cdot Z_0 \ . \quad (10)$$

Hence

$$P_T = \frac{8 \cdot \pi^3 \cdot w^2 \cdot A^2 \cdot I^2 \cdot Z_0}{3 \cdot \lambda^4} \quad (11)$$

The Quality Q of the resonant circuit determines the resonance step-up of the loop current. With the impressed output current I_T from the transmitter to the antenna the effective loop current is equal to

$$I = I_T \cdot Q \quad (12)$$

Furthermore the area A of the circular loop with a diameter D is

$$A = \frac{\pi \cdot D^2}{4} \ . \quad (13)$$

Herewith we get

$$P_T = \frac{\pi^5 \cdot w^2 \cdot Z_0}{6} \cdot \left(\frac{D}{\lambda}\right)^4 \cdot {I_T}^2 \cdot Q^2 \ . \quad (14)$$

Substituting P_T from (14) in (1) we derive

$$P_R = \frac{\pi^5 \cdot w^2 \cdot Z_0}{6} \cdot \left(\frac{D}{\lambda}\right)^4 \cdot {I_T}^2 \cdot Q^2 \cdot \frac{\lambda^2 \cdot G_T \cdot G_R}{(4 \cdot \pi \cdot d)^2} \quad (15)$$

and with the assumption $G_T = G_R = 1.5$ (two small single turn loop aerials) finally

$$P_R = \frac{3 \cdot \pi^3 \cdot w^2 \cdot Z_0}{128 \cdot d^2} \cdot \frac{D^4}{\lambda^2} {I_T}^2 \cdot Q^2 \ . \quad (16)$$

As we can see from this formula, received power is directly proportional to Q^2 and D^4, whereas inversely proportional to λ^2. This equation is only valid, if the diameter D of the loop is small compared to the wavelength λ. Furthermore Q is not independent of D and λ. Particularly losses due to skin effect increase with frequency and reduce Q. Therefore owing to circumstances a practical optimum does exist.

Exemplary the total transmitted and received power will be calculated at 40 MHz, 433.92 MHz and 2400 MHz, because these are frequently used bands. The corresponding Q values are roughly estimated to 100, 60 and 10. Assuming D = 1 cm and I_S = 2 mA, the transmitted power P_T at the above mentioned frequencies is -56, -19 and -5 dBm whereas the received power P_R in a distance d = 20 m will be -83, -67 and -68 dBm respectively. This applies to free space propagation and shows that higher frequencies are favourable when using such a small antenna.

In practical operation some additional factors influence the propagation characteristic. Diffraction and reflection of radio waves at edges and conductive surfaces as well as their capability to penetrate dielectric materials is frequency dependent. RF is shielded by metallic structures if the size of the gaps and slots of the structure are small compared to the wavelength. This fosters higher frequencies as well. On the other side, if one bears in mind, that propagation losses due to H_2O absorption and reflections by dielectric layers (e.g. window panes) are increasing rapidly at frequencies above 2 GHz, the UHF range reveals to be the best frequency choice for our purposes. Moreover the low absorption of radio waves in the UHF band by H_2O molecules is beneficial because this pays regard to human protection.

However, the formulae from above can be used to get a course impression of the required receiver sensitivity for a

given transmitter design and a claimed minimum operating range. The conformity of the levels, calculated according to the above valuations (15,16), with experimental results is good. Under the given circumstances, among others the operating frequency of 433.92 MHz, and considering additional losses due to antenna shielding problems and polarisation mismatch a typical operation sensitivity of -80 dBm is marginal for a reliable and trouble free operation.

TRANSMITTER

The transmitter module contains not only the RF transmitter but also either a data and control interface or even a µC or µP for encoding (see fig.1). Concerning the transmitter we will not go into details because one can find several realization proposals in various application notes for instance of SAW resonator suppliers [4],[5].

In a simple design it consists only of one single stage, a SAW based oscillator whose inductance of the tank circuit is realized as a loop and acts also as antenna. When designing the RF transmitter equation (14) is important. Let us direct our attention to the parameter Q. A doubling of Q yields a four times larger total transmitted power.

Another benefit of high Q is less obvious but as least as important. The higher the quality, the greater the ratio of the effective current of the fundamental wave compared to the current of the harmonics, because the resonance step-up appears only at the resonance frequency of the antenna circuit. Therefore the suppression of radiated harmonics is essentially determined by the quality of the aerial.

The RF transmitter can be amplitude modulated by switching the base voltage of the transistor as well as frequency modulated by the help of a varicap in the tank circuit (see fig. 2 and 3).

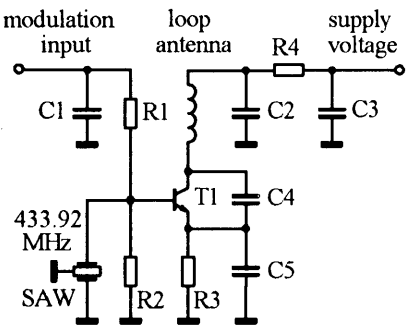


Figure 2: UHF - Transmitter, AM version

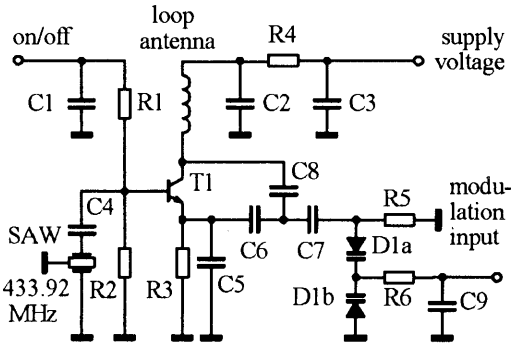


Figure 3: UHF - Transmitter, FM version

RECEIVER

One of the most stringent requirements is the very low current consumption of the receiver. At first claimed out of the quarter of car manufaturers the demand for an average current consumption of maximal 1 mA was adopted in several other fields of application, for instance to supply the receiver from a mains independent solar buffered accumulator.

Principle of operation

To realize such a receiver two principles of operation are favourable:

Using the polling method, the receiver is periodically switched on for short times. During the active periods, current consumption can be higher than 1 mA whereas in the interim the receiver is entirely turned off. Herewith the average current consumption depends on the duty cycle, which is the ratio of times when the receiver is active compared to when it is switched off. Unfortunately this duty cycle determines also the reaction time of the system. This means, that the non active intervals can not be enlarged over the maximal permissible response time of the system. In addition the active period can not be made arbitrary short, because during this time the receiver has to decide whether a relevant signal is being received. In that case the receiver remains in the active mode, at least for the expected duration of a potential transmitted signal. This method is very favourable with respect to system sensitivity, because the receiver has its maximum sensitivity when it is active.

If the reaction time is a critical parameter, a second conception called wake up method, is more advantageous. Also here two modes exist. In the low power standby mode with a current consumption of about 1 mA only those parts are turned on, which are necessary to detect

the presence of a possibly relevant signal. If such a signal is detected, which means that the received signal strength exceeds a given threshold, the receiver itself switches on (wakes up) the remaining parts which are necessary for signal processing. In this active mode, current consumption is increased. After an adjustable hold-time, in the course of which the signal strength is below the threshold, the receiver automatically switches back to the standby mode. The distinctive feature of this system compared to the polling system lies in a reduced sensitivity in the standby mode. To avoid false alarms, which raise the average current consumption for no purpose, the wake up circuit shall not be triggered by noise or weak interference. Therefore the wake up threshold, respectively the time constant of the integrator in the wake up circuit which determines the necessary energy of a trigger signal, must not be too small. A reduction of the false alarm probability implies unfortunately a decrease of the detection probability.

A decoder, receiving permananently a random bit sequence, will sometime detect a valid telegram. The statistic probability of such an event, caused by noise, interference or similar signals, encreases with the frequency and duration of the times, when the receiver is in the active mode. The wake up concept therefore helps to reduce redundance in the transmitted code.

The TEMIC receiver modules can support both conceptions. It is possible to use the wake up concept alone or to poll the receiver additionaly. Of course it is also possible to switch the receiver to continous operation, if the increased current consumption can be permitted. Therefore an application dependent optimization of response time and sensitivity of the system can be done. A less obvious benefit of this feature is the possibility to implement a distance dependent functionality.

Constructional details of the receiver

Our approach to the low current receiver is not only the previously commented standby concept but also a special circuit arrangement consisting of the stacking of circuit stages for current reducing. This DC stacking appears on the one hand in the cascading of the entire tuner with the remaining IF and baseband parts, and on the other hand in the tuner itself (see fig. 4). In the subsequent sections we will describe the circuitry of the receiver. Corresponding to the signal flow, first of all we will present the design of the RF tuner followed by an introduction into the IF and baseband parts.

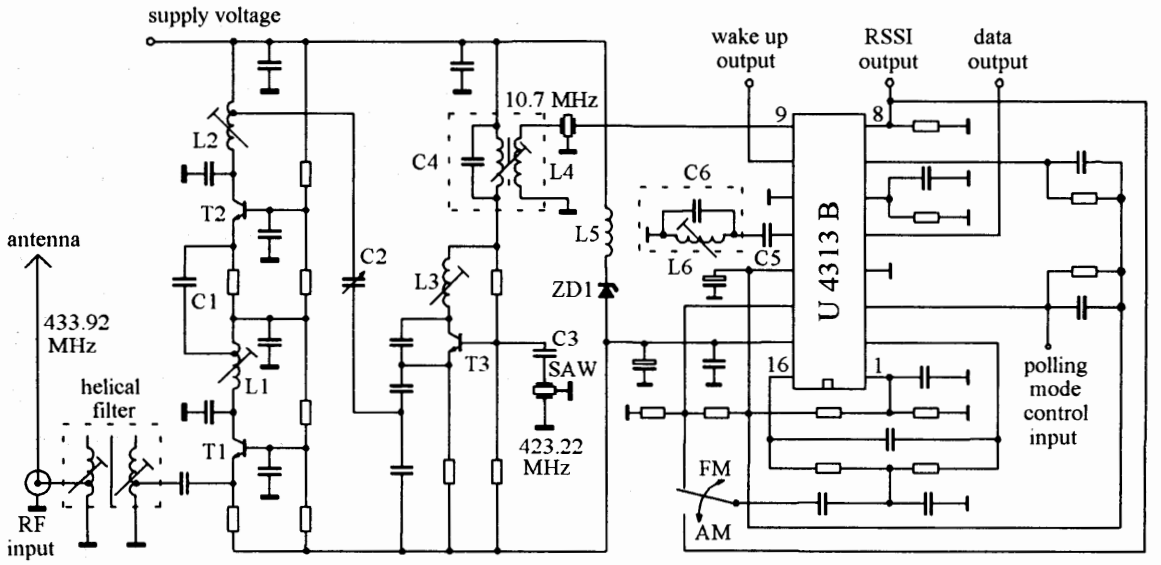


Figure 4: Low current UHF - Remote Control Receiver

Coming from the antenna input with a characteristic impedance of 50 Ω the received signal passes a double-tuned miniature helical filter. This preselector provides good far-off selectivity, improves image rejection and makes the subsequent prestage insensitive to deviations of the antenna impedance. The two preamplifiers in common base circuit are DC cascaded. The grounded base amplifiers are distinguished by a high reverse isolation and guarantee a good suppression of the local oscillator signal to the antenna input. The LO level as well as spurious response and harmonics are less than -65 dBm at any port of the receiver module, which is encased in a tin plate cabinet for shielding. In the tuner special low noise, low current, low voltage bipolar transistors are applied. The transition frequency of the used S 852 T is 3 GHz for a given collector current of 0.5 mA, which provides a gain of about 10 dB per stage at 433.92 MHz.

In the following self-oscillating mixer the signal is converted to the sole intermediate frequency (IF). The large-signal characteristic of the receiver can be improved by using a master-excited mixer whereby the complexity of the circuitry and its power consumption are slightly increased. By means of a SAW resonator as frequency-determining element, the the local oscillator is oscillating at a high frequency in the UHF band and therefore no frequency multiplication is necessary. This results in a tuner free of spourious resonances at a minimal expense.

The IF is choosen to 10.7 MHz as there are various low cost components such as transformers, resonators and filters available. The filter bandwidth should be choosen with regard to the tolerances of the SAW resonators in transmitter and receiver. A worst case appraisal of the frequency tolerance yields ±130 kHz for one SAW, taking into account manufacturing tolerances of ± 75 kHz, temperature variations (-40°...+80°C) of ±50 kHz and a drift due to component ageing of ±5 kHz. The frequency tolerance assessment of SAW based oscillators must include additionally the effects of battery-voltage variations, hand capacitance and shock. We recommend to use ceramic filters with a bandwidth of 350 kHz, as used for instance in large number of pieces in US stereo broadcasting receivers.

As shown in fig.4, the voltage drop at the tuner is clamped to approximately 5.1 V by a zener diode. This diode keeps the operating points of the transistor stages in the tuner constant although the total current consumption depends on the mode of the receiver. In fact the diode takes over the differential current between active and standby mode.

The tuner works without automatic gain control (AGC) to avoid settling time problems especially in AM systems. Therefore the dynamic range of the subsequent stages must be kept in view.

Special care has to be taken when designing the layout of the printed-circuit board. This is necessary to avoid parasitic oscillations and coupling by ground lines.

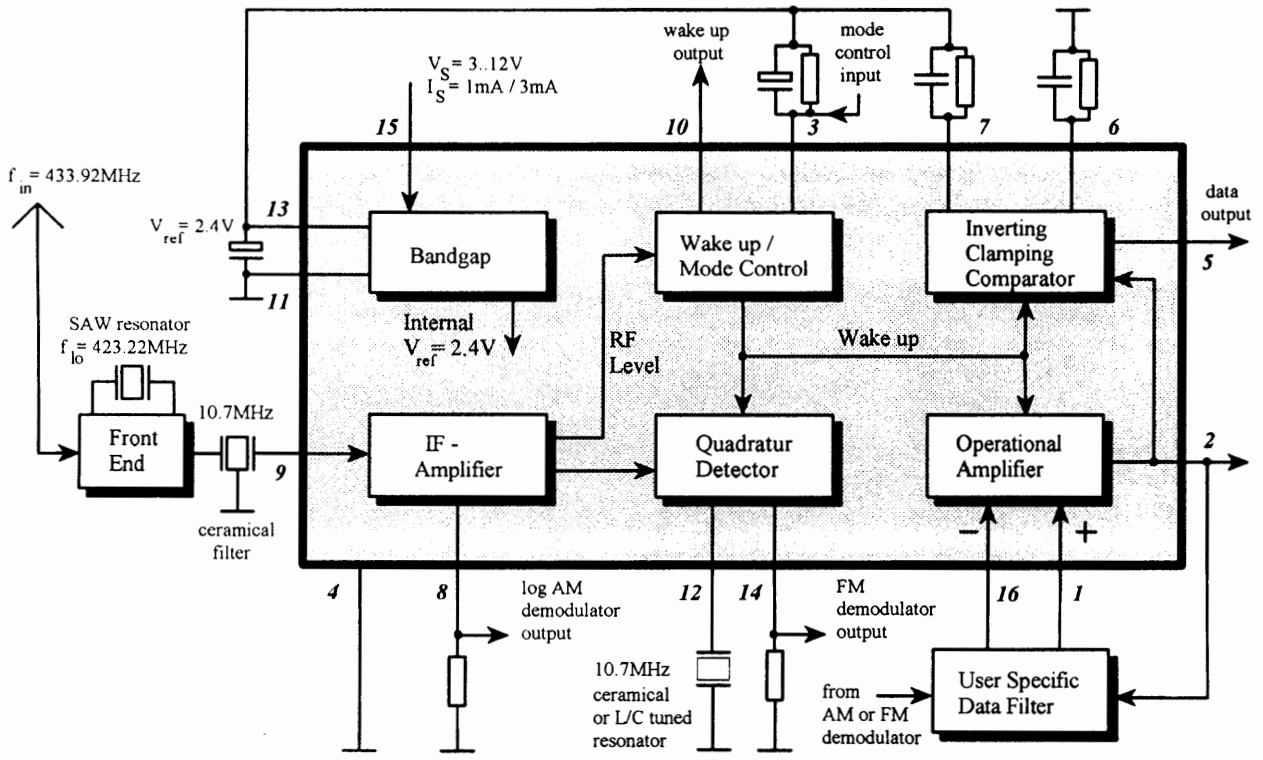


Figure 5: U 4313 B in a superhet receiver concept

We will now concentrate on the remaining IF signal processing, demodulation and data shaping. All these functions including the wake up / mode control circuitry are carried through by a single integrated circuit. For this purpose TEMIC provides a family of ICs in bipolar technology, which are available in DIP as well as in SO case. We will take as an exemple the U 4313 B, which is very universal as will be shown. The presentation will be confined to the principle operation and we will not discuss all electrical parameters. These can be found in great detail in the corresponding data sheets and application note [6].

As described earlier, the tuner voltage is clamped to about 5.1 V. Assuming the claimed voltage range of the power supply to be from 9 to 15 V, the remaining voltage for the IF and baseband parts varies from 3.4 to 9.4 V. The operating range of the used integrated circuit IC is 3 to 13 Volts and therefore the claimed power supply range can be guaranteed. The reference currents and voltages of the various parts of the IC are controlled by a bandgap circuit. This is the basis for a largely voltage and temperature independent performance. The very stable reference voltage of 2.4 V is externally available and can be used to supply peripheral components such as the decoder.

The IF signal comes from the tuner through a ceramic filter to the integrated IF amplifier, whose input impedance is 330 Ω and therefore well matched to most ceramic filters.

The U 4313 B is suited for FM as well as AM demodulation. The dynamic range of the logarithmic received signal strength indicator (RSSI) is more than 60 dB (see figure 6), which is enough as has been proved in practical investigations. This RSSI current output is predestined to act as an AM detector and so an AM receiver without any gain control and settling time problems can be realized. The FM demodulator stage needs either a single ended ceramic resonator or a LC tank circuit. At the latter the S-shaped demodulator characteristic can be aligned with respect to center frequency, steepness and bandwidth (compare with figure 8). Therefore tolerances of the receivers SAW resonator can be equalized to some extent and additionally the demodulator can be easily matched to the bandwidth of the IF filter just as to the deviation of the transmitter.

The additional expenditure of the FM receiver compared to the AM is low and consists in the described discriminator filter plus two resistors.

The FM demodulator is only switched on, if the received signal strength is above the threshold of the wake up circuit. The threshold referred to the input of the IF amplifier is typically 40 dBμV and temperature independent. The delay time as well as the hold time of the wake up function can be externally adjusted. Peripheral components as the decoder can be controlled by the wake up output and thereby incorporated into the standby concept. Jointly with the FM demodulator two other functions of the IC, an operational amplifier and a clamping comparator are turned on.

With the internal high performance operational amplifier a signal adapted active filter can be realized. The amplifier's power-gain-product is about 4 MHz. Therefore even second order filter for high data rates can be realized to reduce the basebands system bandwidth. Important for the dimensioning of the data filter is not only the data rate but also the code to be transmitted. Recommendable is a code without DC component. This is a code with an equal probability of high and low states, as for instance a Manchester code, which can be generated by a logical exclusive-or operation of the data signal with a clock of doubled frequency.

When the received signal is as far as possible cleared of distortion and noise it has to be converted to a digital bit stream. Therefore a binary quantization has to be carried out. For this data shaping a clamping comparator is implemented. The reference level, which is needed as decision threshold, is generated as follows. Positive and negative peaks of the received signal are stored in two RC circuits. The arithmetical mean of these two voltages forms the threshold. By this clamping to peak values an effective suppression of low frequency interference as hum can be achieved. An optimization of the suppression is possible by the proper adaption of the time constants. The difference of the peak values controls the hysteresis of the comparator. This provides an amplitude depending noise suppression. The open collector output of the comparator delivers a binary data signal with very steep flanks and a level, which can be easily adapted to that of the subsequent decoder. The pin compatible U 4311 B-C delivers a data signal, which is inverted compared to that of U 4313 B. So respective customer demands can be accomplished instantaneously and the designer of the data filter is free whether to choose an inverting or non-inverting type.

EXPERIMENTAL PROCEDURE

We will now look at the experimental investigation of the system performance. First the AM version of the receiver is examined, then the FM receiver is studied and finally a comparison of the two systems is made.

Figure 6 shows the temperature dependence of the static RSSI characteristic. Especially at low levels, which is the area of the wake up threshold, as good as no temperature dependence is evident. This region determines the sensitivity of the receiver, which is therefore almost independent of temperature variations. The straight part of the characteristic extends to approx. 95 dBμV. Compression effects, occuring at higher levels, do not

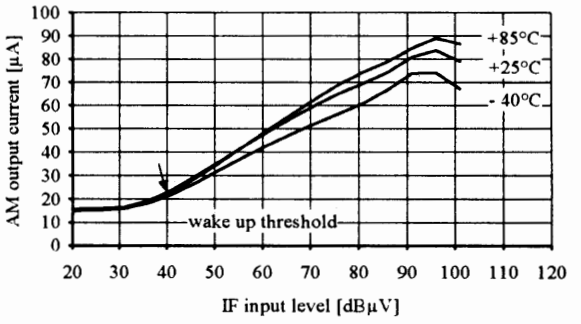


Figure 6: RSSI / AM output current versus IF input level and temperature

disturb the digital system because at such high signal levels the signal-to-noise ratio usually is very high. This is proved by the corresponding measurement and can be seen in figure 7, which will be discussed later.

The RSSI output follows variations of the receiver's input level virtually without any delay. Therefore the data rate can be raised up to several hundred kBauds. At such high rates merely the IF filter has to be replaced by one with a larger bandwidth. However the operational amplifier is still well suited to realize an effective data filter.

In the tested AM receiver a data filter with a voltage gain of 20, a high-end cutoff frequency of 2 kHz and a low frequency cutoff of approx. 20 Hz is applied. The large gain is necessary to provide a signal amplitude, which is sufficient to overcome the hysteresis of the subsequent clamping comparator, when weak signals are received. Diagram 7 reveals the results of a signal-to-noise measurement referred to the output of the operational amplifier, which is simultaneously the output of the data filter. We assume the modulation depth to be 100%, which means that the low bit of the data signal is characterized by no RF signal and the high bit by the corresponding RF input level.

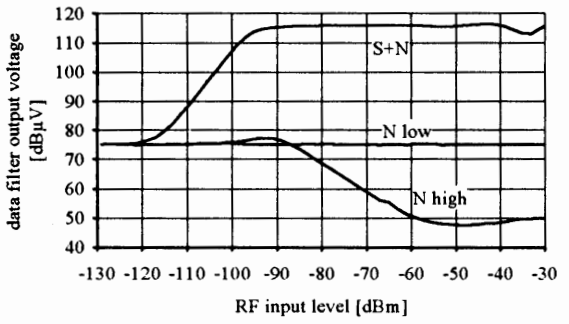


Figure 7: (S+N) / N ratio at the 2 kHz data filter output of the AM receiver, RF is 433.92 MHz, AM modulation depth is 100 %, AF is 1 kHz sinus

To define a signal-to-noise ratio in a digital AM system, it is necessary to distinguish between two different amounts of noise. The noise in the low state N_{low} results from the thermal noise at the receiver input plus the noise originated from the receiver, when no input signal is applied and the gain of all stages is maximal. The noise N_{high}, which appears if a high bit of the data signal is transmitted, can be measured with an unmodulated carrier. While raising the level of the carrier from -105 dBm to approx. -95 dBm, noise increases slightly due to the level dependent directivity of the logarithmic AM detector. With higher values of the input level the gain of the IF amplifier and therefore also the noise decreases. The signal plus noise curve S+N is measured while a RF carrier, which is amplitude modulated with a 1kHz sinusoidal signal, is applied to the RF input. The noise floor of the used Audio Analyzer is 30 dBµV and herewith its influence to the accuracy of the measurement can be neglected.

The S+N/N ratio is the difference between the S+N and the N curves. This ratio is a standard of the signal quality. It increases from 0 at the limiting sensitivity of -120 dBm to more than 60 dB referred to N_{high}, respectively 40 dB referred to N_{low}, at an input level of -55 dBm. In fact the effective S+N/N ratio lies between those two values and depends on the probability of the low and the high bits. The maximum signal-to-noise ratio is limited by the noise respectively the dynamic range of the receiver. At all S+N/N measurings only thermal noise which can be considered as white Gaussian noise is present. Therefore the sensitiveness of AM systems to pulse noise as for example ignition noise becomes not evident.

As has been discussed previously, the FM discriminator filter should be tunable. The discriminator output voltage varies with the input frequency between 0.1 V and 2.3 V with its mean value of 1.2 V at the centre frequency. The demodulator bandwidth depends mainly on the difference of the series and the parallel resonance frequency of the discriminator filter. Hence the bandwidth can be adjusted by changing the series capacitor C5 and retuning the center frequency with L6 (labels according to figure 4). The S-shaped curves for two different filter configurations are plotted in figure 8 .

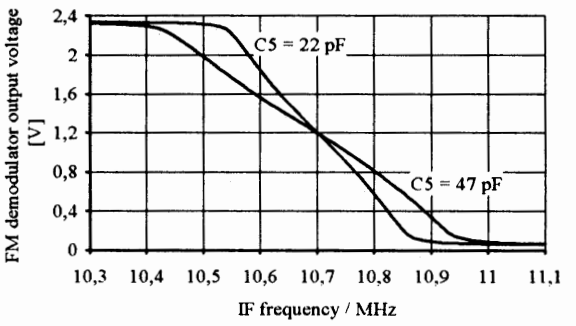


Figure 8: FM demodulator frequency response for different values of C5

The next figure 9 presents the signal-to-noise ratio of the FM receiver versus the RF input level. The measuring was carried out in analogy to that at the AM receiver. The bandwidth of the used data filter was choosen equal to that of the AM system. Its gain was reduced to a value of 3 because the FM demodulator delivers a higher signal amplitude, which is additionally almost independent of the RF input level. The limiting sensitivity is -110 dBm and therefore worse compared to that of the AM system, but the S+N/N ratio encreases more rapidly with the input level due to the threshold effect of the FM system. Here one benefit of the FM system becomes obvious: the level of the RF signal and therefore also the noise is independent of the transmitted information. Therefore the S+N/N ratio at higher input levels is better than that of the AM receiver.

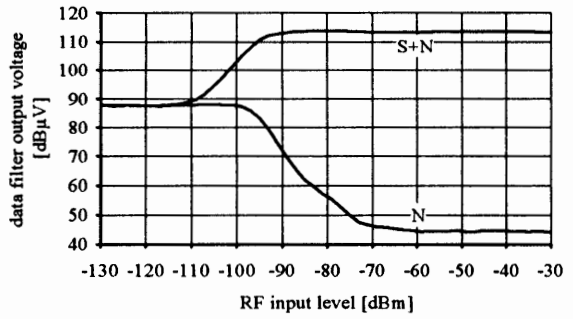


Figure 9: (S+N) / N ratio at the 2 kHz data filter output of the FM receiver, RF is 433.92 MHz, FM deviation is 22.5 kHz, AF is 1 kHz sinus

To characterize the quality of a digital data transmission the specification of a bit error rate (BER) is very common. This is the probabilty of a wrong bit at the output of the receiver. At systems with a limited bandwidth (what applies to every real system), the BER depends on the transmitted bit stream. In systems with bandpass characteristic not only the data rate is limited by the system's high-end cutoff frequency but also the low frequency cutoff is important. The latter limits the maxium number of successive equal bits. Therefore the use of a 0-1-0-1 sequence as a test signal does not reveal the real performance of the system. A pseudo random sequence (PRS) is recommended to be used instead. This is a sequence of a given length of 2^n-1 bits which is transmitted periodically. The distribution of the bits in the sequence are quasi random and the maximum number of successive equal bits is n. The probability of occurence of the low and the high bit is almost equal but never identical, because the sequence has an odd number of bits.

If the complete baseband signal processing functions are DC coupled, the optimal threshold of a binary decision element is the mean value of the low and the high bits' amplitude. This applies as long as no interference is present. In an AC - coupled system in particular the transmission of many successive equal bits leads to a so-called baseline wandering in the decision element, what means that the optimal threshold shifts. The amount of this baseline wandering depends on the the low-end cutoff frequency in proportion to the ratio of data rate to number of successive equal bits. The carrying out of a BER measurement by using a PRS as test signal is well suited to determine the influence of the baseline wandering on the receiver performance. In our case the low-end cutoff frequency can be adapted by the value of the coupling capacitor which connects the datafilter to the output of the demodulator. An optimization of the complete data filter should be done by the help of the eye pattern at its output.

The data filter and the subsequent clamping comparator are DC coupled. The time constants of this comparator must be large compared to n times the length of one bit. The purpose of its gliding threshold is to suppress only low frequency distortions.

The time of decision, whether a right or wrong bit was decoded is set to the middle of the bits. The BER measurement equipment compares the modulation signal of the transmitter with the signal at the output of the clamping comparator and counts the number of faults per time.

With this BER measurement equipment the dependence of the receivers' sensitivity referred to the modulation depth of the AM transmitter respectively the deviation of the FM transmitter is examined. A fixed BER of 10^{-3} is taken as a basis. The RF input level corresponds to the carrier peak level at the output of a signal generator, which must be independent for all values of modulation depth respectively frequency deviation. This means, that the AM modulator must be clamped to the high level of the modulation signal, as done for instance at the transmission of TV signals.

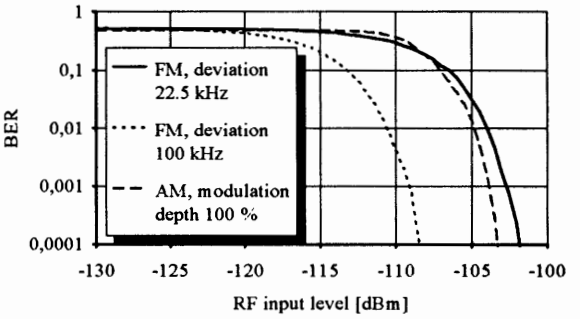


Figure 10: Bit Error Rates of a 2 kbit/s PRS of length 2^5-1

As can be seen in fig. 11 and 12, the AM System using a modulation depth of 100% achieves the claimed BER at lower input levels than the FM system using 22.5 kHz deviation. The FM system is superior to the AM system if the used deviation is more than 35 kHz. At a deviation of 100 kHz, the margin is about 5 dB. This does not surprise because the FM system exploits the system's IF bandwidth of 350 kHz much better than the AM system. Further the FM is superior to AM by principle. The derivation of this theoretical 3 dB margin can be found in [7].

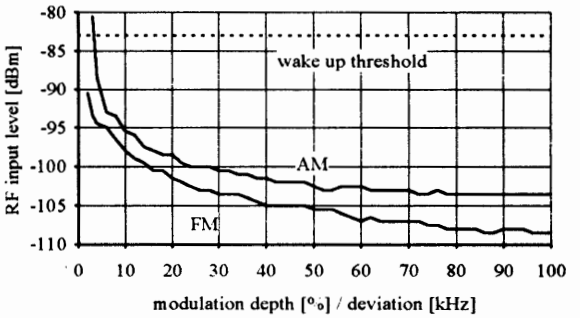


Figure 11: Sensitivity of the AM and FM systems for a 2 kbit/s PRS of length 2^5-1 and a given BER = 10^{-3}

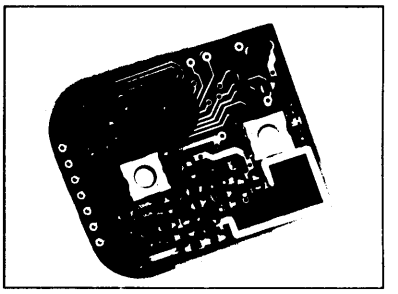
SUMMARY OF THE SYSTEM PERFORMANCE

General:

- RF characteristics according to FTZ 17TR2100, will fulfill the regulations of most countries, please request corresponding specifications
- Operating frequency 433.92 MHz (can be adapted to other frequencies in the UHF range)
- Modulation FM or AM
- Ambient operation temperature -40 °C to +85 °C
- Fulfills requirements of international car manufacturers

Transmitter:

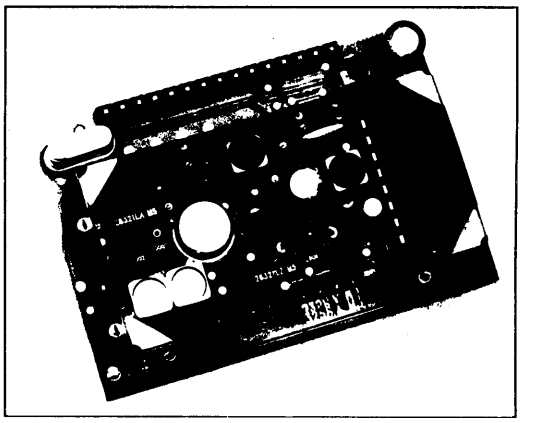
- Custom designed, characterized by performance and outlines
- Example incl. antenna, 4 bit µController and battery see picture 1 (6V, standby current of max. 0.5 µA, active current of max. 8 mA)
- Radiated power: approx. -20 dBm
- Spurious response / harmonics:
  less than -65 dBm up to 1 GHz
  less than -55 dBm above 1 GHz
- AM or FM operation depending on component assembling.
  AM: modulation depth approx. 90 %
  FM: Deviation approx. ±15 kHz
- Size: approx. 38 mm • 32 mm • 10 mm, custom specific solution with a reduced size of 38 mm • 25 mm • 8 mm exists



Picture 1: UHF - Transmitter, FM version

Receiver:

- Power supply: DC 9 V - 16 V, typical currents:
  1.0 mA using U 4311 B / U 4313 B standby mode (AM / FM)
  3.2 mA using U 4311 B / U 4313 B active mode (AM / FM)
  0.9 mA using U 4312 B standby mode (only AM)
  2.7 mA using U 4312 B active mode (only AM)
- AM or FM operation depending on component assembling
- Wake-up function: threshold approximately -83 dBm referred to the 50 Ω antenna input, delay and hold time adjustable
- Polling mode supported
- Output to activate peripheral circuitry e.g. decoding system
- Antenna jack makes customs specific antenna design and location feasible
- Data output for individual external data processing or optional µController on accessory board (see picture 2)
- Spurious response and harmonics less than -65 dBm (at any port of the RF module in a tin plate cabinet)
- Input sensitivity: AM: better than -100 dBm (see figure 7 and figure 10)
  FM: better than -100 dBm (see figure 9 and figure 10)
- Good out-of band rejection due to double tuned helical filter at RF input
- Size of the RF module: approx. 55 mm • 30 mm • 18 mm



Picture 2: UHF - Receiver, FM version, RF module on accessory board

FUTURE CONSIDERATIONS

Finally we give a prospect of possible further development. Due to the limited modulation capability of the actual SAW-based FM transmitter design, deviation is limited to less than ±20 kHz. Unfortunately the tolerance of the SAWs demand an IF-band-width of more than 250kHz. For this reason an increase of FM-deviation to about 100kHz will result in an improvement of the system-sensitivity of approximate 6dB (see figure 11). We intend to develop an PLL-based transmitter with better frequency tolerance and improved modulation capability [8]. Certainly semiduplex and fullduplex radio links will be needed for special applications and we intend to include this also in our future activities.

ACKNOWLEDGEMENT

The authors would like to thank the TEMIC subassembly division for making available receiver and transmitter modules and Dr. Sapotta and Mr. Bürgerhausen for general technical assistance and helpful comments. Moreover we would like to express our sincere appreciations to the colleagues in the development and application groups who gave us unlimited encouragement.

REFERENCES

[1] Sapotta, Bürgerhausen
Infrared or high-frequency transmission for car locking systems ?
TEMIC internal paper 1992

[2] Meinke, Gundlach
Taschenbuch der Hochfrequenztechnik
Springer-Verlag Berlin 1986, Vol. 1, H4

[3] Zinke, Brunswig
Lehrbuch der Hochfrequenztechnik
Springer-Verlag Berlin 1986, Vol. 1, pp. 339-346

[4] Niestroj, Zapsky, Lang
Kostengünstige und zuverlässige Fernsteuerungen durch OFW-Resonatoren
Siemens Components 4/90, pp. 142-145

[5] Vollers jr.
General-purpose SAW resonator oscillator for 300 MHz to 1000 MHz
RF Monolithics Inc. 1984, Application Note No.3

[6] Strohal, Bopp
UHF Remote Control System
TEMIC Application Note No.10

[7] Lüke
Signalübertragung
Springer-Verlag Berlin, 4th edition 1990, pp.167-197

[8] Boese, Gebauer
Kombiniertes Funksende- und -empfangsgerät mit einer PLL-Schaltung
Patent pending, reference P4201415.8

Matthias Bopp was born in Mosbach, Germany, on May 6th, 1964. He received his Dipl.-Ing. degree in electrical communication engineering from the University of Kaiserslautern in 1990. His Dipl.-Ing. research was the development and investigation of a coherent optical PSK homodyne receiver at ANT Bosch Telecom in Backnang. In the same year he joined the TELEFUNKEN electronic GmbH, meanwhile reorganized to TEMIC TELEFUNKEN microelectronic GmbH. He is engaged in the development of RF remote control systems and advanced Integrated Circuits. Mr. Bopp holds a radio amateur licence and is member of AMSAT.

Jürgen Strohal was born in Aalen, Germany, on June 17th, 1963. He studied electrical engineering, concentrating on communication techniques, at the University of Stuttgart. His diploma research was the improvement of an UV sensitive sensor read out by a CCD. He obtained the diploma in 1991 and joined the TELEFUNKEN electronic GmbH, where he is engaged in the application group and is envolved in the application of RF circuits. He is fond of languages and increases his knowledge on periodical journeys.

Comparison Of Path Loss Performance of a Leaky Feeder Cable vs. A Distributed Antenna

J. Ford, R. Perelman, D. Lang
Times Microwave Systems

Abstract
The use of a wireless system in an enclosed area may be inhibited by the lack of signal propagation through walls or in and around metal structures. This paper will compare the measured values of path loss for two systems of signal distribution designed to be part of a larger signal distribution system. The measurements were performed at 900 MHz. This paper will present relative parameters for the design engineer to use to configure an indoor wireless system.

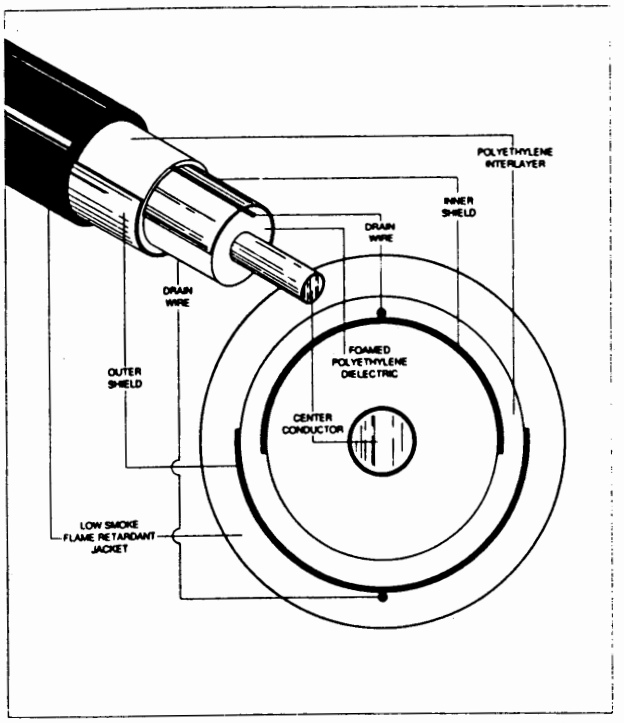
Introduction

A leaky feeder or radiating cable is an RF transmission line which is designed to couple the RF energy propagating its length to the environment. In so doing, it functions as a continuous antenna and is useful for providing RF coverage in enclosed environments, where point source antennas may have been used. A distributed antenna is a set of antennas fed by a single source used to provide RF coverage in enclosed areas. Examples of environments which cannot be effectively covered with point source antennas include tunnels, mines, metal hulled ships and metal framed buildings.

The low levels of energy emitted by radiating cables make them ideal for achieving coverage in limited areas, allowing frequency re-use. This is important because of the many competing demands for RF spectrum which makes efficiency of spectrum use an ever more pressing concern. The creation of mini-cells within buildings and coverage of limited areas for Wireless Local Area Networks are examples of applications where this characteristic of radiating cable can be usefully exploited. The purpose of this paper is to aid the designer of in-building communications systems by providing a comparison of the coverage performance of radiating cable and point source antennas within a building environment.

Types of radiating cables

Radiating cables are of two basic types--coaxial and triaxial. Coaxial types consist of coaxial cables with openings in the outer shield to allow coupling of RF energy to the environment. Within this category many different techniques are used by different manufacturers for forming openings in the outer conductor. One of the most common is to take a corrugated copper outer conductor and mill a continuous slot along the length of the cable. Another construction utilizes a foil outer conductor which is pre-punched with the coupling apertures. Another common cable utilizes loose braids or leaves off carriers on standard braided coaxial constructions. The radiating cable used in this comparison is a triaxial type where the outer conductor is in two sections separated by a polyethylene interlayer, Shown in figure 1.



Schematic for nu-Trac Triaxial Antenna Cable Patent Number 4339733

Figure 1.
Triaxial Radiating Cable

Applications of radiating cables

Radiating cables have been used in many different environments for many different types of communications systems. They have been installed in subway systems for two-way voice communications for public safety, for train control systems and to relay video information to the conductors to help in door control at stations. In hospitals, radiating cables have been installed to extend paging systems to underground tunnels and parking garages and to allow patients wearing monitoring equipment equipped with RF outputs to move about freely. The US Navy has installed radiating cables on virtually all of its ships as part of a system called Damage Control-Wire Free Communications (DC-WIFCOM) and for a shipboard

security system. Radiating cable was used for communications during the construction of the English Channel Tunnel and will be installed for the permanent communications system. Long road tunnels such as the Sumner and Calahan Tunnels in Boston are being furnished with radiating cable in order to allow the use of cellular phones by motorists traveling through them.

Experimental design

One of the areas where radiating cable has the greatest potential for contributing to productivity enhancement and cost savings is in manufacturing. In both office and plant environments, the use of Local Area Networks is allowing the transmission of data, correspondence and voice messages rapidly and efficiently between work stations. One recent trend is to make these interconnections without the requirement for hard wiring. This allows reconfiguration and relocation of equipment and personnel to be achieved more quickly and at lower cost. Wireless connections also allow equipment to be used in a portable fashion, while remaining interconnected to the network.

One of the problems in achieving a truly wireless network is the difficulty in achieving adequate RF coverage throughout a building. This study compares the coverage achieved with point source antennas and radiating cables in a factory environment. The results show that more complete coverage is achieved using radiating cable, which would result in more reliable operation of a wireless network.

Figure 2 shows the positions of two quarter wave monopoles that were mounted near the ceiling at P1 and P2 and the radiating cable location.

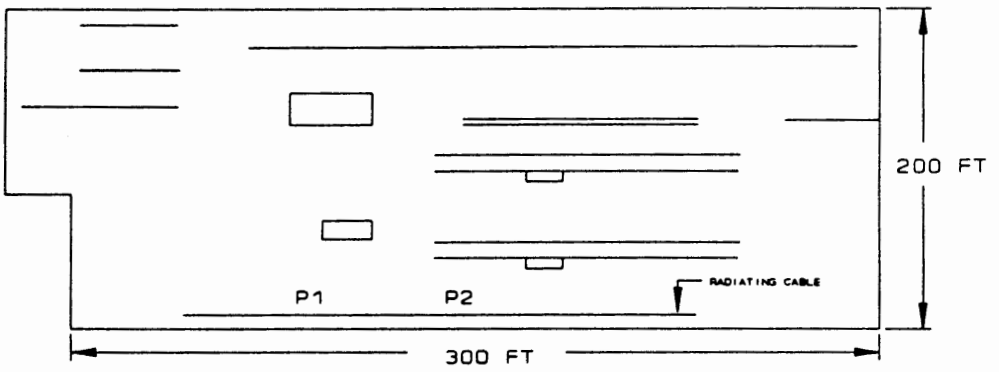


Figure 2
Test Area and Source Layout

The monopoles were fed by a ½" aluminum-foam cable which is commercially available. The monopoles were fed by coupling power off the ½" coax with taps. The lengths of coax used were 130ft. to the first tap 150ft between taps in the test area and 300ft after the second tap to feed a third tap in a separate building. For a total length of 480ft. The monopoles were connected to the feed line by a 16dB and a 10dB tap. The attenuation between the first two taps is 5.4dB. The monopoles were configured this way to function as part of a distributed antenna system that would also feed an area beyond our test area with equivalent signal strength. A loss budget is shown in Figure 3 giving the cable losses and the signal strength delivered to the quarter wave monopole.

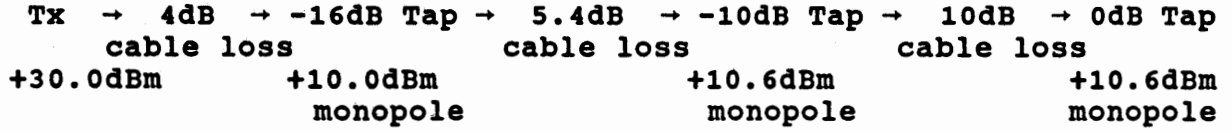


Figure 3.
Loss Budget for Distributed Antennas

The coupling values of the taps were selected to provide equivalent radiated power at each of the monopoles. Only the first two antennas were in the area that was evaluated. The third tap was in an adjacent building and was terminated in a 50 Ohm load for this test. The power level measured at the third tap was +10.6dBm.

The radiating cable ran along side the feed cable for the monopoles. The installation crew that installed both the Aluminum sheathed coax and the radiating cable had experience installing electrical conduit, phone lines, and datacom lines. The only special instructions given was that both cables for our test could not be bundled with any existing cables and would need to be clamped in place separately. A loss budget for the radiating cable is shown in figure 4.

Figure 4.
Loss Budget for Radiating Cable

The signal received by a half wave dipole was measured at 17 locations around the manufacturing area. The technique used to generate the path loss values is similar to that used by previous investigators[1]. The value used is the average of ten values taken evenly over a 20ft. length. The locations of the measurements were identical for each signal distribution technique. The receive dipole was held with horizontal polarization. Recent investigations in wireless communications have compared polarizations for antennas and showed linear vertical to be optimal[2]. Since we are comparing two signal distribution techniques in the presence of many conducting bodies, horizontal polarization was used for convenience. A comparison of optimal receive antenna polarizations for radiating cables is forthcoming.

Results

The average measured values of path loss for the monopoles and the radiating cable are shown in figures 5 and 6 respectively. The received signal strength fades predictably as the measurement point is taken a distance away from the sources. Figure 7 shows a plot of the path loss of each point, the points are randomly located.

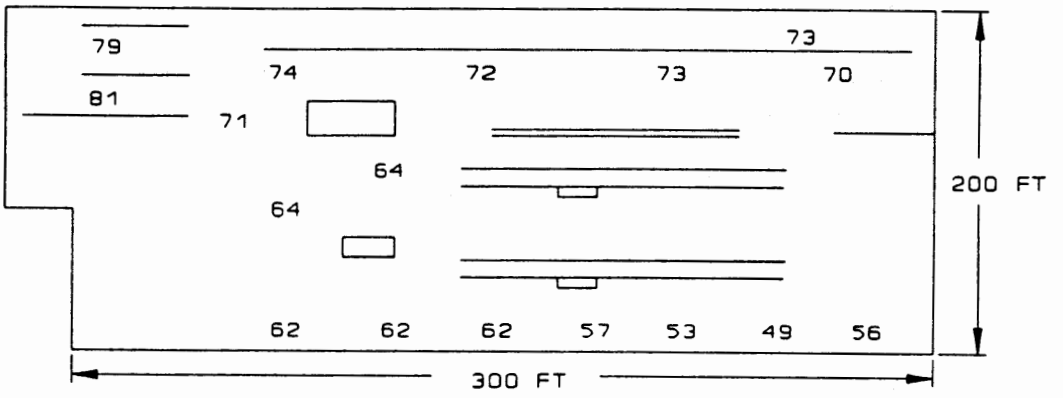


Figure 5.
Path Loss in dB for Distributed Antennas

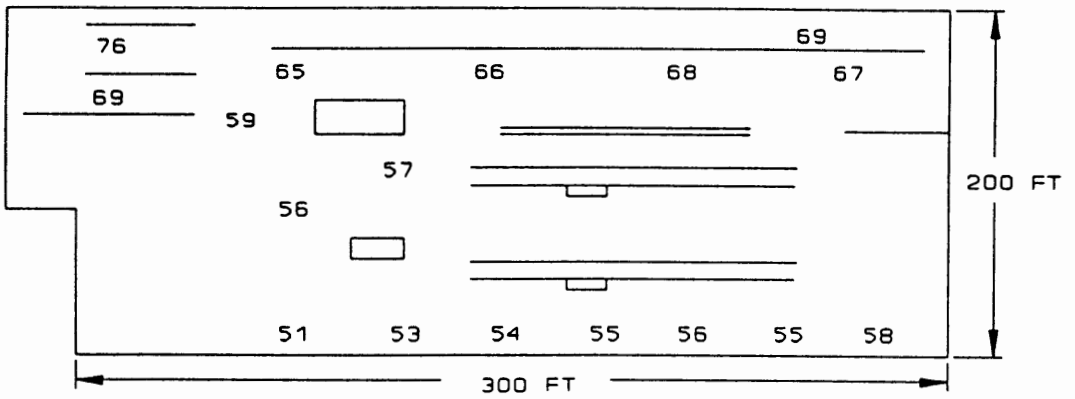


Figure 6.
Path Loss in dB for Radiating Cable

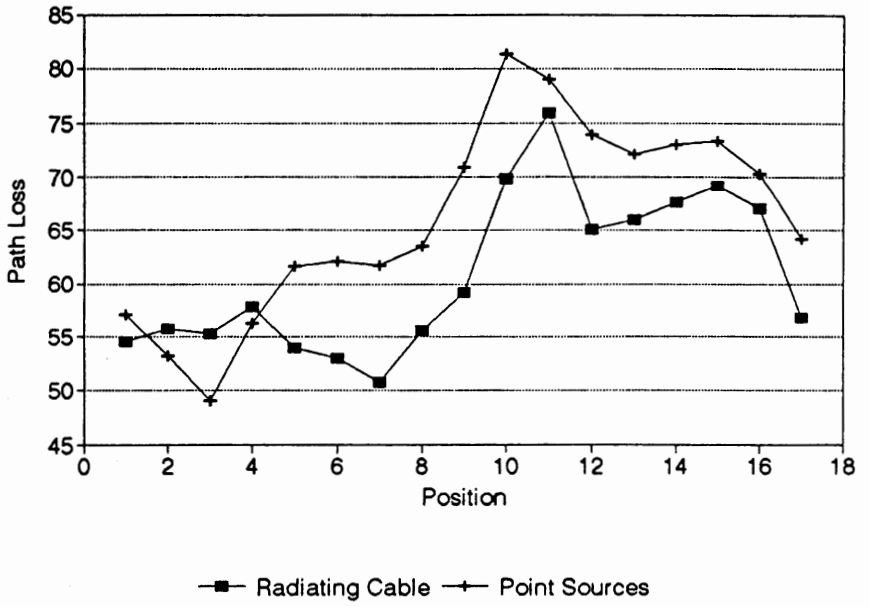


Figure 7.
Relative Path Loss Values (dB)

Figure 8 shows the difference in dB between the two distribution techniques where a positive value would favor the monopoles. The values given for the difference in RF coverage range from 12dB in favor of the radiating cable to 6dB in favor of the two quarter wave monopoles.

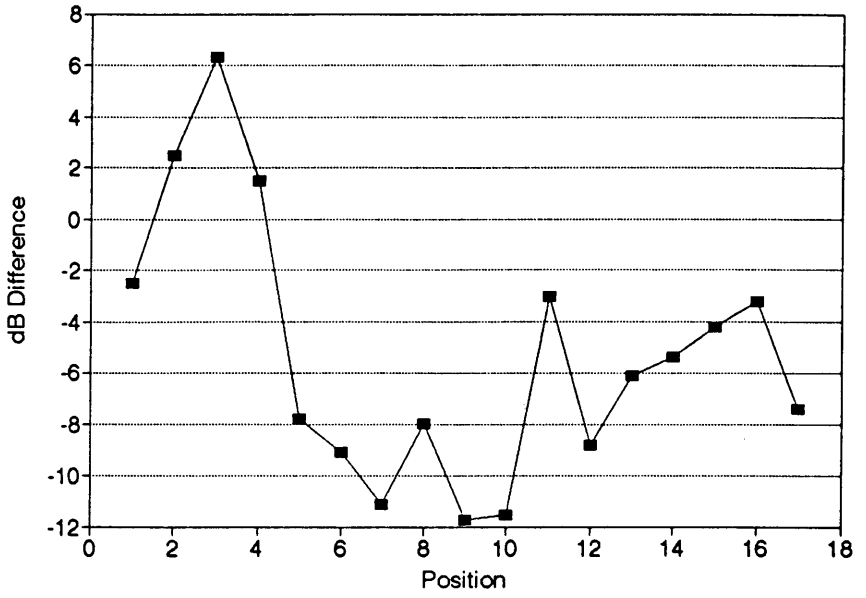


Figure 8
Difference in Path Loss (dB)

If the covered area were smaller the RF distribution would more conveniently be covered by a single source antenna like a monopole. In fact if all of the available power was distributed through the two monopoles there would be an additional 10dB at each of the two monopoles and would therefore reduce the path loss by the same value. The average difference between the path loss values for the two systems is 5.3dB with the advantage going to the radiating cable system. The relative power available at the output of each system shows the advantage of radiating cables in larger systems. An additional benefit of the radiating cables was the ease of installation. Installing the cables on the factory ceiling took twice as long for the aluminum sheathed coax as it did for the radiating cable. The aluminum sheathed coax was used because it is intended to have the best performance with the available taps. Also there was additional labor required installing the taps, mounting plates, and monopoles that was not required with the radiating cable.

Conclusion

For the particular 900 MHz system demonstrated we have shown that radiating cable provided better RF coverage using path loss evaluation. For 14 of the 17 locations in the factory, a higher signal level was measured with the radiating cable and will have a greater advantage when used in larger systems. This point is emphasized by the available power at the output of each system. the available power for an additional area was 16.8dBm for the radiating cable and 10.6dBm for the point source system, Both systems being supplied the same 30dBm input power. Future work will include polarization performance, comparison of performance in larger and smaller systems, and development of design values for general system use.

Radiating cable is a desirable alternative to discrete antennas because of improved RF coverage achieved and because of the ease of installation of this type of system.

1. Seidel,S.Y. and Rappaport,T.S.:"914 MHz Path Loss Prediction Models for Indoor Wireless Communications in Multifloored Buildings" IEEE AP-40

2. Ho,C.M.P. and Rappaport,T.S,:"Effects of Antenna Polarization and Beam Pattern on Multipath Delay Spread and Path Loss in Indoor Obstructed Wireless Channels", "ICUPC '92" Proceedings.

LOW COST F-QPSK MODEM RADIO SOLUTIONS FOR DOUBLING THE CAPACITY OF EUROPEAN STANDARD CELLULAR/PCS SYSTEMS

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Abstract

A low cost combined modulation radio technique **F-QPSK** is proposed for cellular/mobile and personal communications. The F-QPSK technique invented by Feher [18] belongs to an original power and spectrally efficient family of radio/modems developed and used for satellite communications. Similar to GMSK modulation used in the European DECT and other wireless land mobile standards, F-QPSK has constant envelope. This allows it to operate with class C power amplifier without output backoff (OBO). F-QPSK is thus 4 to 8 dB more power efficient than $\pi/4$DQPSK as currently adopted in the US IS-54 standard for land mobile and in the Japanese Digital Cellular (JDC) systems.

Our experimental hardware and computer generated results demonstrate that F-QPSK has a 51% higher spectral efficiency than the European standard GMSK system having a BT=0.5. Additionally, F-QPSK has superior BER performance characteristics. Our research shows that F-QPSK is 5.5 dB better than noncoherent GMSK in Eb/No over Rayleigh fading channels, and it is 2.5 dB more robust in a CCI controlled environment. We demonstrate that the combined spectral efficiency and C/I advantage of our proposed F-QPSK modem radio could nearly double (95% increase) the capacity of DECT.

1 Introduction.

Over the last few years, the worldwide demand for wireless communications has grown spectacularly. This is particularly evident in the cellular mobile communications markets that have been enjoying 33% to 50% annual growth rates [3]. As a parallel development, there is also a strong surge of interest in the emerging micro-cellular personal communications services (PCS) [1,2,3] that allow people to communicate anywhere, anytime. The worldwide demand for PCS services is expected to be huge and annual revenues of between $33 billion to $55 billion by the year 2000 in the United State alone have been projected by

Proceedings of the WIRELESS Symposium and Exhibition, San Jose, CA, Jan. 12-15, 1993.

some analysts [3]. However, successful exploitation of such huge potential market requires coordination and efficient industrial standards.

Currently, the most well-known standards for the emerging PCS are the European "Digital European Cordless Telecommunications" (DECT) [11] and CT-2. DECT is a low power microcellular system that uses TDMA/TDD (Time Division Multiple Access/Time Division Duplex) access method in the 1.8GHz band. CT-2, on the other hand, is designed mainly for telepoint services and is less versatile. But both standards use Gaussian Minimum Shift Keying (GMSK) for digital modulation. In this paper, we propose an alternative coherent F-QPSK (or Feher's QPSK [18,14]) modem radio solution for PCS that is significantly more efficient. Our investigation shows that the proposed scheme can nearly double (95% increase) the capacity of DECT.

F-QPSK is a power efficient digital modulation that belongs to the Intersymbol-interference-and-Jitter-Free Offset Quad-Phase-Shift-Keying (IJF-OQPSK) family originally introduced for satellite communications [9,13,14,18]. Our experimental hardware and computer generated results demonstrate that it is also more spectrally efficient than GMSK as used in European PCS standards. In addition, we find that F-QPSK has superior BER performance to noncoherent GMSK in both additive Gaussian and Rayleigh fading channel. More importantly, it is also more robust in cochannel interference (CCI) controlled environments typically encountered in microcellular PCS operations. **It is the combined spectral efficiency and C/I advantage of our proposed F-QPSK modem radio solution that leads to the significant improvement of capacity over DECT.**

The organization of this paper is as follows. After the introduction in Section 1, the principles and properties of F-QPSK are briefly reviewed in Section 2. The spectral efficiency and adjacent channel interference (ACI) characteristics of F-QPSK are compared with GMSK as used in DECT in Section 3. Section 4 analyses the BER performance of F-QPSK and finds it better than noncoherent GMSK in both Gaussian and Rayleigh fading environment. Finally, the capacity of F-QPSK in a cellular mobile environment is compared with DECT in Section 5. We summarize our results and present the conclusions in Section 6.

2 F-QPSK modulation.

The block diagram of our F-QPSK modulator is shown in Fig.1. It consists of a serial-to-parallel converter, pulse shaping filter $p(t)$, I/Q modulator and a hardlimiter.

The input binary data sequence $\{\alpha_n\}$ is first converted into 2 independent I/Q channel

symbol streams $\{a_n\}$, $\{b_n\}$ before being processed by the pulse shaping filter with impulse response:

$$p(t) = \begin{cases} 0.5[1 + cos(\frac{\pi t}{T_s})] & \text{for } |t| \leq T_s \\ 0 & \text{otherwise.} \end{cases} \quad (1)$$

where T_s is symbol duration. After the quadrature modulator and hardlimiter, we obtain the F-QPSK signal $S_o(t)$:

$$S_o(t) = \frac{x(t)cos2\pi f_c t}{\sqrt{x^2(t) + y^2(t)}} + \frac{y(t)sin2\pi f_c t}{\sqrt{x^2(t) + y^2(t)}} \quad (2)$$

where $x(t) = a_n p(t - nT_s) + a_{n-1}p[t - (n-1)T_s]$ and $y(t) = b_n p[t - (n-0.5)T_s] + b_{n-1}p[t - (n+0.5)T_s] + b_{n-2}p[t - (n+1.5)T_s]$ are the I and Q channel baseband signals respectively [4,9].

It is interesting to note from Fig.1 and equation (2) that F-QPSK is a power efficient modulation. Like GMSK as used in DECT, F-QPSK is also a constant envelope modulation capable of operating with class C power amplifier without output backoff (OBO). This is in contrast with the nonconstant envelope $\frac{\pi}{4}$DQPSK that typically requires 4 to 8 dB OBO to avoid spectral spreading. F-QPSK is thus 4 to 8 dB more power efficient than the popular $\frac{\pi}{4}$DQPSK used in the US IS-54 [10] standard for digital cellular mobile communications and in the Japanese Digital Cellular system.

Another advantage of F-QPSK is the simplicity of its implementation. The pulse shaping function in equation (2) can readily be realized using simple transversal filter technique [14]. Fig.2 shows the circuit diagram of the pulse shaper in a F-QPSK prototype modem [17] built in our Digital Communications Research Laboratory at University of California, Davis. The resulting I/Q channel eye diagrams are shown in Fig.3.

3 Spectral efficiency and ACI characteristics.

The power spectral density of F-QPSK is compared with GMSK in Fig.4. We notice that F-QPSK has a narrower main spectral lobe than GMSK although its tail decays less rapidly at high frequency. This indicates that F-QPSK is more spectrally efficient.

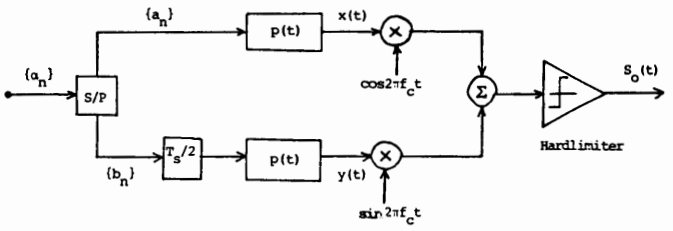

Fig. 1. Block diagram of F-QPSK modulator.

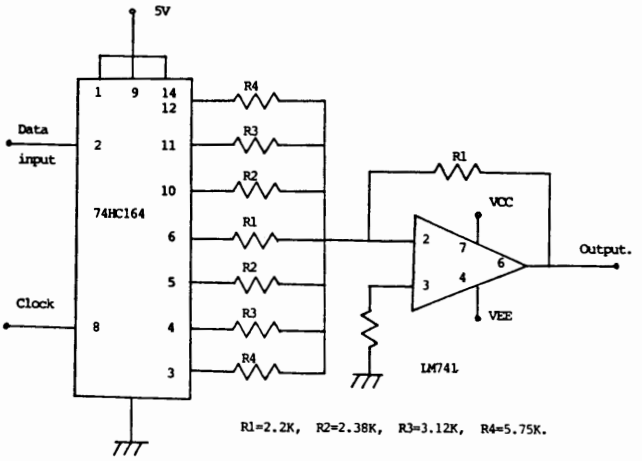

Fig. 1 Block diagram of F-QPSK modulator.

Fig. 2 Circuit diagram of F-QPSK pulse shaper.

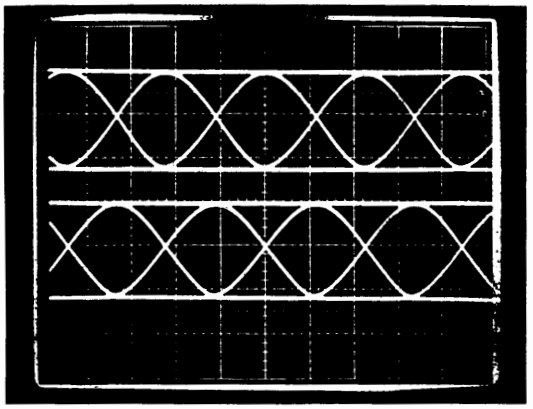

Fig. 3 Measured eyediagram of the experimental 180 Kb/s prototype F-QPSK modem, 5 μs/Div, 1v/Div.

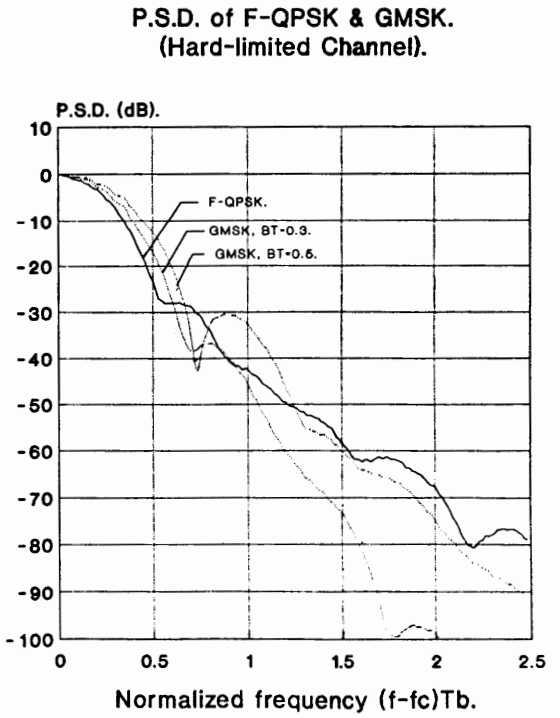

Fig. 4 Power spectrum of F-QPSK and GMSK as a function of the normalized frequency $(f-f_c)T_b$.

Spectral efficiency η_f (b/s/Hz) of a digital modulation is defined as $\eta_f = \frac{1}{WT_b}$ where W is the channel spacing and $\frac{1}{T_b}$ is the data bit rate. In a multicarrier system, normalized channel spacing WT_b is usually determined by the maximum acceptable adjacent channel interference (ACI) level. In this study, we calculate the ACI ratio $A(W)$ as :

$$A(W) = \frac{\int_{-\infty}^{\infty} G(f)|H(f-W)|^2 df}{\int_{-\infty}^{\infty} G(f)|H(f)|^2 df} \tag{3}$$

where $G(f)$ is the PSD of the signal and $H(f)$ the receive BPF transfer function in their baseband equivalent forms. This definition is adopted because it reflects accurately the impact of $H(f)$ on the ACI level.

The ACI characteristics of F-QPSK and GMSK are computed using (3) and the result plotted in Fig.5. It shows that F-QPSK causes significantly less ACI than GMSK and hence is spectrally more efficient in multicarrier systems. In this study, the BPF used for F-QPSK is 4th order Butterworth [7] with normalized 3dB bandwidth B_iT_b=0.55,

$$H(j\omega) = \frac{1}{(\omega^4 - 3.4142\omega^2 + 1) - j2.6131\omega(\omega^2 - 1)} \tag{4}$$

And the BPF used for GMSK is 4th order Gaussian [7] with B_iT_b=0.6,

$$H(j\omega) = \prod_{i=1}^{2} \frac{\omega_i^2}{\omega_i^2 + 2j\xi_i\omega_i\omega - \omega^2} \tag{5}$$

where $\omega = 2\pi f, \omega_1 = 1.9086, \omega_2 = 1.6768, \xi_1 = 0.7441, \xi_2 = 0.9721$. These filters are chosen for their good performance in Gaussian noise channel [5,6].

The spectral efficiency η_f of F-QPSK and GMSK in b/s/Hz are listed in Table 1 for four different ACI levels. For convenience, we also include the modulations' relative spectral efficiency using GMSK BT=0.5 as reference base (100%). This table shows that for ACI=-20 dB, F-QPSK has a spectral efficiency of 1.42 b/s/Hz which is 51% more efficient than GMSK BT=0.5 as used in DECT. Also, the spectral efficiency of F-QPSK could jump up to 1.63 b/s/Hz if -15 dB ACI can be tolerated.

	ACI=-15dB	ACI=-20dB	ACI=-26dB	ACI=-30dB
F-QPSK	1.63 (147%)	1.42 (151%)	1.23 (156%)	1.10 (155%)
GMSK BT=0.3	1.16 (105%)	0.98 (104%)	0.83 (105%)	0.74 (104%)
GMSK BT=0.5	1.11 (100%)	0.94 (100%)	0.79 (100%)	0.71 (100%)

Table 1. Spectral efficiency η_f in b/s/Hz.

4 BER performance.

The BER performance of our coherent F-QPSK scheme in Gaussian noise channel is obtained using computer simulation and the result plotted in Fig.6. This is compared with GMSK BT=0.5 with noncoherent detection as in typical DECT receiver [15]. In this study, the detection method employs frequency discriminator [16] with a Gaussian predetection BPF (B_iT_b=0.6) and a 4th order Butterworth postdetection LPF (B_bT_b=0.4). Fig.6 shows that in Gaussian noise channel, F-QPSK has a 3 dB Eb/No gain over noncoherent GMSK BT=0.5 at BER $P_e = 10^{-4}$.

Fig.7 compares the BER performance of coherent F-QPSK and noncoherent GMSK in slow Rayleigh fading (normalized Doppler frequency $f_DT \approx 0$). It shows that F-QPSK performs better than GMSK BT=0.5 by a wide 5.5 dB Eb/No margin in this environment. The performance of GMSK BT=0.3 is similarly obtained and is found to be within 0.5 dB of the BT=0.5 case.

Finally, F-QPSK's performance in a cochannel interference (CCI) controlled environment with Rayleigh fading is also obtained (see Fig.8). This performance is of considerable interest to system designer since CCI is known to limit the cellular system's performance rather than Gaussian noise [8]. Our study shows that coherent F-QPSK is 2.5 dB more robust than noncoherent GMSK in a cellular mobile environment. Fig.8 shows that while F-QPSK requires only C/I=15.7dB for BER $P_e = 10^{-2}$, GMSK BT=0.5 requires C/I=18.2dB.

5 Capacity in cellular environment.

In microcellular PCS systems, frequencies are reused in geographically separate cells to achieve greater network capacity [8]. In this environment, we need to include the frequency reuse factor K [9] when comparing modulations. Suzuki and Hirade's definition of the overall spectral efficiency η_T (b/s/Hz/m^2) of a modulation in a cellular environment is given by [9]:

$$\eta_T = \eta_f \times \frac{1}{K} \times \frac{1}{S} \tag{6}$$

where η_f is the modulation's spectral efficiency with respect to frequency (in b/s/Hz) and S is the coverage area of a cell (m^2).

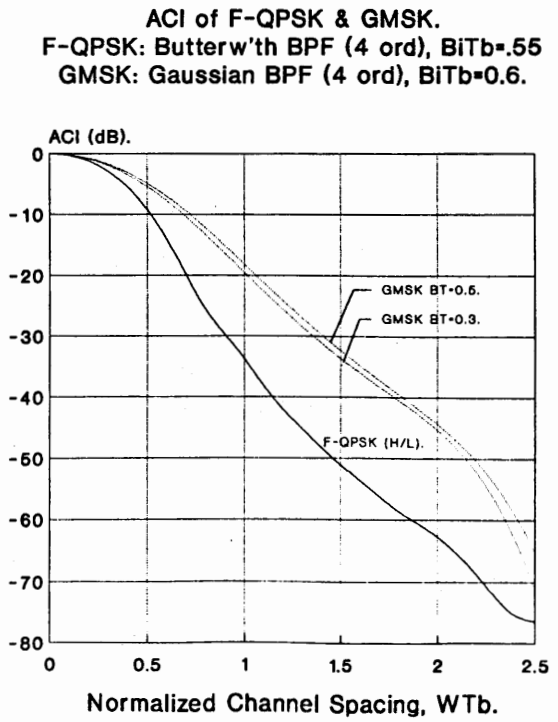

Fig. 5 ACI characteristics of F-QPSK and GMSK as function of normalized channel spacing WT_b. F-QPSK employs Butterworth (4th order) receive BPF with $B_iT_b = 0.55$. GMSK employs Gaussian (4th order) receive BPF with $B_iT_b = 0.6$.

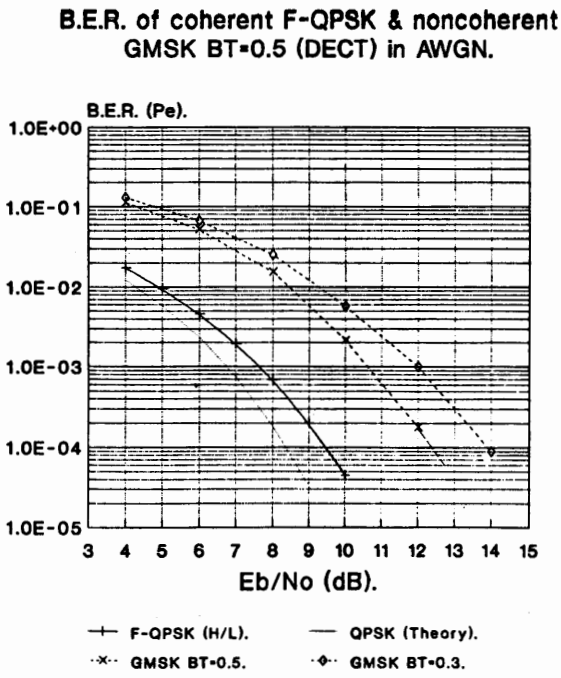

Fig. 6 BER performance of coherent F-QPSK and noncoherent GMSK in Gaussian noise channel.

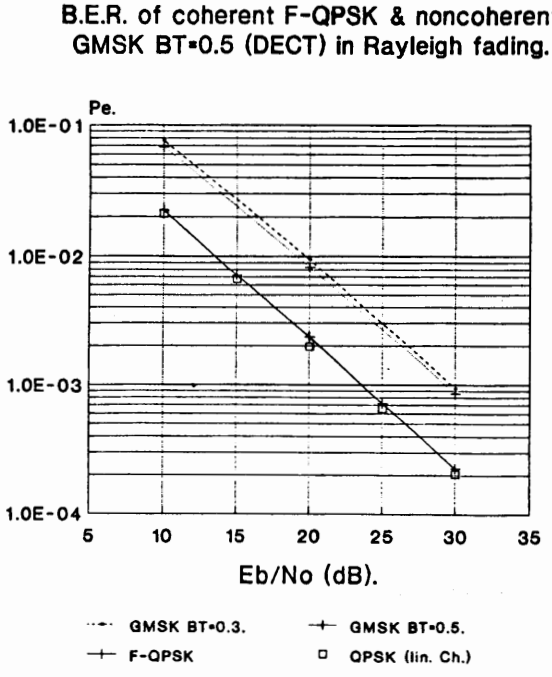

Fig. 7 BER performance of coherent F-QPSK and noncoherent GMSK in slow Rayleigh fading.

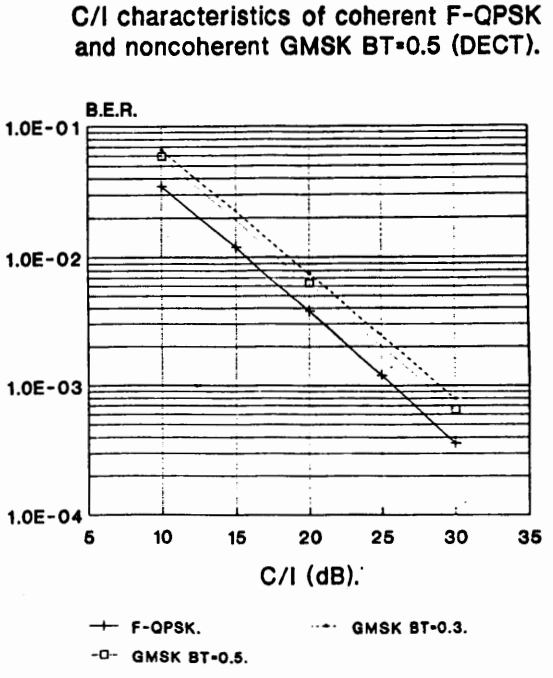

Fig. 8 C/I performance of coherent F-QPSK and noncoherent GMSK in slow Rayleigh fading.

The frequency reuse factor K (cells/cluster) is an integer [9]:

$$K = \frac{1}{3}[1 + (M_f \Lambda)^{\frac{1}{\gamma}}]^2 \tag{7}$$

where Λ is the C/I ratio required for a given BER performance. γ is the propagation constant whose value ranges between 2 and 4 ,and M_f is the C/I margin. The value of K is related to the normalized frequency reuse distance D by the formula $K = \frac{D^2}{3}$ although only some discrete values of K are possible. The allowable values are $K = (i+j)^2 - ij$ where i and j are positive integers including zero (ie. K=1,3,4,7,9,12 etc.) [12,8].

In this analysis, we assume (i) a BER of 10^{-2} for acceptable quality voice, (ii) $\gamma = 0.35$ and (iii) a fade margin of M_f=3dB. This margin corresponds to a geographical outage probability of approximately 10% [9]. Furthermore, without loss of generality, we let S=1 m^2.

The total spectral efficiency η_T of the proposed F-QPSK scheme and GMSK in a micro-cellular mobile PCS communications environment are compared in Table 2. For ease of comparison, we also list the modulations' relative total spectral efficiency, using GMSK BT=0.5 as used in DECT for reference base (100%). This comparison serves as an indicator of the network's capacity.

	η_f	Λ for Pe=10^2	K	η_T
F-QPSK	1.42	15.7 dB.	7	0.203 (195%)
GMSK BT=0.3	0.98	18.9 dB.	12	0.082 (79%)
GMSK BT=0.5	0.94	17.7 dB.	9	0.104 (100%)

Table 2, η_T in b/s/Hz/m^2.

Table 2 shows that the combined spectral efficiency η_f of F-QPSK and its CCI advantage over the noncoherent GMSK leads to a 95% increase of the overall spectral efficiency η_T in a cellular mobile environment. This demonstrates that our proposed F-QPSK modem radio solution can nearly double (95% increase) the capacity of DECT.

6 Conclusion.

In this paper, we propose a low-cost coherent F-QPSK modem radio technique that is ideal for the emerging personal communications services (PCS) standard. F-QPSK is a power efficient digital modulation. Being with a constant signal envelope, it can operate

with class C power amplifier without output backoff (OBO) and hence is 4 to 8 dB more power efficient than the $\frac{\pi}{4}$DQPSK as used in the current US IS-54 and the Japanese Digital Cellular standards.

The ACI characteristics, spectral efficiency in b/s/Hz/m^2 and BER performance of F-QPSK in mobile communications environment have been investigated using computer simulation. The results are compared with GMSK. We show that F-QPSK has an attainable spectral efficiency of 1.42 b/s/Hz, based on the ACI = -20dB criterion. This is up to 51% more spectrally efficient than the GMSK BT=0.5 as used in DECT. Coherent F-QPSK also has superior BER performance characteristics. Our research shows that it is 5.5 dB better than noncoherent GMSK in Eb/No over Rayleigh fading channels, and it is 2.5 dB more robust in a CCI controlled environment.

The impact of using F-QPSK in a microcellular PCS environment is also investigated. We show by numerical example that coherent F-QPSK is up to 95% more spectrally efficient than noncoherent GMSK BT=0.5. This means that our F-QPSK modem radio solution could nearly double (95% increase) the capacity of DECT.

We conclude that F-QPSK's high spectral efficiency and superior BER performance in both Rayleigh fading and CCI controlled channels make it an excellent choice for the future generation high capacity microcellular mobile PCS networks.

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References

[1] S. Ginn, "Personal Communications Services: Expanding the freedom to communicate", IEEE Communications Magazine, Vol.29, No.2, pp.30-39, February 1991.

[2] J.S. Bryan, "PCN: prospects in United States", Telecommunications, Vol.25, No.1, pp.54-56, January 1991.

[3] T. Rappaport, "The wireless Revolution", IEEE Communications Magazine, pp.52-71, Nov. 1991.

[4] T. Le-Ngoc, S. Slimane, "IJF-OQPSK modulation schemes with MLSE receivers for portable/mobile communications," Proc. IEEE 42nd. Veh. Tech. Conference, pp.676-680, Denver 1992.

[5] K. Murota, K. Hirade. "GMSK modulation for digital mobile radio telephony", IEEE Trans. on Comm. Vol. COM-29, No.7, pp.1044-1050, July 1981.

[6] J. Seo, K. Feher. "SQAM: A new superposed QAM modem technique", IEEE Trans. on Comm. Vol. COM-33, N0.3, pp.296-300, March 1985.

[7] C.S. Lindquist. "Active network design with signal filtering applications", Steward and Sons 1977.

[8] W.C.Y. Lee. "Mobile cellular telecommunications systems", McGraw Hill, 1989.

[9] K. Feher. "Advanced Digital Communications Systems and Signal Processing Techniques.", Prentice-Hall, Englewood Cliff, NJ, 1987.

[10] EIA IS54 Dual-mode subscriber equipment - Network equipment compatibility specification. December 1989.

[11] DECT Specification. Physical Layer, CI SPEC Part 1, Rev 06.0.

[12] R.C. French. "The effect of fading and shadowing on channel reuse in mobile radio". IEEE Trans. on Vehicular Technology, Vol. VT-28, No.3, pp.171-181, Aug. 1979.

[13] T. Le-Ngoc, K. Feher, H. Phamvan, "New modulation techniques for low-cost power and bandwidth efficient satellite earth stations", IEEE Trans. Comm. Vol. COM-30, No.1, pp.275-283, Jan. 1982.

[14] K. Feher, "Digital communications satellite/earth station engineering", Prentice-Hall 1983.

[15] D. Fague, "Integrated circuit solutions - Design considerations for DECT", Proc. IEEE Vehicular Technology Conference, pp.101-103, Denver 1992.

[16] K. Ohno, F. Adachi, "Half-bit offset decision frequency detection of differentially encoded GMSK signals", Electronics Letters, Vol.23, no.24, pp.1311-1312, Nov. 19, 1987.

[17] Y. Guo, K. Feher, "Frequency hopping F-QPSK for power and spectrally efficient cellular systems", submitted to IEEE Vehicular Technology conference, 1993.

[18] K. Feher, "Filter: Nonlinear Digital", U.S. Patent No. 4,339,724, issued July 13, 1982; Canada No. 1130871, August 31, 1982.

[19] K. Feher, "Cellular Digital PCS-Mobile Radio Communications", forthcoming book. Copyrighted.

[20] P.S.K. Leung, "GMSK and F-QPSK for high capacity cellular mobile and microcellular personal communications systems", forthcoming Ph.D. thesis, University of California, Davis, 1993.