1.0 INTRODUCTION

1.1 Scope

This preliminary specification covers detail requirements of a quality modem designed for 2 wire dial-up full-duplex operation and operating in the following modes:

a) PSK mode:
   1. 1200 bps asynchronous-character format
   2. 1200 bps synchronous-bit format

b) FSK mode:
   1. 300 bps asynchronous operation

Throughout this document the terms 212A and 212 will be used interchangeable. However, it is the intent of this specification to represent a modem compatible with the Bell System's 212A data set.

1.2 Summary Description

The unit described herein provides full-duplex transmission and reception of serial binary data at two specific bit rates over a switched network. The two modes of operation are identified as low-speed and high-speed.

In the low-speed mode, the unit is compatible with existing switched network low-speed modems such as the 103 and 113 types. The maximum data rate is 300 bps.

In the high-speed mode, the unit can be operated at 1200 bps. The data at the RS-232 interface may be formatted as bit-synchronous or character-oriented asynchronous. All timing signals and data format restrictions (the latter applies to asynchronous operation only) are described in the text of this document.

Various test features and tests are provided to aid in the diagnosis of typical communications systems problems. Among these are: self test, analog loopbacks, digital loopbacks and remote tests. A detailed discussion of the test is given in Paragraph 9.0 of this document.

2.0 APPLICABLE DOCUMENTS

2.1 EIA Standard RS-232-C, August 69

2.2 Bell Systems Technical References (212A Modem)

2.3 CCITT Recommendation V.22 (Where Applicable)

2.4 Part 68 of FCC Regulation

3.0 GENERAL CHARACTERISTICS

The following specifications cover the operational characteristics of the 212A modem.

3.1 Type of Line

Type 3002 telephone lines.

3.2 Data Rate

Mode A: 1200 bps synchronous (PSK Mode)

Mode B: 1200 bps start-stop (PSK Mode)

Mode C: 0-300 bps asynchronous (FSK Mode)

In all cases the data is transmitted and received serially. Interface to the 212A modem shall be RS-232-C compatible.

3.3 Modulation

A - Analog

1) Differentially coherent phase shift keyed on a dibit basis. The carrier frequencies will be 1200 Hz ± 0.01% for the low channel and 2400 Hz ± 0.01% for the high channel.

2) Frequency shift keyed on a bit per bit basis. The average carrier frequencies will be 1170 Hz ± 6 Hz for the low channel and 2125 Hz ± 6 Hz for the high channel.

B - Digital

1) Data Signaling Rates, Overall

Reference Paragraph 3.2.

- Mode A (1200 bps synchronous) shall require a bit rate of 1200 bps ± 0.01%.

- Mode B shall require a data signaling rate (Tx data) of 1200 bps + 1%, -2.5% (See 2 below for detailed description).

- Mode C shall require a data signaling of 300 bps. The deviation of the bit rate will follow the type 103 modem specifications.

2) Data Signaling Rates, Detailed Description

- Mode A shall require 1200 bps ± 0.01% synchronous. In this mode, the modem shall accept synchronous data from Circuit BA (Tx D) under control of Circuit DB (internal clock), Circuit DA (external clock), or Circuit DD (slave option = RX clock); i.e., a conventional synchronous interface.

- Mode B is 1200 bps nominal start-stop 9 or 10 bits per character (including 1 start, 1 stop bit); i.e., a conventional asynchronous interface with a character length restriction.
- Mode C is 300 bps asynchronous with operation and interface characteristics similar to a 103 type modem.

Note: In the start-stop mode, the modem shall accept a data stream of start-stop characters at a rate of 1200 bps + 1%, -2.5%. The start-stop data shall be converted to a form suitable for synchronous transmission at 1200 bps ± 0.01%, then scrambled in accordance with Paragraph 4.1.2 and passed to the modulator for encoding in accordance with Paragraph 4.1.3.

3) Additional Notes on the Signaling Rate Range

The following is applicable to Mode B (1200 bps async).

- When character rate from the DTE is
  from 133.3 to 134.7 characters/sec for 9 bit characters,
  from 120.0 to 121.2 characters/sec for 10 bit characters,

  the start-stop asynchronous-to-synchronous converter within the modem shall as often as necessary delete the stop bit of the incoming characters. However, no more than one stop bit shall be deleted for any 8 consecutive characters.

The receiving modem will in turn re-insert the stop bit(s) which were deleted by the transmitting modem. Thus this process of "catching up" is not readily observable by the DTE on either end of the transmission.

- When the character rate is less than
  133.3 characters/sec for 9 bit characters
  120.0 characters/sec for 10 bit characters

  the asynchronous-to-synchronous converter within the modem is transmitting more bits/sec than are provided by DTE. The converter shall, therefore, insert extra stop bits in between transmitted characters.

Note: Means are also provided to handle BREAK signals as follows:

If the data to be transmitted is M to 2M + 3 bits (where M is the number of bits per character) of start polarity, the converter shall transmit 2M + 3 bits of the same. If the converter detects more than 2M + 3 bits of start polarity, the converter shall transmit all these bits as start polarity.

The DTE MUST transmit on Circuit 103 (TXD) at least 2M bits of STOP polarity after a break signal to insure that the receiving end regains CHARACTER SYNCHRONISM. Then and only then can further data characters be sent.

3.4 Compatibility

The UDS 212 modem shall be both line and functionally compatible with the Western Electric 212A modems.

4.0 DETAILED MODEM REQUIREMENTS

4.1 Transmit Level

The transmitter output level shall be strap selectable in increments of 3 dB, between 0 dBm and -12 dBm. An additional strap position marked RP will allow the transmit level to be set by external programming resistor (RJ45 type connection).

The output shall be transformer coupled to the telephone line and have an output impedance to the line of 600 ohms ± 10%, across the band from 700 to 2700 Hz, when a 100 ma max. D.C. current vector is superimposed on the A.C. signal vector.

4.1.1 Transmitter Output, Sideband Content and Group Delay

Fixed compromise equalization shall be incorporated in the modem. Such equalization shall be equally shared between transmitter and receiver.

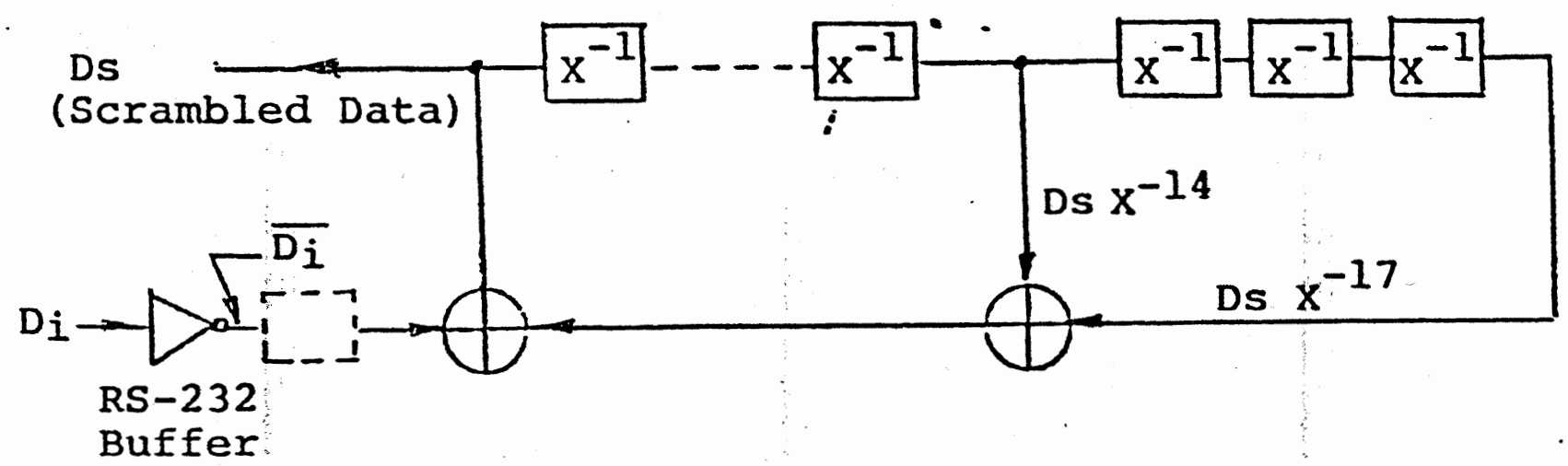
After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal shall have a frequency spectrum equivalent to a raised cosine shaping with a 22% roll-off. Similarly the peak group delay of the transmitter output shall be ± 100 μs over the range 800-1600 Hz (low channel) and 2000 Hz-2800 Hz (high channel). The nominal maximum out of band power (> 4000 Hz) shall not exceed -40 dB with respect to center of transmitted band.

4.1.2 Scrambling of Data Bits (1200/600 bps Operation)

A self synchronizing scrambler having the generating polynomial $1 + X^{-14} + X^{-17}$ shall be included in the modem. The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The scrambler output data sequence is

$$Ds = \overline{D_i} \oplus Ds.\ X^{-14} \oplus Ds.\ X^{-17}$$

The scrambler should be configured as follows:



$\oplus$ = EX-OR Operation

$.$ = Binary Multiplication

$\overline{D_i}$ = D_i Inverted

⬚ = Anti Lock-Up Circuitry (Watches for all $\overline{D_i} = 0$ Condition)

Note: The anti-lock-up circuitry as proposed by CCITT recommendation V.22 is as follows:

SCRAMBLER - If 64 consecutive binary ones are detected at the output of the SCRAMBLER, then the next INPUT bit to the scrambler should be inverted.

DESCRAMBLER - If 64 consecutive binary ones are detected at the input of the DESCRAMBLER, the next output bit should be inverted.

The anti-lock-up feature is incorporated as a strap option in the UDS 212. It is presently not available in the WECO 212A.

4.1.3 Encoding of Data Bits

4.1.3.1 1200 Bits Per Second

The synchronous data stream, generated by the modem for transmission, shall be divided into groups of 2 consecutive bits (DIBITS). Each DIBIT shall be encoded as a phase change relative to the phase of the preceding signal element (See Table 1). The left-hand digit of the dibit (in Table 1) is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

4.1.3.2 300 Bits Per Second

Each bit shall be encoded as a frequency shift relative to its polarity (see Table 2).

TABLE 1. LINE CODING

1200 BPS DIBIT VALUES	PHASE CHANGE
00	+90°
01	0°
11	-90°
10	+180°

TABLE 2. LINE CODING

300 BPS BIT VALUE	LO-CHANNEL FREQ.	HI-CHANNEL FREQ.
1	1270 Hz	2225 Hz
0	1070 Hz	2025 Hz

Note: Bit values are binary values, i.e., 1 = Mark
0 = Space

5.0 TRANSMITTER TIMING

See Appendix A.

6.0 USING SIGNALS DA AND DD (EXTERNAL AND SLAVE TX CLOCKS)

The frequency of these clocks shall be 1200 bps ± 0.025%. The jitter shall not exceed ±1.0% and the duty cycle shall be 50 ± 2.0%.

7.0 RECEIVER

The modem receiver shall conform to the specifications of this section.

7.1 Dynamic Range

For 1200 bps operation, the receiver shall have a nominal dynamic range of 0 to -45 dBm.

For 300 bps operation, the receiver shall have a nominal dynamic range of 0 to -50 dBm.

The received signal shall be transformer coupled to the telephone line. The impedance presented to the line shall meet specification of 2nd paragraph, reference 4.1.

For 1200 bps operation, an option strap will permit reception of a signal in the nominal range of 0 dBm to -30 dBm or -15 dBm to -45 dBm.

For 300 bps operation, the dynamic nominal range will extend from 0 dBm to -50 dBm.

In all cases the hysterisis (from OFF to ON) will be no less than 2 dB, no more than 4 dB.

7.2 Carrier Detect Clamp

When receive carrier detector is false, the received data output will be clamped to MARK hold.

7.3 Carrier Detect Delay

See timing chart in Appendix A.

7.4 Compromise Equalizer

See 4.1.1.

7.5 Receive Filter

The pass-band for the receive filter shall be 1200 Hz ± 450 Hz for Lo-Band and 2400 Hz ± 450 Hz for Hi-Band, where the bandwidths are at the 3 dB points.

7.6 Data Retrieval

7.6.1 Signaling Rate (1200 bps/Async-Sync Operation)

The intracharacter signaling rate provided by the receiver to the DTE over Circuit 104 (Rx D) shall be either 1200 bps synchronous or 1219 bps asynchronous. The nominal length of the start and data elements for all characters shall be the same. The length of the stop element shall not be reduced by more than 12% for the

basic signaling rate range to allow for overspeed in the transmitting terminal.

Note: The data handling within the modem is done in synchronous fashion. The data delivered to Circuit 104 (RXD) has the start-stop format compatible with async terminals. This requires a converter to reinsert the stop bits removed by the transmitter (Ref. 3.3, Paragraph 2 and 3).

7.6.2 Break Signal

Reference 3.3.

The 2M + 3 or more bits of "start" polarity received from the transmitting modem shall be output on Circuit 104 (Rx D). The modem shall then regain character synchronism from the following "STOP" to "START" transition.

7.6.3 Alternatives

See Reference 3.3.

The modem receiver shall be able to handle all modes as described in Reference 3.3. Strap options are utilized for the selection of the appropriate PSK mode.

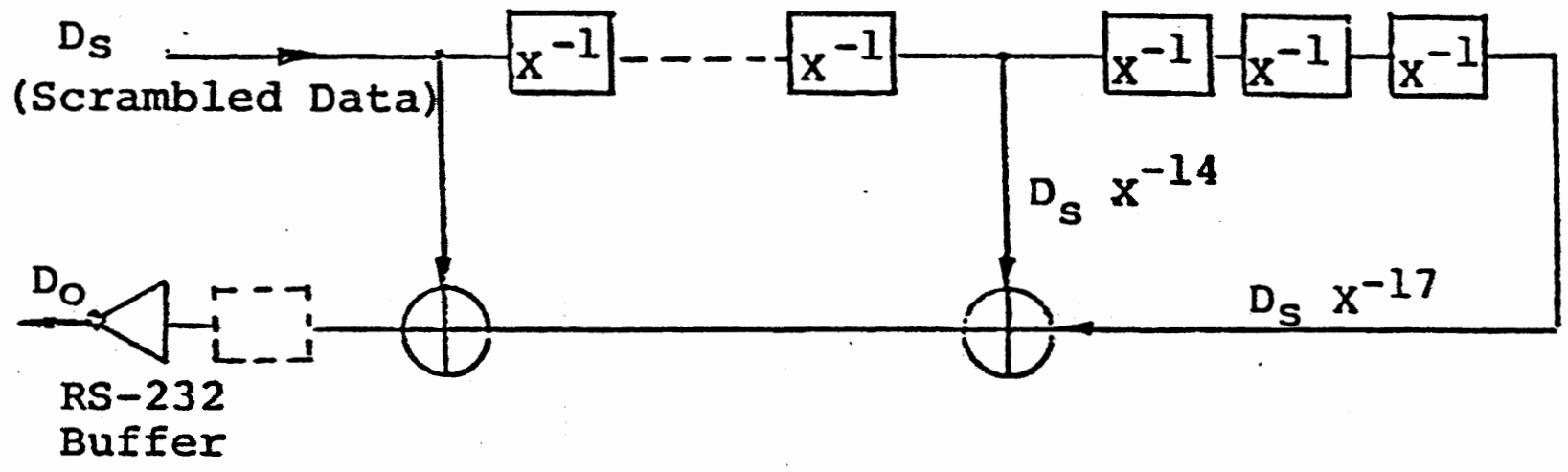
7.6.4 Descrambler

Before received data is fed into the converter for final formatting, it has to be descrambled.

A self-synchronizing descrambler having the polynomial $1 + X^{-14} + X^{-17}$ shall be provided. The message data sequence after demodulation shall be effectively multiplied by the generating polynomial $1 + X^{-14} + X^{-17}$ to form the descrambled message.

$$D_o = \overline{D_s(1 \oplus X^{-14} \oplus X^{-17}}$$

A suitable arrangement shall be as follows:



⊕ = EX-OR Operation

⬚ = Implemented if anti-lock-up is used in the scrambler.

Note: The anti-lock-up circuitry as proposed by CCITT recommendation V.22 is as follows:

SCRAMBLER - If 64 consecutive binary ones are detected at the output of the SCRAMBLER, then the next INPUT bit to the scrambler should be inverted.

DESCRAMBLER - If 64 consecutive binary ones are detected at the input to the DESCRAMBLER, the next OUTPUT bit should be inverted.

The anti-lock-up feature is incorporated as a strap option in the UDS 212. It is presently not available in the WECO 212A.

8.0 OPERATIONAL PROCEDURES

8.1 Channel Allocation

When operating on switched (e.g., telephone) networks and utilizing automatic or manual answering capability, modems at calling locations shall transmit on the Low Channel and receive on the High Channel. Conversely, modems at called locations shall transmit on the High Channel and receive on the Low Channel. The mode (PSK or FSK) is selected by the calling modem. The called modem will automatically adjust to the mode via the initial protocol as described in the later paragraphs.

8.2 212A Protocol: (See Also Timing Chart in Appendix)

The handshaking procedures take place after the transfer to the data mode is accomplished (after CC (DSR) has turned ON). There are four basic sequences which can be followed, depending on the selection of speed and the kind of data sets which are connected. The possible combinations are listed below:

1) The originating data set is a 212A with the High-Speed Mode selected and the answering data set is a 212A.

2) The originating data set is a 212A with the Low-Speed Mode selected and the answering data set is a 212A with the Dual Speed capability.

3) The originating data set is a 212A with the Low-Speed Mode selected and the answering data set is a 300 bps FSK data set other than a 212A (such as a 113B or 103A).

4) The originating data set is a 300 bps FSK data set other than a 212A and the answering data set is a 212A Dual Speed capability.

The sequence for the first combination is given in Section 8.2.1. The handshaking sequence for combination 2 is given in

Section 8.2.2. The handshaking for combinations 3 and 4 are essentially the same as that for combination 2 with time and protocol variations.

8.2.1 High-Speed Mode Handshaking Sequence

See Timing Chart in Appendix A.

After the answering 212A has transferred to the data mode, the channel is kept silent for two seconds. When the silent interval has elapsed, the answering 212A begins transmitting the (2225 Hz) answer tone. The originating 212A requires approximately 155 ± 50 milliseconds to detect the answer tone. The originating 212A will begin to transmit 456 ± 10 milliseconds after answer tone is detected. The answering 212A requires 270 ± 40 milliseconds for its carrier detection process, after which it transmits a scrambled marking signal. The originating 212A also requires 270 ± 40 milliseconds to acquire the carrier, then its CF (RCD) circuit turns ON. The answering data set delays 765 ± 10 milliseconds after it began transmitting the scrambled mark signal, then turns on the CF (RCD) and CB (CTS) circuits. The originating data set delays 765 ± 10 milliseconds after the CF (RCD) circuit turned ON, then turns ON the CB (CTS) circuit. The handshaking is complete at this point, and 1200 bps data can be transmitted in both directions.

After the answering 212A is transferred into the data mode, it begins to time the abort interval. If the CF (RCD) circuit does not turn ON within approximately 18 seconds, the data set will abort the call and disconnect itself from the telephone line. Timing Chart in Appendix A shows the high-speed handshaking sequence with manual calling and manual or automatic answering.

8.2.2 Low-Speed Mode Handshaking Sequence

See Timing Chart in Appendix A.

After the answering data set has been transferred into the data mode, the data set times the two second silent interval before it begins to transmit the high-speed answer tone of mark hold (2225 Hz). The originating data set carrier detector turns ON after 155 ± 50 milliseconds, and the CF (RCD) circuit turns ON. 456 ± 10 milliseconds after the CF (RCD) circuit has turned on, the originate data set begins transmitting a low-speed mark signal (1270). The carrier detector at the answering data set also requires 155 ± 50 milliseconds to detect the carrier, then the CF (RCD) and CB (CTS) circuits turn ON and disable the 2225 Hz marking signal. The originate data set turns on its CB (CTS) circuit 765 ± 10 milliseconds after the CF (RCD) circuit turns ON. Customer data can be transmitted in both directions at this point. Timing Chart in Appendix A shows the low-speed handshaking with manual calling and automatic answering.

9.0 TEST MODES

The test modes are the same for the low-speed mode and the high-speed mode with the following exception:

> Remote digital loop-back is only valid and available in high-speed mode.

The following paragraph describes the different tests available.

9.1 Analog Loop

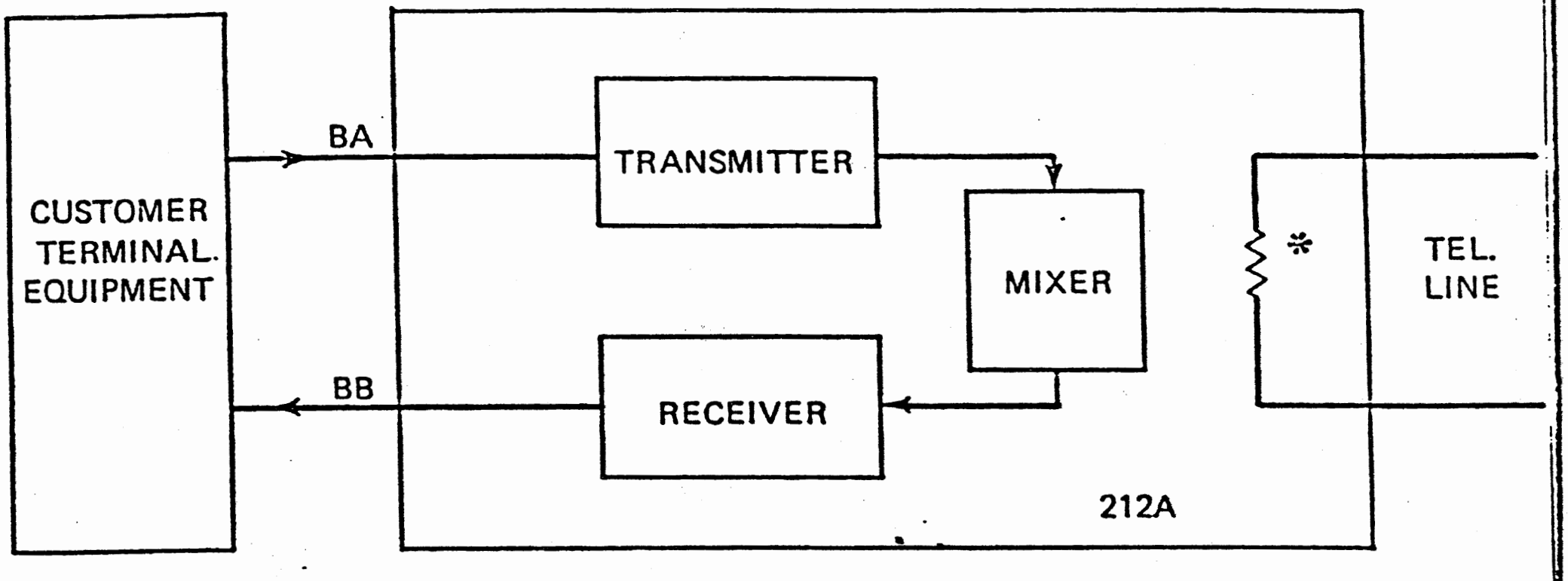
The Analog Loop test mode is used to verify the operation of the 212A modulation/demodulation functions, the terminal receive/transmit functions and the data set/terminal interface. To condition the 212A for an Analog Loop test, the Data Terminal Ready (CD) circuit must be ON. The speed mode of the test is selected by the front panel HS pushbutton. The test is initiated manually or by DTE command. The 212A follows a "handshaking" sequence which resembles the data mode sequence, except that there is no far end data set, and no answer tone sequence. If the 212A is in the originate mode, the transmitter is activated as soon as the test mode is entered. When the carrier detector acquires the signal, the CF (RCD) circuit turns ON, and 765 ± 10 milliseconds later, the CB (CTS) circuit turns ON, allowing transmission and reception of data by the local terminal equipment. If the 212A is in the answering mode, both CF (RCD) and CB (CTS) turn ON when the carrier detector turns on. The speed mode of the test can be changed during the test, in which case the 212A will turn OFF CB (CTS) and CF (RCD) and reinitialize the test sequence in the new speed mode. The Ring Indicator (CE) circuit is operational during the Analog Loop test if the data set is not configured for making the telephone line busy.

If the 212A is configured to operate in the 1200 bps mode synchronously and the Transmitter Timing Slave option is installed, the Analog Loop test in the high-speed mode is not allowed.

The TM lamp on the front panel of the 212A will be illuminated whenever this test is performed.

If the data set is configured for make busy, the telephone line will be placed in the busy state during the Analog Loop test. Figure 1 shows the internal configuration of the data set during the test.

ANALOG LOOP TEST
FIGURE 1

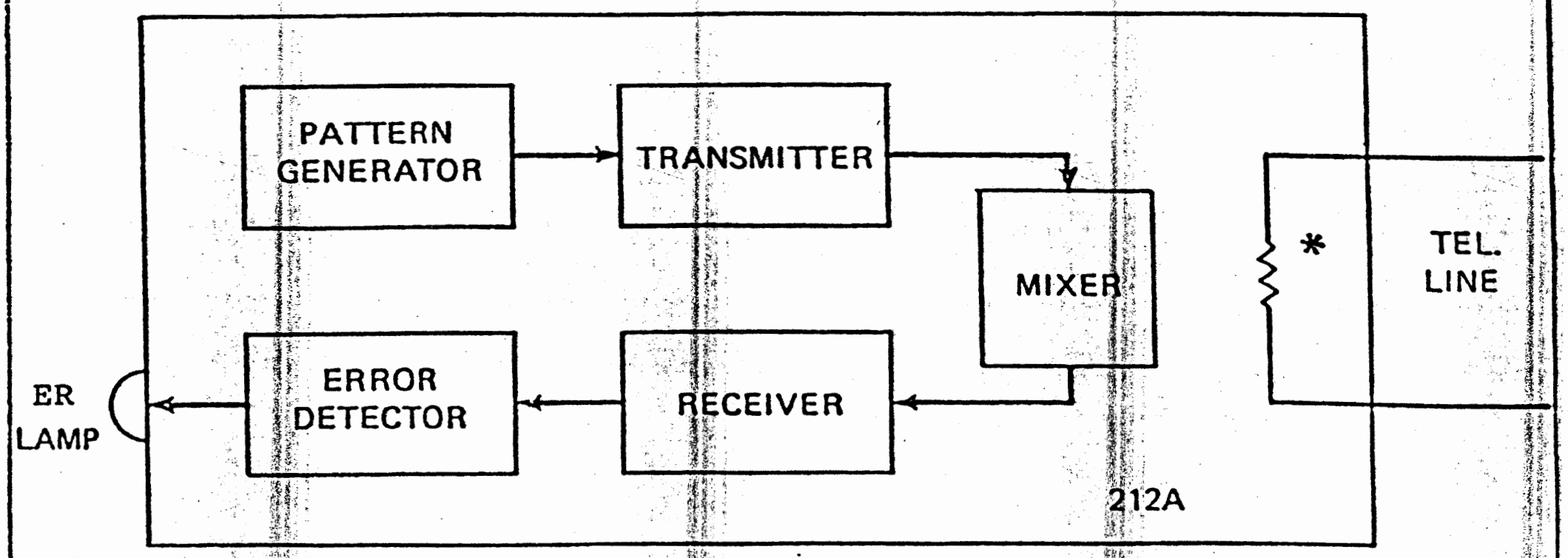


AL

* OPTIONAL TERMINATION DURING TEST

HI In High-Speed Mode

SELF-TEST ANALOG LOOP
FIGURE 2



AL

* OPTIONAL TERMINATION DURING TEST

ST

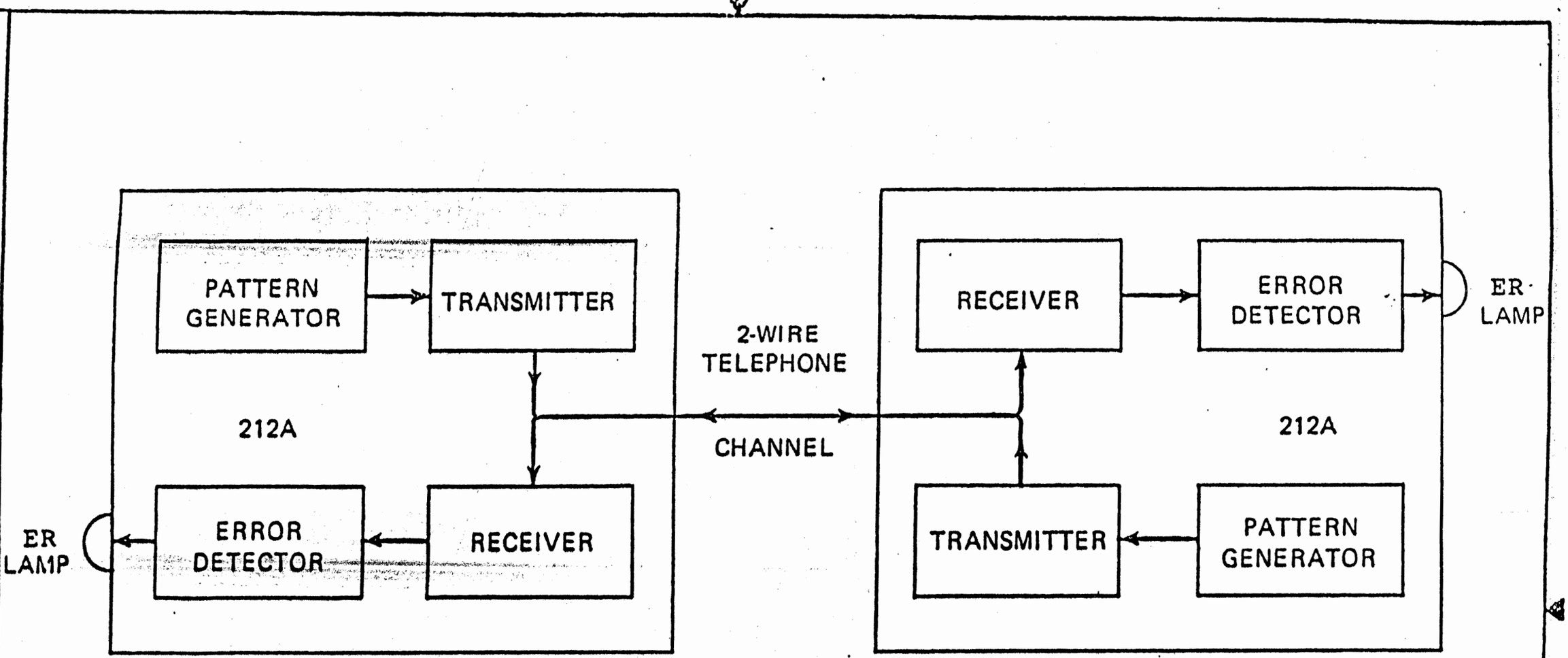
HI In High-Speed Mode

9.2 Analog Loop - Self Test

The test is initiated by manually activating AL and ST command. Internal to the data set, an analog loopback is established in the same way as the Analog Loop test mode, except that the customer interface circuits DSR, CTS, and RCD are clamped OFF and Rx data is clamped to mark hold. The 212A generates a test pattern of scrambled alternating ones and zeros which is applied to the transmitter being tested, and an error detection circuit is placed on the received data circuit. If the AL/ST test is performed in the low-speed mode, the error detection circuit causes the error LED to blink ON if the bit length of a received data bit exceeds the nominal length by more than 25% of a nominal bit length. If the 212A is in the high-speed mode, the error LED will blink ON if a bit error is detected in the received data. For either kind of detected error, the LED remains ON for approximately 300 milliseconds. Figure 2 shows the internal configuration of the data set during the test mode.

9.3 End to End Self Test

This test can be used to check the operation of the local modulator/demodulator, the far-end modulator/demodulator, and the integrity of the communication channel in each direction independently. No terminal equipment is needed at either data station. The Self Test mode in the 212A overrides the condition of the Data Terminal Ready (CD) circuit from the terminal, forcing it to the ON condition internal to the data set. The ST feature is enabled before or during the data mode establishment except if the terminals are not connected, or if circuit CD is not ON, in which case the ST feature would have to be enabled before the data mode. The error detection circuit at each end monitors the received data signal, and illuminates the error LED at that end if a bit error is detected, or the distortion threshold is exceeded. Each data set sends the test pattern of scrambled alternating ones and



END TO END SELF-TEST
FIGURE 3

zeros through the communication channel to the other data set, with both directions of transmission occurring simultaneously. Either speed mode can be checked with the End to End Self Test if selected. Figure 3 shows the internal configuration of the data sets during the test.

9.4 Remote Digital Loop

This test is used to remotely condition the far-end 212A to act as a repeater for the data being transmitted by the local 212A. The test is only effective when the 212A is in the high-speed mode. The Remote Digital Loop test can only be initiated at the local 212A by manually enabling the RDL function. The digital loop will take place at the far-end data set. To digitally loop an unattended data set, that station must be optioned for Automatic Answer and have the CD (DTR) circuit ON. When the test is initiated, the local 212A turns OFF the CB (CTS) circuit until the digital loop through the far-end is established. At the far-end data set, the interface circuits CB (CTS), CF (RCD), and CC (DSR) are turned OFF for the duration of the test. The test lamp is illuminated at both ends during the test. The space disconnect feature is disabled, overriding the Receive Space Disconnect option in both 212A's. At the far-end data set, the Loss of Carrier Disconnect option is forced ON during the test mode and for the remainder of the time that the data set is in the data mode. Also, at the far-end data set, the customer interface circuit Data Terminal Ready is overridden internally to the ON state during the test, and reverts back to customer control when the test mode is terminated.

During the Remote Digital Loop test, the local terminal equipment can transmit data to the far-end and monitor the local received data, which should be a duplicate except for a delay time equal to the total round trip delay.

A Remote Digital Loop test is not allowed if the Transmit Timing Slave option is installed at the originating modem. Figure 4 shows the internal configuration of the data sets during the test mode.

9.4.1 RDL Protocol

Signals controlling the application of RDL may only be transmitted after the synchronizing handshake has been completed.

As in Recommendation V.54, the modems are referred to as Modem A (Origination Modem) and Modem B (Answer Modem).

When Modem A is instructed to instigate a RDL, the modem shall transmit an initialization signal of unscrambled Binary 0.

Modem B shall detect 154-231 ms of the initialization signal, and then transmit to Modem A scrambled alternate binary ones and zero (reversals) at 1200 bps.

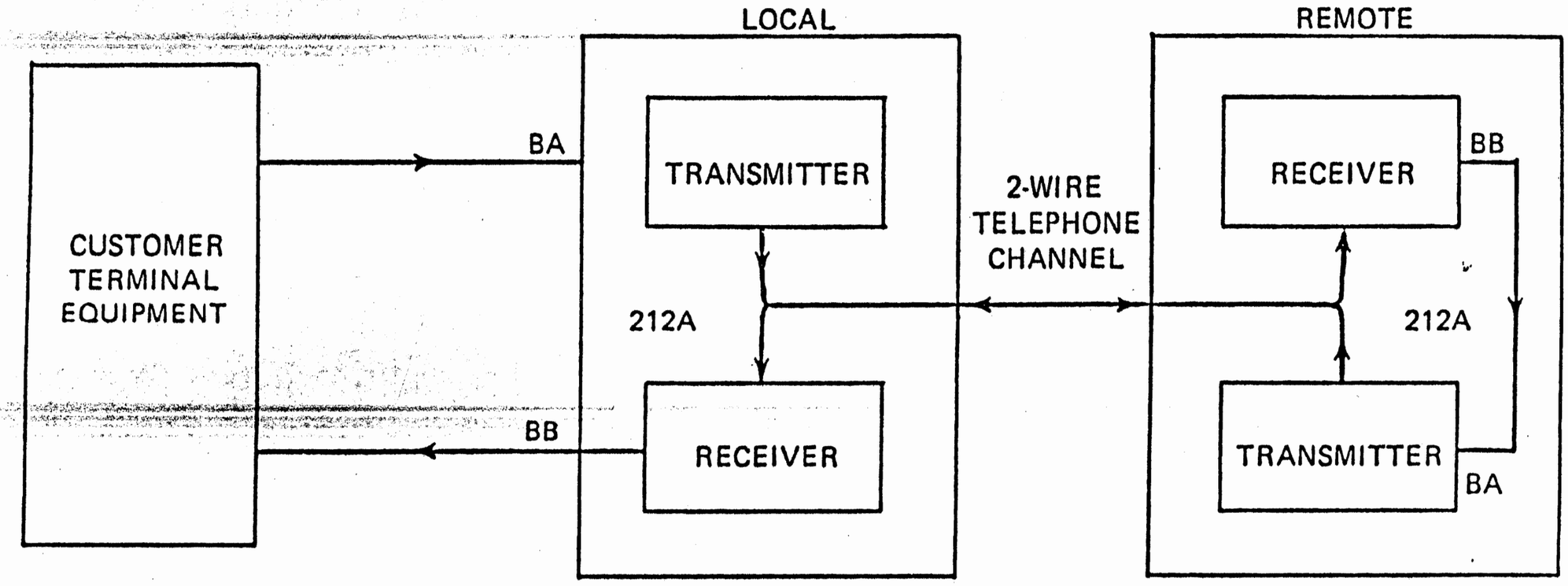
Modem A shall detect 231-308 ms of scrambled reversals, cease transmission of the initialization signal, and then transmit scrambled Binary 1 at 1200 bps.

Modem B shall detect the loss of initialization signal and activate the loop within Modem B.

Modem A, upon receiving 231-308 ms of scrambled Binary 1, shall indicate to the DTE that it may begin sending test messages.

Modem B is instructed to terminate a remote loop when the line signal from Modem A is suppressed for a period of 77 ± 10 ms by manually disabling the RDL function, after which transmission shall be restored.

Modem B detects the loss of line signal in 17 ± 7 ms and detects the re-appearance of the signal within 155 ± 50 ms, after which it returns to normal operation.



NOTE: HIGH SPEED ONLY

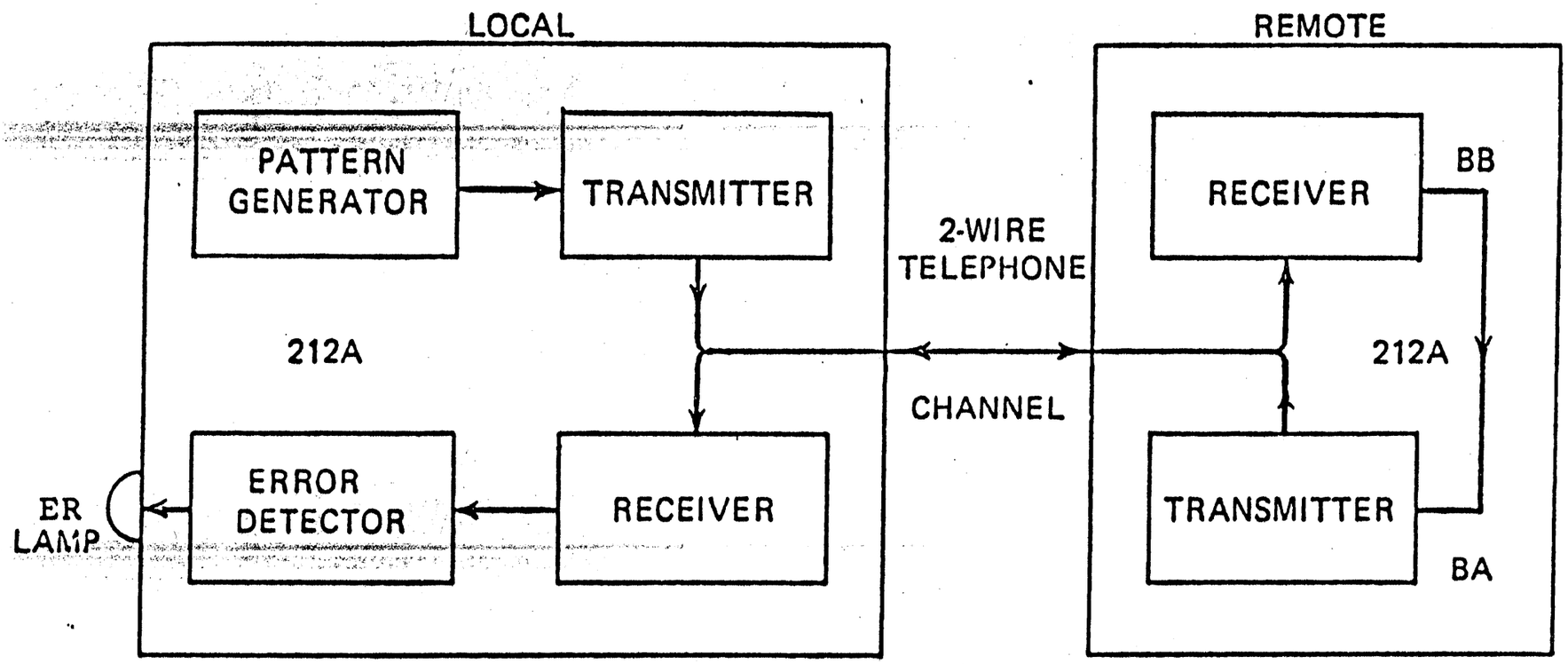
REMOTE DIGITAL LOOP
FIGURE 4

9.5 Remote Digital Loop - Self Test

This test allows the local attendant to verify the operation of both local and far-end 212A data sets and both directions of the connecting communications channel without local terminal equipment. The data path from the local 212A to the far-end 212A and back again is the same as in the Remote Digital Loop test, except that in this test the data pattern consisting of scrambled alternating ones and zeros is provided by the local 212A and is checked for accuracy by the local 212A. The customer send data circuit is ignored at both of the 212A data sets. To condition the 212A for this test, both the ST and RDL functions must be enabled, either before or during the data mode (high-speed only), in either order. The far-end data set must have CD (DTR) ON and the Automatic Answer option enabled. At the local 212A, the interface circuits CC (DSR), CB (CTS), and CF (RCD) are turned OFF for the duration of the test. These same circuits are also turned OFF at the far-end data set. At both data sets, the Data Terminal Ready circuit is forced to the ON state internally, and the customer CD circuit is ignored. At the local data set, the error LED indicates an error in the looped test pattern by flashing ON for approximately 300 milliseconds. When the RDL-ST test is completed, the ST and RDL functions are released and the data sets are returned to the normal high-speed data mode (CC, CB, CF ON). Figure 5 shows the internal configuration of the data sets during the test mode.

9.6 Digital Loop

The 212A can be manually conditioned to loop the received data back to the transmitter circuits in all data formats by manually enabling the DL function. This test is used to test the 212A from a remote location such as a data test center. When the function is enabled, the 212A will be optioned for Automatic Answer IN with customer circuit CD (DTR) internally forced to



ST

RDL

HI

NOTE: HIGH SPEED ONLY

SELF-TEST REMOTE DIGITAL LOOP
FIGURE 5

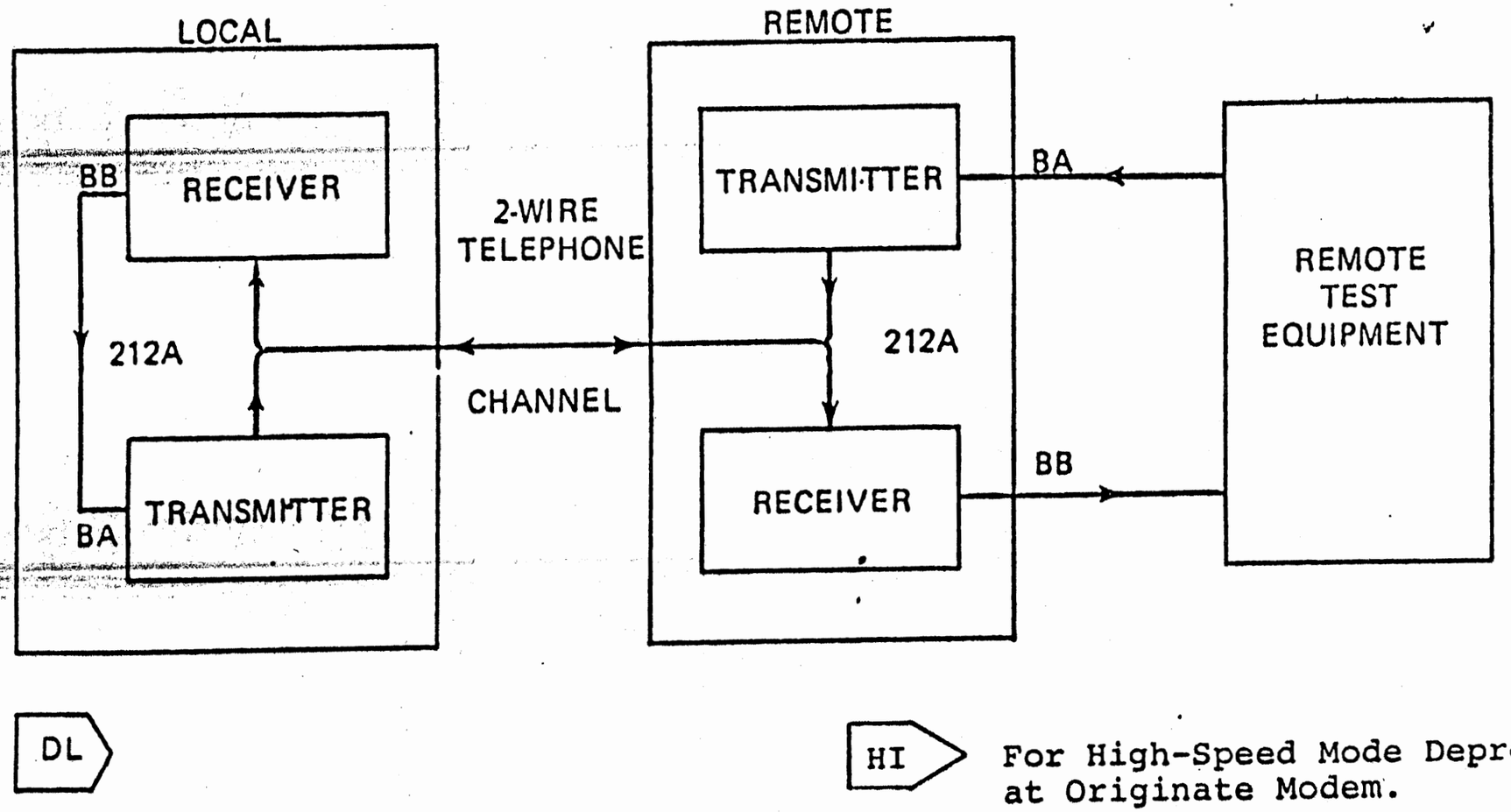
the ON state, and will loop the received data back to the transmitted data circuit, and connect the received timing to the transmit timing when in the data mode. Also, the interface circuits CC (DSR), CB (CTS), and CF (RCD) will turn OFF. The test lamp will turn ON indicating that the data set is in a test mode. The local data set can then be tested from the far-end by using terminal equipment at the far-end to transmit a test pattern and examine the looped data. At the far-end data set, all interface circuits will behave normally as in the data mode. At the conclusion of the test, the DL button is released, and the local data set is returned to the normal data mode automatically with control reverting to the customer CD (DTR) circuit. At the local data set, the Loss of Carrier option is forced ON for the duration of the test and the remainder of the time that the data set is in the data mode.

The Digital Loop test cannot be used in the high-speed mode if the far-end 212A has the Transmitter Timing Slave option installed.

At the end of the test, the far-end station can cause the local 212A to disconnect by hanging up the telephone connection after transferring to the talk mode, causing a loss of carrier. The local 212A is conditioned to disconnect on the loss of carrier by the DL function. Figure 6 shows the internal configuration of each data set during the test mode.

9.7 Digital Loop - Self Test

This test is the same as the Digital Loop test except that the test pattern is supplied by the far-end 212A internally, and the looped data are checked by the far-end data set. At the far-end 212A, the ST function is to activate these functions, and turn OFF the customer circuits CC (DSR), CB (CTS), and CF (RCD) for the



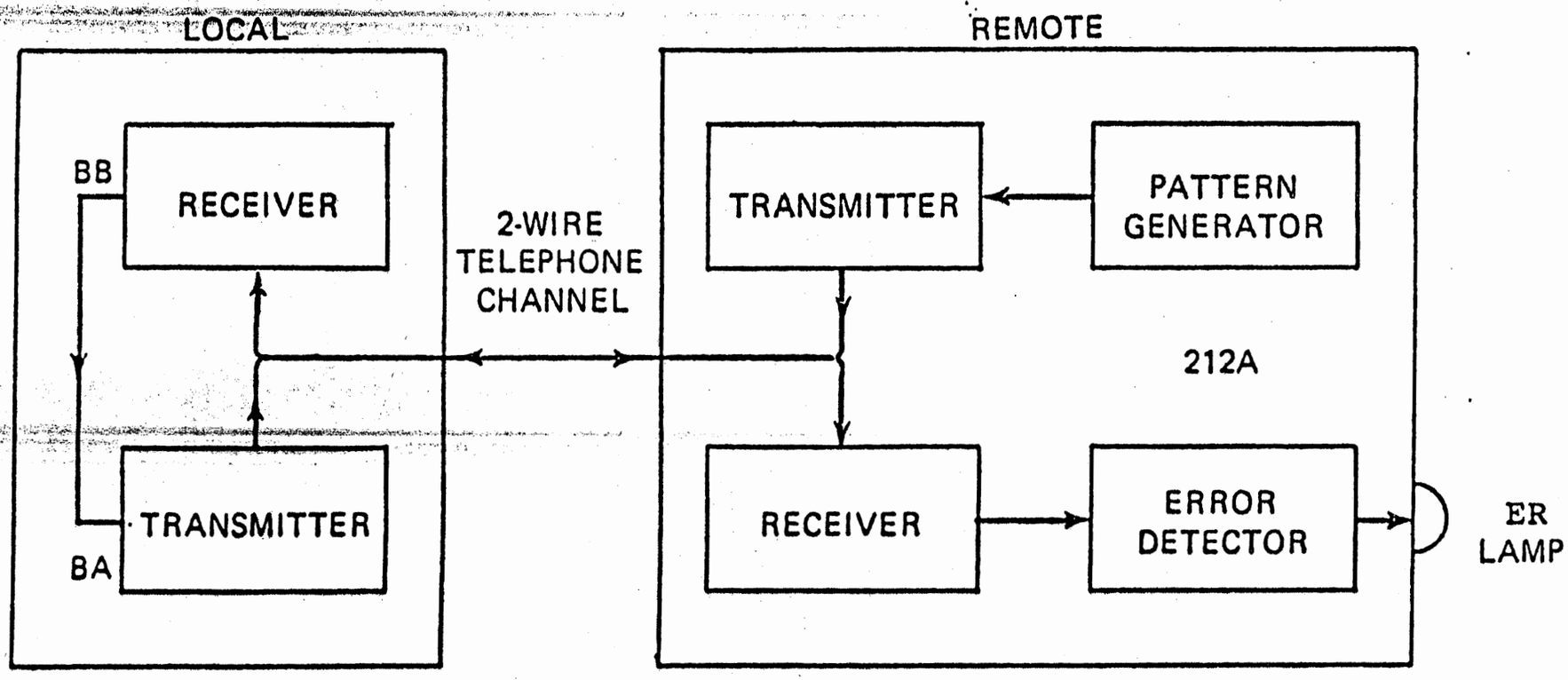
DIGITAL LOOP
FIGURE 6

duration of the test. At the far-end, the customer CD (DTR) circuit is forced ON internally, and the interface CD circuit is ignored. The error LED at the far-end acts as an indicator for the quality of the looped data by flashing ON whenever a received error occurs (high-speed) or the distortion of a received data bit exceeds 25% (low-speed). At the end of the test, the ST and DL functions are disabled and both data sets revert to the normal data mode if the customer CD circuits are ON. At the local 212A, the Loss of Carrier Disconnect option is forced ON for the duration of the data call. Figure 7 shows the configuration of each data set during the test mode.

9.8 Customer Test Interface Summary

	TEST			SELF - TEST				
TYPE	ANALOG	DIGITAL (1)		ANALOG	END-TO-END (2)		DIGITAL (3)	
PUSH BUTTON	AL	RDL OR DL		AL & ST	ST & ST		RDL & ST OR DL & ST	
I/O \ MODEM	LOCAL	LOCAL	REMOTE	LOCAL	LOCAL	REMOTE	LOCAL	REMOTE
DSR	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
CTS	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
RCD	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
TXD	DATA	DATA	(4)	(4)	(4)	(4)	(4)	(4)
RXD	DATA	DATA	MARK	MARK	MARK	MARK	MARK	MARK
DTR	ON	ON	(4)	(4)	(4)	(4)	(4)	(4)

Notes:
1. DL Depressed at Remote or RDL Depressed at Local
2. ST Depressed at Both Local and Remote
3. Either DL at Remote, ST Local or RDL and ST Local
4. Ignored by 212A



SELF-TEST DIGITAL LOOP
FIGURE 7

10.0 STATUS INDICATORS

Eight (8) LED indicators shall be provided.

MB	Make Busy	ON in AL Test
TD	Transmit Data	ON in Space Condition
ER	Error	Flashes or ON in ST When Errors Occur
HI	HI/LO	ON for 1200 bps Operation
MR	Modem Ready	ON After Mode Goes OFF On-Hook DSR
RD	Received Data	ON in Space Condition
TM	Test Mode	ON When Any Test is Performed
TR	Terminal Ready	ON When DTR is Enabled

11.0 PUSH BUTTONS

DL	Digital Loop-Back
TLK	TALK/DATA
ST	Self Test
HI	HI/LO Speed (1200/300)
RDL	Remote Digital Loop-Back
AL	Analog Loop-Back

12.0 DTE INTERFACE

TABLE

Interchange Circuits

Circuit	Circuit CCITT No.	Interchange Circuit Description	Pin #
AB	102	Signal Ground or Common Return	7
BA	103	Transmitted Data	2
BB	104	Received Data	3
CB	106	Ready for Sending	5
CC	107	Data Set Ready	6
	108/1	Connect Data Set to Line (CCITT)	
CD	108/2	Data Terminal Ready	20
CF	109	Data Channel Received Line Signal Detector	8
	111*	Data Signaling Rate Selector (DTE Source)	N/A
DA	113	Transmitter Signal Element Timing (DTE Source)	24
DB	114	Transmitter Signal Element Timing (DCE Source)	15
DD	115	Receiver Signal Element Timing (DCE Source)	17
CE	125	Calling Indicator	22
	140*	Remote Loopback	
CN	141	Local Loopback/M.B.	25
	142*	Test Indicator	
CI		Speed Mode Indication (From DCE)	12

*The numbers with asterisks are CCITT recommendation V.22.

13.0 DATA CALL TERMINATION

13.1 Abort Disconnect

The Abort disconnect feature is not optional, but is always activated when when the 212 enters the data mode as an answering data set. From the time that the CC (DSR) circuit turns ON, received carrier must be detected within 17.87 ± 0.15 seconds or the data set will go On Hook.

13.2 DTR Disconnect Option

The local 212 enters an irreversible disconnect sequence when the Data Terminal Ready (DTR) circuit is turned OFF during the data mode for more than 50 milliseconds, unless the data set is in certain test modes. If the Long Space Transmit Disconnect option is not enabled, the Data Set Ready circuit will turn OFF 68 ± 10 milliseconds after the CD (DTR) circuit turns OFF. If the Long Space Transmit Disconnect option is installed, then the data set enters the space transmit sequence, which is detailed in Section 13.4. The CD (DTR) circuit can be turned ON any time after the 50 milliseconds required for the OFF interval.

See Appendix A, Figure 2A for Timing Diagram.

13.3 Carrier Fail Disconnect Option

This option when enabled causes the 212 to terminate a data call when a substantial loss of received carrier energy is detected. The customer interface circuits CC (DSR) and CB (CTS) will turn OFF 433 ± 17 milliseconds after the carrier falls below the preset threshold (-30 dBm or -45 dBm). If the carrier is interrupted for less than 175 milliseconds, a disconnect will not occur; if a carrier interrupt lasts for more than 307 milliseconds, a disconnect will occur. The CF (RCD) circuit turns OFF 17 ± 7 milliseconds

after the loss of carrier, and turns ON 155 ± 50 milliseconds after the carrier is present at the receiver. If the 212 is put into the Digital Loop test mode (RDL or DL), this disconnect option is forced to the enabled condition.

See Appendix A, Figure 2A for Timing Diagram.

13.4 Long Space Transmit Disconnect Option

When this option is enabled, the space transmit sequence is initiated by either of two conditions:

1) Customer interface circuit CD (DTR) is turned OFF for at least 50 milliseconds.

2) The Loss of Carrier Disconnect ~~option is enabled~~ and the carrier detector has turned OFF for at least 307 milliseconds.

The space transmit sequence begins after one of the above events has occurred. The transmit data to the modulator is clamped to a space condition and the CF (RCD) circuit is turned OFF. After 3.95 ± 0.15 seconds has elapsed, the 212 will go On-Hook and CC (DSR) turns OFF. The sequence cannot be interrupted by any condition of the DTR circuit or a restoration of received carrier energy.

See Appendix A, Figure 3A and 4A for Timing Diagram.

13.5 Long Space Receive Disconnect

When the Receive Space Disconnect option is enabled, the 212 will go On-Hook when the received data circuit detects a scrambled condition for 1.6 ± 0.15 seconds. At the time of disconnect, the CC (DSR), CB (CTS) and CF (RCD) circuit will turn OFF. If the Remote Digital Loop feature is enabled in the 212 by the RDL front panel pushbutton, the Long Space Receive Disconnect option is overridden. At a 212 which is put into the Digital Loop test mode,

this option is similarly overridden. These overrides exist only as long as the 212 is in the test mode.

See Timing Diagrams for all other features (Appendix A).

APPENDIX A

Timing Diagrams WECO 212A Compatible

ORIGINATING STATION

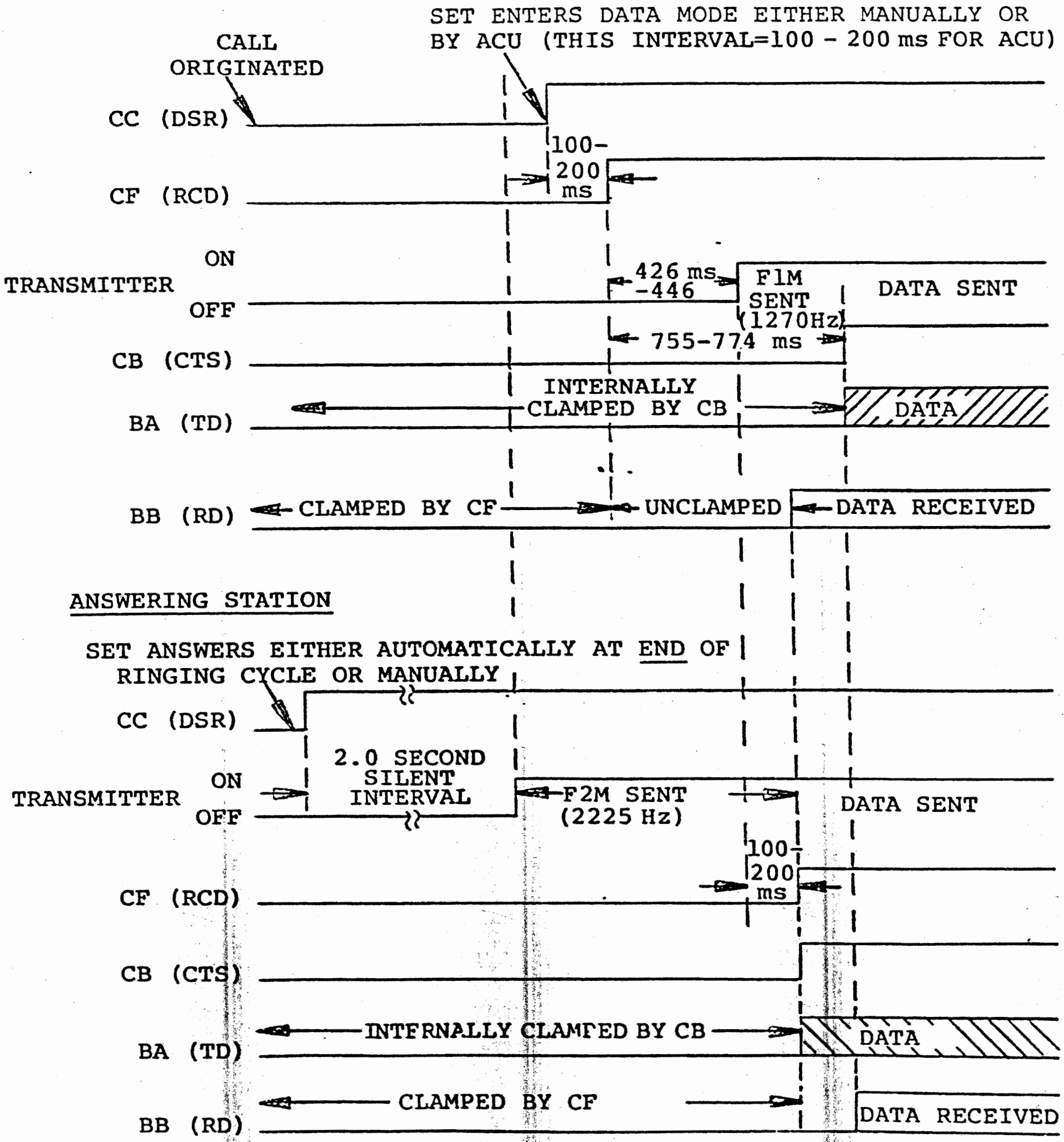
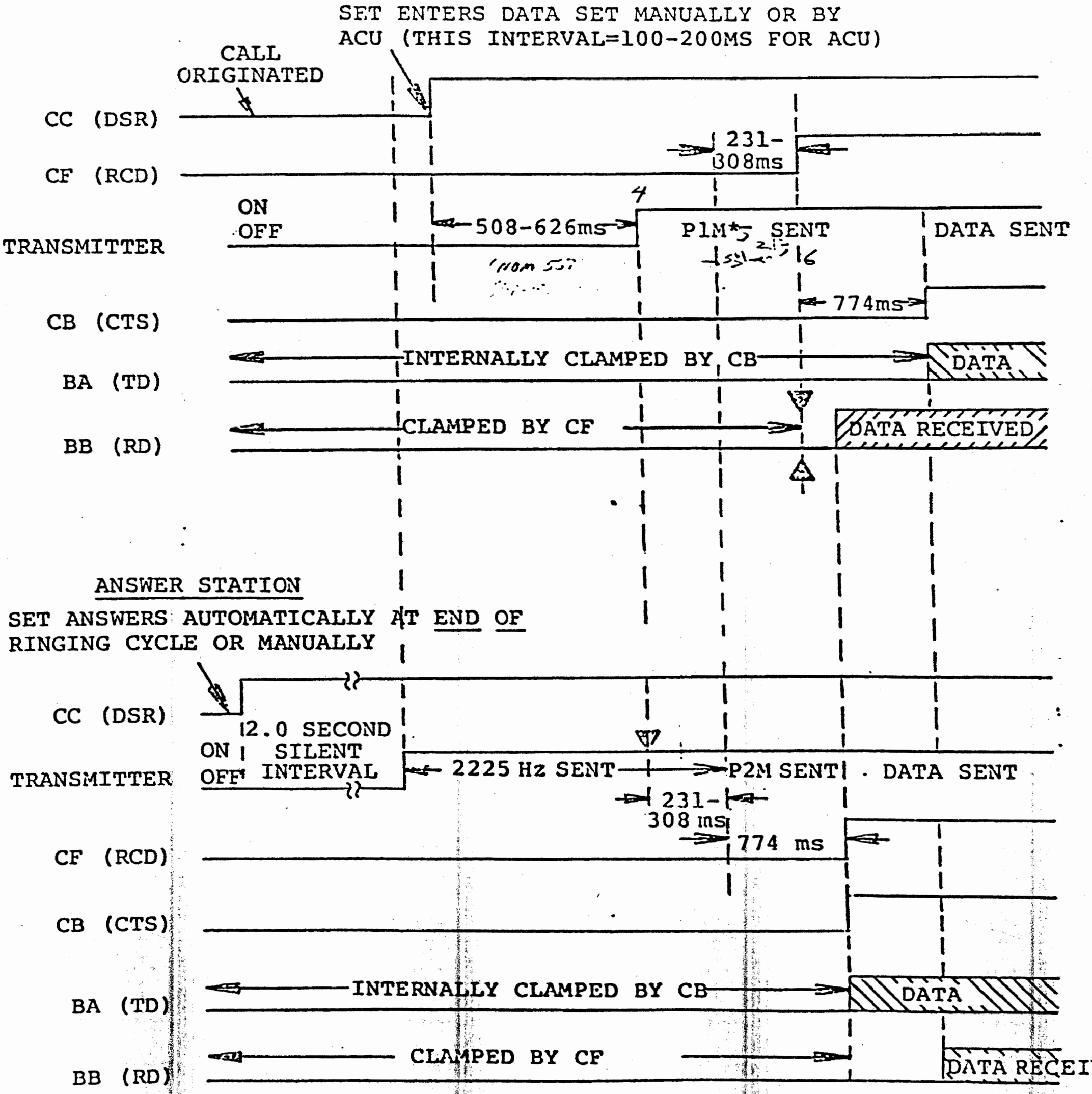


Figure 1A - 212A LOW SPEED CONNECT SEQUENCE
CD ON; EITHER AUTOMATIC OR MANUAL OPERATION

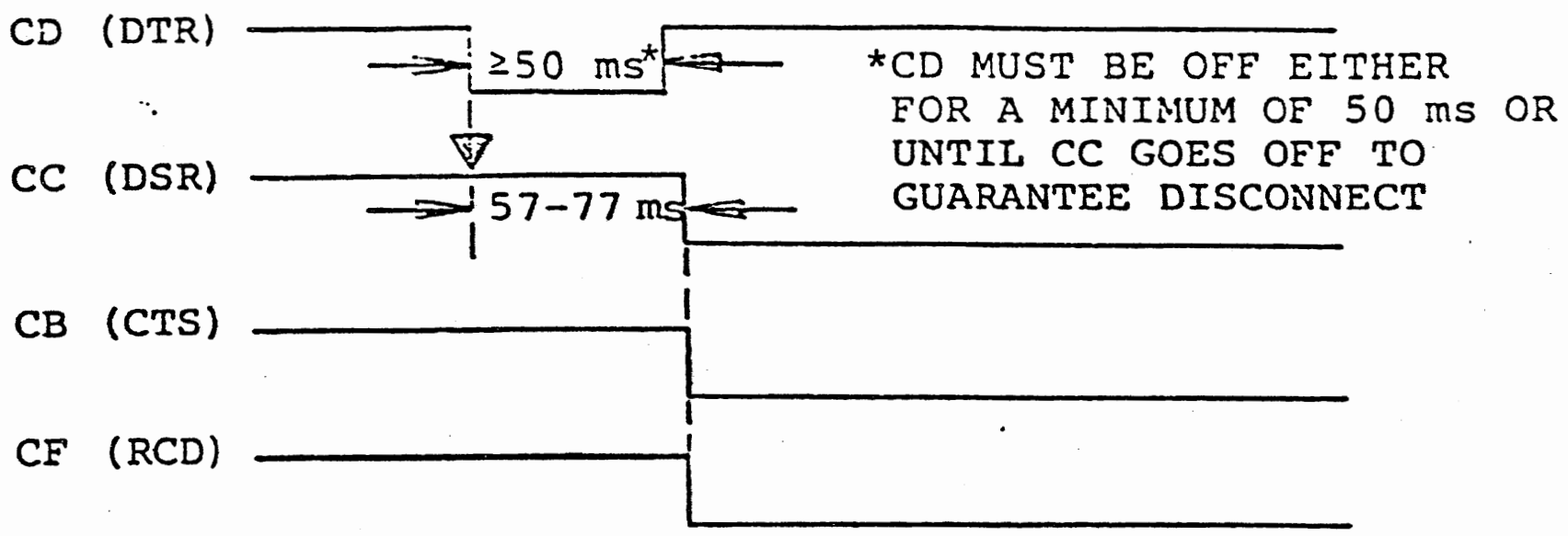
ORIGINATING STATION



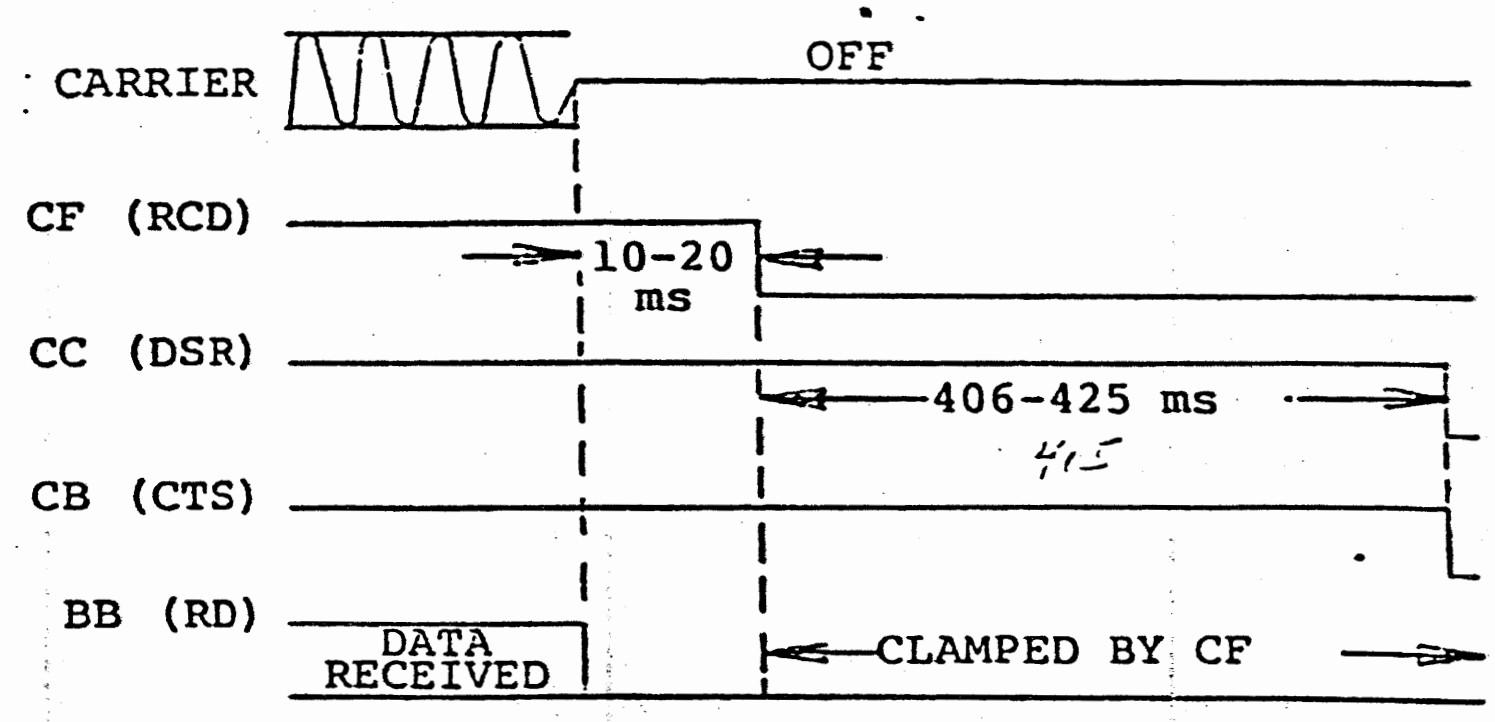
*P1M IS THE LOW BAND PHASE SHIFT KEYED SIGNAL REPRESENTING A MARKING DATA SEQUENCE. P2M IS THE SIMILAR SIGNAL IN THE HIGH BAND.

Figure 2A - 212A HIGH SPEED CONNECT SEQUENCE
CD ON; EITHER AUTOMATIC OR MANUAL OPERATION

CD DISCONNECT



CARRIER FAIL DISCONNECT (MAY BE USED WITH LONG SPACE DISCONNEC



DATA TO TALK TRANSFER

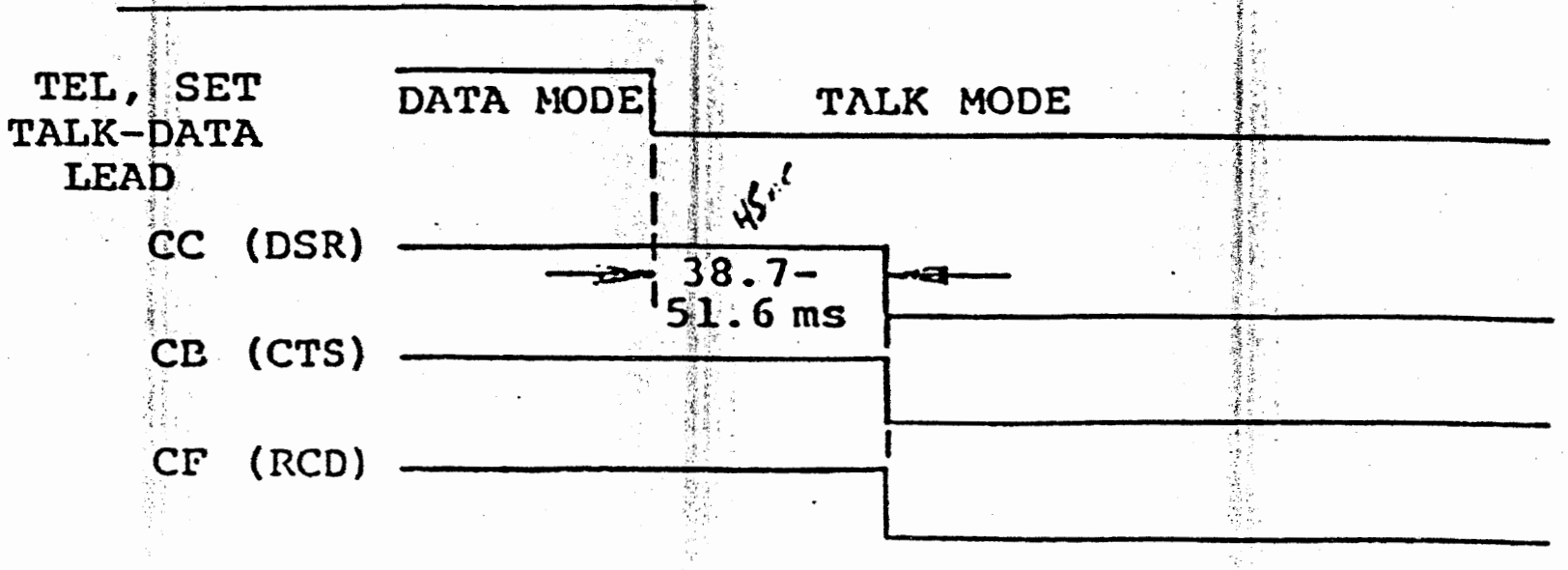
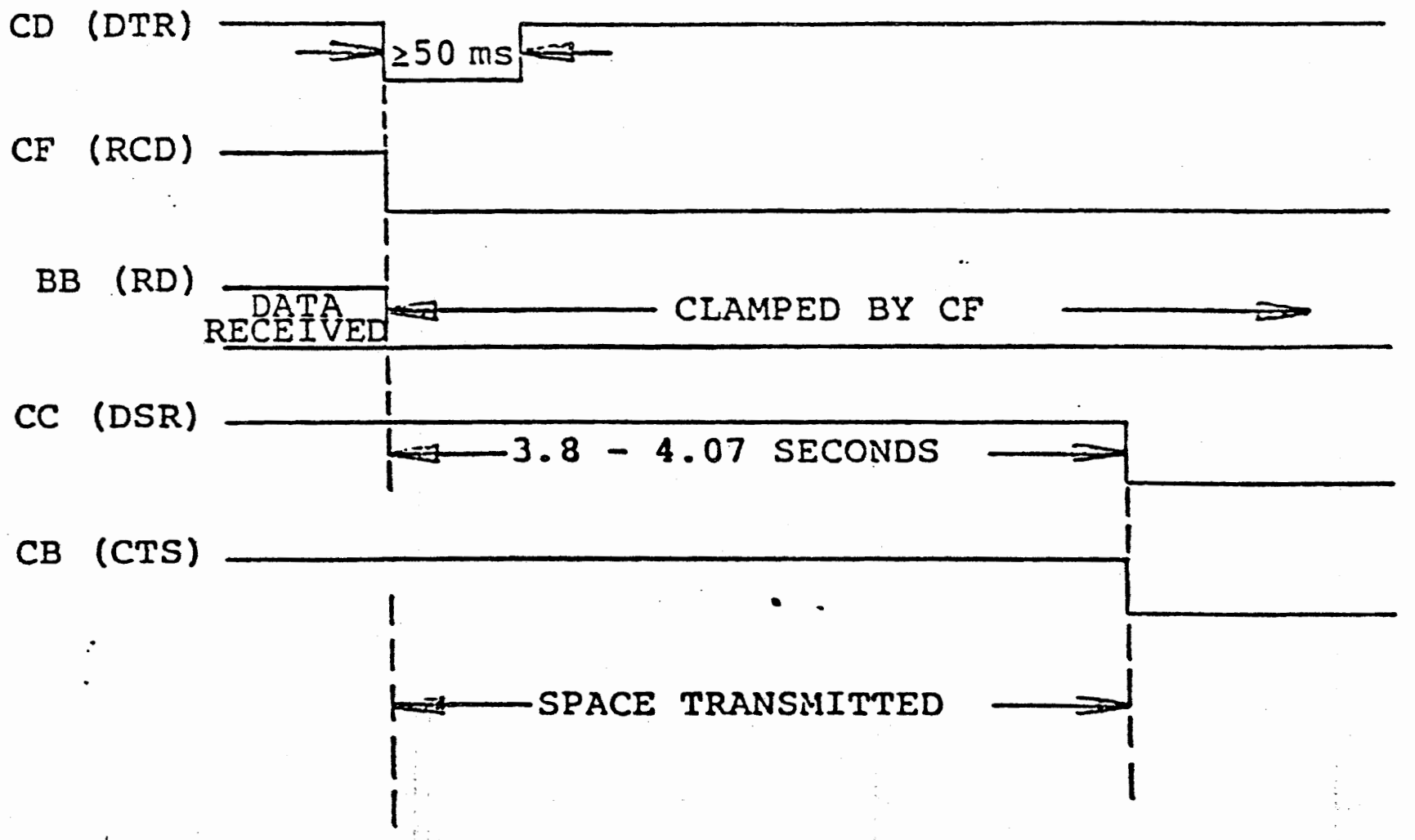


Figure 3A - 212A DISCONNECT SEQUENCES (HIGH OR LOW SPEED)

LONG SPACE TRANSMIT BY CD OFF (THIS END INITIATES DISCONNECT)



LONG SPACE DISCONNECT (THIS END DISCONNECTS UPON RECEIVING LONG SP

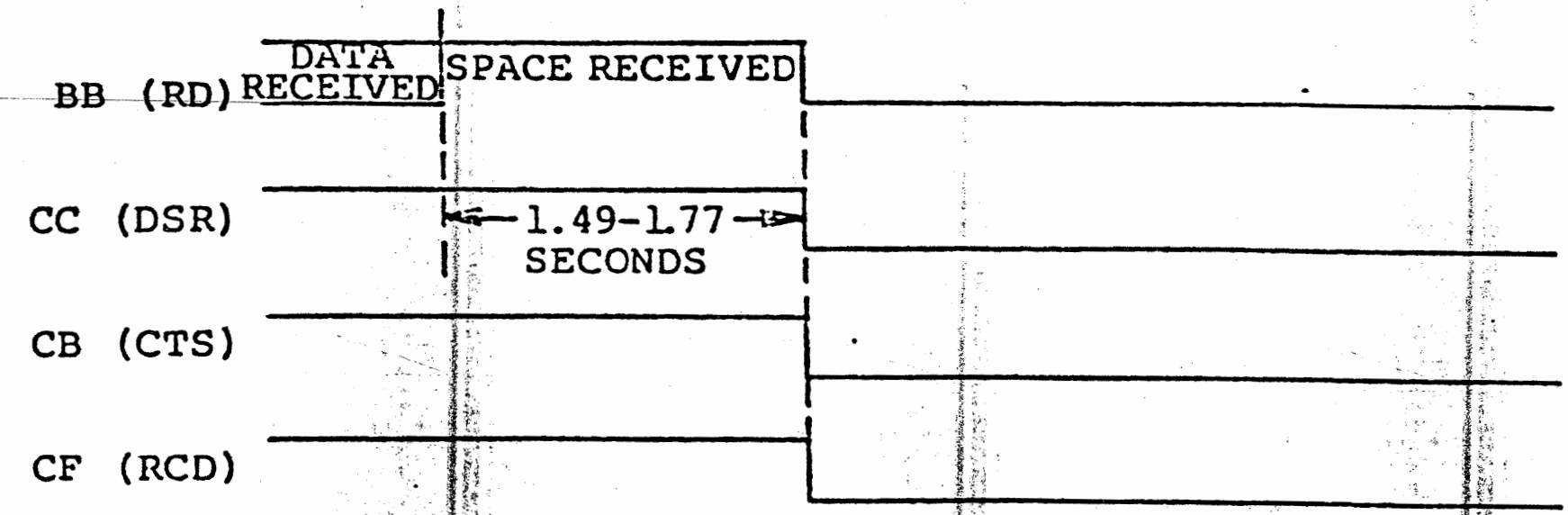


Figure 4A - 212A DISCONNECT SEQUENCES
(HIGH OR LOW SPEED)

LONG SPACE TRANSMIT BY CARRIER FAIL DISCONNECT

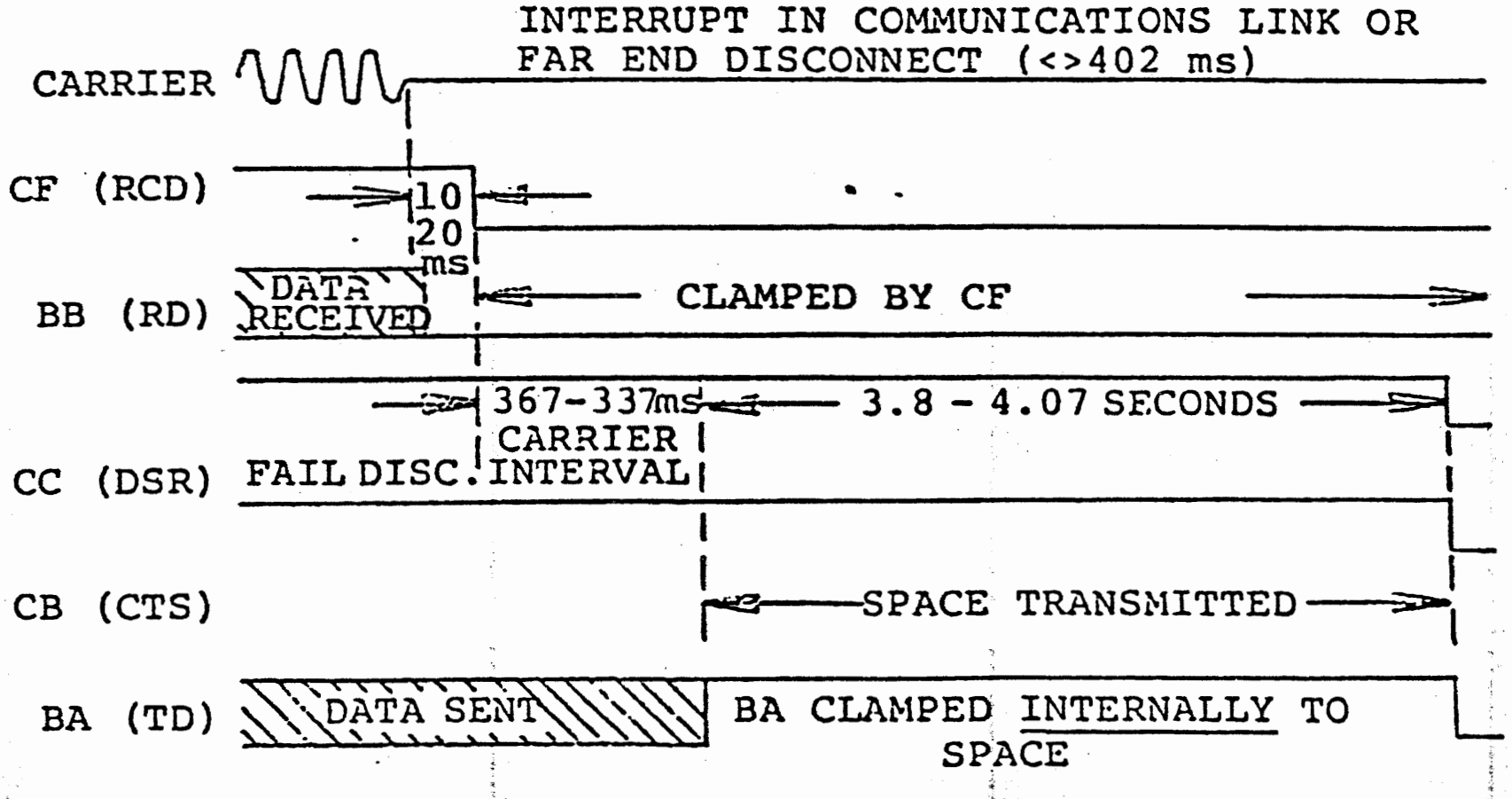


Figure 5A - 212A DISCONNECT SEQUENCES (HIGH OR LOW SPEED)