TeleVideo AT Technical Reference Manual

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TeleVideo Systems, Inc.

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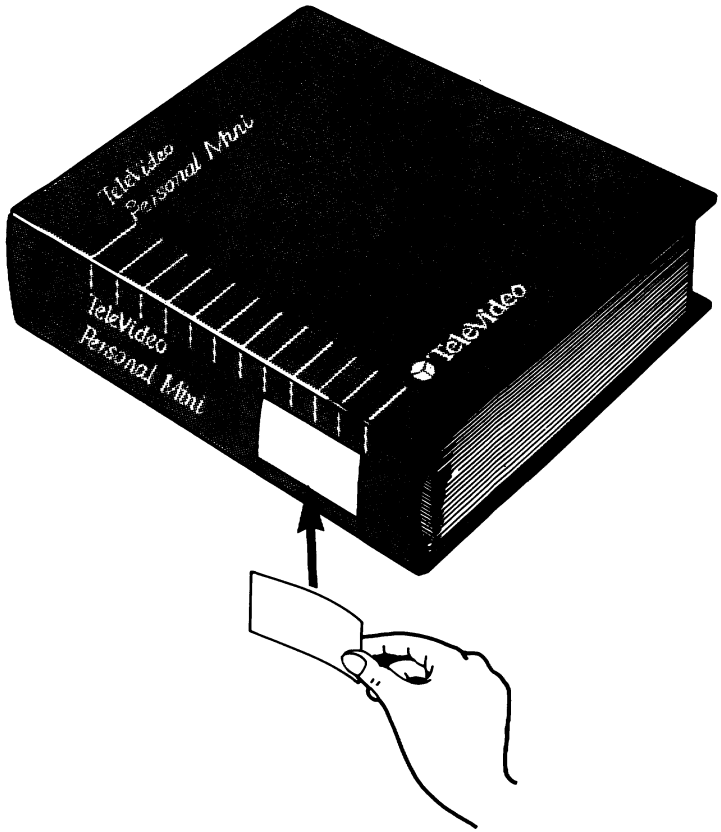

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FCC

This device is classified as either a Class A or Class B computing device. Class A devices may only be used in commercial, business, or industrial environments, whereas Class B devices have been approved by the Federal Communications Commission for use in residential areas by the general public. Check the FCC label on the bottom of your terminal to ensure that you have purchased the version appropriate for your end-use environment.

Class B Warning

This peripheral equipment has been certified to comply with the limits for a Class B computing device, pursuant to Subpart J of Part 15 of the FCC Rules, which are designed to provide reasonable protection against interference to radio and TV reception when operated in a residential environment. The use of good shielded I/O cables is required.

WARNING! There are no user serviceable parts inside the TeleVideo AT. All service should be referred to a qualified technician. Disconnect the power cord from the unit before opening or servicing the AT.

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1 OVERVIEW

INTRODUCTION TO THIS MANUAL

The information in the TeleVideo AT Technical Reference Manual is intended as a hardware reference for those who service or test the AT electronics, or those who write or modify system software for use with the TeleVideo AT. This manual describes only those circuits contained on the motherboard, diskette/fixed disk controller board, and high resolution graphics board (HGB). It does not cover monitors, keyboards, disk subsystems, or other peripheral devices plugged into the I/O channel slots. Separate manuals are provided for these devices.

Overview: The overview chapter of this manual provides a general description of the TeleVideo AT.

Chapters 2 - 4: These chapters provide block-level descriptions of the logic on the motherboard, diskette/fixed disk controller board and HGB.

Chapters 5 - 7: Programming aspects of the AT are described in chapters 5 through 7. Subsections within these chapters are divided with regard to the function performed in the system. Subsections in chapters 2 through 4 parallel those in chapters 5 - 7.

Chapter 8: The "Interface" chapter details the pin-outs and signals for the internal and external connectors in the system.

These eight chapters are supported by information contained in four appendices:

Appendix A: "Specifications" describes the electrical, physical, environmental, memory and peripheral information regarding the TeleVideo AT.

Appendix B: "DIP Switch Settings," identifies the settings for CPU speed, color/graphics or monochrome adapter, and motherboard RAM.

Appendix C: "Jumper Configurations," describes the jumper configurations on the motherboard for selecting I/O port addresses and on the diskette/fixed disk controller board for selecting the primary address port.

Appendix D: "Logic Diagrams," contains the logic diagrams of the motherboard, HGB, and power supply, and an assembly drawing showing component, jumper, and connector locations on the motherboard.

INTRODUCTION TO THE TELEVIDEO AT

The TeleVideo AT is a high-performance 16-bit computer configurable as either a single- or multi-user system, depending on the function of add-on circuit boards. The TeleVideo AT is fully hardware and software compatible with the IBM PC AT.

The basic AT system is supplied with a motherboard, 220-watt switching power supply, and eight I/O channels (hardware slots) that can accommodate a very broad range of peripherals, controllers, and communication adapters.

In addition to the motherboard described in this manual, a typical user configuration for the TeleVideo AT also includes a monochrome or color monitor, two floppy disk drives (one 48-tpi drive and one high-capacity 96-tpi drive), one hard disk drive of 20 or 44 megabyte capacity, and a detachable keyboard.

The motherboard contains a high-performance Intel 80286 CPU, an 80287 Numeric Coprocessor (optional), two 8237A DMA controllers, two 8259A interrupt controllers, a three-channel 8254 counter/timer circuit, and a Motorola MC146818 real-time clock (with battery backup). Motherboard memory consists of 256K, 512K or 640K bytes of RAM with parity checking and up to 128K bytes of EPROM. Additional circuits on the motherboard include an 8042 keyboard controller, one RS-232C serial port, a parallel printer port, and hardware necessary for controlling the timing of these circuits, and the eight I/O channels.

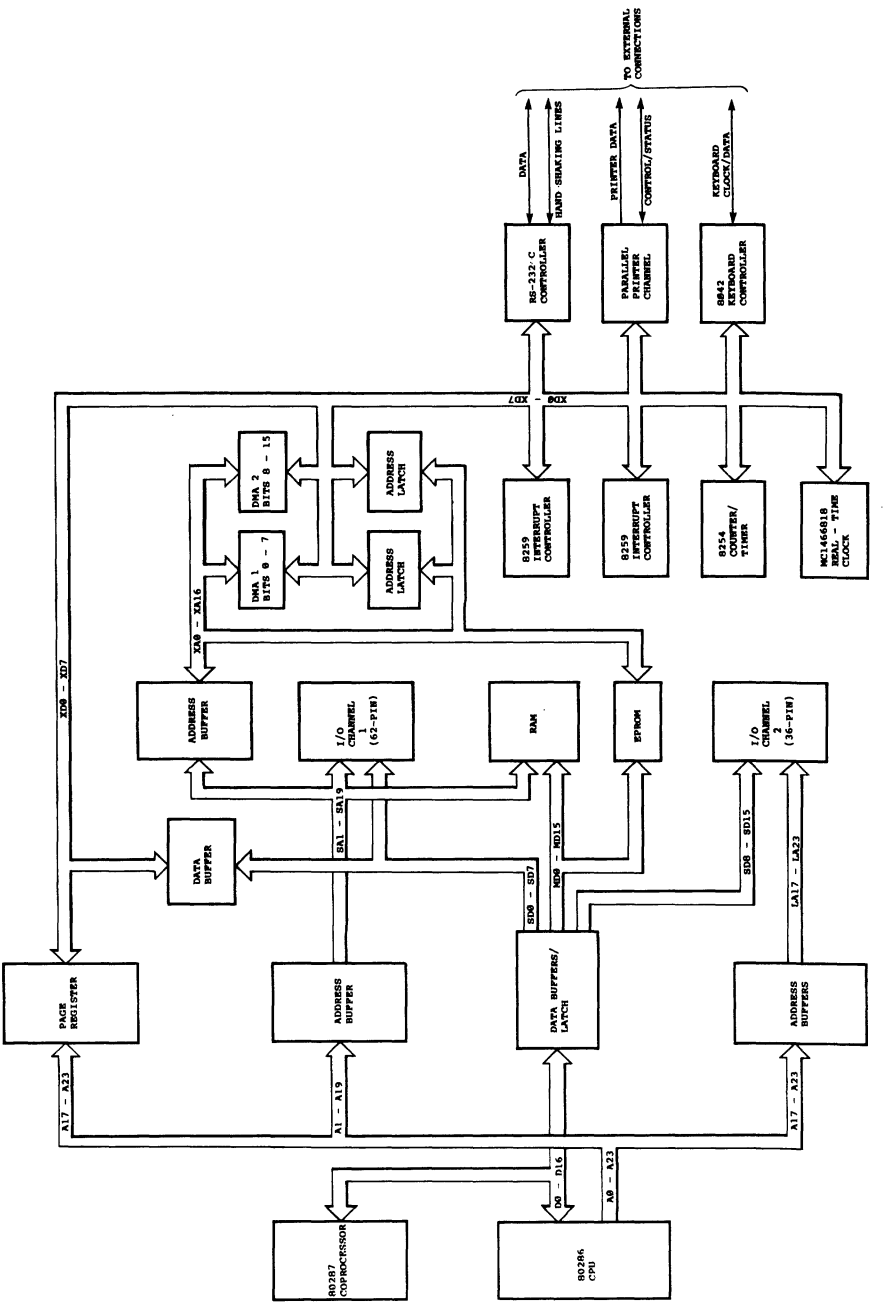
2 HARDWARE FUNCTIONS - MOTHERBOARD

INTRODUCTION

The TeleVideo AT computer is based on a 16-bit Intel 80286 CPU with a switch selectable execution speed of 6 or 8 MHz. The default execution speed is 8 MHz.

A companion numeric coprocessor circuit, the Intel 80287, can be plugged into the system motherboard to expand the architecture of the CPU to include hardware processing of floating point, extended integer, and BCD data types. Figure 2-1, TeleVideo AT Functional Block Diagram, shows the major functional blocks of the system.

Figure 2-1
AT Functional Block Diagram



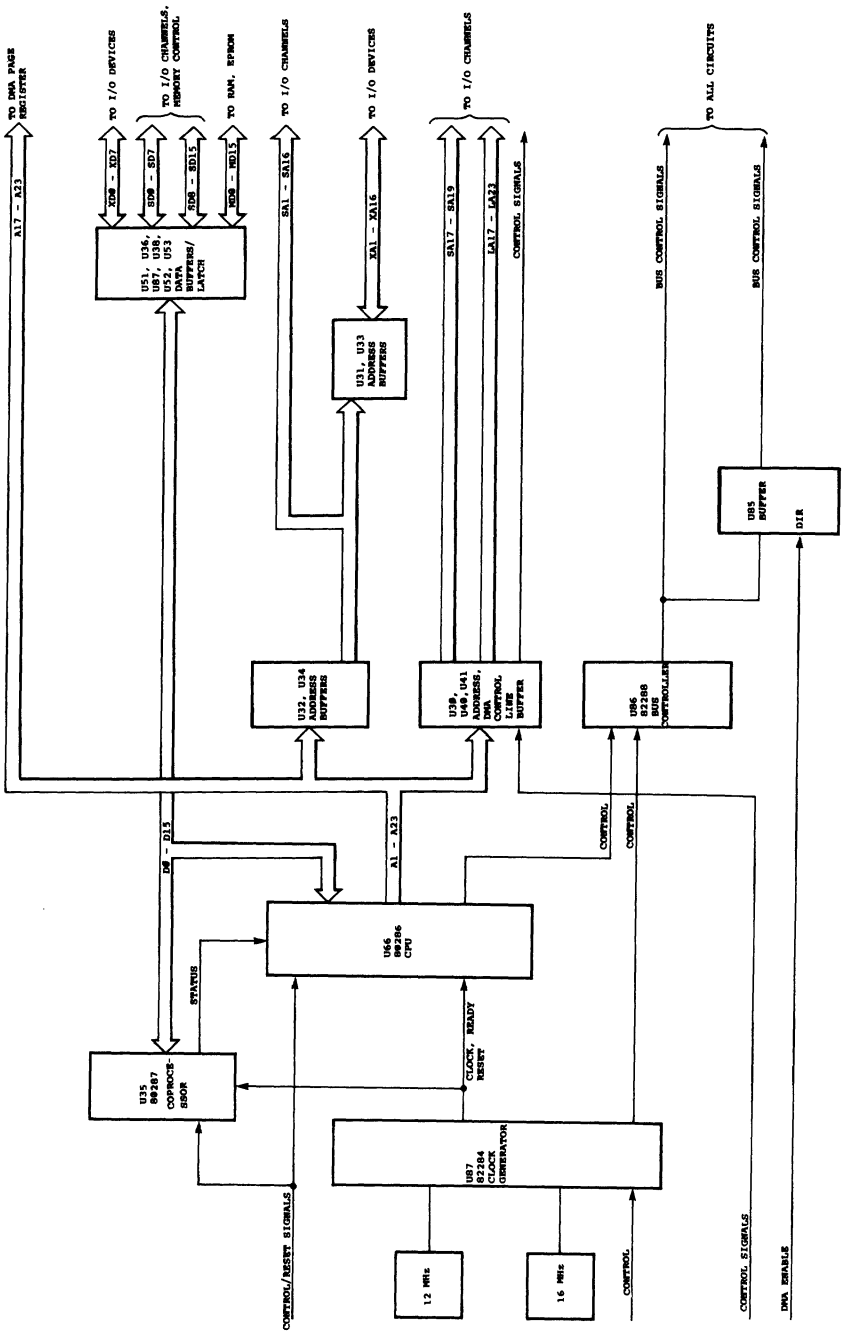
80286 CENTRAL PROCESSING UNIT

See Figure 2-2, Processor and Bussing Block Diagram, during the following discussions (note that sheet numbers refer to the TeleVideo AT Motherboard Schematic).

On the right side of Sheet 2, the Intel 80286 CPU at U66 is a high-performance microprocessor with specially optimized features useful in multi-user/ multi-tasking systems, such as the TeleVideo AT. The CPU directly addresses up to 16 megabytes of memory and 64K bytes of I/O addresses through 24 address lines A0 - A23. Data is transfered between U86 and memory of I/O devices in 16-bit words or 8-bit bytes through the data bus lines D0 - D15.

Operational details of the 80286-family of devices used in the TeleVideo AT is given extensive attention in the Microsystem Components Handbook, published by the Intel Corporation.

Figure 2-2
Processor and Bussing Block Diagram



CPU Support Circuits

The 80286 requires two support circuits to function properly in the TeleVideo AT system. First, clock, ready, and reset signals for the CPU are provided by U87, an Intel 82284 Clock Generator and Ready Interface shown on the left side of Sheet 2 of the schematics. The 82284 Clock Generator conditions (squares up) the clock, and provides reset and ready signals synchronized to the clock.

Switch 1 of SW1 (Sheet 12) controls the selection of the clock source to be sent to the CPU. When Switch 1 is open, the 6 MHz/8 MHz line to clock generator is high to enable the output of 16-MHz oscillator U67 at the 82284's EFI input to provide the clock for the CPU. The CPU internally divides the clock by two to arrive at the 8-MHz processor speed. If switch 1 is closed, the 12-MHz crystal across the X1 and X2 inputs of the clock generator provides the clock to the CPU.

The RESET output of the 82284 generates a reset signal from an RC circuit composed of R1 and C3 to provide a power-up reset to the CPU and the 80287 coprocessor.

Other reset signals from Sheet 11 of the schematics (RESET 286, RESET 287 and RESET 287 BUSY) are NORed with the power-up reset at gates U88 and U50. Two of these reset signals, RESET 286 and RESET 287, are software resets. RESET 286 is used when software must switch the CPU from its Protected mode to its Real-Address mode. RESET 287 is used by the CPU to reset the 80287 in the event of that device encountering an error in execution. The READY- output of the 82284 clock generator is low whenever the current CPU instruction cycle is complete.

The second supporting circuit required by the CPU is the Intel 82288 Bus Controller, shown on Sheet 1 as U86. The 82288 generates 80286 control signals for the various 8-bit I/O devices on the motherboard and 8- or 16-bit devices on the I/O channels. Control input lines to the Bus Controller include the system clock, READY- output of the 82284 clock generator, S0 and S1 control outputs of the CPU, and the COMMAND OFF- and Command Delay (CMDLY) lines from the memory controller logic.

Based on these input signals, the 82288 Bus Controller generates memory and I/O read and write signals, the Interrupt Acknowledge (INTA-) line from the CPU to an interrupting I/O device, Data Enable (DEN), Address Latch Enable (ALE), a memory or I/O selection line, and a Hold Acknowledge (HLDA) line to the DMA circuits. Buffer U85 and inverters at U106 buffer most of these lines to other circuits on the motherboard.

Wait-State Generation

Wait-state generation circuits and the logic that controls the 8/16-bit conversion buffer U37 is on Sheet 6 of the schematics.

A wait-state causes the CPU to extend one or more clock cycles into any memory or I/O read/write cycle to accommodate I/O devices that cannot respond in the time allocated to a normal I/O or memory read/write cycle. For I/O devices or memory on the motherboard, the number of wait-states can range from one to a maximum of four, depending on the internal speed of the device.

For I/O devices or memory on the I/O channels, 6-MHz operation requires up to four wait-states for all 8-bit processing and one wait-state for 16-bit operations; 8-MHz operation requires up to six wait-states for 8-bit processes, one wait-state for 16-bit memory processes and two wait-states for 16-bit I/O operations.

All devices may request as many wait-states as required for reliable operation of the device. Note that too many wait-states will effect the operation of the memory refresh generation logic. The wait-state generation circuits consist of ten flip-flops clocked by SYSCLK- and controlled by a custom circuit at U98. Certain conditions, such as a request for zero wait-states from hardware on the I/O channels (OWS), the 6-MHz/8-MHz CPU clock setting, and the memory or I/O (M/IO) selector determine the output of U98, which in turn, determines the number of wait-states generated at the COMMAND OFF- output of the circuit.

During a normal 8-bit I/O cycle, four wait-states are generated. This is in addition to two wait-states the CPU adds during execution of an I/O cycle. This wait timing of almost 1.0 microsecond (actually 996 nanoseconds) makes the I/O cycle timing compatible with the earlier 8088-based PC-type machines. For 16-bit I/O operations, the total wait timing is about 500 nanoseconds. System memory requires one wait-state; faster memory hardware on the I/O channels can request that no wait-states be inserted in the cycle.

On the bottom of Sheet 6 is the control logic for buffer U37. As stated above, this buffer controls the conversion between 16-bit I/O devices in the system and 8-bit I/O devices. The control logic generates two signals, GATE245- and DIR245 from the outputs of a custom circuit at U99. This custom circuit uses the MEMR- and MEMW- to select the direction of data flow in the buffer; XA0, AEN1-, AEN2-, XBHE-, and IOR-, in conjunction with FSYS16- and IOCS16-, determine when the buffer is gated. FSYS16- and IOCS16- come from the I/O channels to indicate that an addressed memory or I/O device on the I/O channel is capable of word length data transfers.

On Sheet 11 three I/O decoders at U77, U78, and U79 decode many of the I/O addresses, that is, chip selects and control signals, used by the system's devices. The decoders are addressed using the XA0 - XA9 address lines and the XIOR- and XIOW- read and write strobes.

80287 NUMERIC COPROCESSOR

On Sheet 2 of the schematic, the Intel 80287 numeric coprocessor at U35 is upward-compatible with the Intel 8087 coprocessor used in PC-type systems. The numeric coprocessor operates in parallel with the CPU to provide hardware processing of floating point, extended integer, and BCD data types. Using the 80287 to process these operations in hardware is much faster than using the 80286 CPU to implement an equivalent function in software. While the 80287 receives the same 12-MHz or 16-MHz clock output of the 82284 clock generator, it internally divides the clock by three to operate at either 4.00 or 5.33 MHz.

The CPU regards the 80287 coprocessor almost like any other I/O device, such as the DMA or interrupt controller, in the sense that IOW- and IOR- control signals are used for communication. U35 is connected to the data bus through D0 - D15. If the coprocessor encounters an error in the execution of an instruction, flip-flop U61 generates interrupt request (IRQ13) to the interrupt controller U21. The CPU then interrogates the interrupt controller, services the interrupt, and resets the flip-flop using the RESET 287 BUSY line.

SYSTEM CLOCK AND CPU RESET

The circuitry on the top half of Sheet 5, composed of gates in U84 and a flip-flop at U121, generates the 6-MHz or 8-MHz system clock for the eight I/O channels and some circuits on the motherboard. Another flip-flop at U121 generates a 3-MHz or 4-MHz clock for the DMA controller. Both clocks are synchronized to the clock derived from the CLK output of the 82284 clock generator and used internally by the CPU.

Finally, a gate at U120, and flip-flops at U139 and U140 generate RESET 286. RESET 286 is a stretched pulse required by the CPU and generated when 1) the logic detects that the CPU is in a shut down condition as indicated by the state of the S0 and S1 lines from the CPU, or 2) a software reset changes the CPU from the protected-address mode to the real-address mode.

MC 146818 REAL-TIME CLOCK

On Sheet 13, the Motorola real-time clock at U19 serves two functions in the TeleVideo AT. First, it supplies time and date information to the CPU. Secondly, the real-time clock contains 50 bytes of RAM used by the system to store system configuration. Data to or from the real-time clock is transferred on the XD0 - XD7 data lines and controlled using several I/O signals decoded by decoder U78 (Sheet 11). The time base is supplied by a 32.768-KHz crystal at Y2. The time, date, and memory are retained by a lithium battery backup circuit made up of transistors Q1, Q2, and Q3 and a 6.0-volt lithium cell at connector J23. When the system is off, that is, once the +5-volt power in the system drops below 3.5 volts, the battery backup circuit allows current from the battery to flow to the clock. Otherwise, the battery is not used. The battery itself has a shelf life of over five years and can supply continuous current to U19 for about 1.5 years. The battery is replaceable.

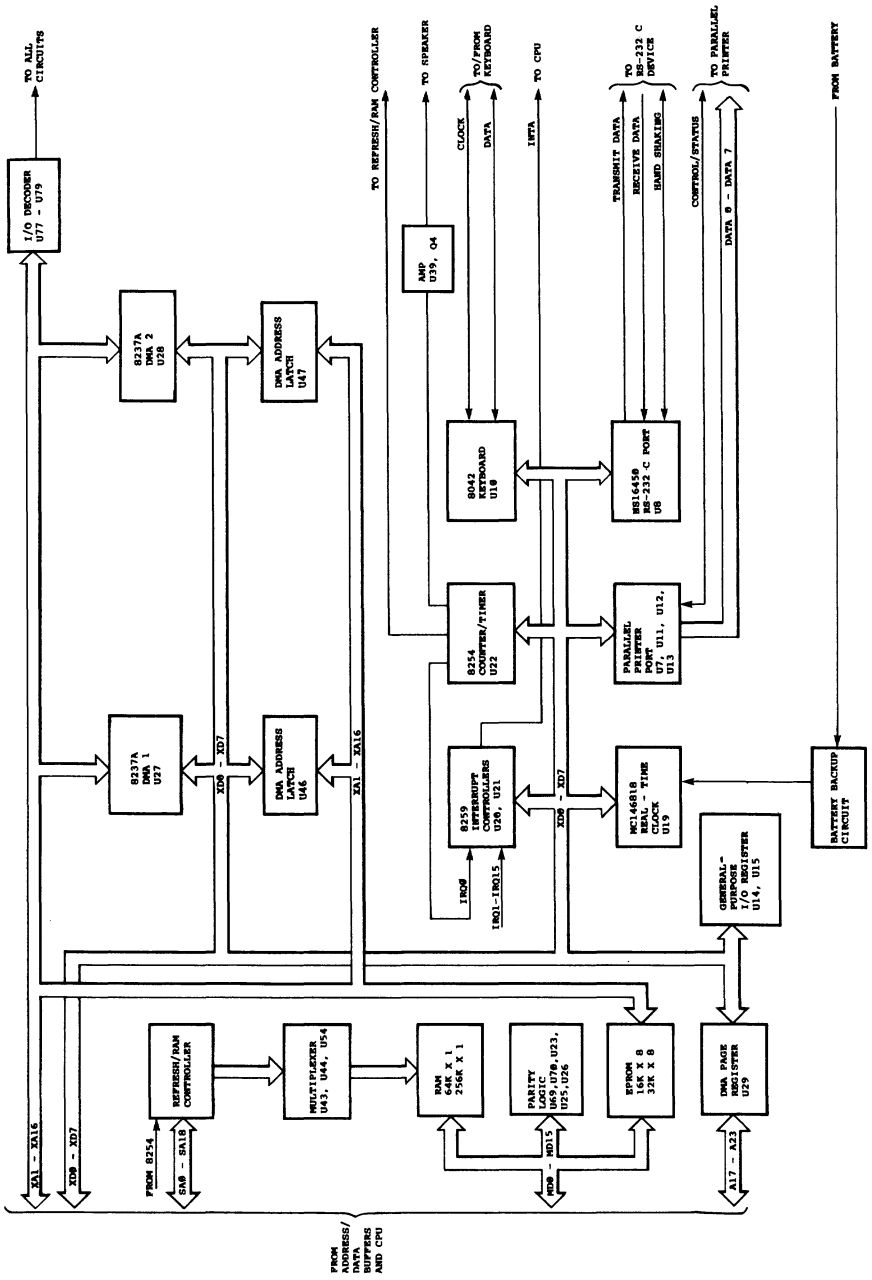
SYSTEM EPROM

On the top half of schematic Sheet 9, four EPROMs can be accommodated. There can be two types: 16Kx8-bit (27128) or 32Kx8 (27256). Jumpers W3 and W4 select XA15 and XA16 address line assignments for each type. The EPROMs operate in parallel using the XA1 - XA16 lines for address and the MD0 - MD7 lines for data. The Chip Enable (CE) input for the EPROMs occurs through the EPROM CS- line from address latch U41 (Sheet 3). All four EPROMs are enabled at the same time; however the Output Enable (OE) input for each EPROM is unique as gated by U126 and inverter U24.

SYSTEM MEMORY CONTROL AND ORGANIZATION

See Figure 2-3, System Memory and I/O Device Block Diagram, during the following discussions. The system memory control circuits operate to refresh the complement of dynamic RAMs in the system. The circuits also generate the proper timing for access of memory locations by the CPU or DMA controllers.

Figure 2-3
System Memory and I/O Device Block Diagram



SYSTEM RAM

Motherboard memory may be composed three ways:

1. 256 Kbytes using 36 - 64 x 1 RAM chips
2. 512 Kbytes using 18 - 256 x 1 RAM chips
3. 640 Kbytes using 18 - 256 x 1 RAM chips and 18 - 64 K X 1 RAM chips.

External RAM can be added by expansion cards on the I/O channels to bring the total RAM complement to 15 megabytes. The dynamic RAMs are refreshed by a separate memory refresh controller, unlike the previous PC-type systems, which use DMA to provide refresh. Up to four 16 Kbyte or 32 Kbyte EPROMs can be installed in the TeleVideo AT.

On Sheets 8 and 8A, two banks of RAM are present in the system. Each bank consists of a high and low byte. Nine RAMs per byte are required: one for each data bit plus one for a parity bit. The respective row and column address signals, RAS0, RAS1, CAS0L, CAS0H, CAS1L, and CAS1H are sent to their respective banks and bytes. Address lines SA0 - SA18 are sent to multiplexers U43, U44, and U58 to specify the row and column addresses of the memory location. ADDR MUX is delayed 40 nanoseconds from the memory read or write strobe by U72.

Data to and from the RAMs is transferred over the MD0 - MD15 memory data lines to buffers U52 and U53 as discussed above. When data is written into the RAMs, RAM WR- from U40 is active during the time that data is on the memory data lines.

Memory Controller

The memory controller on schematice Sheet 7 generates control signals necessary to access the locations in memory. U56 is a custom memory decoder that generates row and column address strobes, and RAM and ROM selection lines. Inputs to this decoder are address lines A17 - A23, MEM CS 16- from the I/O channels to indicate a word operation, REFRESH- from the refresh controller to indicate that a refresh cycle is active, and three lines from switches at SW1 (Sheet 12) indicating how much memory is in the system.

During a memory read or write cycle, the outputs of U56 are latched at U57 by ALE. The RAS and CAS signals are sent to gates at U74 and U75 to generate the row and column address strobes while the RAM and ROM selection lines are sent to enable their respective devices. The MEMR- or MEMW- strobes are also delayed by delay line U72 to stagger the generation of the RAS and CAS signals. CMDLY is sent to the 82288 Bus Controller during I/O operations only to delay generation of the I/O read or write strobes. The RAMs receive their address in a multiplexed fashion; one of 256 row address is applied to the address inputs of the RAM while RAS- is active. Next, one of 256 columns is specified at the address inputs while CAS- is active.

Memory Refresh Controller

Dynamic RAMs must be refreshed at certain intervals order to retain their data. Refreshing is accomplished by, one at a time, strobing all 128 or 256 row (128 refresh cycle or 256 refresh cycle) addresses of the RAM array. A normal memory access by the CPU or DMA controllers requires that a row address and a column address be used to specify a valid address.

The TeleVideo AT can use two types of RAM: either 64Kx1-bit or 256Kx1-bit RAMs. The "128 refresh cycle" RAMs must have all their row address lines strobed (refreshed) within 2 milliseconds if they are to retain their data; "256 refresh cycle" RAMs allow 4 milliseconds for a complete refresh.

Memory refresh controller logic also arbitrates requests to access the memory by the refresh controller and DMA controllers during a CPU cycle. The circuitry to generate refresh signals for memory is located on the bottom half of Sheet 5.

Two signals are necessary to refresh a row of memory: a refresh address and a memory read signal. The refresh address must be incremented from 0 to 255 to refresh all of the rows of memory in the system. Every 15 microseconds, Counter Channel 1 of U22 times out to generate REFRESH TIME OUT, which starts the refresh access. Counter U42 (LS590) generates the refresh addresses on the SA0 - SA7 system address lines. The counter is clocked from the REFRESH line from pin 6 of U105 to increment the address on its outputs. The pin 3 Q- output of U107 gates the address to the counter's outputs. When the refresh address is incremented, U107 also forces a memory read signal as System Memory Read (SMEMR-).

Bus Arbitration

During the time that a row of RAM is being refreshed, the refresh controller places the CPU in a hold state so that it does not try to generate a memory address. When REFRESH TIME OUT occurs and no DMA request is pending on the DMA 2 HRQ line, the refresh controller generates CPU HRQ. When the CPU acknowledges that it is holding (HLDA), the refresh controller gets control of the address bus and generates REFRESH. After a row of RAM has been refreshed, the refresh controller removes the hold request and hands control of the address bus back to the CPU.

Similarly, since the refresh controller is also competing with the DMA controllers for access to the memory, DMA operations must wait until a row of RAM has been refreshed. If the DMA controllers request the address bus while DMA 2 HRQ and REFRESH TIME OUT are active, the arbitration logic ensures that DMA will not be granted its request until a row of memory has been refreshed. Otherwise, the DMA controller will be allowed to take control of the address bus.

Parity Logic

The parity logic is composed of parity generators U69 and U70, and several gates and flip-flops at U23 through U26. The parity generators operate by examining the bit pattern of a data byte as it is written into a location in RAM on the MD0 - MD7 memory data lines.

For example, assuming that an even parity is desired, if the bit pattern written into the RAM location contains an odd number of 1 bits, e.g., 00100011, the parity generator for that bank of RAM (either U69 for bank 1 or U70 for bank 0) stores a 1 by generating a 1 on its EVEN output. The EVEN outputs of U70 and U69 are stored in the RAM as PAR DOUT 0 and PAR DOUT 1. The resulting nine bits stored in RAM then contain an even number of 1s or 00100011(1). When the same RAM location is read back at a later time, the bit from the parity RAM (PAR DIN 0 or PAR DIN 1) is also read.

As long as the parity generator still sees an odd number of 1 bits in the data byte and a 1 in the parity bit, the parity generator will assert its EVEN output (note that since a memory-read operation is taking place, the EVEN output of the parity generator is not stored in the parity RAM; it is just thrown away). If the data bits plus the parity bit do not contain an even number of 1s the ODD output of the parity generator goes high.

The ODD outputs of the parity generators are sent to logic that generates a non-maskable interrupt (NMI) to the CPU. The odd parity bit that caused the error is latched into U25. The Q output of U25 is sent to other gates that generate the NMI input to the CPU. The Q- output is sent to buffer U15 on Sheet 12 as a parity check signal (PCK on Sheet 12) where it is transferred to the XD7 data line to the CPU. When the CPU receives a NMI, it immediately goes to a software routine that tries to identify which RAM location generated the parity error. An NMI can also be generated by expansion memory hardware on an I/O channel by asserting an I/O channel memory check (IO CM CK-).

8237A DIRECT MEMORY ACCESS (DMA) CONTROLLERS

Direct Memory Access (DMA) of RAM by external devices, such as a disk drive, is provided by a pair of Intel 8237A DMA controllers operating at 3 MHz or 4 MHz. DMA minimizes the time that the CPU must wait for these other I/O devices requiring service. For example, when the CPU wants to read from a diskette, it programs the DMA controller with the number of bytes to be transferred and a memory address at which to start the transfer. The CPU can then return to another task in the system while the DMA controller waits for the data from the disk controller to arrive.

On Sheet 10 of the schematic, two Intel 8237A 8-bit DMA controllers are used in the TeleVideo AT. Operational details of the DMA controllers are given in the Microsystem Components Handbook, published by the Intel Corporation.

Byte data transfer is accomplished by DMA Controller 1 (U27). Word data transfer is accomplished by DMA Controller 2 (U28) working with DMA Controller 1. Controller 2 is not used during byte operations. To operate, the DMA controllers must have control of the address, data and control busses in the system. When an I/O device requests DMA service by asserting its DRQx line, the DMA controller tries to get control of the busses by asserting DMA2 HRQ. This signal is sent to the memory refresh generation logic, which grants the request if a memory refresh cycle is not in progress. If a refresh cycle is in progress, the DMA controller will wait. If the refresh cycle is not active, the DMA will take control of the busses.

The DMA controller then asserts a DMA acknowledge (DACK) to the requesting I/O device to indicate that it has been granted a DMA cycle. When the DMA operation is finished, the DMA controller removes its DMA 2 HRQ and the CPU or memory refresh controller resumes control of the busses.

The DMA controllers can address up to 64 Kbytes of memory using 16 address lines. The data lines, shown on the device as D0 - D7, are multiplexed to provide the upper eight bits of the address. Address latches U46 and U47 hold the upper eight bits of the memory address while address lines A0 - A7 hold the lower eight bits. The address strobe signals (ADSTB) from controller 1 and controller 2 are used to gate the address latches.

In word operations, data transfers always take place on even-byte boundaries, that is, the least-significant bit of the address is always zero. Therefore, controller 2 outputs its address on the A1 - A16 address lines, while controller 1 uses the A0 - A15 address lines. The D0 - D7 lines are then used to transfer the data to or from the requesting I/O device.

Page Registers

DMA controller 1 can transfer 64 Kbyte blocks of data to a total of 256 blocks (or pages). Using DMA Controller 2, 128 Kbyte blocks (64K words) can be transferred to a total of 128 byte blocks of memory during each DMA operation.

Using the first DMA Controller, the page register at U29 specifies one of 256 pages of memory in the system where the transfer will occur. Using the second DMA, the page register specifies one of 128 pages of memory. The CPU loads U29 with the page number on the XD0 - XD7 data lines. When the first DMA has control of the address bus, the page register supplies the page address on the A16 - A23 address lines. When using the second DMA controller, the page address is supplied on the A17 - A23 address lines.

DMA Wait-Circuit

Some slower I/O devices require extra time between DMA cycles. A flip-flop at U63 provides a wait-circuit between DMA cycles. The ready (RDY) input to the DMA will go high when the I/O device is ready for the next cycle.

ADDRESS AND DATA BUSSES

A 24-bit address bus and an 8/16-bit data bus allow the CPU to communicate with memory, peripheral devices, and its I/O channels, which support up to eight circuit boards plugged into connectors on the motherboard. Since a 24-bit address bus is used, up to 16 megabytes of RAM and ROM can be addressed. Furthermore, the CPU can access bytes (eight bits) or words (sixteen bits) depending on the mode selected by software.

To maintain compatibility with the earlier 8088-based PC-type machines, much of the peripheral hardware, such as interrupt controllers, DMA controllers, and serial and parallel printer ports, are eight-bit devices. That is, data transfers between these I/O devices and the CPU occur only in bytes, not full sixteen-bit words. Also, memory locations can be addressed in either bytes or words. An extensive address and data buffering scheme ensures this compatibility with the PC-type machines.

Address and Data Buffering

The address bussing scheme consists of address latches and buffers that allow the CPU and DMA controllers to provide addresses for memory and I/O devices on the motherboard and I/O channels. On Sheet 3, address lines A1 - A19 are latched by U41, U32, and U34 as the System Address lines for use by system memory and I/O devices. U41 also latches several control signals relevant to operation of certain system components.

Unlatched, buffered address lines A17 - A23 are also made available to the I/O channels for hardware requiring them as LA17 - LA23. After latching, the SA1 - SA15 data lines are sent to two bidirectional buffers U31 and U33 on Sheet 4, which provide the XA1 - XA16 address lines to the I/O devices on the motherboard. When DMA is active, the direction of data flow reverses. Also concerning DMA operations, U40 buffers address lines A17 - A19 and four control signals.

Data buffers U51 and U36 buffer data between the CPU, memory and I/O devices. U51 handles data bits D0 - D7 and is a combination latch and buffer. The CPU is capable of either byte or word operations using 8-bit I/O devices. When the CPU wants to read a word (16 bits) from an 8-bit device, the control logic on the motherboard will generate two read cycles.

The first cycle reads the 8-bit device and latches the lower byte of data on U51. During the second cycle, the CPU reads eight more bits (the high byte) from the device and buffers them through U36. At that time, the CPU reads both bytes on its D0 - D15 data line. The same process works in reverse when the CPU writes 16 bits of data to an 8-bit I/O device. For 16-bit I/O devices or memory, the lower byte of data is not latched; data is simply transferred between D0 - D15 and SD0 - SD15.

The SD0 - SD15 data lines are sent to two pairs of bidirectional buffers on Sheet 4, U53 and U38, and U52 and U37. For memory addresses, buffer pair U53 and U52 buffers SD0 - SD15 to or from the memory as MD0 - MD15 depending on the state of their DIR inputs. For I/O devices in the system, buffer pair U38 and U37 buffers the SD0 - SD15.

For example, if the CPU is reading 16 bits of data from an I/O device, the lower byte appears at the inputs of U38 on the XD0 - XD7 data lines. The buffer is gated to place the byte on the SD0 - SD7 lines to latch/buffer U51. The high byte then appears on the XD0 - XD7 data lines and is sent through U38 to U37. U37 sends the data to the SD8 SD8 - SD15 data lines to U36.

When the CPU writes data to an I/O device, the process is reversed. Control of buffer U38's DIR and G- inputs is performed by gates in U39 and U120. For external 16-bit I/O devices connected to the eight I/O channels, the SD8 - SD15 lines go directly to the 36-pin I/O channel connectors.

8259 INTERRUPT CONTROLLERS

On Sheet 11 of the schematic, the two Intel 8259A interrupt controllers at U20 and U21 are cascaded to allow up to 15 I/O devices to request service (interrupt) from the CPU. The 8259As manage multiple interrupt sources for the CPU. They are programmed by the CPU using the XD0 through XD7 data lines for data, the XA0 address line to select internal registers, and the XIOR- and XIOW- read and write strobes to control read and write operations.

When an I/O device interrupts, the request is processed within the 8259A as previously programmed by the CPU. Interrupt priorities are then resolved and any requests for service can be ignored. An interrupt controller asserts INTR to inform the CPU that an I/O device has requested service.

The CPU then interrogates the 8259As to determine which device interrupted. Interrupt requests from such devices as Channel 0 of counter/timer U22 appear at an IR0 input of U20.

Channel 0, a general-purpose interrupt, is assigned the highest priority interrupt line IRQ0. Other interrupts from the I/O channels, keyboard, etc. are assigned lower priority (higher numbered) inputs into the interrupt controllers. Both controllers are tied together by the CAS0 - CAS2 cascade lines. U21 interrupts U20 by sending its INT output to the IR2 input of U20. U20, in turn, asserts INT to the CPU.

The sources of interrupts are from the keyboard, real-time clock, numeric coprocessor, floppy disk controller, hard disk controller, and devices on the I/O bus. A non-maskable interrupt directly to the CPU is provided in the event that a parity error occurs in RAM or an error occurs on the I/O bus.

8254 PROGRAMMABLE TIMER

On Sheet 11, the 8254 counter/timer has three programmable timer channels. The 8259As are programmed by the CPU using the XD0 - XD7 data lines for data, the XA0 and XA1 address lines to select internal registers, and the XIOR- and XIOW- read and write strobes to control read and write operations.

The 1.19-MHz clock for the counter channels is generated by U45 and U59 on Sheet 17. Channel 0 generates a general-purpose interrupt to 8259A U20. Every 15 microseconds, Channel 1 issues the REFRESH TIME OUT signal to trigger a memory refresh cycle. Channel 2 provides a square wave to modulate a speaker.

This square-wave output is ANDed with speaker data (SPK DATA from latch U14) and sent through an amplifier at Q4 to the J22 speaker connector. The output is also sent to buffer U15 to be returned to the system data bus.

KEYBOARD CONTROLLER

An Intel 8042 at U10 on Sheet 12 is a single-chip microcomputer that provides the interface between the system data bus and the keyboard. The 8042 contains proprietary firmware to scan the keyboard for depressed keys and to convert the keycodes into standard eight-bit ASCII character codes used by the system's software.

KBD DATA is a bidirectional signal. The signal can be sent either by the 8042 to the keyboard or by the keyboard to the 8042. The KBD CLK signal is sent by the keyboard to the 8042. When a key is depressed, corresponding clock and data are sent back to the TEST 0 and TEST 1 inputs.

The microcomputer then interrupts the CPU via the IRQ1 line to interrupt controller U20. The CPU reads the ASCII code on the XD0 - XD7 data lines using the XIOR- read strobe. During system power up U10 is reset by the RESET line going high from U87 (Sheet 2). When the CPU is in its Protected-

Address mode, U10 can also recognize a software reset to the CPU (SOFT RESET 286) that will cause it to go into the Real- Address mode.

Also on Sheet 12 and connected to the XD0 - XD7 data lines is a general-purpose latch composed of latch U14 and buffer U15. The latch and buffer are controlled by IN/OUT BUFF- from I/O decoder U78 (Sheet 11) and by the XIOR- and XIOW- I/O read and write strobes.

The output of U14 includes signals to enable a parity check (EN PAR CK), supply a speaker gate to Channel 2 of the 8254A (SPK GATE) and data (SPK DATA), and a I/O channel check line (CH IO CK) to the relevant circuits indicated. Buffer U15 reads several similar signals.

RS-232C INTERFACE CHANNEL

The EIA-standard RS-232C serial channel is controlled by a National 16450 Asynchronous Communications Element. The 16450 supports asynchronous serial communication at standard baud rate increments from 50 to 9,600 baud.

The TeleVideo AT uses a nine-pin, D-subminiature type connector for interconnection with peripheral devices. Two RS-232C channels can be accommodated in the AT. The assignment of the serial port is jumper-selectable to Port 1 or Port 2. See the "External Interfaces" chapter for pinouts and electrical characteristics of this and other external connectors.

RS-232C Serial Port

On Sheet 14, National 16450 Communications Controller U8, receivers U1 and U3, and driver U2 implement a standard RS-232C communications channel. The National NS16450 Asynchronous Communication Element performs parallel-to-serial conversion of outgoing data from the XD0 - XD7 data lines to the TXD line, and serial-to-parallel conversion of incoming data from the RXD line to the data bus.

The communications controller contains its own baud rate generator clocked by a 1.843-MHz crystal at Y1. U2 is a standard 75188 RS-232C line driver carrying signals Transmit Data (TXD), Request to Send (RTS), and Data Terminal Ready (DTR) to the peripheral device from U8.

Similarly, U1 and U3 are standard 75189 line receivers carrying signals Ring Indicator (RI), Receive Data (RXD), Clear to Send (CTS), Data Set Ready (DSR), and Carrier Detect (CDC) from the peripheral device to U8.

PARALLEL PRINTER PORT

The parallel printer port is intended primarily for support of a Centronix-compatible parallel printer, but can be used with other output-only devices if desired. A female, 25-pin D-subminiature type connector is used. All signals are at standard TTL levels. The assignment of the parallel port is jumper-selectable to Port 1 or Port 2. Refer to the "External Interfaces" chapter for pinouts and electrical characteristics.

At the bottom of Sheet 14, the Centronix-compatible parallel printer port is composed of two latches at U7 and U12, and two buffers at U11 and U13. Data sent to the printer from the XD0 - XD7 data lines from the CPU are latched by U7 by PAR DATA WR- (Sheet 12) and sent out to connector J17 as DATA0 - DATA7. Buffer U13 is wired across the inputs and outputs of U7 for diagnostic loopback purposes and to test whether port 1 or port 2 is selected on the motherboard. U13 is enabled by PAR DATA RD-.

Control signals to the printer are also sent on the system data bus to latch U12. Signals sent to the printer are the data strobe (STROBE), auto line-feed (AUTO FDXT), an initialization line (INIT-), and a printer selection line (SLCT IN-).

These four signals are also sent to buffer U11 and tri-state buffer U17. The incoming status signals include a line to indicate a printer error (ERROR-) printer selection (SLCT), paper empty (PE), a printer acknowledge line (ACK-), and a printer busy signal (BUSY).

I/O CHANNELS

A total of eight I/O channels on the motherboard are used by plug-in boards, such as memory expansion, modems and peripheral controllers, and so forth. Six of the channels provide the plug-in board with two connectors. One 62-pin connector is identical to that used in earlier 8-bit 8088-based PC-type systems, and a smaller 36-pin connector is used to expand bus data transfer capability to a full 16 bits.

Each I/O channel is electrically parallel with the other seven channels, as shown on Sheets 15 - 19 of the schematic The 62-pin connector (J1 - J8) is functionally identical to that on PC-type systems providing control, address and data lines useful for 8-bit I/O hardware.

A second, 36-pin, connector (J10 - J14 and J16) is compatible with PC AT-type systems providing the control, address and data lines necessary for 16-bit I/O hardware. See the External Interfaces chapter of this manual for pinouts and electrical characteristics.

3 HARDWARE FUNCTIONS - DISKETTE (FLOPPY)/ FIXED (HARD) DISK CONTROLLER

Introduction

The Diskette/Fixed Disk Controller, an adaptor board, connects to the motherboard using one of the 16-bit expansion slots. This single board provides all signals necessary to operate up to two fixed drives and two 5 1/4-inch diskette drives. The controller allows concurrent data operations on one diskette and one fixed disk drive.

This chapter is divided into two sections. The first section is devoted to diskette controller functions. The second section covers fixed disk (Winchester) controller functions.

DISKETTE CONTROLLER

The diskette control circuitry (see Figure 3-1) is based around the 8272A (U28) or NEC D765AC diskette controller chip. The chip provides parallel-to-serial and serial-to-parallel data conversion and drive selecting and head tracking functions. The 8272A FDC is programmed to operate in the burst transfer mode. The programming is done by the EPROM during system initialization.

The support 9229B (U48) performs all write precompensation functions. The 9229B also separates data and clock pulses that compose the MFM data being read off the diskette to ensure accurate data exchanges with the 8272A.

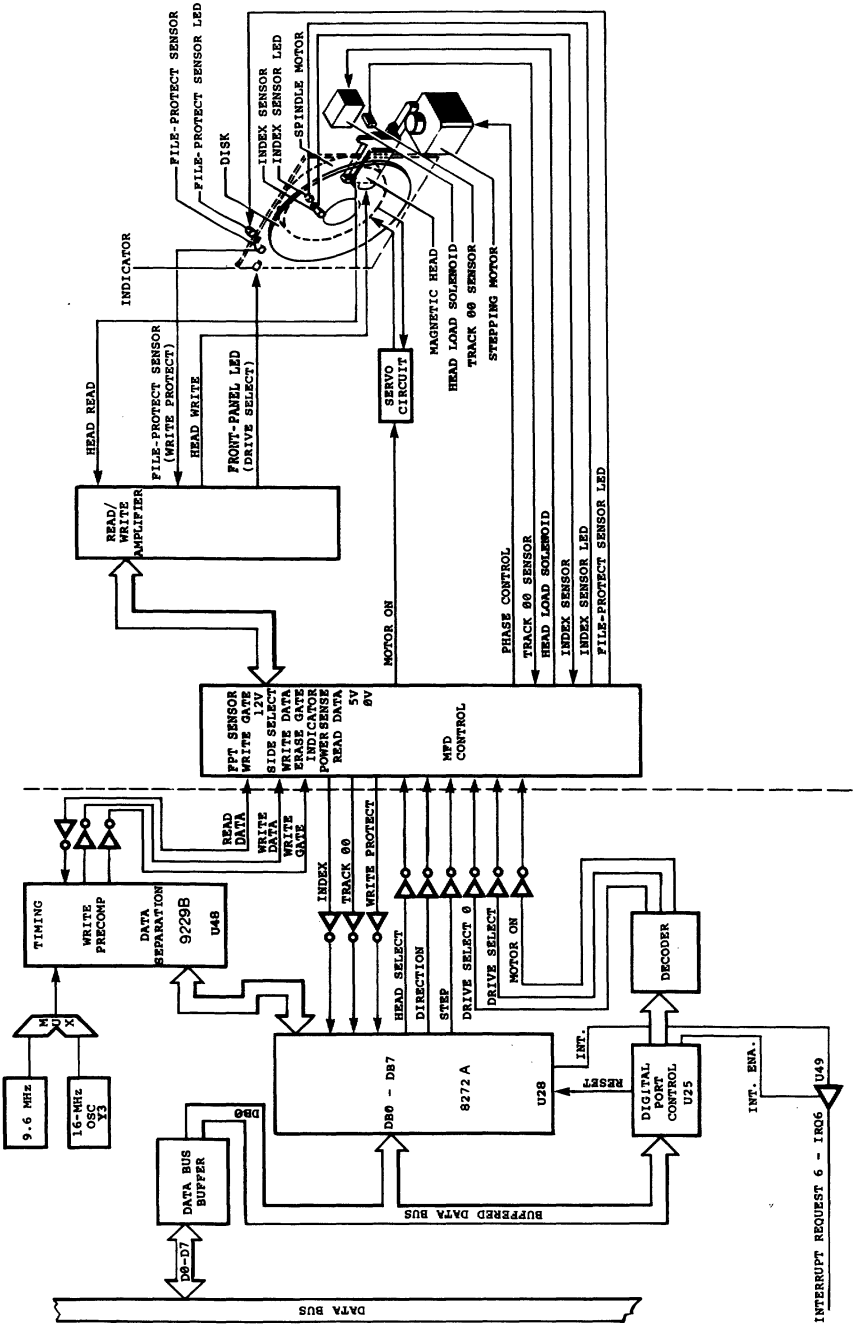
The bidirectional buffer (U81) and the diskette drive latch (U17) are important support IC's. They control disk drive selection and starting the diskette motor. These are taken as control words from the system data bus.

The basic functions of the diskette controller circuitry are:

1. Writing data to the diskette
2. Reading data from the diskette
3. Determining where to write on the diskette
4. Turning the drive off and on and selecting drive A or B

Functions 1, 2, and 3 are all controlled by the 8272A diskette controller.

Figure 3-1
Diskette Controller



The major components of the diskette controller are:

U28	Intel 8272A Diskette Controller Device
U17	Diskette Drive Control Latch
U48	FDC9229B Data Separator

The diskette controller components and their descriptions are listed in Table 3-1.

Table 3-1
Diskette Controller Components

Device or Line	Source/Description
Diskette Controller	Provides parallel-to-serial conversion of data from the system to the diskette, and serial-to-parallel conversion from the diskette to the system. Provides all drive control functions, such as head step, head direction, write protect, and track 0 detection. The controller can be programmed to handle seek track, read sector, write sector, read address, read track, and write track operations. The DB0-DB7 Data Transceiver carries data and programming signals between the diskette controller and CPU.
-COMP READ DATA	FDD. Carries composite read data from the diskette drives.
-COMP WR DATA	FDC. Carries composite write data to diskette drives.
Diskette Drive Control	Controls the selection of the diskette drive, turning the motor on/off, enabling/disabling interrupt, enabling/disabling DMA operation, and resetting the diskette controller.
Data Separator	Performs write precompensation and data separation.

FIXED DISK (WINCHESTER) CONTROLLER INTERFACE

The major components of the Winchester controller interface and their descriptions are listed in Table 3-2.

A block diagram of the Winchester controller interface is shown in Figure 3-2.

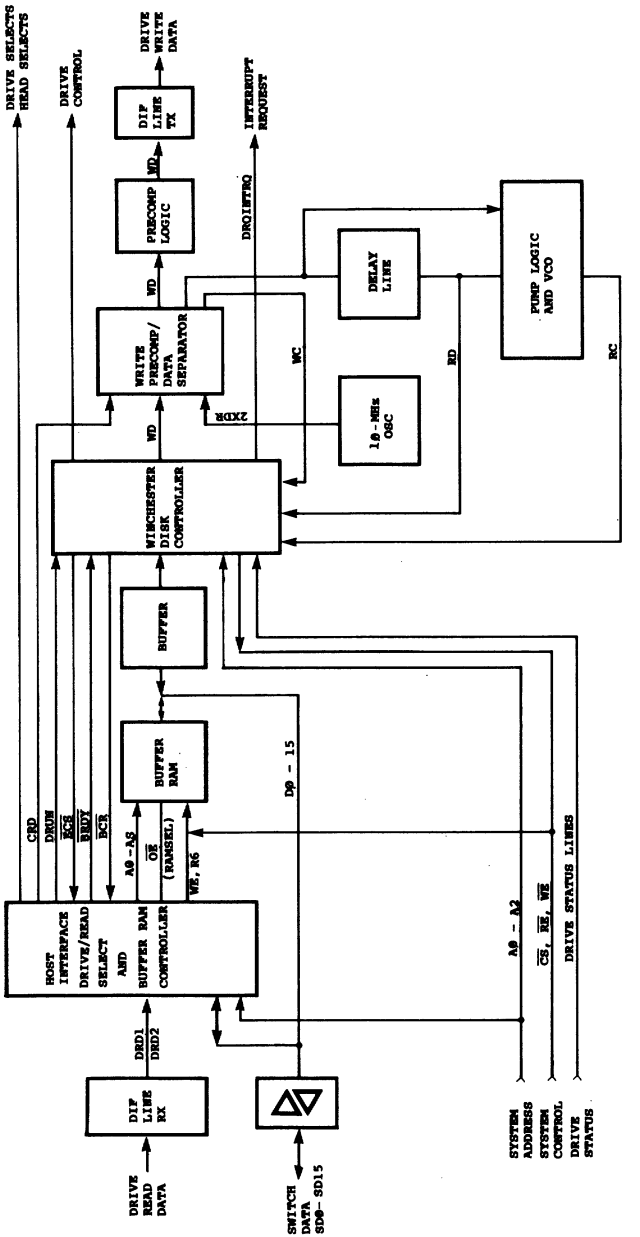
Table 3-2
Fixed Disk (Winchester) Controller Interface Components

Device or Line	Source/Description
Data/Address Transceiver and Control Signals Buffer	The transceiver and buffer pass data, and control signals to an external Winchester disk controller board.
WD0-WD7	Data/Address Transceiver. Buffered data lines to the Winchester controller board.
WA0-WA2	Control signals buffer. Buffered address lines to the Winchester controller board.
-WCS,-WWE, -WRE,WMR, -WDC,RD	Control signals buffer. Buffered control signals to the Winchester controller board.

FIXED DISK (WINCHESTER) CONTROLLER

The Winchester disk controller provides all control and data handling functions needed to interface the system with a 5 1/4-inch Winchester disk drive. Figure 3-2 shows a block diagram of the Winchester disk controller board.

Figure 3-2
Fixed Disk (Winchester) Controller Board Block Diagram



The major components of the fixed disk controller are:

U8	WD1010-05 Winchester Disk Controller
U26	WD1100-10 Write Precompensation and Data Separator
U60,61	Buffer RAM (two provided)
U62	Error Amplifier
U2,19	Pump Logic
U39	Voltage Controlled Oscillator (VCO)
U5	Differential Line Receiver
U4	Differential Line Transmitter

System/Controller Interface

The system programs the Winchester disk controller by accessing the task file registers of the WD1010-05 controller device.

The system/controller interface lines are shown in Figure 3-2.

Table 3-3 lists the system/controller interface components and their descriptions.

Table 3-3
System/Controller Interface Components

Active Line	Source/Description
A0 to A2	System. Task file register address.
-WE or -RE	System. -WE to activate task file write, or -RE to activate task file read.
SD0 to SD15	System. Data or command.

Operations With Dual-Port Buffer RAM

The Winchester disk controller uses dual 1 kilobyte by 8-bit buffer RAM to interact with the system during disk read and write operations. When writing to the disk, the system writes the data to the buffer RAM by sector. After a sector of data is loaded into the buffer RAM, the WD1010-05 writes the data from the buffer RAM to the disk. Table 3-4 lists the write from buffer RAM signals.

Table 3-4
Write From Buffer RAM

Active Line	Source/Description
SD0 to SD15	System. Sets up the Task File Register and the Write Sector command in the WD1010-05 task file and writes data to buffer RAM.
-BCR	WD1010-05. Strobed to zero counter.
BDRQ	WD1010-05. Active to indicate that the buffer RAM is empty.
-BCS	WD1010-05. Set high to enable the host control of buffer RAM. Transceiver direction is ready for write.
-WE	System. Loads the buffer and increments the counter with - HDCS.
BRDY	Active to indicate the buffer is full.
-BCS	WD1010-05. Active to disconnect the host control of the buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent the system access during the next operation.
-WDRE	WD1010-05. Reads the buffer RAM to transfer data to disk (See Writing Disk Data).

Table 3-4 (continued)
Write From Buffer RAM

Active Line	Source/Description
-BCS	WD1010-05. Set high to allow the next operation by the system. Board busy tristate buffer is inactive.
INTRQ	WD1010-05. Signals the end of the command to the system.

Reads of dual-port buffer RAM occur after a sector of data has been loaded to the RAM from the disk. For a read from buffer RAM, see Table 3-5.

Table 3-5
Read From Dual-Port Buffer RAM

Active Line	Source/Description
SD0 to SD15	System. Sets up the Task File Registers and places the Read Sector command in the WD1010-05 task file.
-BCS	WD1010-05. Active to disconnect the host control of buffer RAM.
-BCR	WD1010-05. Strobed to zero counter.
-WDWE	WD1010-05. Loads the buffer from the disk (See Reading Disk Data), and increments the counter with -CS.
BRDY	Active to indicate that the buffer is full.
-BCR	WD1010-05. Strobed to zero counter.

Table 3-5 (continued)
Read From Dual-Port Buffer RAM

Active Line	Source/Description
-BCS	WD1010-05. Set high to enable the system control of buffer RAM.
BDRQ	WD1010-05. Active to initiate transfer to the system.
-RE	System. Reads buffer RAM and increments the counter with -CS.
BRDY	Active to indicate that the buffer is empty.
INTRQ	WD1010-05. Set high to stop the operation.

Writing Disk Data

The write sector command requires that the Winchester controller locate the place on the disk that is to receive the data. The command also controls the write operation to buffer RAM. It must then read the data from the buffer RAM, condition the data into MFM format, and write the data to disk.

Under MFM, clock bits are recorded only when two successive data bits are missing in the serial data stream. Using MFM reduces the total number of bits required to record a given amount of information on the disk. Because this effectively doubles the amount of disk capacity, it is termed "double density."

Encoding MFM follows three rules:

1. If the current data cell contains a data bit, then no clock is generated.

2. If the previous data cell contained a data bit, then no clock is generated,

3. If the previous data cell and the present data cell are vacant, then a clock is generated in the current clock cell.

Data and clock cells are defined by the state of the write clock (WC) line. If WC is low, it is a data cell; if WC is high, it is a clock cell. Both clock and data cells are 100 nanoseconds long in ST506-compatible drives.

The active lines for writing disk data are shown in Figure 3-3 and listed with a description in Table 3-6.

Figure 3-3
Writing Disk Data

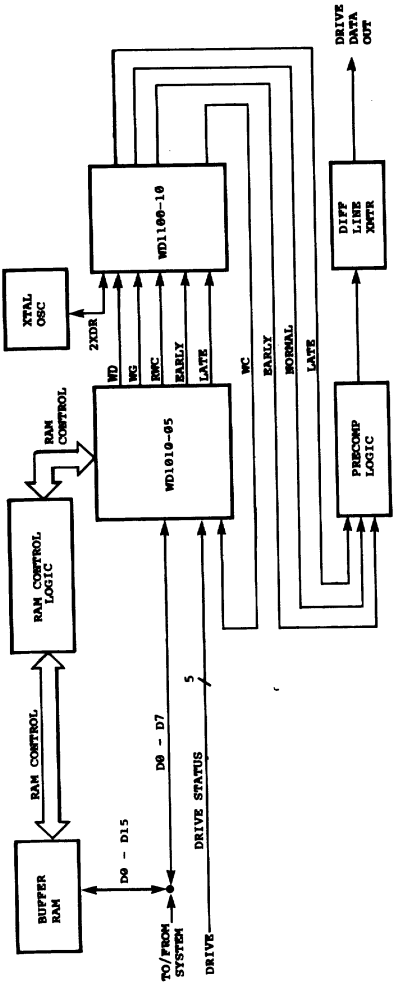


Table 3-6
Writing from Buffer RAM

Active Line	Source/Description
D0 to D7	System. Contains the write sector command. When the WD1010-05 receives this command, it checks its cylinder registers against the current cylinder position.
-BCR	WD1010-05. Strobed to begin write to buffer RAM by the system.
BRDY	Buffer RAM is full.
-BCS	WD1010-05. Active to disconnect the host control of the buffer RAM.
-STEP,-DIRET	WD1010-05. Moves head to locate cylinder.
SEEK COMPLETE	Drive. Informs the WD1010-05 that the head settling time for the current step is expired. If the current step is not the required cylinder position, the head is moved again. After seek to desired cylinder, the controller checks for the desired sector address by reading data from the drive.
WG	WD1010-05. Write gate signal to WD1100-10.
WC	WD1100-10. Carries the 5-MHz write clock, derived from the 2XDR clock signal, to WD1010-05.
-RWC	WD1010-05. Reduced write current signal; turns on precompensation circuits for write to disk.
-WD	WD1010-05. Write data as read from buffer RAM and serialized by WD1010-05.

Table 3-6 (continued)
Writing from Buffer RAM

Active Line	Source/Description
-EARLY, -LATE	WD1010-05. Precompensation signals to WD1100-10. Precompensation is used to counteract the effects of dynamic bit shift when writing the inside recorded tracks of the disk. Dynamic bit shift results when a bit on the disk influences the position of an adjacent bit. The leading edges of the bits are moved closer together, or further apart, depending upon the polarity of each bit. Because positions of bits shift as they are written to the disk, data is harder to recover without error. Write precompensation is applied to counteract the effects of dynamic bit shift. Precompensation predicts the direction a bit will be shifted. It then writes the bit out of position in the opposite direction of the shift. The prediction is done in the WD1010-05 by checking the next two data bits, the last bit written, and the present bit.
EARLY, NORMAL, LATE-	WD1100-10. Precompensation signals to precompensation logic. Data is shifted +/-12 nanoseconds from the normal position through a delay line.
Data	Differential Line Driver. Carries MFM formatted, precompensated, RS-422 write data to the drive head.

Table 3-6 (continued)
Writing from Buffer RAM

Active Line	Source/Description
-BCS	Set high to allow the next operation by the system.

Reading Disk Data

For disk reads, the Winchester disk controller board locates the sector to be read, identifies the start of the data field, reads the data in from the disk, separates the data and clock signals, writes the data to buffer RAM, and controls the system read of the data out of buffer RAM.

The active lines for reading disk data are shown in Figure 3-4 and listed with a description in Table 3-7.

Figure 3-4
Reading Disk Data

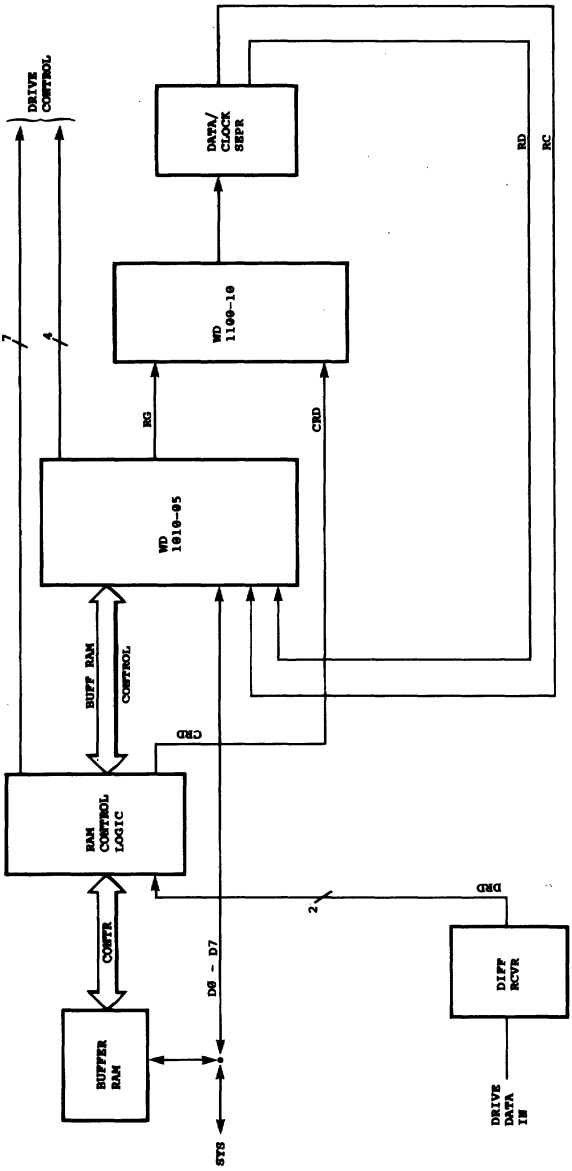


Table 3-7
Disk Data

Active Line	Source/Description
D0 to D7	System. Contains read sector command. When the WD1010-05 receives this command, it checks its cylinder registers against the current cylinder position.
-BCS	WD1010-05. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during the next operation.
-STEP,-DIRET	WD1010-05. Moves head to locate cylinder.
-SEEK COMPLETE	Drive. Informs WD1010-05 that head settling time for the current step is expired. If the current step is not the required cylinder position, the head is moved again. After seek to desired cylinder, controller checks for desired sector address by reading data from the drive.

4 HARDWARE FUNCTIONS - HIGH RESOLUTION ALPHA/GRAPHICS BOARD

Introduction

The TeleVideo AT High-Resolution Alpha/Graphics Board (HGB) can replace the IBM Monochrome Display and the IBM Color/Graphics Monitor Adapter while adding improvements not provided by either board.

As shown in Figure 4-1, TeleVideo AT High-Resolution Alpha/Graphics Board Block Diagram, the HGB contains the following major functional blocks:

* The I/O Channel Interface buffers data and control signals to and from the I/O channel, and provides system CPU's I/O address decoding to control the logic used on the HGB.

* The Motorola 68B45P CRT Controller (CRTC) provides control of the raster scan video display (CRT) as well as video RAM refresh timing and cursor control. The CRTC is initially programmed by the system CPU for display parameters, such as horizontal and vertical image size, number of retrace periods in the display, and so forth.

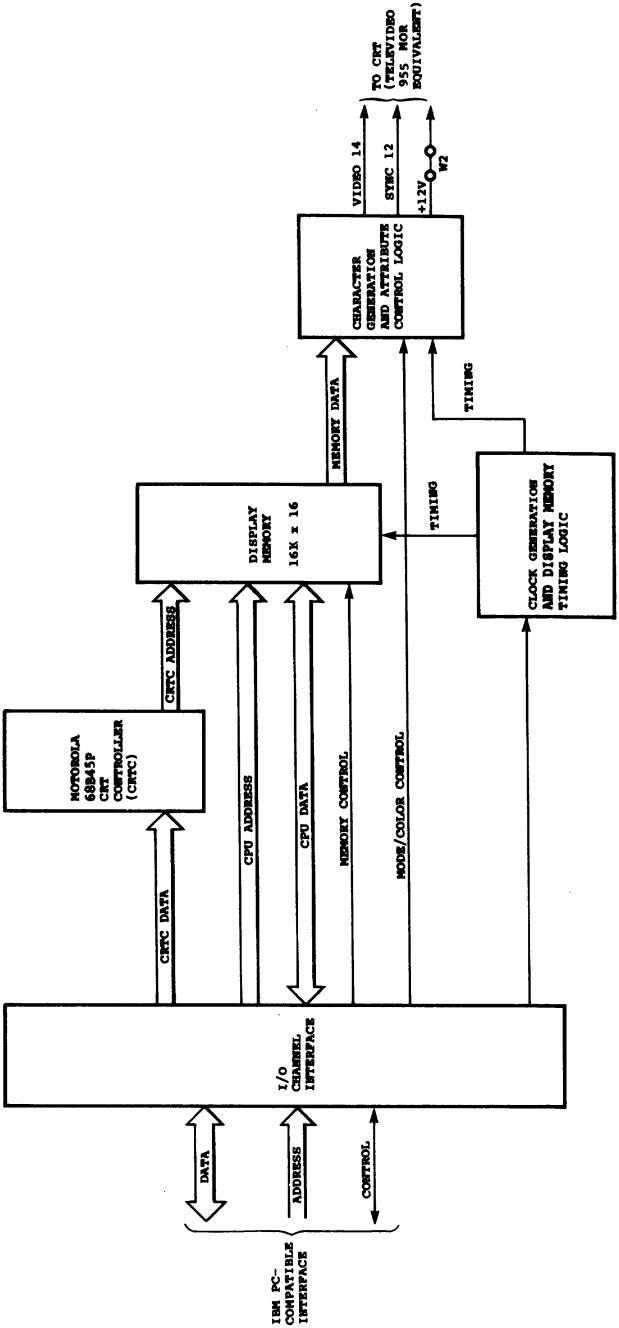
* The Clock Generation and Display Memory Timing Logic generates various clocks and sychronization signals for the CRTC, display memory and display logic.

* A Display Memory contains 32 Kbytes of 16-bit alphanumeric or graphic words, representing the video map. The display memory is updated by the system CPU, read, and refreshed by the CRTC for display on the CRT.

* The Character Generation and Attribute Control Logic converts data from the display RAM to characters or video attributes and sends them to the video display logic when the HGB is in an alpha mode. Otherwise, data is shifted directly to the video display when the HGB is in a graphics-only mode.

The HGB supports five display formats in two modes. The alpha mode supports, 40 characters by 25 lines or 80 characters by 25 lines. The graphics mode supports IBM-compatible formats of 320 by 200 pixels and 640 by 200 pixels. In addition, TeleVideo graphics software supports a high-resolution 640 by 400 pixel format.

Figure 4-1
High Resolution Alpha/Graphics Board



In the following discussions, note that sheet numbers refer to the TeleVideo AT High-Resolution Alpha/Graphics Board schematic.

I/O CHANNEL INTERFACE

See Figure 4-2, I/O Channel Interface, CRTC, and Clock Generation Logic Block Diagram and graphics board schematic diagrams during the following discussions.

On the left side of schematic Sheet 1, I/O address decoding logic enables operation of the HGB at hexadecimal addresses 3B0 - 3BB and 3D0 - 3DF, which correspond to those used by the IBM Monochrome Display and the IBM Color/Graphics Monitor Adapter, respectively. Since the HGB has no parallel printer port, it does not respond to hexadecimal addresses 3BC - 3BF. Those addresses can be allocated to another parallel printer port, if desired.

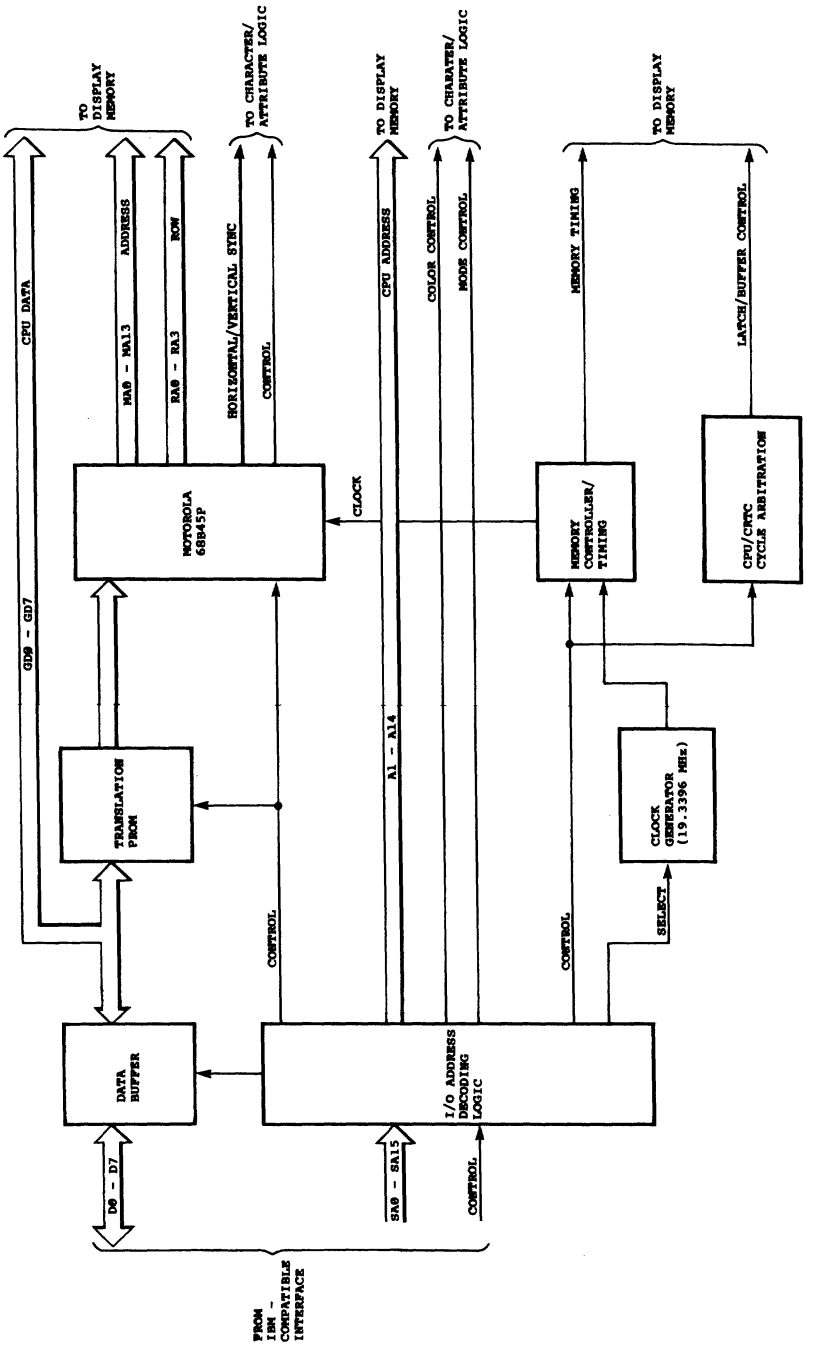
Address lines SA19 - SA16 (System Address 19 - 16) on I/O channel lines A12 - A15 select the 32 Kbyte display RAM as GMSLT-, gate display memory read/write strobes at decoders U56, and enable data buffer U65. Address lines SA9 - SA0 on A22 - A31 perform additional I/O address selection for the CRTC at U40 and at decoder U53. U53 provides enable signals for the mode control register (MODECNT-), color control register (COLCNT-), and the status bits (STS RD-) and card present (CARD-) to the logic on sheet 4.

Eight bits of data as SD0 - SD7 (System Data 0-7) on I/O channel lines A9 - A2 are sent to bidirectional data buffer U65. U65 is enabled by the I/O address decoding logic whenever a data transfer is taking place between the system CPU and the CRTC, or the system CPU and the display RAM. The direction of data transfer is determined by gates at U58 and by a combination of IOR- at B14 and SMEMR at B12 and AEN at A11.

From buffer U65, data is transferred on the GD0 - GD7 (Graphic Data 0 - 7) lines to the display memory or CRTC. Data going to the CRTC passes through PROM U28. U28 is selected along with the CRTC and contains 512 bytes of data that is used as a translation table for incoming commands. Half of the PROM is used to ensure that commands from software originally written for IBM hardware will translate to the specific commands required by the CRTC; the other half of the PROM allows software written specifically for the HGB to directly control the CRTC.

The commands tell the CRTC, for example, how many horizontal lines are to be traced across the display, the number of retrace lines, and the cursor position. When the high-order address line at pin 19 of U28 is high, the incoming IBM-compatible parameter on GD0 - GD7 addresses a location that translates to the necessary parameter required for the CRTC.

Figure 4-2
I/O Channel Interface, CRTC, and Clock Generation Logic Block Diagram



When pin 19 is low, the incoming parameter addresses a location that contains the same parameter. The commands are sent from the outputs of the PROM to the DB0 - DB7 data inputs of the CRTC. Flip-flop U52, along with gates at U17, U55, U32, and U41, control the selection of the high-order address line to U28.

At the bottom of schematic Sheet 4, the color control register and mode control register are fed by the GD0 - GD7 data lines. U43 is clocked by the Color Control (COLCNT) bit from decoder U53 on Sheet 1 and provides the IBM-standard six bits of color control information (COLOR SLT, BGI, OVRSI, OVRSR OVRSG, and OVRSB) plus 400GL to control display memory addressing when the 640- by 400-line graphics mode is selected.

Latch U27 is clocked by the Mode Control (MODE CNT) bit from decoder U53. The six mode control bits are blink enable (BLINK EN), horizontal mode selection (640/320C-), video enable (VID EN), monochrome enable (B&W), graphics mode enable (GRAPH), and high-resolution enable (HIGH RES). Both registers are cleared by the master reset line (RESET-) upon system power up or manual reset.

In place of the CRTC status register, which is not used, three bits of status information for the system CPU are also provided. CARD- attached to GD7 indicates that the HGB is in the system. Two other bits, which are enabled by status read (STS RD) from decoder U53 are a video synchronization bit (VSYNC) at GD3 and a system display cycle bit (SCDE-) at GD0.

When the system is using IBM software, it is assumed that one of the IBM display adapters is used. These bits, read periodically by the software, determine when the system CPU can access display memory. Because of the cycle arbitration scheme used (Sheet 2), the HGB allows a CPU cycle at any time. The SYNC and SCDE bits are provided to satisfy the software requirement.

MOTOROLA 68B45P CRT CONTROLLER (CRTC)

The Motorola 68B45P CRTC operates at 2.42 MHz from the character clock (CCLK) generated on Sheet 2 of the schematic. The CRTC at U40 has 12 I/O registers, which when programmed by the system software, define the parameters of a raster scan video display. The CRTC refreshes the video display by reading data from display memory locations. The display memory contains a binary "image" of the display.

In the alpha mode, the CRTC reads the addresses for an entire line of characters using its MA0 - MA13. Its row counter, characterized by the RA0 - RA3 lines, increments and the addresses for the line are read again.

Since the character size is set at eight by eight dots, each row of characters is read eight times. In graphics mode, the row counter outputs are used as additional address lines. A total of 32 Kbytes of display memory is available when using the high-resolution graphics display.

The CRTC and the system CPU share access to the display memory. During a display cycle, when the DISPEN output of U40 is high, the CRTC reads a part of display memory. The data read is sent to logic that converts it to characters, attributes, and/or colors on the display. When DISPEN is low, the system CPU has the opportunity to address display memory.

The CRTC addresses display memory, and also generates two signals for proper vertical- and horizontal-trace synchronization. The horizontal-synchronization signal operates at a rate of about 16 kHz and the vertical-synchronization signal operates at 60 Hz.

Further information about the operation and programming of the MC68B45 CRTC is provided in the Motorola Microprocessor Data Manual, published by Motorola, Austin, Texas.

CLOCK GENERATION AND DISPLAY MEMORY TIMING LOGIC

The clock generation and timing circuits on schematic Sheet 2 provide the basic dot and character clocks for video processing throughout the HGB. The timing logic generates a split memory cycle to read or write two 16-bit words (4 bytes) from or to the display memory. Either the system CPU, through the I/O channel interface, or the CRTC addresses the display memory on alternate split cycles. The system CPU can read data from, or write data to, the display memory, while the CRTC can only read data for further processing.

The buffered output of crystal oscillator U26 provides the 19.3396-MHz master clock (MCLK) to the video output logic. The output is also sent to flip-flop U4 and AND/OR gate U5 to select the clock output for the high- or low-resolution modes. When HIGH RES is high from the mode control register on Sheet 4, the pin 8 output of U5 is 19.3396 MHz.

When HIGH RES is low, flip-flop U4 divides the 19.3396-MHz input by two to generate 9.6698 MHz at the output of U5. In the high-resolution mode, (i.e., the 80 characters by 25 line alpha mode), the logic requires a fast clock because it must access from display memory not only an eight-bit character but an eight-bit hidden attribute for the character as well.

The high- or low-speed clock is sent through four flip-flops in U8 to generate various divide-by-eight timing signals for the memory controller and video logic. All of the flip-flops are cleared by RESET- from the I/O channel interface. Timing signals are picked off of the Q or Q- outputs of the flip-flops.

At the 19.3396-MHz (the high-resolution mode) clock frequency, one cycle of the dot clock (DCLK) equals 51.7 nanoseconds. With the character width of the HGB at eight dots, the character clock (CCLK) cycle is equal to 413.7 nanoseconds, the total time for access of two 16-bit words of data from the display memory. The split cycle is controlled by the outputs of U8 as LOW-/UPPER, which acts as the low-order address line (MA0) of the CRTC or system CPU.

During the cycle a row address strobe (RAS-) and two column address strobes (CAS-) are sent to the display memory's address inputs to select the row and two columns of data for each access, respectively. When the data is read from the display memory during a cycle, W1 LATCH and W2 LATCH are used to latch the data. Timing for the display memory cycle is shown in Figure 4-3.

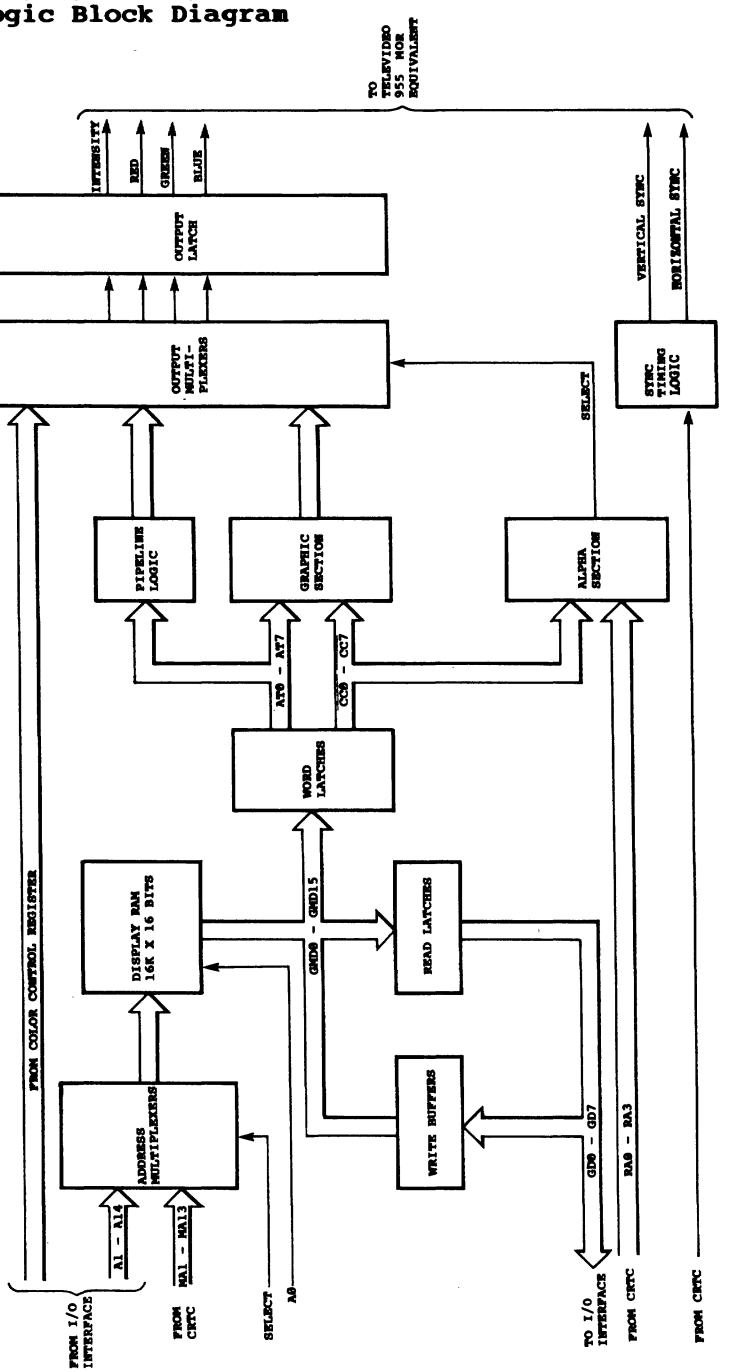
Flip-flops at U16, U47, and U57 arbitrate display memory access between the system CPU and CRTC. Once the CRTC has read data from the display memory, the system CPU can take its turn. Note that, since access to the display memory is evenly divided between the system CPU and CRTC, the number of bytes in each horizontal line on the display must be an even number. Also, the generation of the RAS- and CAS- signals occurs automatically as a result of the timing of U8.

When the system CPU addresses the display memory, it causes the graphic mode select (GMSLT) line to go low at the I/O channel interface. If the display enable signal (CDE) from the CRTC is not active, I/O channel ready (I/O CH RDY) goes high on pin A10 indicating that the system CPU can write data to the display memory. During this time, U47 generates graphics write enable (GWE-) to enable the writing of data to display memory through decoder U56 (see Sheet 1).

DUAL-PORT DISPLAY MEMORY

The display memory is composed of input address multiplexers, four 16K by 4-bit RAMs, and buffers and latches to handle data transfers to or from the RAMs. See Figure 4-3, Display Memory and Character/Attribute Logic Block Diagram during the following discussions.

Figure 4-3
Display Memory and Character/Attribute Logic Block Diagram



On the left side of schematic Sheet 3, the four-into-one multiplexers, controlled by D/C- CYCLE and MUX, select which lines are connected to the A0 - A7 address inputs of RAMs U35, U36, U45, and U46. During a display cycle (access by the CRTC; signal D/C- CYCLE is high), the MUX signal from the display memory controller switches between the low six bits of the address and the high eight bits of the address, which corresponds to the column and row addresses of the RAMs. During a CPU cycle (D/C- CYCLE is low), the MUX signal switches between the high and low address from the system CPU.

Another multiplexer, U50, provides a way to switch between the 320- by 200-line and 320- by 400-line display modes. When the HGB is in a low-resolution alpha or graphics mode, that is, 40 characters by 25 lines of alpha text or 640 by 200 pixels or 320 by 200 pixels, the high address from the CRTC comes from the MA12 and MA13 lines.

If a high-resolution graphics mode is selected (GRAPH and 400GL are high), that is, 640 by 400 pixels, the CRTC uses the row counter address lines RA0 and RA1 to address the display memory. Using 14 address lines, MA0 - MA13, the CRTC can address 16 Kbytes of RAM. The 640 by 400 mode requires, without accounting for retrace, 32,000 bytes of data. The RA lines are used to address the additional memory. For IBM-compatible software, the 640- by 200-line graphic resolution is the maximum supported. In this case, 400 lines are still shown on the display. Each horizontal scan line is displayed twice.

The RAM chips on the board are 4416 types with a 150-nanosecond access time. Each RAM stores 16K by four bits with the address lines wired in parallel with those of the other three RAMs so that a total of 32 Kbytes are available. Write enable (WE-) inputs are controlled during a CPU cycle and are outputs of decoder U56 on Sheet 1 of the graphics board schematics.

During a CPU cycle, buffers U33 and U34 transfer a byte of data from the GD0 - GD7 data lines to a pair of the RAMs. During one CPU cycle, the system CPU sends one byte of data to an even or odd byte address in memory. The byte appears at the outputs of both buffers, but only the RAM pair with the active WE- inputs allow data to be written into them. When data is read out of the RAMs by the CPU or CRTC, all 16 bits appear as GMD0 - GMD15.

On Sheet 4 of the graphics board schematics, GMD0 - GMD15 are sent to two pairs of latches operated by the display memory controller, one for the first word read in the split cycle and one for the second word. Latches U12 and U13 latch the first word using W1LATCH and enable their outputs using W1EN. Latches U1 and U2 latch the second word and then enable their outputs using W2LATCH/EN. With respect to the word latches, GMD0 - GMD7 become the character code bits (CC0 - CC7) and GMD8 - GMD15 become the attribute bits (AT0 - AT7). These designators assume that the alpha mode is selected. In graphics mode, each line each represents a pixel on the video display.

When the CPU reads data from the display memory during a CPU cycle, the data from the GMD0 - GMD15 lines are applied to the inputs of latches U23 and U24, which perform a 16- to 8-bit conversion to the GD0 - GD7 data lines. Signals RD DATA latches the data from the GMD0 - GMD15 lines, while EVEN RD- and ODD RD- enable the outputs of U23 and U24, respectively.

CHARACTER GENERATION AND ATTRIBUTE CONTROL LOGIC

On Sheet 5 of the graphics board schematics, the CC0-CC7 character code bits are sent to character generator EPROM U22 along with the RA0 - RA3 row address lines from the CRTC. U22 holds two fonts - one single dot and one double dot - that are selectable by either connecting jumper W1 to ground (single dot) or +5 volts (IBM-like double dot).

The character EPROM is enabled only when GRAPH is low, indicating a non-graphics mode. U22 sends the character data to shift register U44, which serially shifts the data to the input of gate U37 where it is ORed with UL from the underline logic on Sheet 6. U44 is enabled alpha shift/load (AS/L) and clocked every 51 nanoseconds by the dot clock, DCLK. The output of U37 is then sent to pipeline flip-flop U62 where it is delayed and again synchronized to DCLK. Finally, the pipelined character data is ORed with the output of U14 (VSYNC divided by 16) and sent to a data input of U25.

Character data is also sent to the "A" selector input of multiplexer U25. Also at the inputs of U25 are the blinking input from U15 and the GRAPH signal from the mode control register. The blinking is accomplished by dividing the 60-Hz VSYNC signal at U14 to 2 Hz and ANDing with the blink enable signal from control register U27 (Sheet 4).

One of the inputs to U25 is selected by: (1) the output of the character logic section, (2) the display cursor signal, DCUR, pipelined on Sheet 6 from the CRTC, and (3) the graphics mode selector, GRAPH. U25 is strobed by the OR of DISPEN- and 640/320C-. When strobed, the output of U25 supplies another selector input to four-into-one multiplexers U10 and U21.

When the HGB is in the graphics mode, CC0 - CC7 and AT0 - AT7 lines contain only graphic data, not character or attribute data as they do in the alpha mode. CC0 - CC7 and AT0 - AT7 supply the graphic data to shift registers U7 and U18 where it is loaded by GS/L and shifted out by DCLK. The outputs of U7 and U18 are sent to multiplexers U10 and U21 and are also gated with two bits from color control register U43, B&W and COLOR SLT, and sent to the inputs of multiplexer U19. The selected output of U19 is sent to the strobe input (STB) of multiplexers U10 and U21.

In either alpha or graphics mode, depending on the state of selector bits A (foreground color/background color) and B (graphics/alpha, U10 and U21 select data from color control register U43 (Sheet 4) or attribute data from latch U9 (Sheet 6). The outputs of U10 and U21 are for intensity, (EI), red (ER), green (EG), and blue (EB).

Therefore, each bit shifted out of U10 and U21, even if the bit is part of a character, can have colors and attributes associated with it. ER, EG, EB, and EI are latched at U11 by MCLK sent to the video display on pins P-3 - P-6, respectively, along with the horizontal and vertical synchronization pulses at P-8 and P-9, respectively.

At the bottom of Sheet 6 of the schematic, U6 and U4 generate the underline signal, UL, for the logic on Sheet 5. Decoded from the row address lines RA0 - RA3 and the state of attribute lines AT0 - AT2, U6 decodes the underline data for flip-flop U4. U4 is clocked by ULCLK from Sheet 2 to generate UL at its Q- output.

Also, gates U3, U15, and U29 intercept the AT bits associated with underline to generate white characters with a true underline in either monochrome or color modes. (Using an IBM Color/Graphics Monitor Adapter, the underline attribute shows underlined text as a dark blue color.) All of the attribute bits are latched at U9 by QCI for synchronization and are then sent to multiplexers U10 and U21 as DAT0 - DAT7.

In the middle of Sheet 6 of the schematic is synchronized logic at U11, U16, U20, and U55 to delay the horizontal- and vertical-synchronization signals, the cursor, and display enable signals so that the data has enough time to be shifted out of the character or graphic section shift registers. U54 provides a three-micro second wide, positive horizontal-synchronization, in the high- or low-speed mode, for the TeleVideo 955 monitor.

5 HARDWARE PROGRAMMING - MOTHERBOARD

Introduction

This chapter provides the system programmer with basic information necessary to write machine-level code for the TeleVideo AT. Included in this chapter are summaries of I/O addresses and devices used in the system. Table 5-1 lists all of the I/O addresses used.

For ease of reference between hardware I/O registers and the programable I/O devices, this chapter parallels, for the most part, topics listed in Chapter 2, Hardware Functions - Motherboard. Detailed descriptions of programmable I/O devices for the TeleVideo AT are given in the manufacturer's literature listed in Table 5-2.

Table 5-1.
TeleVideo AT I/O Address Summary

Address (h)	I/O Device
000 - 01F	DMA Controller 1
020 - 03F	Interrupt Controller 1
040 - 05F	Counter/Timer
060 - 06F	Keyboard Controller
070 - 07F	Real-Time Clock, NMI Mask
080 - 09F	DMA Page Register
0A0 - 0BF	Interrupt Controller 2
0C0 - 0DF	DMA Controller 2
0F0	Clear Coprocessor Busy
0F1	Reset Coprocessor
0F8 - 0FF	Coprocessor
1F0 - 1F8	Fixed Disk Controller
278 - 27F	Parallel Printer Port 2
2F8 - 2FF	Serial Port 2
378 - 37F	Parallel Printer Port 1
3D0 - 3DF	Color/Graphics Monitor Adapter
3F0 - 3F7	Diskette Drive Controller
3F8 - 3FF	Serial Port 1

Table 5-2
I/O Device Reference Literature

Device/ Manufacturer	Function	Literature Reference #
Intel 80286 (iAPX 286/10)	CPU	1
Intel 80287	Numeric Coprocessor	1
Intel 8237A	DMA Controller	1
Intel 8259A	Interrupt Controller	1
Intel 8254	Counter/Timer	1
Intel 8042	Single-Chip Microcomputer	1
National NS16540	Asynchrounous Communications Element	2
Motorola MC146818	Real-Time Clock with RAM	3

References:

1. Microsystem Components Handbook, 1984, published by the Intel Corporation, Santa Clara, CA

2. NS16450 and INS8250A Asynchronous Communications Elements, a preliminary data sheet published by National Semiconductor Corporation, Irvine, CA

3. MC146818 Real-Time Clock Plus RAM (RTC), a data sheet published by Motorola Semiconductors, Austin, TX

80286 CENTRAL PROCESSING UNIT

The Intel 80286 CPU has a 16-bit data bus and an address range of 24 bits or 16 megabytes of memory. The 80286 has an extensive instruction set with instructions to provide special operations to support the efficient implementation and execution of operating systems. Two operating modes, Real-Address Mode and Protected-Address Mode, provide compatibility with previous PC-type systems while expanding the physical and virtual memory address space of the system. Both modes provide the same basic instruction set, registers and addressing modes.

Real-Address Mode

In the real-address mode the 80286 addresses up to one megabyte of memory by generating a 20-bit segment address. The segment address is composed of the upper 16 bits of the address, termed the selector portion, and the lower 4 bits of the address, which are always zero. Therefore, each segment address begins on multiples of 16 bytes and are 64 Kbytes in size.

Protected-Address Mode

In protected-address mode the 80286 maps one gigabyte of virtual memory per task into a 16-megabyte real-address space. This mode provides four levels of memory protection to isolate the operating system and ensure the privacy of each task's programs and data. The 80286 enters the protected-address mode from the real-address mode by setting the Protection Enable PE bit of the Load Machine Status Word (LMSW) instruction. Note that once the 80286 has been placed into the protected-address mode, a reset must be applied to the 80286 to return it to the real-address mode.

SYSTEM PERFORMANCE

Either the 6-MHz or 8-MHz version of the 80286 CPU can be used in the TeleVideo AT, which gives a clock cycle time of 167 or 125 nanoseconds. The CPU speed is selectable from switch 1 of dip switch SW1 on the motherboard.

One bus cycle requires three clock cycles, one of which is a wait state. Therefore, a 16-bit microprocessor cycle time of 500 or 375 nanoseconds, is required. Operating at 6 MHz, transfer operations from 16-bit to 8-bit devices require 12 clock cycles, 10 of which are wait states, or 2000 nanoseconds; eight-bit bus operations to 8-bit devices take 6 clock cycles, including 4 wait states, or 1000 nanoseconds.

Operating at 8 MHz, transfers from 16-bit to 8-bit devices require 16 clock cycles, 14 of which are wait states, or 2000 nanoseconds. Eight-bit bus operations (8 MHz) to 8-bit devices take 8 clock cycles, including 6 wait states, or 1000 nanoseconds.

One refresh cycle equals three clock cycles. It requires 256 refresh cycles every 4 milliseconds to refresh the system RAM.

The 8237A DMA controller operates at 3 or 4 MHz. All DMA data-transfer bus cycles are five clock cycles, 1.66 or 1.25 microseconds, not including bus transfer cycles. DMA channels allocation: 8-bit transfers, channels 0, 1, 2, and 3; 16-bit transfers, channels 5, 6, and 7; channel 4 cascades channels 0 through 3 to the CPU.

80287 NUMERIC COPROCESSOR

The Intel 80287, a numerics processor extension, extends the 80286 architecture with floating point, extended integer and BCD data types. Using a numeric-oriented architecture, the 80287 adds over 50 instructions to those available with the 80286.

The 80287 has two operating modes corresponding to those in the 80286. When reset, the 80287 is in the real-address mode. It can be placed in the protected-address mode by executing the SETPM ESC instruction. The 80287 cannot be switched back to the real-address mode except by a reset. In the real-address mode, the 80286 is completely software compatible with earlier PC-type systems.

Once in the protected-mode, all references to memory for numeric data or status information obey the 80286 memory management and protection rules. This gives a fully protected extention to the 80286 CPU. In protected mode, 80286-numerics software is also completely compatible with earlier PC-type systems.

The 80287 is organized around a stack of eight 80-bit data registers, an instruction pointer, a data pointer, a tag word, and control and status registers. Detailed information about the operation of the 80287 is given in Reference 1 of Table 5-2, above.

Any I/O address generated by the system between 0F8h - 0FFh causes the 80287 to be selected. If the 80287 encounters an error in processing, an error flip-flop reports it to the 80286. I/O address 0F0h causes the error-reporting flip-flop to be reset. I/O address 0F1h causes a reset to the 80287. Both resets are automatically exercised upon power up of the system.

MC146818 REAL-TIME CLOCK PLUS RAM

The real-time clock plus RAM circuit contains the real-time clock and 64 bytes of low-power RAM. Fourteen of those bytes are used by the internal clock. The remaining 50 bytes of RAM are used to store system configuration information. Table 5-3 lists the RAM addresses.

Table 5-3.
Real-Time Clock Plus RAM Addresses

Address (h)	Description
00 - 0D	*Real-time clock information
0E	*Diagnostic status byte
0F	*Shutdown status byte
10	Floppy disk drive byte - drives A and B
11	Reserved
12	Fixed disk drive byte drives C and D
13	Reserved
14	Equipment byte
15	Low-base memory byte
16	High-base memory byte
17	Low-expansion memory byte
18	High-expansion memory byte
19 - 2D	Reserved
2E - 2F	2-byte RAM checksum
30	*Low-expansion memory byte
31	*High-expansion memory byte
32	*Date-century byte
33	*Information flags (set during power-up)
34 - 3F	Reserved

* NOTE: This information is not included in the checksum calculation and is not part of the system configuration information.

Real-Time Clock Information

Table 5-4 lists the real-time clock information at addresses 00 - 0D. Status Registers A - D are initialized during execution of the setup program. Interrupt 1A, BIOS' interface to read/set the time and date, initializes the status byte the same as the setup program.

Table 5-4.
Real-Time Information

Address (h)	Byte Number	Description
00	0	Seconds
01	1	Second alarm
02	2	Minutes
03	3	Minute alarm
04	4	Hours
05	5	Hour alarm
06	6	Day of week
07	7	Date of month
08	8	Month
09	9	Year
0A	10	Status Register A
0B	11	Status Register B
0C	12	Status Register C
0D	13	Status Register D

Status Register A

Bit 7 — **UIP** - This update in progress bit flags the status of the program. If UIP equals 0, then the update cycle is not in progress and the time and date can be read.

Bit 6 - Bit 4 — **DV2, DV1, DV0** - These three bits identify the frequency being used. The system initializes this divider to select the 32.768-kHz time base used in the system.

Bit 3 - Bit 0 — **RS3, RS2, RS1, RS0** - These rate selection bits allow the selection of an output frequency or periodic interrupt. The system initializes the rate selection bits for frequency (1.024 - KHz) and interrupt rate (976.562 microseconds).

Status Register B

Bit 7	**Set** - When set to 0, this bit updates the cycle by advancing the counts at one-per-second. A 1 aborts any update cycle in progress and the program can initialize the time and calendar bytes without any further updates occurring until a 0 is written to this bit.
Bit 6	**PIE** - The Periodic Interrupt Enable is a read/write bit which allows an interrupt to occur at a rate specified by the RS3, RS2, RS1, and RS0 bits in Register A. A 1 enables an interrupt, and a 0 blocks it. The PIE bit is initialized to 0.
Bit 5	**AIE** - The Alarm Interrupt Enable bit is set to 1 to engage the alarm interrupt to register C. A 0 disables the AIE. The AIE is initialized to 0.
Bit 4	**UIE** - The Update-Ended Interrupt Enabled is set to 1 to engage the update-ended interrupt to register C. A 0 disables the UIE. This bit is initialized to 0.
Bit 3	**SQWE** (Square Wave Enabled) A square-wave signal appears on the SQW pin when this bit is set to 1. The frequency is specified by the RS3 to RS0 bit in Register A. The bit is disabled when the signal is low. The system initializes this bit to 0.

Status Register B (continued)

Bit 2	**DM** - The Data Mode bit indicates whether the time and calendar updates are to use binary or BCD formats. A 1 identifies binary data. A 0 represents binary coded data. The DM bit is initialized to 0.
Bit 1	**24/12.** This bit determines whether the information is in the 24-hour mode (1) or 12-hour mode (0). The 24/12 bit is initialized to 1.
Bit 0	**DSE** - Daylight Savings Enabled. This bit is set to 1 in October and April in order to update the time, otherwise, it is set to 0.

Status Register C

Bit 7 - Bit 4	**IRQF, PF, AF, UF** - These flag bits are read only and are affected when the UIE, AIE, and PIE interrupts are enabled.
Bit 3 - Bit 0	**Reserved**

Status Register D

Bit 7	**Valid RAM and Time (VRT)** - By reading the power sense pin, this bit indicates the condition of the contents of the RAM. A 0 occurs when the power is low, indicating that the real-time clock has lost power. A 1 indicates power to the real-time clock and thus data is valid in the CMOS RAM. When power is supplied to the clock, the VRT is set to 1.
Bit 6 - Bit 0	Not used.

RAM Configuration

Table 5-5 shows bit definitions for the RAM configuration bytes at addresses 0E - 3F (h).

Table 5-5
RAM Configuration Information

Diagnostic Status Byte (0Eh)

Bit 7	**Power Loss** - A power loss is indicated by 1. Power on is indicated by 0.
Bit 6	**Checksum Status Indicator** - This bit indicates the status of the configuration record stored in the real-time clock CMOS memory. A 0 means the checksum is good. A 1 means the checksum is bad.
Bit 5	**Incorrect Configuration Information** - After the power is turned on to the unit, a check is made of the equipment byte of the configuration record equipment byte. A 0 indicates that information is valid. A 1 indicates it is invalid. Power-up checks require: (1) at least one floppy disk drive (bit 0 of equipment byte set to 1) and (2) the primary display adapter setting in the configuration matches the motherboard's display switch setting and the actual display hardware in the system.
Bit 4	**Memory Size Miscompare** - This bit compares memory size at the time of power-on with the memory size in the configuration record. A match between the two values is indicated by a 0. A mismatch is indicated by a 1.

Table 5-5 (continued)
RAM Configuration Information

Diagnostic Status Byte

Bit 3	**Disk Controller and Drive C Installation Status** - This bit checks for proper functioning of the fixed disk controller and fixed drive. If both are operating normally, the system can attempt a bootstrap procedure from the fixed disk. A 0 indicates proper functioning, a 1 indicates a failure.
Bit 2	**Time Status Indicator (POST Validity Check).** A 0 indicates that the time is valid, and a 1 indicates that the time is invalid.
Bit 1 - Bit 0	**Reserved.**

Shutdown Status Byte (0Fh)

The status of this byte is determined during a computer self check at the time of power-on.

Type of Diskette Drive (10h)

Bit 7 - Bit 4	Type of first floppy disk drive installed:	
	0000	No drive present
	0001	Double-sided drive (48 TPI)
	0010	High-capacity drive (96 TPI)
	0011 - 1111	**Reserved.**

Table 5-5 (continued)
RAM Configuration Information

Shutdown Status Byte

Bit 3 - Bit 0 Second floppy disk drive type installed:

0000 No drive present

0001 Double-sided drive (48 TPI)

0010 High-capacity drive (96 TPI)

0011 - 1111 Reserved

Address 11h contains a reserved byte.

Fixed Disk Type Byte (12h)

Bit 7 - Bit 4 Identifies the first fixed disk drive installed (drive 1):

0000 No fixed disk drive present

0001 - 1111 Define disk type 1 - (See Fixed Disk Parameters, below)

Bit 3 - Bit 0 Identifies the second fixed disk drive installed (drive 2):

0000 No fixed disk drive present

0001 - 1111 Defines the second fixed disk type (See Fixed Disk Parameters, below)

Table 5-5 (continued)
RAM Configuration Information

Fixed Disk Parameters

Fixed Disk Types					
Type	**Cylinders**	**Heads**	**Capacity (MB)**	**Landing Zone**	**Write Pre-Comp**
*1	306	4	10	305	128
*2	615	4	20	615	300
*3	615	6	31	615	300
*4	940	8	61	940	512
*5	940	6	47	940	512
*6	615	4	20	615	no
*7	462	8	31	511	256
*8	733	5	31	733	no
*9	900	15	114	901	no
10	977	5	41	977	732
*11	855	5	36	855	no
12	640	8	43	640	680
13	1024	8	69	1024	768
14	1024	5	43	1024	768
15	reserved				

* IBM AT compatible

Address 13h also contains a reserved byte.

Equipment Installed Byte (14h) - Defines system configuration at power-up.

Bit 7 - Bit 6 Indicates the number of floppy disk drives installed: 00 = 1 drive, 01 = 2 drives, 10 and 11 are reserved.

Bit 5 - Bit 4 Primary display

00 Reserved
01 Primary display is attached to a color/graphics monitor board in 40-column mode.

Table 5-5 (continued)
RAM Configuration Information

	10 Primary display is attached to a color/graphics monitor board in 80-column mode.
	11 Primary display attached to a monochrome display/printer adapter.
Bit 3 - Bit 2	Not used.
Bit 1	80287 Coprocessor bit:
	0 80287 not installed
	1 80287 installed
Bit 0	Diskette drives installed/not installed.

Low- and High-Base Memory Bytes (15h and 16h)

Bit 7 - Bit 0	**Address:** 15h Low-byte base size 16h High-byte base size
	Valid Sizes:
	0100h 256-Kbyte motherboard RAM
	0200h 512-Kbyte motherboard RAM
	0280h 640-Kbyte motherboard RAM and 128 Kbytes of expansion RAM.

Table 5-5 (continued)
RAM Configuration Information

Expansion Memory Bytes (17h and 18h)

Bit 7 - Bit 0	**Address:** 17h Low-byte size 18h High-byte size Valid Sizes: **0200h** 512-Kbyte I/O channel expansion **0400h** 1024-Kbyte I/O channel expansion **0600h to 3C00h** 15,360-Kbyte I/O channel expansion (15 Mbytes maximum) **Address:** 19h - 2D Reserved

Checksum (10h - 20h)

2Eh	High byte of checksum
2Fh	Low byte of checksum

Low- and High-Expansion Memory Bytes (30h - 31h)

Bit 7 - Bit 0	**Address:** Low-byte expansion size 30h Low-byte expansion size 31h High-byte size Valid sizes: **0200h** 512-Kbyte I/O channel expansion **0400h** 1024-Kbyte I/O channel expansion

Table 5-5 (continued)
RAM Configuration Information

Low- and High-Expansion Memory Bytes (continued)

0600h	1536-Kbyte I/O channel expansion
to	
3C00h	15360K-byte I/O channel expansion (15M bytes maximum)

Expansion memory size is detected through interrupt 15, see schematic sheet 11.

Date Century Byte (32)

Bit 7 - Bit 0	This byte is a binary coded digit value.

Infomation Flag (33h)

Bit 7	Set if the 128 Kbyte I/O channel expansion is installed.
Bit 6	Initiates first user message after SETUP utility program is run.
Bit 5 - Bit 0	Reserved
Addresses 34 - 3F:	Reserved

I/O Operations

Writing real-time clock RAM data:

1. OUT instruction to I/O port 70h with the address to be written to.

2. OUT instruction to I/O port 71h with data to be written.

Reading real-time clock RAM data:

1. OUT instruction to I/O port 70h with the address to be written to.

2. IN instruction from I/O port 71h. Data is returned to the CPU's AL register.

SYSTEM EPROM

Standard 32 Kbytes of EPROM is used for power-up, self test, and I/O driver firmware. Four sockets allow the total EPROM size to be increased up to 128 Kbytes using 32 Kbyte parts. 16 Kbyte ROMs can also be used for a total of 64K bytes. EPROM is not parity checked. Like RAM, the ROM has an access time of 250 nanoseconds.

SYSTEM RAM

The total RAM space in the TeleVideo AT can be up to 15 megabytes. If 64K-bit (type 4164) RAMs are used, up to 256K bytes can exist on the motherboard. If 256K-bit (type 41256) RAMs are used, the motherboard can support up to 512 Kbytes. Using both RAM types, up to 640 Kbytes can exist on the motherboard. The remaining RAM, up to 15 megabytes, can be connected via the eight I/O channels provided on the motherboard. Switches at SW1 on the motherboard tell the system how much memory is currently on the motherboard: 256K, 512K, or 640K. The memory access time is 150 nanoseconds with a full memory cycle time of 275 nanoseconds. The memory map for the TeleVideo AT is listed in Table 5-6.

Table 5-6.
System Memory Map

Address Range(h)	Size	Function
000000 - 07FFFF	512K	System RAM on motherboard
080000 - 09FFFF	128K	Expansion RAM on I/O channel
0A0000 - 0BFFFF	128K	Video RAM
0C0000 - 0DFFFF	128k	Expansion ROM on I/O channel

Table 5-6 (continued)
System Memory Map

Address Range(h)	Size	Function
0E0000 - 0EFFFF	64K	Reserved ROM on motherboard
0F0000 - 0FFFFF	64K	ROM on motherboard
100000 - FDFFFF	15M	Expansion RAM on I/O channel
FE0000 - FEFFFF	64K	Duplicated code at 0E0000h
FF0000 - FFFFFF	64K	Duplicated code at 0F0000h

Each byte of system RAM has nine bits, including one bit for parity. Even parity is used.
The memory refresh circuits request a memory cycle every 15 microseconds through Channel 1 of the 8254 counter/timer. A RAM initialization routine first initializes Channel 1 of the 8254 to generate a 15-microsecond refresh timeout. Once Channel 1 is initialized, the memory refresh circuit performs a memory read operation to the 256 rows of memory in the RAM array, one row per refresh cycle. During each refresh cycle, the memory refresh circuits require the use of the address bus. Therefore, every 15 microseconds, the memory refresh circuits must also arbitrate bus requests by the DMA controller and CPU, which are also trying to get control of the address and data busses for their own operations.

8237A DMA CONTROLLERS

Seven DMA channels are available in the TeleVideo AT for use by various controllers on the I/O channels. A pair of Intel 8237A DMA Controllers are used, each supporting four channels. DMA Controller 1 contains channels 0 - 3 for 8-bit data transfers between 8-bit devices on the I/O Channels and 8- or 16-bit memory. A DMA data transfer can occur anywhere within the 16-megabyte address space. However, because of the internal structure of the 8237A, the maximum number of bytes that can be transferred at one time is a block of 64 Kbytes. The DMA channels are assigned as listed in Table 5-7.

Table 5-7.
DMA Channel Assignments

Channel Number	Function
DMA Controller 1	
0	Spare
1	Spare
2	Floppy Disk Controller
3	Spare
DMA Controller 2	
4	Cascade for DMA Controller 1
5	Spare
6	Spare
7	Spare

DMA Controller 2 manages channels 4 - 7. Channel 4 cascades the four DMA Controller 1 channels through to the CPU. The remaining channels, 5, 6, and 7, support 16-bit data transfers between 16-bit devices on the I/O Channels and 16-bit memory. These channels can transfer data in the 16-megabyte address space in blocks up to 128 Kbytes. Channels 5, 6, and 7 can transfer data only on even-byte boundaries.

Page Register

For a DMA transfer to operate in the entire address range of the AT, the CPU addresses a page register to specify which 64 Kbyte block, that is, page of memory will be transferred. Table 5-8 lists the addresses for the page register.

Table 5-8.
Page Register Assignments

Address (h)	Page Register
0087	DMA Channel 0
0083	DMA Channel 1
0081	DMA Channel 2
0082	DMA Channel 3
008B	DMA Channel 5
0089	DMA Channel 6
008A	DMA Channel 7

Source address generation for DMA controllers is as follows:

DMA Channel	DMA Page Registers	8237A
0 - 3	A23 to A16	A15 to A0
5 - 7	A23 to A17	A16 to A1

Generating the Byte High Enable (BHE) address signal for channels 0 - 3 is accomplished by inverting address line A0 and for channels 5 - 7 by forcing address line A0 to logic 0.

Programming 16-Bit DMA Channels 5, 6, and 7

Since DMA Channels 5, 6, and 7 can only handle 16-bit data transfers, access can be gained only to 16-bit I/O devices on the I/O channels. Control of DMA Controller 2, which contains these channels, is via I/O addresses 0C0 - 0DF. The command codes for DMA Controller 2 is listed in Table 5-9.

Table 5-9.
DMA Controller 2 Command Codes

Address (h)	Command Code
0C0	Channel 0 Base and Current Address
0C2	Channel 0 Base and Current Word Count
0C4	Channel 1 Base and Current Address
0C6	Channel 1 Base and Current Word Count
0C8	Channel 2 Base and Current Address
0CA	Channel 2 Base and Current Word Count
0CC	Channel 3 Base and Current Address
0CE	Channel 3 Base and Current Word Count
0D0	Read Status Register/Write Command Register
0D2	Write-Request Register
0D4	Write Single-Mask Register Bit
0D6	Write-Mode Register
0D8	Clear Byte Pointer Flip-Flop
0DA	Read Temporary Register
0DC	Clear Mask Register
0DE	Write All Mask Register Bits

Data written to the base address registers of channels 5, 6 and 7 is the dividend of the real address divided by two. Also, when the base word count for channels 5, 6, and 7 is specified, the count is the number of 16-bit words to be transferred.

Therefore, these DMA channels transfer a maximum of 64K words or 128 Kbytes for any selected page in memory, thus dividing the total memory space of the system into 128 Kbyte pages. When the page for DMA Channels 5, 6, and 7 is specified, data bits D1 - D7 should contain the high-order seven address bits (A17 - A23) of the desired memory space. Data bit D0 is not used in the generation of the DMA memory address.

Note that after the system is powered-up, all internal locations of the DMA controllers should be loaded with some valid value, even if some of the channels are not used. Also, DMA transfers occur on even-byte boundaries for channels 5, 6 and 7. See Reference 1 in Table 5-2 for more information.

8259A INTERRUPT CONTROLLERS

Sixteen levels of system interrupts are provided by the 80286 CPU's Interrupt request (INTR) and a pair of Intel 8259A Interrupt Controllers. Any or all interrupts can be masked (ignored) by the CPU, including the CPU's own NMI. Table 5-10 lists the interrupt levels in decreasing priority.

Table 5-10.
System Interrupts

Interrupt Level		Function
80286 NMI		Parity or I/O Channel Check
Interrupt Controllers 1	2	
IRQ0		Timer Output 0
IRQ1		Keyboard (Output Buffer Full)
IRQ2		Interrupt from Interrupt Controller 2
IRQ3		Serial Port 2
IRQ4		Serial Port 1
IRQ5		Parallel Port 2
IRQ6		Floppy Disk Controller
IRQ7		Parallel Port 1
	IRQ8	Real-Time Clock Interrupt
	IRQ9	Software Redirected to INT 0Ah (IRQ2)
	IRQ10	Reserved
	IRQ11	Reserved
	IRQ12	Reserved
	IRQ13	80287 Coprocessor
	IRQ14	Fixed Disk Controller
	IRQ15	Reserved

8254 PROGRAMMABLE TIMER

An Intel 8254 counter/timer circuit provides three programmable counter/timer channels: a system timer, refresh request generator, and tone generator for the speaker. The 8254 is treated by the system software as four external I/O ports. Three of the ports are treated as counters; the fourth is a control register for mode programming. See Reference 1 listed in Table 5-2 for more information. The channel assignments are listed in Table 5-11.

Table 5-11.
Counter/Timer Channel Assignments

Control/Output	Connection
Channel 0	**System Timer**
GATE 0	Tied On
CLK IN 0	1.190-MHz Oscillator
CLK OUT 0	8259A IRQ 0
Channel 1	**Refresh Request Generator**
GATE 1	Tied On
CLK IN 1	1.190-MHz Oscillator
CLK OUT 1	Refresh Request Cycle (REFRESH)
Channel 1	**Tone Generator**
GATE 2	Controlled by bit 0 of port 61 PPI bit
CLK IN 2	1.190-MHz Oscillator
CLK OUT 2	Used to drive speaker

8042 KEYBOARD CONTROLLER

The keyboard is controlled by an Intel 8042 single-chip microcomputer. The chip is programmed to transmit and receive data from the keyboard, translate scan codes and give data to

the system. Communication between the controller and keyboard is in serial format and is synchronized by the clock supplied by the keyboard.

Receiving Data from the Keyboard

Keyboard data is sent in serial format over clock and data lines using an 11-bit data packet:

1 - start bit (0 bit)
8 - data bits (bit 0 first)
1 - parity bit
1 - stop bit

The keyboard generates the clock signal to time the data to the controller. If the keyboard controller does not receive the data correctly, FFh is placed in its output buffer and bit 7 of the status register is set to 1, indicating a parity error. The keyboard controller also times a byte of data from the keyboard. If the keyboard does not receive data from the controller within two milliseconds, FFh is set in the keyboard controller's output buffer (status register bit 6). The controller will not attempt retries when a receive time-out error occurs.

Scan-Code Translation

Scan codes received from the keyboard by the keyboard controller are converted before being placed in the controller's output buffer. Figure 5-1 shows the keyboard layout with key numbers and Table 5-12 lists the keyboard scan codes and translated system scan codes for each key.

Figure 5-1.
Key Layout

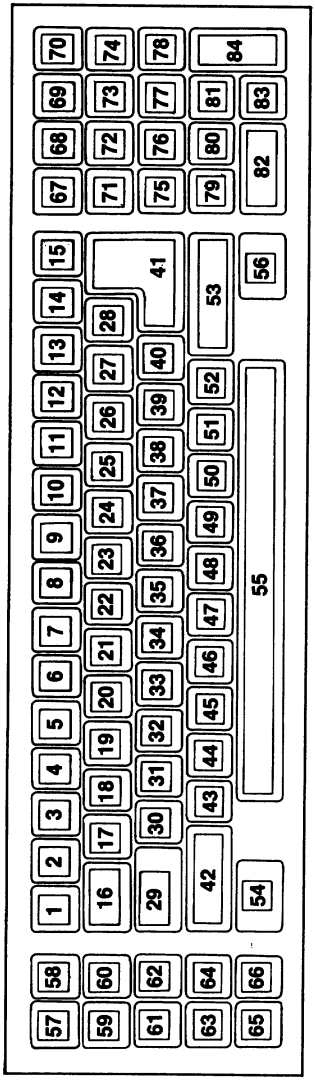


Table 5-12.
Keyboard Scan-Code Translation Table

Key #	Keyboard Scan Code	System Scan Code
Active Scan Codes:		
1	OE	29
2	16	02
3	1E	03
4	26	04
5	25	05
6	2E	06
7	36	07
8	3D	08
9	3E	09
10	46	0A
11	45	0B
12	4E	0C
13	55	0D
14	5D	2B
15	66	0E
16	OD	0F
17	15	10
18	1D	11
19	24	12
20	2D	13
21	2C	14
22	35	15
23	3C	16
24	43	17
25	44	18
26	4D	19
27	54	1A
28	5B	1B
29	14	1D
30	1C	1E
31	1B	1F
32	23	20
33	2B	21
34	34	22
35	33	23
36	3B	24
37	42	25
38	4B	26
39	4C	27
40	52	28
41	5A	1C
42	12	2A
43	1A	2C

Table 5-12.
Keyboard Scan-Code Translation Table

Key #	Keyboard Scan Code	System Scan Code
44	22	2D
45	21	2E
46	2A	2F
47	32	30
48	31	31
49	3A	32
50	41	33
51	49	34
52	4A	35
53	59	36
54	11	38
55	29	39
56	158	3A
57	05	3B
58	06	3C
59	04	3D
60	0C	3E
61	03	3F
62	0B	40
63	02 or 83	41
64	0A	42
65	01	43
66 or 83	09	44
67	76	01
68	77	45
69	7E	46
70	7F or 84	54
71	6C	47
72	75	48
73	7D	49
74	7C	37
75	6B	4B
76	73	4C
77	74	4D
78	7B	4A
79	69	4F
80	72	50
81	7A	51
82	70	52
83	71	53
84	79	4E

Sending Data to the Keyboard

If the keyboard does not start clocking data out of the controller within 15 milliseconds, or finish clocking the data out (after it starts clocking) within 2 milliseconds, bit 5 of the status register is set and FEh is placed in the output buffer.

If the keyboard does not respond to the data sent (the keyboard must respond to all data sent from the controller) within a specified time, bits 5 and 6 of the status register are set and FEh is placed in the output buffer.

If the keyboard does not finish clocking the reponse into the controller within 25 milliseconds, bits 5 and 6 are set in the status register and FEh is placed in the output buffer.

If the keyboard response is received with a parity error, bits 5 and 7 are set in the status register and FEh is placed in the output buffer.

Inhibit Capability

The AT is provided with the capability to physically inhibit the keyboard. However, the user must install the mechanical/electrical means for inhibiting the keyboard. This can be accomplished by connecting J21 to a key switch. The controller tests the data received from the keyboard to determine if it is a command response or a scan code. A command response is placed in the keyboard controller's output buffer. It is ignored if the data is a scan code.

Keyboard Controller System Interface

The keyboard controller communicates with the system through a status register, an output buffer, and an input buffer.

The status register is an 8-bit register at I/O address 64h providing the current controller status. System input to I/O address 64h is considered a controller command. System input to I/O address 60h is intended for the keyboard and will be checked for parity. It will then be transmitted to the keyboard with odd parity.

Table 5-13.
Keyboard Controller System Interface - Status Register

Bit 7	**Parity Error.** A 0 represents odd parity, and no parity errors were detected in data received from the keyboard. Even parity in the data received from the keyboard represents an error and bit 7 is set to 1.
Bit 6	**Receive Time-Out Error** - A 1 indicates that a transmission from the keyboard was not finished in the specified time.
Bit 5	**Transmit Time Out** - A 1 indicates that a transmission by the keyboard was not clocked out within 2 milliseconds. If the byte is clocked out but the keyboard does not respond, then the receive time out and transmit time outs are set to 1. If the byte is received with a parity error, then the parity error bit and the transmit time-out bit are set to 1.
Bit 4	**Inhibit Switch** - This bit checks the status of the keyboard, whether inhibited or non-inhibited. The check occurs at the input port, bit 7. A 1 identifies the non-inhibited state.
Bit 3	**Command/Data** - The 8042 controller uses this bit to decide if the byte in the input buffer is at the command port or the data port. Writing to address 60h sets this bit to 0, writing to address 64h sets the bit to 1.

Table 5-13. (continued)
Keyboard Controller System Interface - Status Register

Bit 2	**System Flag** - This bit can be set or reset by writing to the system's flag bit in the keyboard controller's command byte. It is set to 0 after a power-up reset.
Bit 1	**Input Buffer Full** - A 1 indicates that the input buffer (I/O address 60h or 64h) is full but the controller has not read the data. The buffer is empty when the bit is set to 0.
Bit 0	**Output Buffer Full** - A 1 indicates that the controller has placed data into its output buffer but the system has not read the data. This bit is reset to 0. The output buffer should not be read when the output buffer full bit is 0.

Output Buffer

The keyboard controller uses the output buffer to send data bytes and scan codes to the system. This 8-bit read-only register at I/O address 60h should be read only when the output buffer's is full (bit 0 = 1).

Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60h or 64h. Data input to 60h will be checked for parity and sent to the keyboard unless the data is intended for use by the controller. Data input to address 64h is compared to known controller commands for a match. Data should not be written to address 64h when the controller's input buffer full bit is 1.

Table 5-14 is a list of the keyboard controller interface system commands.

Table 5-14.
Keyboard Controller System Interface - System Commands (I/O Address 64h)

20	**Read Keyboard Controller's Command Byte.** The controller puts its current command byte in its output buffer.
60	**Write Command Byte.** The next byte of data written to the controller is placed in the controller's command byte.

Command byte bit definition:

Bit 7	Not used (set to 0)
Bit 6	**IBM PC-Compatibility Mode** When set to 1, this bit notifies the controller to convert scan codes received from the keyboard into those used by the IBM PC.
Bit 5	**IBM PC Mode** - When set to 1, this bit programs the controller for communication with the IBM PC keyboard interface.
Bit 4	**Keyboard Disable** - When set to 1, this bit blocks the keyboard interface by keeping the clock signal low.

Table 5-14.
Keyboard Controller System Interface - System Commands (I/O Address 64h)

Bit 3 **Inhibit Override** - Overrides the keyboard inhibit function when set to 1.

Bit 2 **System Flag** - The value written to this bit is placed in the system flag bit of the controller's status register.

Bit 1 Not used (set to 0)

Bit 0 **Enable Output-Buffer-Full Interrupt** - A 1 causes the keyboard controller to generate an interrupt when it places data in its output buffer.

AA **Self-Test.** Self-test instructs the controller to perform internal tests. A 55h is placed in the output buffer if no errors are detected.

AB **Interface Test.** Tests the keyboard clock and data lines. Test Results:

00 No error detected.

01 The keyboard clock line is stuck low.

02 The keyboard clock line is stuck high.

03 The keyboard data line is stuck low.

04 The keyboard data line is stuck high.

Table 5-14.
Keyboard Controller System Interface - System Commands (I/O Address 64h)

AC	**Diagnostic Dump** - Sends 16 bytes of keyboard controller RAM and the current status of the following: Input port, output port, and program status word.
AD	**Disable Keyboard Feature** - Sets bit 4 of the command byte, disabling the keyboard interface by keeping the clock line low. No data is sent or received.
AE	**Keyboard Interface Enable** - Clears bit 4 of the command byte, releasing the keyboard interface.
C0	**Read Input Port** - This command instructs the controller to read the input port and place that information in its output buffer.
D0	**Read Output Port** - This command instructs the controller to read its output port and place the data in its output buffer. Issue this command only if the output buffer is empty.
D1	**Write Output Port** - The 8042 controller uses this command to write the next data byte written to I/O address 60h to its output port. Setting this bit to zero (0) will cause a system reset.
E0	**Read Test Inputs** - This command signals the controller to read test inputs T0 and T1. The controller then places the results in the output buffer. Bit 0 represents T0 and bit 1 represents T1.

Table 5-14. (continued)
Keyboard Controller System Interface - System Commands (I/O Address 64h)

F0-FF	**Pulse Output Port** - The controller pulses bits 0 to 3 of the output port for approximately 6 microseconds. Bits 0 - 3 of this command indicate which bits are to be pulsed. The bit should be pulsed if a 0 is encountered, and a 1 indicates the bit should not be pulsed. Bit 0 of the controller's output port is connected to System Reset and pulsing this bit resets the CPU.

Controller Ports

The controller receives input from the system or the keyboard at the input port and information is output through the output port. Input and output are transmitted serially using the clock and data lines. Test inputs T0 and T1, generated by system command E0, indicate clock and data line status.

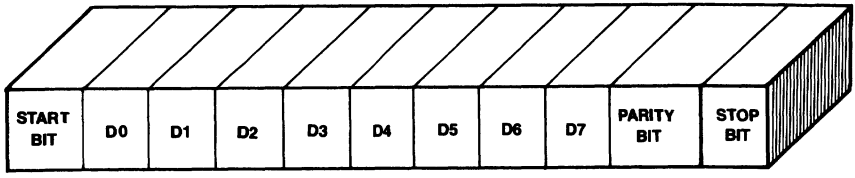
RS-232C SERIAL PORT

The RS-232C serial port is based on a National NS16450 Asynchronous Communications Element (ACE). The NS16450 is fully programmable and will add and remove start, stop, and parity bits. It will support 5- to 8-bit characters with 1, 1.5, and 2 stop bits. Baud rate generation can be programmed for one of eight levels, ranging from 110 to 9600 baud. The NS16450 provides prioritized interrupt of the error, line status and receive signals. It also provides data set interrupts. The rear-panel connector for the serial port is a 9-pin D-type connector (refer to Chapter 8, Interface, of this manual for pin assignments).

Serial Data Structure

Figure 5-2 shows the data structure of the serial interface. The start bit is automatically inserted at the beginning of the transmission by the controller. This is followed by bit 0 of the data byte (bit 0 is the first bit to be sent or received). The parity (if supplied) and stop bits are then added to the data format by the controller after bit 7 of the data byte is transmitted/received. The input and output signals for the NS16450 device are fully in accord with EIA standard RS-232C and are described in Reference 2 listed in Table 5-2.

Figure 5-2. Serial Interface Data Transmission Structure



Serial Port Registers

The NS16450 has many registers accessible to the system programmer through the CPU. The serial port can be addressed as either Communications Port 1 or Communications Port 2 as defined by jumper W1 on the motherboard (refer to User's Manual).

Serial port I/O addresses specified in this manual are prefaced with an X. X can be either 3 for Communications Port 1 (interrupt level 4) or a 2 for Communications Port 2 (interrupt level 3). The registers control serial port operations. Specific registers are selected according to Table 5-15. Detailed descriptions of the registers are given in Reference 2 of Table 5-2, I/O Device Reference Literature.

Table 5-15. Serial Port Registers

Address	Register	DLAB State
XF8	TX Buffer	0 (write)
XF8	RX Buffer	0 (read)
XF8	Divisor Latch LSB	1
XF9	Divisor Latch MSB	1
XF9	Interrupt Enable Register	0
XFA	Interrupt Identification Register	
XFB	Line Control Register	
XFC	Modem Control Register	
XFD	Line Status Register	
XFE	Modem Status Register	
XFF	Reserved	

PARALLEL PRINTER PORT

The parallel port, a standard, Centronics-compatible printer, that supports most parallel, output-only devices. On the rear panel of the system, the parallel port connector is a 25-pin D-type connector.

The system can support two parallel ports. This port can be selected to operate as Parallel Port 1 or Parallel Port 2 as defined by jumpers at W2 on the motherboard. Parallel port I/O addresses specified in this manual are prefaced with X. X can be either 3 for Parallel Port 1 or a 2 for Parallel Port 2.

Data Latch (X78h, X7Ch)

A read command to this address sends data in the printer buffer to the CPU. A write command to this address stores data in the printer buffer.

Parallel Printer Control Signals (X7Ah, X7Eh)

The signals stored at this address are read by the CPU. The following are the bit definitions:

Bit 0 **STROBE** - Strobe is a 0.5-microsecond minimum, high, active pulse for clocking data. The data must be present for a minimum of 0.5 microseconds before and after the pulse.

Bit 1 **AUTO FD XT** - A 1 causes the printer to line-feed after a line is printed.

Bit 2 **INIT** - A 0 starts the printer (50-microsecond pulse, minimum).

Bit 3 **SLCT IN** - A 1 in this bit position selects the printer.

Bit 4 **IRQ Enable** - A 1 in this position allows an interrupt to occur when "ACK-" changes from true to false.

Bit 5 - Bit 7 **Not used.**

Printer Status (X79h, X7Dh)

This byte is read by the CPU. The following are bit definitions:

Bit 0 - Bit 2 **Unused**

Bit 3 **Error** - A 0 indicates printer error.

Bit 4 **SLCT** - When set to 1, this bit indicates that the printer has been selected.

Bit 5 **PE** - A 1 indicates that the printer has reached the end of the paper.

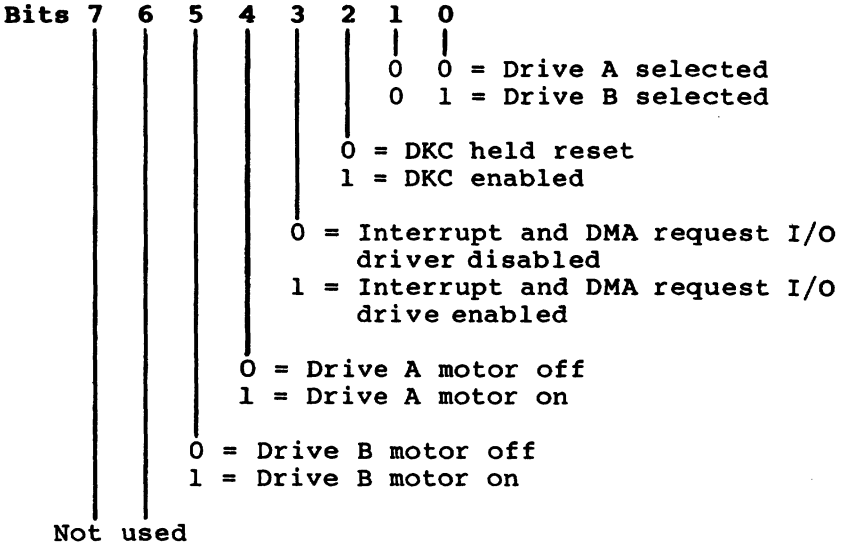
Bit 6 **ACK** - When set to 0, this bit indicates that the printer has received a character and is ready to receive another character.

Bit 7	**BUSY** - This bit indicates that the printer is busy and cannot accept data. The busy signal may indicate that the printer is not working, the print head is moving, or that the printer is currently receiving data.

DISKETTE CONTROLLER

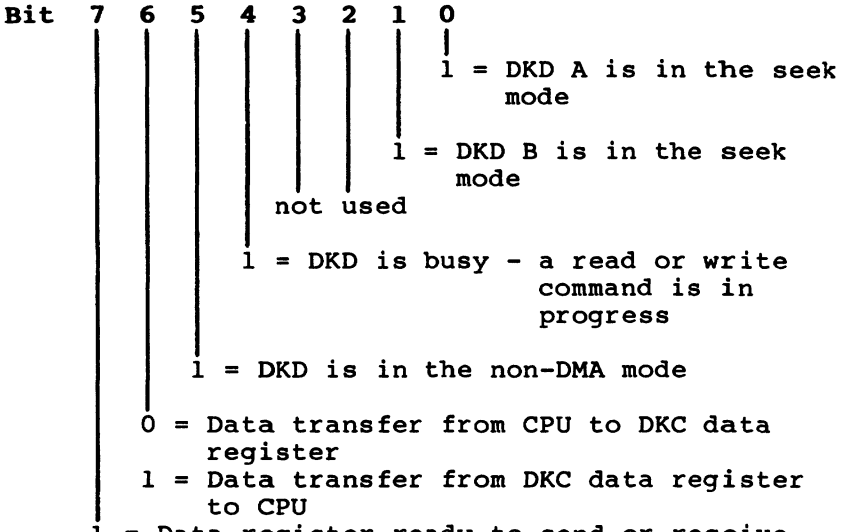
The diskette controller (DKC) uses a write only, digital-output register at 3F2h to control the drive motors, drive selection, and feature enable. Table 6-1 lists the bit assignments for the digital-output register.

Table 6-1
Digital-Output Register



The DKC has two registers accessible to the CPU: a status register at 3F4h and a data register at 3F5h. The status register contains status information on the DKC, shown in Table 6-2, and may be accessed at any time. The data register stores data, commands, and parameters and provides diskette drive (DKD) status information. Data bytes are read from or written to the data register in order to program or obtain results after a command.

Table 6-2
DKC Status Register
(3F4h)



The DKC is capable of performing 15 different commands. Commands are initiated by a multibyte transfer from the CPU. The result after execution of a command may include a multibyte transfer back to the CPU. Table 6-3 is a summary of the DKC commands. Table 6-4 defines the symbols used in the command table.

Table 6-3
DKC Command Summary

		DATA BUS								
Command Phase	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Remarks**
					READ DATA					
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution.
	W				GPL					
	W				DTL					

Table 6-3 (continued)
DKC Command Summary

Execution											Data transfer between DKD and system.
Result	R				ST0						Status information after command execution.
	R				ST1						
	R				ST2						
	R				C						Sector ID information after command execution.
	R				H						
	R				R						
	R				N						

READ DELETED DATA

Command	W	MT	MF	0	0	1	0	0	1		Command Codes
	W	x	x	x	x	x	HD	US1	US0		
	W				C						Sector ID information prior to command execution
	W				H						
	W				R						
	W				N						
	W				EOT						
	W				GPL						
	W				DTL						
Execution											Data transfer between DKD and system.
Result	R				ST0						Status information after command execution.
	R				ST1						
	R				ST2						
	R				C						Sector ID information after command execution.
	R				H						
	R				R						
	R				N						

WRITE DATA

Command	W	0	MF	SK	0	0	0	1	0		Command Codes
	W	x	x	x	x	x	HD	US1	US0		
	W				C						Sector ID information prior to command execution
	W				H						
	W				R						
	W				N						
	W				EOT						
	W				GPL						
	W				DTL						

Table 6-3 (continued)
DKC Command Summary

Execution										Data transfer between DKD and system.
Result	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

WRITE DELETED DATA

Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID information prior to command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between DKD and system.
Result	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

READ A TRACK

Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID information prior to command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					

Table 6-3 (continued)
DKC Command Summary

Execution				Data transfer between DKD and system. DKC reads all cylinders from index hole to EOT.
Result	R		ST0	Status information
	R		ST1	after command
	R		ST2	execution.
	R		C	Sector ID
	R		H	information
	R		R	after command
	R		N	execution.

READ ID

Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
Execution										First correct ID information cylinder is stored in data register.
Result	R				ST0					Status
	R				ST1					information
	R				ST2					after command
	R				C					execution. Sector
	R				H					ID information
	R				R					during execution.
	R				N					

FORMAT A TRACK

Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				N					Bytes/Sector
	W				SC					Sector/Track
	W				GPL					Gap 3
	W				D					Filler byte.
Execution										DKC formats an entire cylinder.

Table 6-3 (continued)
DKC Command Summary

Result	R	ST0	Status
	R	ST1	information
	R	ST2	after command
	R	C	execution. In
	R	H	this case, ID
	R	R	information
	R	N	has no meaning.

SCAN EQUAL

Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution.
	W				GPL					
	W				DTL					
	W				STP					
Execution										Data compared between DKD and system.
Result	R				ST0					Status information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID
	R				H					information
	R				R					after command
	R				N					execution.

SCAN LOW OR EQUAL

Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution.
	W				GPL					
	W				DTL					
	W				STP					

Table 6-3 (continued)
DKC Command Summary

Execution			Data compared between DKD and system.
Result	R	ST0	Status information after command execution.
	R	ST1	
	R	ST2	
	R	C	Sector ID information after command execution.
	R	H	
	R	R	
	R	N	

SCAN HIGH OR EQUAL

Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID information prior to command execution.
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
	W				STP					
Execution										Data compared between DKD and system.
Result	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

Table 6-3 (continued)
DKC Command Summary

RECALIBRATION

Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	x	x	x	x	x	0	US1	US0	
Execution										Head retracts to track 0.

SENSE INTERRUPT STATUS

Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R				ST0					Status information at end of seek operation.
	R				PCN					

SPECIFY

Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	---SRT--------|-------HUT---								
	W	|------HLT--------------| ND							

SENSE DRIVE STATUS

Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
Result	R				ST3					Status DKD information

SEEK

Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				NCN					
Execution										Head positioned over proper cylinder on diskette.

INVALID

Command	W	Invalid Codes	Invalid command codes (NoOp-DKC goes into standby state).
Result	R	ST0	ST0 = %80.

Table 6-4
DKC Command Symbols

Symbol	Name	Description
C	Cylinder Number	The current/selected cylinder (track) number.
D	Data	The data pattern that is written into a sector.
D7-D0	Data Bus	8-bit data bus, where D7 stands for the most significant bit and D0 the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for data length that users read from or write to the sector.
EOT	End of Track	The final sector number on a cylinder.
GPL	Gap Length	The length of gap 3 (spacing between sectors excluding VCO sync field).
H	Head Address	The head number 0 or 1, as specified in the ID field.
HD	Head	A selected head number 0 or 1. (H=HD in all command words.)
HLT	Head Load Time	The head load time in the DKD (2 to 256 milliseconds in 2-millisecond increments for the 1.2-Mbyte drive and 4 to 512 milliseconds in 4-millisecond increments for the 360-Kbyte drive).

Table 6-4 (continued)
DKC Command Symbols

Symbol	Name	Description
HUT	Head Unload Time	The head unload time after a read or write operation has occurred (0 to 240 milliseconds in 16-millisecond increments for the 1.2-Mbyte drive and 0 to 480 milliseconds in 32-millisecond increments for the 360-Kbyte drive).
MF	FM or MFM Mode	If MF is low, FM mode is selected. If it is high, MFM mode is selected only if MFM is implemented.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)
N	Number	The number of data bytes written in a sector.
NCN	New Cylinder	A new cylinder number to define the desired position of the head after the seek operation.
ND	Non-DMA Mode	Operation in the non-DMA mode.
PCN	Present Cylinder	Cylinder number at the completion of sense-interrupt-status command that indicates the position of the head at the present time.
R	Record	The sector number to be read or written.
R/W	Read/Write	Either a read or write operation.

Table 6-4 (continued)
DKC Command Symbols

Symbol	Name	Description
SC	Sector	Indicates the number of sectors per cylinder.
SK	Skip	Skip deleted-data address mark.
SRT	Step Rate Time	DKD stepping rate 2 to 32 microseconds (in 2-microsecond increments).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	One of four command status registers that stores status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register. The registers shown here may only be read after a command has been executed, and contain information relevant to that particular command.
STP	Scan Test	If STP=1 during a scan operation, the data in contiguous sectors is compared byte-by-byte with data sent from the CPU. If STP=2, then alternate sectors are read and compared.

Command Status Register 0

Bit	Name	Description
D0	Unit Select 0	Used to indicate a drive unit number at interrupt.
D1	Unit Select 1	

Command Status Register 0 (continued)

Bit	Name	Description
D2	Head Address	Used to indicate the state of the head at interrupt.
D3	Not Ready	This bit is set when the DKD is in the not-ready state and a read or write command is issued.
D4	Equipment Check	This bit is set if a fault is received from the DKD, or if the track 0 signal fails to occur after 77 step pulses (recalibrate command).
D5	Seek End	This bit is set when the DKC completes the seek command.
D6	Interrupt	
D7	Code	
	D7 D6	
	0 0	Normal termination of command. Command was completed and properly executed.
	0 1	Abnormal termination of command. Execution of the command was started, but was not successfully completed.
	1 0	Invalid command issue. The command that was issued was never started.
	1 1	Abnormal termination because, during execution, the ready signal from the DKD changed states.

Command Status Register 1

Bit	Name	Description
D0	Missing Address	This bit is set if the DKC cannot detect the ID address mark. Note, the missing address mark in the data field of status register 2 is also set.
D1	Not Writeable	This bit is set if the DKC detects a write-protect signal from the DKD during execution of a write data, or format disk command.
D2	No Data	This bit is set if 1) the DKC cannot find the sector specified in the ID register during execution of a read data, write deleted data, or scan command, 2) the DKC cannot read the ID field without an error during execution of the read ID command, or 3) the starting sector cannot be found during execution of the read a cylinder command.
D3	Not Used	Always set = 0
D4	Over Run	This bit is set if the DKC is not serviced by the main system during data transfers within a certain time interval.
D5	Data Error	This bit is set if the DKC detects a cyclic redundancy check (CRC) error in either the ID field or the data field.
D6	Not Used	Always set = 0
D7	End of Cylinder	This bit is set when the DKC tries to access a sector beyond the final sector of a cylinder.

Command Status Register 2

Bit	Name	Description
D0	Missing Address Mark in Data Field	This bit is set if the DKC cannot find a data address mark or deleted data address in Data Field when data is read from the medium.
D1	Bad Cylinder	This bit is set when contents of C on the medium are different from that stored in ID register, or when the contents of C are FFh.
D2	Scan Not Satisfied	This bit is set if DKC cannot find a sector on the cylinder that meets the condition during execution of scan command.
D3	Scan Equal Hit	This bit is set if equal condition is satisfied during execution of scan command.
D4	Wrong Cylinder	This bit is set when the contents of C on the medium are different from that stored in the ID register.
D5	Data Error in Data Field	This bit is set if the DKC detects a CRC error in the data.
D6	Control Mark	This bit is set if the DKC encounters a sector containing a deleted data address mark during execution of read data or scan command.
D7	Not Used	Always = 0

Command Status Register 3

Bit	Name	Description
D0	Unit Select 0	The status of the unit-select-0 signal from the DKD.
D1	Unit Select 1	The status of the unit-select-1 signal from the DKD.
D2	Head Address	The status of the side-select signal from the DKD.
D3	Two Side	The status of the two-side signal from the DKD.
D4	Track 0	The status of the track 0 signal from the DKD.
D5	Ready	The status of the ready signal from the DKD.
D6	Write Protect	The status of the write-protected signal from the DKD.
D7	Fault	The status of the fault signal from the DKD.

FIXED (WINCHESTER) DISK CONTROLLER

The Winchester disk controller contains a WD1010-05 Winchester disk controller device to perform executive control over fixed disk operations. To command the board, the system addresses a set of task file registers in the WD1010-05 with the I/O port address of each individual register. Table 6-5 is a list of the individual registers, along with their I/O port addresses for the AT:

Table 6-5
AT Registers

Address	Read	Write
01F0h	Data Access	Data Access
01F1h	Error Flags	Write Precomp Cylinder
01F2h	Sector Count	Sector Count
01F3h	Sector Number	Sector Number
01F4h	Cylinder Low	Cylinder Low
01F5h	Cylinder High	Cylinder High
01F6h	Sector/Drive/Head	Sector/Drive/Head
01F7h	Status Register	Command Register

A detailed description of the WD1010-05 device is given in the Storage Management Products Handbook, June, 1984, published by the Western Digital Corporation, Irvine, CA.

Data Access

For a typical operation, the task file registers are written to or read for status, and a command is given to the command register. The WD1010-05 then tri-states the address bus and executes the command. At the end of the operation, the task file is again opened to the system.

Error Register

The error register contains error flags for bad block detect, CRC data field, ID not found, aborted command, TK0000 error, and data address mark error. During read operations, the error register is read after the data is read out of buffer RAM, that is, after the byte count goes to zero. The error register bit assignments are listed in Table 6-6.

Table 6-6.
Error Register Bit Assignments

Bit	Description
0	This bit is set during a read sector command if the data address mark is not found after the proper sector ID is read.
1	This bit is set only by the restore command. It indicates the head is not positioned over track 000.
2	This bit is set if a command was issued while the status register shows a drive fault (bit 5), or command disable (bit 6) condition. This bit is also set if an undefined command is issued.
4	This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk. This bit is also set if a cyclic redundancy check error has occurred.
6	This bit is set if a data field CRC error has occurred or the data mark address has not been found.
7	This bit is set if an ID field has been encountered that contains a bad block mark (used for bad sector mapping).

Write Precomp

Write precomp defines the starting cylinder number at which reduced write current (RWC) begins. This value is in the range 0 to 255, and is internally multiplied by four to obtain the actual cylinder.

Sector Count

Sector count represents the number of sectors that are to be transferred to buffer RAM. Because this is a decrementing function, all zeros are written for a 256-sector transfer and a 1 is written for a one-sector transfer.

Sector Number

Sector number contains the starting sector of a transfer in the range 0 to 255. This register is incremented with every transfer.

Cylinder Number Low

Cylinder number low represents the least-significant eight bits of the starting cylinder number in the range 0 through 1023.

Cylinder Number High

Cylinder number high carries the most-significant bits of the starting cylinder number as bits 0(8) and 1(9). The other bits of this register are unused.

Sector/Drive/Head Register

The sector/drive/head register contains the sector size, drive number, and head number parameters for the operation:

```
Bit   7   6   5   4   3   2   1   0
      |   |   |   |   |   |   |   |
                    0   0   0   0 = Select head 0
                    0   0   0   1 = Select head 1
                    .   .   .   . =     .   .
                    1   0   0   0 = Select head 8
                    .   .   .   . =     .   .
                    1*  1   1   1 = Select head 15
                |
                0   = Select drive 1
                1   = Select drive 2
            |
            1 = 512 bytes/sector
        0 = 512 bytes/sector (bit 5 set to 1)
    |
0 = CRC mode
```

***NOTE:** Set bit 3 (3F6h) to 1 for heads 8 through 15.

Bit 7, an extension bit, extends the data field by seven bytes when ECC codes are used. When set to 1, CRC is not appended to the end of the data field; the data field becomes sector size + 7 bytes long.

The sector/drive/head (SDH) byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written and contains a bad block in bit 7.

Status Register

The status register identifies the status bits for device busy, device ready, write fault (same as WF line), seek complete (same as SC line), data request (same as BDRQ line), command in progress, and error register flags set. The status register bit assignments are listed in Table 6-7.

Table 6-7
Status Register Bit Assignments

Bit	Description
0	This bit is set whenever any bits in the error register are set. The bit is reset when a new command is written into the command register.
1	When this bit is set, a command is being executed and a new command should not be loaded.
2	Not used
3	This bit is set when the sector buffer should be loaded or read (depending on the command). It is reset upon completion of the operation.
4	This bit is set when a seek is completed.
5	This bit indicates a fault condition at the drive when set. An interrupt is generated when this bit is set.
6	This bit reflects the state of DRDY and must be set for commands to execute.
7	This bit is set whenever the disk is being accessed. Commands should not be loaded into the command register when this bit is set. This bit is reset at the end of all commands except the read sector command. This bit is reset after the sector buffer is filled on the read sector command.

Control Register - Manipulates fixed disk logic. Allows the programmer to set the read and write enable, interrupt acknowledge, reset, buffer ready, buffer counter reset and LED select. The control register bit assignments are listed in Table 6-8.

Table 6-8
Control Register Bit Assignments

Bit	Description
0	The fixed disk controller will be reset when this bit is set to 1 followed by resetting to 0.
1	Prior to read sector operation, this read enable bit should be set to 1. It should stay high till the end of the read sector command.
2	Prior to write sector or write format, this write enable bit should be set to 1. It should stay high until the end of the write sector or write format command.
3	The buffer ready bit will be set to 1 after the host transfers a sector of data to/from the buffer during the write/read sector command.
4	Acknowleges IRQ14 signal. This bit is set to 1 when the host receives an IRQ signal with data request present (bit 3 of the status register). The host should then transfer a sector of data to/from the disk buffer.
5	This bit should be set to 1 and then reset to 0 to reset the buffer counter. This must occur prior to any operation relating to data transfer to/from the disk buffer.
6	Not used.
7	Fixed drive LED select: 0 = on 1 = off

Command Register

This write-only register is used to load the desired command. A command begins to execute immediately upon loading. This register should not be loaded while bit 1 or 7 is set in the status register.

The command set consists of six commands, as shown in Table 6-9. Prior to loading a command, the task file registers must be set with the proper parameters. Except for the command register, the task file registers can be loaded in any order.

Table 6-9
Command Register Format

Command	7	6	5	4	3	2	1	0
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read sector	0	0	1	0	I	M	0	T
Write sector	0	0	1	1	0	M	0	T
Scan ID	0	1	0	0	0	0	0	T
Write format	0	1	0	1	0	0	0	0

Note:
1. R0 through R3 is the rate field:

0	0	0	0 = approx. 35 microseconds
0	0	0	1 = 0.5 milliseconds
0	0	1	0 = 1.0 milliseconds
0	0	1	1 = 1.5 milliseconds
0	1	0	0 = 2.0 milliseconds
0	1	0	1 = 2.5 milliseconds
0	1	1	0 = 3.0 milliseconds
0	1	1	1 = 3.5 milliseconds

Table 6-9 (continued)
Command Register Format

R3	R2	R1	R0	
1	0	0	0	= 4.0 milliseconds
1	0	0	1	= 4.5 milliseconds
1	0	1	0	= 5.0 milliseconds
1	0	1	1	= 5.5 milliseconds
1	1	0	0	= 6.0 milliseconds
1	1	0	1	= 6.5 milliseconds
1	1	1	0	= 7.0 milliseconds
1	1	1	1	= 7.5 milliseconds

2. M is the multiple sector flag:
   0 = transfer 1 sector
   1 = transfer multiple sectors

3. T is the retry flag: 0 = retries enabled
   1 = retries disabled

4. I is the interrupt enable:

   0 = set interrupt when bit 3 of the status register is set (sector buffer is ready to be loaded or read)
   1 = set interrupt upon completion of command

RESTORE - Restore heads. The restore command is usually used on a power-up condition. The head is stepped back to track 000. If after 1024 stepping pulses, the head is not over track 000, bit 1 of the error flag is set. The stepping rate used is determined by the head settling time. The rate entered into the rate field of the restore command is stored in an internal register and used in future commands with implied seeks (the default stepping rate is 7.5 ms.)

SEEK - For seek operations between multiple drives. Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The rate field step rate is used and then stored in an internal register for future use.

The value is calculated by comparing the contents of the cylinder high/low registers to the cylinder position number stored internally. After all steps have been issued, the command is terminated.

READ SECTOR - Transfers one or more sectors to disk. The task file registers are loaded with the transfer parameters:

Sector count
Sector number
Cylinder high/low
SDH (Sector size, drive number, and head number)

The read sector command must be entered when bit 7 (busy) of the status register reaches a reset condition. When the WD1010-05 receives the read sector command, it checks cylinder registers against the actual cylinder position. The controller must then locate the cylinder and search for an ID field with the proper parameters.

After data is read to the buffer, the BDRQ signal is sent to the host indicating the buffer is ready to be emptied. An interrupt signal is sent to the host upon completion of the command. The host acknowledges the interrupt by strobing address 1F8 (IRQ14ACK) of the interrupt controller.

Multiple sector read transfers are loop operations where M (bit 2) in the read sector command is set to 1. The program decrements the sector count register and increments the sector number register. When the sector count reaches 0, the interrupt request is generated terminating the command.

If the error bit (bit 0 or the status register) is set during the operation, the error register can be read for specific error information.

WRITE SECTOR - Writes one or more sectors of information. The task file registers are loaded with the transfer parameters:

Write precomp cylinder
Sector count
Sector number
Cylinder high/low
SDH (sector size, drive number, head number)

The write sector command must be entered when bit 7 (busy) of the status register reaches a reset condition. When the WD1010-05 receives the write sector command, it checks cylinder registers against the actual cylinder position.
A BDRQ signal sent to the host indicates the

buffer is ready to be loaded. The WD1010-05 then scans the disk for proper ID location and writes data to the disk. An interrupt signal is sent to the host upon completion of the command. The host acknowledges the interrupt by strobing address 1F8 (IRQ14ACK) of the interrupt controller.

Error interrupts occur prior to host to buffer data transfer. If the error bit (bit 0 or the status register) is set during the operation, read the error register for information.

Multiple sector write transfers are loop operations where M (bit 2) in the write sector command is set to 1. The program decrements the sector count register and increments the sector number register. When the sector count reaches 0, the interrupt request is generated terminating the command.

SCAN ID - Updates the head, sector size, sector number, and cylinder registers. The internal cylinder position is also updated. This operation is used for multiple drives for an implied seek.

WRITE FORMAT - Used to format a single track using the task file and sector buffer. The sector buffer is used for additional parameter information instead of sector data. The task file registers are loaded with the parameters:

Write precomp cylinder: Desired precomp start track/4
Sector count: Number of sectors to be formatted.
Sector number: Number of bytes minus three to be used for Gap 1 and Gap 3.

Gap 3 = 2 * M * S + K + E

Where: M = motor speed variation (.03 for +-3%)
S = sector length in bytes
K = 25 for an interleave factor of 1 and 0 for any other interleave factor
E = 7 if the sector is to be extended

Cylinder high/low: Desired cylinder number
SDH: Sector size, drive number, and head number

The write format command must be entered when bit 7 (busy) of the status register reaches a reset condition. When the WD1010-05 receives the write format command, it checks cylinder registers against the actual cylinder position.

The interleave table in the sector buffer is filled. Each sector to be formatted requires a two-byte sequence. The first byte indicates whether a bad block mark is to be recorded in the sector's ID field. An 80H indicates a bad block mark for that sector; a 00H is normal. The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value (but must be filled with one sector size worth of data). Table 6-10 lists the interleaves.

Table 6-10
Interleaves (1 to 1)

00, 01, 00, 02, 00, 03, 00, 04, 05, 00, 06, 00, 07, 00, 08, 00, 09, 00, 0A, 00, 0B, 00, 0C, 00, 0D, 00, 0E, 00, 0F, 00, 10, 00, 11

The write format command will continue a loop operation until the sector count equals 0. An interrupt is then generated terminating the command.

Error interrupts are not generated using the write format command.

7 HARDWARE PROGRAMMING - HIGH-RESOLUTION GRAPHICS BOARD

Introduction

The high-resolution graphics board operates in an alphanumeric mode and bit-mapped graphics modes.

The alphanumeric (alpha) mode provides two resolutions. The low-resolution mode is a 40-column by 25-row display using an 8 x 16-dot high character box and 7 x 9 dot character font with two descenders. The high-resolution mode is an 80-column by 25-row display with an 8 x 16-dot high character box and 7 x 9 dot character font with two descenders. The alphanumeric modes support 256 different character codes (see Appendix C). An 8-kilobyte ROM character generator contains the two different fonts and a jumper option gives a single-dot font or double-dot font in a character size of 8 x 9 dot in any alphanumeric mode.

The monochrome mode provides reverse video, blinking, underlining and highlighting character attributes. The color mode has sixteen foreground and eight background colors for each character. Blinking on a per character basis is also available.

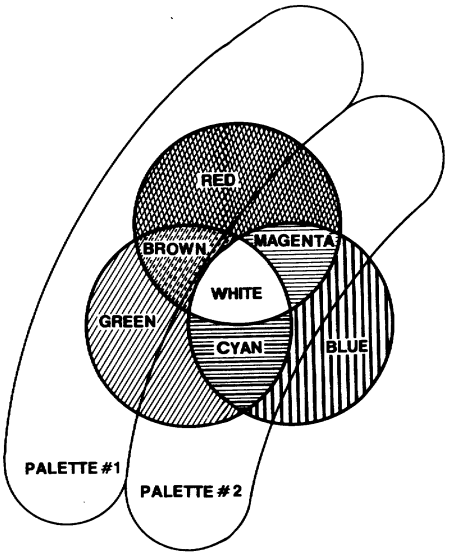
There are 32 kilobytes of dynamic memory used for the display buffer. In the alphanumeric modes, eight screen displays can be stored in the 40 x 25 mode and four screen displays can be stored in the 80 x 25 mode. The start of each display page begins at an even 2- or 4-kilobyte offset and is accessed by changing the offset in the start-address registers.

Two resolutions are provided in the bit-mapped IBM compatible graphics mode: a medium resolution monochrome or four-color graphics mode of 320 x 200 pixels and a high-resolution monochrome mode of 640 x 200 pixels.

An extendable non-IBM compatible graphics mode provides a medium-resolution monochrome or four-color graphics mode of 320 x 400 pixels and a high-resolution monochrome mode of 640 x 400 pixels.

Each pixel can have one of four colors in the medium-resolution mode. The background color can be one of sixteen colors, with one of two software-selectable palettes providing the three remaining colors. One palette contains red, green, and brown and the other palette contains cyan, magenta, and white, as shown in Figure 7-1. Since both graphics modes require 16 kilobytes of the buffer to define the screen display, the high resolution is available only in black-and-white.

Figure 7-1
Software-Selectable Palettes



CONTROLLER PROGRAMMING

There are eighteen internal registers in the CRT controller that define and control a raster-scan CRT display. The 5-bit, write-only Index register is used as a pointer to the other eighteen registers. This register is loaded from the CPU by executing an OUT instruction to I/O address 3B4h or 3D4h.

Any one of the 18 controller registers can be loaded by loading the Index register with the necessary pointer (0-17 decimal) and then loading the Data register with the desired value using an OUT instruction to 3B5h or 3D5h. Table 7-1 lists the values that are loaded into the CRT controller registers for controlling the various operational modes.

Table 7-1
CRT Controller Registers

Reg. No.	Register	I/O	40x25 Alpha Hex	80x25 Alpha Hex	Graphics Mode Hex
R0	Horizontal Total	WO	38	71	38
R1	Horizontal Displayed	WO	28	50	28
R2	Horizontal Sync Position	WO	2D	5A	2D
R3	Horizontal Sync Width	WO	0A	0A	0A
R4	Vertical Total	WO	1F	1F	7F
R5	Vertical Total Adjust	WO	06	06	06
R6	Vertical Displayed	WO	19	19	64
R7	Vertical Sync Position	WO	1C	1C	70
R8	Mode Control	WO	02	02	02
R9	Max. Scan Line Address	WO	07	07	01
R10	Cursor Start	WO	6	6	6
R11	Cursor End	WO	07	07	0
R12	Start Address MSB	WO	0(Pg 0)	0(Pg 0)	0
R13	Start Address LSB	WO	0(Pg 0)	0(Pg 0)	0
R14	Cursor Address MSB	WO			
R15	Cursor Address LSB	WO			
R16	Light Pen Address MSB	Not Used			
R17	Light Pen Address LSB	Not Used			

Table 7-1 (continued)
CRT Controller Registers

NOTE: Addresses in start-address and cursor-address registers are offset into graphics memory. The CRT controller views these values as offsets into the character positions, ignoring attribute bytes; therefore, the offsets are 1/2 the offset value as viewed by the CPU.

MODE-SELECT REGISTER

The 6-bit, write-only, mode-select register is located at 3B8h or 3D8h and is used to select the video mode. Table 7-2 lists the bit assignments for the mode-select register and Table 7-3 summarizes this register.

Table 7-2
Mode-Select Register

Bit	State	Function
0	0	40 x 25 alphanumeric/graphics mode (low resolution)
	1	80 x 25 alphanumeric mode (high resolution)
1	0	Selects alphanumeric mode
	1	Selects graphics mode
2	0	Selects color mode
	1	Selects black-and-white mode
3	1	Enables the video signal at certain times when modes are being changed (the video signal should be disabled when changing modes)
4	1	Selects 640 x 200, high-resolution, black-and-white graphics mode
5	1	Enables blinking attribute in alphanumeric modes

Table 7-3
Mode-Select Register Summary

Bits 5	4	3	2	1	0	Mode Selected
1	0	1	1	0	0	40 x 25 alphanumeric black-and-white
1	0	1	0	0	0	40 x 25 alphanumeric color
1	0	1	1	0	1	80 x 25 alphanumeric black-and-white
1	0	1	0	0	1	80 x 25 alphanumeric color
x	0	1	1	1	0	320 x 200 black-and-white graphics
x	0	1	0	1	0	320 x 200 color graphics
x	1	1	1	1	0	640 x 200 or 640 x 400 black-and-white graphics

COLOR-SELECT REGISTER

The 6-bit, write-only, color-select register, located at 3B9h or 3D9h controls the foreground color when in the 640 x 200 or 640 x 400 graphics mode. This register also controls background color when in the 320 x 200 graphics mode. Table 7-4 lists the bit assignments for the color-select register.

Table 7-4
Color-Select Register

Bit	Function	MODE 320x200 Graphic	640x200 Graphic
0	Set blue	Background	Foreground
1	Set green	Background	Foreground
2	Set red	Background	Foreground
3	Set intensity	Background	Foreground
4	Set background intensity	Intensified Set	
5	Palette select	0 - red, green, brown 1 - cyan, magenta, white	
6	Not used		
7	640 X 400 pixel mode select:	0 - modes except 640 X 400 1 - 640 X 400 monochrome	

When bit 5 is set to 0, colors are determined as follows by the outputs C1 and C0 of shift registers U7 and U18:

C1	C0	Set Selected
0	0	Background, determined by bits 0-3
0	1	Green
1	0	Red
1	1	Brown

When bit 5 is set to 1, colors are determined as follows:

C1	C0	Set Selected
0	0	Background, determined by bits 0-3
0	1	Cyan
1	0	Magenta
1	1	White

STATUS REGISTER

Bits 0 - 6 of this read-only status register are located at 3BAh or 3DAh. Bit 7 is located at hex address 3DF. Table 7-5 lists the status register bit assignments.

Table 7-5
Status Register

Bit	Function	Description
0	Display enable	A 1 indicates an active display cycle.
1-2	Not used	
3	Vertical sync	When active, indicates that the raster is in a vertical retrace mode.
4-6	Not used	
7	Card present	0 indicates that the TeleVideo High-Resolution Graphic Board (HGB) is present. This bit is not read by IBM-compatible software and is relevant only to software using the 640 X 400 pixel display mode.

ALPHANUMERIC MODE

The alphanumeric mode supports 256 character codes (refer to Appendix D). Each display character is defined by two bytes in the display buffer memory. An even-addressed byte contains the character code, and the following odd-addressed byte contains the corresponding character attribute. Table 7-6 lists the bit assignments for the character attribute byte.

Table 7-6
Character Attribute Byte

	Attribute Byte									
	7	6	5	4	3	2	1	0	Background	Foreground
Function	Blk	R	G	B	I	R	G	B	Color	Color
Normal	BL	0	0	0	In	1	1	1	Black	White
Reverse Video	BL	1	1	1	In	0	0	0	White	Black
Blank (Black)	BL	0	0	0	In	0	0	0	Black	Black
Blank (White)	BL	1	1	1	In	1	1	1	White	White
Underline	BL	0	0	0	In	0	0	1	(mode register black and white set)	

NOTE: R = Red BL = 1: Blinking, 0: steady
G = Green In = Intensity (foreground)
B = Blue In = 1: Intensity set, 0: normal

Bits 0-3 indicate the foreground color and bits 4-6 indicate the background color. The standard display produces white characters on a black background with all other foreground/background code combinations. A color monitor produces the foreground or background colors listed in Table 7-7. The background intensity is set in bit 4 of the color-select register.

Table 7-7
Color Codes

R	G	B	I	Color
0	0	0	0	Black
0	0	1	0	Blue
0	1	0	0	Green
0	1	1	0	Cyan
1	0	0	0	Red
1	0	1	0	Magenta
1	1	0	0	Brown
1	1	1	0	White
0	0	0	1	Gray
0	0	1	1	Light Blue
0	1	0	1	Light Green
0	1	1	1	Light Cyan
1	0	0	1	Light Red
1	0	1	1	Light Magenta
1	1	0	1	Yellow
1	1	1	1	White (High Intensity)

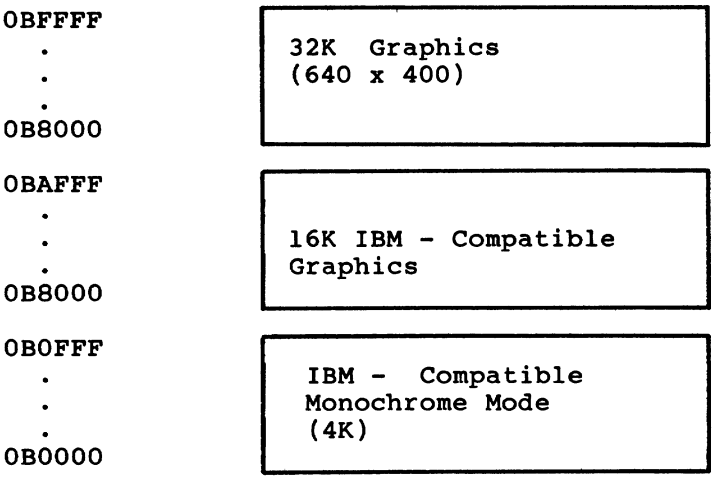
NOTE: Not all RGB monitors recognize the intensity bit.

GRAPHICS MODE

There are two graphics modes: a 320 x 200 pixels, medium-resolution, color graphics mode and a 640 x 200 pixels, high-resolution, black-and-white mode. Both modes use memory-mapped graphics and require 16 kilobytes to define the screen.

The graphics information for the screen display is stored in two 16-kilobyte banks, as shown in Figure 7-2.

Figure 7-2
Graphics Memory Addresses



In the medium-resolution mode, each byte contains information for four pixels, as shown in Table 7-8.

Table 7-8
Medium-Resolution Byte Usage

7	6	5	4	3	2	1	0
C1	C0	C1	C0	C1	C0	C1	C0
First display pixel		Second display pixel		Third display pixel		Fourth display pixel	

Each pixel can have one of four colors, while the background color can be one of 16 colors. One of two software-selectable palettes provides the remaining three colors. These are selected by bit 5 of the color-select register. Table 7-9 shows the color selection logic.

Table 7-9
Medium-Resolution Color Selection Logic

C1	C0	Color
0	0	1 of 16 preselected background colors
0	1	If palette 1 Green If palette 2 Cyan
1	0	Red Magenta
1	1	Brown White

In the high-resolution, black-and-white mode, each bit of a display byte contains the state of one display pixel. Bit 7 corresponds to the first display pixel and bit 0 corresponds to the eighth display pixel.

8 INTERFACE

Introduction

This chapter describes the internal connector interfaces and external connector ports. These ports provide the means to expand or perform major internal functions while allowing external system expansion. The chapter is divided into internal and external interfaces.

Internally, there are six 16-bit expansion slots on the motherboard. The configuration of each 16-bit slot is the same. There are two 8-bit expansion slots. Each 8-bit slot has the same configuration.

Connectors for the motherboard, the system battery, the diskette/fixed disk controller board and power connectors for the disk drives are among the internal connections for the AT.

Externally, there are serial, parallel, keyboard and graphics board interface connections.

INTERNAL INTERFACES

Table 8-1
Power Supply (P1)

PIN	SIGNAL	DESCRIPTION
1	115/230V	115/230V line voltage
2	---	No connection
3	NEUT	Neutral
4	---	No connection
5	GND	Main ground

Table 8-2
Power Supply (P2A)

PIN	SIGNAL	DESCRIPTION
1-6	GND	Ground (+5V return)
7	---	No connection
8	GND	Main ground

Table 8-3
Power Supply (P2B)

1	GND	Ground (+5V return)
2	+12V	+12 volts supply (7.5 amps)

Table 8-4
Power Supply (P2C)

PIN	SIGNAL	DESCRIPTION
1-2	+12V	+12 Volt supply (7.5 Amp)

Table 8-5
Power Supply (P3)

PIN	SIGNAL	DESCRIPTION
1-5	+5V	+5 volts supply (20 Amps)
6-9	GND	Ground (+12V return)
10	---	No connection
11-12	+12V	+12 volts supply (7.5 amps)

Table 8-6
Power Supply (P4)

PIN	SIGNAL	DESCRIPTION
1	PWR Good	Power good
2	---	No connection
3	+12V	+12 volts supply (2 amps)
4	---	No connection
5	GND	Ground (+12V return)
6	-5V	-5 volts supply (0.3 amps)
7	-12V	-12 volts supply (0.3 amps)
8	---	No connection
9	GND	Ground (-5V, -12V return)
10-12	+5V	+5 volts supply (20 amps)

Table 8-7
Power Supply - Diskette/Fixed Disk Drives (DR1-DR4)

PIN	SIGNAL	DESCRIPTION
1	+12V	+12 volts supply (7.5 amps)
2	GND	Ground (+12V return)
3	GND	Ground (+5V return)
4	+5V	+5 volts supply (20 amps)

Table 8-8
Battery (J23 - motherboard)

PIN	SIGNAL	DESCRIPTION
1(edge)	GND	Ground
2(center)	+6V	+6 volts (battery)
3(edge)	GND	Ground

Table 8-9
Power Supply (P1A - motherboard)

PIN	SIGNAL	DESCRIPTION
1	-12V	-12 volts (0.3 amps)
2	---	No connection
3	GND	Ground (+12V return)
4	+5V	+5 volts (20 amps)
5	+12V	+12 volts (2 amps)

Table 8-10
Power Supply (P1B - motherboard)

PIN	SIGNAL	DESCRIPTION
1-3	GND	Ground
4-6	+5V	+5 volts
7	---	No connection
8	-5V	-5 volts
9	PWR good	Power good

Table 8-11
Speaker (J22 - motherboard)

PIN	SIGNAL	DESCRIPTION
1	Speaker out	Speaker out
2	Speaker ret	Speaker return

Table 8-12
8-Bit Expansion Board Slot (62-pin connector)

PIN	SIGNAL	DESCRIPTION
A1	I/O CH CK	I/O channel check
A2	SD7	Data bit 7
A3	SD6	Data bit 6
A4	SD5	Data bit 5
A5	SD4	Data bit 4
A6	SD3	Data bit 3
A7	SD2	Data bit 2
A8	SD1	Data bit 1
A9	SD0	Data bit 0
A10	-I/OCH RDY	I/O channel ready
A11	AEN	Address enable
A12	SA19	Address bit 19
A13	SA18	Address bit 18
A14	SA17	Address bit 17
A15	SA16	Address bit 16
A16	SA15	Address bit 15
A17	SA14	Address bit 14
A18	SA13	Address bit 13
A19	SA12	Address bit 12
A20	SA11	Address bit 11
A21	SA10	Address bit 10
A22	SA9	Address bit 9
A23	SA8	Address bit 8
A24	SA7	Address bit 7
A25	SA6	Address bit 6
A26	SA5	Address bit 5
A27	SA4	Address bit 4
A28	SA3	Address bit 3
A29	SA2	Address bit 2
A30	SA1	Address bit 1
A31	SA0	Address bit 0
B1	GND	Ground
B2	RESET	Reset
B3	+5V	+5 volts
B4	IRQ9	Interrupt request 9
B5	-5V	-5 volts
B6	DRQ2	Data request 2
B7	-12V	-12 volts
B8	-OWS	Zero wait states
B9	+12V	+12 volts
B10	GND	Ground
B11	-SMEMW	System memory write
B12	-SMEMR	System memory read
B13	-IOW	I/O write
B14	-IOR	I/O read

Table 8-12 (continued)
8-Bit Expansion Board Slot (62-pin connector)

PIN	SIGNAL	DESCRIPTION
B15	-DACK3	Data acknowledge 3
B16	DRQ3	Data request 3
B17	-DACK1	Data acknowledge 1
B18	DRQ1	Data request 1
B19	-REFRES	Refresh memory
B20	SYSCLK	System clock
B21	IRQ7	Interrupt request 7
B22	IRQ6	Interrupt request 6
B23	IRQ5	Interrupt request 5
B24	IRQ4	Interrupt request 4
B25	IRQ3	Interrupt request 3
B26	-DACK2	Data acknowledge 2
B27	T/C	Terminate count
B28	ALE	Address latch enable
B29	+5V	+5 volts
B30	OSC(14.318 MHz)	Oscillator
B31	GND	Ground

Table 8-13
16-Bit Expansion Board Slot

PIN	SIGNAL	DESCRIPTION
A1	I/O CH CK	I/O channel check
A2	SD7	Data bit 7
A3	SD6	Data bit 6
A4	SD5	Data bit 5
A5	SD4	Data bit 4
A6	SD3	Data bit 3
A7	SD2	Data bit 2
A8	SD1	Data bit 1
A9	SD0	Data bit 0
A10	-I/OCH RDY	I/O channel ready
A11	AEN	Address enable
A12	SA19	Address bit 19
A13	SA18	Address bit 18
A14	SA17	Address bit 17
A15	SA16	Address bit 16
A16	SA15	Address bit 15
A17	SA14	Address bit 14
A18	SA13	Address bit 13
A19	SA12	Address bit 12
A20	SA11	Address bit 11
A21	SA10	Address bit 10
A22	SA9	Address bit 9

Table 8-13 (continued)
16-Bit Expansion Board Slot

PIN	SIGNAL	DESCRIPTION
A23	SA8	Address bit 8
A24	SA7	Address bit 7
A25	SA6	Address bit 6
A26	SA5	Address bit 5
A27	SA4	Address bit 4
A28	SA3	Address bit 3
A29	SA2	Address bit 2
A30	SA1	Address bit 1
A31	SA0	Address bit 0
B1	GND	Ground
B2	RESET DR	Reset drive
B3	+5V	+5 volts
B4	IRQ9	Interrupt request 9
B5	-5V	-5 volts
B6	DRQ2	Data request 2
B7	-12V	-12 volts
B8	-OWS	Zero wait states
B9	+12V	+12 volts
B10	GND	Ground
B11	-SMEMW	System memory write
B12	-SMEMR	System memory read
B13	-IOW	I/O write
B14	-IOR	I/O read
B15	-DACK3	Data acknowledge 3
B16	DRQ3	Data request 3
B17	-DACK1	Data acknowledge 1
B18	DRQ1	Data request 1
B19	-REFRES	Refresh memory
B20	SYSCLK	System clock
B21	IRQ7	Interrupt request 7
B22	IRQ6	Interrupt request 6
B23	IRQ5	Interrupt request 5
B24	IRQ4	Interrupt request 4
B25	IRQ3	Interrupt request 3
B26	-DACK2	Data acknowledge 2
B27	T/C	Terminate count
B28	ALE	Address latch enable
B29	+5V	+5 volts
B30	OSC(14.318 MHz)	Oscillator
B31	GND	Ground
C1	-SBHE	System byte high enable
C2	A23	Address bit 23
C3	A22	Address bit 22
C4	A21	Address bit 21

Table 8-13 (continued)
16-Bit Expansion Board Slot

PIN	SIGNAL	DESCRIPTION
C5	A20	Address bit 20
C6	A19	Address bit 19
C7	A18	Address bit 18
C8	A17	Address bit 17
C9	-MEMR	Memory read
C10	-MEMW	Memory write
C11	SD8	Data bit 8
C12	SD9	Data bit 9
C13	SD10	Data bit 10
C14	SD11	Data bit 11
C15	SD12	Data bit 12
C16	SD13	Data bit 13
C17	SD14	Data bit 14
C18	SD15	Data bit 15
D1	-MEM CS 16	Memory chip select 16
D2	-I/O CS 16	I/O chip select 16
D3	IRQ10	Interrupt request 10
D4	IRQ11	Interrupt request 11
D5	IRQ12	Interrupt request 12
D6	IRQ15	Interrupt request 15
D7	IRQ14	Interrupt request 14
D8	-DACK0	Data acknowledge 0
D9	DRQ0	Data request 0
D10	-DACK5	Data acknowledge 5
D11	DRQ5	Data request 5
D12	-DACK6	Data acknowledge 6
D13	DRQ6	Data request 6
D14	-DACK7	Data acknowledge 7
D15	DRQ7	Data request 7
D16	+5V	+5 volts
D17	-MASTER	Master
D18	GND	Ground

Table 8-14
Diskette/Fixed Disk Controller Board -
Diskette Bus Connector (J1)

PIN	SIGNAL	DESCRIPTION
1-33(odd)	GND	Ground
2	-RWC	Reduced write
4	RESERVED	Reserved
6	RESERVED	Reserved
8	-FIDX	Index

Table 8-14 (continued)
Diskette/Fixed Disk Controller Board -
Diskette Bus Connector (J1)

PIN	SIGNAL	DESCRIPTION
10	-MON	Drive select 0
12	-DS2	Drive select 1
14	-DS1	Drive select 2
16	-MON2	Motor on
18	-FDIR	Direction select
20	-FSTEP	Step
22	-FWD	Write data
24	-FWE	Write gate
26	-FTK0	Track 00
28	-FWPT	Write protect
30	-DISKD	Read data
32	-FHS1	Side 1 select
34	-DCHG	Diskette change

Table 8-15
Diskette/Fixed Disk Controller Board -
Fixed Disk Control Signal Connector (J5)

PIN	SIGNAL	DESCRIPTION
1-33(odd)	GND	Ground
2	-HHS3/-RWC	Reduced write current/ Head select 3
4	-HHS2	Head select 2
6	-WG	Write gate
8	-HSK COMPLT	Seek complete
10	-HTK0	Track 000
12	-HWT FAULT	Write fault
14	-HHS0	Head select 0
16	RESERVED	Reserved
18	-HHS1	Head select 1
20	-HINDEX	Index
22	-HREADY	Ready
24	-HSTEP	Step
26	-HDS0	Drive select 1
28	-HDS1	Drive select 2
30	RESERVED	Reserved
32	RESERVED	Reserved
34	-HDIR	Direction in

Table 8-16 Diskette/Fixed Disk Controller Board - Fixed Disk Data Signal Connectors (J3 and J4)

PIN	SIGNAL	DESCRIPTION
2, 4, 6, 11, 12, 15, 16, 19, 20	GND	Ground
13	WD	Write data
14	WD	Write data
17	RD	Read data
18	RD	Read data

All other pins are unused.

EXTERNAL INTERFACES

Table 8-17
Parallel Printer Port (J17)

PIN	SIGNAL	DESCRIPTION
1	-STROBE	Data strobe to printer
2	DATA 0	Data bus bit 0
3	DATA 1	Data bus bit 1
4	DATA 2	Data bus bit 2
5	DATA 3	Data bus bit 3
6	DATA 4	Data bus bit 4
7	DATA 5	Data bus bit 5
8	DATA 6	Data bus bit 6
9	DATA 7	Data bus bit 7
10	-ACK	Printer ready to receive data
11	BUSY	Printer busy
12	PE	Paper empty
13	SELECT	Printer selected
14	-AUTO FD XT	Automatic feed
15	-ERROR	Error state
16	-INIT	Reset printer
17	-SLCT IN	Select to printer
18-25	GND	Ground

Table 8-18
Serial Communications Port (J-18)

PIN	SIGNAL	DESCRIPTION
1	CDC	Carrier detect
2	RXD	Receive data
3	TXD	Transmit data
4	DTR	Data terminal ready
5	GND	Ground
6	DSR	Data set ready
7	RTS	Request to send
8	CTS	Clear to send
9	RI	Ring indicator

Table 8-19
Keyboard Connector

PIN	SIGNAL	DESCRIPTION
1	KBD CLK	Keyboard clock
2	KBD DATA	Keyboard data
3	---	No connection
4	GND	Ground
5	+5V	+5 volts

Table 8-20
High-Resolution Graphics Board

PIN	SIGNAL	DESCRIPTION
1-2	GND	Ground
3	ER	Red
4	EG	Green
5	EB	Blue
6	EI	Intensity
7	+12V	+12 volts
8	HSYNC	Horizontal sync
9	VSYNC	Vertical sync

APPENDIX A SPECIFICATIONS

MICROPROCESSOR/MEMORY

CPU	Intel 80286 16-bit microprocessor (processor speed 6 or 8 MHz) socketed for Intel 80287 numeric coprocessor (jumper-selectable coprocessor speed: 4 MHz, 4.77 MHz, and 5.3 MHz)
MEMORY	Model I: 256-Kbytes dynamic RAM Model II: 512-Kbytes dynamic RAM The AT is expandable to 15 Mbytes of memory with expansion cards 32-Kbytes EPROM with bootstrap loader and hardware diagnostics routines Motherboard RAM: 36 - 64K x 1 for 256 Kbytes 18 - 256K x 1 for 512 Kbytes 18 - 64K x 1 plus 18 - 256K x 1 for 640 Kbytes. ROM: 2 - 16K x 8 EPROM for 32 Kbytes 4 - 32K x 8 EPROM for 128 Kbytes Expansion Memory: 64K x 1 to 15 Mbytes, or 256K x 1 to 15 Mbytes

HIGH CAPACITY DISKETTE DRIVE

TYPE	5 1/4-inch diskette
DISKETTES	5 1/4-inch, double-sided, high-density, soft-sectored, 96- or 48-tpi diskettes
STORAGE CAPACITY (formatted)	1.2 Mbyte at 96 tpi
TRANSFER RATE	500 Kbits/second at 96 tpi 300 Kbits/second at 48 tpi
ACCESS TIME	94 milliseconds average 18 milliseconds track to track
ROTATION SPEED	360 rpm

FIXED DISK DRIVE

TYPE	One full-height, 5 1/4-inch Winchester hard disk
STORAGE CAPACITY	40 Mbytes formatted 53 Mbytes unformatted
TRANSFER RATE	5 Mbits per second
ACCESS TIME	8 milliseconds, track to track 55 milliseconds, average
VENDOR	Rodime (other sources may be used)

INPUT/OUTPUT

SERIAL I/O	RS-232C asynchronous 9-pin serial port; configured as DTE. Eight baud rates (110, 150, 300, 600, 1200, 2400, 4800, 9600)
PARALLEL I/O	Parallel (Centronics-type) printer port (DB-25S connector)

EXPANSION SLOTS	Six PC AT-compatible, 16-bit slots, two PC-compatible 8-bit slots

POWER REQUIREMENTS

U.S.	115 Vac (+/- 10%) 50/60 Hz
INTERNATIONAL	115/230 Vac (+/- 10%) 50/60 Hz
POWER CONSUMPTION	2.5 amp maximum at 115 Vac 1.25 amp maximum at 230 Vac 220 watts

DC POWER

Voltage	Current	Power Output
+5V	20A	100W
+12V	9.5A	114W
-12V	0.3A	3.6W
-5V	0.3A	1.5W

POWER CORD	NEMA standard 5-15R, 3-prong receptacle (United States only)

ENCLOSURES

COMPUTER DIMENSIONS	Height: 6 1/4 inches Width: 20 3/4 inches Depth: 16 1/2 inches
COMPUTER COMPOSITION	Top, bottom: Sheet steel Bezel: ABS plastic
KEYBOARD DIMENSIONS	Height: 1 1/2 inches Width: 18 1/4 inches Depth: 8 1/2 inches
KEYBOARD COMPOSITION	Top, bottom: ABS plastic

ENVIRONMENT

OPERATING	50 to 85 degrees Fahrenheit 10 to 30 degrees Celsius Maximum humidity 95 percent relative, noncondensing Maximum altitude 10,000 ft. above sea level
NONOPERATING (SHIPPING)	32 to 120 degrees Fahrenheit 0 to 50 degrees Celsius

OPTIONAL HARD DISK UPGRADE

TYPE	One half-height 5 1/4-inch Winchester hard disk
STORAGE CAPACITY	20 Mbytes formatted 24 Mbytes unformatted
TRANSFER RATE	5 Mbits per second
ACCESS TIME	15 milliseconds, track to track 85 milliseconds, average
VENDOR	Miniscribe (other sources may be used).

OPTIONAL 360-KBYTES DISKETTE DRIVE

TYPE	5 1/4-inch diskette
DISKETTES	5 1/4-inch, double-sided, high-density, soft-sectored, 48-tpi diskettes
STORAGE CAPACITY (formatted)	360 Kbytes
TRANSFER RATE	250 Kbits/second
ACCESS TIME	95 milliseconds, average 20 milliseconds, track to track
ROTATION SPEED	300 rpm
VENDOR	Toshiba (other sources may be used)

OPTIONAL GRAPHICS CARD AND MONITOR

MONITOR	14-inch, tilt-and-swivel, green screen
GRAPHIC RESOLUTION	IBM PC-compatible graphics mode - 640 x 200 monochrome - 320 x 200 4-color graphics - 320 x 200 monochrome Extendable graphics mode - 640 x 400 monochrome - 320 x 400 four colors

TEXT	Alphanumeric mode
	- 80 x 25 screen (or 40 x 25)
	- 256-character set
	  - 15 special characters for game support
	  - 16 for word processing support
	  - 96 for the standard ASCII code set
	  - 48 for the foreign language support
	  - 48 for the business block graphics
	  - 16 for selected Greek characters
	  - 15 for selected scientific notations
	- 8 x 16 dot matrix (7 x 9 font size with two descenders)
	- Hidden attributes (intensity, blinking, reverse, blank, underline)
	- 16 colors on RGB color monitor
	- 16 different gray scales for monochrome monitor

MEMORY	32 Kbytes of RAM

APPENDIX B - MOTHERBOARD DIP SWITCH SETTINGS (SW1)

The DIP switch settings are defined as follows:

Switch Number	Switch Position	Function
1	ON	6-MHz operation (CPU)
	OFF	8-MHz operation (CPU)
2	ON	Primary display attached to color/ graphics display card
	OFF	Primary display attached to monochrome card
	Settings for 256K motherboard RAM	
3	OFF	
4	ON	
5	ON	
	Settings for 512K motherboard RAM	
3	ON	
4	OFF	
5	ON	
	Settings for 640K motherboard RAM	
3	ON	
4	ON	
5	OFF	
6 - 8	Not used	

NOTE: ON = CLOSED
OFF = OPEN

APPENDIX C JUMPER CONFIGURATIONS

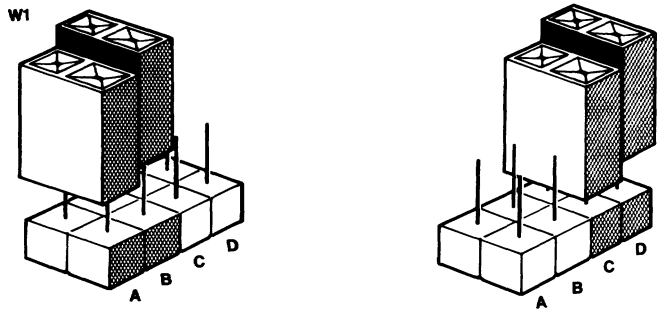
This appendix lists the jumper default configurations and describes the function of each jumper for the motherboard and the Diskette/Fixed Disk Controller board. The jumper configurations provide flexibility in operation and are set up in a basic (default) configuration.

MOTHERBOARD JUMPER CONFIGURATIONS

Serial Communications Port

Your AT system is shipped with the primary serial port set to the default configuration. If you add an additional serial port, refer to the installation instructions provided with that device before making the serial port 2 jumper connection. See Figure C-1.

Figure C-1
Serial Port Jumper (W1)



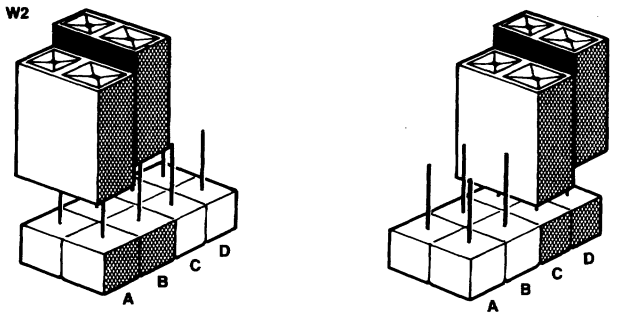
Serial Port 1 (default)

Serial Port 2

Parallel Communications Port

Your AT system is shipped with the primary parallel port set to the default configuration. If you add an additional parallel port, refer to the installation instructions provided with that device before making the port 2 jumper connection. Refer to Figure C-2.

Figure C-2
Parallel Printer Port (W2)



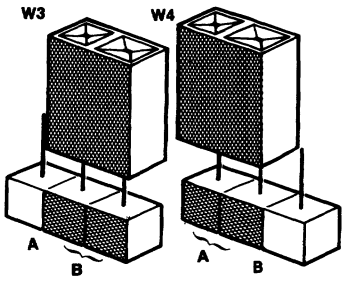
Parallel Port 1 (Default)

Parallel Port 2

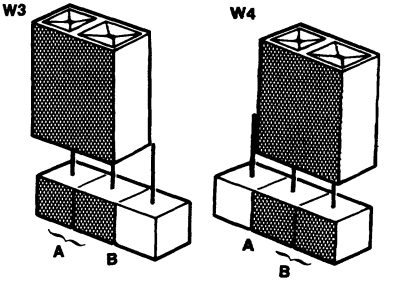
EPROM

Your AT system is provided with a standard 32 Kbytes of EPROM. EPROM size is expandable to 128 Kbytes. See Figure C-3.

Figure C-3
EPROM Jumper Configuration (W3 and W4)



Using 27128 EPROM
(16K X 8 - default)



Using 27256 EPROM
(32K X 8)

80287 Coprocessor

The AT system has a selectable CPU execution speed of 6 or 8 MHz. With jumper W9 in the default configuration, the selected execution speed of the CPU dictates the coprocessor speed. Selecting the 4.77 MHz configuration will cause the coprocessor to run at 4.77 MHz regardless of the CPU execution speed. See Figure C-4.

Figure C-4
Coprocessor Jumper (W9)

CPU speed 6 MHz
Coprocessor speed 4 MHz

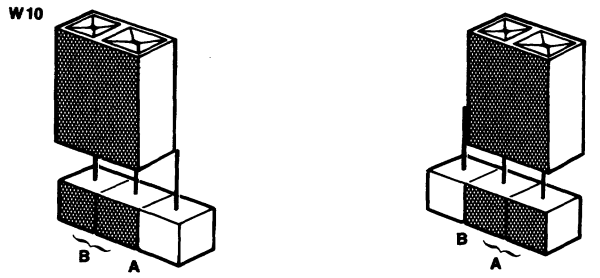
CPU speed 8 MHz
Coprocessor speed 5.33 MHz
(default)

Coprocessor speed
4.77 MHz

Custom Coprocessing

The default configuration of jumper W10 is set for any coprocessing speed as directed by jumper W9. The custom coprocessing configuration must be set for any coprocessing speed other than the default values. See Figure C-5.

Figure C-5
Custom Coprocessing Speed Jumper (W10)



Coprocessing Speed: 4, 4.77 or 5.33 MHz (default)

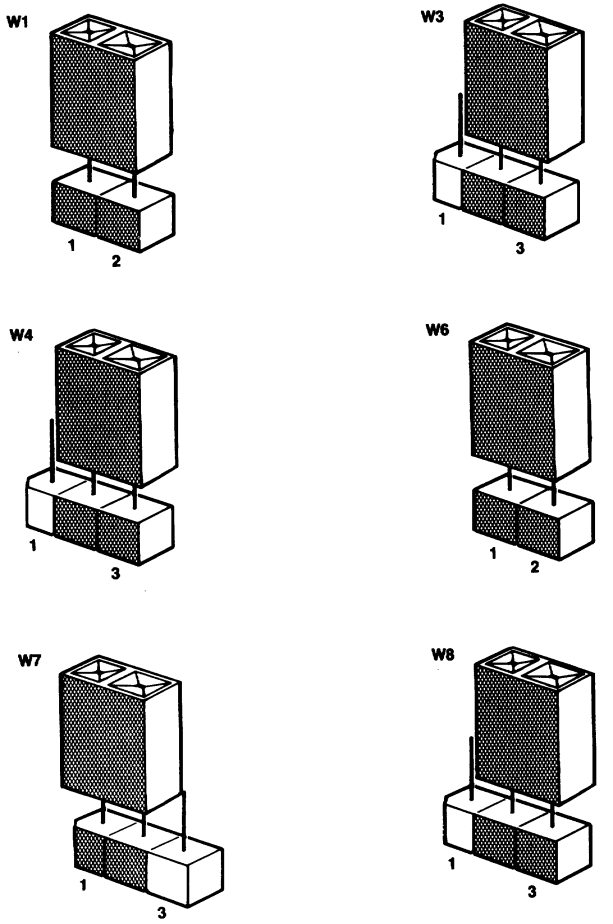
Custom Coprocessing Speed: Clock input supplied by the user.

Note: Jumpers W5, W7 and W8 on the motherboard are not used.

DISKETTE/FIXED DISK CONTROLLER BOARD JUMPER CONFIGURATIONS

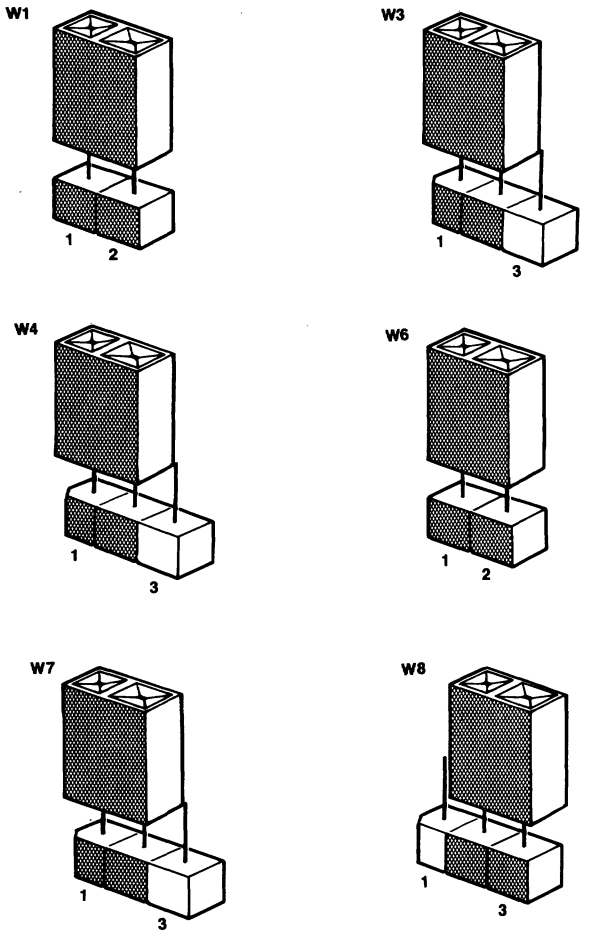
The jumper configuration illustrated in Figure C-6 is set when one controller board is provided in the system (default). The jumper configuration illustrated in Figure C-7 must be set when using two disk controller boards in the system.

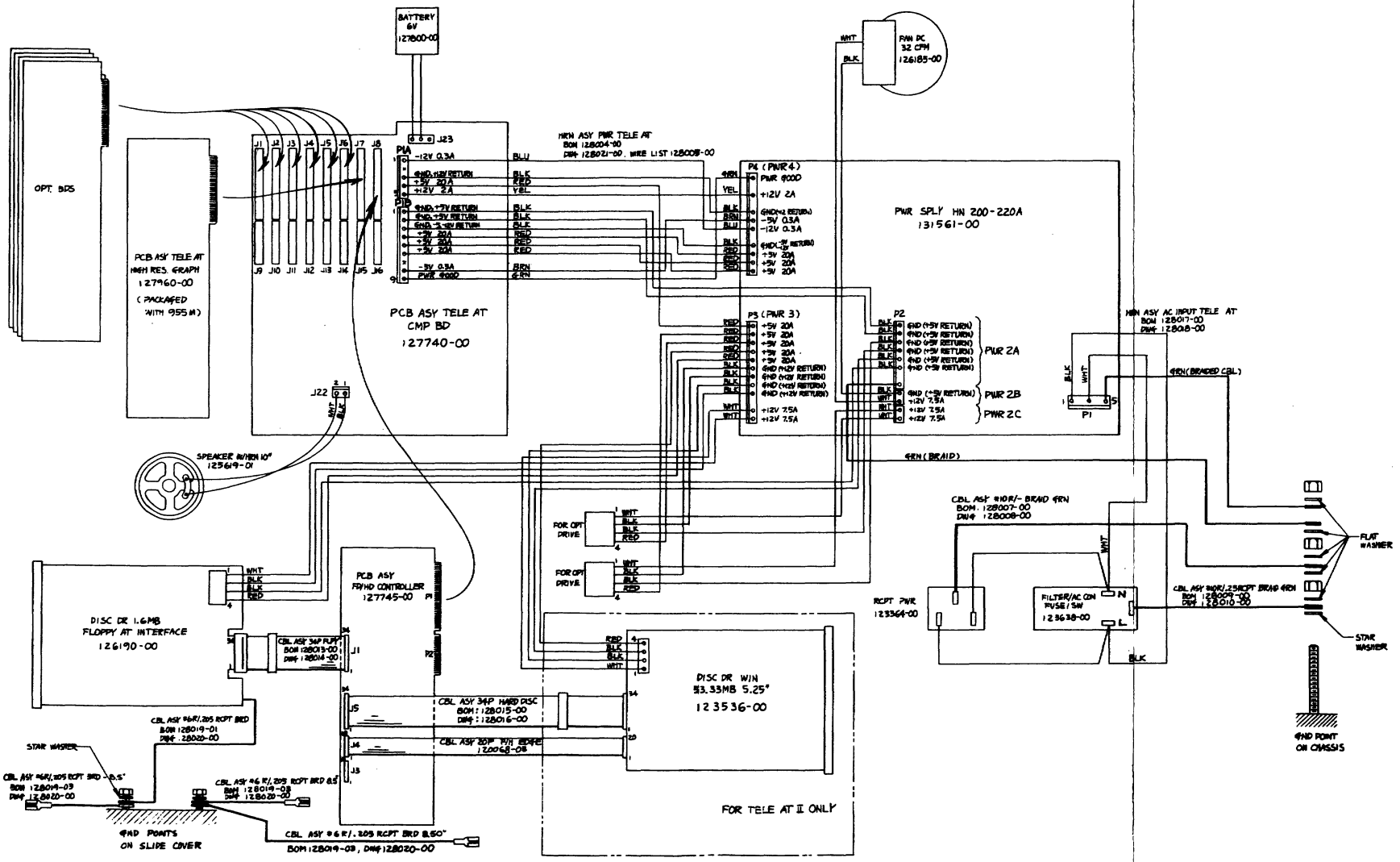
Figure C-6
Diskette/Fixed Disk Controller Board



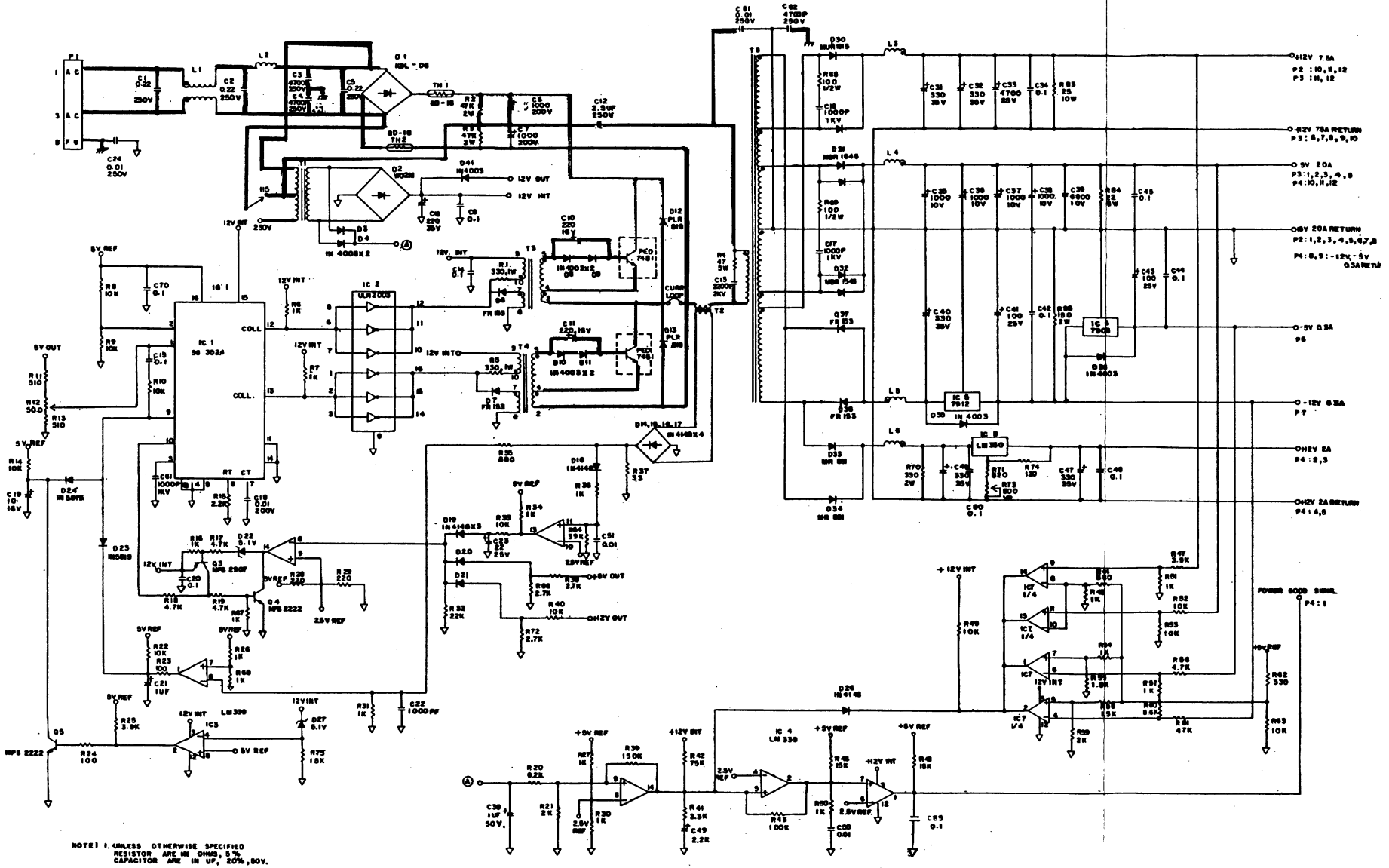
Default jumper configuration (primary address)

Figure C-7
Secondary Disk Controller Board
Jumper Configuration

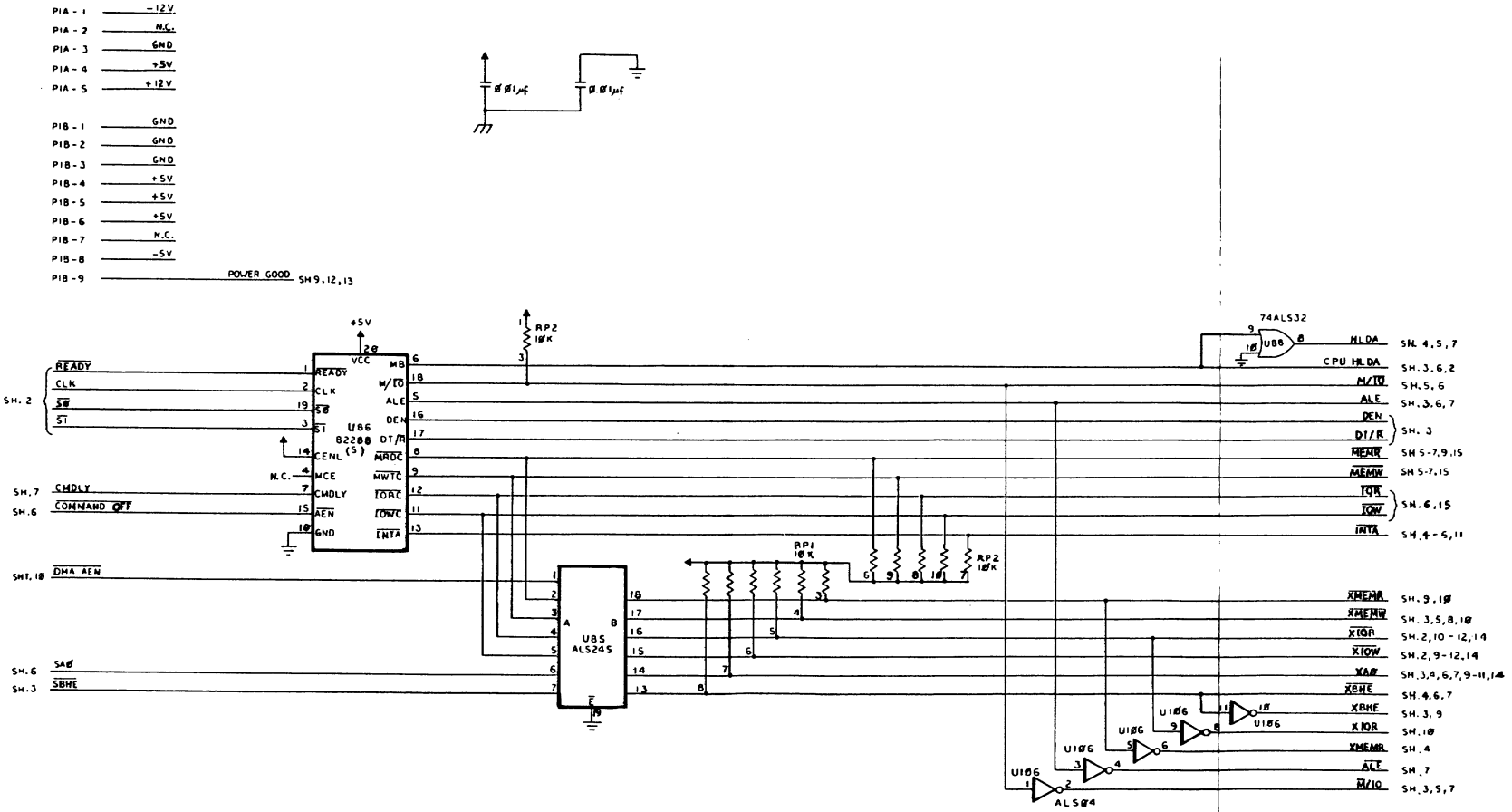




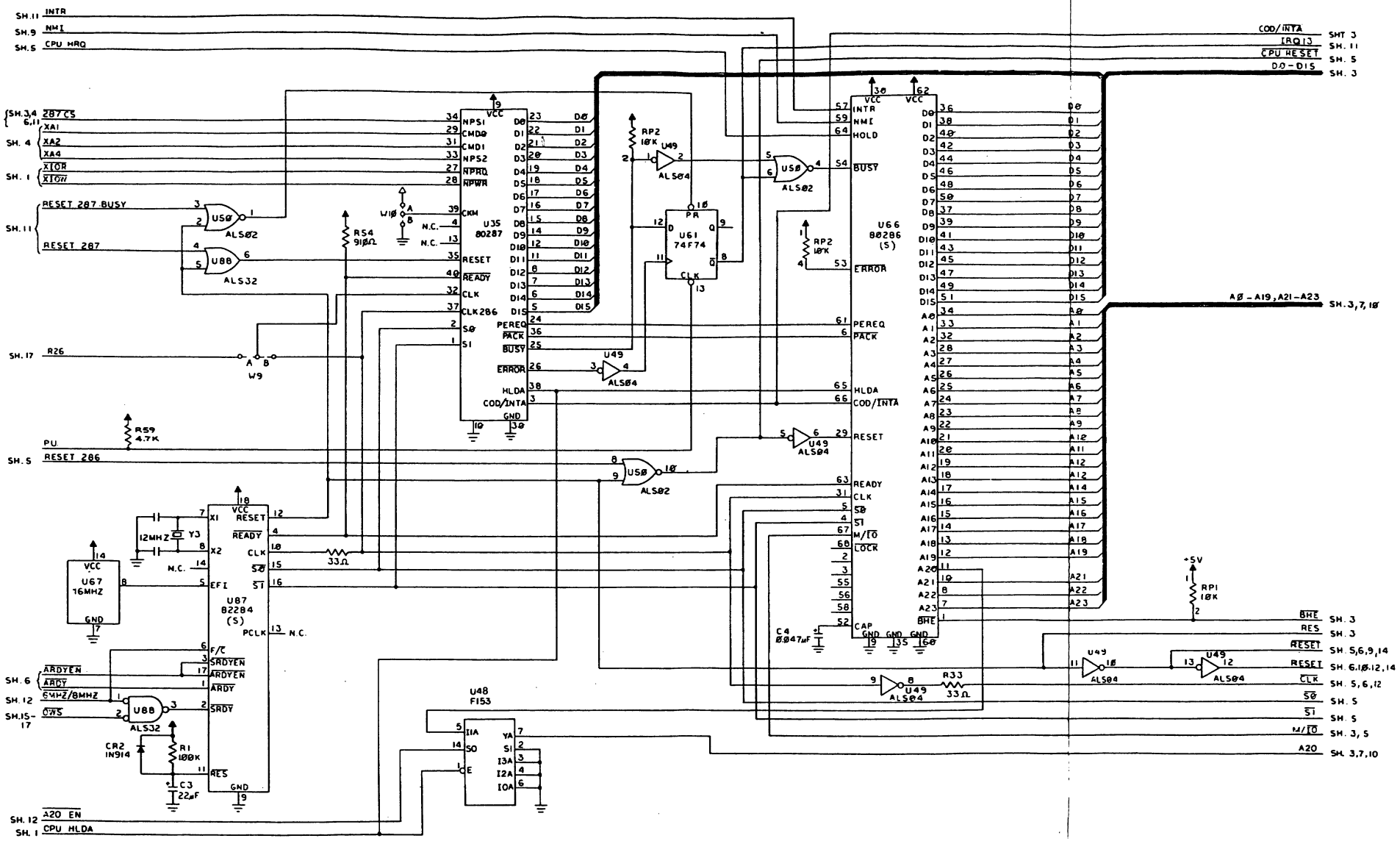
D.1 WIRING DIAGRAM



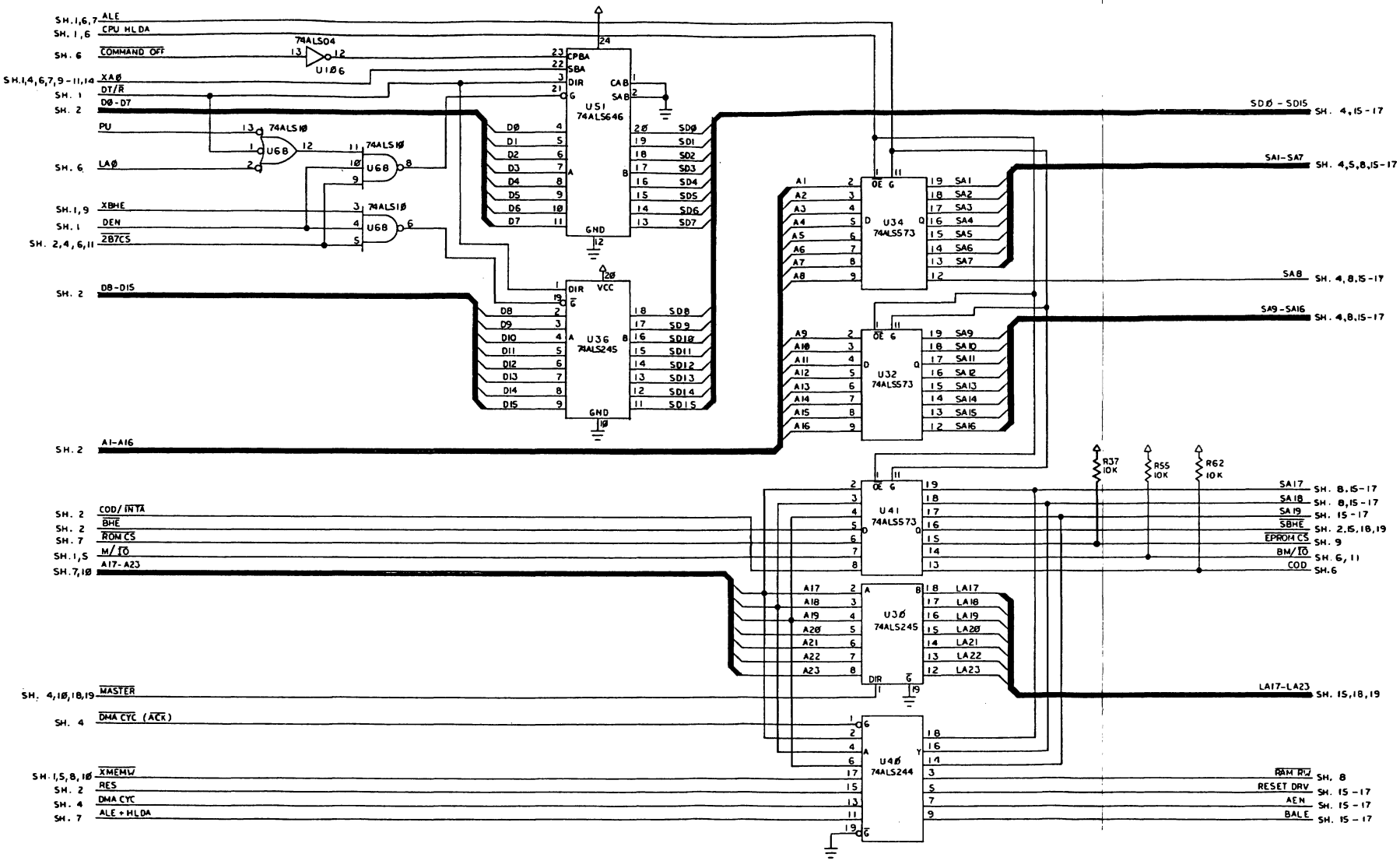
D.2 POWER SUPPLY



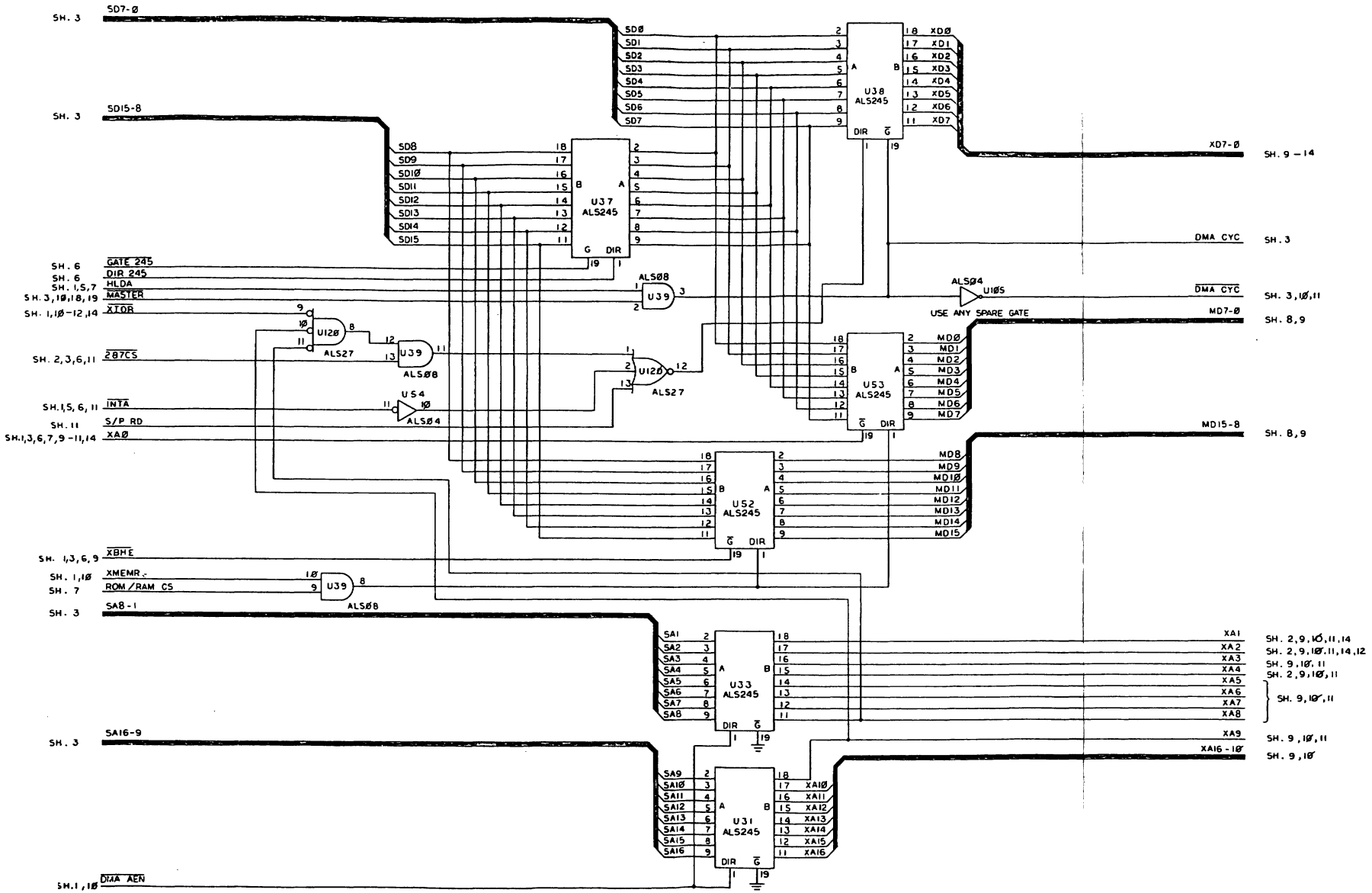
D.3 MOTHERBOARD - SHEET 1



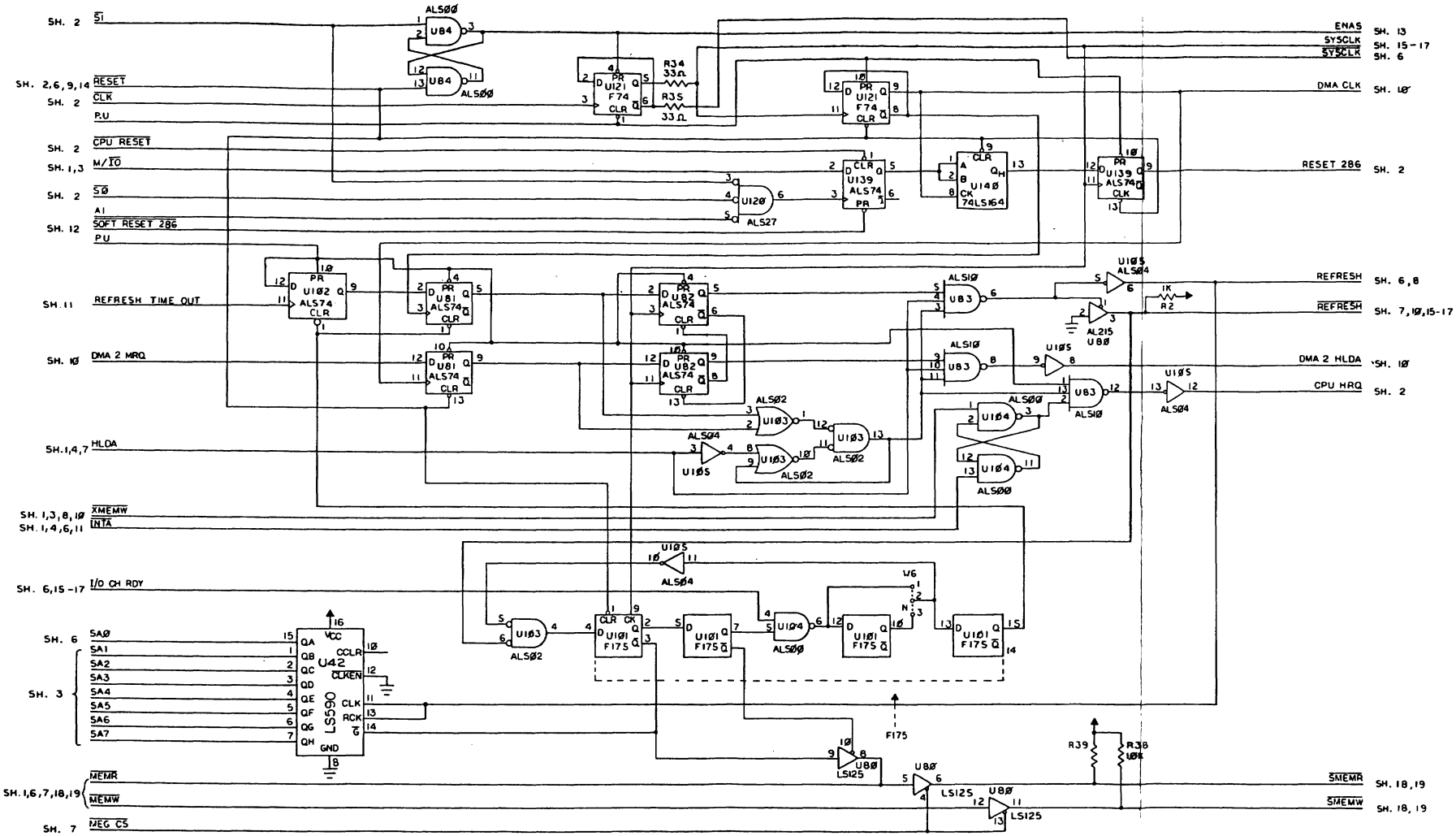
D.4 MOTHERBOARD - SHEET 2



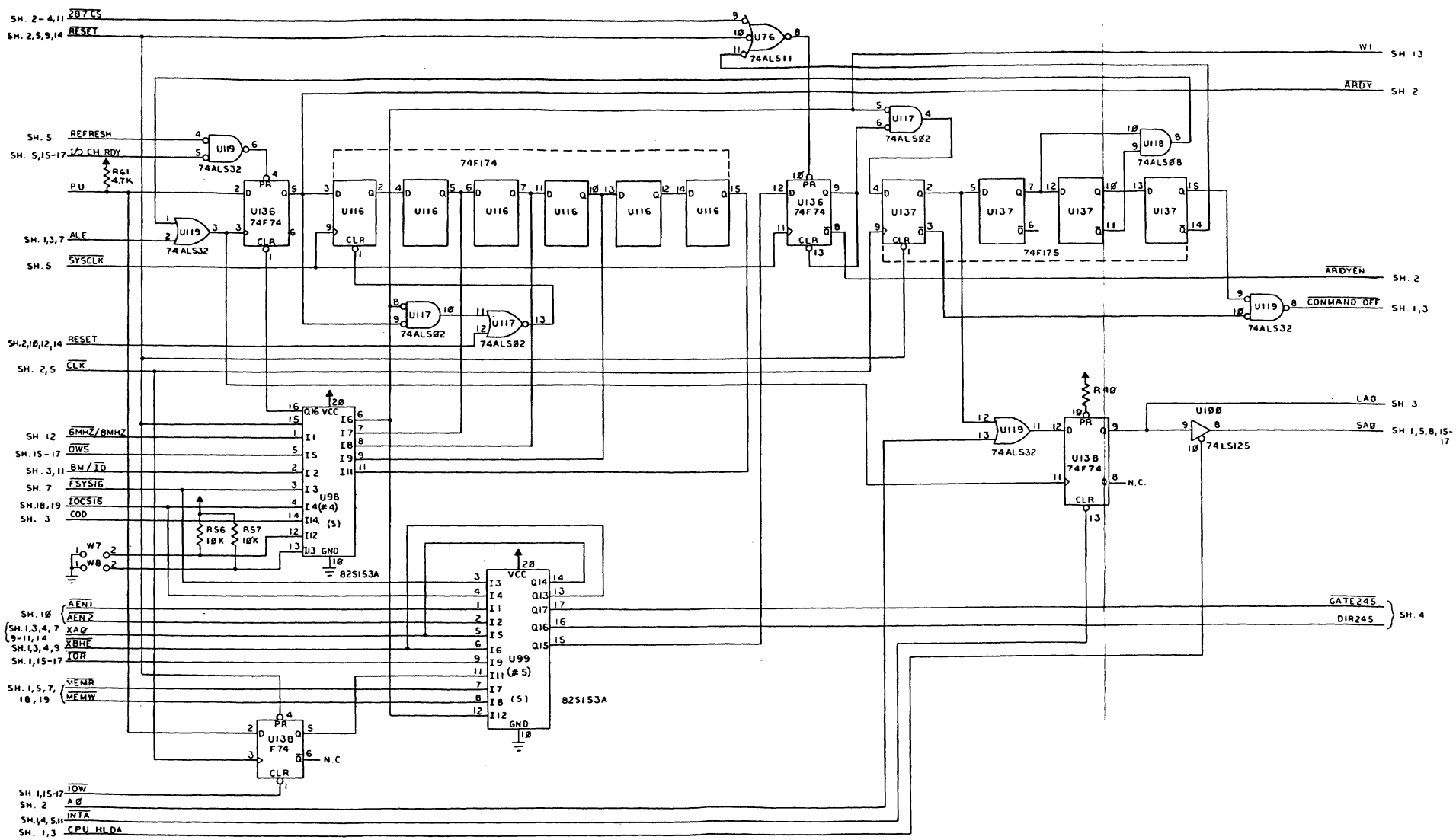
D.5 MOTHERBOARD - SHEET 3



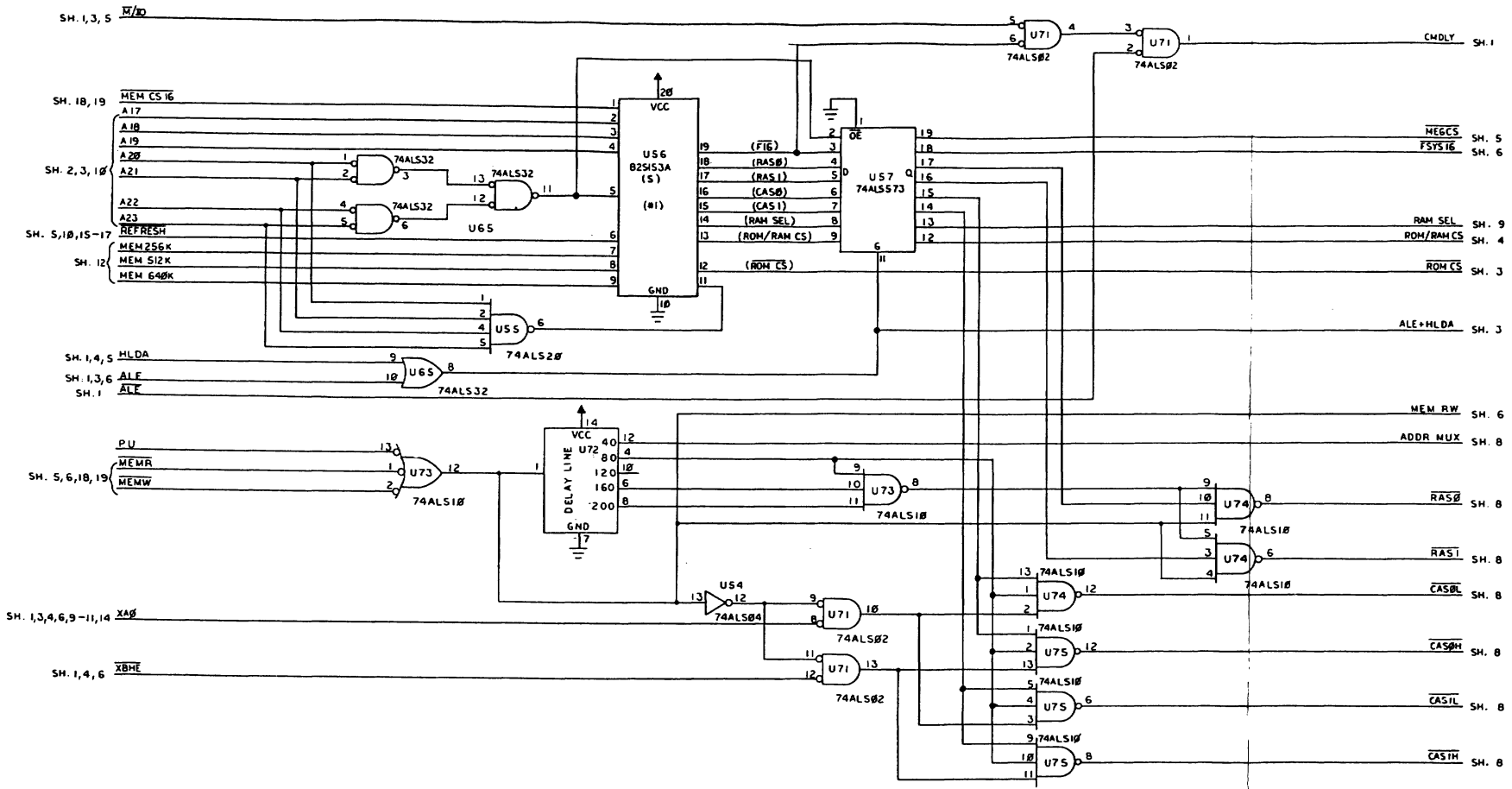
D.6 MOTHERBOARD – SHEET 4

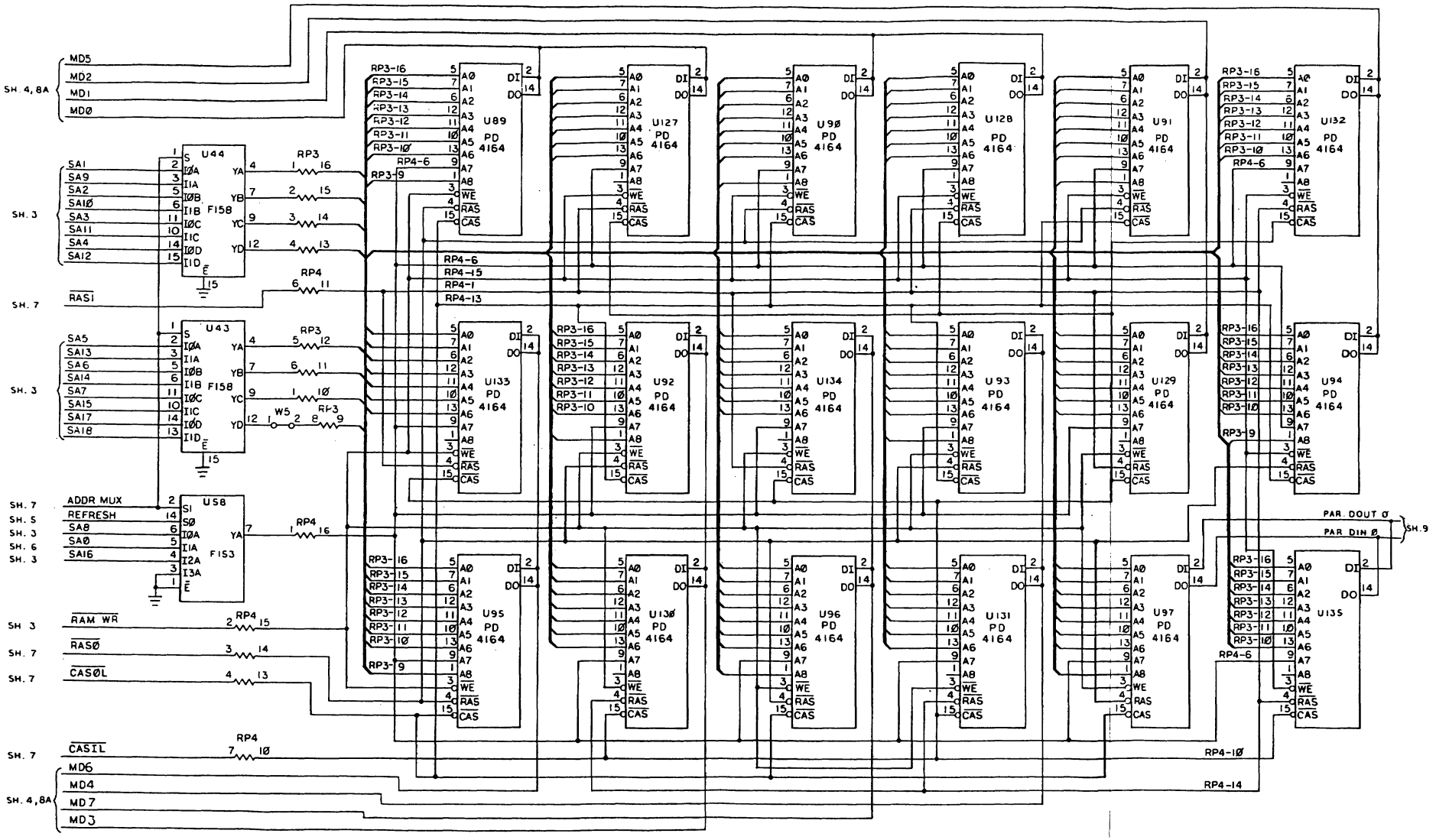


D.7 MOTHERBOARD – SHEET 5

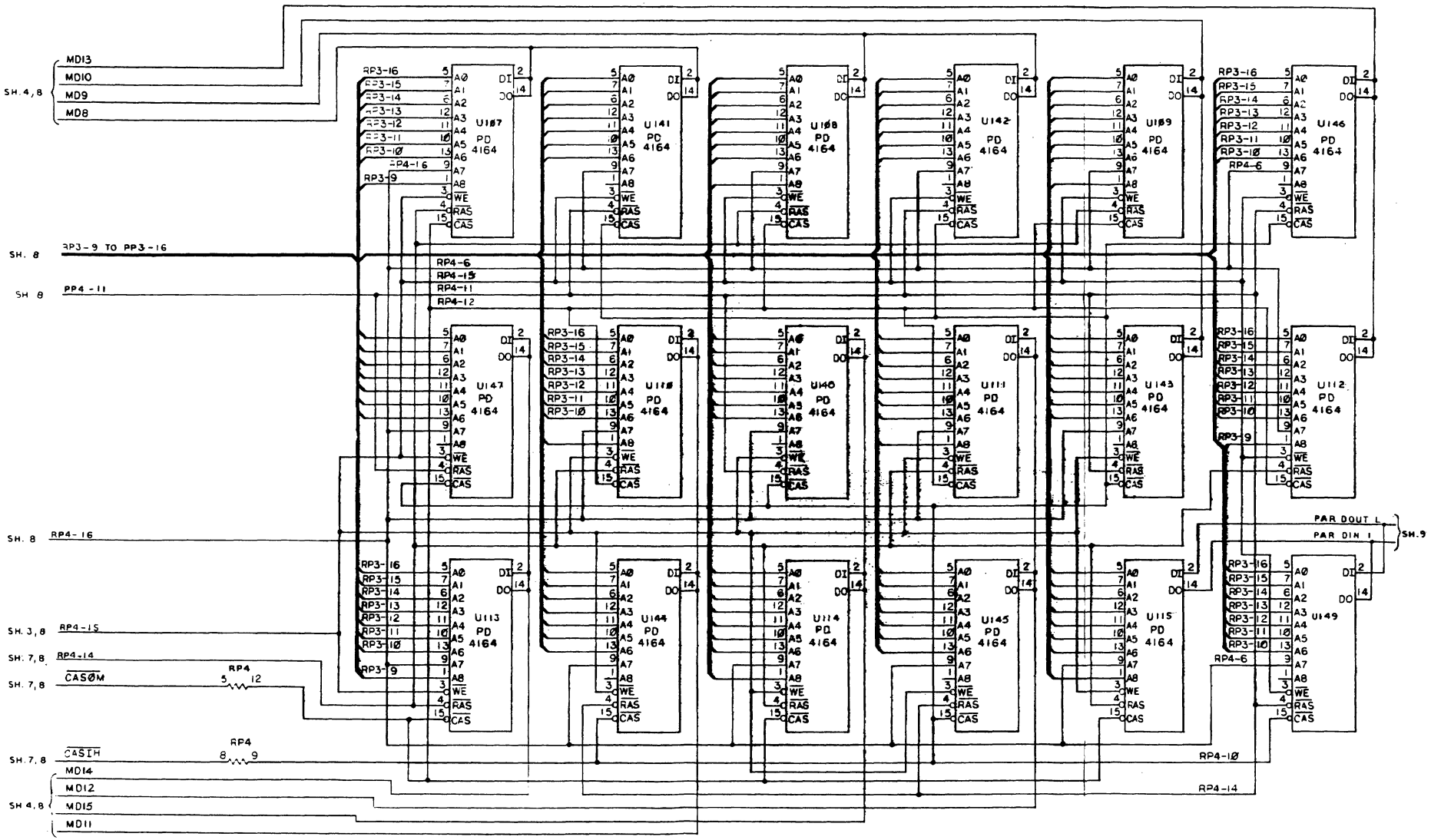


D.8 MOTHERBOARD - SHEET 6

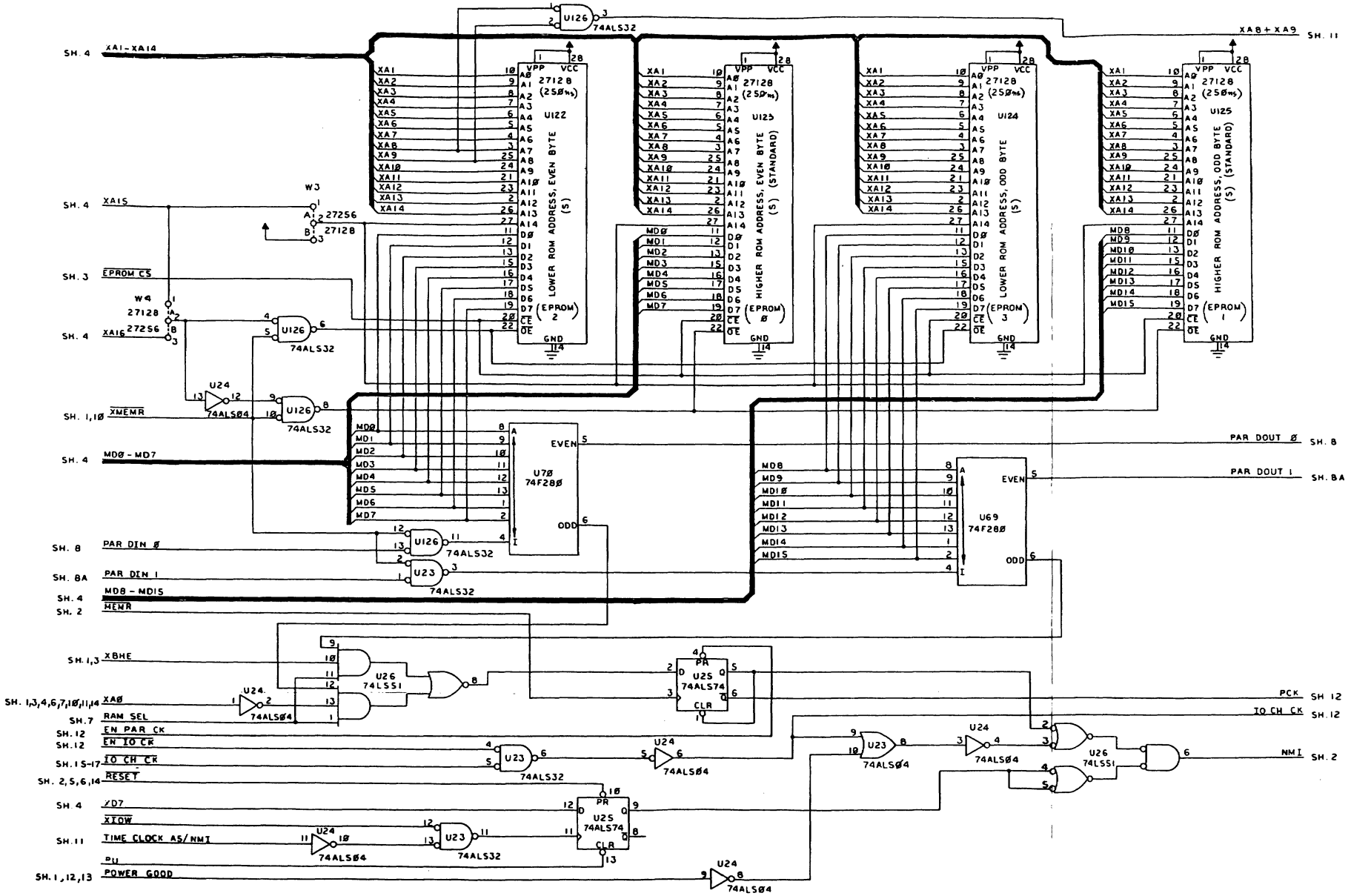

SH. 1,3,5 M/IO
U71
74ALS02
CMDLY
SH. 1
SH. 18,19 MEM CS16
A17
A18
A19
A20
SH. 2,3,10 A21
A22
A23
SH. 5,10,15-17 REFRESH
SH. 12 MEM256K
MEM 512K
MEM 640K
74ALS32
U65
U56
82S153A
(S)
(81)
20
VCC
GND
10
(FIG)
(RAS0)
(RAS1)
(CAS0)
(CAS1)
(RAM SEL)
(ROM/RAM CS)
(ROM CS)
U57
74ALS573
OE
MEGCS
SH. 5
FSYS16
SH. 6
RAM SEL
SH. 9
ROM/RAM CS
SH. 4
ROM CS
SH. 3
U55
74ALS20
ALE+HLDA
SH. 3
SH. 1,4,5 HLDA
SH. 1,3,6 ALE
SH. 1 ALE
MEM RW
SH. 6
ADDR MUX
SH. 8
PU
SH. 5,6,18,19 MEMR
MEMW
U73
74ALS10
U72
DELAY LINE
14
VCC
GND
7
40
80
120
160
200
U74
74ALS10
RAS0
SH. 8
RAS1
CAS0L
CAS0H
CAS1L
CAS1H
U75
U54
74ALS04
SH. 1,3,4,6,9-11,14 XA0
SH. 1,4,6 XBHE



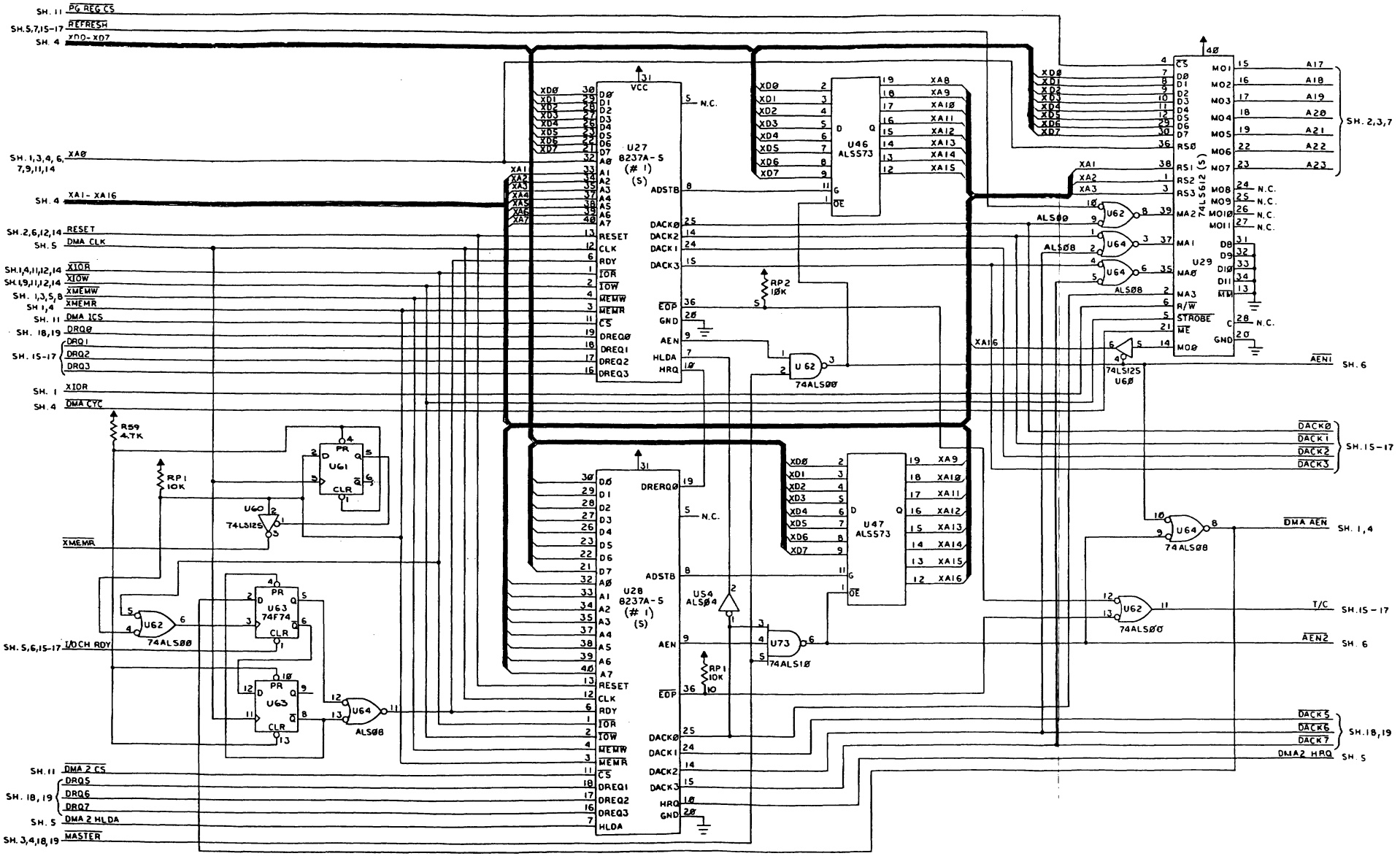
D.10 MOTHERBOARD - SHEET 8



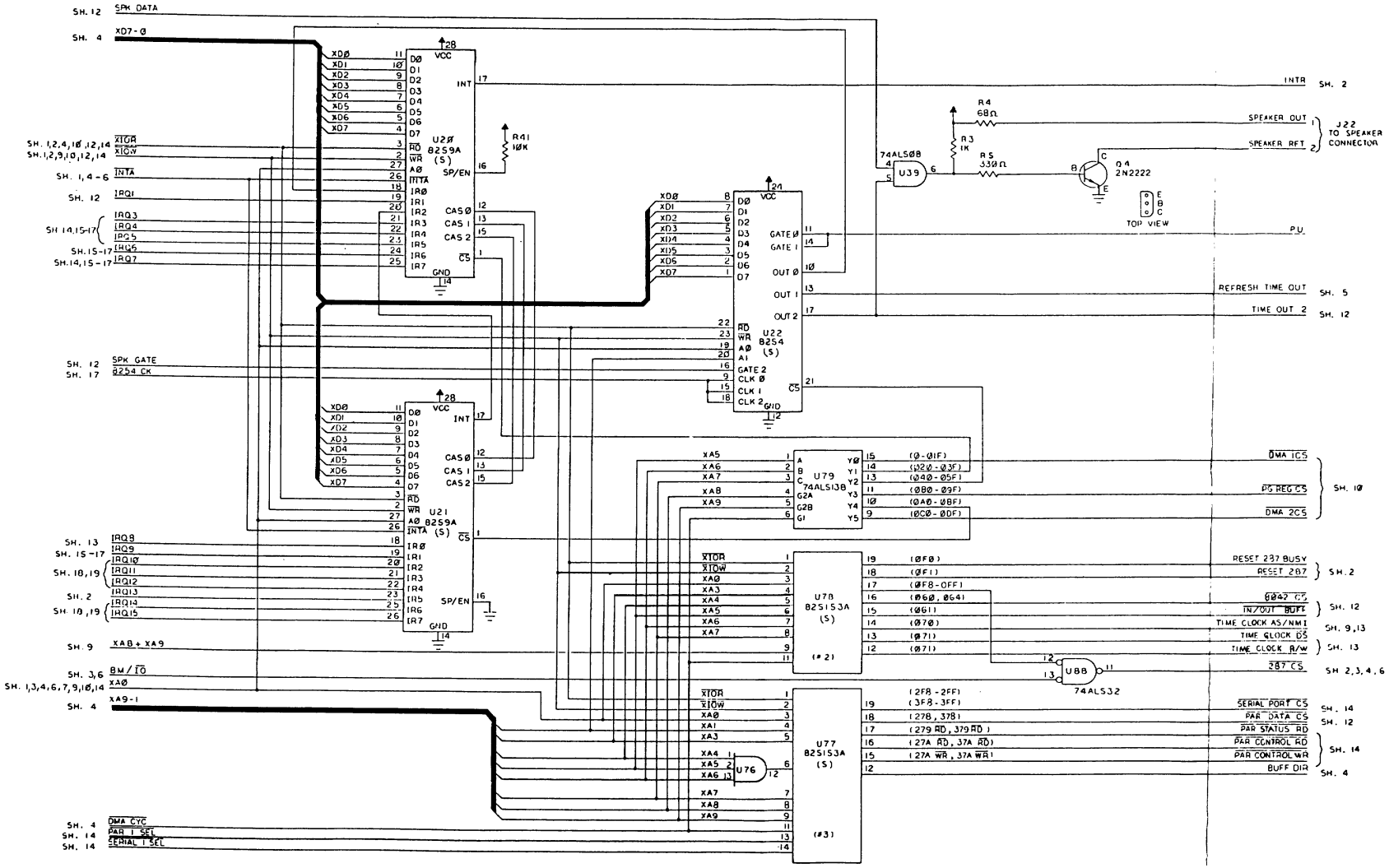
D.11 MOTHERBOARD - SHEET 8A



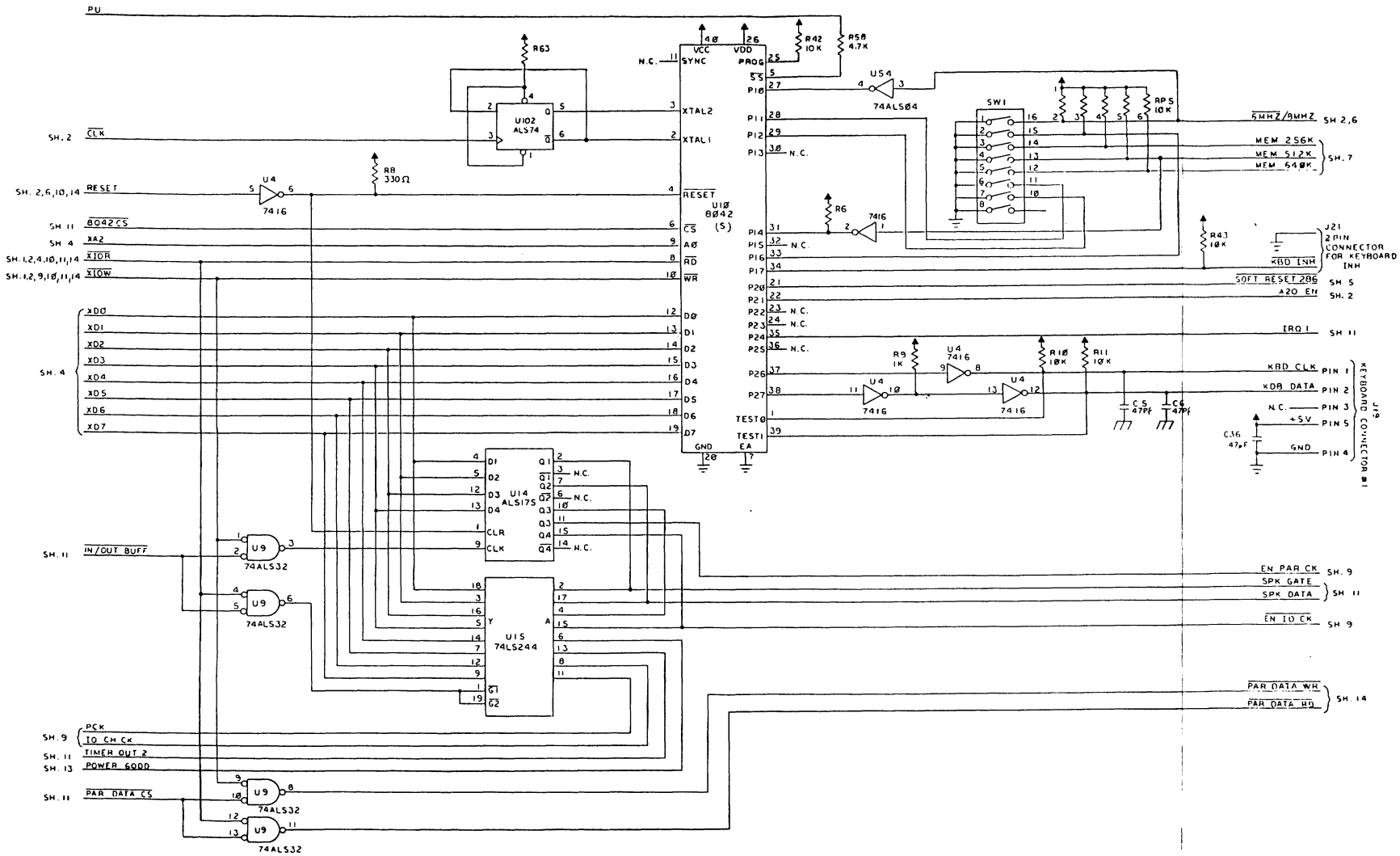
D.12 MOTHERBOARD - SHEET 9



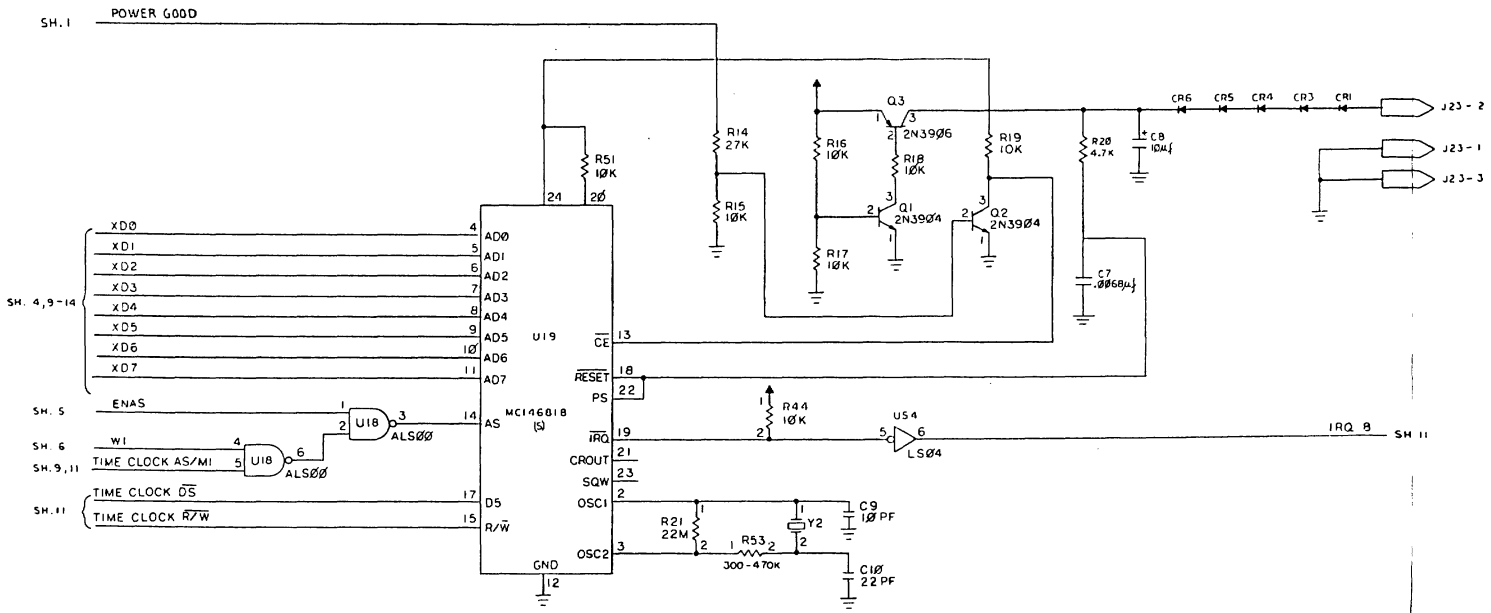
D.13 MOTHERBOARD - SHEET 10

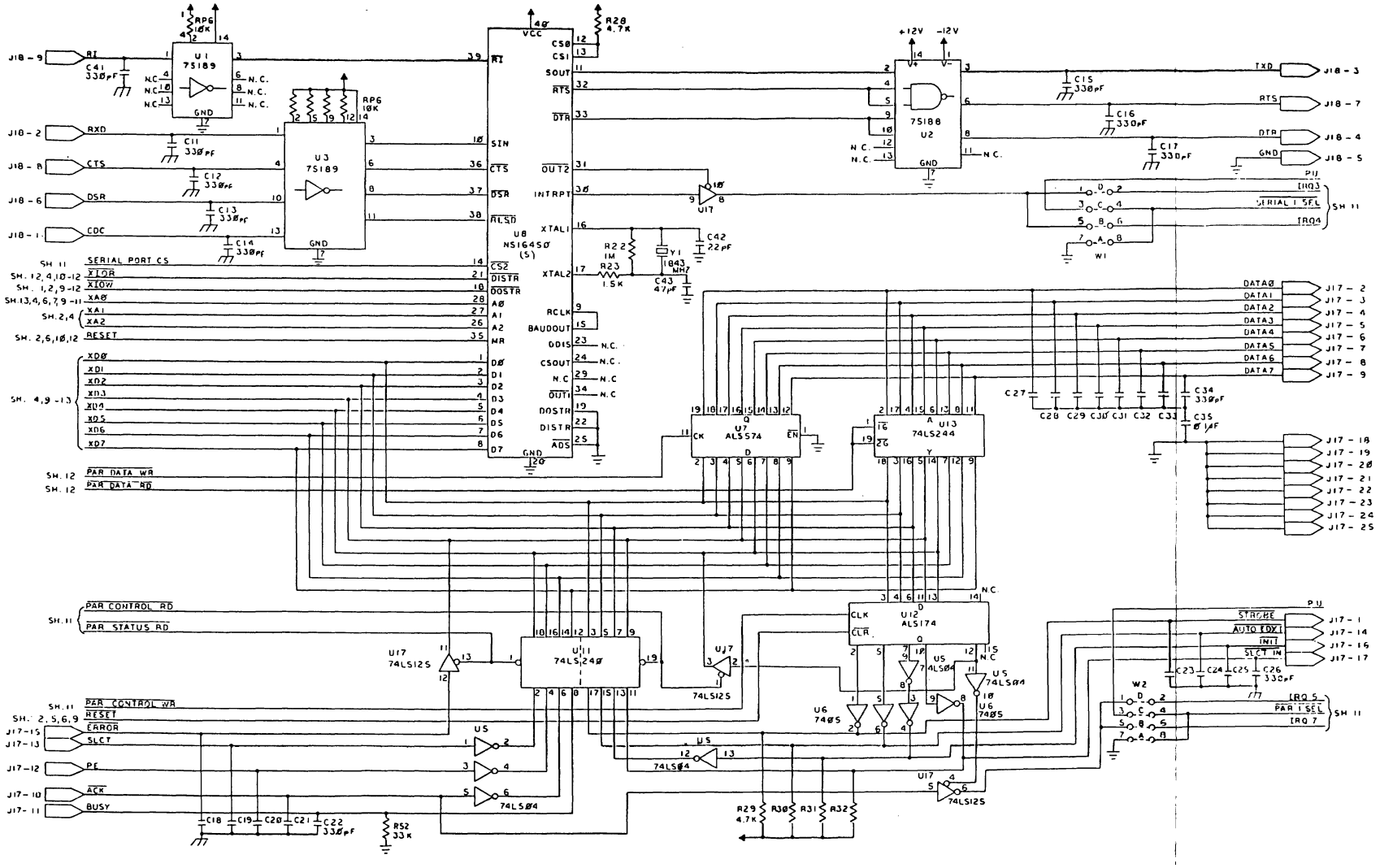


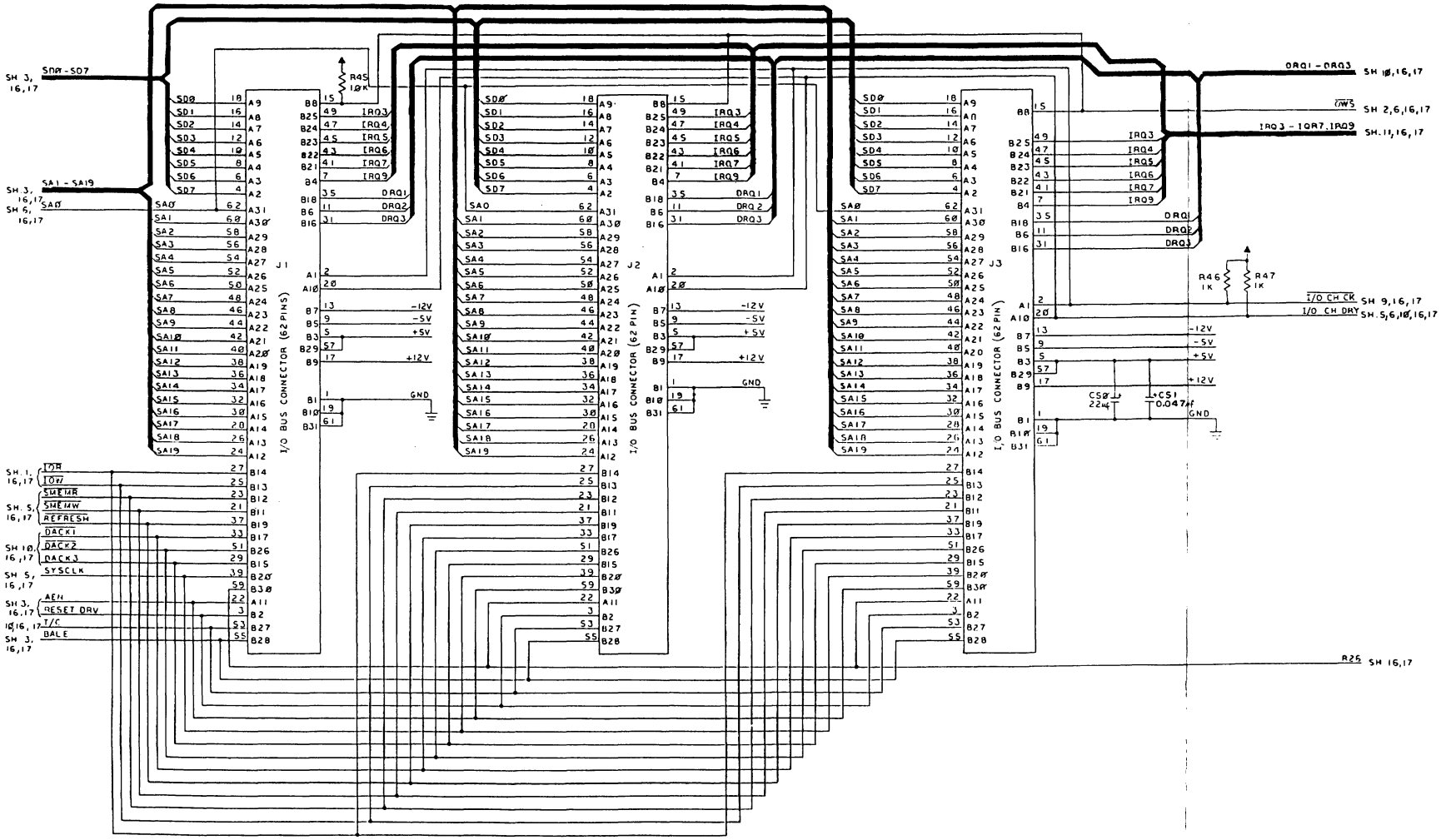
D.14 MOTHERBOARD - SHEET 11



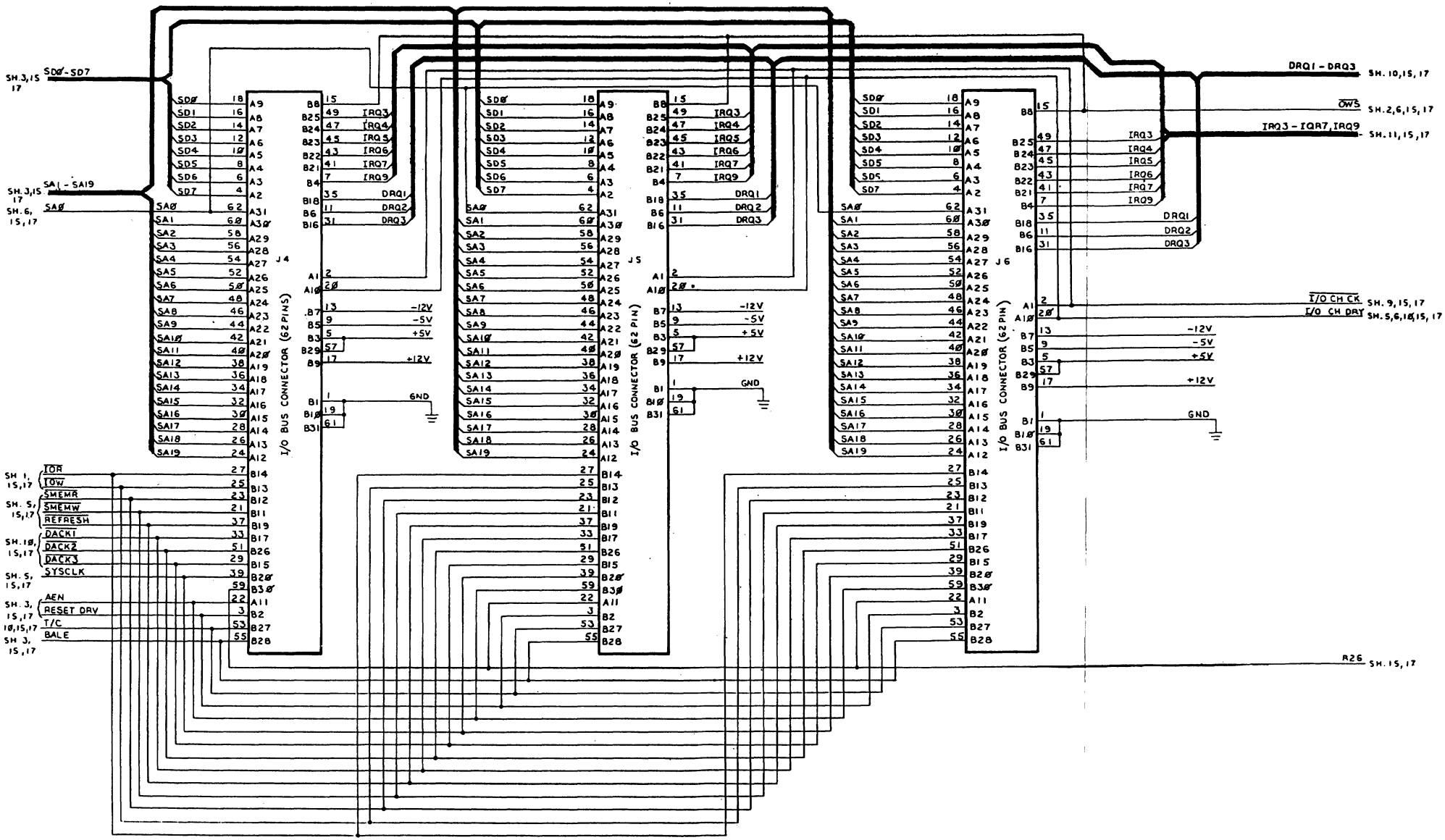
D.15 MOTHERBOARD - SHEET 12


SH. 1
POWER GOOD
R51 10K
R14 27K
R15 10K
R16 10K
R17 10K
R18 10K
R19 10K
R20 4.7K
C8 10µf
C7 .0068µf
Q3 2N3906
Q1 2N3904
Q2 2N3904
CR6 CR5 CR4 CR3 CR1
J23-2
J23-1
J23-3
SH. 4,9-14
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
U19
MC146818 (5)
CE
RESET
PS
IRQ
CROUT
SQW
OSC1
OSC2
AS
DS
R/W
GND
SH. 5
ENAS
SH. 6
W1
SH. 9,11
TIME CLOCK AS/MI
U18
ALS00
SH. 11
TIME CLOCK DS
TIME CLOCK R/W
R44 10K
U54
LS04
IRQ 8
SH 11
R21 22M
R53 300-470K
Y2
C9 10 PF
C10 22 PF

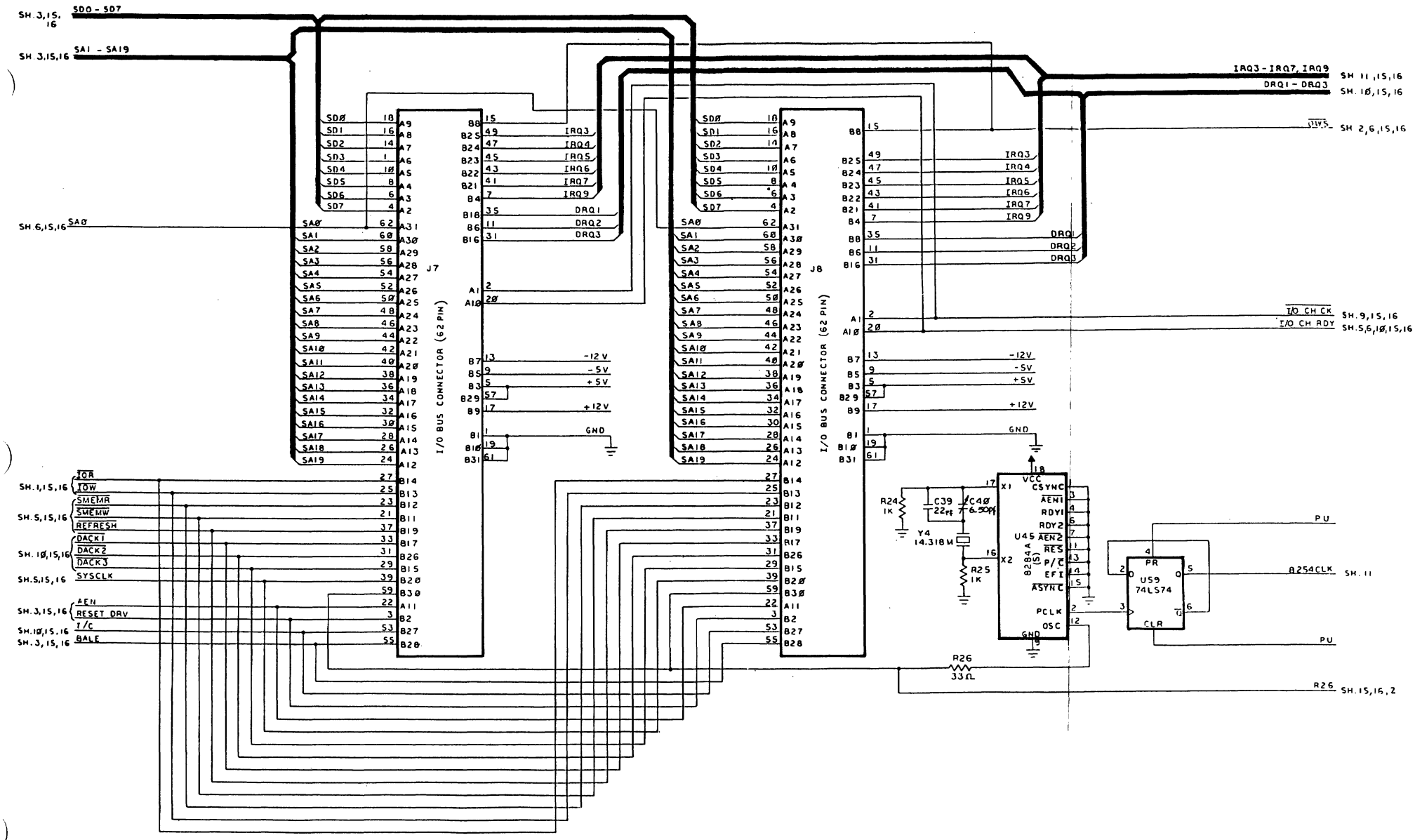




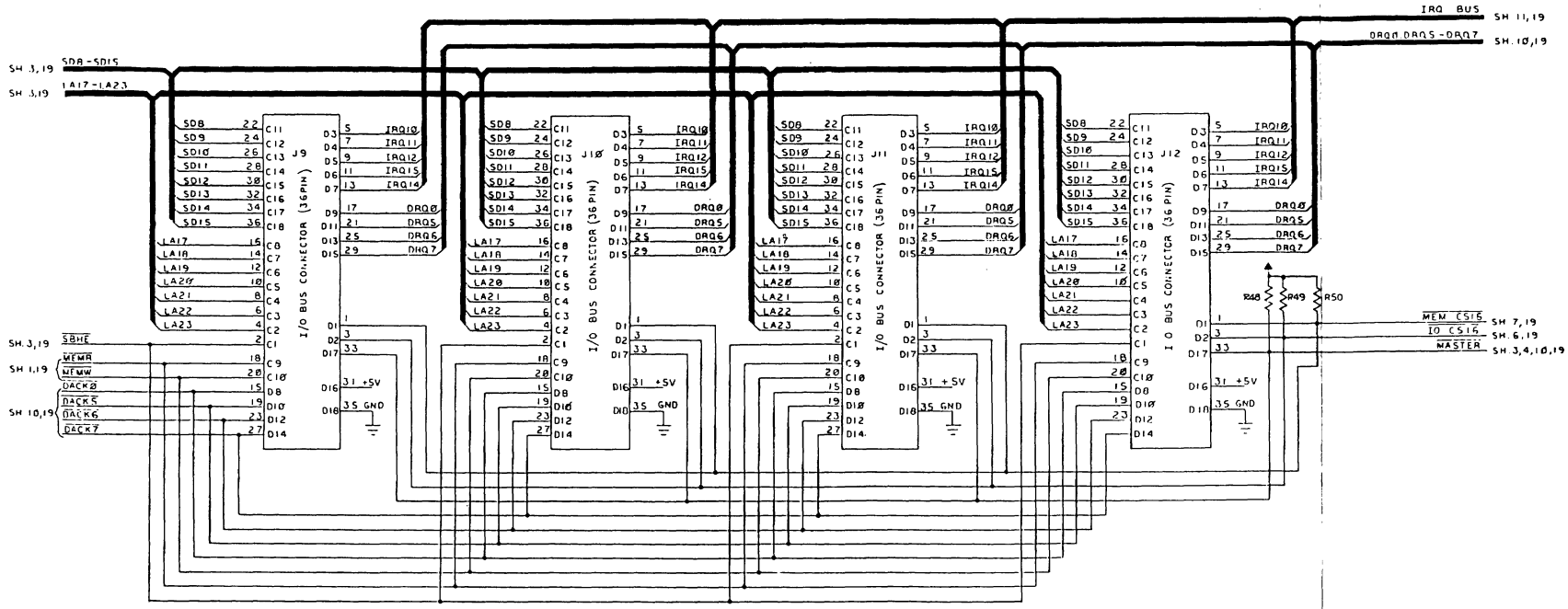
D.18 MOTHERBOARD - SHEET 15

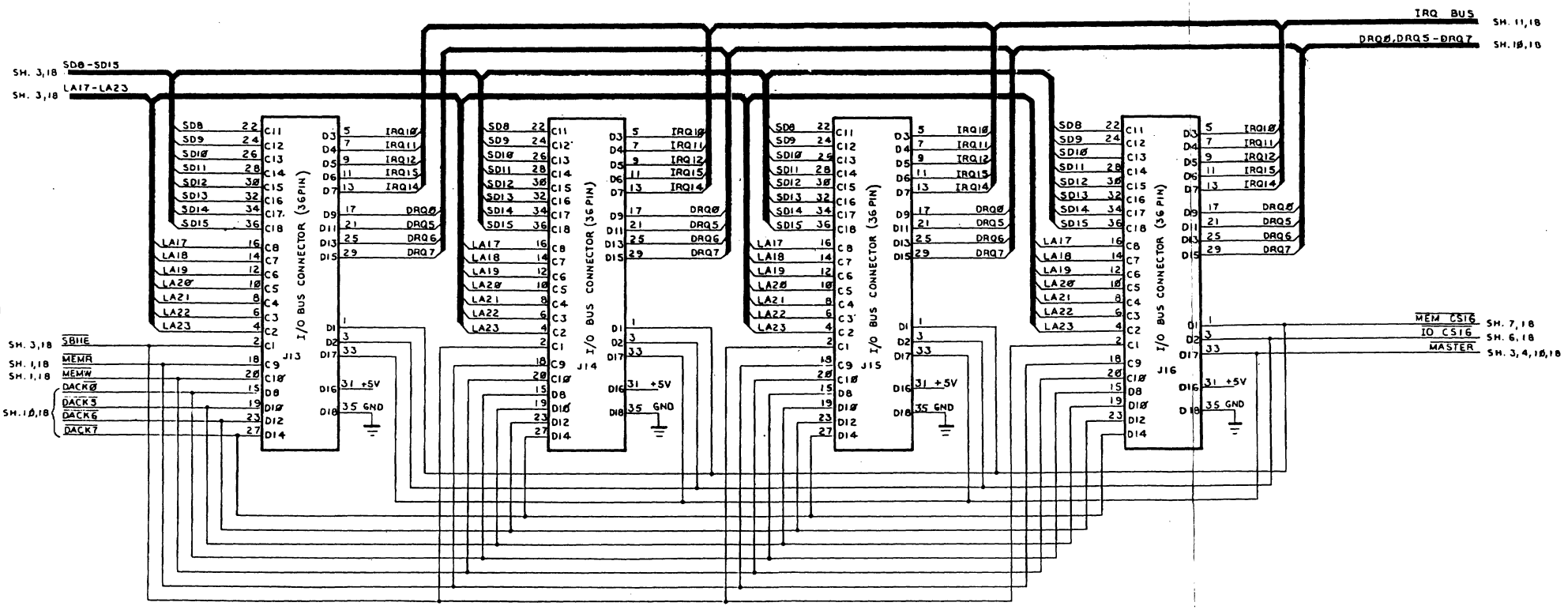


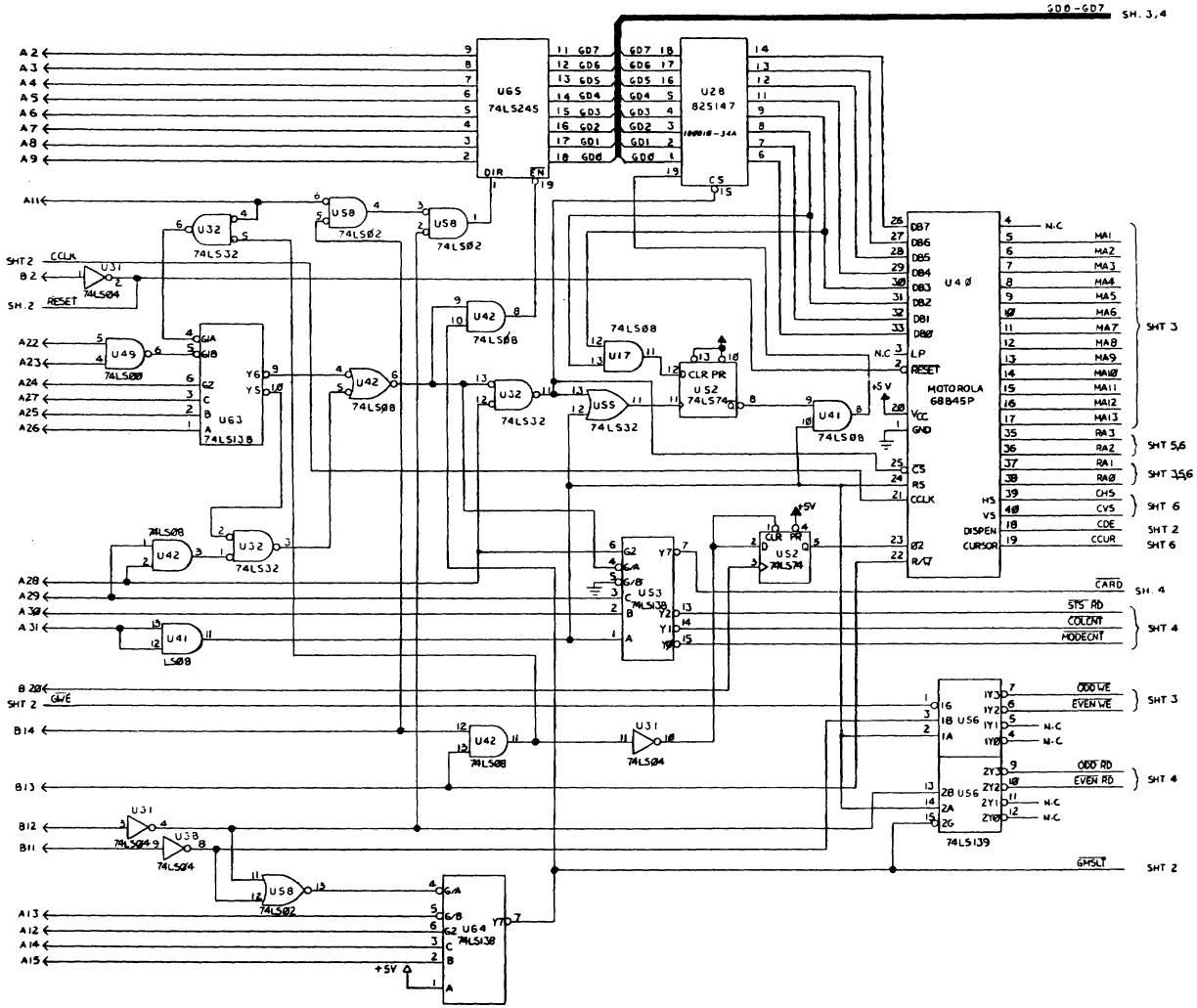
D.19 MOTHERBOARD - SHEET 16



D.20 MOTHERBOARD - SHEET 17

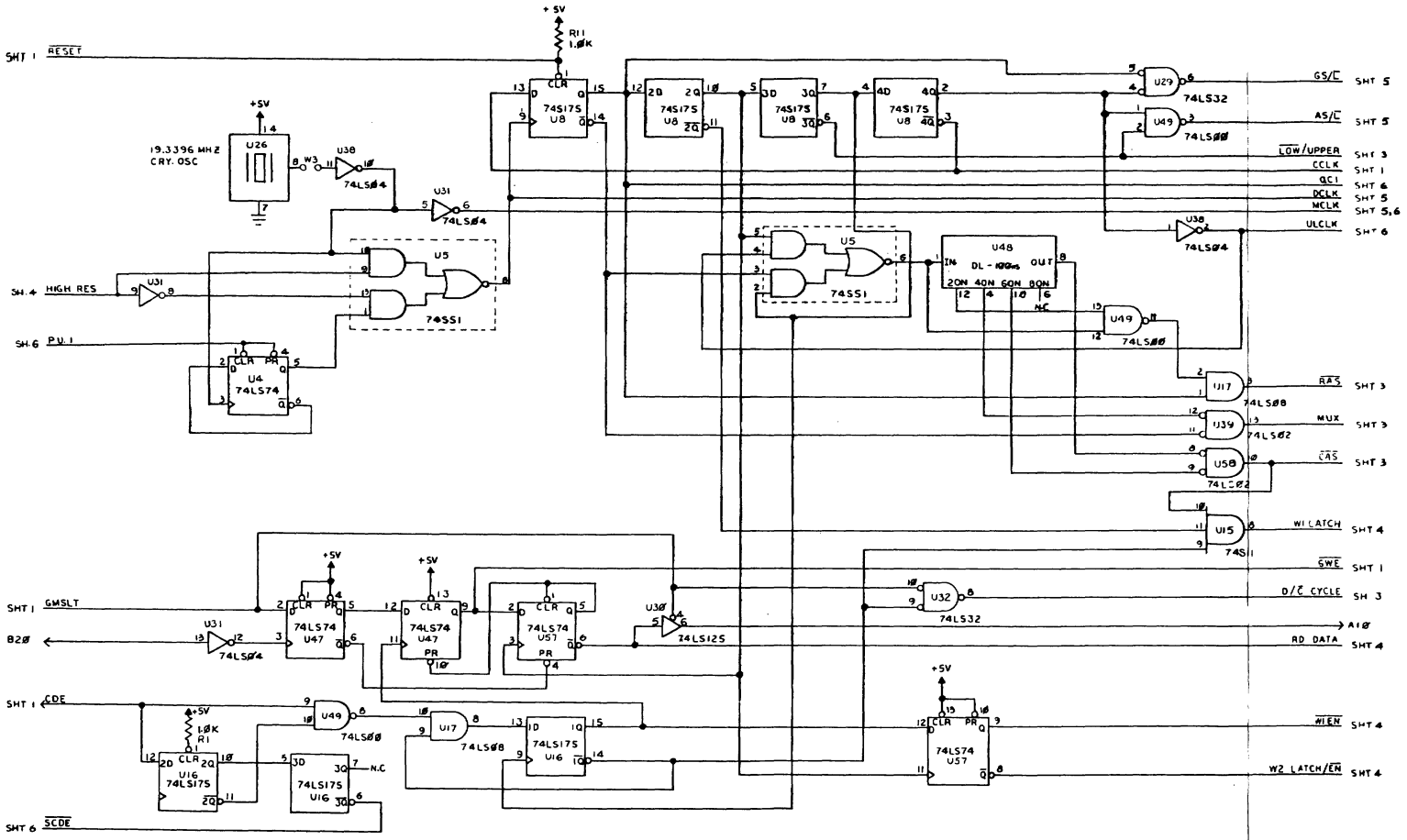

IRQ BUS
SH 11,19
DRQ0,DRQ5-DRQ7
SH.10,19
SH 3,19 SDA-SD15
SH 3,19 LA17-LA23
I/O BUS CONNECTOR (36 PIN)
J9
J10
J11
J12
SH.3,19 SBHE
SH 1,19 MEMR
MEMW
DACK0
DACK5
SH 10,19 DACK6
DACK7
R48
R49
R50
MEM CS16 SH 7,19
IO CS16 SH.6,19
MASTER SH.3,4,10,19


IRQ BUS
SH. 11,18
DRQØ,DRQ5-DRQ7
SH. 18,18
SH. 3,18 SD8-SD15
SH. 3,18 LA17-LA23
I/O BUS CONNECTOR (36PIN)
J13
J14
J15
J16
SH. 3,18 SBHE
SH. 1,18 MEMR
SH. 1,18 MEMW
SH. 18,18 DACKØ DACK5 DACK6 DACK7
MEM CS16
IO CS16
MASTER
SH. 7,18
SH. 6,18
SH. 3,4,18,18
+5V
GND

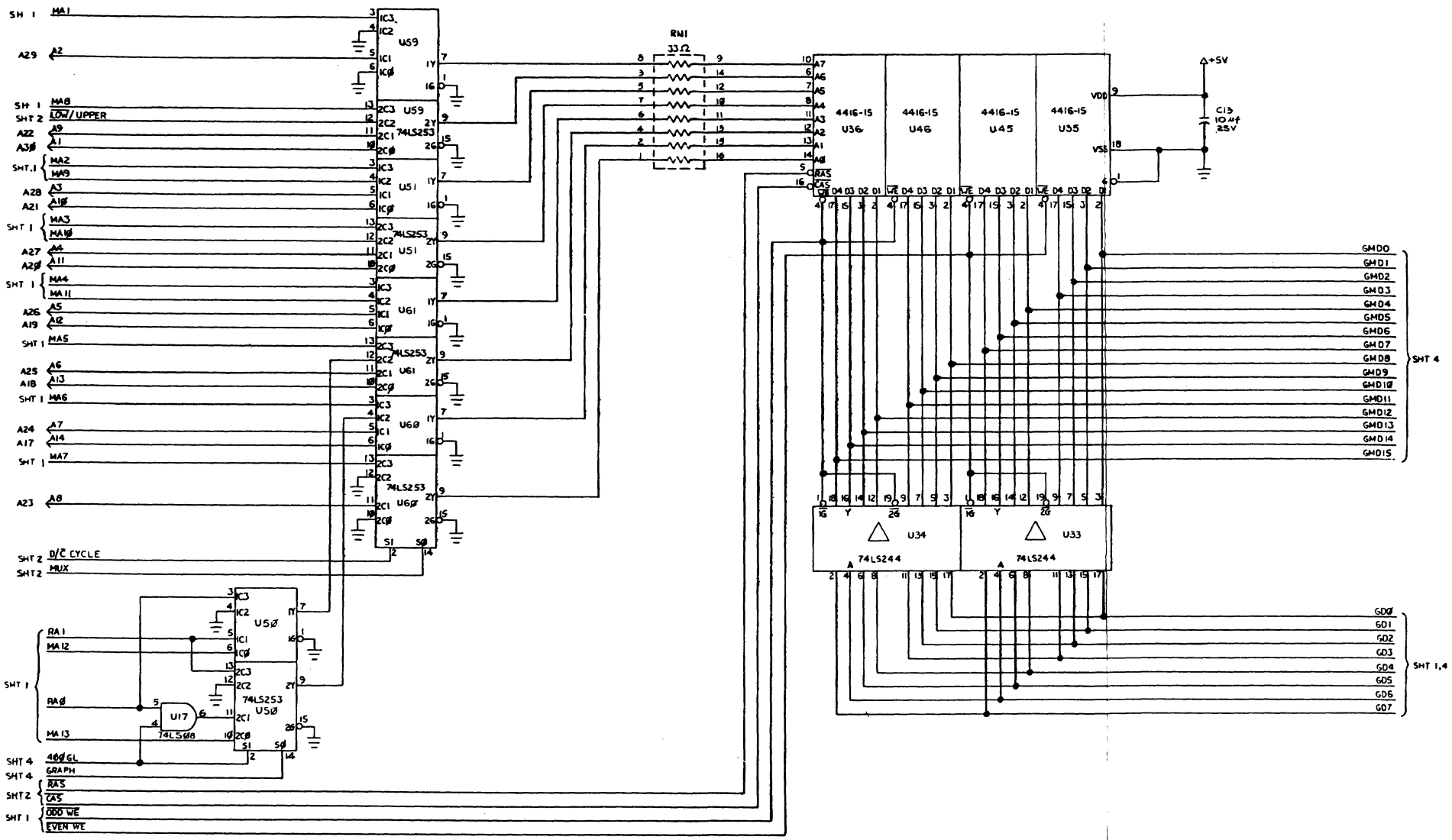


JUMPER SELECTION			INSTALLED
W1	1-2	DOUBLE DOT	2-3
	2-3	SINGLE DOT	
W2	ON	955M USED	ON
W3	ON	TEST	ON
W4	1-2	955M USED	1-2
	2-3	COLOR MONITOR	

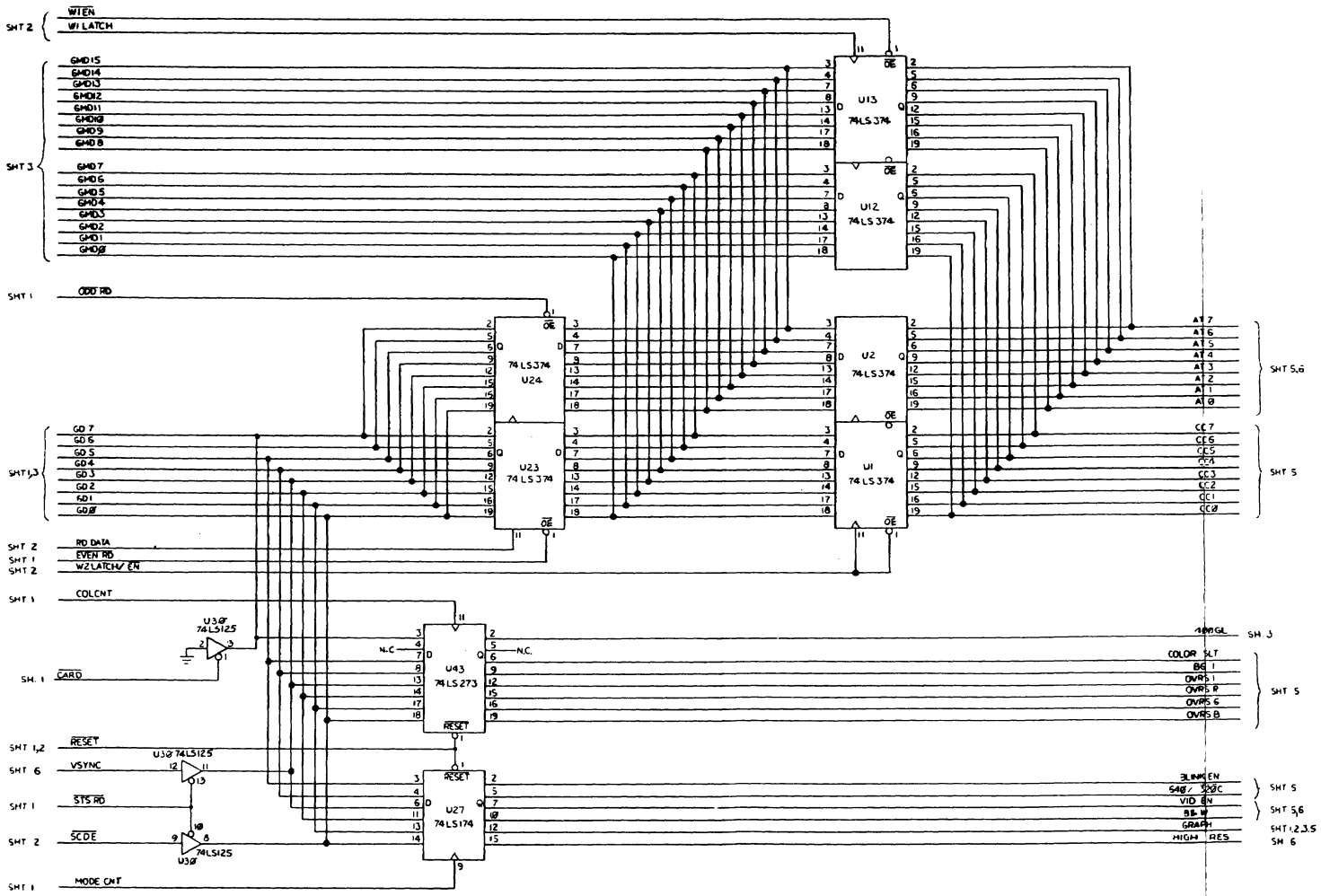
D.23 GRAPHICS BOARD - SHEET 1



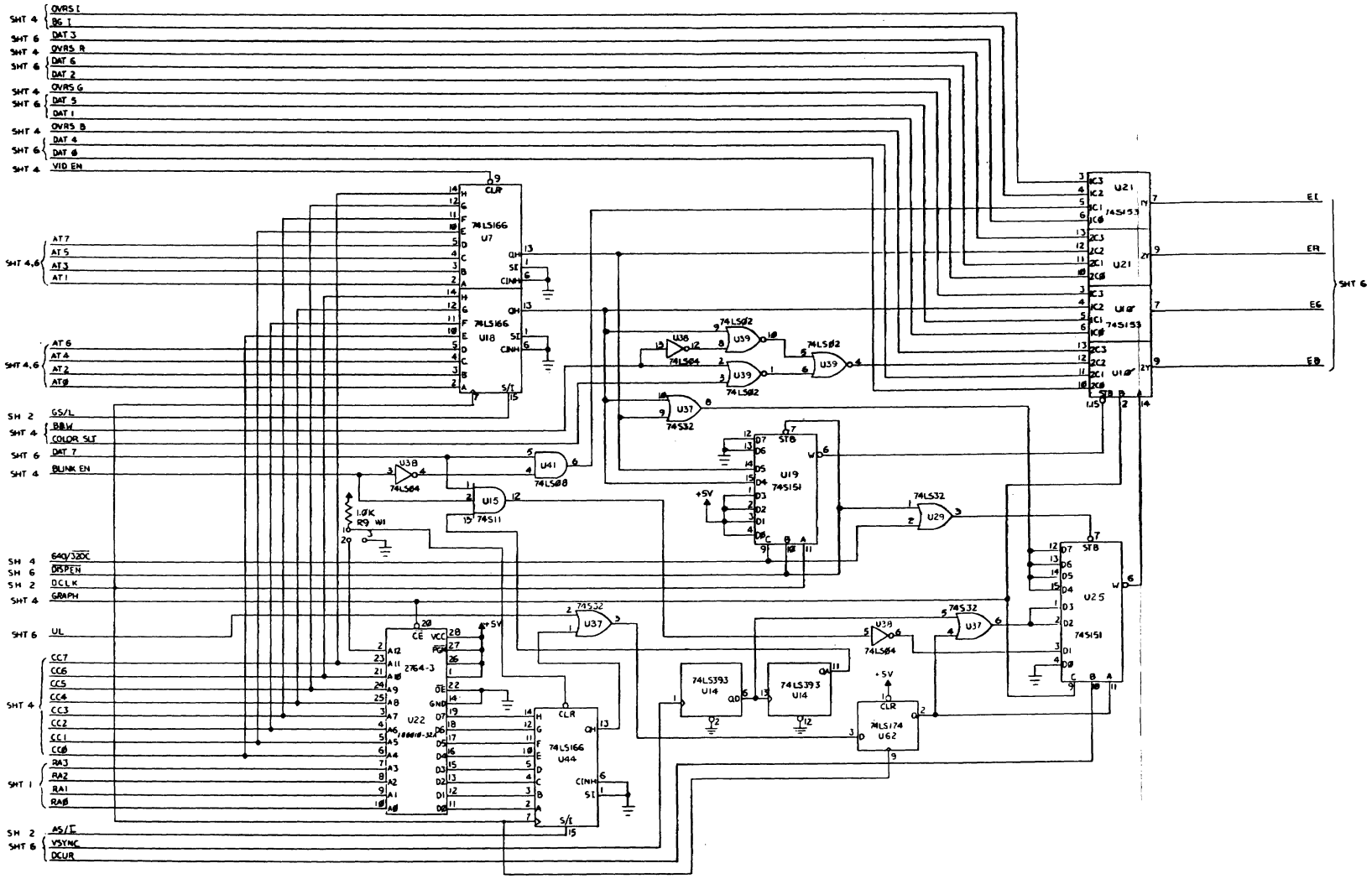
D.24 GRAPHICS BOARD - SHEET 2



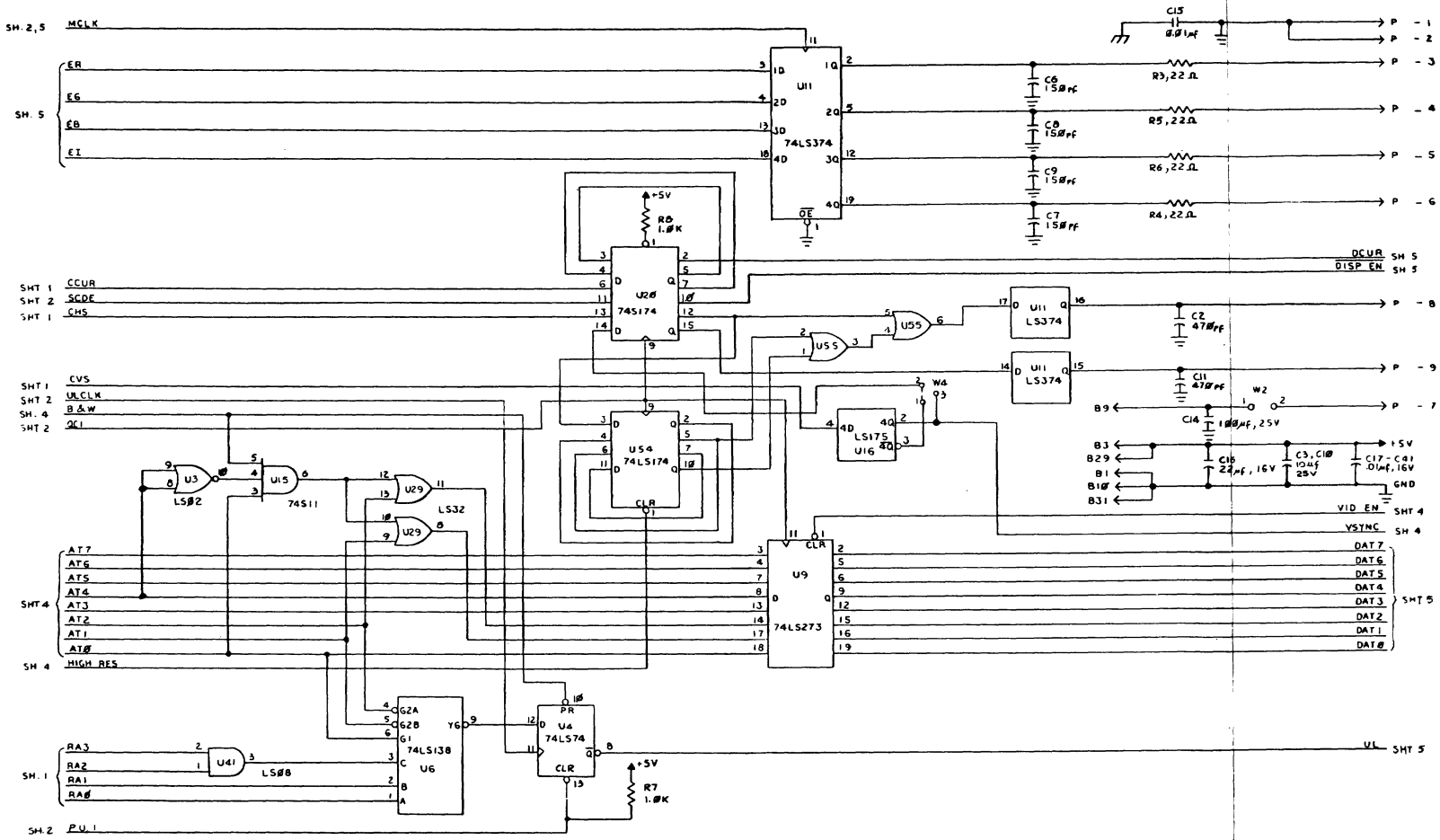
D.25 GRAPHICS BOARD - SHEET 3



D.26 GRAPHICS BOARD - SHEET 4



D.27 GRAPHICS BOARD - SHEET 5


SH. 2,5 MCLK
ER
EG
EB
EI
SH. 5
U11
74LS374
OE
C15 0.01μF
C6 150pF
C8 150pF
C9 150pF
C7 150pF
R3, 22Ω
R5, 22Ω
R6, 22Ω
R4, 22Ω
P - 1
P - 2
P - 3
P - 4
P - 5
P - 6
+5V
R8 1.0K
U28
74S174
DCUR SH 5
DISP EN SH 5
SHT 1 CCUR
SHT 2 SCDE
SHT 1 CHS
U55
U11 LS374
C2 470pF
P - 8
SHT 1 CVS
SHT 2 ULCLK
SH. 4 B&W
SHT 2 QCI
U54
74LS174
CLR
W4
LS175 U16
C11 470pF
W2
B9
C14 10μF, 25V
P - 9
P - 7
B3
B29
B1
B10
B31
C15 22μF, 16V
C3, C10 10μF 25V
C17 - C41 .01μF, 16V
+5V
GND
U3 LS02
U15 7411
U29 LS32
VID EN SHT 4
VSYNC SH 4
AT7
AT6
AT5
AT4
AT3
AT2
AT1
AT0
SHT 4
SH 4 HIGH RES
U9
74LS273
CLR
DAT7
DAT6
DAT5
DAT4
DAT3
DAT2
DAT1
DAT0
SHT 5
G2A
G2B
G1
74LS138
U6
Y6
PR
U4
74LS74
CLR
VL SHT 5
RA3
RA2
RA1
RA0
SH. 1
U41 LS08
R7 1.0K
SH. 2 PU 1

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