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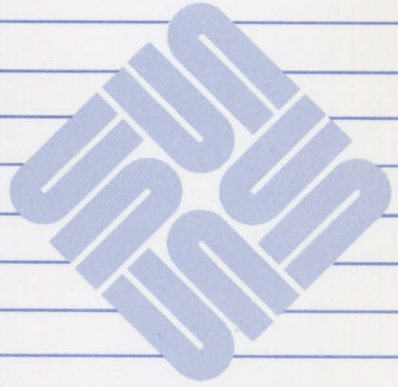
Sun 3400 CPU Board Configuration Manual



Part No: Part Number: 813-2055-11
Revision A of 15 May 1989

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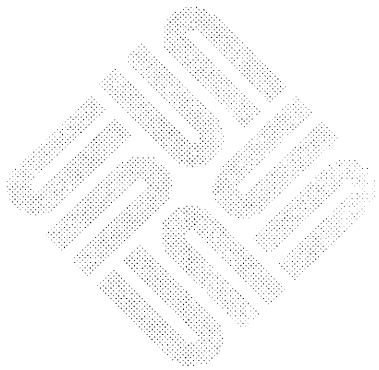
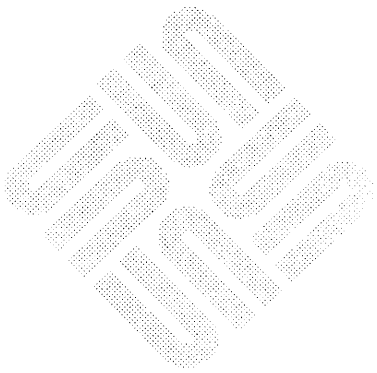
Contents

Chapter 1 General Description and Configuration **3**
Introduction 3
General Sun 3400 CPU Board Description 3
Video Daughter Boards 4
Configuration of the Jumpers on the 3400 CPU Board 4
ECC Memory Configuration 4



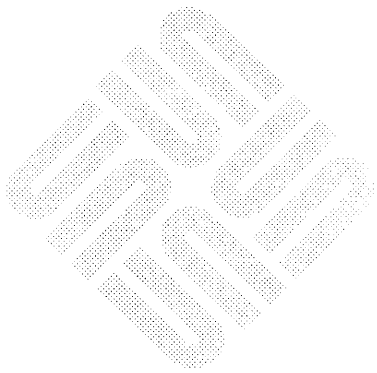
Tables

Table 1-1 *Factory Configuration of Jumpers on the 3400 CPU Board* 5



Figures

Figure 1-1 *Section A-H of the Board* 6
Figure 1-2 *Section I-O of the Board* 7



1

General Description and Configuration

General Description and Configuration 3

Introduction 3
General Sun 3400 CPU Board Description 3
Video Daughter Boards 4
Configuration of the Jumpers on the 3400 CPU Board 4
ECC Memory Configuration 4

1

General Description and Configuration

Introduction

This document identifies jumper–block locations and describes required jumper configurations on the Sun 3400 CPU Board.

Instructions for the removal and installation of your boards are contained in their respective board installation manuals. Instructions for board access and backplane jumper access are contained in your system installation manual. Instructions for the configuration of your backplane jumpers are contained in your *Sun-3/460 and 3/480 Cardcage Slot Assignments and Backplane Configuration Procedures* manual (P/N 813–2056), CCSA and BCA (P/N 2004) or in your *Sun-3/470 Cardcage Slot Assignments and Backplane Configuration Procedures* manual (P/N 813-2073).

Instructions for the configuration of your memory boards or your frame buffer boards are covered in their respective memory board or frame buffer board manuals.

General Sun 3400 CPU Board Description

Standard features of the Sun 3400 CPU board include:

- A 68030 central processor with separate internal 256 byte instruction and data caches and an address translation cache (ATC) for CPU address translation. The data cache is designed as a write–through cache. Both the data and instruction caches are structured as 32 blocks of 16 bytes each. The 68030 runs at 33 MHz.
- A central cache configured as a 64 kbyte writeback cache.
- An I/O cache that supports 16 byte blocks.
- A 68882 Floating Point Coprocessor (FPC) running on the same 33MHz clock as the CPU and enabled by the system enable register bit.
- A VMEbus arbitration and diagnostic mode for DVMA interface testing on the board.
- 64-bit multiplexed address/data bus memory with support for both 8MB and 32MB ECC memory boards and the Sun-3 Floating Point Accelerator (FPA) board.
- P4 bus support that allows a variety of video daughter boards to be used.
- P2 MEZZ bus support that allows the FPA+ to be used.

- Interface circuitry that supports the VMEbus, Ethernet, two serial ports, the keyboard, and the mouse.

An optional feature is the Data Ciphering Protocol (DCP) Processor chip set. This chip set provides additional security for your sensitive files by encrypting network data.

Video Daughter Boards

The Sun 3400 CPU board will be paired with either a monochrome video daughter board or one of three color video daughter boards. In some systems, a separate terminal will be connected to one of the serial ports on the rear edge of the 3400 CPU board. In other systems, a monitor will operate from a separate color or graphics board.

Configuration of the Jumpers on the 3400 CPU Board

Table 1 on the following page shows the factory configuration of the jumper–blocks on the Sun 3400 CPU board.

Each board has grid markings that form an X–Y coordinate system. Letters of the alphabet define the X coordinate and numbers define the Y coordinate of the grid. Table 1 lists the location coordinates of pin 1 of each jumper–block. For example, referring to Table 1, pin 1 of jumper–block J100 is located at the intersection of coordinates "L" and "34".

In Table 1, the *Configuration* column indicates which pins can be jumpered together and whether or not the board is shipped with the referenced jumper connection installed on the indicated pins. For example, "1–2" in the Configuration column means that a jumper is installed across pins 1 and 2. "IN" means that the CPU board is shipped with the jumper connection installed. "OUT" means that the board is shipped with the jumper connection not installed.

Again referring to Table 1, the *Description* column lists the effect of each jumper–block when it is installed in the indicated position. With one exception, when a jumper is "IN", a function is enabled or selected. The exception is jumper–block J100 which disables functions when installed.

To find pin 1 on a given jumper–block, turn the board over to the solder side and look closely at the pins. Pin 1 is soldered into a square shaped pad while the other pins are soldered into circular shaped pads.

Figures 1 and 2 show where jumper–blocks are located on the Sun 3400 CPU board.

ECC Memory Configuration

When the Sun 3400 CPU board is shipped with the 8MB or the 32MB ECC memory board installed, no reconfiguration of the Sun 3400 CPU board or the ECC memory board is required. However, if you install another memory board, you will need to configure that memory board at the time of installation.

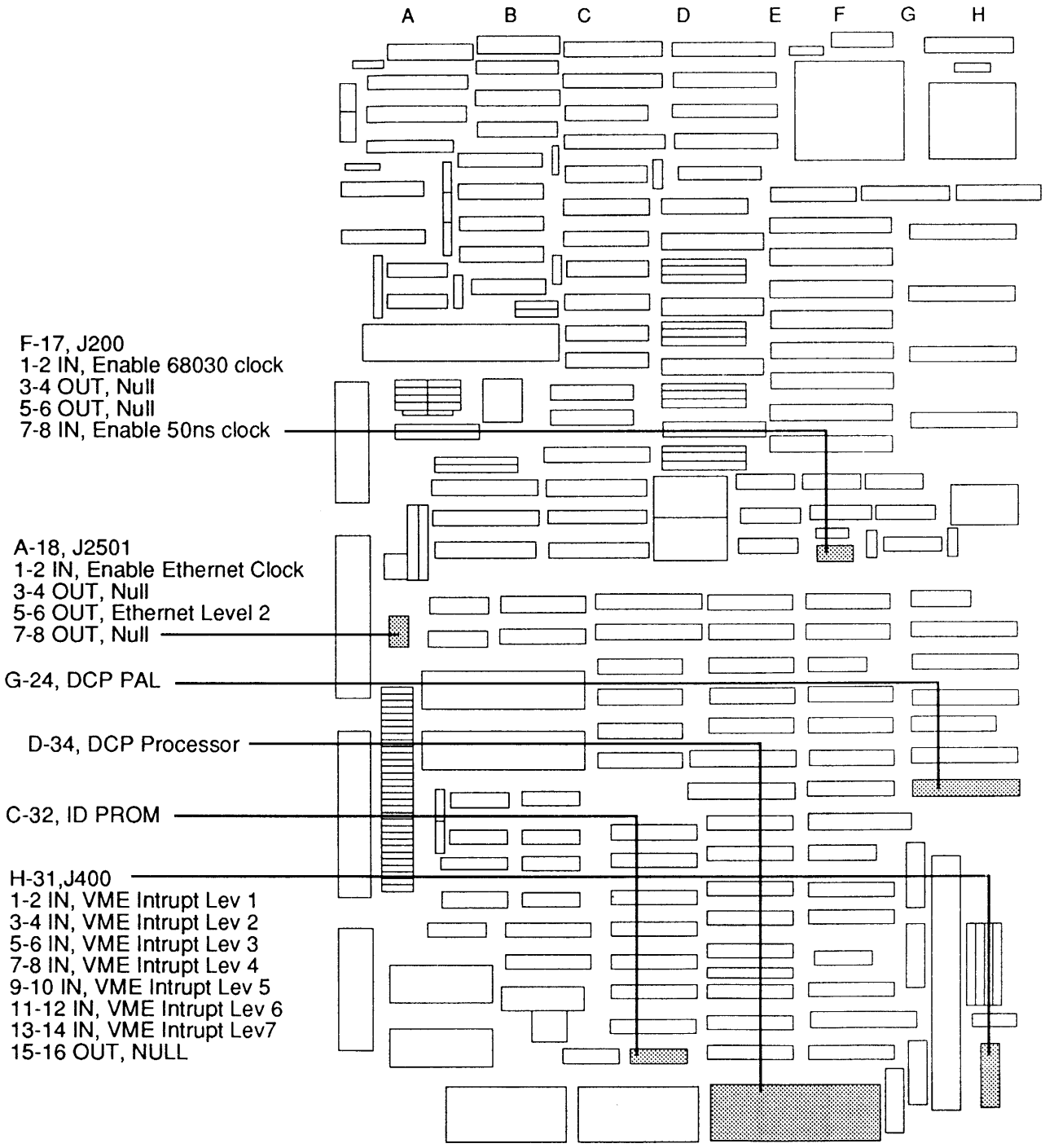
To configure the 8MB memory board refer to the *Sun 501–1102 Memory Board Configuration Procedure*, P/N 813–2018.

For information on configuring the 23MB memory board, please refer to the *Installation Notes for the 32 Mbyte Memory Board*, P/N 800–2123.

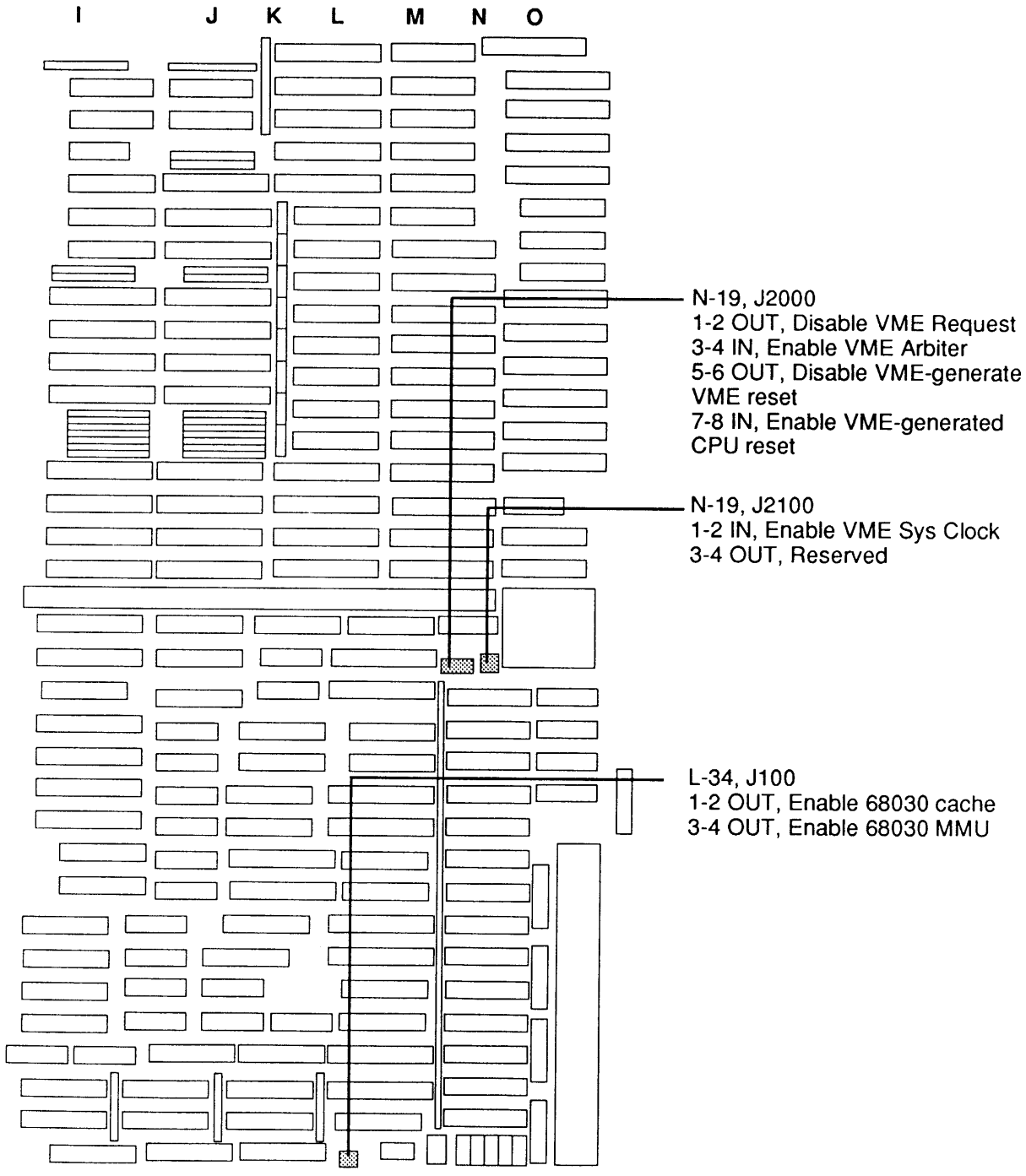
Table 1-1 *Factory Configuration of Jumpers on the 3400 CPU Board*

Jumper Configuration			
Jumper	**Location**	**Configuration**	**Description**
J100	L–34	1–2, OUT	Enable cache on 68030 (IN = Disable...)
J100	L–34	3–4, OUT	Enable MMU on 68030 (IN = Disable...)
J200	F–17	1–2, IN	Enable 68030 clock
J200	F–17	3–4, OUT	Null
J200	F–17	5–6, OUT	Null
J200	F–17	7–8, IN	Enable 50ns clock
J400	H–31	1–2, IN	VME Interrupt Level 1
J400	H–31	3–4, IN	VME Interrupt Level 2
J400	H–31	5–6, IN	VME Interrupt Level 3
J400	H–31	7–8, IN	VME Interrupt Level 4
J400	H–31	9–10, IN	VME Interrupt Level 5
J400	H–31	11–12, IN	VME Interrupt Level 6
J400	H–31	13–14, IN	VME Interrupt Level 7
J400	H–31	15–16, OUT	Null
J2000	M–19	1–2, OUT	Disable VME Requestor
J2000	M–19	3–4, IN	Enable VME Arbiter
J2000	M–19	5–6, OUT	Disable VME–generated VME reset
J2000	M–19	7–8, IN	CPU–generated VME reset
J2100	N–19	1–2, IN	Enable VME Sys Clock
J2100	N–19	3–4, OUT	Reserved
J2501	A–18	1–2, IN	Enable Ethernet Clock
J2501	A–18	3–4, OUT	Null
J2501	A–18	5–6, OUT	Ethernet Level 2 (IN = Level 1)
J2501	A–18	7–8, OUT	Null

Figure 1-1 *Section A-H of the Board*

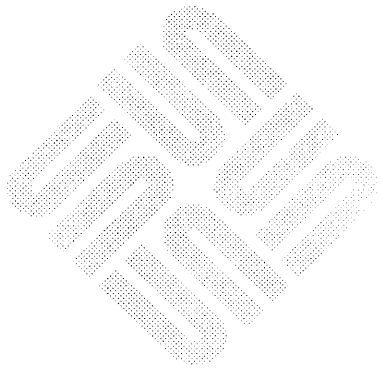


Section I-O of the Board Figure 1-2



Revision History

Revision	*Dash Number*	*Date*	*Comments*
01	**01**	11 April 1988	Alpha Review Draft
02	**02**	3 October 1988	Second Review Draft.
50	**03**	14 November 1988	Beta Review and Engineering Release.
50	**04**	23 January 1989	Review Draft.
50	**05**	29 January 1989	Beta Draft
A	**10**	17 April 1989	Released for customer shipment
A	**11**	15 May 1989	FCS



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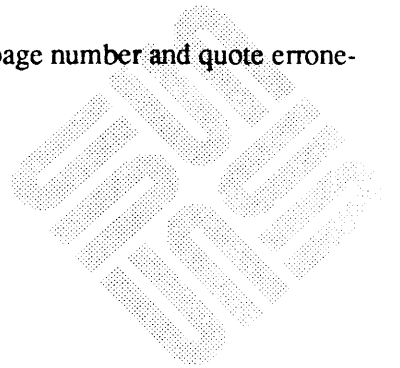

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Revision A of 15 May 1989

Content

Did this manual meet your needs? If not, please indicate what should be changed, added, or deleted in order to meet your needs. Please comment if you believe other information should be included in this manual. Also please advise us if you are aware of information in other manuals that would be more convenient if it were included in this manual.

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