800-1034-01

Micropolis Corporation
21123 Nordhoff Street
Chatsworth, CA 91311
(213) 709-3300 Telex 651486

To All Micropolis Model 1300 Customers:

Congratulations! You have received the most advanced 5¼" Winchester disk drive available today - the Micropolis Model 1300. It includes the following features:

- Industry standard appearance, mounting, and interface (ST 506/412 compatible).
- 33 msec (including settling) average seek rate.
- All DC operation and low power consumption (+5 VDC, +12 VDC).
- Fully shock mounted and isolated Head/Disk Assembly for protection against head/media damage and easy system integration. Please refer to the Product Description for important information regarding handling of the 1300.
- Capacity of 17, 34, 51.9 Mbytes.

I have included a complete set of documents to assist you in your evaluation of the Model 1300. As in the past, Micropolis is ready to assist our customers in any way possible. If you need additional information or assistance, please do not hesitate to contact me at:

(213) 709-3300

Thank you for your order.

Bob Rauch
Technical Support Manager

BR/dsm

MICROPOLIS™

Model 1304 51.9 MB

1300 Parts List

The following are the field-replaceable parts of the 1300 Rigid Disk Drive.

Preamplifier PCBA (including flex cable)	101182-01-2
Device Electronics PCBA	101242-01-4
Motor Control PCBA	101232-01-5
Shipping Kit	101019-01-6
Device Assembly, 4 Disk	101004-01-8
Bezel	101190-01-5
Terminator Pack (220/330 ohm SIP)	116-0011-1
2-Pin Jumper	680-0204-7
Solenoid Assembly	101010-01-5
Brake Arm Assembly	101011-01-3
Frame	101104-01-6

PRODUCT DESCRIPTION

Rigid Disk Drive - MODEL 1300

DOCUMENT NO.
101000A

February, 1983

MICROPOLIS CORPORATION
21123 NORDHOFF STREET, CHATSWORTH, CALIFORNIA, 91311
(213) 709-3300 TELEX: 651486

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SECTION 1 - INTRODUCTION

1.1 General Information

Applications requirements for high performance, high capacity, random access data storage are best met by the Micropolis 1300 family of Winchester-technology 5 1/4-inch disk drives. Important applications include:

- Multi-user Systems
- Multi-tasking Systems
- Digital/Voice PBX
- Local Area Networks
- Distributed Processing
- CAD/CAM Systems

Important Features	Real Benefits
Industry Standard ST506 Interface 5 1/4-inch flexible disk form-factor and mounting DC voltages	Ease of Integration Uses existing controllers Fits current system package Uses existing power supplies
Design Reliability Integral shock and vibration isolators Data-free landing zone, automatic positioner lock & spindle brake Clean area free of active components Oxide media Balanced rotary positioner	Product Integrity Eliminates major source of media damage due to handling and transportation abuses and harsh usage Positive media protection 25,000 hours HDA MTBF Proven performance, volume availability Improved shock & vibration immunity; unrestricted mounting orientation as compared to linear positioners
High Performance Voice-coil positioner with automatic velocity profiling Step pulse buffering	High system throughput 33 msec. average seek time Optimal system performance through overlapped seeks and high speed step pulsing
High Capacity	Up to 200 MBytes per controller using four drives
Serviceability Simple PCBA replacement No adjustments	Low cost of ownership Minimal technician training No special tools required MTTR less than 15 minutes
Micropolis Total Experience	
Manufactured by established, volume producer of high performance disk drives	Reliable delivery in OEM volumes
Proven technology for tomorrow's requirements	Long life plus continuing cost/performance improvement
Experienced technical and applications back-up	Total customer support

SECTION 2 - DESCRIPTION

2.1 General

The Model 1300 drive is comprised of a PCBA package and a mechanical assembly. These components perform the following functions:

a. Interpret and generate interface control signals.
b. Sequence the drive to the Ready state.
c. Position the read/write heads on the desired track.
d. Read and write data.

2.2 Mechanical Assembly

The Model 1300 drive's mechanical assembly is composed of a Head/Disk Assembly (HDA) and an outer chassis (Frame).

a. The HDA is comprised of a die-cast structure containing all of the drive's mechanical components. An aluminum cover seals the opening in the casting to create a "clean" area. Included in the clean area are the recording heads, platters, and voice-coil motor. Air is circulated throughout the clean area by disk rotation induced flow. The flow is directed through a 0.3 micron absolute filter. The sealed area breathes to the outside via a similar filter for pressure equalization.

   There are no active electronic parts within the clean area. Electrical connection is made between this area's components and the electronics package via flexible circuits.

b. The HDA is suspended within a die-cast outer Frame on shock mounts. This method of suspension isolates the HDA, with all its mechanical components, from mounting related distortion, stress, shock, and vibration.

2.2.1 Drive Motor

Rotational drive for the platters is provided by a direct-coupled, brushless, DC motor. This combination provides a very low profile, allowing up to four platters to be packaged in an envelope only 3 1/4 inches high. Switching information for the electronic commutator is supplied by three Hall-effect sensors mounted within the drive motor assembly. A drive motor brake is provided to quickly stop the spindle when power is removed from the drive.

2.2.2 Positioner System

The positioner is a balanced voice-coil/swing-arm mechanism. The voice coil is attached to the system on the opposite side of the bearings from the heads, and the whole mechanism is statically balanced. This balancing provides the positioner with immunity to external shock forces.

The voice-coil motor is of the short-coil/long-magnet type. Position reference is made to tracks recorded on a dedicated servo surface on the platter nearest the HDA die-cast base. These tracks are recorded with position information in a "Modified Dibit" format.

When power is removed from the drive, the positioner is automatically retracted to the landing zone and a positioner latch is activated to prevent the positioner from moving. Therefore, no operator intervention is necessary when shipping the drive or the equipment in which the drive is installed.

2.2.3 Read/Write Heads

This assembly consists of a slider of the Winchester type with the slider surface designed to run at 3600 RPM.

2.3 Electronics Package

a. The Preamplifier Assembly provides:

1. Termination for the head flexible circuits as they exit the HDA clean area, and interconnection with the rest of the electronics package.
2. Head selection (from the 2, 4, or 6 data heads).
3. Read preamplification.
4. Write current drivers.
5. Servo preamplification.
6. Fault detection circuitry.

b. The Motor Control board provides:

1. Spindle motor drive circuits.
2. Positioner power amplifier circuits.

c. The Device Electronics board provides:

1. Write logic circuits.
2. Read amplifier and peak detection circuits.
3. Servo electronics, which includes a signal amplifier AGC and a modified dibit demodulator.
4. Microprocessor-based control logic, which includes velocity profile generation and drive sequencing.
5. Interface drivers and receivers.
6. A digital processing gate array which provides speed control circuits and servo demodulator control signals.
7. Power sensing circuits.

2.4 Indicators

A Light Emitting Diode (LED) is provided on the front of the bezel. The LED is illuminated when the drive is selected.

SECTION 3 - SPECIFICATIONS

3.1 Performance Specifications

Unformatted Capacity (Includes all physical tracks)

MODEL NO.	1302	1303	1304
Disks	2	3	4
Data Surfaces	2	4	6
Data Heads	2	4	6
Bytes per Track	10,416	10,416	10,416
Tracks Per Surface	830	830	830
Physical Tracks	1660	3320	4980
M Bytes Per Surface	8.65	8.65	8.65
Unit Total M Bytes	17.3	34.6	51.9
Transfer rate - M Bits/second	5.00	5.00	5.00

Formatted Capacity (MFM - 32 Sectors) (Includes all physical tracks)

MODEL NO.	1302	1303	1304
Bytes per Sector	256	256	256
Bytes Per Track	8192	8192	8192
M Bytes Per Surface	6.8	6.8	6.8
Unit Total M Bytes	13.6	27.2	40.8

Formatted Capacity (MFM - 33 Sectors) (Includes all physical tracks)

MODEL NO.	1302	1303	1304
Bytes per Sector	256	256	256
Bytes Per Track	8448	8448	8448
M Bytes Per Surface	7.01	7.01	7.01
Unit Total M Bytes	14.02	28.05	42.07

Start Time: 25 sec, maximum

Stop Time: 20 sec, maximum

Seek Time (includes settle time) *

Track to Track	7 ms
Average Seek Time **	33 ms
Full Stroke	66 ms
Average Latency	8.3 ms

* Step pulses transmitted to drive at 20 usec rate or faster.

** Average seek time is the time taken to perform all possible seeks divided by the number of seeks.

3.2 Functional Specifications

Encoding Method	MFM
Recording Density (bpi)	9400
Flux Density (frpi)	9400
Spindle Speed (rpm)	3600
Speed Variation (%)	±0.5
Track Density (tpi)	960
Cylinders	830

3.3 Physical Specifications

3.3.1 Mechanical Dimensions

Depth	8.00" (203 mm)
Width	5.75" (146 mm)
Height	3.25" (82.6 mm)
Bezel Width	5.88" (149 mm)
Bezel Height	3.375" (85.7 mm)
Weight	6.0 lbs (2.7 kg) nominal

3.3.2 Media Dimensions - Oxide coated disks (IBM 3350 technology)

Outside Diameter	5.118" (130 mm)
Inside Diameter	1.575" (40 mm)
Thickness	0.075" (1.9 mm)

3.3.3 Environmental

	Operating	Storage
Ambient Temperature	10° to 45°C	-40° to 65°C
Relative Humidity	10% to 80% non-condensing	10% to 80% non-condensing
Thermal Shock	1°C/5 Minutes	24°C/Hour
Altitude	-200 ft to 7000 ft	N/A

3.3.4 Dissipation (typical)

	Stand-by		Positioning	
	Watts	BTU/hr	Watts	BTU/hr
1302	22	75	30	102
1303	24	82	32	109
1304	26	89	34	115

3.3.5 Vibration

Operating:

5-40 Hz	0.006 inches, peak-peak
40-300 Hz	0.5 G peak

Non-operating:

Packaged

5-10 Hz	0.2 inches, peak-peak
10-44 Hz	1 G peak
44-98 Hz	0.01 inches, peak-peak
98-300 Hz	5 G peak

Unpackaged

5-31 Hz	0.02 inches, peak-peak
31-69 Hz	1 G peak
69-98 Hz	0.004 inches, peak-peak
98-300 Hz	2 G peak

3.3.6 Shock

Operating:

1/2 Sinusoidal pulse

5 msec	3 G peak
20 msec	1 G peak

Non-operating:

Packaged

Free-fall drop	36 inches	
1/2 Sinusoidal	20 msec duration	50 G max

Unpackaged

Free-fall drop	0.75 inches	
Topple test	1.5 inches	
1/2 Sinusoidal	5 msec duration	40 G max
	11 msec duration	20 G max
	20 msec duration	15 G max
	50 msec duration	15 G max
	100 msec duration	20 G max

3.3.7 Acoustic Noise: Less than 51 dPA

3.3.8 Reliability Specifications

Soft Read Errors	1 in 10^{10}
Hard Read Errors	1 in 10^{12}
Seek Errors	1 in 10^{6}
Unit MTBF	13,000 Power-On Hours
HDA MTBF	25,000 Power-On Hours
MTTR	Less than 15 minutes

3.4 DC Power Requirements (each module)

Voltage *	Average Current 1302	1303	1304	Peak Current	Ripple
+5V ±5%	0.9A	0.9A	0.9A	0.9A	2% Max.
+12V ±5%	2.5A	2.65A	2.8A	3.5A	2% Max.
* Voltages to be measured at the power connector on the drive.					

Voltages may be applied to the drive in any sequence. The rise time of the +5V must be less than 50 milliseconds for proper operation of the power-on reset circuits on the Device Electronics board, which are based on the +5V.

3.5 Mounting

The Model 1300 drive utilizes industry-standard mounting techniques for 5 1/4-inch Winchester disk drives (which are the same as for the 5 1/4-inch flexible disk drives). Figure 3-1 shows the mounting hole locations. Recommended orientation is either vertical on either side or horizontal with the circuit board down.

3.5.1 Cooling

The enclosure and mounting structure must be designed to allow natural convection of heat by permitting the free flow of air around and between the printed circuit boards. If the enclosure is small or if natural convection is restricted, a fan may be required.

A Model 1304 drive typically dissipates 26 watts (89 BTU/hr) in stand-by mode and 34 watts (115 BTU/hr) while positioning. This heat must be removed from the enclosure at a rate sufficient to maintain the ambient temperature around the drive at or below 45°C (113°F).

3.5.2 Shock Protection

Model 1300 drives employ contact start-stop (Winchester) head and disk technology. The drives use very low-mass heads, and each head is lightly preloaded against an air bearing by low-rate spring suspensions. The heads rest on the lubricated disk surface when the drive is stopped.

If the drive is subjected to shock in excess of the specified maximum value, the heads may lift from the disk surface and return with sufficient force to cause damage. The head material is a very hard grade of ferrite, while the disk surface is coated with a comparatively soft ferrous-oxide.

Both the head and disk surfaces are polished to a mirror-like finish, and any damage to these surfaces will nearly always result in degraded read/write performance.

To protect against such media damage, Model 1300 disk drives incorporate an HDA which is shock isolated from the outer Frame. This suspension system is adequate to protect the heads/disks from shock forces resulting from toppling the drive onto a hard surface with any end raised to a height of 1.5 inches.

For additional protection, an area of the disk, not used for data storage, is reserved for "landing" the heads. Whenever power is removed from the drive, the heads are automatically returned to this landing zone. An automatic latching mechanism then locks the positioner in place.

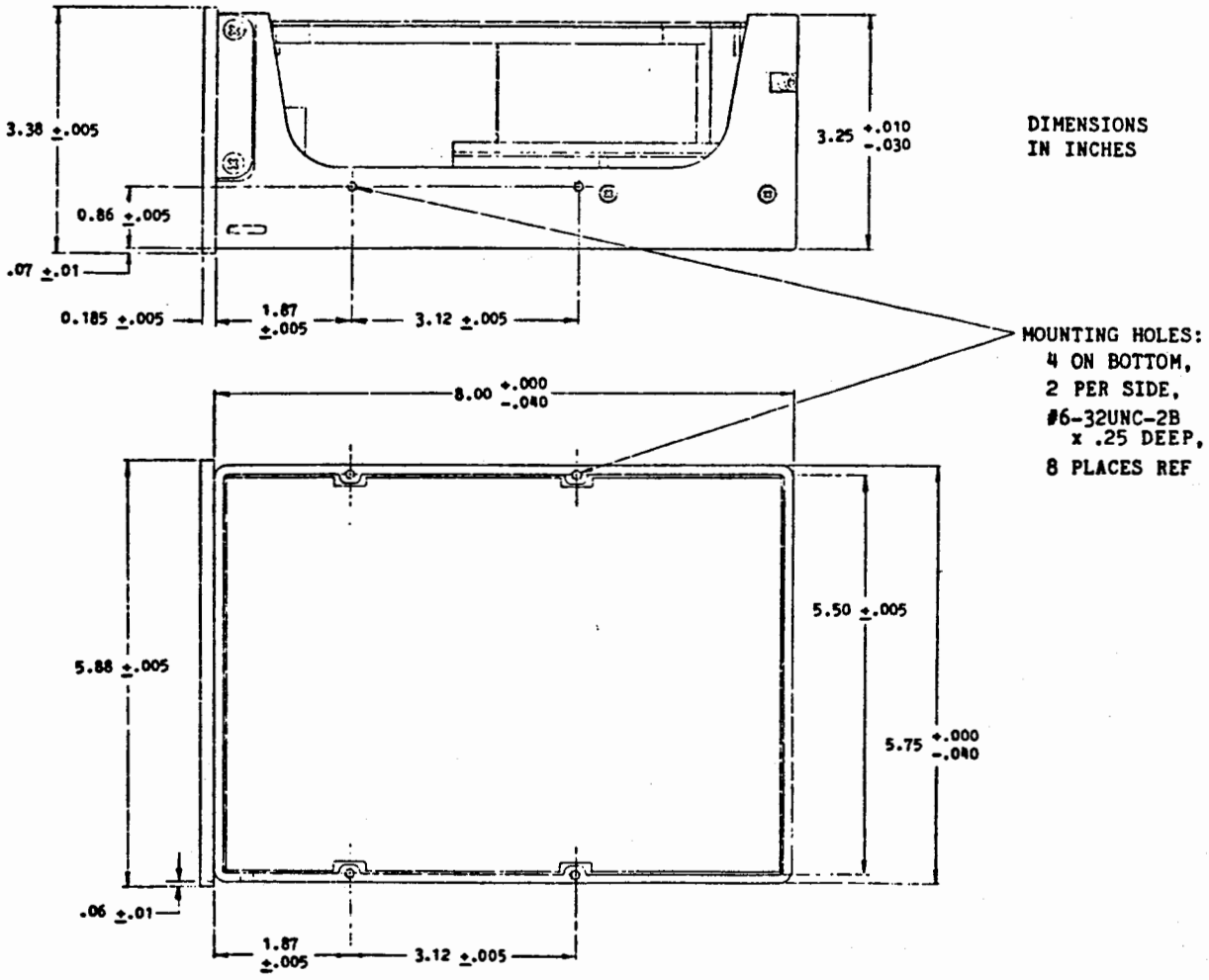


Figure 3-1. Dimensions & Mounting

SECTION 4 - MEDIA DEFECTS AND ERRORS

4.1 Introduction

In high density recording storage systems it is necessary to increase reliability and improve operational performance by providing an error detection and correction scheme.

For disk storage systems, the predominant error pattern is a burst of errors occurring on one or more tracks. Errors may be drop-outs (missing bits), drop-ins (extra bits), or bits shifted from their nominal position beyond the tolerance of the data separator.

Errors may be caused by defects or imperfections in the disk media, by a marginal system signal-to-noise ratio, or by mis-positioning of the read/write heads during reading.

4.2 Error Definition

An error is defined as any discrepancy between recovered data and true, correctly recorded data.

a. An error may be an extra bit or a missing bit (i.e., a "zero" can be transformed into a "one," or a "one" can be changed to a "zero"). Bits may also be shifted from their nominal positions in the data stream due to pulse superposition, disk speed variation, or random noise.

b. Errors may be classified as "hard" or "soft" errors. A read error which is not recoverable within six retries (re-reads) is considered a hard error, otherwise it is a soft error. Hard errors are usually a result of media defects.

The error rates for soft and hard errors other than media defects are given in Section 4.8.

4.3 Media Defect Definition

Most errors resulting from media defects are classified as hard errors. They are attributable to small imperfections in the oxide coating of the disk. Examples are an impurity within the oxide itself or a microscopic scratch on the surface of the oxide coating.

As the storage density of information increases, these defects become more apparent to the system. Winchester technology uses a higher bit packing ratio (5000 to 10000 bpi) than older disk technologies, and is more susceptible to this type of error.

Some media defects may be ignored if they reside in unused areas of the format. For used areas that contain media defects, alternate track/sector locations must be allocated and the defective areas avoided. The defect handling scheme selected depends upon the level of sophistication of the host controller/software.

4.4 Media Defect Identification

Each drive is tested on a media test system during the manufacturing process. This test system exercises the drive under extreme marginal conditions and identifies the location of media defects. All media defects identified are logged in a defect map. This map is recorded on a printout which is shipped with each drive. The defective areas will be identified by cylinder and head address, number of bytes from index, and number of bits in length.

The defect map, accompanying each drive, typically provides the locations of more defects than will be detected by the user system. There are situations, however, when a magnetic anomaly in the disk coating or extra defects caused by improper handling may cause a bit shift that is unique to a particular format or bit pattern. This bit shift will manifest itself as a hard error in addition to those reported in the defect map. If this occurs, it is recommended that this error location be added to the defect map and mapped out.

4.5 User Defect Mapping

The user system should be capable of mapping the defects as listed on the defect map and should include any additional hard errors found during the user's functional test. One method of mapping is to create a defect directory at Cylinder Ø. This directory would then contain the locations of all defective areas, as well as alternate sector/track assignments for those areas.

4.6 Defect Acceptance Criteria

There will be no more than 20 tracks with defects per surface, of which no more than four tracks will contain multiple defects. Also, Cylinder Ø is guaranteed to be defect free.

A single defect is defined as a media defect less than two bytes long. A multiple defect is defined as a media defect greater than two bytes long, or more than one single defect in the same track.

4.7 System Generated Errors

It should be noted that errors, in addition to those which are drive related, may be present as a result of system electrical noise. This noise may be due to marginal timing conditions, ground loops in the DC power distribution cables, or faulty controller power sequencing.

4.8 Error Rate Definition

4.8.1 Soft Errors

The soft error rate of 1 in 10^{10} is defined as the probability that any bit read is in error excluding retries or error correction, given that all known defects have been eliminated.

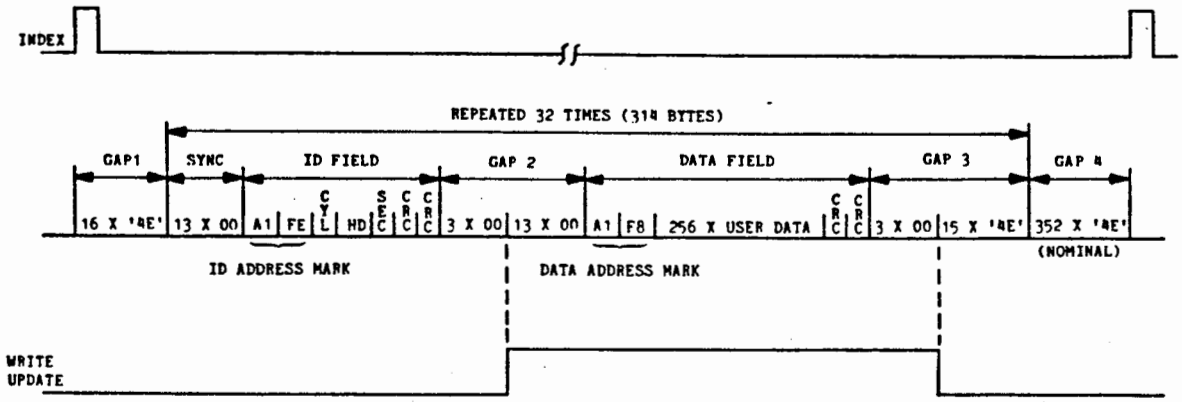
4.8.2 Hard Errors

The hard error rate of 1 in 10^{12} is defined as the probability that any bit written cannot be recovered including retries, given that all known defects have been eliminated. Retries consist of re-read attempts but not error correction. Such hard errors may result from remnant particle defects, noise transients, etc.

To minimize the effect of hard errors, each write operation should be followed by a read-after-write verification, and any failing sectors be re-written.

5.1 General Information

The purpose of a format is to organize a data track into smaller, sequentially numbered blocks of data called sectors. The Model 1300 drive is designed to use a soft-sectored format. In a soft-sectored format, the beginning of each sector is defined by information recorded on the disk. This information is referred to as the Identification (ID) field of the sector and typically contains the sector address, cylinder address, and head address. Additional information such as flags for defect handling may also be included. The ID field is followed immediately by the user data field. Figure 5-1 illustrates a widely used format for 5 1/4-inch Winchesters.



NOTES:

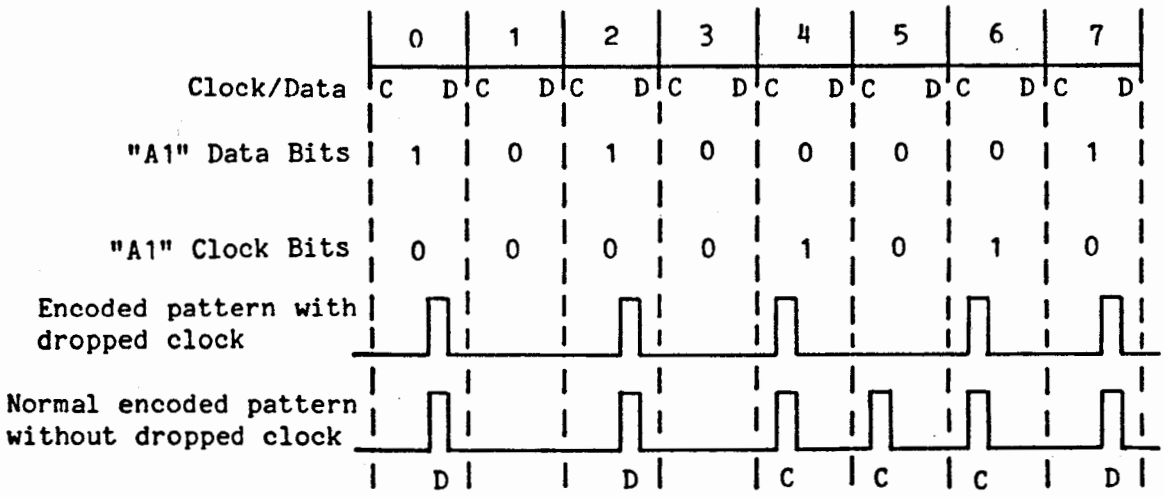
1. Nominal track capacity = 10416 bytes
2. Total data bytes/track = 256 x 32 = 8192
3. CRC Fire Code = $X^{16} + X^{12} + X^{6} + 1$
4. Bit 7 of the head byte ID Field = 1 in a defective sector (Cylinder Ø is error free).
5. Bit 5 of the head byte is reserved for numbering cylinders greater than 256.
6. Bit 6 of the head byte is reserved for numbering cylinders greater than 512.

Figure 5-1. Typical Track Format

The soft-sectored format of Figure 5-1 is a slightly modified version of the IBM System 34 format, which is commonly used on flexible disk drives. The encoding method used is modified frequency modulation (MFM).

a. Each track is divided into 32 sectors, and each sector has a data field 256 bytes long.

b. The beginnings of the ID field and the data field are flagged by unique characters called address marks. An address mark is two bytes long. The first byte is an "A1" data pattern. This is followed by either an "FE" pattern (which is the pattern used to define an ID address mark), or an "F8" pattern (which is the pattern used to define a data address mark). The "A1" pattern is made unique by violating the encoding rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination, see Figure 5-2.



C = clock bit
D = data bit

Figure 5-2. "A1" Address Mark Byte

c. Each ID and data field is followed by a 16-bit Cyclic Redundancy Check (CRC) used for data verification. Each CRC polynomial is unique for a particular data pattern.

d. Surrounding the ID field and the data field are gaps to establish physical and timing relationships.

5.2 Format Parameters

This section gives a detailed description of the format shown in Figure 5-1 and describes the drive-related parameters necessary to design a format.

One of the most important drive parameters related to the design of a disk format is the spindle speed tolerance. The format shown in Figure 5-1 was designed for ±3% speed variation. With the ±0.5% speed tolerance of the Model 1300 drive, it is possible to design a more efficient format; i.e., 33 sectors of 256 bytes.

5.2.1 Gap 1

Gap 1 provides for variations in Index detection. The 16 bytes shown in Figure 5-1 relates to the tolerance associated with the magnetic index transducers used in lower technology drives. In the 1300 series drive, Index is derived from information recorded on the servo disk, and requires a tolerance of only ±1 byte.

Gap 1 may also be used as a head switching recovery period so that when switching heads, sequential sectors may be read without waiting a rotational latency time. In this event, an additional five bytes (corresponding to the 8-microsecond head switching time) should be added to the Index tolerance.

5.2.2 Sync

The Sync field contains 13 bytes of zeroes, which are used to synchronize the phase-locked loop and address mark circuitry in the data separator. The minimum length of the Sync field is determined by the lock-up characteristics of the data separator in the host controller.

5.2.3 ID Field

The sector identification field contains information to associate a unique address with the data field which immediately follows. The beginning of the ID field is defined by the ID address mark, in which the A1 byte is specially encoded.

The ID field contains cylinder, head, and sector address information and a two byte check field for error detection purposes. In the format shown, the check field is a standard 16-bit CRC, although a longer ECC code may be used.

5.2.4 Gap 2

Gap 2 separates the ID field from the data field and is composed of two areas. The three zero bytes, following the ID field check bytes, are referred to as the ID field postamble. When the data field is written, WRITE GATE should not be enabled until the end of this postamble, thereby protecting the ID field check bytes. The area where WRITE GATE is enabled is referred to as the write splice and is approximately one byte in length.

Following the write splice is a field of 12 zero bytes used to synchronize the data separator as described in Section 5.2.2.

5.2.5 Data Field

The data fields contains user data.

The beginning of the data field is defined by the data address mark in which the A1 byte is specially encoded.

Following the data bytes (256 bytes in this example) is the check field. In the format shown, the check field consists of a 16-bit CRC check. Depending upon the level of system sophistication, improved performance may be achieved by use of a longer error correcting code for the check field.

5.2.6 Gap 3

Gap 3 provides a 3-byte postamble for the data field, which protects the data field check bytes when WRITE GATE is turned off after a data field write.

Gap 3 also provides a speed tolerance gap which prevents overwriting the ID field of the following sector when a data field is written. The minimum length of this gap is computed as:

$$N \times 2 \times (ST + WOT)$$

Where ST = spindle speed tolerance
WOT = write oscillator tolerance
N = number of bytes recorded in the sector update, which in turn is calculated as follows

Example (256-byte sector):

13	data field sync
2	data address mark
256	data
2	check field
3	postamble

276	

For example, assuming a 0.1% write oscillator tolerance and a 0.5% speed tolerance, the minimum Gap 3 tolerance would be

$$276 \times 2 \times (.005 + .001) = 3.3 \text{ bytes}$$

In practice, a longer Gap 3 tolerance is generally allowed to increase system reliability.

If the system design requires the ability to write physically adjacent sectors, Gap 3 must be increased by five bytes to allow for the 8-microsecond, read-after-write recovery time of the read channel.

5.2.7 Gap 4

Gap 4 is the speed tolerance area for the entire track, applicable when formatting the full track. This gap aviods overflowing the Index area in track formatting operations. The actual length of the gap depends upon the actual spindle speed during the format operation, which begins writing with the first Index encountered and ends with the next Index.

$$\text{Gap 4} = (10416) \times (\text{ST} + \text{WOT}) + 2 \times (\text{Index tolerance})$$

For example, assuming WOT = 0.1%, ST = 0.5%, and Index tolerance = 1 byte (see Section 5.2.1), then

$$\text{Gap 4} = (10416) \times (.005 + .001) + (2) \times (1) = 64 \text{ bytes}$$

In designing a format, the usable disk area available for recording sectors is 10416 minus Gap 4.

5.3 Write Precompensation

Whenever two bits are written in close proximity to each other, a phenomenon called pulse superposition occurs, which tends to cause the two bits to move away from each other. This is a large factor of bit shift. Other phenomena such as random noise, speed variations, etc., will also cause bit shift, but to a lesser degree. Bit shift is more apparent on the innermost tracks, due to pulse crowding.

The effect of bit shift can be reduced by a technique called write precompensation. By detecting which bits will occur early and which bits will occur late, precompensation is performed by writing these bits in the opposite direction of the expected shift.

To achieve the specified error rates for the drive, the system must provide write precompensation as follows:

a. The optimum amount of write precompensation is twelve nanoseconds for both early and late written bits.

b. Bit shift is more apparent on the inner data tracks due to pulse crowding; thus, write precompensation should be applied to data on track numbers greater than 400.

While details of the precompensation generator are at the discretion of the system designer, the following notes are provided for guidance purposes to illustrate the required precompensation algorithm.

a. Table 5-1 shows the data bit patterns, the expected bit shift direction, and the write precompensate direction and type of pulse to write for MFM recording.

b. The write bits are shifted through a 4-bit shift register to detect those patterns requiring precompensation and to determine what type of pulse to write. Data or Clock pulses are then written on the disk according to the rules for MFM recording, and are written either on time, early, or late in the cell period according to the direction of the expected shift. Timing is such that the cell period for a pulse starts when the Data bit is shifted into Position 3 and ends when the bit is shifted into Position 4.

Table 5-1. Precompensation Values

Data Pattern				Expected Shift Direction of Pulse for Cell 2*	Precompensate Direction and Pulse for Cell 2*
4	3	2	1		
0	0	0	0	None	On Time, Clock Pulse
0	0	0	1	Late	Early, Clock Pulse
0	0	1	0	None	On Time, Data Pulse
0	0	1	1	Early	Late, Data Pulse
0	1	0	0	None	No Clock or Data Written
0	1	0	1	None	No Clock or Data Written
0	1	1	0	Late	Early, Data Pulse
0	1	1	1	None	On Time, Data Pulse
1	0	0	0	Early	Late, Clock Pulse
1	0	0	1	None	On Time, Clock Pulse
1	0	1	0	None	On Time, Data Pulse
1	0	1	1	Early	Late, Data Pulse
1	1	0	0	None	No Clock or Data Written
1	1	0	1	None	No Clock or Data Written
1	1	1	0	Late	Early, Data Pulse
1	1	1	1	None	On Time, Data Pulse

* Determination of pulse and precompensation is made in Cell 2; the pulse is actually written from Cell 3.

SECTION 6 - ELECTRICAL INTERFACE

6.1 Introduction

The electrical interface to the Model 1300 drive is pin and function compatible with the industry standard for 5 1/4-inch Winchester disk drives. Electrical connection is made via four connectors, which are accessible at the rear of the drive enclosure (see Figure 6-4). Connectors J1 and J2 provide signal interconnection between the drive and host controller, J3 is the DC power connector, and J4 provides for grounding to the system.

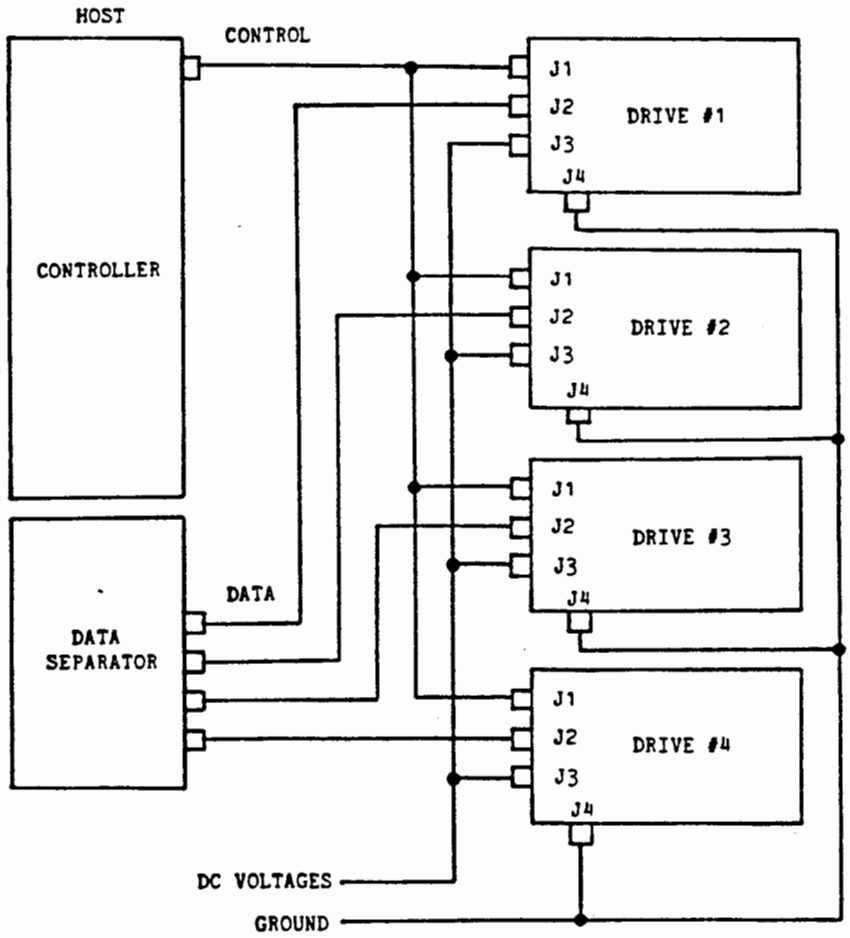


Figure 6-1. System Configuration/Cabling

6.2 Control Signal Connector J1 (see Figure 6-4)

The Control Signal connector is a 34-pin PCBA edge connector, which contains control and drive status signals. Up to four drives may be connected to a single host controller/formatter; the signals on J1 provide drive selection as well as control functions for the selected drive.

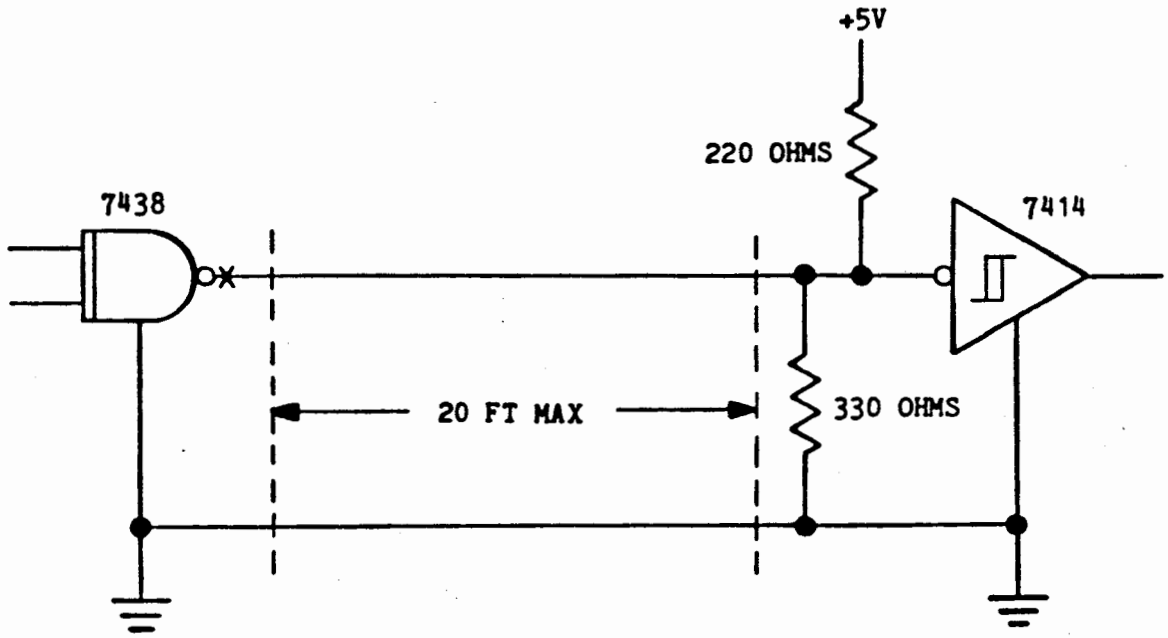
Table 6-1 lists the Control Signals, and Figure 6-2 summarizes the electrical characteristics of each signal. These TTL signals are low true (indicated by "/") and have the following logic levels:

True = 0V to +0.4V @ 48 ma (maximum)
False = +2.5 to +5V @ 250 ua (open collector)

The termination network in the drive is mounted in a socket on the Device Electronics board. In multiple drive systems, it should be installed in the last drive only.

Table 6-1. Control Signal Connector J1 - Pinouts

J1 Connector Pin Signal	J1 Connector Pin Ground	Signal Name	Source
2	1	Reserved	-
4	3	HEAD SELECT 2^2/	Host
6	5	WRITE GATE/	Host
8	7	SEEK COMPLETE/	Drive
10	9	TRACK Ø/	Drive
12	11	WRITE FAULT/	Drive
14	13	HEAD SELECT 2^0/	Host
16	15	Reserved (to J2 pin 7)	-
18	17	HEAD SELECT 2^1/	Host
20	19	INDEX/	Drive
22	21	READY/	Drive
24	23	STEP/	Host
26	25	DRIVE SELECT 1/	Host
28	27	DRIVE SELECT 2/	Host
30	29	DRIVE SELECT 3/	Host
32	31	DRIVE SELECT 4/	Host
34	33	DIRECTION IN/	Host
Recommended Cable: 3M Scotchflex 3365/34 Mating Connector: 3M Scotchflex 3463-0001 (key slot between pins 4 and 6)			



NOTES: 1. All signals are low true at the interface and high true into drivers and out of receivers:

True = 0V to +0.4V @ 48 ma max
False = +3V (open)

2. For multiple-drive systems, terminators are installed in last drive only.

Figure 6-2. Control Signal Electrical Characteristics

6.3 Data Transfer Connector J2 (see Figure 6-4)

The Data Transfer connector is a 20-pin PCBA edge connector that contains read data and write data signals. These data signals are differential in nature and are connected radially in multiple-drive systems.

A TTL-level DRIVE SELECTED/ status line is also provided at this connector.

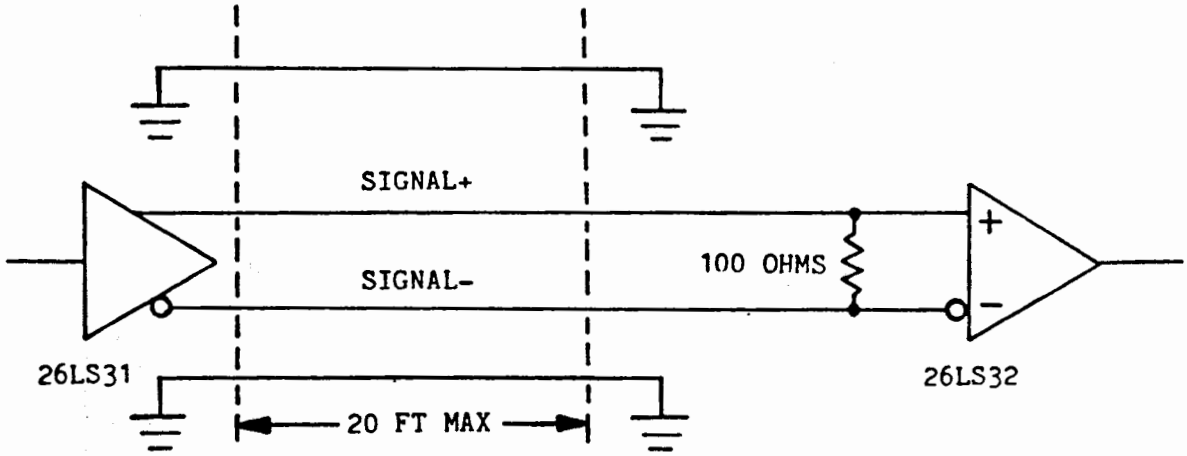
Table 6-2 lists the Data Transfer Signals, and Figure 6-3 shows the electrical characteristics of the differential signals. The differential signals have the following levels (EIA RS-422):

High = +2V
Low = +0.5V

Table 6-2. Data Transfer Connector J2 - Pinouts

J2 Connector Pin		Signal Name	Source
Signal	Ground		
1	2	DRIVE SELECTED/	Drive
3	4	Reserved	-
5	6	Reserved	-
7	8	Reserved (to J1 pin 16)	-
9	10	Reserved	-
-	11	Ground	-
-	12	Ground	-
13	-	MFM WRITE DATA+	Host
14	-	MFM WRITE DATA-	Host
-	15	Ground	-
-	16	Ground	-
17	-	MFM READ DATA+	Drive
18	-	MFM READ DATA-	Drive
-	19	Ground	-
-	20	Ground	-

Recommended Cable: 3M Scotchflex 3365/20
Mating Connector: 3M Scotchflex 3461-0001 (key slot between pins 4 and 6)



NOTES:

1. Drivers/receivers conform to EIA RS-422.

2. All differential signals are high true into drivers and out of receivers. On the interface:

   True = + signal minimum of 0.2V more positive than - signal.
   False = + signal minimum of 0.2V more negative than - signal.

Figure 6-3. Data Transfer Signal Electrical Characteristics

6.4 DC Power Connector J3 (see Figure 6-4)

DC power is applied to the drive through the 4-pin, keyed AMP MATE-N-LOK connector, J3. Pin assignments are shown in Table 6-3. The mating connector is AMP 1-480424-0 utilizing AMP pins P/N 350078-4.

The DC supplies used should be capable of delivering the currents shown in Section 3.4 with a comfortable margin.

Table 6-3. DC Power Pin Assignments

J5 Pin	Voltage	Suggested Wire Size
1	+12 VDC	18 AWG
2	+12 RETURN	18 AWG
3	+5 RETURN	18 AWG
4	+5 VDC	18 AWG

6.5 Ground Connector J4 (see Figure 6-4)

A Ground Connector (AMP 61761-2) is available for connecting the drive's internal ground to the system ground. The recommended mating connector is AMP 62187-1 or equivalent.

Ground Connector J4 is located behind the frame, near the left hand shock mount (as viewed from the rear of the drive).

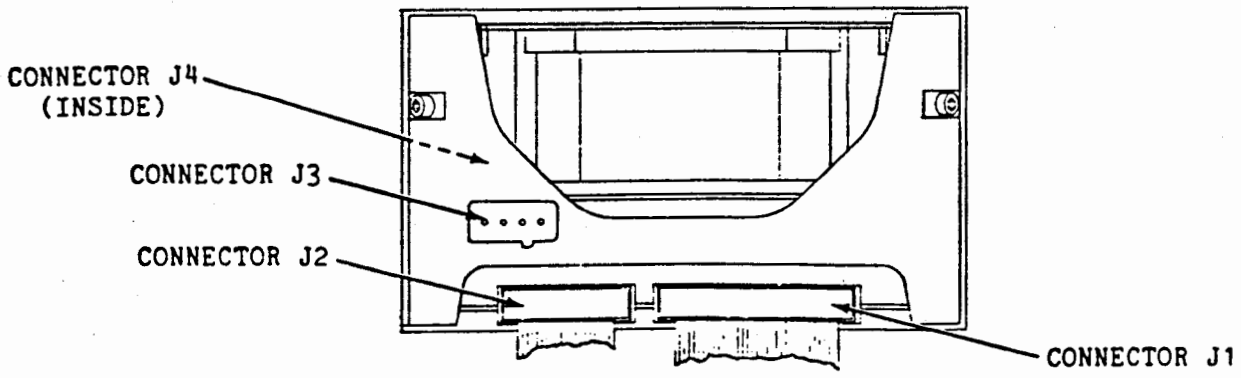


Figure 6-4. Electrical Connection

SECTION 7 - INTERFACE SIGNAL DESCRIPTION

7.1 Control Signal Connector J1 - Input Signals

There are two types of control input signals, those to be multiplexed in a multiple drive system and those that do the multiplexing):

a. The control input signals to be multiplexed are WRITE GATE/, HEAD SELECT 2^0/, HEAD SELECT 2^1/, and HEAD SELECT 2^2/, STEP/, and DIRECTION IN/.

b. The signals to do the multiplexing are DRIVE SELECT 1/, DRIVE SELECT 2/, DRIVE SELECT 3/, and DRIVE SELECT 4/.

7.1.1 DRIVE SELECT 1/ through DRIVE SELECT 4/ (Pins 26,28,30,32)

Each DRIVE SELECT line, when logically true, connects the corresponding drive to the control lines. Only one DRIVE SELECT line may be active at any given time.

Jumpers on the Device Electronics board are used to specify the address of each drive. In multiple drive systems, where several drives are connected to a common controller/formatter, each drive must have a unique address.

7.1.2 DIRECTION IN/ (Pin 34)

This signal defines the direction of motion of the read/write heads when the STEP/ line is pulsed.

a. If DIRECTION IN/ is false, the direction is defined as "out." If a pulse is applied to the STEP/ line, the read/write heads will move away from the center of the disk.

b. If DIRECTION IN/ is true, the direction is defined as "in." If a pulse is applied to the STEP/ line, the read/write heads will move toward the center of the disk.

7.1.3 STEP/ (Pin 24)

This control line causes the read/write heads to move in the direction defined by the DIRECTION IN/ line.

A seek operation is performed by specifying the direction of motion and issuing a sequence of STEP/ pulses, one pulse for each cylinder to be moved. Any change in the DIRECTION IN/ line must be made at least 100 nanoseconds before the leading edge of the first STEP/ pulse. The DIRECTION IN/ line must be stable until after the last pulse of the sequence has been issued.

After the last STEP/ pulse has been issued, the DRIVE SELECT line may be dropped and another drive selected, allowing overlapped seek operations.

Seek operations are performed in a semi-buffered mode. SEEK COMPLETE/ will go false upon receipt of the first STEP/ pulse in a sequence, and the drive will immediately begin seeking. Additional pulses are buffered into a counter, and the heads will move at a rate proportional to the rate of the STEP/ pulses. Maximum performance is achieved when the STEP/ pulses are issued at a rate of 20 microseconds per pulse or less.

When the drive has finished seeking and has settled on track, SEEK COMPLETE/ will go true. The drive is then ready to read, write, or accept another seek command. General seek timing is given in Figure 7-1.

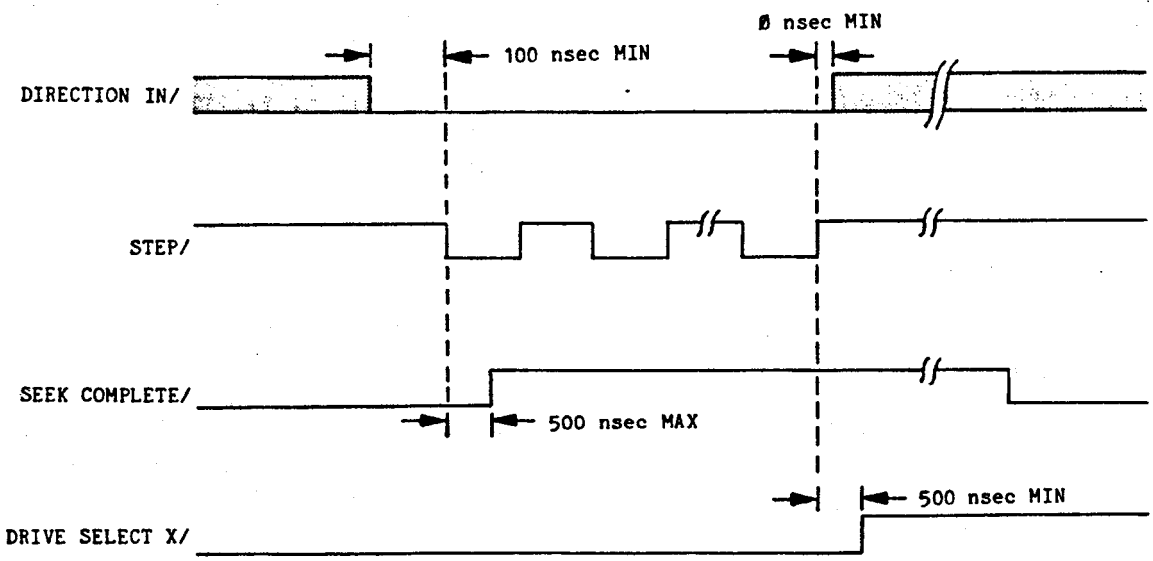
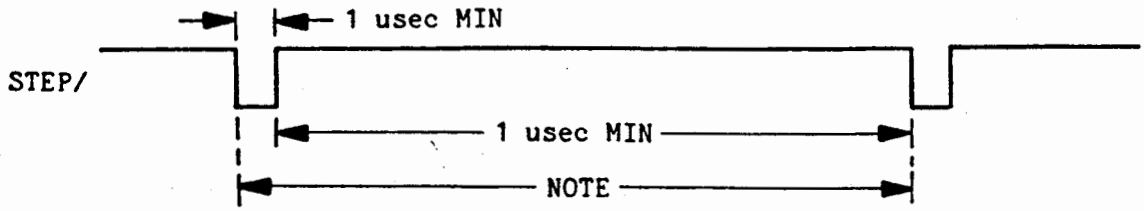


Figure 7-1. General Seek Timing

During a Seek operation, the STEP/ pulses should be issued at a constant rate. This rate must be from 2 microseconds per step to 200 microseconds per step or greater than 1 millisecond per step. Seek accuracy is not guaranteed for step rates between 200 microseconds and 1 millisecond.

STEP/ pulse timing is given in Figure 7-2.



NOTE:

1. The Step rate may be 2 microseconds to 200 microseconds or 1 millisecond or greater.

2. Seek accuracy is not guaranteed for Step rates that are between 200 microseconds and 1 millisecond.

Figure 7-2. Step Pulse Timing

7.1.4 WRITE GATE/ (Pin 6)

When WRITE GATE/ is true, Write Data is recorded on the selected surface. READ DATA is invalid.

When WRITE GATE/ is false, writing is inhibited and data read from the selected surface is transmitted on the READ DATA lines. The WRITE DATA lines must be driven to the inactive state during reading.

Read Data is valid within eight microseconds after WRITE GATE/ goes false after a write operation; see Figure 7-5 for Read/ Write Timing.

7.1.5 HEAD SELECT 2^0/, 2^1/, and 2^2/ (Pins 14,18,4)

These three lines provide for the selection of each individual read/write head in a binary-coded sequence. HEAD SELECT 2^0 is the least significant line. When all three HEAD SELECT lines are false, Head Ø will be selected. Table 7-1 shows the head select sequence for the HEAD SELECT lines (refer to Figure 7-3 for the timing sequences).

Table 7-1. Head Selection

Head Select Line			Data Head Selected		
2^2	2^1	2^0	1302	1303	1304
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	-	2	2
0	1	1	-	3	3
1	0	0	-	-	4
1	0	1	-	-	5
1	1	0	-	-	-
1	1	1	-	-	-

0 = False
1 = True

For 1302 and 1303 drives, a jumper is provided on the Device Electronics board to disconnect the HEAD SELECT 2^2/ from the interface if this line has been dedicated to another function.

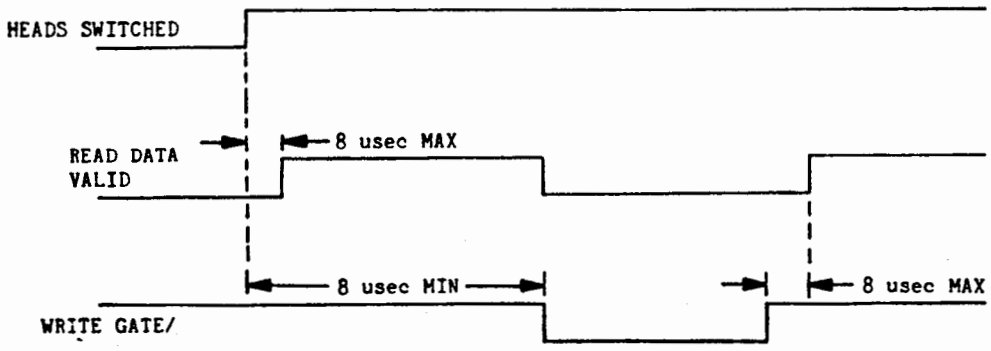


Figure 7-3. Head Selection Timing

7.2 Control Signal Connector J1 - Output Signals

The control output signals are driven with an open-collector output stage capable of sinking a maximum of 48 milli-amps at logical true, with a maximum voltage of 0.4 volts measured at the driver.

When the output of the line driver is at logical false level, the driver transistor is off and the collector cut-off current is a maximum of 250 micro-amps.

All the J1 outputs are enabled by their respective DRIVE SELECT line.

7.2.1 TRACK Ø/ (Pin 10)

This interface signal is true only when the selected drive's read/write heads are positioned over Track Ø (the outermost data track). The signal is false when the selected drive's read/write heads are over any other track.

7.2.2 INDEX/ (Pin 20)

An Index pulse is generated once per revolution of the disk (16.7 milliseconds) to indicate the beginning of each track. This signal is normally false and makes the transition to logical true for a period of approximately 200 microseconds; refer to Figure 7-4.

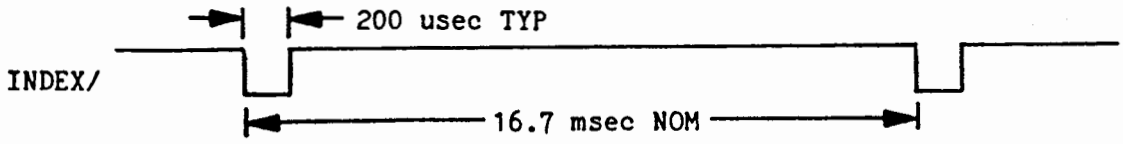


Figure 7-4. Index Timing

7.2.3 READY/ (Pin 22)

Ready will be true after the drive is up to speed and has positioned the read/write heads over Track Ø. The typical time for READY to become true after power-on is 20 seconds.

This interface signal, when true together with SEEK COMPLETE, indicates that the selected drive is ready to read, write, or seek. When this line is false, all writing to the disk and seeking is inhibited at the drive.

7.2.4 WRITE FAULT/ (Pin 12)

When this signal is true, it indicates that a fault condition exists at the drive. Writing is inhibited until the condition no longer exists or the condition is cleared by a Fault Reset (deselect/reselect sequence).

The following fault conditions are detected:

a. DC Power - DC voltages grossly out of tolerance.

b. Write Fault - one or more of the following conditions is detected when WRITE GATE/ is true:

- Shorted head.
- Open head.
- No Write Data transitions.
- No Write Current.

c. Write Unsafe - WRITE GATE/ is true when SEEK COMPLETE/ is false, or the heads are not positioned within 90 micro-inches of nominal track center.

d. Spindle Servo Fault - spindle speed cannot be reached or maintained.

e. Positioner Fault - servo fault prevents the completion of a seek operation.

The host controller should edge-detect this signal as WRITE FAULT/ is true only as long as the fault condition exists for faults a through c.

If fault d or e is detected, the drive is shut down until a Fault Reset is issued. Reset the fault by selecting the drive for 50 microseconds minimum then deselecting for 50 microseconds minimum.

7.2.5 SEEK COMPLETE/ (Pin 8)

The SEEK COMPLETE signal will go true when the read/write heads have settled on the final track at the completion of a seek. Reading or writing should not be attempted until SEEK COMPLETE is true.

SEEK COMPLETE will go false for either of two cases:

a. Within 500 nanoseconds (typical) after the leading edge of a STEP pulse (or the first of a series of STEP pulses).

b. When recalibration is initiated (by the drive logic) at power-on.

7.3 Data Transfer Connector Signals (J2)

All lines associated with the transfer of data between the drive and the host system are differential in nature. These lines are provided at the J2 connector on all drives. Two pair of balanced signals are used to transfer the data: WRITE DATA and READ DATA. Figure 6-3 illustrates the driver/receiver combination used in the drive for data transfer signals.

7.3.1 MFM WRITE DATA +/- (Pins 13,14)

This pair of signals defines the transitions (bits) to be written on the disk. When WRITE GATE is active, MFM WRITE DATA+ going more positive than MFM WRITE DATA- will cause a flux reversal on the track under the selected head. This signal must be driven to an inactive state (MFM WRITE DATA+ more negative than MFM WRITE DATA-) by the host system when in the read mode. Figure 7-5 shows the MFM WRITE DATA timing.

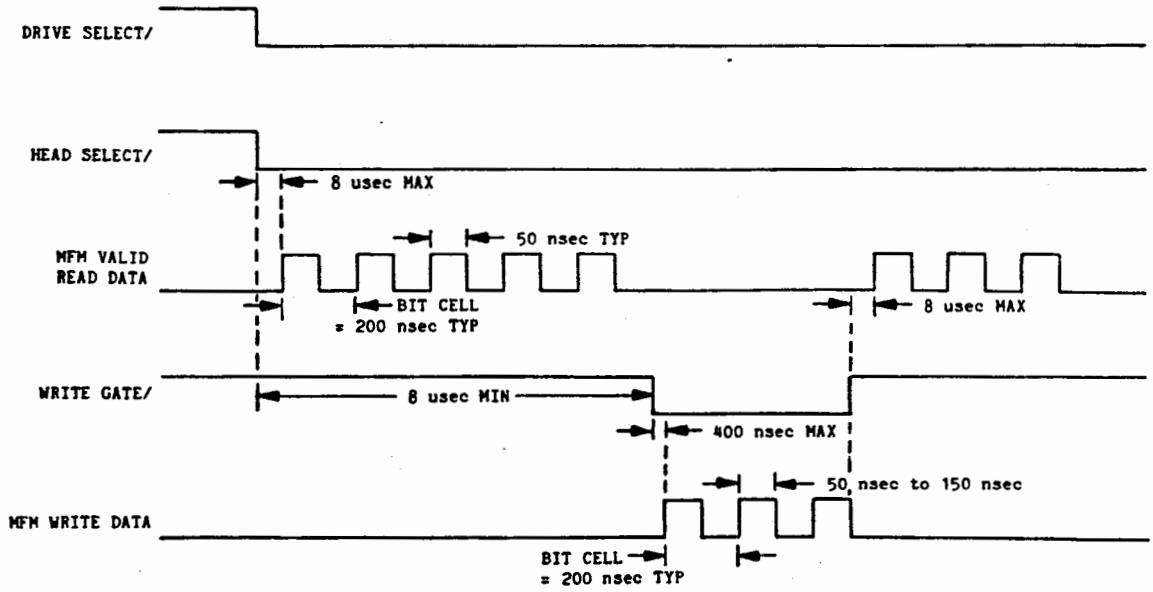


Figure 7-5. MFM Read/Write Data Timing

Write Data precompensation (see Section 5.3) is required on cylinders greater than 400 to meet the specified error rates.

7.3.2 MFM READ DATA +/- (Pins 17,18)

The data read from the selected surface is transmitted to the host system via the differential pair of MFM READ DATA lines. While WRITE GATE is inactive, a transition of the MFM READ DATA+ line going more positive than the MFM READ DATA- line represents a flux reversal on the track of the selected head; refer to Figure 7-5.

7.3.3 DRIVE SELECTED/ (Pin 1)

A TTL status line is provided at J2 to inform the host system of the selection status of the drive. This DRIVE SELECTED line is the output of a TTL open-collector gate, driven as shown in Figure 6-2. The signal goes active only when the drive is programmed as drive X (where X is 1, 2, 3, or 4) by proper placement of the drive selection jumper, and the corresponding DRIVE SELECT X line at J1 is activated by the host.

7.4 General Timing Requirements

The timing diagram shown in Figure 7-6 specifies the sequence of events (with the associated timing restrictions) for proper operation of the drive. A recalibrate to Track Ø sequence is initiated automatically at every DC power-on.

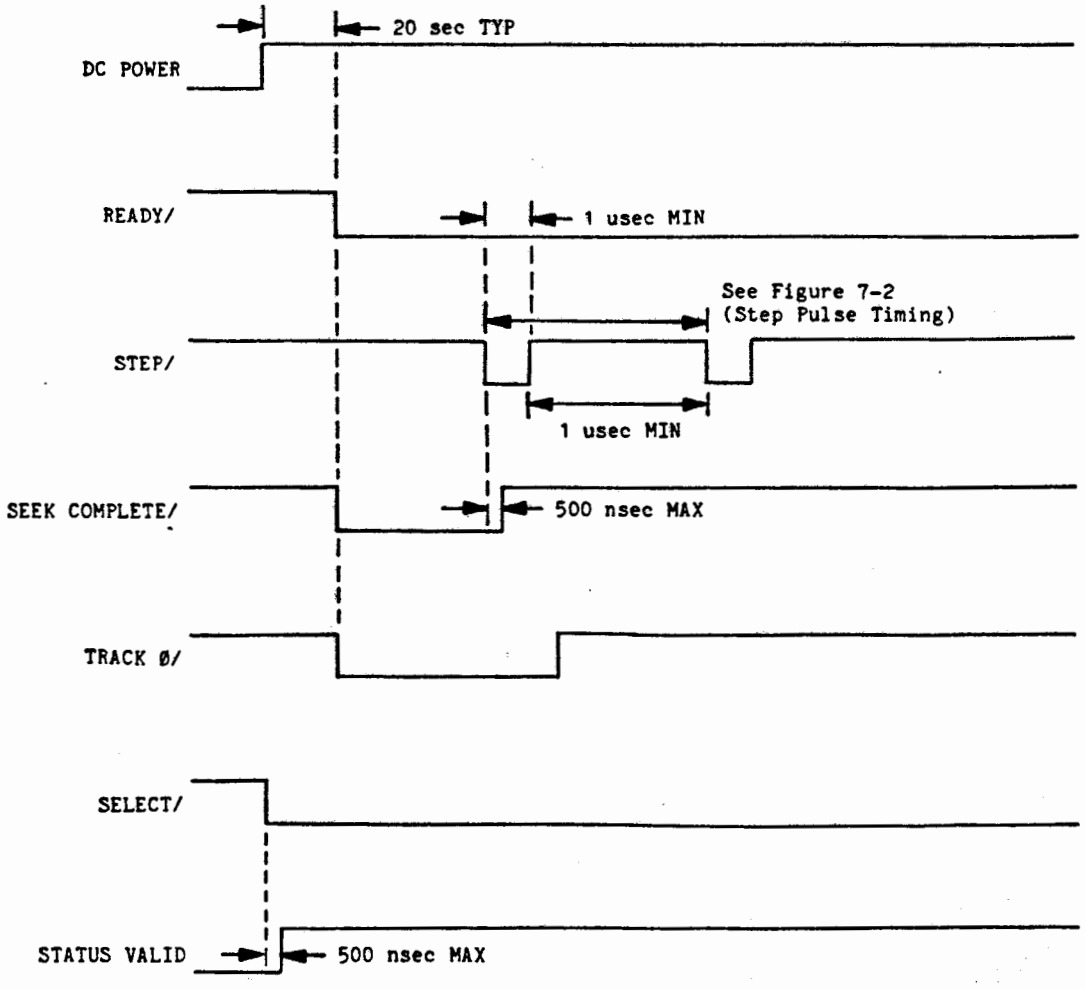


Figure 7-6. General Control Timing Requirements