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SiliconGraphics
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FUNCTIONAL DESCRIPTION - GR1.5

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SHEET 1 of 21

GR1.5 Graphics Board Functional Description

Marc Hannah
Chandlee Harrell

Silicon Graphics, Inc.

1. INTRODUCTION

This document provides a functional description of the GR1 graphics board.

The reader will get to peruse the following exciting tales:

- overview
- block diagram
- interfaces - what comes on and off the board
- Geometry Engine (GE5)
- GRF1 fixes
- RE1 and frame buffer memory organization
- XMAPs and color lookup tables
- hardware cursor & RAMDACs
- display state machine

2. OVERVIEW

Refer to Figure 1, the block diagram.

The GR1 performs the graphics functions for the Eclipse system. The host provides the GR1 with descriptions of 2D and 3D objects, and the GR1 takes care of drawing these objects and displaying them on the screen. The descriptions take the form of Graphics Library commands and world coordinate vertex data, and they describe the object's geometric position, color, and surface normal vectors used for lighting calculations. The GR1 board performs transformations and other graphics operations to calculate specific pixel values for each of the 1.3 million pixels on the 1280 by 1024 high resolution monitor. These pixel values are stored in the video RAM frame buffer and displayed on the monitor at a refresh rate of 60 Hz.

The GR1 consists of three sections: the Geometry Subsystem, the Raster Subsystem, the Display Subsystem. The Geometry Subsystem (called the GE5 module for Geometry Engine 5) includes the interface to the host as well as the floating point graphics computation engine. Commands and data from the host are examined by the GE5 and routed to one of two places. Display commands such as color map or cursor data are sent out over the display bus to update the appropriate location. Drawing commands for the geometry engine are stuffed in a fifo to even the flow between the host and the GE5. While commands remain in the fifo, the GE5 will read those commands and their associated data out of the fifo and perform the necessary calculations. The Raster Subsystem knows how to draw points, lines and spans (horizontal lines). Therefore, the GE5 breaks down world coordinate graphics primitives received from the host to the level of points, lines or spans described in screen coordinates. (Primitives from the host include points, lines, convex and concave polygons, mesh triangles, characters, splines, NURBS.) These simple point/line primitives are then passed to the Raster Subsystem for scan conversion.

The GE5 also maintains the status of the current graphics context. This status includes a 4 by 4 matrix stack for coordinate data transformations, a 3 by 3 matrix stack for surface normal transfromations, and light source information such as position, direction and intensity. Whenever the current graphics context is replaced with a new context, the GE5 passes the current status information to the host, and replaces it with new information from the host.

The Raster Subsystem scan converts lines (random or horizontal spans) into pixel values at each point on the screen, and controls all memory timing for writing these values into the frame buffer. The GR1 board includes 12 bitplanes of frame buffer on board. However, the Raster Subsystem includes all the necessary signals for expansion to 32 total bitplanes of frame buffer, and 24 planes of Z buffer. One optional daughter board (the BP4 board) may be plugged into the top of the GR1 to add 20 bitplanes of frame buffer, while another optional daughter board (the ZB3) adds the 24 planes of Z buffer. The Raster Subsystem includes hardware support for stippling lines, patterning horizontal spans, anti-aliasing color index lines, and dithering 12 bit RGB pictures. The frame buffer is broken up into image bitplanes, overlay/underlay bitplanes, and window ID bitplanes. Image bitplanes hold the color image to be displayed on the screen. In the 12 bitplane system, 8 bitplanes are provided for an 8 bit single buffered color index image, or a 4 bit double buffered color index image. Two bitplanes are dedicated for overlay or underlay applications such as pop-up menus and background colors. The last two bitplanes are for window ID providing hardware support for a windowed environment. 24 bitplanes of image, 4 bitplanes of overlay/underlay, and 4 bitplanes of window ID are supported in the fully loaded system.

The Display Subsystem accepts data from the serial output ports of the frame buffer and appropriately maps these outputs depending upon display mode before actually sending the pixels to be displayed on the monitor. The window IDs found in the frame buffer WID bitplanes tell the XMAP devices whether to interpret the data in the image bitplanes as single buffered or double buffered, color index or RGB images. The XMAP chips multiplex the image data appropriately and conditionally route it through the color maps such that the correct 24 bit values are fed to the RAMDAC inputs. The overlay/underlay bitplanes override the standard 24 bit values inside the XMAPs whenever an overlay or underlay is required. A hardware cursor is provided which overrides the standard 24 bit values inside the RAMDACs to assure the cursor gets highest priority.

The Display State Machine provides timing for the five pixel pipes (video RAM shift registers, XMAP, hardware cursor), and the monitor sync and blank. The timing changes with different kinds of monitors used. Four monitor timings come standard on this board. The four are: 1) 1280 by 1024 pixel non-interlaced 60Hz; 2) 1280 by 1024 pixel interlaced 30Hz; 3) 645 by 485 pixel RS170 30Hz; 4) 780 by 575 pixel EURO 30Hz. To support a timing not listed above, one of the oscillators must be swapped out and the Display State Machine PROM must be reprogrammed. The Display State Machine generates all sync, blank, load, clock signals for the various standards, as well as generating data transfer requests to the Raster Subsystem, and a vertical interrupt to the host.

3. BLOCK DIAGRAM

Refer to Figure 1. The following breaks down each subsystem of the block diagram.

The Geometry Subsystem consists of:

- HQ1 Gate Array: This chip provides control for the interface to the host, control for three burst DMA channels, and control for the geometry engine (GE5) floating point compute module. On the host interface side, the GR1 acts as a slave device on the interface bus. The whole Geometry Subsystem runs off the 10 MHz I/O clock provided by the host, such that the host interface may run completely synchronously. The HQ1 monitors the bus for host accesses, and decodes the addresses when an access arrives, sending strobes to the destination devices. The HQ1 handshakes with the host to extend cycles for slower devices or speed cycles for faster devices.

  Bidirectional burst DMA transfers may occur between three seperate pairs of endpoints. The host may perform read or write burst DMA transfers between its own main memory and the GE5 data RAM, or between its own main memory and the frame (or Z) buffer. The third DMA channel is between the GE5 data RAM and the frame (or Z) buffer. The HQ1 provides handshake control and a special GE5 microinstruction in order to operate the burst DMA channels. (All burst DMAs are performed under GE5 microcode supervision.)

  The HQ1 acts as the microcontroller for the GE5. It controls all program flow and all data movement across the GE5 data bus. Inside the HQ1 is a program control unit which allows branching and

subroutining, pointer control units for addressing the GE5 data ram and the register bank inside the RE1 gate array, and a data bus management unit which controls output enables on the GE5 data bus, on the host interface bus, and on the display bus. Stall control is incorporated on the HQ1 which stalls GE5 microcode allowing real-time host accesses to the GE5 data ram at any time during GE5 microcode execution. The microcode may pass flags and other information to the host through the data ram. (Note, with the current RE1, a host read during a burst DMA from frame buffer to GE5 data ram will cause microcode to hang. The RE2 will fix this problem. See GRF1 sections below for current fixes.)

- Display Bus Buffer: This is an eight bit transceiver which allows data to pass between the host interface and the display bus. Only the low eight bits off the host interface bus are passed on to the Display Bus.
- GE5 Data Bus Buffer: This is four eight bit transceivers allowing data to be passed between the GE5 bus and the host interface. Host accesses to entities on the GE5 data bus (e.g. data ram, microcode ram) move the data through these transceivers. Also, burst transfers that involve the host pass the data through this route.
- FIFO: This is a 512 by 40 fifo. Thirty-two bits of data and 8 bits of address are shoved into this FIFO. The 8 address bits are the 8 LSBs used on the host interface bus and are used as a tag for the HQ1. Sixteen of the 256 possible tags will force the HQ1 to switch to a new graphics context on the next read from fifo. The other 240 possible tags provide microcode jump addresses for the graphics commands passed down from the host. These tags are used in conjuntion with the FETCH instruction of the microcode. When simply data is being read from the fifo, the thirty-two bits of data are dumped onto the GE5 data bus. The fifo is used to even the flow of commands from the host, and execution by the GE5. Some commands take longer than others to execute on the GE5; the inclusion of a fifo allows the host to continue to write down graphics commands independent of what the GE5 is currently up to.
- Microcode RAM: There are 16K 40-bit words of microcode RAM. Address into the microcode RAM is generated by the HQ1. Some microcode instructions are vertical in that they occupy two locations in this microstore. Most highly utilized microinstructions fit into a single 40 bit micro-word. Output from the microstore controls the operation of the Weitek 3132, and feeds back to the HQ1 to help decide what is the next microinstruction and data bus transaction. During reset, the host loads all the microcode before unstalling the HQ1.
- Microcode RAM buffer: This is the data path for the host to load the microcode before operation begins.
- Data RAM: 8K 32-bit words of data RAM are provided. Data RAM is used to store constants and variables needed in the geometry calculations.
- Weitek 3132: This is a floating point data path chip. It provides pipelined floating point multiply and adds and 32 working registers within which to do the computations. All geometry and lighting transformations are performed in this chip. It is the core of the GE5. Refer to the 3132 data sheet.
- GRF1 Gate Array: The sole purpose of this gate array is to fix other problems in the system. It solves four problems. The first is within the HQ1. When a host access comes in while microcode is executing a read from fifo instruction, incorrect handshakes are passed back to the host. The GRF1 monitors this condition and corrects the handshake. The next three problems are all related to misinterpretation of the burst DMA handshakes between the HQ1 and the RE1. The fixes will be described in more detail below, but essentially the GRF1 corrects the handshakes such that all burst DMA transfers operate correctly, and provides two flag bits which the host may read off the host interface bus. The up and coming RE2 will solve the last three problems, while the first problem must 1) continue to use the GRF1; 2) or re-spin the HQ; 3) or add a couple 14-pin DIPs to the graphics board.

The Raster Subsystem consists of:

- RE1 Gate Array: This is a large gate array which performs scan conversion of endpoints of lines into pixels on the screen, and controls all memory timings into 32 bits/pixel of frame buffer and 24 bits/pixel of Z buffer. The GE5 loads a bank of registers on the RE1 chip to indicate what kind of

drawing operation is desired. The RE1 then iterates lines (random or horizontal spans) into individual pixels and performs the appropriate write cycles into memory. The chip can flat shade or Gouraud shade RGB or color index values while at the same time testing for WID and Z buffer consistencies. The chip uses a unique interleaving scheme into the frame buffer and Z buffer memories to allow page mode access speeds. The RE1 can stipple random lines, pattern horizontal spans, anti-alias color index lines, and dither 12 bit RGB images.

- Twelve Frame Buffer Bitplanes: Twelve bitplanes are provided with the base system. Twenty more bitplanes may be had with the addition of the BP4 daughter card. An optional ZB3 Z buffer card is also available as a plug in.

The Display Subsystem consists of:

- XMAP2 Gate Arrays: Five XMAP2 gate arrays are used, one for each pixel pipe out of the frame buffer. Each accepts up to 32 bits of data from the frame buffer, examines the window ID data and overlay data, and outputs the appropriate data to the RAMDACs (through the color maps if necessary). The XMAPs are by now rather standard SGI functionality. Refer to the XMAP2 specification for more information. Suffice it to say that they allow simultaneous single and double buffering in various modes in multiple windows, overlays, underlays, and all options chosen on the basis of the contents of the window ID bitplanes.
- Color Maps: Each of the five pixel pipes has a 4K 24-bit word color lookup table. These support up to twelve bits of color index that are used as the pointer into the color map to determine the 24 bit value that will be passed to the RAMDACs. When only eight image bitplanes are available in the system, the upper four bits may be wired on a window by window basis inside the XMAP2.
- Hardware Cursor: Two Brooktree Bt431 cursor chips may be inserted into the GR1. Each chip contains a 64 by 64 cursor glyph and some X,Y counters which keep track of the current position of the monitor beam on the screen. When the monitor beam is at a location where a bit in the cursor glyph is active, the Bt431 outputs an active signal to the overlay inputs on the RAMDAC. The RAMDAC will turn that pixel on as a cursor bit. Two bits of cursor color may be had by installing both cursor chips. Refer to the chip spec.
- RAMDACs: Three RAMDACs are used, the Brooktree BT457, one for each of red, green and blue. The RAMDACs provide multiplexing of the five pixel pipes down to one data stream, another color lookup table for gamma correction of values in this data stream, two overlay inputs to allow the cursor to be superimposed on the data stream, and D/A conversion of the data stream into RS343 level signals appropriate for the monitor. Refer to the chip spec.
- The Display State Machine (DSM): The DSM controls the timing of pixel data as it flows through the 5 pixel pipes, as well as timing for the SYNC and BLANK signals which control the monitors. Which timing to use is indicated by two bits that the host may modify in an XMAP display register. The timings supported on the standard product are: 1) 1280 by 1024 pixel non-interlaced 60Hz; 2) 1280 by 1024 pixel interlaced 30Hz; 3) 645 by 485 pixel RS170 30Hz; 4) 780 by 575 pixel EURO 30Hz. There are three oscillators that reside on the GR1 board that are used to provide the timing. The first provides a 107.352 MHz clock to support both 1280 by 1024 modes. The second provides a 12.27 MHz clock for RS170, and the third runs at 15.00 MHz to support PAL and SECAM. There is a fourth choice of clock which is from the J4 connector. This is typically sourced off the genlock board (described below), although it could be used as the clock source for some unusual timing mode.

  For a given timing standard, the DSM allows varying the widths of the SYNC and BLANK signals, varying the length of a frame buffer line to be displayed (all images less than 1280 pixels wide must be left adjusted), varying the number of lines displayed, and choosing between interlaced and non-interlaced. SYNC and BLANK pulses are adjustable within a 5 pixel resolution.

  The DSM interacts with Raster Subsystem by requesting a data transfer cycle of the RE1. Every new display line, new data must be loaded into the serial shift register which is part of every video RAM chip (from the chip's dynamic RAM array). This loading is done with a data transfer cycle. The DSM

understands when horizontal blanking is going on and asks the RE1 to perform the transfer from RAM to shift register inside the video RAMs during the horizontal blanking period. The RE1 provides the proper page address and shift start address for the data row to be displayed next (see video RAM data sheets).

The DSM is built out of a Xilinx 2018 programmable logic array, an 8K by 8-bit PROM, a 2K by 8-bit RAM, a Bt438 clock generator chip, and some other miscellaneous clock control circuitry.

4. INTERFACES

The GR1 incorporates the following interfaces:

— interface to the host CPU (IP6)

— interface to the bitplane expansion board (BP4)

— interface to the Z buffer option board (ZB3)

— interface to the Genlock Board (CG3)

— stereoptic bit and other miscellaneous signals

4.1 Interface to the Host

The host interface runs across a ribbon cable between the IP6 and the GR1.

4.1.1 Hardware Interface All control signals (except VERTSTAT\) are buffered on the GR1 board before being used on or sent off the board. The multiplexed address/data bus goes to five destinations on the GR1 without being buffered. Worst case capacitance is low, and reasonable time is provided before the data on the bus is sampled to allow the data to settle (possible because the bus is synchronous). Four clock signals (HOST.PRECLK, HOST.10MHZ, HOST.OE-EN\, HOST.CASSTB\) are passed from the host to the GR1 to drive the interface and the GE5. The first three of these are actually used by the GR1. The system is designed assuming there can be no more than 10ns of skew between the clock signal on the GR1 and its equivalent clock on the IP6. The amount of skew is determined by the buffer delay on each of the boards where they receive the clocks off the interface (the IP6 sends its clocks onto the cable then wraps them back through buffers before using them). Figure 2 shows how the buffered clocks should appear on the GR1.

The host interface signals are:

- HOST-10MHZ: The host provides the 10MHz clock which drives the GE5. The 10MHz clock is distributed to the GE5 on two lines, one is free running, and the other can be stopped for stalling the 3132 when the HQ1 determines a stall is necessary.
- HOST-PRECLK: This is a 10MHz clock which is shifted approx 15ns ahead of the HOST-10MHZ. This clock is used to compensate for the possible 10ns skew between clocks on the two boards. All signals passed between the host and the graphics board are latched using this clock.
- HOSTOE-EN\: This is a 10MHz clock which follows HOST-10MHZ exactly but with a much shorter high time. The high time of this signal is used to disable all drivers onto the host interface address/data bus, as well as most drivers on the GE5 data bus. The intent is to eliminate contention among drivers on a given bus.
- HOST-CASSTB\: This signal is unused on the GR1.
- HOST-RST\: A low level on this signal will reset the following items on the GR1: HQ1, fifos, GRF1, RE1, Bt431, Bt438s, XMAP2s.
- HOST-AS\: The address strobe goes low for one clock cycle to initiate a transfer and to indicate a valid address is on the bus.
- HOST-RD\: Indicates whether this is a host read or a host write access.

- HOST-DLY\: The host asserts this signal low after an address strobe to lengthen a transfer. The HQ1 re-clocks HOST-DLY\ before using it. The cycle when both re-clocked HOST-DLY\ and IO-DLY\ are high after an address strobe is the last cycle of the access.
- IO-DLY\: The HQ1 asserts this signal low after an address strobe to lengthen a transfer. The host does NOT re-clock this signal before using it. The cycle when both re-clocked HOST-DLY\ and IO-DLY\ are high after an address strobe is the last cycle of the access.
- HOST-BURST\: When the host wishes to perform a burst DMA transfer, and after the GE5 has indicated via software that it is ready to transfer, the host asserts this signal low to initiate the actual burst transfer. The burst transfer continues until this signal goes inactive.
- FIFOHALF\: This signal goes low whenever the fifo is half full. It is an indication to host software that it should hold off sending commands down the graphics pipe.
- IO.INTR\: This interrupt bit may be set by GE5 microcode and cleared by a host access.
- VERTINTR\: This interrupt is asserted once every monitor frame slightly ahead of vertical blanking. The exact positioning of the interrupt may be controlled by the Display State Machine firmware.
- VERTSTAT\: This is a status bit which is asserted during vertical blanking which may be polled by host software. The exact positioning of this signal within vertical blanking may be controlled by Display State Machine firmware.
- HOST-AD[0-31]: Address and data are multiplexed on these pins. Twenty bits of address are valid while the address strobe is active, and 32 bits of data are valid depending on the state of HOST-DLY\ and IO-DLY\. These lines have pullups on them on the GR1.

Timing for the host interface handshake signals is given in Figure 3.

4.1.2 Software Interface Ten bits of address (HOST-AD[2-11]) are decoded by the HQ1. Two additional bits (HOST-AD[12-13]) are decoded by the GRF1 to allow for implementation of fixes involving the host interface. The twelve address bits are decoded along with the address strobe and the read strobe to determine who's involved in what kind of cycle. Offsets into the graphics address space are given in the following table:

ADDRESS	ADDRESSED	
0 - 1023 (plus MADDRREG[7]=0)	ucode RAM, low word	(read/write)
0 - 1023 (plus MADDRREG[7]=1)	ucode RAM, high byte	(read/write)
1024 - 2047 (plus MADDRREG[7]=0)	data RAM w/o GRF1 fifo fix	(read/write)

MADDRREG[7]=1 FOR ACCESSING THE FOLLOWING LOCATIONS:

1024 - 1055	xmap channel 0	(read/write)
1056 - 1087	xmap channel 1	(read/write)
1088 - 1119	xmap channel 2	(read/write)
1120 - 1151	xmap channel 3	(read/write)
1152 - 1183	xmap channel 4	(read/write)
1184 - 1215	xmap broadcast	(write only)
1216 - 1247	xmap display reg 3	(read/write)
1248 - 1279	xmap display reg 4	(read/write)
1280 - 1311	red brooktree dac	(read/write)
1312 - 1343	green brooktree dac	(read/write)
1344 - 1375	blue brooktree dac	(read/write)
1376 - 1407	cursor chip 0	(read/write)
1408 - 1439	cursor chip 1	(read/write)
1440 - 1471	xmap display reg 0	(read/write)
1472 - 1503	xmap display reg 1	(read/write)
1504 - 1535	xmap display reg 2	(read/write)
1600 - 1663	clear stall	(write only)
1664 - 1727	set single step mode	(write only)
1728 - 1791	clear single step mode	(write only)
1792 - 1855	execute a single step	(write only)
1856 - 1919	read current PC	(read only)
1920 - 1983	clear interrupt 0	(write only)
1984 - 2047	clear interrupt 1	(write only)
2048 - 3071	fifo	(read/write)
3072 - 3583	load MADDRREG[6-0]	(write only)
3584 - 4095	load MADDRREG[7]	(write only)
5120 - 6143 (plus MADDRREG[7]=0)	data RAM with GRF1 fifo fix	(read/write)
8192	GRF1 flag bit 1	(read/write)
8196	GRF1 flag bit 2	(read/write)

Unused addresses above 4096 should not be accessed. Only addresses 1536 - 1599 are not recognized by the HQ1.

4.2 Interface to Bitplane Expansion

This interface consists of a bundle of timing control signals sent from the RE1 to the bitplane expansion board (BP4), and both parallel and serial port data buses.

4.2.1 Hardware Interface The following signals are passed across the J8 and J9 connectors:

- FADDR[0-7]: The multiplexed row and column address lines.
- LEN[0-3]: These are the serial clock enables which select which of the four rows of video RAMs is currently being displayed on the screen. Only the one of four rows which is currently selected gets it shift register clocked.
- VIDLDD[0-2]: These are the serial shift register clocks which clock data out of the video RAM shift registers. These signals are gated on the BP4 with the LEN signals to produce the actual serial clock to the VRAMs.
- FDATA[8-27]: The parallel port data bus for the 20 bitplanes on the BP4.
- PIXH[A-E][8-23]: These are the serial data streams providing another sixteen bitplanes of image data to the XMAP2s.
- AUX[A-E][0-3]: These are the four auxiliary bitplanes that come with the BP4.
- RAS[0-3]\: The row address strobes for the four rows of video RAMs.
- CAS[0-4]\: The column address strobes for the five columns of video RAMs.
- OE[0-4]\: The output enables for the five columns of video RAMs.
- FWE\: The VRAM write enable.
- RECLK.BP: The same clock as drives the RE1, used to clock certain registered drivers.
- BPIN\: This simply indicates to software via an XMAP2 readable register that the BP4 is actually installed.

The timing of these signals is identical to those which drive the bitplanes which come standard on the GR1 board. Refer to the RE1 documentation.

4.3 Interface to the Z-Buffer Board

This interface consists of a bundle of timing control signals sent from the RE1 to the Z buffer board (ZB3), data and address buses. The Z buffer board simply holds the memory for the Z data, while the actual Z compares and decision making goes on inside the RE1 chip.

- ZADDR[0-8]: Nine bits of multiplexed row and column address to accomodate the one megabit DRAMs which make up the Z buffer.
- ZDATA[0-23]: Twenty-four bits of Z data.
- ZRAS\: A single row address strobe as the one megabit DRAMs are arranged one row by five columns.
- ZCAS[0-4]\: The column address strobes for the five columns of DRAMs.
- OE[0-4]\: The output enables for the five columns of DRAMs.
- ZWE\: The write enable for the Z buffer DRAMs.
- Z1G[0-2]\: Output enables for the registered transceivers which sit between the RE1 and the actual DRAM devices.
- ZBIN\: This indicates to software via an XMAP2 readable register that the ZB3 is actually installed.

The timing of these signals is very similar to those which drive the bitplanes which come standard on the GR1 board. Refer to the RE1 documentation for more information.

4.4 Interface to the Genlock Board (CG3)

Using the GR1 with the genlock board allows synchronous video display between two machines running with the same monitor type selected. When in genlock, the source for the pixel clock comes off the CG3

board. This pixel clock is derived from the incoming master signal from the other (external) system. Thus, the two systems clock at the same rate. To ensure the two systems provide data at the same time, the CG3 sends a synchronization signal, called GENSYNC\, to the GR1. GENSYNC\ forces the GR1 display state machine to a particular spot in its video timing sequence. The CG3 chooses when it asserts GENSYNC\ such that the video timing sequences match up between the two machines. Genlocking is supported for any of the four monitor types. GENSYNC\ is a frame rate signal (i.e. NOT field rate for interlaced). Note that the GR1 horizontal sync should be used by the CG3 board to phase lock the ECL clock that is driving the GR1 (thus getting the accuracy to within the phase error of the phase comparator, rumored at less than 1/2 pixel). Genlock signals are sent out over the J5 connector. The CG3 uses the signals listed below.

- Composite Vertical and Horizontal Sync
- Horizontal Drive
- Composite Vertical and Horizontal Blanking
- Field Bit indicating whether the current field is the odd or even field.
- Least significant bit of blue on each of the five pixel pipes. These five bits are used for multiplexing the images from the two genlocked machines on a pixel by pixel basis (done on the CG3).

4.5 Stereoptic Bit and Other Miscellaneous

A bit in an XMAP2 register may be written by software. The bit drives out on the genlock connector and may be used by application programs to control stereoptic viewers.

Also driven onto the genlock connector are four diagnostic signals: FIFOEMPTY\ - tells if the fifo is empty; FIFOHALF\ - indicates when the fifo is more than half full; CLKSTALL\ shows when the GE5 is in a stalled state; RELOADEN1\ - shows when the RE1 is idle, i.e. not drawing.

5. GE5

See Figure 4.

The GE5 is a floating point compute engine controlled by 16K 40-bit words of microstore. The microcode word is detailed in Figure 5. The microcode word is either 40 bits wide, or two cycles may be taken to access 80 bits of information for a single microinstruction. The 40 bit microinstruction has all the information necessary to control the internal functions of the 3132, all PC control, the ability to increment the REPTR and MEMPTR, and control over the commonly used data bus output and write enables. Most instructions may simply use this single field, including conditional branches which do not get taken. The second 40 bit field is mostly used for constants, for instance target addresses for branches and values to load in the MEMPTR. Also found in the second field are tools for setting the interrupt bit and controls for the burst DMA channel.

The HQ1 includes all the decode circuitry for the portions of the microcode field which affect the Program Counter (PC), the Data Memory Pointer (MEMPTR), the RE Pointer (REPTR), and the data bus enables. The PC, MEMPTR, and REPTR registers reside on the HQ1. Inside the HQ1 is a two stage pipeline. The first stage decodes the current output from the microcode memory to determine what the next instruction will do, how the next instruction will affect the PC, MEMPTR, REPTR and data bus enables. The second stage of the pipeline controls the current activity on the data bus and in the 3132, and represents the result of the previous cycle's output from the microcode memory. Reinterating the pipeline concept, it takes one clock cycle before the activity for the current microinstruction is seen on the GE5 data bus and in the 3132.

The pipeline may be stalled in its current state by several conditions. First, the HQ1 provides a single step mode whereby only one instruction gets executed every time the host writes to a particular GR1 address. Second is the provision of a microinstruction which stalls microcode execution at the command of software until the host unstalls the GE5. The third condition happens when the microcode is attempting to read a value from the fifo, but the fifo is empty. The microcode will stall with the PC pointing to the microinstruction after the fifo read but no output enable will be issued to the fifo. The GE5 will stay in this state until the fifo goes not empty. At this point a fifo output enable will be issued and the GE5 will be

unstalled. The fourth event which causes a stall which maintains the current state of the pipeline is a read or write to the RE1 register bank when the RE1 is not ready to accept a transfer. The RE1 interface to the GE5 includes two banks of 32 registers. The HQ1 looks at the upper bit of the REPTR which determines in which bank the register to be accessed sits. The HQ1 then conditions the access with the state of either RE-LOADEN0\ or RE-LOADEN1\ (using the former if REPTR5 is 0 and the latter if REPTR5 = 1). An access where the appropriate RE-LOADENx\ is not low will stall the GE5 pipeline until such a time as it does go low.

The HQ1 will also stall the GE5 on an access to the GE5 data memory (this is the only part of the address space which may be accessed while microcode is actually running; all other accesses must ensure that the GE5 is already stalled via a reset or a stall microinstruction). This differs from the other stalls in that the second stage of the pipeline is not maintained in its current state. Instead, it is flushed for the period of the host access (which forces MEMOE\ or MEMWE\ and HOSTOE\ active). The second stage of the pipeline is then restored from save away registers before the HQ1 unstalls the GE5.

A stall is evidenced on the GR1 by the CLKSTALL signal which is high throughout a stall. This signal is brought out on the third LED for immediate viewing. Note also that the second 40 bit field of an 80 bit microinstruction is accessed by stalling the 3132 for a single clock. Whenever the second field of a microinstruction is accessed, CLKSTALL will go high for a single clock cycle. The HQ1 is still messing with the PC, MEMPTR, REPTR and data bus enables, but the 3132 is kept in its current state for this clock tick.

Data may be passed between any combination of the fifo, the 3132, the data RAM, and the RE, with the exception that data may not pass from the fifo directly into the RE (reason: a host access will fail if it occurs during a transfer like this when the appropriate RE-LOADENx\ is not active). Typical operation has the GE5 getting its command from the fifo (the PC jumps to the value found on FIFO-TAG shifted left once), followed by whatever variables the host has stuffed in the fifo associated with that command. Then computations are done inside the 3132 with constants and variables being passed extensively between the 3132 and the GE5 data ram. Finally, drawing commands are loaded into the RE register banks to tell the RE to scan convert lines into pixels.

All burst DMA transfers are controlled by a specially provided microcode instruction called REPEATGEZ. For a burst DMA transfer, the microcode enters the HQ1 into DMAMODE, loads a counter in the HQ1 with the number of transfers about to happen, then executes a REPEATGEZ instruction with the appropriate source and destination data bus enables set. The same scenario occurs whether the transfer be host-ram or host-RE or ram-RE. The only microcode difference is which data bus enables are set. The HQ1 (and GRF1 as explained below) takes over from there. Depending upon which burst transfer is happening, the HQ1 monitors the HOST-BURST\ signal and the RE-DLY\ signal to determine when a transfer has actually happened. If the transfer is host-RE, any clock cycle where HOST-BURST\ is low and RE-DLY\ after being re-clocked is high indicates a transfer has happened and the counter inside the HQ1 is decremented. The host may stall in the middle of a DMA transfer by asserting HOST-BURST\, and the RE may stall by asserting RE-DLY\. HOST-BURST\ is passed through the HQ1 to the RE1 on the GE5-DLY\, while RE-DLY\ is re-clocked and passed through the HQ1 to the host as IO-DLY\. The host and RE1 both maintain their own separate counts of the number of transfers left in the current burst. The host-ram and ram-RE handshakes are subsets of the host-RE handshake where the signals do not get passed through the HQ1.

More detail on the GE5 and its operation may be found in the HQ1 specification.

6. GRF1 Fixes

The GRF1 gate array was designed to fix four problems on the original GR1 design. The first problem is a trouble inside the HQ1 chip in the event that the HQ1 is output enabling the fifo at the same time that a host accesses GE5 data ram. The HQ1 notes a request has been received from the host to access the data ram, and does not service that request until it has finished outputting the fifo. It then performs the requested host access. What is missing is that the HQ1 should hold off the host using the IO-DLY\ signal until the fifo transaction is completed. Instead, IO-DLY\ remains unchanged in the high state and the host believes the

transfer to be immediately complete. The fix for this problem requires software to assert HOST-AD12 for every access to the GE5 data ram (see address map above). Whenever HOST-AD12 is high, the GRF1 chip will automatically assert IO-DLY\ until the IO-DLY\ from the HQ1 goes low, at which point the HQ1 IO-DLY\ gets passed straight through. This succeeds in keeping the host waiting until the HQ1 has finished servicing any microcode fifo reads.

The second problem involves burst DMA transfers which write data to the RE1. For burst transfers in this direction, the RE1 does not expect the HQ1 to re-clock the RE-DLY\ signal before examining its state. Therefore, the handshake is off by one clock cycle and the two endpoints of the burst transfer end up out of sync with each other. The GRF1 chip looks at several board level signals and manages to predict the RE-DLY\ signal in such a fashion that it comes out of the GRF1 chip one clock ahead of when it comes out of the RE1. Essentially, the RE1 burst control state machine is re-created in the GRF1 with fixes included.

The next two problems are both related to burst DMA transfers which read data from the RE1. Burst read transfers take two 10MHz clock cycles for each datum transfered. The RE1 produces an RE-DLY\ low on every other 10MHz clock cycle to draw the transfer out to two cycles. Since RE-DLY\ is re-clocked before being used by either the HQ1 or the host, it is actually the state after that in which RE-DLY\ is high that data is used by the host or the GE5. Now, if GE5-DLY\ goes low during the state when the data was to be used (RE-DLY\ now low), the data should be maintained on the GE5 bus by the RE1 until GE5-DLY\ goes high again. Instead, the RE1 does not recognize GE5-DLY\ at all on this cycle and puts the next datum out on the bus and decrements its transfer counter. The RE1 only recognizes GE5-DLY\ on the same cycle as its RE-DLY\ output is high.

For ram-RE transfers, GE5-DLY\ never goes low until the transfer is finished, so no problem ever occurs. For host-RE transfers, the GRF1 chip predicts the rising edge of HOST-BURST\ one clock ahead of when it actually is received from the host, curing the handshake mismatch.

The fourth problem, also a consequence of this read DMA handshake mismatch, occurs when the host does a regular access to the GE5 data ram while a ram-RE burst transfer is in progress. The host access will cause GE5-DLY\ to go low randomly. The initial assertion of GE5-DLY\ may be lost by the RE1 if it occurs on the wrong half of a read DMA transfer, and the RE1 will incorrectly decrement its transfer counter. The only time the host could access the GE5 data ram while a ram-RE read DMA was in process is when the host is testing some flag locations. The GRF1 solves the problem by providing two flag bits to the host which may be set by microcode using one of the unused MEMPTR address bits, and read by the host by asserting HOST-AD13.

7. RE1 and Frame Buffer Organization

The RE1 is a dense gate array which controls the parallel port timing for the frame buffer video RAM chips, timing for the Z buffer DRAM chips, and interpolates pixels along random-angled or horizontal scan lines. Detailed timing diagrams and explanations for the RAM chip control signals are given in the RE1 chip specification.

The RE1 has three ports. The first port is the interface to the GE5 which holds 64 registers that may be accessed by the GE5. The second port is to the frame buffer which holds up to 24 bitplanes of image memory, and four bitplanes of overlay/underlay memory. The third port is to the Z buffer which holds 24 planes of Z buffer memory, and four bitplanes of window ID (WID) memory. The two possible bitplane configurations for the GR1 are shown in Figure 6. Frame buffer and Z buffer organization are shown in Figure 7.

The RE1 performs rectangular clears by clearing the 20 pixel word all in one page mode cycle. The Z buffer is cleared by actually writing the WID planes 20 pixels at a time, using one of the WID bits as a dirty (i.e. cleared) bit for the Z buffer. Flat fills are performed on the 5 pixel frame buffer and Z buffer word. Shaded fills are done using an interleaving scheme across the 5 pixel frame and Z buffer words. All five chips are put into page mode, with the CAS\ and OE\ of only one of them being asserted at a time in synchrony with the data for that chip. This allows shaded pixels to be filled one pixel every RE1 clock tick. Z buffered shaded pixels take one pixel every clock tick for pixels that are not written, and approx

one pixel every two clock ticks for pixels that are written.

The RE1 takes care of both refreshing the memory, and ensuring that the RAS\ low time specification is not exceeded for long shaded span fills. The Display State Machine sends TRRQ\ to the RE1 to indicate it should perform a video RAM data transfer cycle. The RE1 keeps track of the row address to use during this data transfer cycle.

The RE1 includes DDA iterators for X, Y, Z, R, G, B. The red iterator may also be interpreted as a 12-bit color index. The GE5 loads the RE1 registers with initial values and delta values for X, Y, Z, R, G, B, and a count register with the number of pixels to fill. The RE1 is then issued a command to draw the line (or flat shaded screen clear). The RE1 will add the delta to each of the initial values to determine pixel values along the line. Iteration will continue until the count register reaches zero. Z buffer and WID compare circuitry is also part of the RE1. Writes can be made conditionally on a pixel by pixel basis dependent on the values in the Z buffer and WID planes.

Pattern masking and line stippling may be enabled or disabled within the RE1. Uncorrected anti-aliased color index lines are supported in RE1 hardware. Dithering is accomplished for 12 bit RGB images by semi-randomly incrementing the RGB nibbles, the randomness being chosen by a hardwired dithering table.

The RE1 supports burst DMA reads and writes to the frame buffer or the Z buffer. The GE5 loads the transfer count and then issues a read DMA or write DMA command. The RE1 readies the memory chips in page mode, then performs rapid reads or writes while decrementing its transfer count and monitoring the GE5-DLY\ line to ensure a transfer should occur. Upon receiving a burst DMA command, the RE1 switches its own clock (via external gates) so that it is running off the same 10MHz clock that drives the host and GE5. Typically the RE1 is driven of the PAL 15MHz oscillator.

8. XMAP2s & Color Look-Up Tables

The XMAP2s provide multiplexing for the image bitplane data on a window by window basis, as well as allowing for overlays and underlays. For every pixel which enters the XMAP2, the WID is checked against a table in the XMAP2 loaded by software over the Display Bus. The table connects a particular WID to a certain display mode for that window. A WID may indicate that the window is in color index or RGB mode, that it is single or double buffered, that this is a 4-bit color index image or 12-bit RGB image. Using the WID, the XMAP2 correctly routes the data it receives from the bitplanes on a pixel by pixel basis. For an RGB pixel, the bitplane data is padded and shifted as necessary, and put out as three 8 bit quantities as inputs to the three DACs, one for red, green, blue. For a color index pixel, the bitplane data is padded and shifted if necessary, and put out as the address into the color lookup tables. The XMAP2 also monitors data from the auxiliary bitplanes. If some of the overlay or underlay functions are activated, the XMAP2 will override the data from the image bitplanes with 24 bits of data from an internal auxiliary lookup map (indexed by the value from the auxiliary planes). See the XMAP2 spec for further details.

Color index pixels are passed through the color lookup maps which output the 24 bit RGB quantities. The color map outputs are tied directly to the RGB outputs of the XMAP2. One critical timing is in swapping the output drive between the color maps and the XMAP2. They are currently allowed to contend. The second critical timing is from driving an address into the color maps to getting their output data set up to the RAMDAC inputs. 4K entries in the color maps are provided to allow for 12 bit color index images. All 4K are free to use by user programs, as the RAMDACs hold enough ram (256 words) to perform gamma correction on all pixel values they receive.

All XMAP2 internal registers and color maps are loaded across the Display Bus. Each XMAP2 includes 5 general purpose register bits, three writeable by the host, and two more readable by the host. These bits are used on the GR1 for controlling and monitoring miscellaneous functions on the board.

9. Hardware Cursor and RAMDACs

Locations for two Bt431 hardware cursor chips are provided on the GR1. The output from each chip, when high, will cause the RAMDAC chips to force a value from internal overlay registers to be forced on their

outputs instead of the values received from the XMAPs. If only one chip is used, only one cursor color is available. If two chips are used, three cursor colors are available because either one of the two outputs may be high, or both at once. Inside the Bt431 is storage for a 64 by 64 cursor glyph. Registers maintain the current position of the cursor on the screen, and counters maintain the current position of the monitor beam in the output pixel stream. When the two match, the Bt431 output will force a cursor overlay. Software updates the current cursor position over the Display Bus.

Three Bt457 RAMDAC chips are included on the GR1, one for the red, green and blue components of 1280 by 1024 pixel monitor. Each RAMDAC outputs RS343 compatible voltage levels. Inputs to the RAMDAC are 5 pixel pipes of 10 bits apiece. Eight bits are the bits of color component which typically are translated to the analog output. The other two bits, when high, force an overlay over the eight bit color component value for cursor applications. The forced value comes from a tiny lookup table indexed by the two input overlay bits. The five pixel pipes are multiplexed down to a single data stream running at the monitor rate (107MHz for high resolution monitor). This data stream is then passed through a lookup table to produce a different 8 bit output quantity which is subsequently translated to an analog output signal. The interim lookup table is used for gamma correcting the values received from the XMAP2s to correct for color nonlinearities in the monitor being used. The gamma correction map and cursor overlay map are updated over the Display Bus.

10. Display State Machine

SOON TO BE PROVIDED

FIGURE 1: BLOCK DIAGRAM

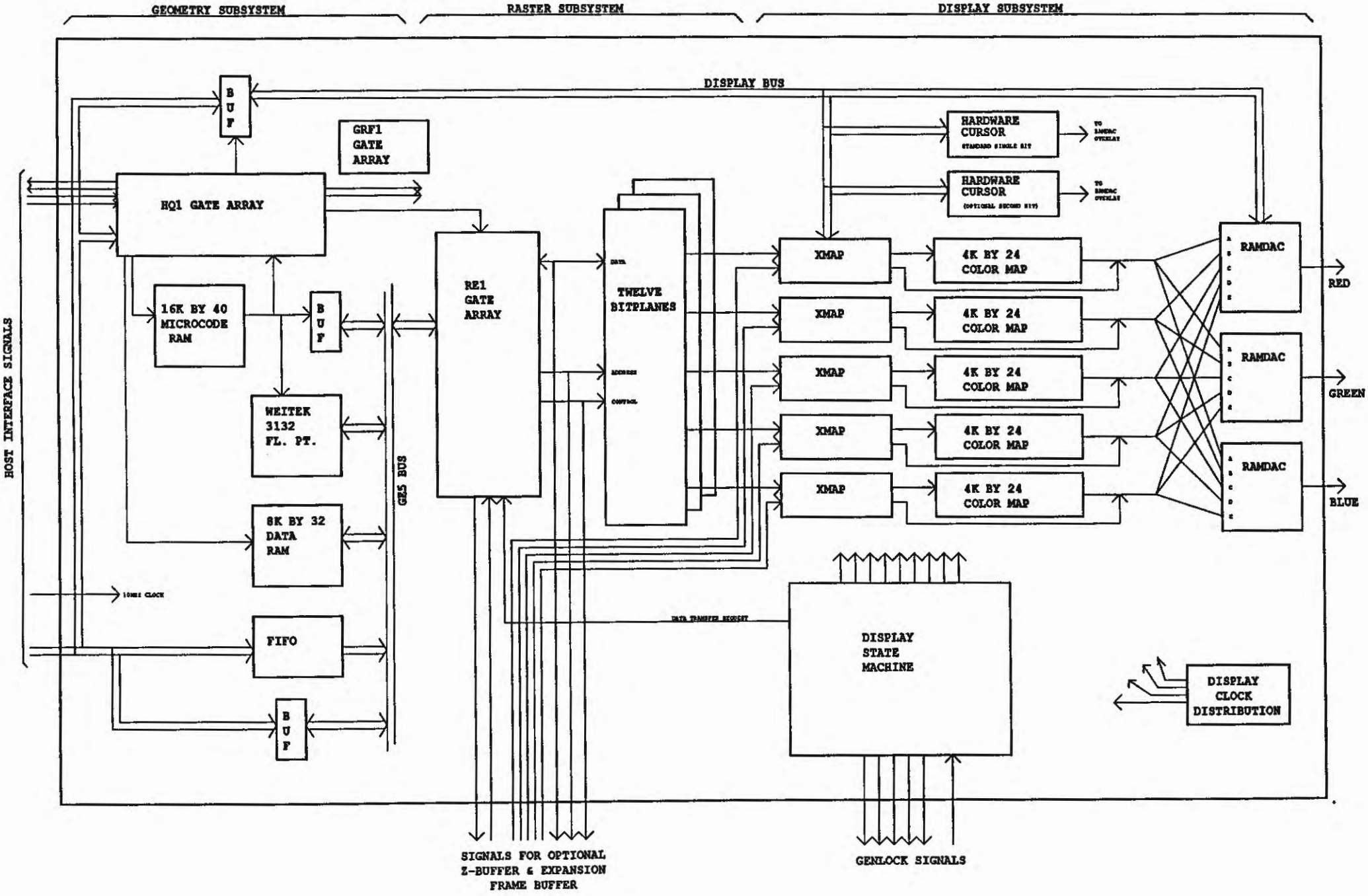
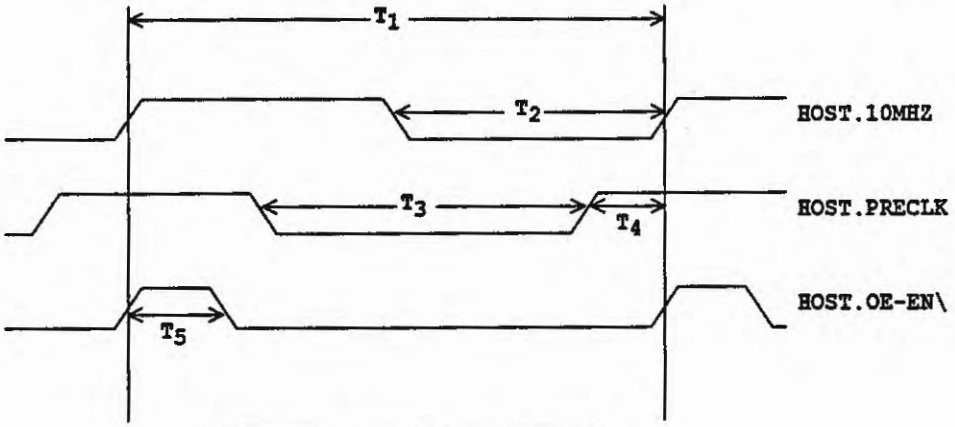


FIGURE 2

CLOCKS AS SEEN ON CABLE BETWEEN BOARDS, AND ON GR1 AFTER BUFFERING



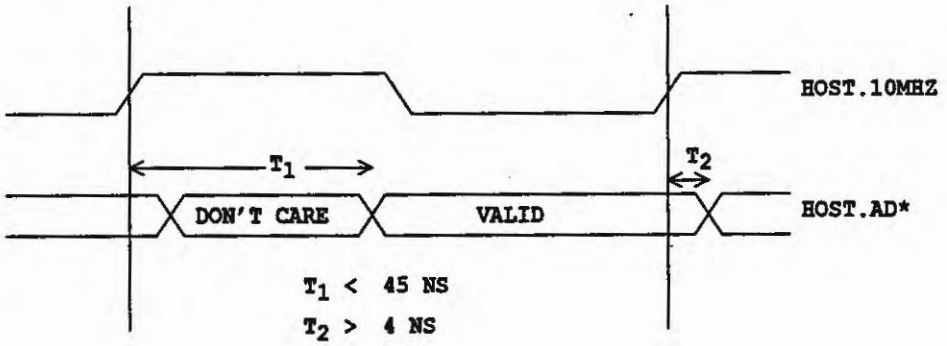
(ns)	MIN	NOM	MAX
T_1	99	100	101
T_2	46	50	54
T_3	54	58	62
T_4	14	16	18
T_5	14	16	18

THE BUFFERS ON THE GR1 MEET THE FOLLOWING DELAY
RESTRICTION ON THE LOW TO HIGH TRANSITIONS:

6 NS <= BUFFER PROPAGATION DELAY <= 16 NS

THE GR1 PROVIDES ADDRESS AND DATA ON THE CABLE BETWEEN THE BOARDS

AS SHOWN BELOW WITH RESPECT TO THE BUFFERED CLOCK ON THE GR1:



T_1 < 45 NS
T_2 > 4 NS

THIS GUARANTEES 28 NS SETUP AND 8 NS HOLD WITH RESPECT TO
THE BUFFERED HOST.PRECLK AS SEEN ON THE HOST BOARD
(THIS SET UP BEING SEEN ON THE CABLE).

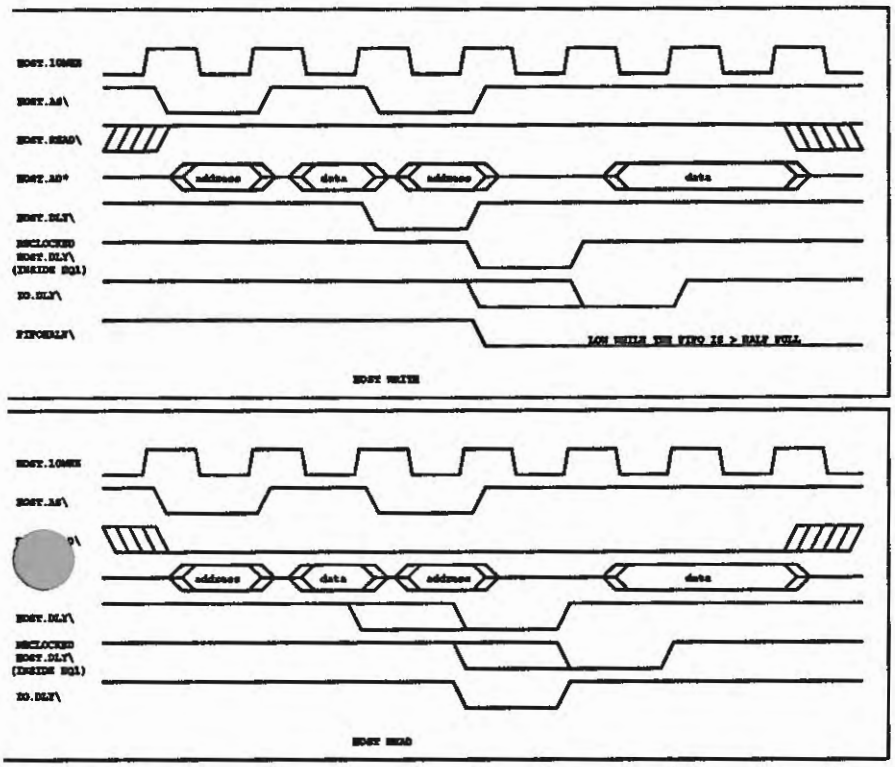
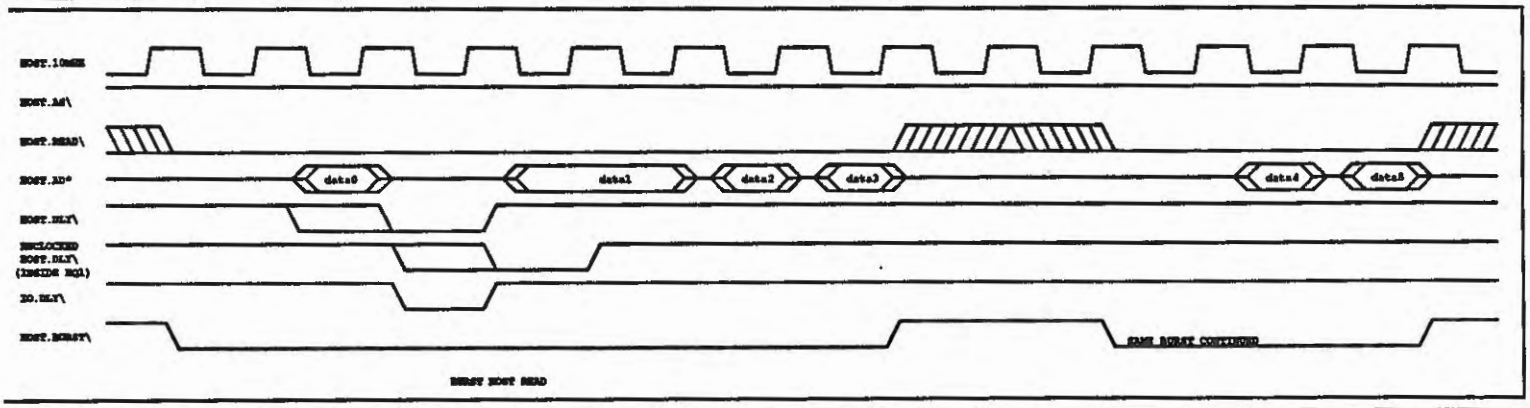
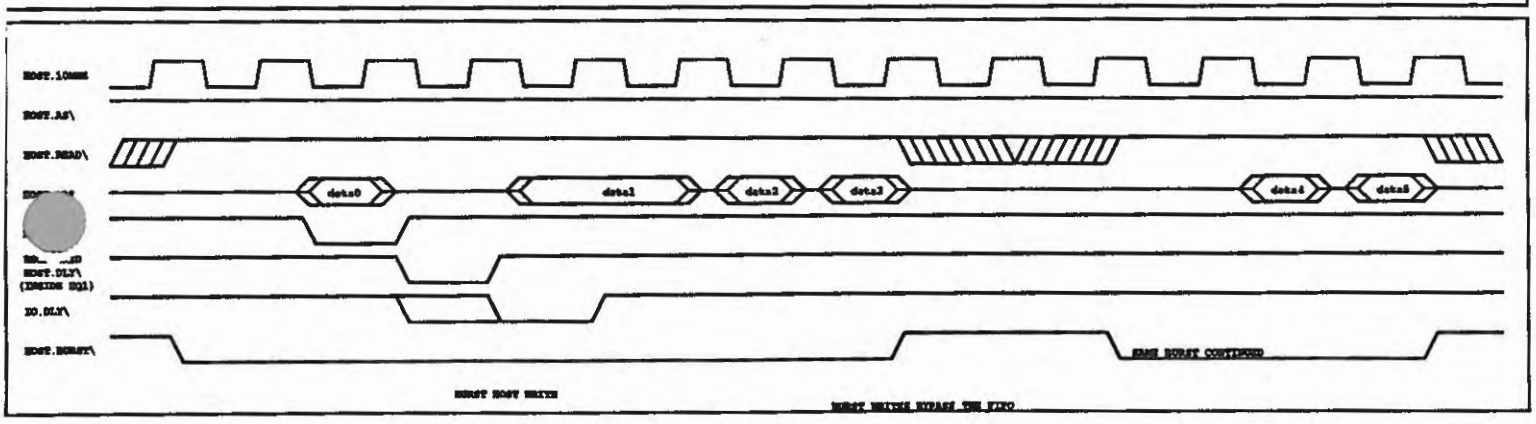


FIGURE 3:

HANDSHAKE SIGNAL TIMINGS





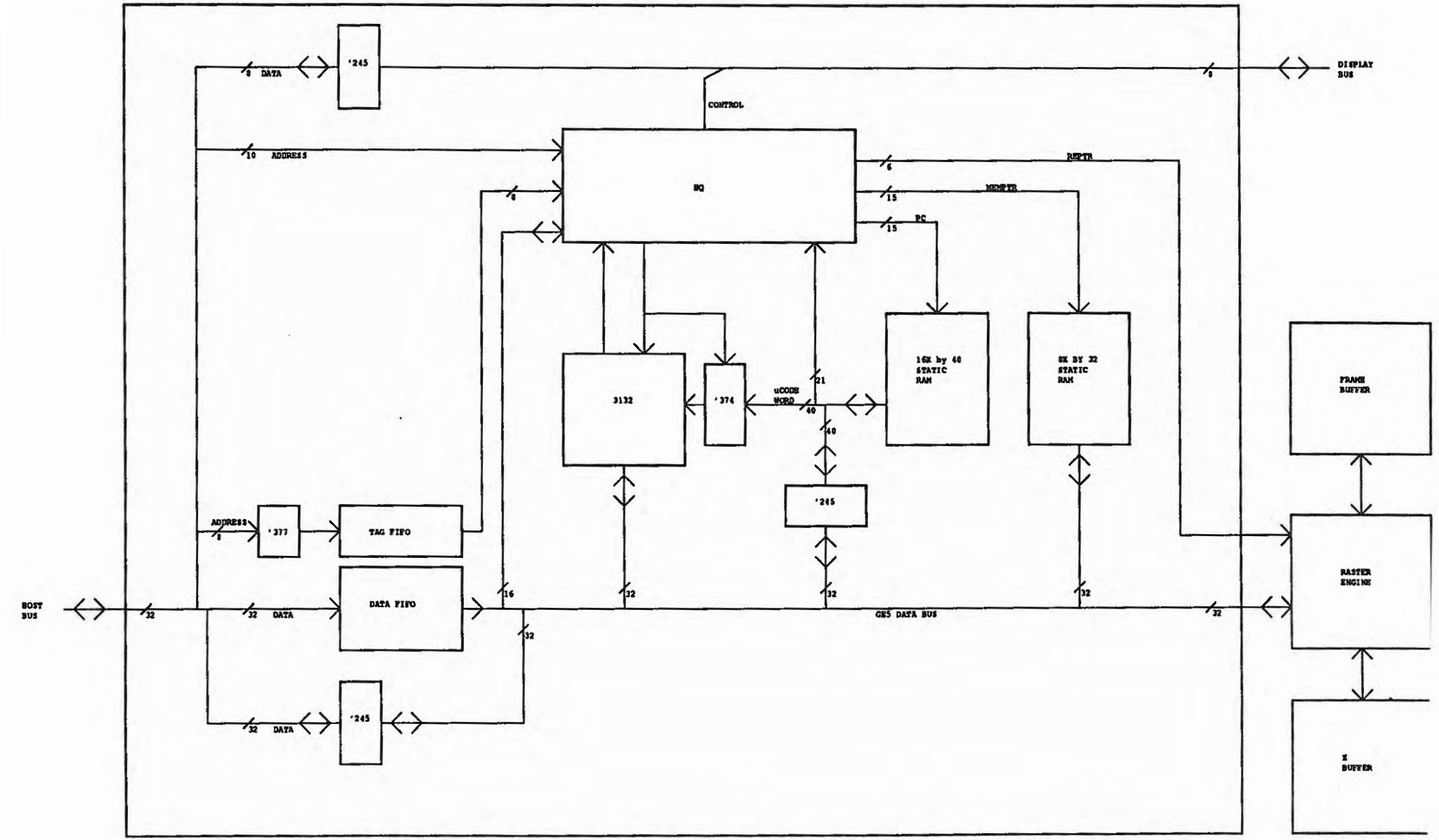
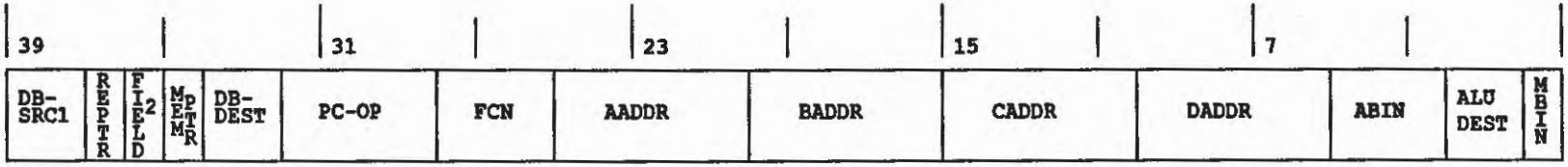


FIGURE 4: GE5 BLOCK DIAGRAM

FIELD ONE



FIELD TWO

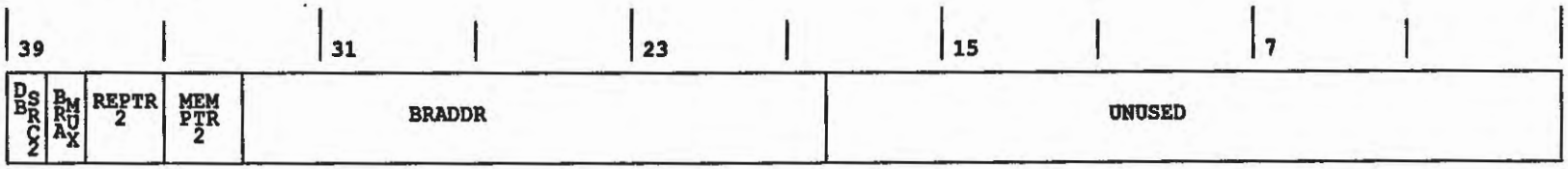


FIGURE 5: MICROCODE WORD DEFINITION