Rockwell

RM 65 DATA SHEET

8K STATIC RAM MODULE

RM 65

The RM 65 product line is designed for OEM and end user microcomputer applications requiring state-of-the-art performance, compact size, modular design and low cost. Software for RM 65 systems can be developed in R6500 Assembly Language, PL/65, BASIC and FORTH. Both BASIC and FORTH are available in ROM and can be incorporated into the user's system.

The RM 65 product line uses a motherboard interconnect concept and accepts any card in any slot. The 64-line RM 65 Bus offers memory addressing up to 128K bytes, high immunity to electrical noise and includes growth provisions for user functions. A selection of card cages provides packaging flexibility. RM 65 products may also be used with Rockwell's AIM 65 Microcomputer for product development and for a broad variety of portable or desktop microcomputer applications.

ORDERING INFORMATION

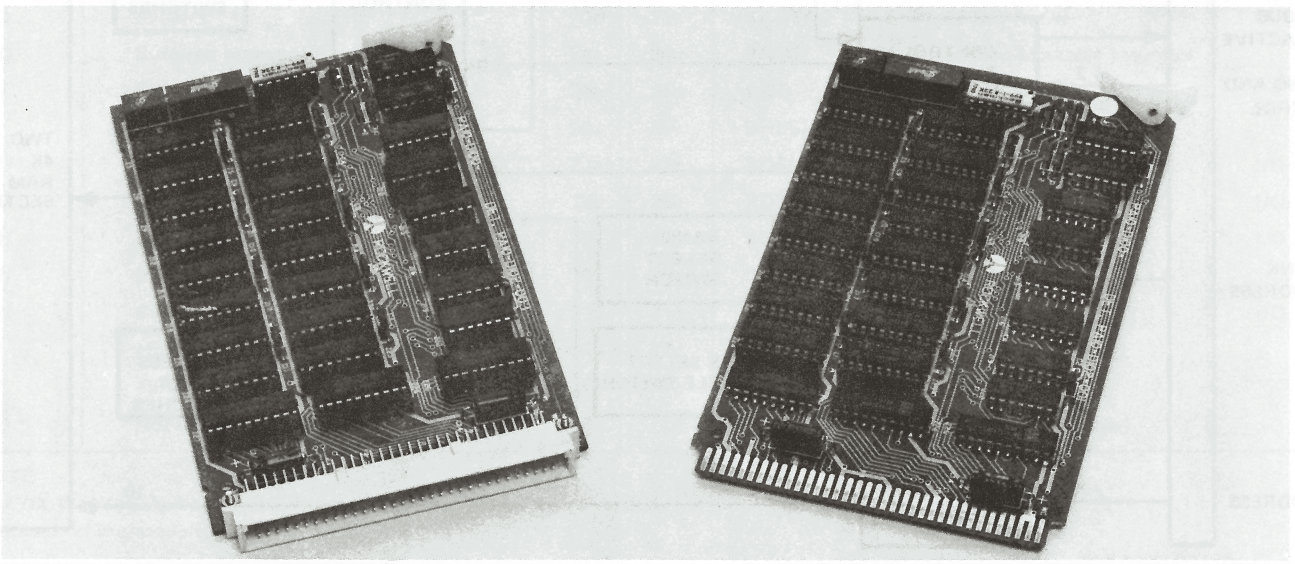
The 8K Static RAM Module is available in an Edge Connector version (RM65-3108) and a Eurocard version (RM65-3108E). These modules may also be ordered without the RAM devices installed, as part numbers RM65-3108N and RM65-3108NE, respectively.

FEATURES

- Compact size – about 4" x 6¼" (100 mm x 160 mm)
- Edge Connector and Eurocard versions
- RM 65 Bus compatible
- Buffered address, data and control lines
- Two separately addressable 4K byte sections
- 16 socketed 2114 static RAM devices
- Write-protect switch for each memory section
- Bank Select and Enable switches
- +5V operation
- Fully assembled, tested and warranted.

PRODUCT OVERVIEW

The RM 65 8K Static RAM Module contains 8192 8-bit bytes of Random Access Memory (RAM), in sixteen 2114 static RAM devices. The memory is arranged as two separately addressable 4K memory sections. The starting address of each 4K section is selectable by on-board address switches. A Bank Select switch allows the RAM module to be assigned to one of two 64K memory banks.



Eurocard Version
RM65-3108E

Edge Connector Version
RM65-3108

Specifications subject to change without notice
Document No. RMA65 N01
Rev. 1, March 1981

FUNCTIONAL DESCRIPTION

8K bytes of static 2114 RAM are divided into two separately addressable 4K blocks. Two devices per 1K bytes are required since each device is 1K x 4 bits.

The Data Transceivers invert and transfer 8-bits of parallel data between the RAM devices and the RM 65 Bus, based on data direction signals from the Data Transceiver Control Circuit.

The Address Buffers invert and transfer 16 address bits from the RM 65 Bus to the RAM devices, to the Base Address Decoders and to the Chip Select Decoder.

The Control Buffers invert and transfer phase 2 clock and read/write control signals from the RM 65 Bus onto the RAM module, and drive the bus active signal onto the RM 65 Bus.

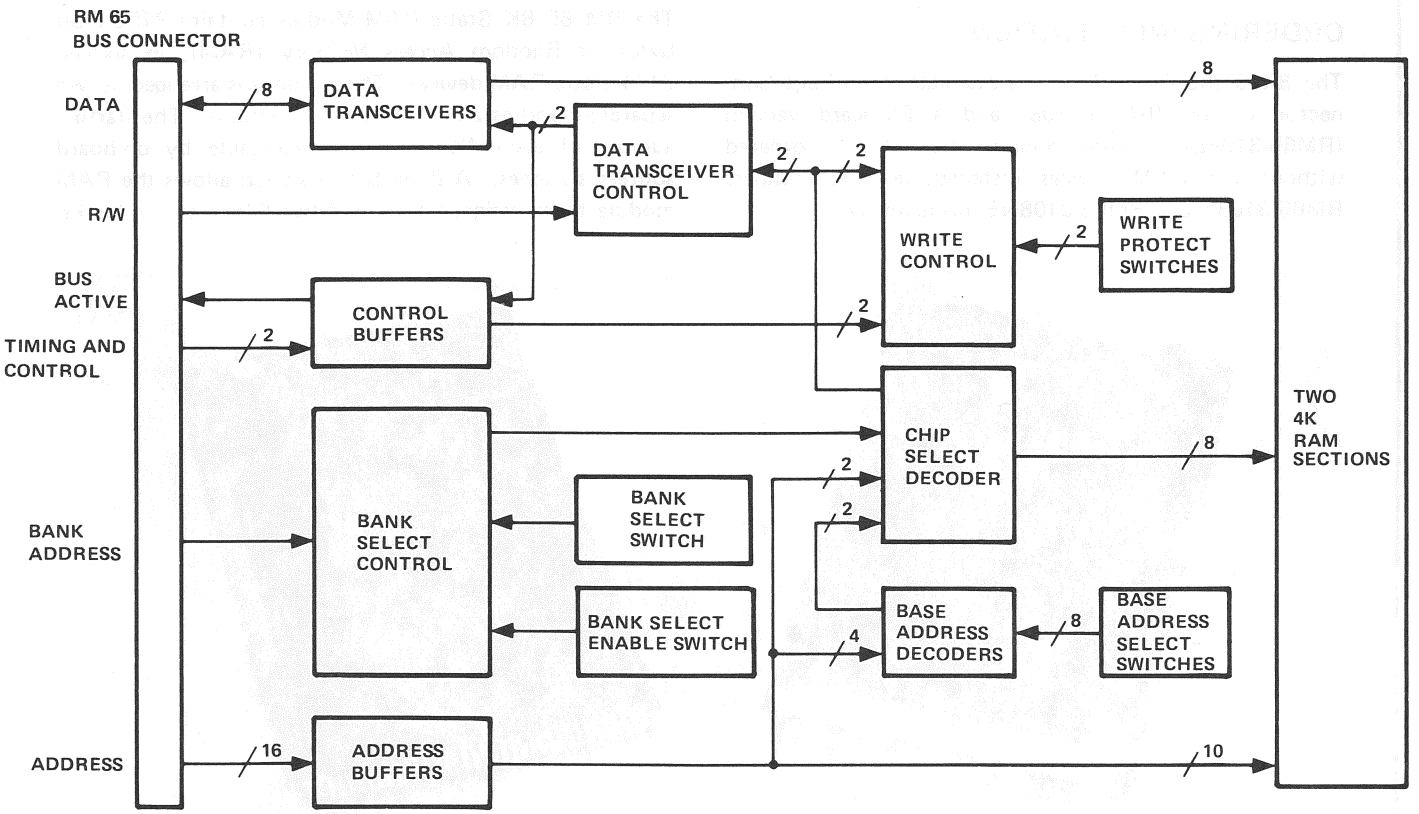
The Bank Select Controller detects when the RAM module's assigned memory bank is addressed, by comparing the bank address signal from the RM 65 Bus to the settings of the Bank Select and Bank Select Enable switches. If the addressed bank is the same as the selected memory bank, an enable signal is sent to the Chip Select Decoder.

Two Base Address Decoders detect when either 4K RAM Section (1 or 2) is addressed, by comparing the address lines to Base Address Select switch settings. When a match occurs, an enable signal is sent to the Chip Select Decoder.

The Chip Select Decoder uses outputs from the Bank Select Control circuit, the Base Address Decoders, and the PROM/ROM size jumpers as well as address lines A11 and A10 to generate one of eight chip select lines to the RAM devices. A signal indicating that a chip select line is active is also sent to the Write Control and Data Transceiver Control circuits.

The Write Control circuit generates the write enable signals to the RAM devices and to the Data Transceiver Control circuit. If the corresponding write protect switch is off, the write enable signal is activated. If the Write Protect switch is on, the Data Transceivers are disabled.

The Data Transceiver Control circuit determines whether a valid read or write operation is in progress, and provides transceiver enable and data direction signals to the Data Transceivers. The Data Transceivers are enabled if both the bank address and the address lines correspond to the selected bank and a selected base address, respectively.



8K Static RAM Module Block Diagram

RM 65 Bus Pin Assignments

Bottom (Solder Side)				Top (Component Side)			
Signal Mnemonic	Signal Name	Input/ Output	Pin	Pin	Signal Mnemonic	Signal Name	Input/ Output
	Not Connected (See Note)		Wa	Wc		Not Connected (See Note)	
+5V	+5 Vdc Line (See Note)		Xa	Xc	+5V	+5 Vdc (See Note)	
GND	Ground		1a	1c	+5V	+5 Vdc	
BADR/	Buffered Bank Address	I	2a	2c	BA15/	Buffered Address Bit 15	I
GND	Ground		3a	3c	BA14/	Buffered Address Bit 14	I
BA13/	Buffered Address Bit 13	I	4a	4c	BA12/	Buffered Address Bit 12	I
BA11/	Buffered Address Bit 11	I	5a	5c	GND	Ground	
BA10/	Buffered Address Bit 10	I	6a	6c	BA9/	Buffered Address Bit 9	I
BA8/	Buffered Address Bit 8	I	7a	7c	BA7/	Buffered Address Bit 7	I
GND	Ground		8a	8c	BA6/	Buffered Address Bit 6	I
BA5/	Buffered Address Bit 5	I	9a	9c	BA4/	Buffered Address Bit 4	I
BA3/	Buffered Address Bit 3	I	10a	10c	GND	Ground	
BA2/	Buffered Address Bit 2	I	11a	11c	BA1/	Buffered Address Bit 1	I
BA0/	Buffered Address Bit 0	I	12a	12c	BØ1	*Buffered Phase 1 Clock	
GND	Ground		13a	13c	BSYNC	*Buffered Sync	
BSO	*Buffered Set Overflow		14a	14c	BDRQ1/	*Buffered DMA Request 1	
BRDY	*Buffered Ready		15a	15c	GND	Ground	
	*User Spare 1		16a	16c	-12V/-V	*-12 Vdc/-V	
+12V/+V	*+12 Vdc/+V		17a	17c		*User Spare 2	
GND	Ground Line		18a	18c	BFLT/	*Buffered Bus Float	
BDMT/	*Buffered DMA Terminate		19a	19c	BØ0	*Buffered External Phase 0 Clock	
	*User Spare 3		20a	20c	GND	Ground	
BR/$\overline{W}$/	Buffered Read/Write "Not"	I	21a	21c	BDRQ2/	*Buffered DMA Request 2	
	*System Spare		22a	22c	BR/$\overline{W}$	Buffered Read/Write	I
GND	Ground		23a	23c	BACT/	Buffered Bus Active	O
BIRQ/	*Buffered Interrupt Request		24a	24c	BNMI/	*Buffered Non-Maskable Interrupt	
BØ2/	Buffered Phase 2 "Not" Clock	I	25a	25c	GND	Ground	
BØ2	*Buffered Phase 2 Clock		26a	26c	BRES/	*Buffered Reset	
BD7/	Buffered Data Bit 7	I/O	27a	27c	BD6/	Buffered Data Bit 6	I/O
GND	Ground		28a	28c	BD5/	Buffered Data Bit 5	I/O
BD4/	Buffered Data Bit 4	I/O	29a	29c	BD3/	Buffered Data Bit 3	I/O
BD2/	Buffered Data Bit 2	I/O	30a	30c	GND	Ground	
BD1/	Buffered Data Bit 1	I/O	31a	31c	BD0/	Buffered Data Bit 0	I/O
+5V	+5 Vdc		32a	32c	GND	Ground	
+5V	+5 Vdc (See Note)		Ya	Yc	+5V	+5 Vdc (See Note)	
	Not Connected (See Note)		Za	Zc		Not Connected (See Note)	

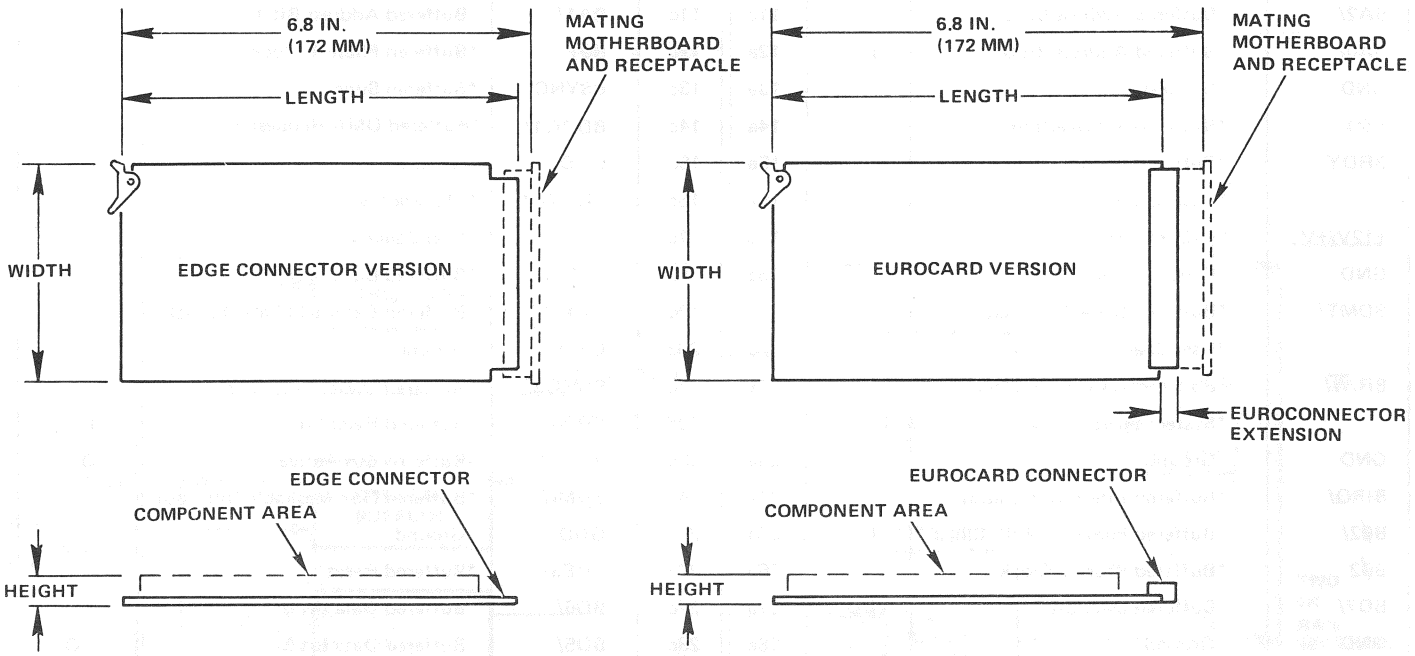
NOTE
Pins Wa, Wc, Xa, Xc, Ya, Yc, Za, Zc are not used on the Eurocard version.
*Not used on this module.

8K Static RAM Module Physical and Electrical Characteristics

Characteristic	Value	
Physical Characteristics (See Notes)		
	Edge Connector	Eurocard
Width	3.9 in. (100 mm)	3.9 in. (100 mm)
Length	6.5 in. (164 mm)	6.3 in. (160 mm)
Height	0.56 in. (14 mm)	0.56 in. (14 mm)
Weight	4.9 oz. (135 g)	5.3 oz. (145 g)
Environment		
Operating Temperature	$0^{o}C$ to $70^{o}C$	
Storage Temperature	$-40^{o}C$ to $+85^{o}C$	
Relative Humidity	0% to 85% (Without condensation)	
Power Requirements	+5 Vdc ±5% @ 1.0A (5.0W) – Typical 1.9A (9.5W) – Maximum	
Access Time	450 ns – Maximum	
RM 65 Bus Interface		
Edge Connector Version	72-pin edge connector (0.100 in centers)	
Eurocard Version	64-pin plug (0.100 in centers) per DIN 41612 (Row b not installed)	

NOTES:

1. The height includes the maximum values for component height above the board surface (0.4 in. for populated modules), printed circuit board thickness (0.062 in.), and pin extension through the bottom of the module (0.1 in.).
2. The length does not include the added extension due to the module ejector.
3. The Eurocard dimensions conform to DIN 41612.



Module Dimensions

ELECTRONIC DEVICES DIVISION REGIONAL ROCKWELL SALES OFFICES

HOME OFFICE
Electronic Devices Division
Rockwell International
3310 Miraloma Avenue
P.O. Box 3669
Anaheim, California 92803
(714) 632-3729
TWX: 910 591-1698

UNITED STATES
Electronic Devices Division
Rockwell International
1842 Reynolds
Irvine, California 92626
(714) 632-3710
DDD (714) 545-6227

Electronic Devices Division
Rockwell International
921 Bowser Road
Richardson, Texas 75080
(214) 996-6500
Telex: 73-307

Electronic Devices Division
Rockwell International
10700 West Higgins Rd., Suite 102
Rosemont, Illinois 60018
(312) 297-8862
TWX: 910 233-0179 (RI MED ROSM)

Electronic Devices Division
Rockwell International
5001B Greentree
Executive Campus, Rt. 73
Marlton, New Jersey 08053
(609) 596-0090
TWX: 710 940-1377

EUROPE
Electronic Devices Division
Rockwell International GmbH
Fraunhoferstrasse 11
D-8033 Munchen-Martinsried
Germany
(089) 859-9575
Telex: 0521/2650

Electronic Devices Division
Rockwell International
Heathrow House, Bath Rd.
Cranford, Hounslow,
Middlesex, England
(01) 759-9911
Telex: 851-25463

FAR EAST
Electronic Devices Division
Rockwell International Overseas Corp.
Itohpia Hirakawa-cho Bldg.
7-6, 2-chome, Hirakawa-cho
Chiyoda-ku, Tokyo 102, Japan
(03) 265-8806
Telex: J22198

YOUR LOCAL REPRESENTATIVE