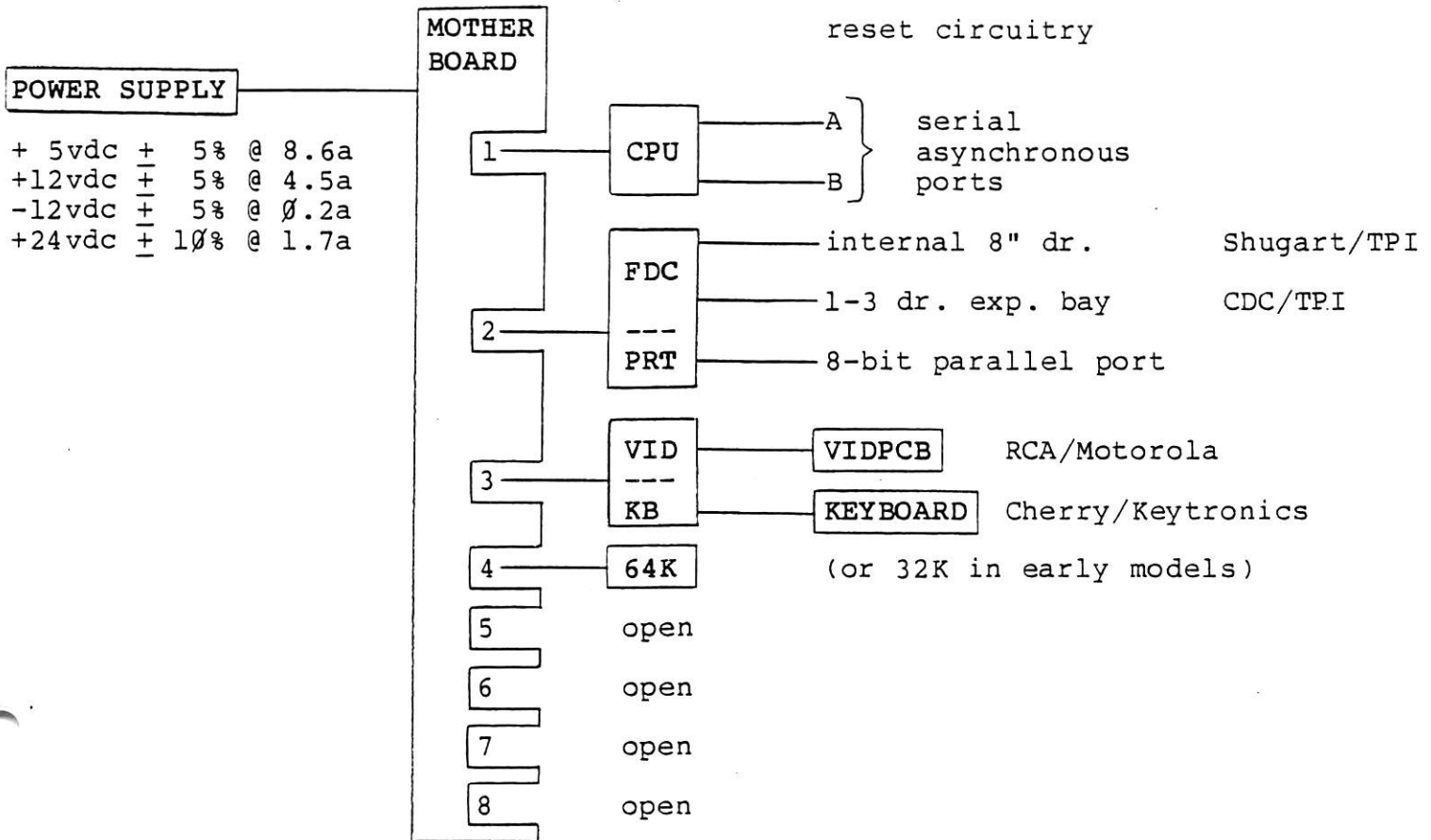


INTRODUCTION  
MODEL II BLOCKS

STANDARD CONFIGURATION



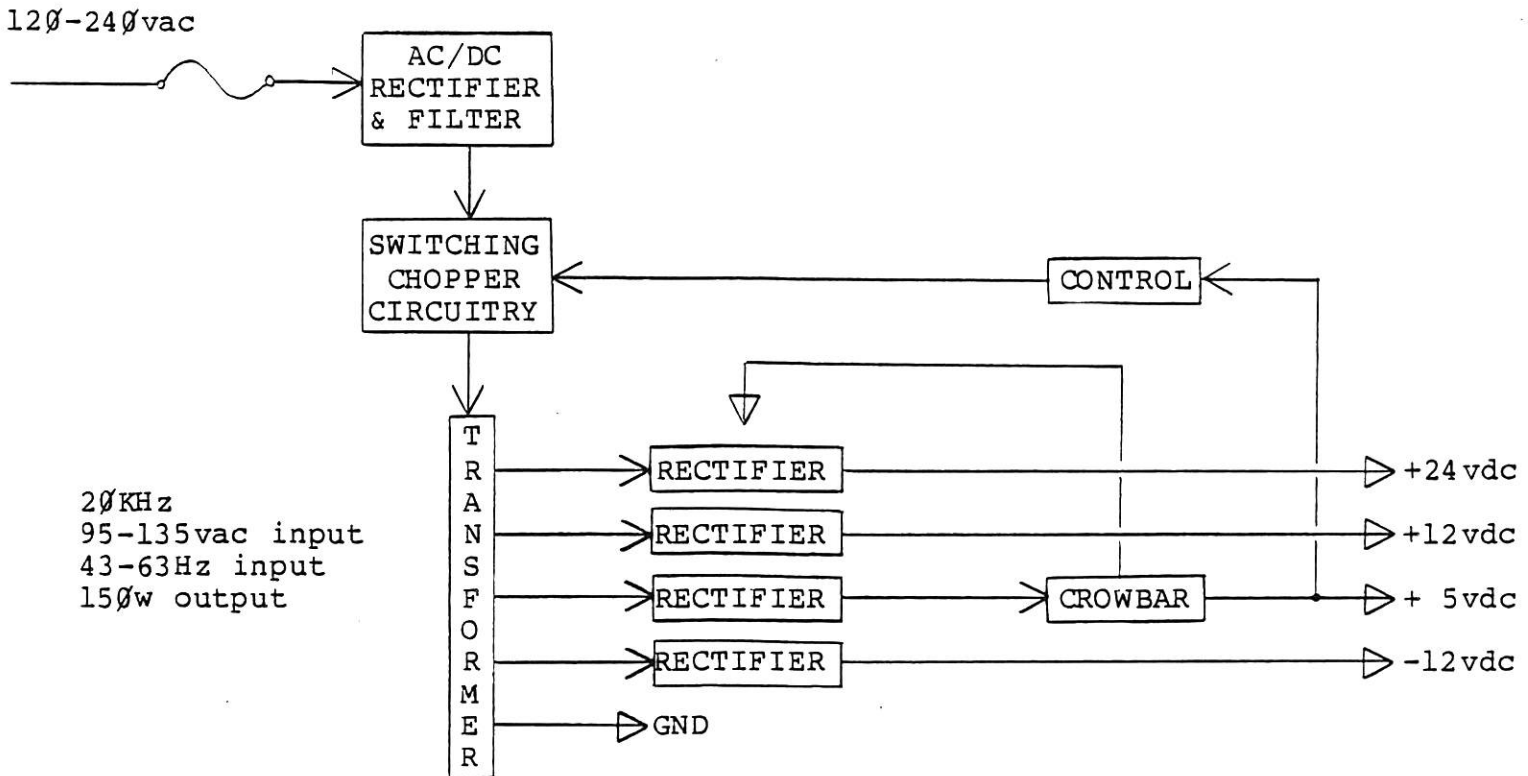
BOARD ORDER WITH OPTIONAL ADD-ON CONFIGURATIONS

	Characteristics	Modifications	Versions
1. CPU	Z80A/4MHz, Boot ROM	Hard Disk, Bisynch	Rev. A-D
2. FDC	FM/MFM, pre-comp.	Rev. A/B, sat. bd.	Rev. A-D
3. HARD DISK	8 Meg or 12 Meg		
4. ARCNET	2-255 Machines		
5. VID/KB	15 MHz Bandwidth		
6. HI-RES	640 x 240		
7. 64K		7a. 32K 7b. 32K add-on	
8. 64K	Visicalc only	jumpers	
9. 144K	Arcnet only		
10. 68000 CPU	6MHz		
11. 128/256K	68000 RAM	jumpers	
12. 384/512K	68000 RAM	jumpers	

Note: not all optional add-ons can be configured in the Model II together

MODEL II  
POWER SUPPLIES

BLOCK DIAGRAM



See Section 9, Model II TRM

*150 watt supplies*

SPECIFICATIONS OF 4 TYPES

NP STOCK NO.	AXX-6003		AXX-6008	AXX-6009
PART NO.	80	81	81A	82
	<i>big black box</i>	<i>no black box</i>		<i>caps standing up.</i>
+ 5vdc $\pm$ 5%	Note 1	8.6a	13.6a	13.4a
+12vdc $\pm$ 5%	Note 2	4.5a	2.5a	2.5a
-12vdc $\pm$ 5%	Note 3	0.2a	0.2a	0.2a
+24vdc $\pm$ 10%	Note 4	1.7a	1.7a	1.7a
FUSES	1	1/3	1/3	1/3
OTHER			TRIM POT	
NUMBER OF MODEL II BOARDS	4	4	5	6-8

WARNING: Never run unloaded, since they can then go into dangerous oscillation.

- Note 1: Used by TTL throughout Model II
- Note 2: Used by RS232C, VCO (old style FDC), RAM, CRT
- Note 3: Used by RS232C, VCO (old style FDC), RAM, discrete (not LSI) disk controller board
- Note 4: Used by disk driver motors and head load solenoid

MODEL II/16/12/16B  
DISK OPERATING SYSTEMS

Version	Issued For	Upward Compatability	Characteristics
TRSDOS 1.2	The first system for early RS application packages	XFERSYS to 2.0 except ML prog's using DOS routines directly	Single Directory No keyahead Slow backup
TRSDOS 2.0	Improvement over 1.2 for early packages and for new ML programs	All 1.2 SVC's honored 1.2 data files transferable. Different Directory structure	Alternate Dir. Keyahead Better backup Bigger LIB
TRSDOS 1.2a	Software "fix" to an		
TRSDOS 2.0a	01-FDC problem		
TRSDOS 2.0b	2.0a for Thinlines	All 2.0a packages	Single-sided
<p>Versions 1.2 - 2.0b have 96 file maximum directory, use 26 sectors/Tk (25 user + 1 system), 77 Tracks (0-76) with 0 as boot in FM, 1-76 in MFM, 0.5 MByte storage, pre-comp at Track 44, retry R/W on disk error, use dynamic file allocation (pre-settable) at 5 Sectors per Granule, support both FLR and VLR files</p>			
TRSDOS 4.0	Double-sided Thinline and Hard Disk DOS (Will also manage single-sided floppies in Thinlines)	2.0 SVC's honored and expanded. 2.0 data files transferable, most application packages FCOPY'able	Has defects. Not to be used
TRSDOS 4.1	Correction of problems in 4.0.	Packages should be put on 4.2	
TRSDOS 4.2	Improved version of 4.1 for better disk I/O	Presently the basis for all RS software Cannot directly R/W with 1.2-2.0b. FCOPY	Thinlines and 8/12M HD
TRSDOS 4.2.5	Special version for use with WD-1010		
TRSDOS 4.2.6	Special version for Hard Drives with >256 Cylinders. Limited No.		
TRSDOS 4.3	Special version for use in ARCNET systems. Not considered an upgrade from 4.2		
TRSDOS 4.3.11	Now available - may use 15 meg HD's in ARCNET		
TRSDOS 16	Operating system for the 68000 CPU: on diskette with TRSDOS 4.2		

4.x versions format single- and double-sided floppies at 32 Sectors/Tk. Single-sided still uses 77 Tracks (0-76), 0.622 MBytes storage. Double-sided uses 154 Tracks (0-153), 1.25MBytes storage. Track 0 is boot for both in FM, 1-76 or 1-153 in MFM, precomp at level of Track 44, retry R/W on disk error, use dynamic file allocation with single-sector allocation, support both FLR and VLR.

4.x versions format Hard Disks at 17-512 Byte Sectors/Tk. 8M HD uses 256 Cylinders, 4 Heads, 1024 Tracks (8.91MB). 12M HD uses 230 Cylinders, 6 Heads, 1380 Tracks (12.01MB). 15M HD uses 306 Cylinders, 6 Heads, 1836 Tracks (15.98MB) MFM, precomp, dynamic file allocation single-sector.

C/P/M - 3.0. Hardware needs.

XENIX requires 256 K...

9 versions of boot ROM  
all upward compatible

## INTRODUCTION

### MODEL II/16 POWER UP SEQUENCE AND SELF-DIAGNOSIS

1. On power up, before the "Insert Diskette" message, the Model II:
  - .switches BOOT ROM in, addressed as the lower 2K of memory
  - .initializes stack at 2800H, enables vidram, disables RTC
  - .resets DMA, <sup>5 times</sup> disables CTC, PIO, resets SIO
  - FE00-FFF vidram*.fills video white (A0) in 40 character mode with a block move
  - .initializes CRTC synchronization, cursor (now flashing)
  - .does a ROM checksum to test ROM integrity
  - .checks main and alternate Z80A registers except IR, IX, IY, SP, PC
  - .checks lower RAM, 1000H - 7FFFH
  - .flushes the keyboard buffer (skips if not ready)
  - .looks for HDC, restores all HD's to Tk0
  - .programs FDC
  - .displays "Insert Diskette" message if no HD, else boot from HD
  - .loop resets FDC until diskette is in *Index pulses - drive closed switch signal  
→ from boots.*
2. After insertion of the diskette, the Model II:
  - .checks the door close switch
  - .clears the screen, seeks Tk0, sets up to read Sector 1, checks FDC
  - .checks format of Sector 1, loads at 1000H; loads diagnostic routine from next Sectors at 1400H, calls diagnostics
  - .checks step direction and step pulse, checks Track 0, does a head load and disk read, checks high memory (8000H-FFFFH), etc.
  - .jumps to bootstrap at 1000H. ROM is now done.
  - .bootstrap code now starts process of loading TRSDOS into base page at 0000H, and loads the diskette DIRECTORY.
  - .TRSDOS displays the Tandy logo, the license notice, and stops for operator input at the date stamp.

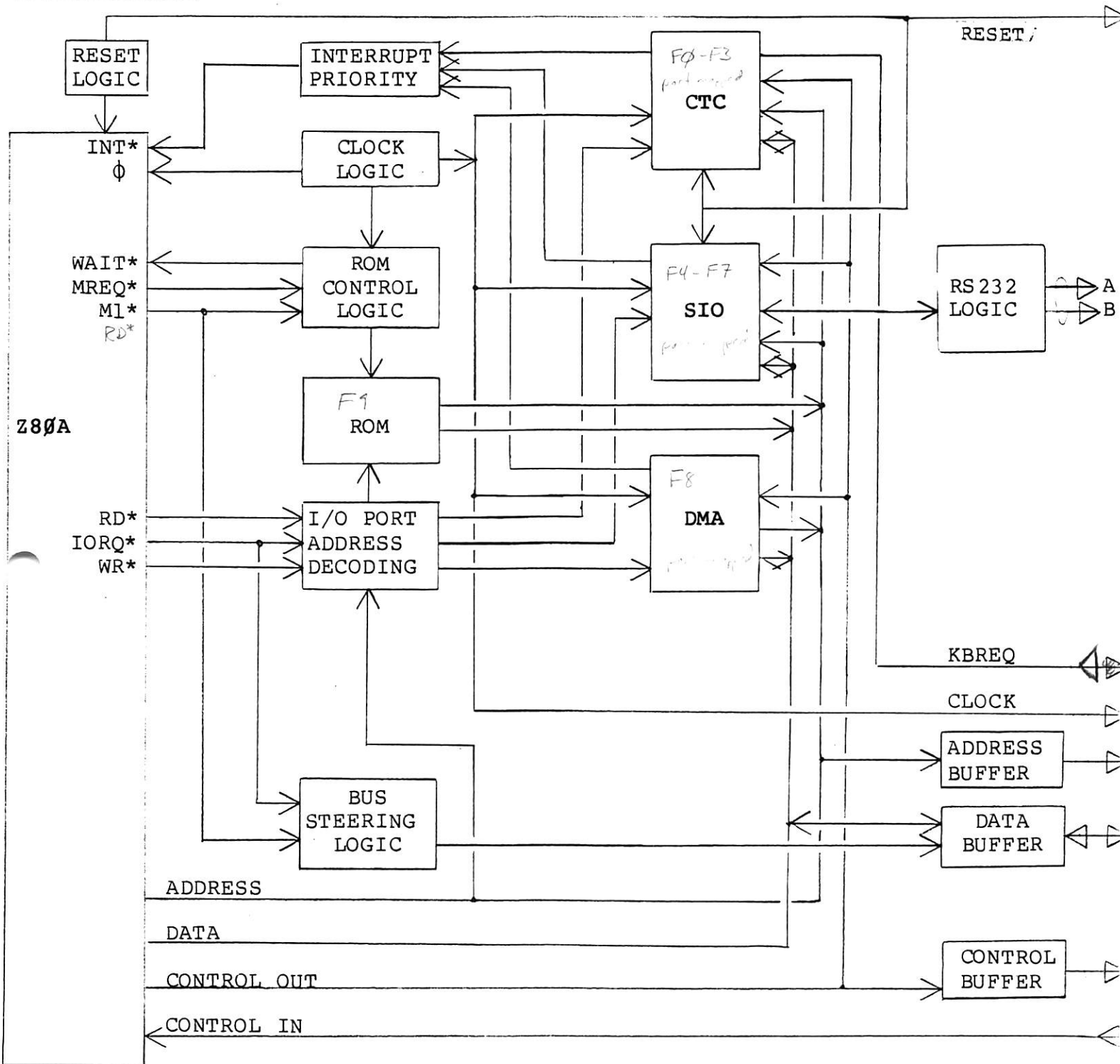
TRSDOS @ about 24 K

INTRODUCTION  
MODEL II BOOT ERROR CODES

- .DC - FDC error
- .DØ - Drive Ø not ready
- .SC - CRC - Bad data or bad diskette
- .TK - Record not found on bootstrap track
- .LD - Lost data during read
- .RS - Non-Radio Shack Diskette
- .CK - ROM checksum error
- .Z8 - Z8ØA error
- .MF - RAM fault, lower 32K *or LM*
- .PI - PIO chip failure
- .DM - DMA chip failure
- .MB - RAM fault
- .MH - RAM fault, upper 32K
- .SI - SIO chip failure
- .TM - turn on 8 meg @ hit break ~~key~~ (time out)*

MODEL II  
CENTRAL PROCESSING UNIT

BLOCK DIAGRAM



**Z80A (A)**

**DMA (B)**

**ROM (C)**

**ADDRESS BUFFER (D)**

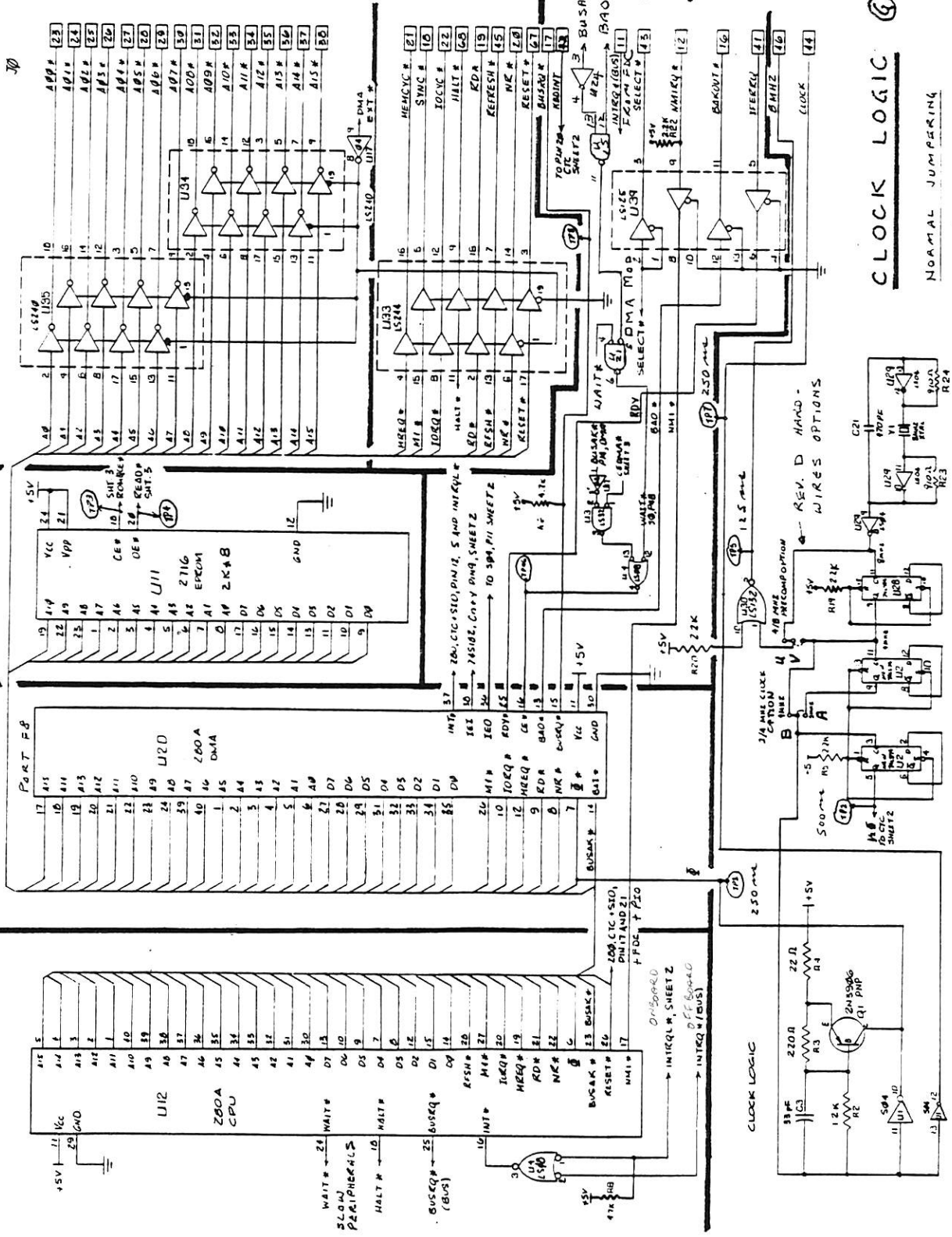
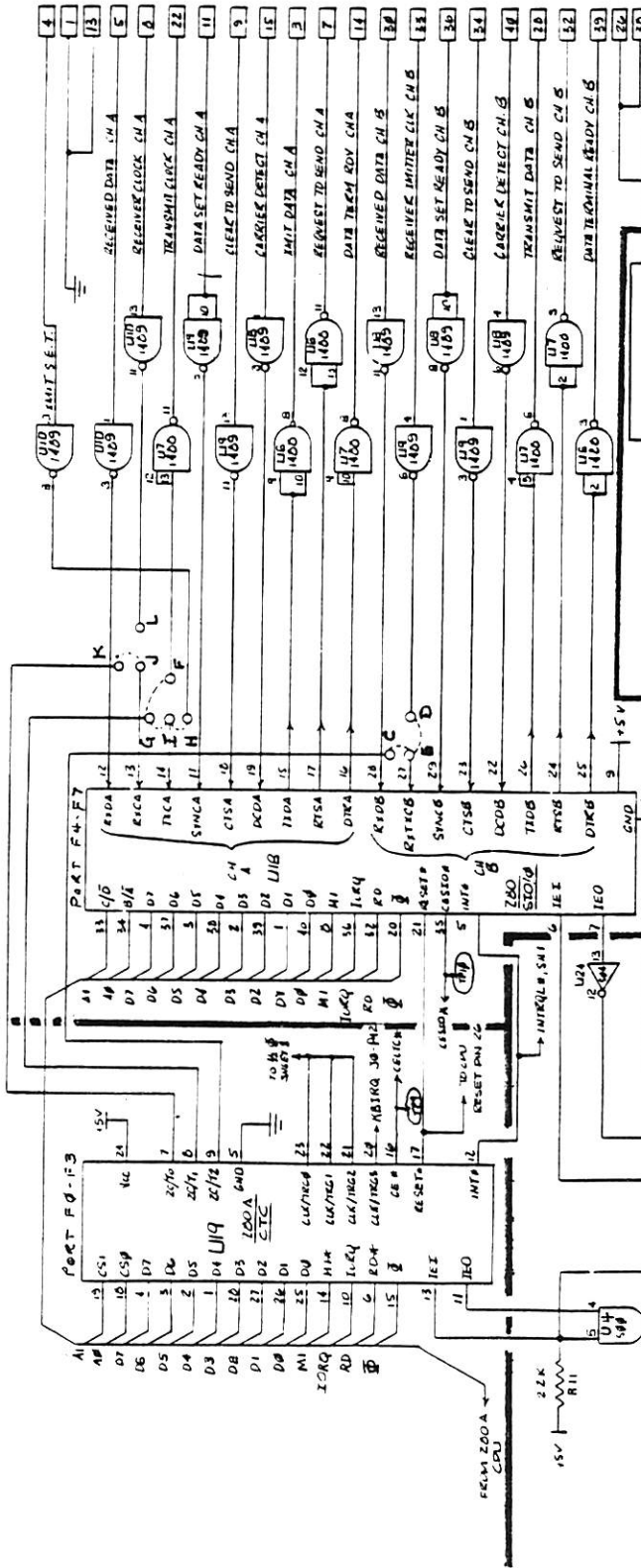


Figure 3. CPU Schematic Diagram - Sheet 1  
REV. C  
Diver's choice  
Clock Conditioning  
CLOCK LOGIC  
NORMAL JUMPING  
B-A\* U-V  
CONTROL BUFFER (E)  
CONTROL IN (F)

CTC (H)

SIO

RS232C LOGIC (I)



# INTERERRUPT PRIORITY

(J)

# ROM CONTROL

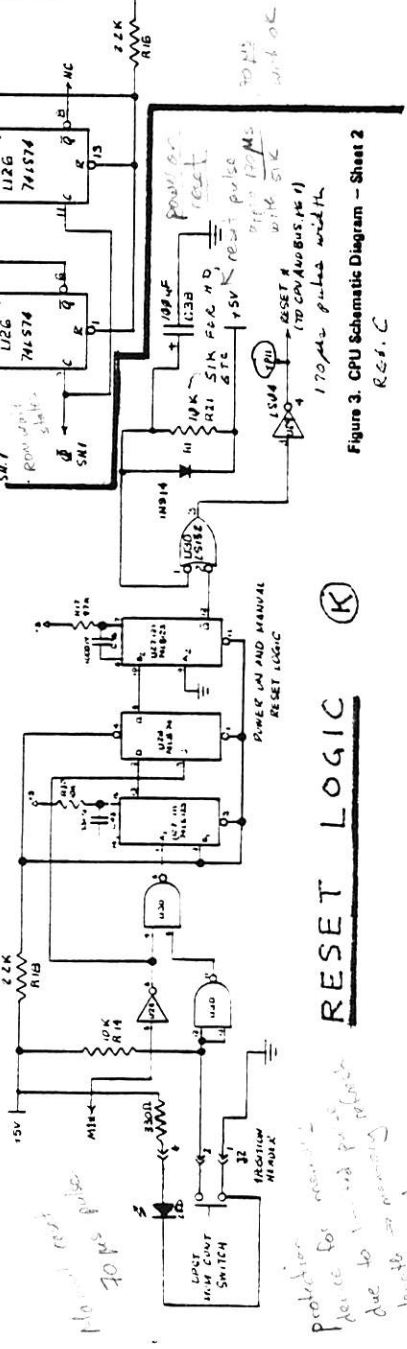
NORMAL JUMPING  
N-P S-T  
& RAM control

(L)

Figure 3. CPU Schematic Diagram - Sheet 2

# RESET LOGIC

(K)



power on reset pulse  
170µs pulse width  
15V reset pulse  
with SW

production  
due to memory  
issues

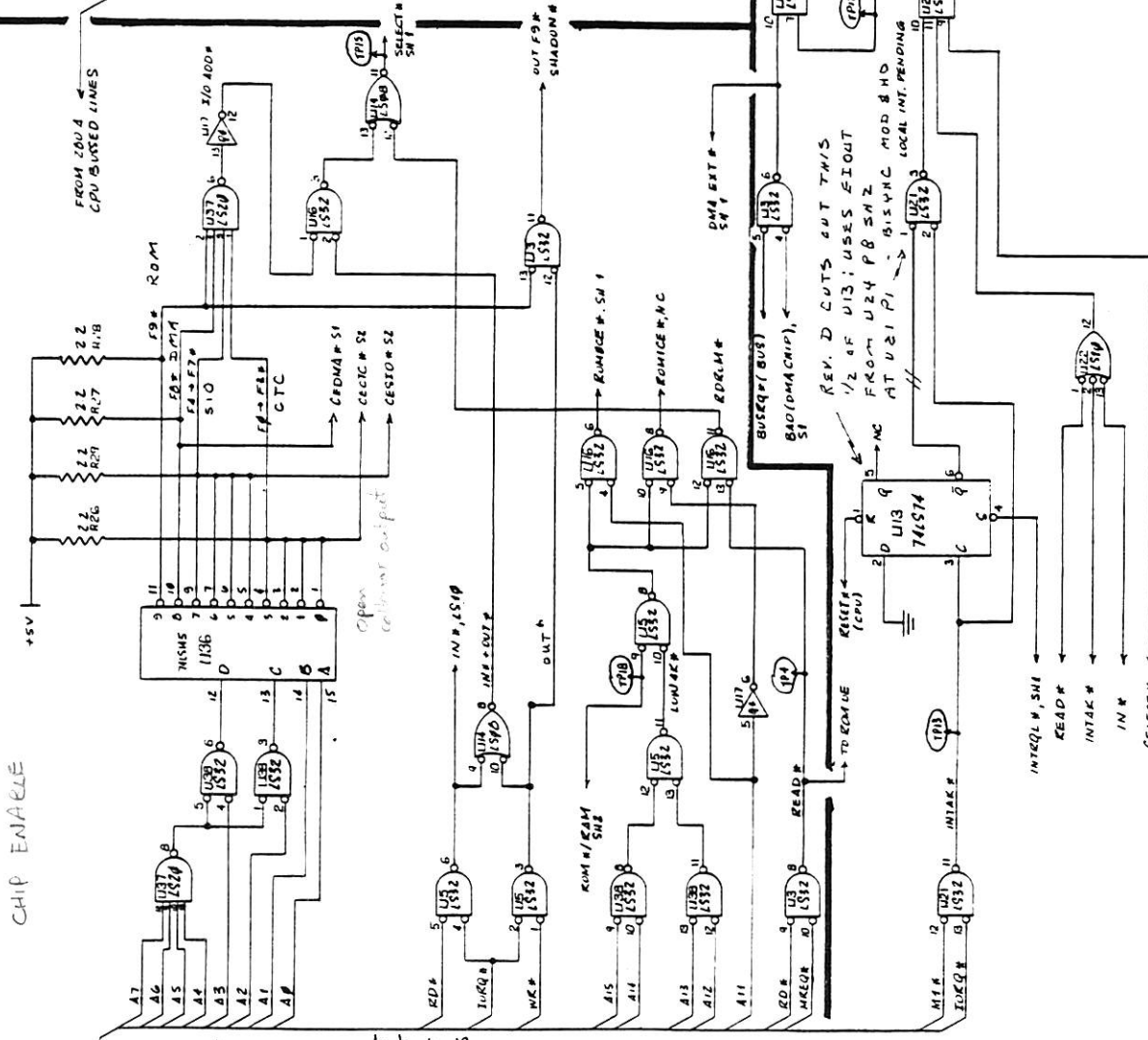


# I/O PORT ADDRESS DECODING

## CHIP ENABLE

BUSSIED DATA LINES FROM ZERO A CPU

PORT ALLOCATION	DATA
F0	CTC
F1	CTC
F2	CTC
F3	CTC
F4	SIOA DATA
F5	SIOB DATA
F6	SIOA CMD/ST
F7	SIOB CMD/ST
F8	DATA
F9	ROM EN/DIS



# BUS STEERING LOGIC

# DATA BUFFER

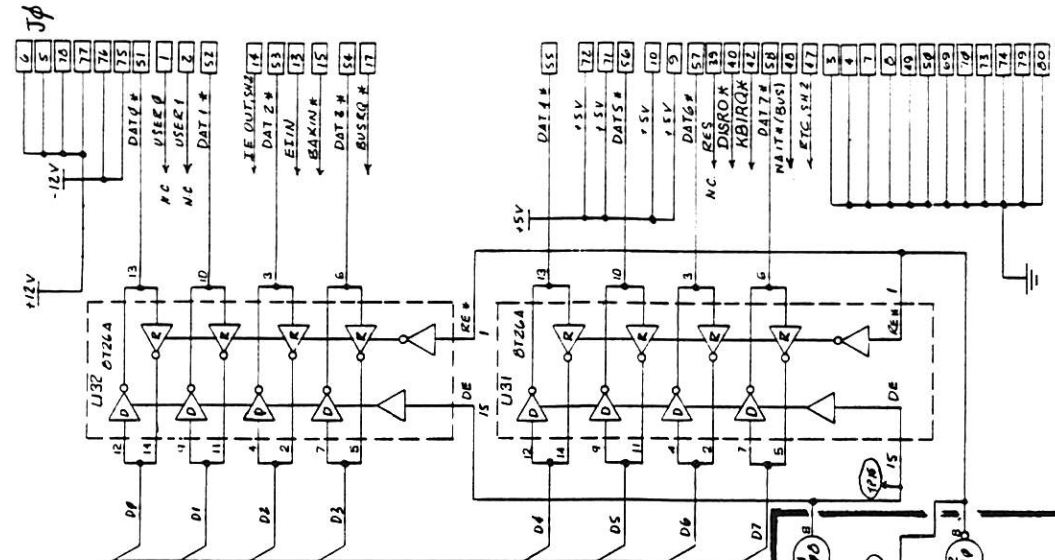
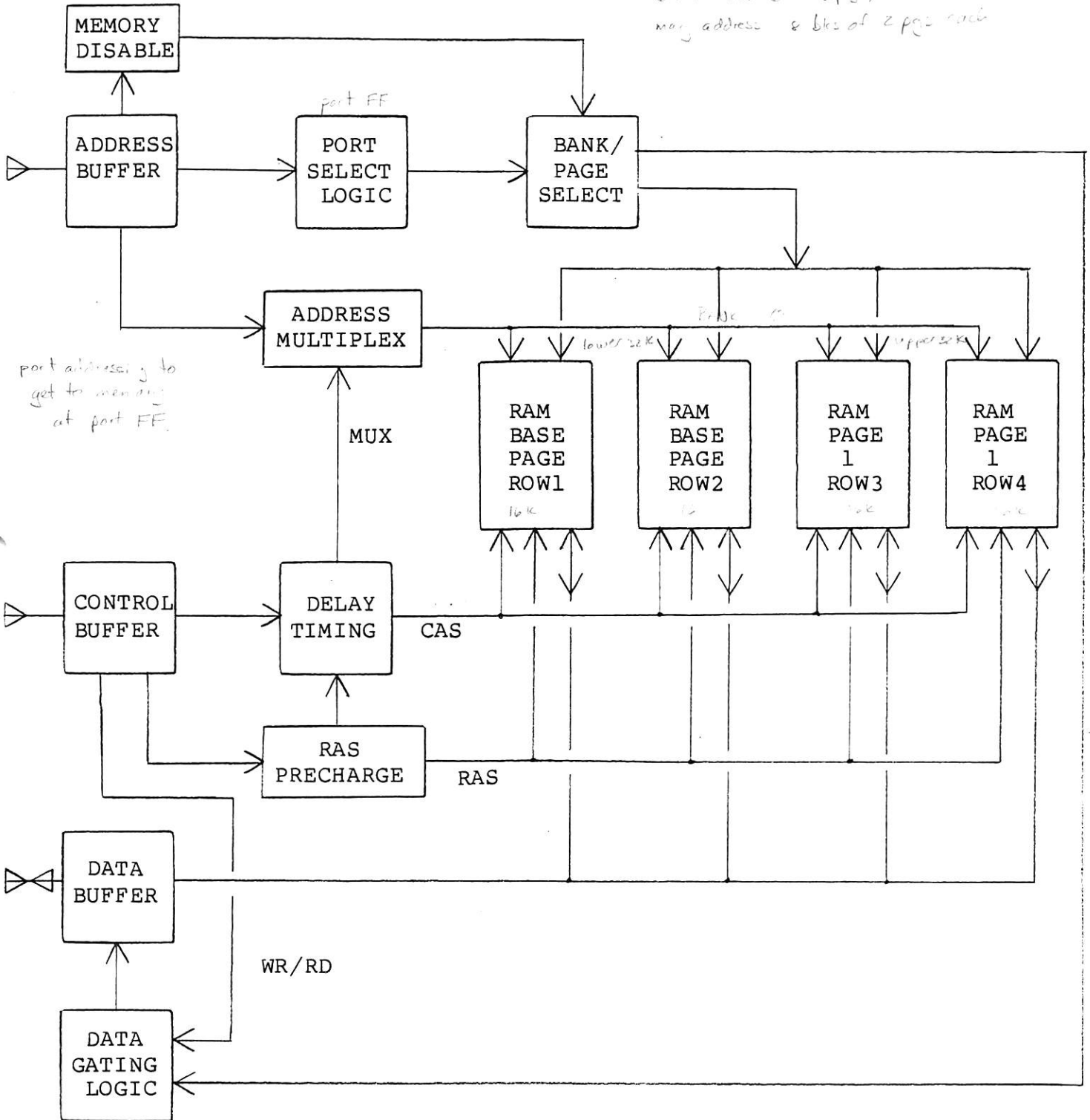


Figure 3. CPU Schematic Diagram - Sheet 3  
REV. C

MODEL II  
64K MEMORY BOARD

BLOCK DIAGRAM

*base page always enabled  
64 K banks ← 2 pgs/bk  
main address & bits of 2 pgs each*



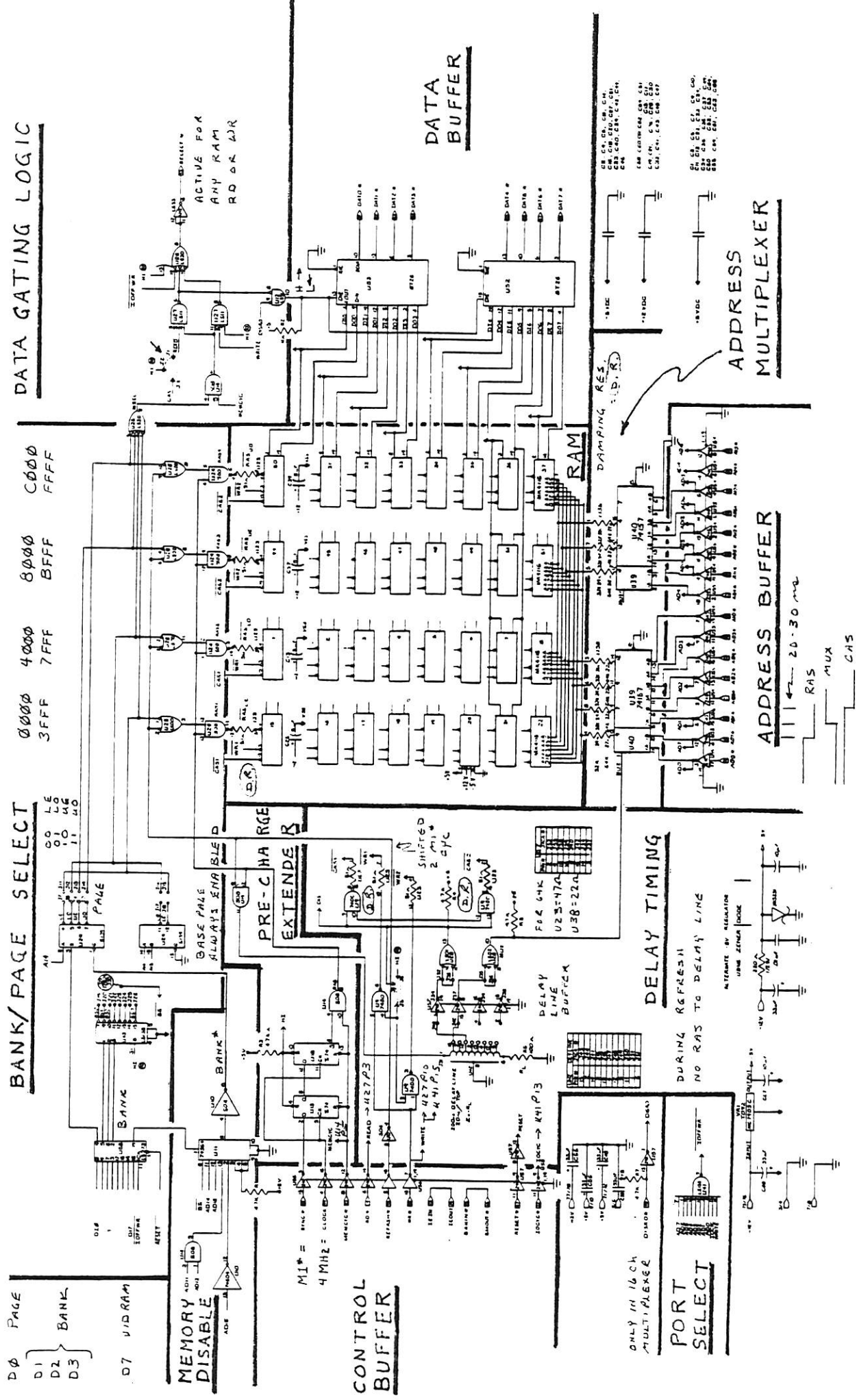


Figure 6. Memory Board Schematic Diagram