STUDENT INFORMATION SHEET

MOTOROLA 68000 MICROPROCESSOR

The intent of this discussion is to give the student a general overview of the 68000 MPU. This is meant to be only an overview, and will hopefully give the reader a chance to develope some backround to the architecture, functions, and capabilities of the 68000.

This is not meant to be an in depth study of the programming features, nor to explain how functions are achieved, but instead to identify the registers and pinouts, and their uses.

Throughout the text we will refer to signals being either "ASSERTED", or "NEGATED". When we say a signal is asserted we mean simply that it is active, regardless of if it is high or low.

If we indicate a signal is negated, we would imply that it is inactive, again without regard to its state.

We can tell if a signal is active HIGH or active LOW by the name. For example if a signal is barred, or ends with the symbol "*" it would indicate an active low, if it has neither then it would be considered active high, in either case we use the term asserted.

If a signal contains the symbol "/" this would indicate that it is used as a control, and is always active. In the case of R/W* if this line is high we are be performing a read operation, if it is low we are performing a write operation. As you can see the signal is always active, however the state of the signal causes quite a change to take place.

PINOUTS

The tables on the following page list the signal groups and give their respective pin assignments. A brief description of each follows.

ADDRESS LINES

A1 - A23 These outputs are used to address the RAM and PERIPHERAL devices. All peripherals are memory mapped. Address line A0 is internal to the 68000 and used to decide if UDS* or LDS* is to be asserted.

LDS* Lower Data Strobe is used to enable an 8 bit memory transfer on the lower 8 data lines (D0 - D7)

UDS* Upper Data Strobe is used to enable an 8 bit memory transfer on the upper 8 data lines (D8 - D15)

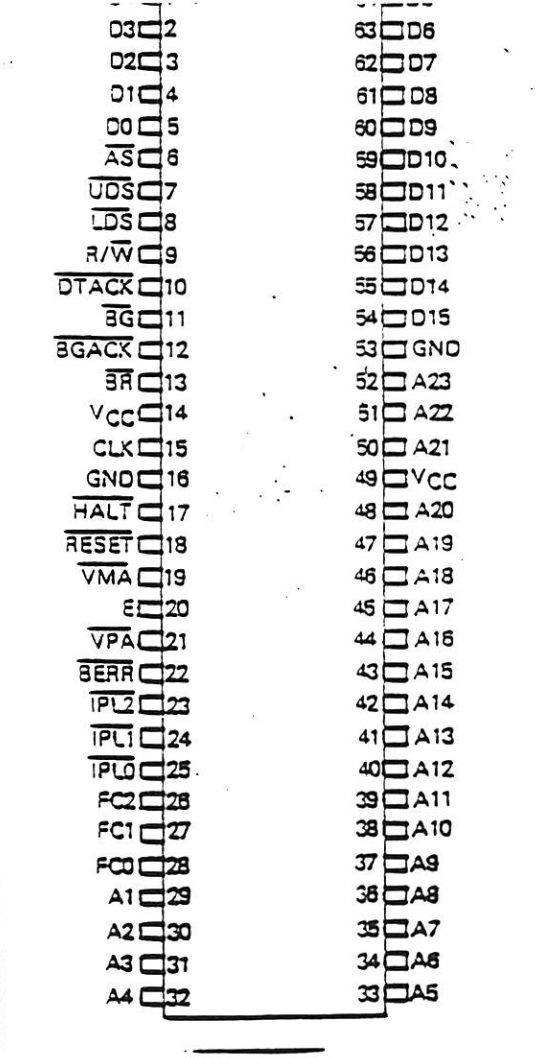
If both LDS* & UDS* are asserted at the same time a 16 bit data transfer would occur. If neither are asserted no transfer can occur.

AS* Address Stobe is used to signify that there is a valid address on the bus.

R/W* Read/Write* is used to indicate if the transfer is a read or a write cycle.

TABLE 1 – SIGNAL SUMMARY

Signal Name	Mnemonic	Input/Output	Active State	Three State
ddress Bus	A1-A23	output	high	yes
ata Bus	D0-D15	input/output	high	yes
r[illegible] Strobe	$\overline{AS}$	output	low	yes
ead/Write	R/$\overline{W}$	output	read-high write-low	yes
pper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	output	low	yes
ata Transfer Acknowledge	$\overline{DTACK}$	input	low	no
us Request	$\overline{BR}$	input	low	no
us Grant	$\overline{BG}$	output	low	no
us Grant Acknowledge	$\overline{BGACK}$	input	low	no
errupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	input	low	no
us Error	$\overline{BERR}$	input	low	no
eset	$\overline{RESET}$	input/output	low	no*
alt	$\overline{HALT}$	input/output	low	no*
able	E	output	high	no
alid Memory Address	$\overline{VMA}$	output	low	yes
alid Peripheral Address	$\overline{VPA}$	input	low	no
unction Code Output	FC0, FC1, FC2	output	high	yes
lock	CLK	input	high	no
ower Input	V_{CC}	input	–	–
round	GND	input	–	–



ASYNCHRONOUS BUS CONTROL

DTACK* Data Transfer ACKnowledge is used to indicate the completion of a bus cycle. All data transfers must create this signal to be sent back to the 68000. If this signal is not recieved within a predetermined amount of time an error would occur.

This signal is present to relieve the need for wait states in the case of slower memory devices. All tranfer cycles are asynchronous, in other words hardware handshaking is supported by the 68000.

We will discuss the necessary sequence of events in detail later.

BUS ARBITRATION CONTROL

In order to maintain a systematic and orderly means of contolling which device is in control of the bus the 68000 employs several control lines called the BUS ARBITRATION LINES. Any device which is using the bus is considered to be the BUS MASTER.

The 68000 considers any request for bus mastership to be of equal priority, and considers itself to have the lowest. External circuitry is used to establish individual priorities and all bus requests are handled through this device.

This external device monitors all requests and status, makes request for the bus to the 68000, and, at the appropriate time, grants bus mastership to the requesting device.

The 68000 bus interface lines and a brief description of each is as follows:

BR* (Bus Request) Used to inform the 68000 that some other device desires to become BUS MASTER.

BG* (Bus Grant) Used to inform the requesting device that the bus will be released at the end of the current bus cycle.

BGACK* (Bus Grant ACKnowledge) Used to indicate to the 68000 that some other device has become bus master. The device requesting the bus cannot assert BGACK* until the following four conditons have been met.

1. a bus grant has been recieved, indicating that the current bus master will relinquish the bus when ready.
2. address strobe is negated indicating, that the 68000 is not using the bus.
3. DTACK* is negated, indicating that no memory or peripheral device is using the bus.
4. BGACK* is inactive, indicating that no other device is still claiming bus mastership. In other words the device requesting bus mastership must monitor the line and wait for any device which is presently using the bus to finish it's bus cycle

EXCEPTION PROCESSING

Before continuing our discussion on the pinouts we must first discuss the 68000's interrupt and error handling routines. The term used to describe this action is EXCEPTION PROCESSING.

MODES OF OPERATION

The 68000 MPU is always in one of three modes of operation. These are normal, exception or, halted.

When the MPU is running an application program we say it is in the normal, or USER mode.

If, for example, an interrupt or error should occur the processor would enter the exception, or SUPERVISOR mode.

PRIVILEGE STATES

There are two privilege states possible, the user state, and the supervisor state. The user has a lower set of privileges then the supervisor These privileges are set up to insure that programs do not enter areas that they do not need and must not modify.

The structure is such that it allows most programs to run in the user mode, allowing access only to the user program and data area as defined by the system.

The operating system executes in the supervisor state, giving it access to all resources, and allowing it to perform any overhead tasks requested by the user state program.

EXCEPTIONS

In a multi-user environment, each user is given a specific and unique area of ram in which program execution and data storage is allowed. If an attempt is made to access a memory location outside a particular users ram area the processor must be informed. The device which informs the processor is called the MEMORY MANAGEMENT UNIT. This is the external support circuitry which sets up the program area and handles the partitioning of ram.

If an error is reported, the 68000 would enter the SUPERVISOR MODE, and exception processing would begin. This is not the only condition that will cause the 68000 to enter exception processing. Some other causes would be an interrupt, devide by zero, illegal instruction, reset, as well as others.

PROCESSING

When an error or exception is encountered the processor handles it in the following manner.

1. A copy of the STATUS REGISTER (more on this later) is made and the status register is set up to run in the SUPERVISOR or EXCEPTION mode.

2. There is a "lookup table" internal to the 68000 which contains several "vectors", one for each type of exception. A vector is simply a binary code which is used as an address reference by the 68000.

The 68000 retrieves the proper vector byte and stores it.

3. The contents of the 68000 registers are stored in ram.

4. The 68000 then retrieves the contents of the ram location pointed to by the vector which was retrieved in step two. The contents of this memory location is used as an address to point the 68000 to the start of an exception processing service routine located in the supervisor area of ram.

The 68000 then performs the exception processing routine as directed by the program at this location. At the end of each exception routine is an RTE (ReTurn from Exception) command which puts the processor back in the user mode.

The following table show the different type of exceptions, as well as there vector numbers, and the address that the 68000 is pointed to.

FIGURE 23 — ADDRESS TRANSLATED FROM 8-BIT VECTOR NUMBER

A23	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
All Zeroes		v7	v6	v5	v4	v3	v2	v1	v0	0	0

TABLE 18 — EXCEPTION VECTOR ASSIGNMENT

Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset: Initial SSP
—	4	004	SP	Reset: Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16-23*	64	04C	SD	(Unassigned, reserved)
	95	05F		—
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	191	0BF		—
48-63*	192	0C0	SD	(Unassigned, reserved)
	255	0FF		—
64-255	256	100	SD	User Interrupt Vectors
	1023	3FF		—

*Vector numbers 12, 13, 14, 16 through 23 and 48 through 63 are reserved for future enhancements by Motorola. No user peripheral devices should be assigned these numbers.

FUNCTION CODES

The 68000 MPU is a highly structured microprocessor. It has the capability of keeping track of both SUPERVISOR and USER ram area. It also devides these areas into their respective program and data ram storage areas.

The function control outputs are used to indicate to the system what section of ram the 68000 is accessing. This information is used to permit or deny access to that area as determined by the system.

For instance, in a multi - user situation, the FC outputs would inform the system which area of ram was being accesed. If a user tries to access outside of his area the memory management would report an error.

If, however, a call was made to an operating system sub-routine we would be in the supervisor mode (as described above) and would need a complete and free run of ram. In order to do this we could monitor the FC outputs and disable the memory management unit any time the 68000 entered the supervisor mode.

As well as indicating where in ram the 68000 is attempting to access, the FUNCTION CODE outputs are used to indicate when an interrupt acknowledge cycle is in progress.

The condition of the outputs inform the system of the status of the 68000.

The truth table for the FCO lines is as follows:

FUNCTION CODE OUTPUT			FUNCTION BEING PERFORMED
FC2	FC1	FC0	
0	0	0	(Unassigned)
0	0	1	USER DATA
0	1	0	USER PROGRAM
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	SUPERVISOR DATA
1	1	0	SUPERVISOR PROGRAM
1	1	1	INTERRUPT ACKNOWLEDGE

READ AND WRITE CYCLES

The following diagrams show the flow charts for read and write memory cycle. The bus master is the device in control of the bus, the slave is the device which the bus master is addressing.

FIGURE — WORD WRITE CYCLE FLOW CHART

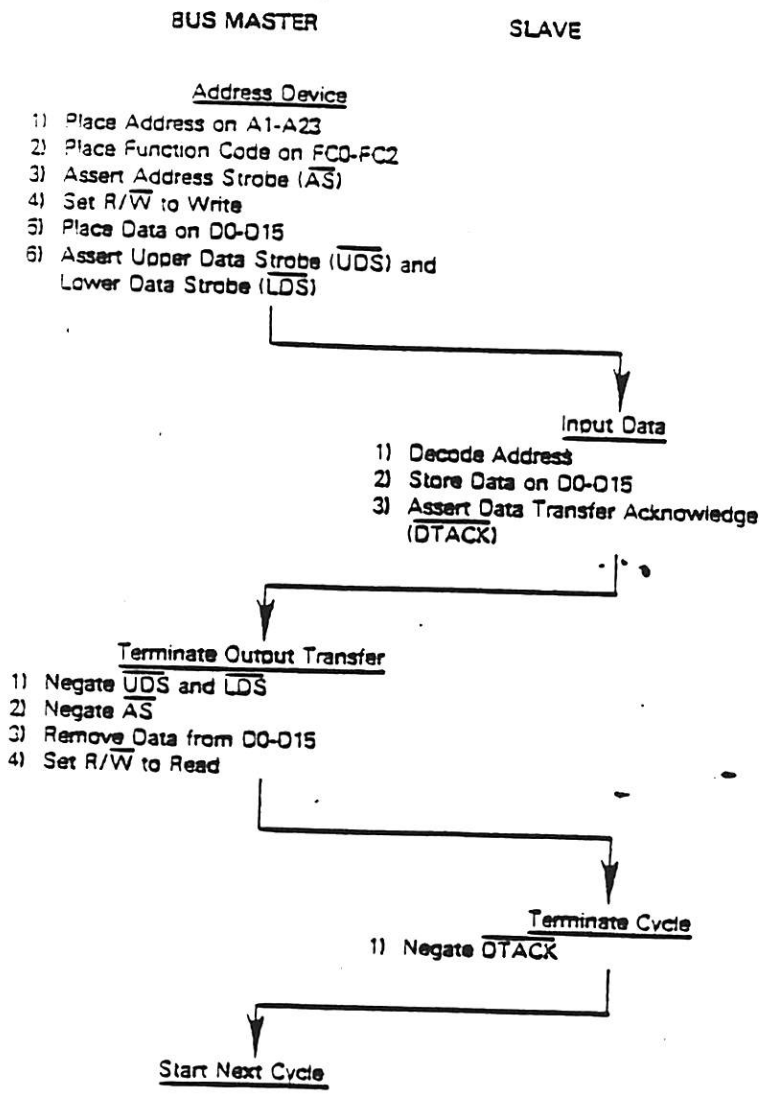


FIGURE — BYTE WRITE CYCLE FLOW CHART

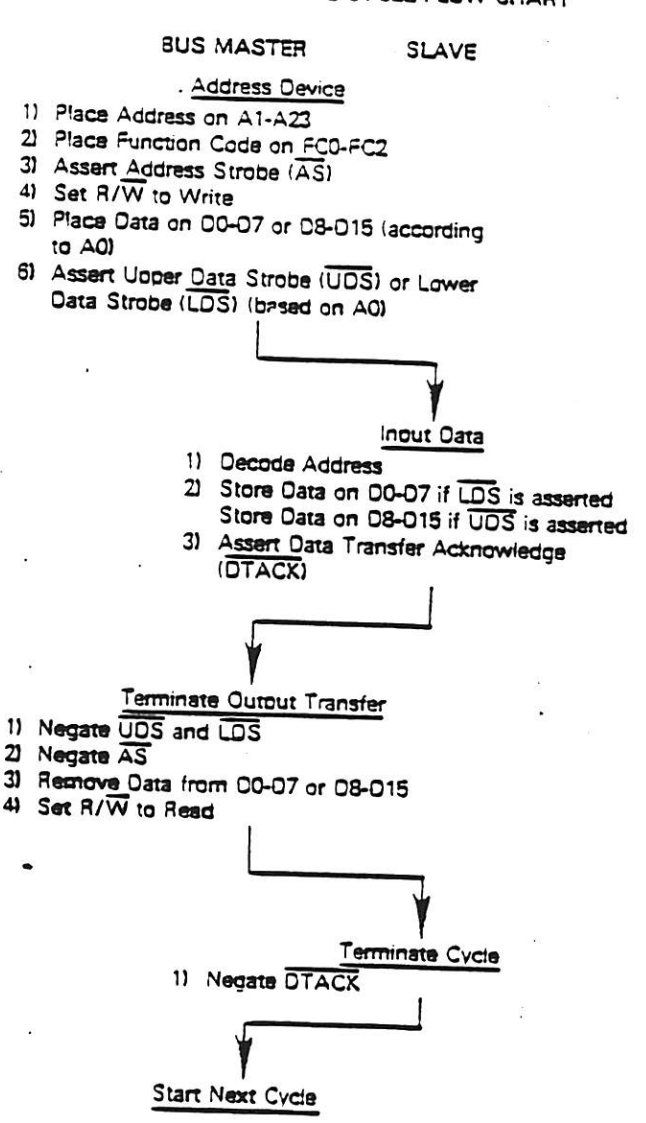


FIGURE — WORD READ CYCLE FLOW CHART

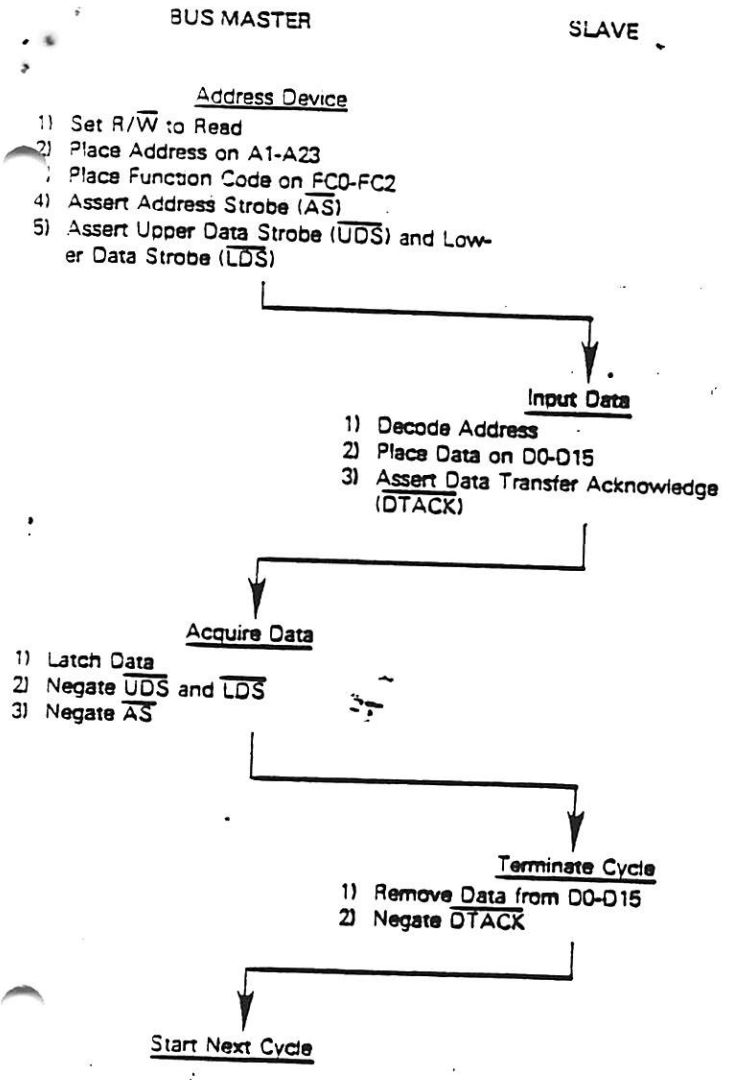
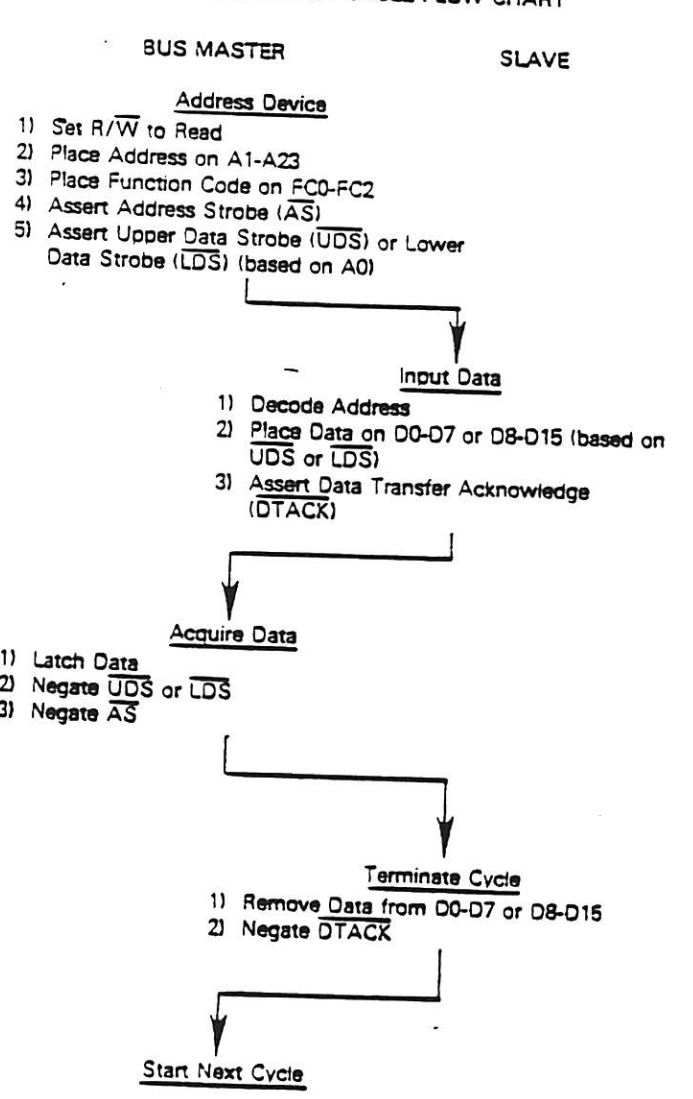


FIGURE — BYTE READ CYCLE FLOW CHART



INTERRUPT CONTROL LINES

The IPL lines are used to inform the 68000 of an interrupt and to assign priorities. The system is set up so that when an interrupt is generated, the device will present it's level to the 68000 by placing a binary code on the IPL lines.

There are 7 levels of interrupts which can be recognized by the 68000. A level 7 interrupt is the highest level interrupt and a level 1 is the lowest. A binary 000 on these control lines indicates no interrupt.

SYSTEM CONTROL LINES

BERR* (Bus ERRor) Used to indicate that an error has occurred during a bus request cycle.

A few examples of bus errors are:

1. an attempt to access memory which is out of the user's boundary

2. no DTACK* response to a data transfer. The reason we need this is if the 68000 does not get a DTACK* it will simply wait for one indefinitely. If no response is received by a predetermined length of time an external watchdog circuit will be used assert BERR*.

HALT If a HALT instruction is received at the same time as BERR* the 68000 will re-run the bus cycle.

The HALT line is also used to allow programmers to single step through a program. This single step feature is a function of the 68000 and is used to provide an easy means of debugging during program developement.

RESET

RESET is a bi-directional pin which may be used to perform a reset to the system devices by the 68000 without performing a 68000 reset, or to reset the 68000 and system devices

The ONLY way to reset the 68000 is to assert BOTH HALT AND RESET at the same time. If a reset is recieved without a halt it will reset all subsystem, but not the 68000 itself.

M6800 PERIPHERAL CONTROL LINES

The 68000 MPU has been designned to work in conjunction with Motorola's 6800 peripheral devices. The following pins are used to interface this group to the 68000.

E (Enable) common to all 6800 peripheral devices and is used to synchronize data transfers.

VPA* (Valid Peripheral Address) Used to inform the 68000 that an address is for a 6800 subsytem, and that the data transfer should be synchronized with the enable pin.

VMA* (Valid Memory Address) Used to inform 6800 subsytem that the address is a valid memory address and the output is synchronized to Enable. This signal is only asserted after the receipt of VPA*.

INTERNAL STRUCTURE

DATA REGISTERS

The 68000 contains 8 inernal data register, D0 - D7. These registers are 32 bits wide, and are capable of handling data in either 8 bit BYTES, 16 bit WORDS, or 32 bit LONG WORDS.

ADDRESS REGISTERS

There are 7 address registers, A0 - A6. These registers are 32 bits wide and can handle either WORDS (16 bits) or LONG WORDS (32 bits).

STACK POINTERS

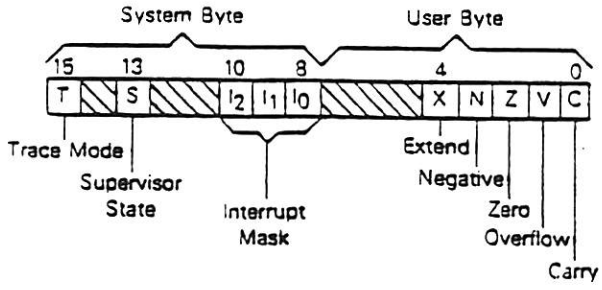
There are two stack pointers, A7 & A7'(A7 prime). A7 is used as the USER stack pointer, and A7' is used as the SUPERVISOR stack pointer. Both SP's are set up to stack from the top down and to access LIFO.

STATUS REGISTER

In addition to the seventeen 32 bit registers, there is a 16 bit register called the STATUS REGISTER. This register is set up so that the lower byte indicates the user status, and the upper byte indicates the system status.

The table below shows the bit assignment for the status register.

STATUS REGISTER



The user byte is used to check condition during program operation under the USER mode.

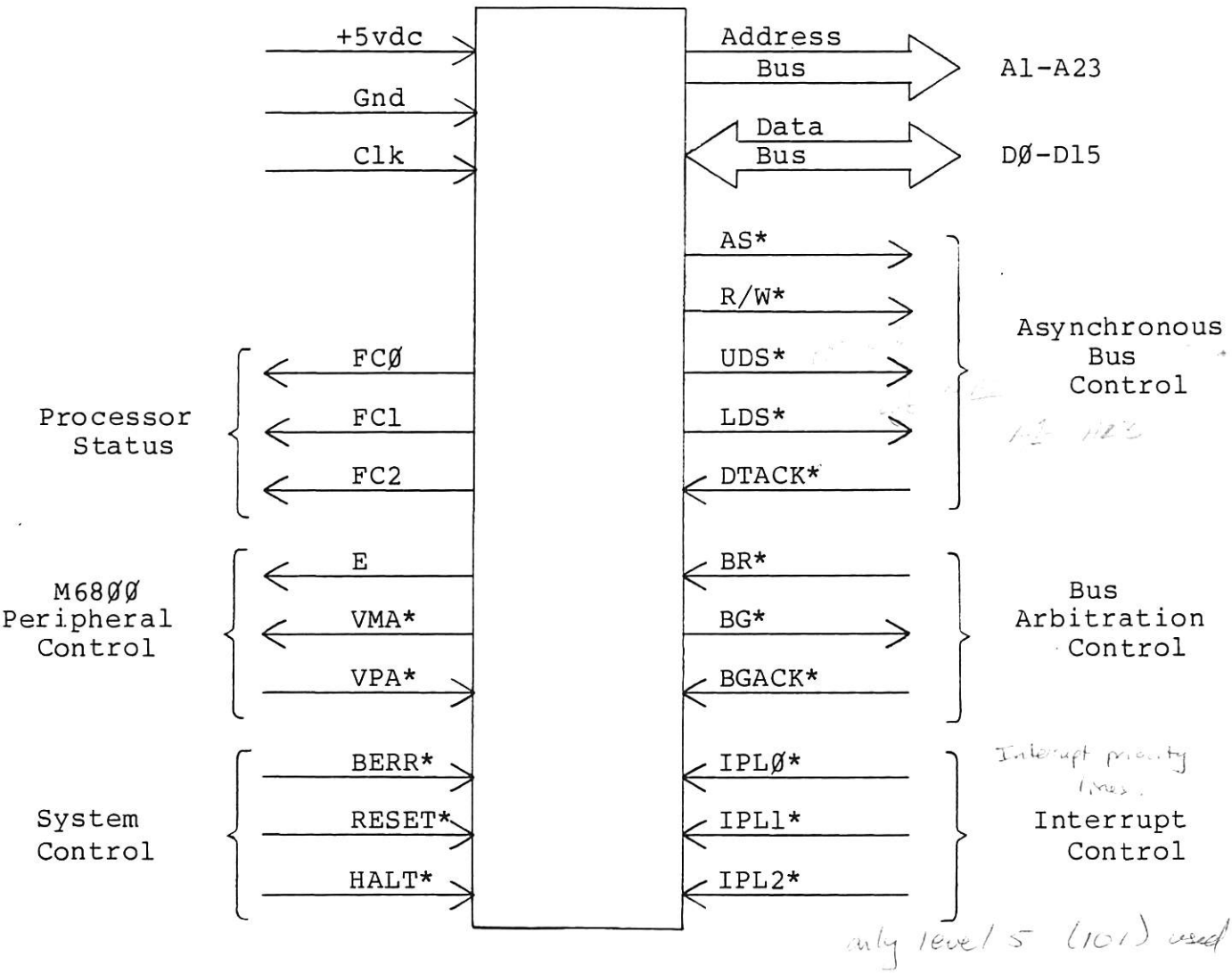
The system byte is used to as follows:

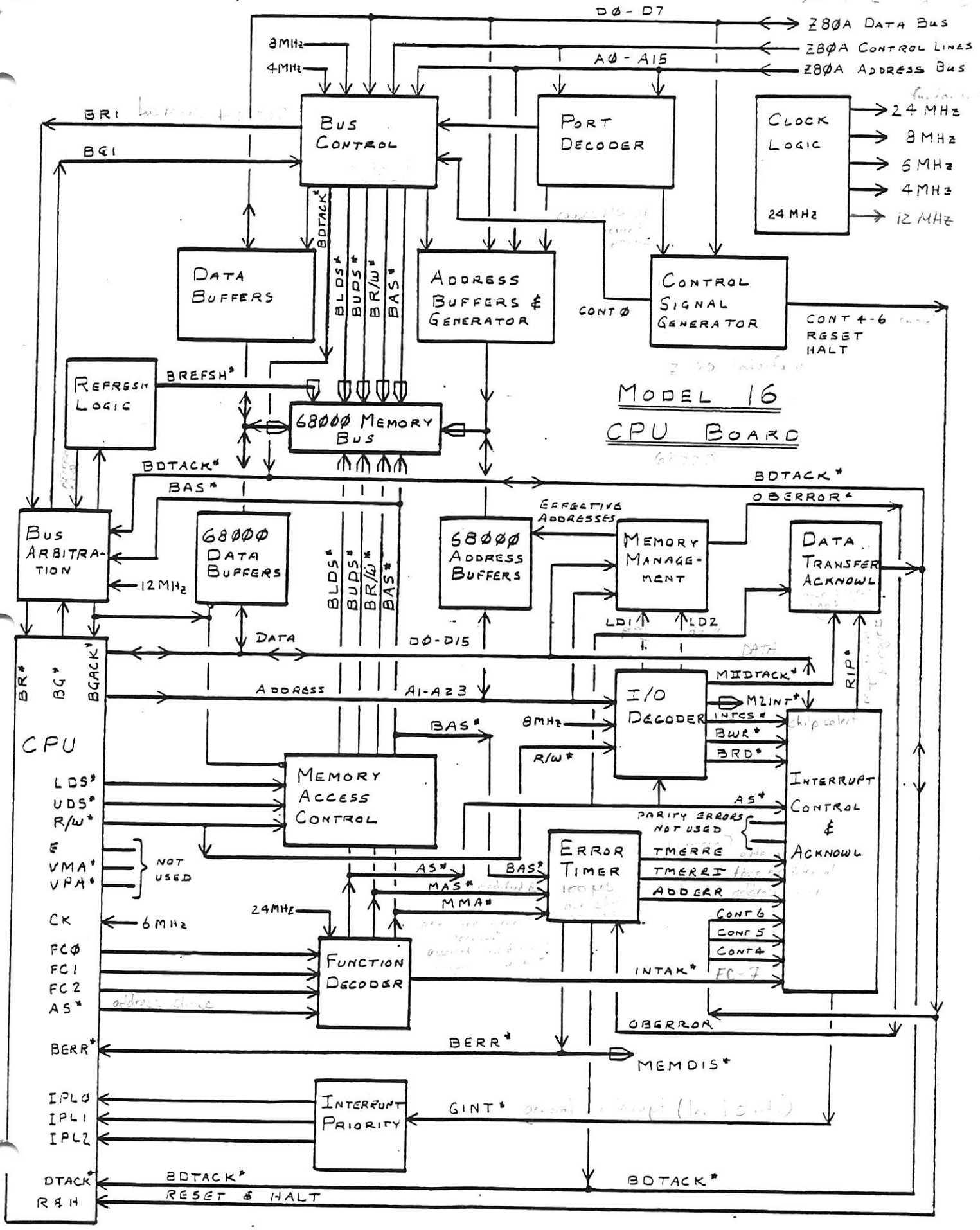
1. The interrupt mask is set to allow only interrupts of that level or higher, as determined by the 3 bit combination at bit 8, 9, & 10, to be accepted by the 68000. A level 7 interrupt (highest priority) is not capable of being masked out.

2. If bit 13 is set the processor is in the SUPERVISOR mode. If it is reset it is in the USER mode.

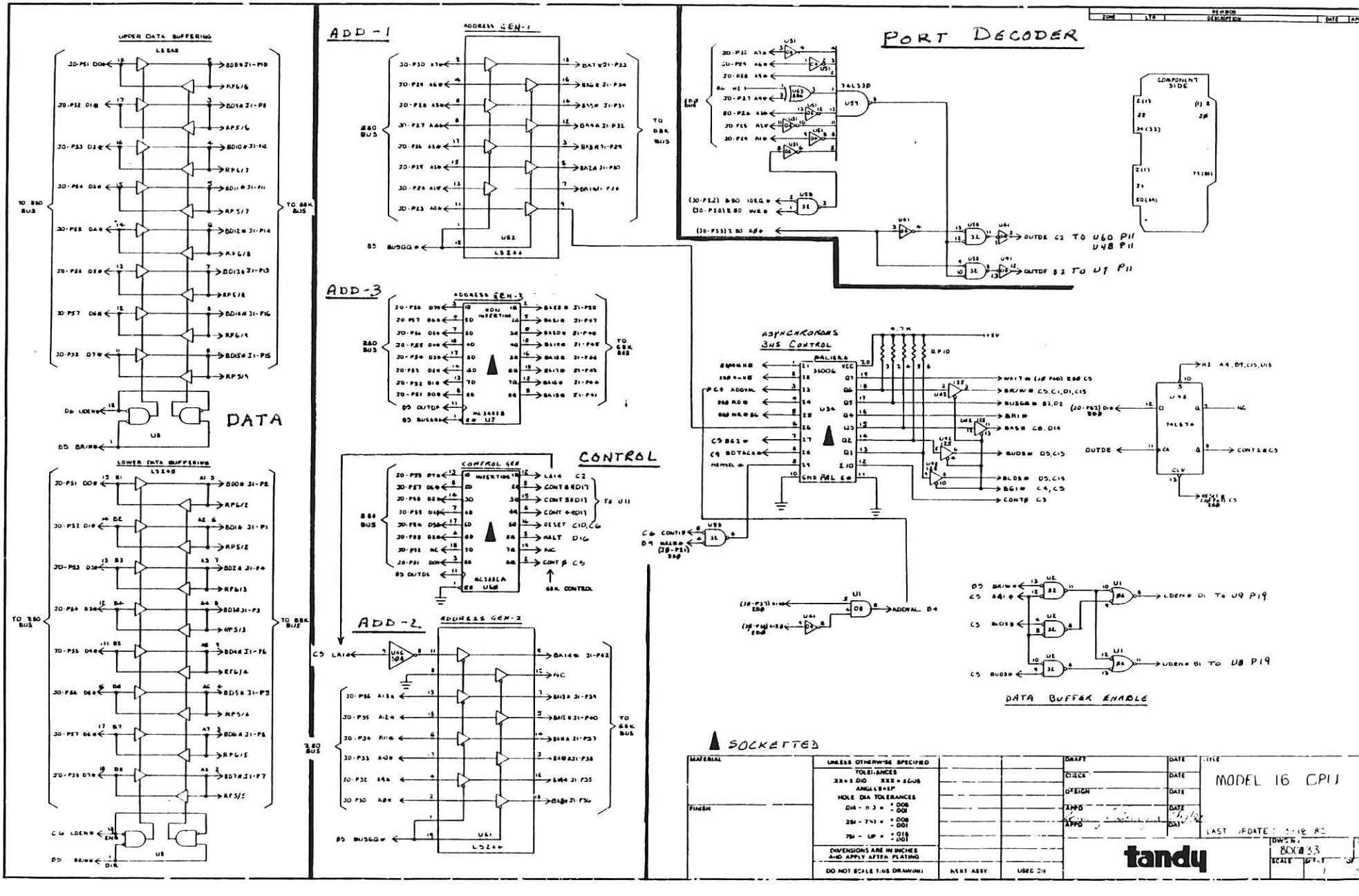
3. If bit 15 is set the processor is in the TRACE, or single step mode.

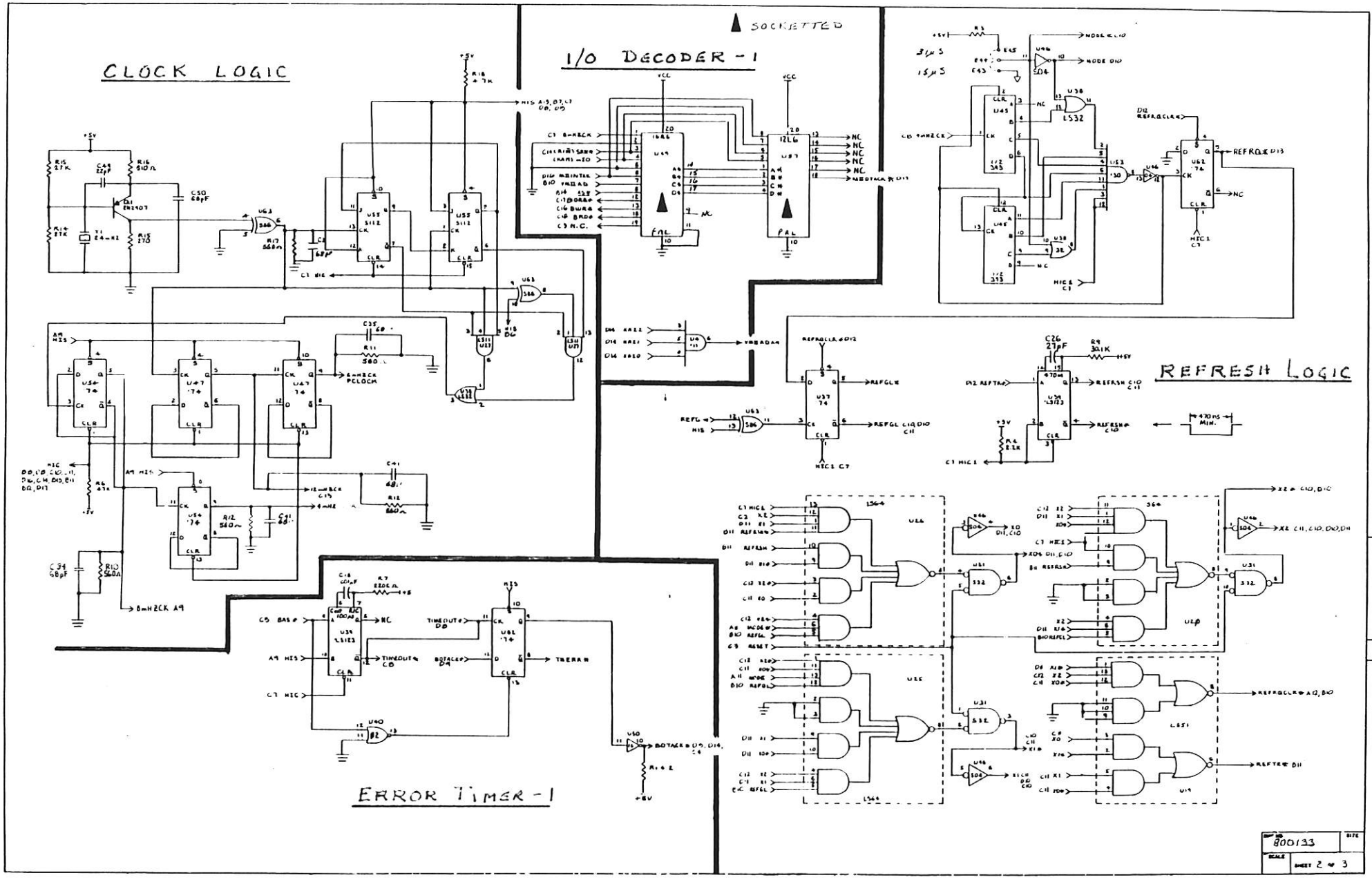
FUNCTIONAL PINOUT DIAGRAM
THE 68ØØØ CPU

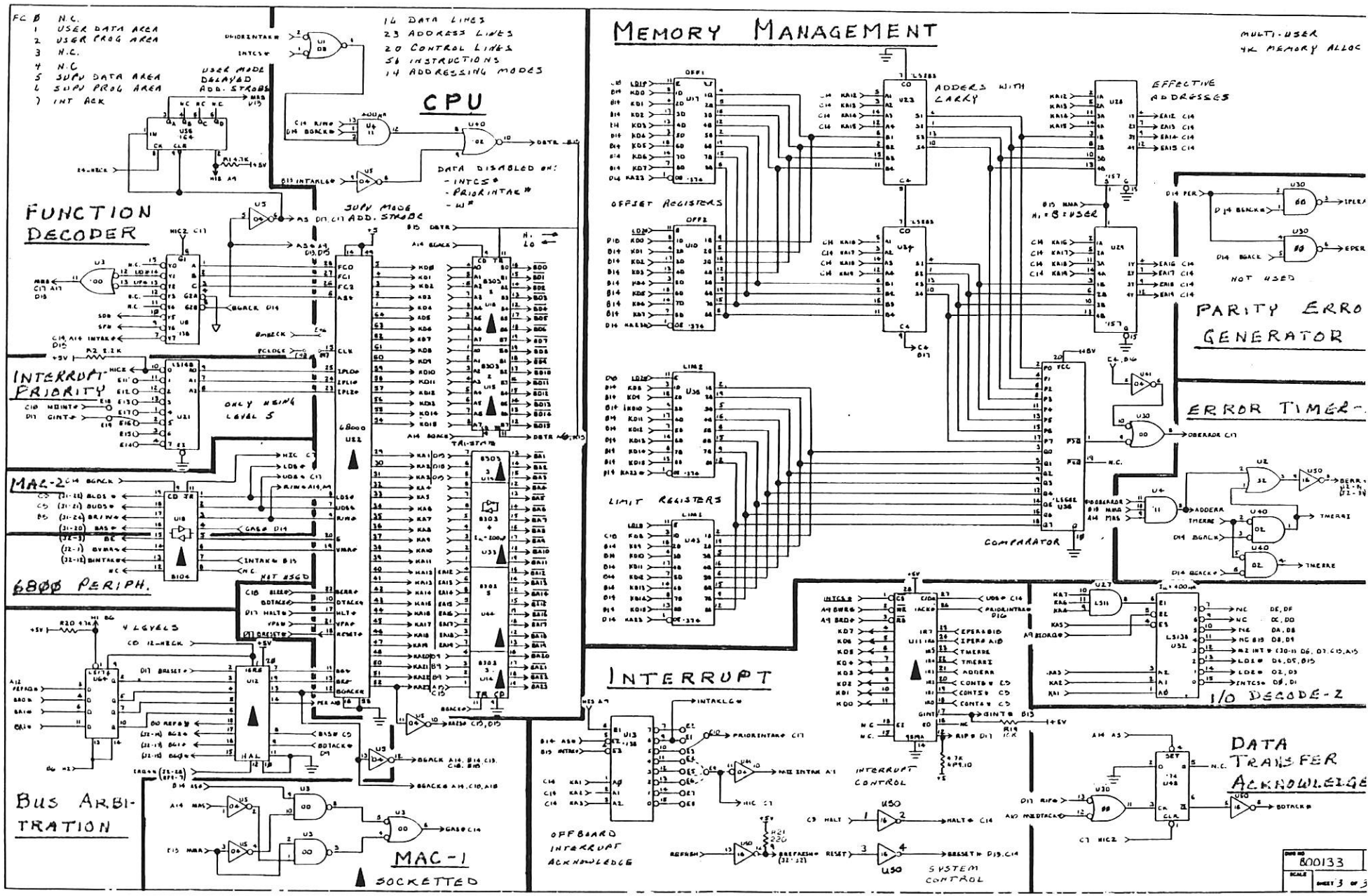



D0 - D7
Z80A Data Bus
Z80A Control Lines
A0 - A15
Z80A Address Bus
8MHz
4MHz
BRI
BGI
Bus Control
Port Decoder
Clock Logic
24 MHz
24 MHz
8 MHz
6 MHz
4 MHz
12 MHz
BDTACK*
BLDS*
BUDS*
BR/W*
BAS*
Data Buffers
Address Buffers & Generator
CONT0
Control Signal Generator
CONT 4-6
RESET
HALT
Refresh Logic
BREFSH*
68000 Memory Bus
MODEL 16
CPU BOARD
BDTACK*
BAS*
BDTACK*
OBERROR*
Bus Arbitration
12 MHz
68000 Data Buffers
68000 Address Buffers
Effective Addresses
Memory Management
Data Transfer Acknowl
LD1
LD2
DATA
D0-D15
MIIDTACK*
RIP*
ADDRESS
A1-A23
I/O Decoder
M2INT*
INTCS*
BWR*
BRD*
8MHz
R/W*
BAS*
CPU
BR*
BG*
BGACK*
LDS*
UDS*
R/W*
E
VMA*
VPA*
NOT USED
CK
6 MHz
FC0
FC1
FC2
AS*
BERR*
IPL0
IPL1
IPL2
DTACK*
R & H
Memory Access Control
Interrupt Control & Acknowl
AS*
PARITY ERRORS NOT USED
Error Timer
TMERRE
TMERRI
ADDERR
AS*
BAS*
MAS*
MMA*
24MHz
CONT6
CONT5
CONT4
FC-7
Function Decoder
INTAK*
OBGERROR
BERR*
MEMDIS*
Interrupt Priority
GINT*
BDTACK*
BDTACK*
RESET & HALT

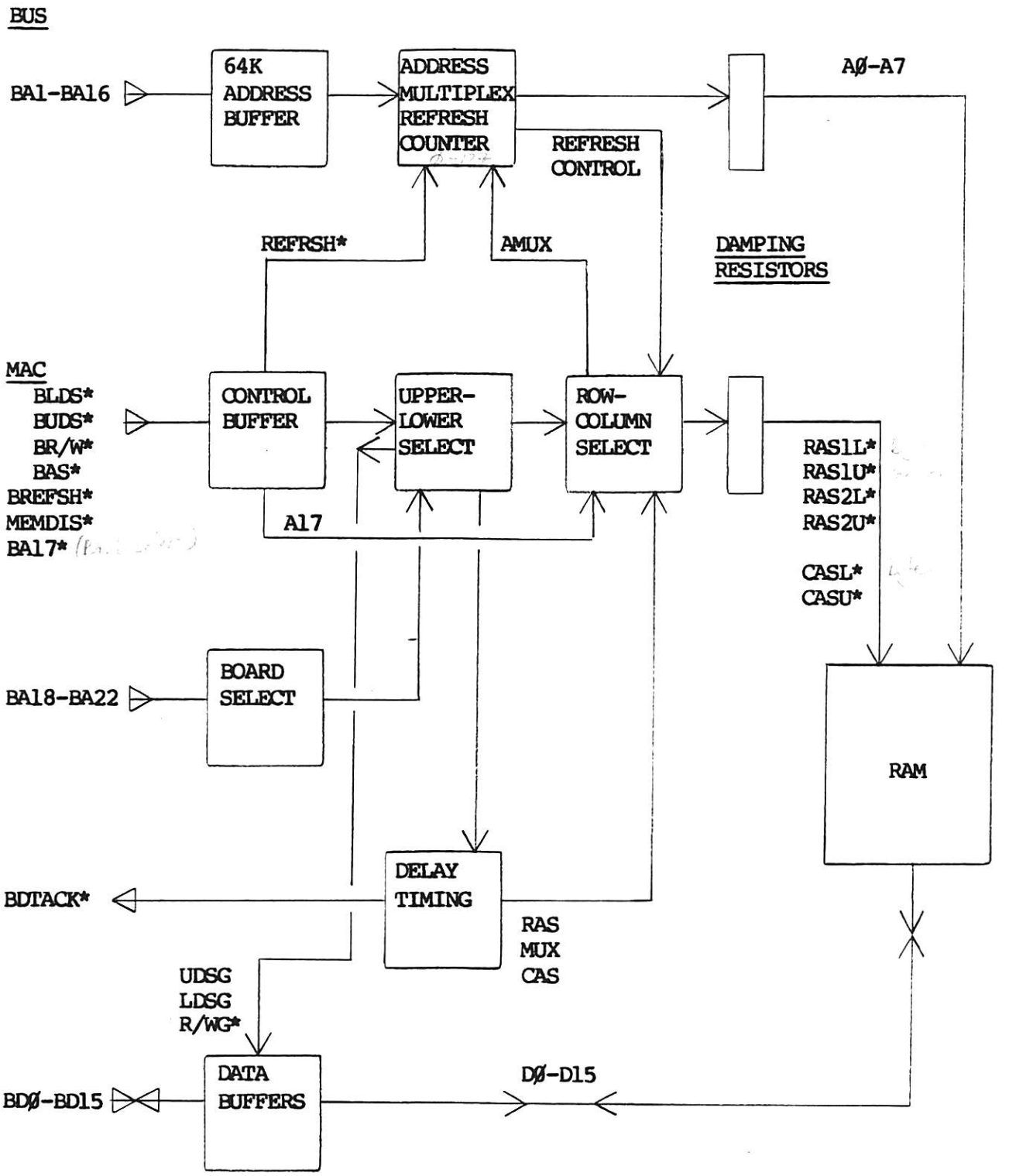
Z80A - 68000 INTERFACE

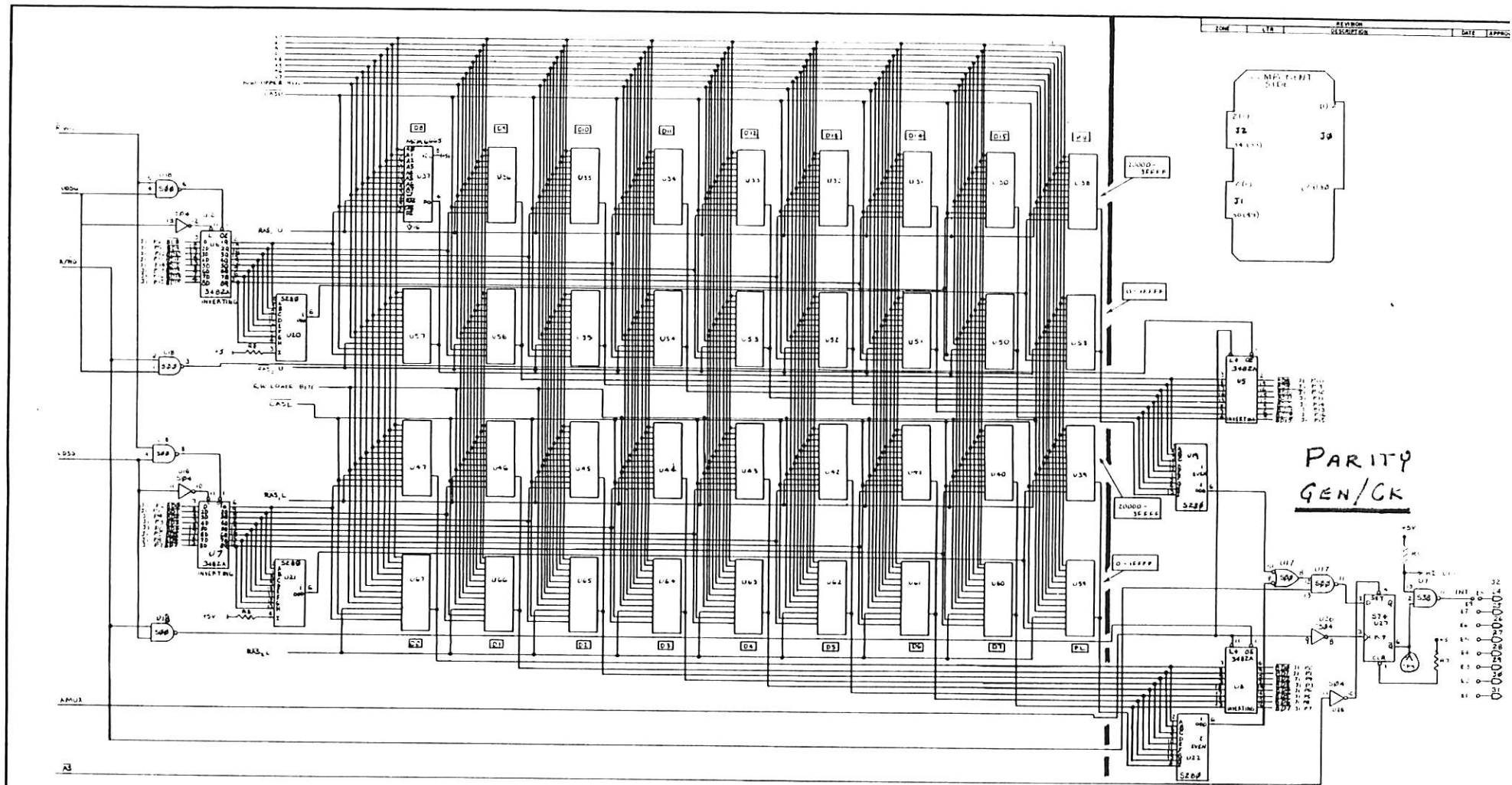



CLOCK LOGIC
I/O DECODER - 1
SOCKETTED
REFRESH LOGIC
ERROR TIMER - 1
800133
SHEET 2 OF 3

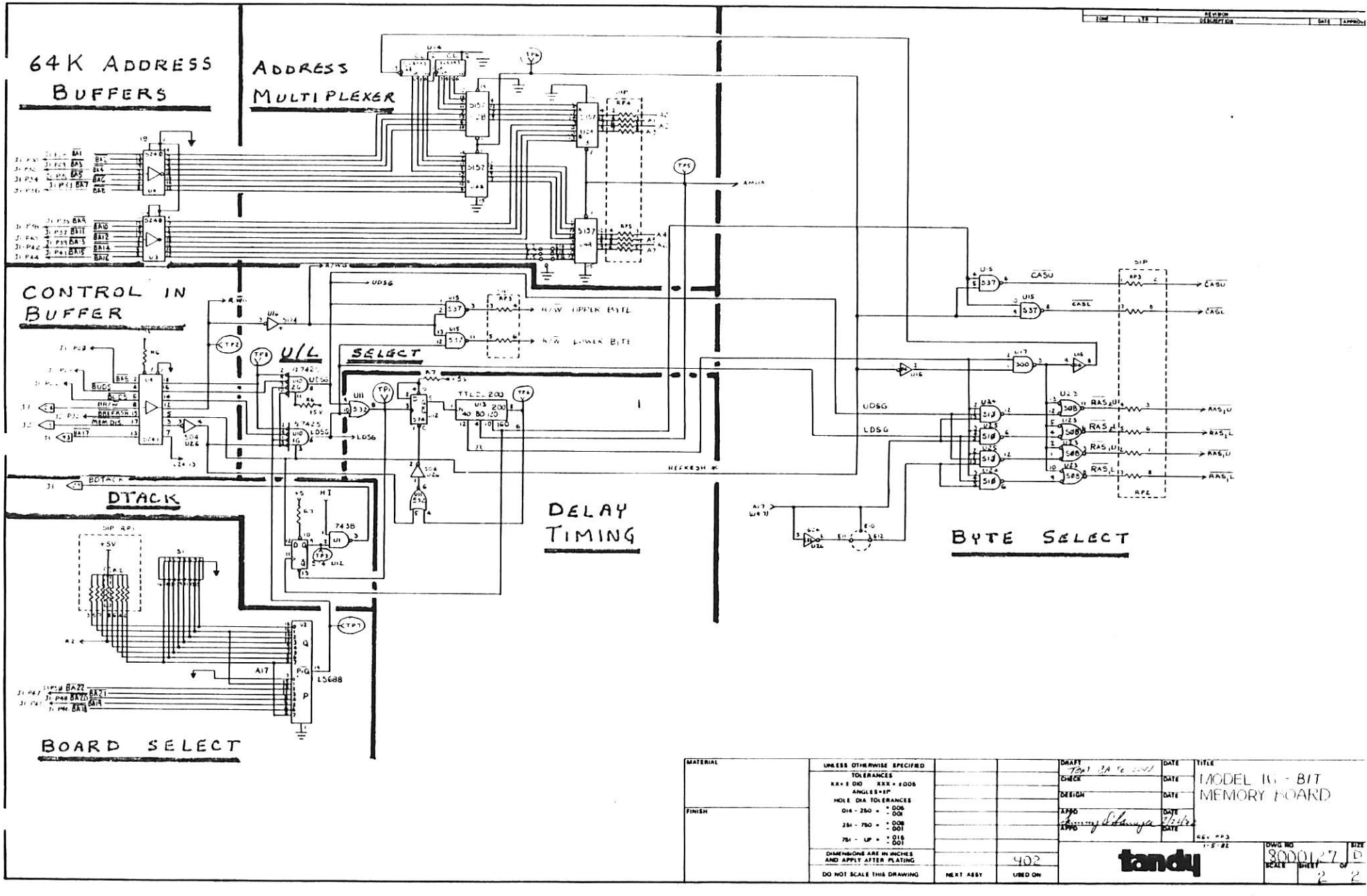

FC 0 N.C.
1 USER DATA AREA
2 USER PROG AREA
3 N.C.
4 N.C.
5 SUPV DATA AREA
6 SUPV PROG AREA
7 INT ACK
16 DATA LINES
23 ADDRESS LINES
20 CONTROL LINES
56 INSTRUCTIONS
14 ADDRESSING MODES
CPU
FUNCTION DECODER
INTERRUPT PRIORITY
ONLY USING LEVEL 5
MAC-2
68000 PERIPH.
BUS ARBITRATION
4 LEVELS
MAC-1
SOCKETTED
MEMORY MANAGEMENT
MULTI-USER
4K MEMORY ALLOC
OFFSET REGISTERS
ADDERS WITH CARRY
EFFECTIVE ADDRESSES
LIMIT REGISTERS
COMPARATOR
PARITY ERRO
GENERATOR
NOT USED
ERROR TIMER-
I/O DECODE-2
INTERRUPT
INTERRUPT CONTROL
OFFBOARD INTERRUPT ACKNOWLEDGE
SYSTEM CONTROL
DATA TRANSFER ACKNOWLEDGE
800133

MODEL 16
128K-256K MEMORY BOARD





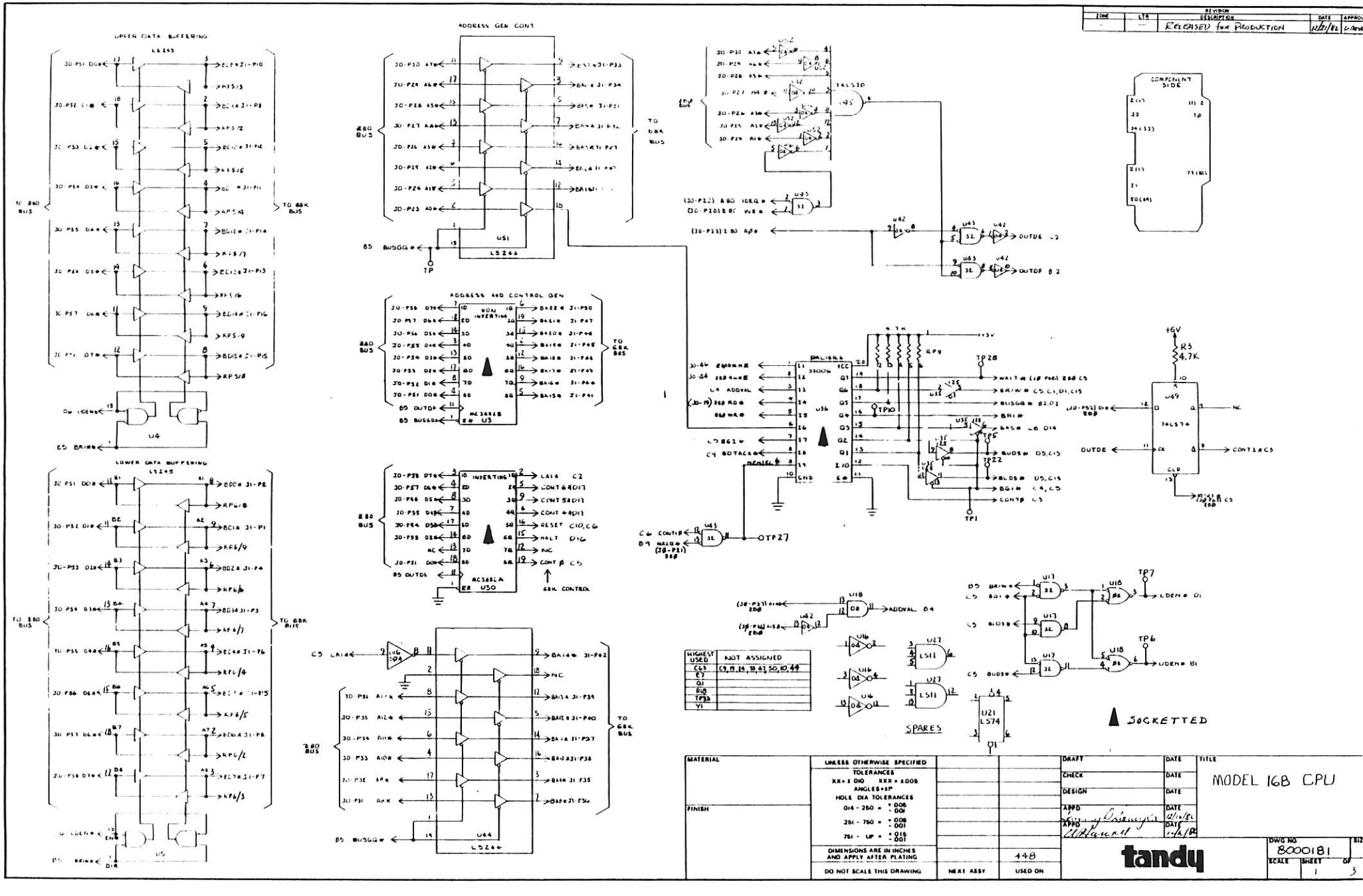
MATERIAL	UNLESS OTHERWISE SPECIFIED TOLERANCES XX = ± 010 XXX = ± 005 ANGLES = 1° HOLE DIA TOLERANCES .014 - .250 = +.005 -.001 .251 - .750 = +.008 -.001 .751 - UP = +.015 -.001 DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING DO NOT SCALE THIS DRAWING	NEXT ASSY	USED ON	DRAFT / DATE CHECK / DATE DESIGN / DATE APPD / DATE APPD / DATE	TITLE MODEL 16 BIT MEMORY BRD REV PPS 1-5-82
FINISH				tandy	DWG NO 81-10127 SIZE D SCALE SHEET 1 OF 2

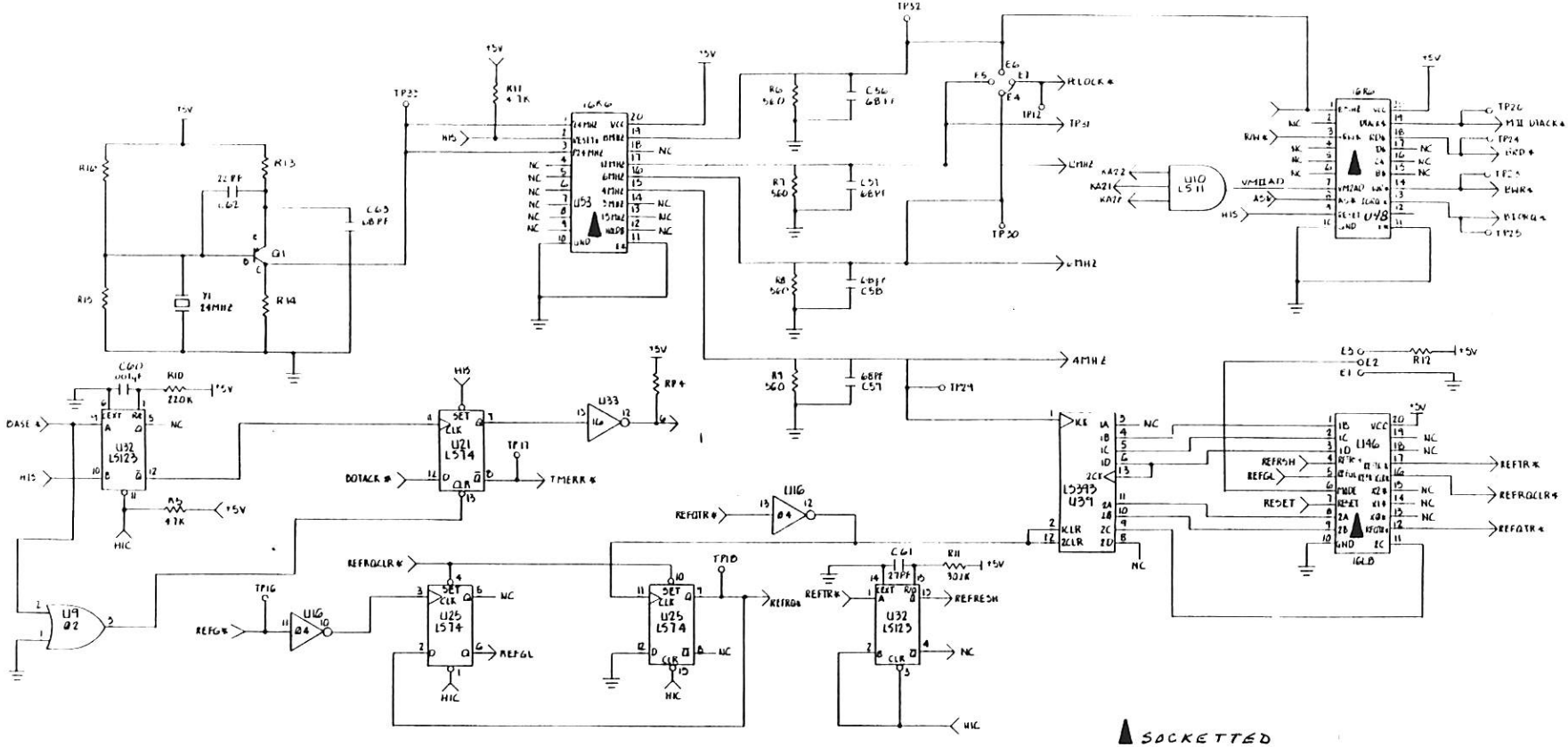


MATERIAL	UNLESS OTHERWISE SPECIFIED TOLERANCES XX ± .010 XXX ± .005 ANGLES ± 1/2° HOLE DIA TOLERANCES .014 - .250 + .005 -.001; .251 - .750 + .009 -.001; .751 - UP + .016 -.001 DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING DO NOT SCALE THIS DRAWING	NEXT ASSY	USED ON 402	DRAFT Tom DA Te 5-1-82	DATE	TITLE MODEL 16 - BIT MEMORY BOARD
FINISH				CHECK	DATE	
				DESIGN	DATE	
				APPD	DATE 5/14/82	
				APPD	DATE	
				66K PP3 1-5-82		tandy
						DWG NO 8000127 SIZE D
						SCALE SHEET 2 OF 2

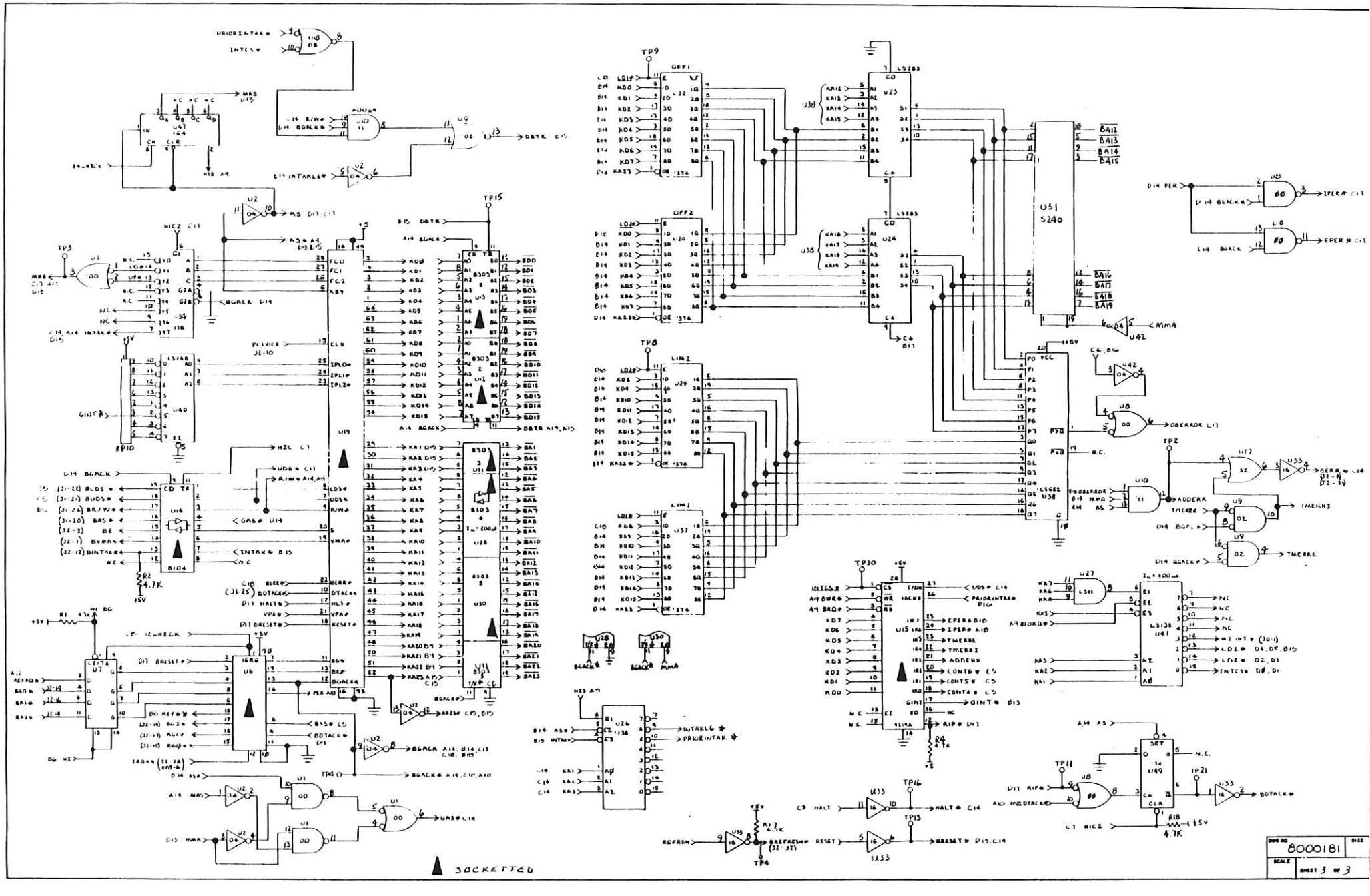
Z-80 Module

ZONE	LTR	REVISION DESCRIPTION	DATE	APPROV
-	-	RELEASED for PRODUCTION	12/1/82	[illegible]





DWG NO	REV
8000181	-
SCALE 1/1	SHEET 2 OF 3


PRIORINTAK#
INTCS#
MRS
U47
74
CK
CLR
MRS A9
B14 BGACK#
U10
U9
DBTR
B15 INTAK6#
U2
MS DIR CT1
TP15
B15 DBTR
A14 BGACK
TP3
U1
U34
138
MRS CT1 A11
C14, A14 INTAK#
U5V
U40
LS148
IPL0#
IPL1#
IPL2#
GINT#
RP10
5
CLOCK 22-10
CLK
HIC2 CT1
HIC CT
U19
D14 BGACK
UDS# CT1
R/W# A14, A15
CD TR
U16
8304
LDS#
UDS#
R/W#
GAS# D14
VMA#
INTAK# B15
R2
4.7K
+5V
BERR#
DTACK#
HALT#
VPA#
RESET#
C10 (31-25)
D11
BGACK#
U28
U30
U11
B303
B303 S
B303 Z
U29
U37
LIN2
LIN1
LDLB
LDUB
KD8
KD9
KD10
KD11
KD12
KD13
KD14
KD15
KA1 D15
KA2 D15
KA3 D15
KA4
KA5
KA6
KA7
KA8
KA9
KA10
KA11
KA12
KA13
KA14
KA15
KA16
KA17
KA18
KA19
KA20 D9
KA21 B9
KA22 A9
C15
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BA10
BA11
BA12
BA13
BA14
BA15
BA16
BA17
BA18
BA19
BA20
BA21
BA22
BA23
U7
74
16RG
U6
R1
4.7K
BG HI
BG
BUS REQ#
BUS#
BDTACK#
BGACK#
BGACK A14, B14, C15
C10, B10
A14 AS#
A14 MAS
D15 MMA
U1
00
GAS# C14
TP4
TP9
OFF1
OFF2
U22
U20
LD1#
LD2#
U23
U24
C0
C4
LS283
U38
BA12
BA13
BA14
BA15
BA16
BA17
BA18
BA19
U51
S240
MMA
U42
D14 PER
D14 BGACK#
U5
U6
IPER# C13
EPER# C13
D14 BGACK
TP8
U29
U37
LIN2
LIN1
+5V
P5V
N.C.
OBERADR C11
C4, D10
TP2
U17
32
U33
BERR# C14
D2-11
D3-19
TMERR#
U9
02
TMERR
ADDERR
D14 BGACK#
TP20
U15
6116
INTCS#
A9 BWR#
A9 BRD#
KD7
KD6
KD5
KD4
KD3
KD2
KD1
KD0
EPER# B10
IPER# A10
TMERR
TMERR#
ADDERR
CONT3# C5
CONT2# C5
CONTA# C5
GINT#
INTCS# C14
PRIORINTAK# D10
RIP# D11
R9
4.7K
U27
L511
L5138
U41
KA7
KA6
KA5
KA4
KA3
KA2
KA1
A9 BIORQ#
M2 INT# (30:1)
LDS# D4, D5, B15
LDS# D2, D3
INTCS# D8, D1
A14 AS
SET
U49
TP11
TP21
D11 RIP#
A10 MRDTACK#
C7 HIC2
R18
4.7K
U33
BDTACK#
TP16
TP13
TP4
C9 HALT
HALT# C14
REFRESH
R7
4.7K
BREFRESH#
(32:32)
RESET
BRESET# D15, C14
U33
LS33
SOCKETTED
DWG NO
8000181
SIZE
SCALE
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