VCC AND GND LIST

DEVICE	REF DESIGNATOR	+5V	GND	+12V	-12V
7416	U138,140	14	7		
7438	U19	14	7		
74F00	U112	14	7		
74F02	U109	14	7		
74F04	U89,97	14	7		
74F08	U106,123	14	7		
74F32	U25,101,107,114,125,136	14	7		
74F64	U96	14	7		
74F138	U99	16	8		
74F161	U61,74	16	8		
74F244	U28,35	20	10		
74F245	U34,52,53,56,65,66,88	20	10		
74F258	U45,46	16	8		
74F373	U116,127	20	10		
74LS00	U4,91	14	7		
74LS02	U133	14	7		
74LS04	U23,128,122,137,141	14	7		
74LS08	U20,86	14	7		
74LS14	U139	14	7		
74LS30	U119	14	7		
74LS32	U2,21,85,136	14	7		
74LS38	U38,87	14	7		
74LS74	U3,84,88*,96,92,118,138	14	7		
74LS123	U24,132	16	8		
74LS125A	U22,27,83	14	7		
74LS138	U67,71	16	8		
74LS139	U98	16	8		
74LS161A	U73,106,104	16	8		
74LS193	U94	16	8		
74LS195	U131	16	8		
74LS241	U135	20	10		
74LS244	U10,11,17,33,58,78,81,105, 117,128,32	20	10		
74LS245	U8,44,50,51,54	20	10		
74LS273	U49,78,79	20	10		
74LS323	U9	20	10		
74LS373	U63,64,77	20	10		
74LS374	U36,57	20	10		
74LS393	U29	14	7		
74S00	U1	14	7		
74S74	U69	14	7		
74S112	U113,124	16	8		
74S139	U26	16	8		
74S157	U18	16	8		
74S260	U93	14	7		
74S280	U115,126	14	7		
75477	U129	8	4		
80186	U76	9,43	26,60		
8251A	U41	26	4		
8253-5	U40	24	12		
8255A-5	U75	26	7		
8259A-2	U42,43	28	14		
8272	U121	40	20		
82S153	U62,68	20	10		
CRT9007	U16	21	40		
CRT9021	U14	8	20		
CRT9212	U15,55	8	23		
FDC9216	U134	8	4		
MC1488	U5		7	14	1
MC1489	U6,7	14	7		
NE564	U72**		8		
PAL10L8	U82	20	10		
PAL16L8A	U95,102,103*	20	10		
PAL20L8	U103*	24	12		
PD4016	U12,13	24	12		
SPARE	U31	20	10		
SPARE	U142	20	10		
SPARE	U143	20	10		
74LS145	U30	16	8		
74LS174	U60	16	8		
74LS378	U37	16	8		
74S04	U39	14	7		

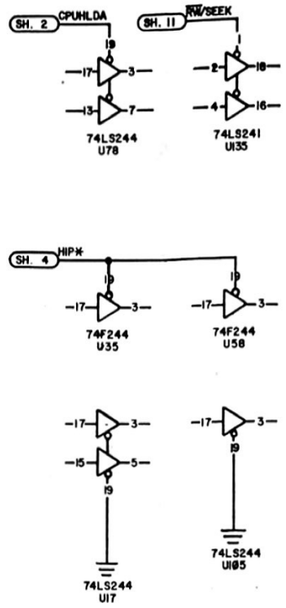
* UI03 MAY USE A PAL16L8A OR PAL20L8 DEPENDING UPON PROGRAM REQUIREMENTS (SEE SHEET 3).

** U72 AND U88 ARE LOCATED IN AN ISOLATED Vcc AND GND AREA (SEE SHEET 7).

SPARE GATES LIST

DEVICE	REF. DESG.	GATES NOT USED
7416	U138	1-6
7438	U19	1-6
74F00	U108	1-3,11-13
74F02	U109	4-6
74F08	U106	4-6,8-13
74F32	U25	11-13
74F32	U107	1-3,8-10
74LS00	U4	11-13
74LS00	U91	4-6
74LS02	U133	8-10
74LS04	U128	3-6,12,13
74LS04	U141	3-6,10,11
74LS08	U20	1-3
74LS14	U139	1,2
74LS32	U2	1-3
74LS32	U85	4-6,8-10
74LS32	U136	1-6
74LS38	U38	1-6,8-10
74LS38	U87	8-10
74LS74	U118	8-13
74LS123	U132	1-4,13-15
74LS125A	U22	11-13
74LS125A	U83	1-6
74S00	U1	1-3
74S157	U18	9-14
74S260	U93	1-3,5,12,13
MC1489	U7	11-13

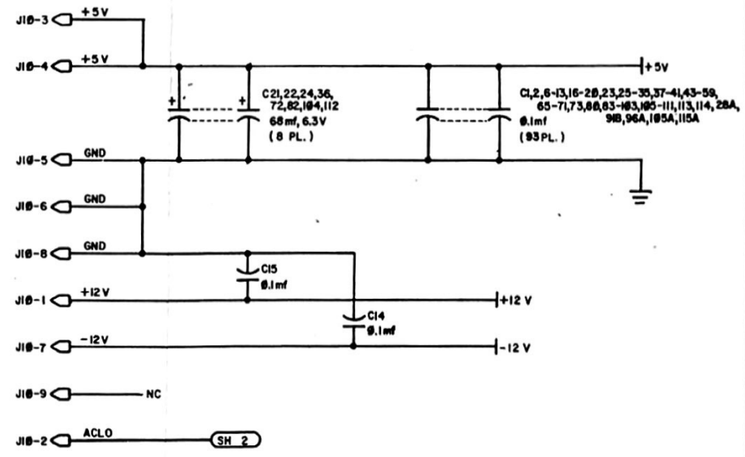
SPARE BUFFERS



REFERENCE DESIGNATORS

LAST USED	NOT USED
UI43	UIII
YI	
RP5	
CRI	
Q2	
JII	
R59	R17
CII6	
LI	

LTR	REVISION DESCRIPTION		DATE	APPROVED
PP1			5/25/83	
PP2			6/27/83	
REV. A	RELEASED FOR PRODUCTION		11/11/83	G/1048
A-1	CORRECT U63,64,77(SH2) & UII4(SH9)	IE	2/28/84	MB



DC POWER SCHEMATIC

03	REV. A	RELEASED FOR PRODUCTION	11/11/83
03	PP3.5	LIMITED PRODUCTION RELEASE	9/1/83
03	PP3	PRE-PROTOTYPE	8/22/83
02	PP2	PRE-PROTOTYPE	6/27/83
01	PP1	PRE-PROTOTYPE	
HEX CODE	PCB REV LTR.	DESCRIPTION	DATE

CONFIGURATION STATUS ⚠

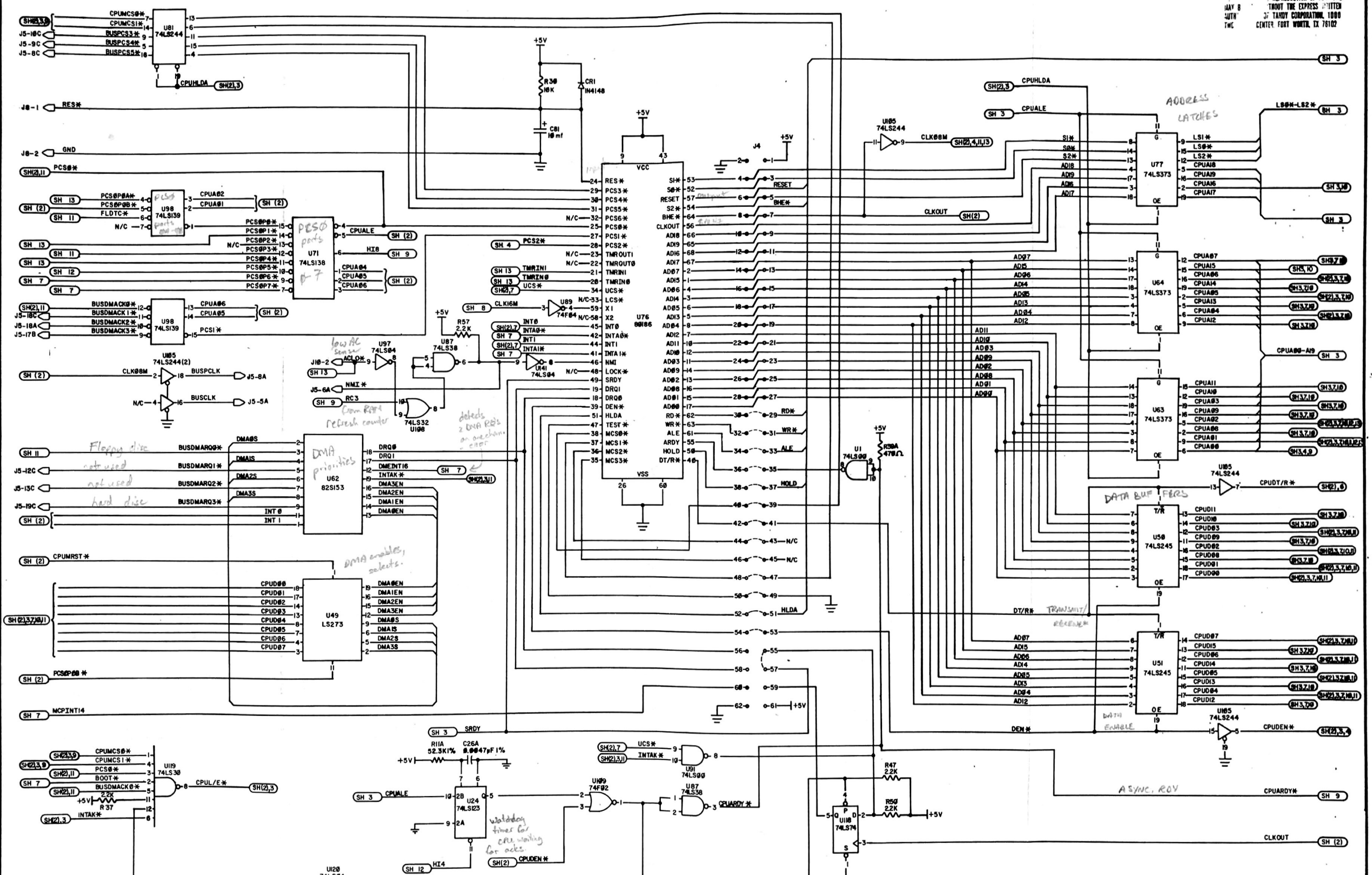
⚠ CONFIGURATION STATUS PORT: THE MAIN LOGIC BOARD HAS AN 8-BIT PORT THAT INDICATES THE CONFIGURATION STATUS OF THE PRINTED CIRCUIT BOARD WITH RESPECT TO SOFTWARE. THE INPUT STRAPPING TO THIS REGISTER (UI0) MUST BE INCREMENTED BY ONE FOR EACH REVISION OF THE PC BOARD THAT DIRECTLY AFFECTS PROGRAMMING. THE HEX CODE FOR EACH PC BOARD CONFIGURATION CHANGE APPEARS IN THE CONFIGURATION STATUS SCHEDULE AT RIGHT (SEE SHEET 12).

RELEASED FOR PRODUCTION

DRAFT D.CRONCH, K.NEWTON	DATE 7/83	TITLE SCHEMATIC- MAIN LOGIC BOARD PROJECT J-507
CHECK	DATE 9/11/83	
DESIGN	DATE	
APPD	DATE 9/11/83	
APPD	DATE 11-11-83	

tandy

DWG NO.	SIZE
8000203	D
SCALE N/A	SHEET 1 OF 13



CPU	DWG NO 8000203
SIZE	D
SCALE	NONE
SHEET	2 OF 13

PROPRIETARY INFORMATION

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CPU bus control lines

Bus addresses

address lines bidirectional due to DMA in CPU.

Data buffers (bidirectional)

video holds, priority levels

refresh inhibit (used to speed vid access)

decoder status lines

20 pin chip in 24 pin socket

28.0 or 22.4 MHz

BUS INTERFACE	DWG NO 8000203 REV
	SCALE N/A SHEET 3 OF 13

RP1 2.2K
RP3 2.2K
+5V
+5V
2 4 7 6 3 5 8
2 5 4 3 8 7 6

14 address lines → access 16 k of mem by itself
-all transfers are 16 bit, ∴ A0 always low. → so use A1-A11 as A0-A13

cursor position only from VPAC
Blanking at top screen, reboot

U34 74F245
U35 74F244
U82 PAL16L8
U16 CRT 9007 VPAC
U56 74F245
U55 CRT 9212
U15 CRT 9212
U69 74S74
U141 74LS04
U90 74LS74
U90 74LS74
U60 74LS174

BUSA01 BUSA02 BUSA03 BUSA04 BUSA05 BUSA06 BUSA07
BUSA08 BUSA09 BUSA10 BUSA11 BUSA12 BUSA13 BUSA14
BUSA01 -BUSA14
HIP
HIP*
NC
DIR
EN
OE
CS
RST
INT
ACK
DMAR
GND
SLG
SLD
CURSOR
CBLANK
VS
HS
VIDCCLK
WBEN
DRB
VLT
CSYNC
VA00 VA01 VA02 VA03 VA04 VA05 VA06 VA07 VA08 VA09 VA10 VA11 VA12 VA13
VIDDLYCS*
CPUMRST*
VIDINT11
LHLDA
DMAR
VD0 VD1 VD2 VD3 VD4 VD5 VD6 VD7
BUSD00 BUSD01 BUSD02 BUSD03 BUSD04 BUSD05 BUSD06 BUSD07
DRB*
DI0 DI1 DI2 DI3 DI4 DI5 DI6 DI7
WEN1
TOG
CLRCNT
REN
WEN2
Vcc
DO0 DO1 DO2 DO3 DO4 DO5 DO6 DO7
ROF
WOF
WCLK
RCLK
VIDLA0 VIDLA1 VIDLA2 VIDLA3 VIDLA4 VIDLA5 VIDLA6 VIDLA7
VIDLA0-VIDLA7
char. code
BUSD08 BUSD09 BUSD10 BUSD11 BUSD12 BUSD13 BUSD14 BUSD15
BLC BKC CHABL MS0 MS1 BLINK INT REVID
CBLANK
attributes.
BLANK
BLINK
INT
REVID
VIDLDSH
HI12
DBLC
DBKC
DBLANK
ADDLWE*
VIDCS*
VIDCS
ADDLWE*
R15 2.2K
R35 2.2K
CLR
CPUBHE*
CPUA00
CPUDEN*
PCS2*
CPUIOW*
CLK08M
LHLDA
VIDHLDA*
VIDRD*
CPUMRST*
VIDHOLD
BUSD00-BUSD15

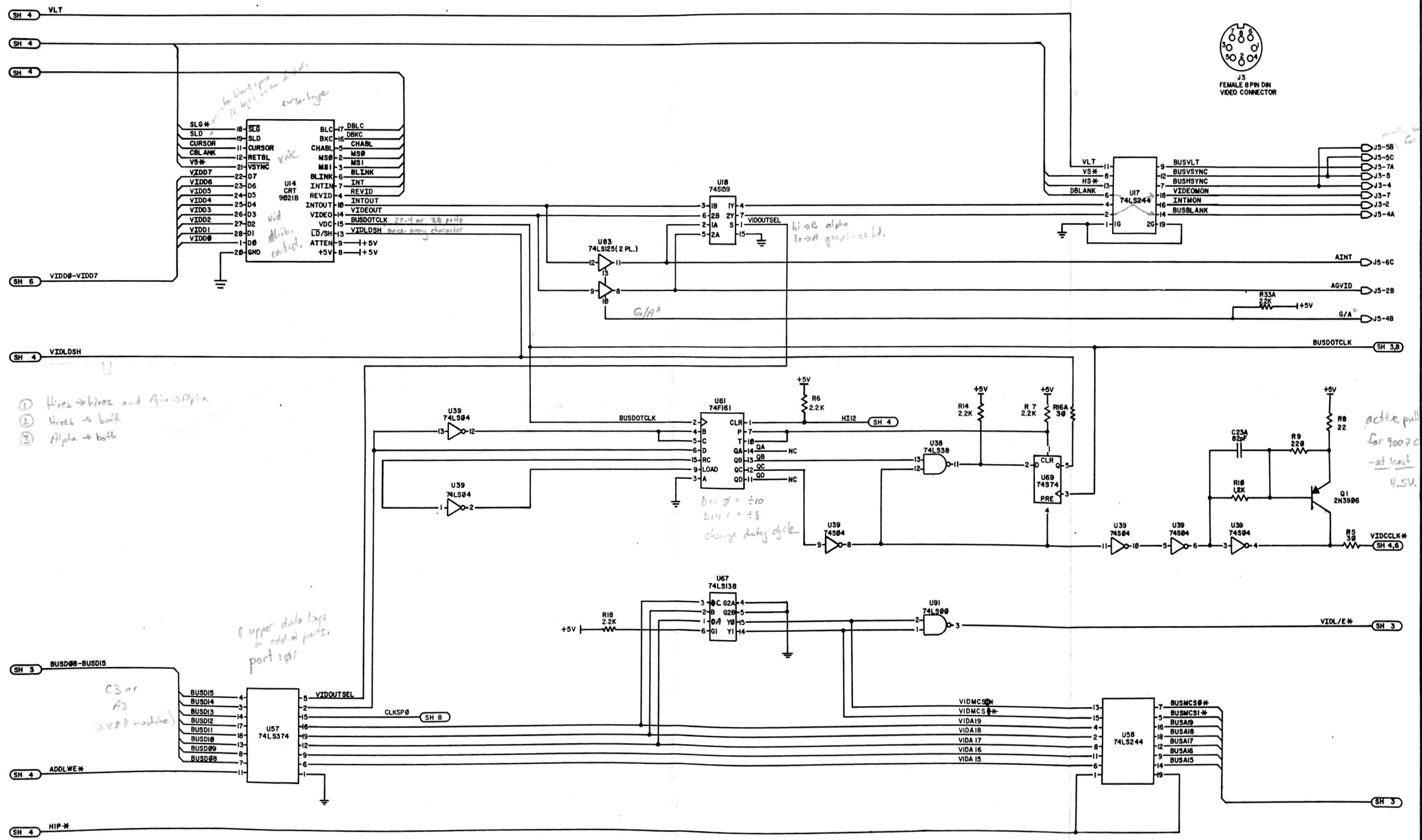
SH 5,8
SH(4)
SH 6
SH 5
SH 3
SH 7
SH 2
SH 6
SH(3)(4)

NO RD/WR Line on this. Add. line 5 rd/wr.

double row buffers → rows of video info

one char. delay

CRT CONTROLLER / MAIN VIDEO LOGIC	DWG NO. 8000203	REV
	SCALE N/A	SHEET 4 OF 13



PROPRIETARY INF...

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MAIN VIDEO LOGIC	DWG NO. 8000203	REV.
	SCALE N/A	SHEET 5 OF 13

SIPO

SH 5

U37 74LS378 — SLG* (1), VIDCCLK* (9), SLD (3), (4), (2); outputs (12), (13), (10), (11), (7), (6), (5)

VID5Q
VID4Q
VID3Q
VID2Q

U32 74LS244 — inputs (6), (2), (8), (4); outputs (14), (18), (12), (16); ~G 26; (1)

CGRA00
CGRA01
CGRA02
CGRA03

CGRCS

U33 74LS244 — BUSA05 (6), BUSA06 (2), BUSA07 (11), BUSA08 (17), BUSA09 (4), BUSA10 (15), BUSA11 (13), BUSA12 (8); (1), (19)

CGRA04
CGRA05
CGRA06
CGRA07
CGRA08
CGRA09
CGRA10
CGRA11

CGRCS*

U32 74LS244 — BUSA01 (13), BUSA02 (17), BUSA03 (11), BUSA04 (15); (19)

CGRA00
CGRA01
CGRA02
CGRA03

SHT. 3 BUSA01-BUSA12

U13 μPD4016 — 2K x 8 RAM static — char gen — even scan lines — ~CS 18

(8), (7), (6), (5), (4), (3), (2), (1), (23), (22), (19)

VIDD0
VIDD1
VIDD2
VIDD3
VIDD4
VIDD5
VIDD6
VIDD7

OELOW*
WELOW*

VIDD0-VIDD7 SHT. 5

VIDCCLK* SHT. 5

U59 DELAY LINE — (1), (14) +5V, (7), (6) — DDU4-5125

VIDCCLK *

CGRA00

CPUDT/R* SHT. 2

U68 82S153 PAL — (19), (18), (17), (16), (7), (5), (11)

VIDCCLK*
DLYCCLK*
VIDHOLD SHT. 4
LHLDA
BUSA00 SHT. 4
BUSBHE*
BUSMW*
BUSMR*
SHT. 3

VIDRD* SHT. 4

BUSD00-BUSD07 SHT. 3

CGRCS* SH 7

odd scan lines

U12 μPD4016 — 2K x 8 RAM static — char gen — ~CS 18

(9), (10), (11), (13), (14), (15), (16), (17), (20), (21)

VIDD0
VIDD1
VIDD2
VIDD3
VIDD4
VIDD5
VIDD6
VIDD7

OEHIGH*
WEHIGH*

U54 74LS245 — (1); (17), (18), (16), (12), (15), (14), (11), (13); (19), (9)

BUSD00
BUSD01
BUSD02
BUSD03
BUSD04
BUSD05
BUSD06
BUSD07

U36 74LS374 — VIDLA0 (17), VIDLA1 (8), VIDLA2 (7), VIDLA3 (4), VIDLA4 (3), VIDLA5 (13), VIDLA6 (14), VIDLA7 (18); ~OE (1); (11)

CGRA04
CGRA05
CGRA06
CGRA07
CGRA08
CGRA09
CGRA10
CGRA11

SHT. 4 VIDLA0-VIDLA7

VIDCCLK*

U23 74LS04 — CGRCS (2) (1) CGRCS*

lo-CPU has control of u.v RAM's U12, U13

CGRCS* ⇒ 0 = 18K. } reads
1 = 9007 }

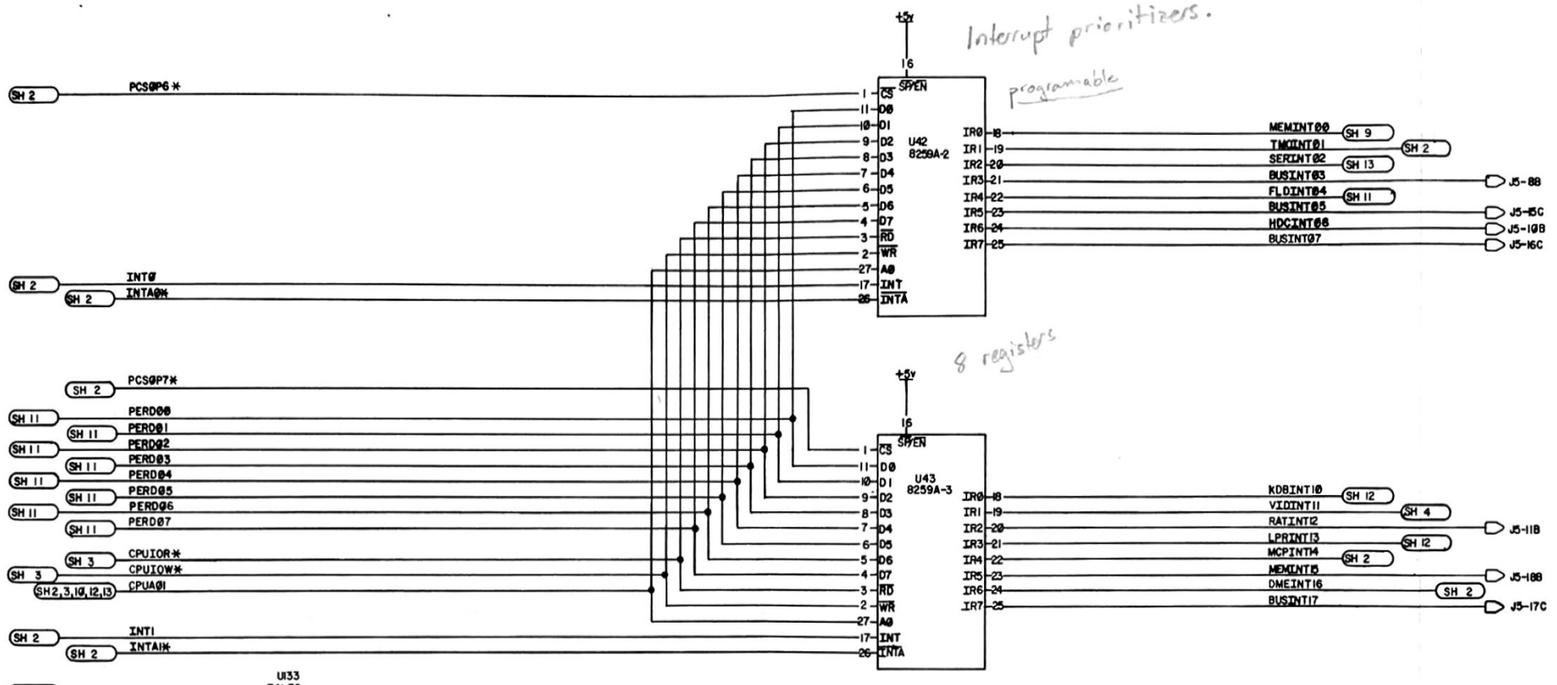
PROPRIETARY

THE INFORMATION CONTAINED HEREIN [illegible]

CHARACTER GENERATOR I/F LOGIC	DWG NO 8000203	REV
	SCALE NONE	SHEET 6 OF 13

Interupt prioritizers.

programable



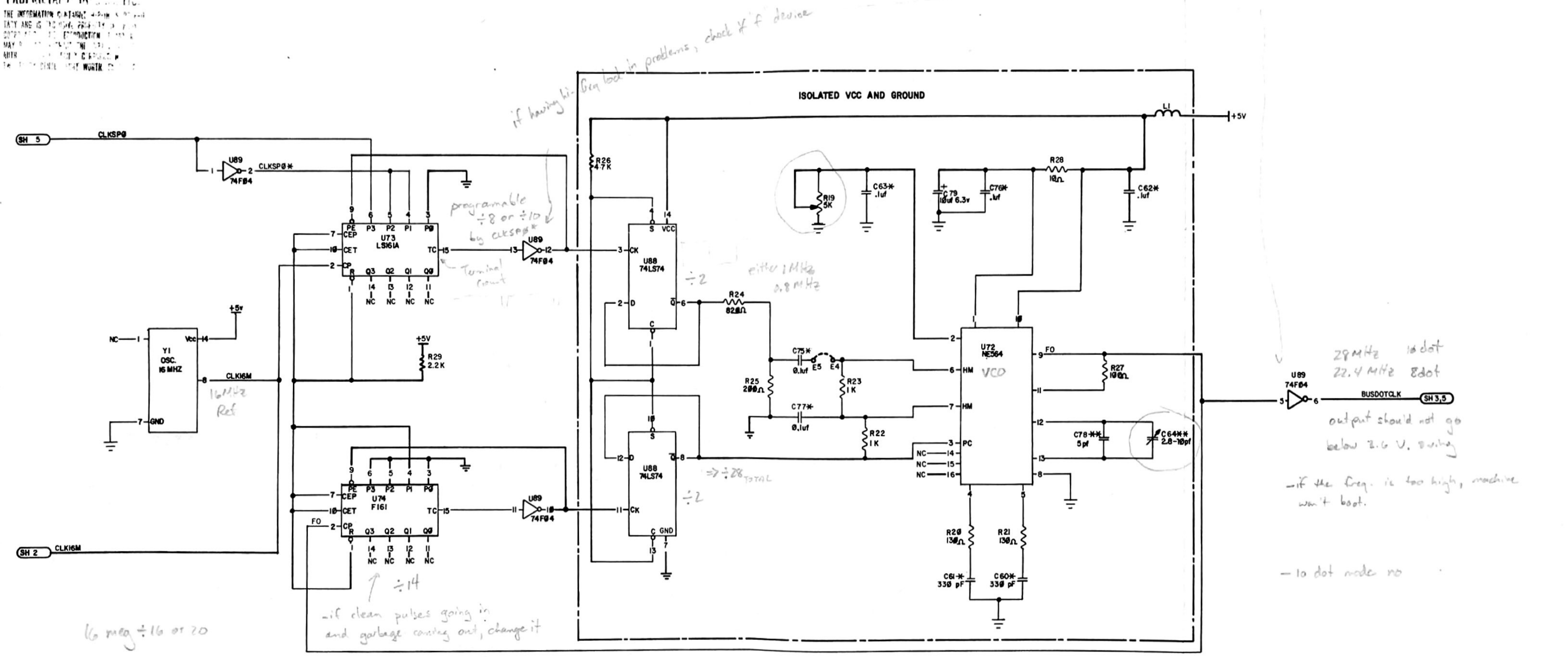
peripherals

all data (peripheral) transfers are 8 bits
all port transfers are 8 bits.

char graphics ram CS*

16 bit wide boot sequence

INTERRUPT CONTROLLER/BOOT ROM	DWG NO D- 8000203	REV
	SCALE N/A	SHEET 7 OF 13



* – MUST BE THOMPSON CSF CAPACITORS

** – MUST BE NPO TEMPATURE COEFFICIENT CAPACITORS

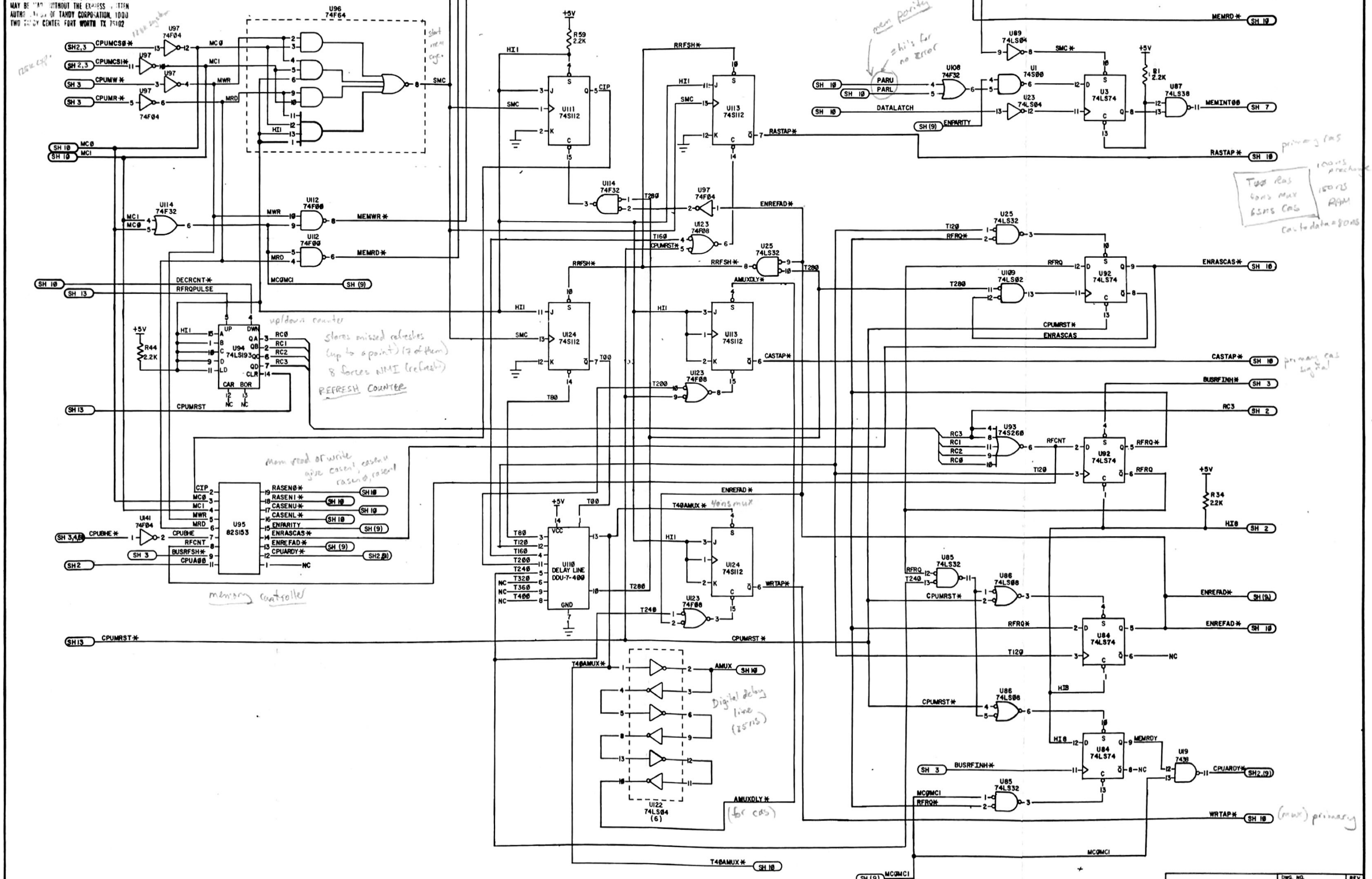
$FO = \frac{CLK16M \times 28}{16 \text{ or } 18 \text{ or } 20}$

	Fin (MHZ)	
	15.990921	16.000
Fout (MHZ)	27.984111	28.00
	22.387289	22.400

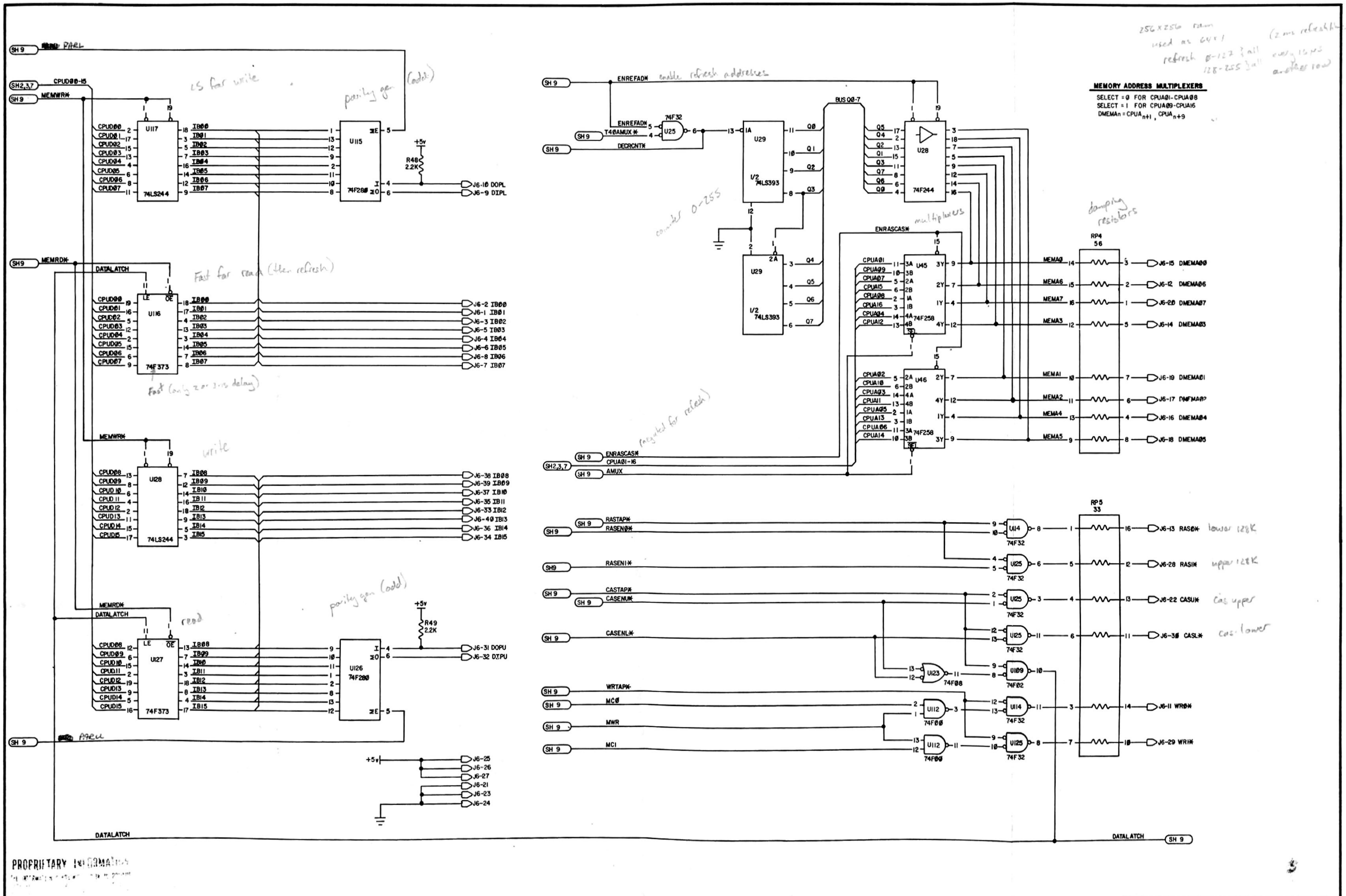
CLOCK/PHASE LOCK LOOP

DWG NO	SIZE
8000203	D

SCALE	SHEET	OF
N.A	8	13



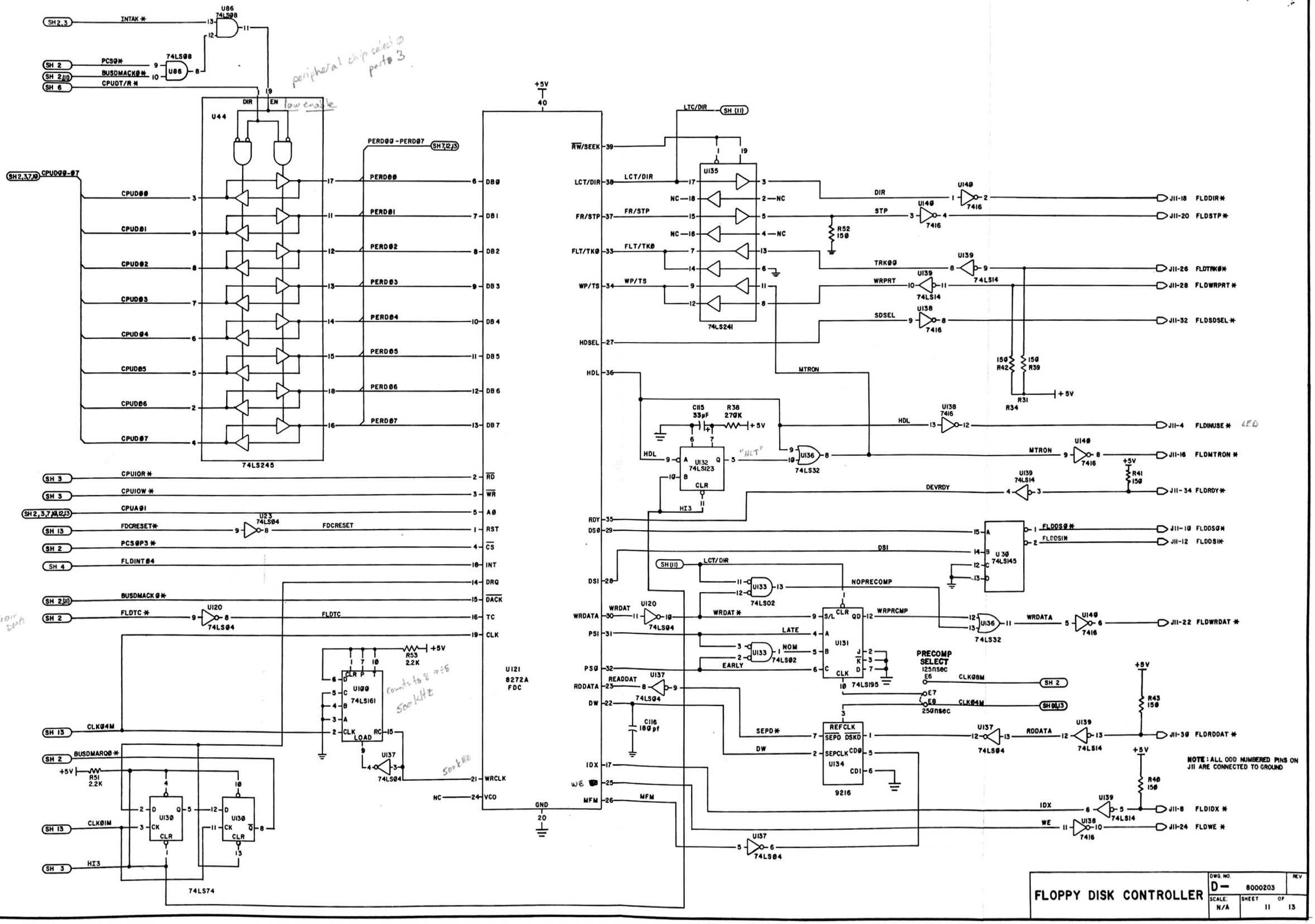
MEMORY TIMING	DWG. NO. 8000203	REV
	SCALE N/A	SHEET 9 OF 13



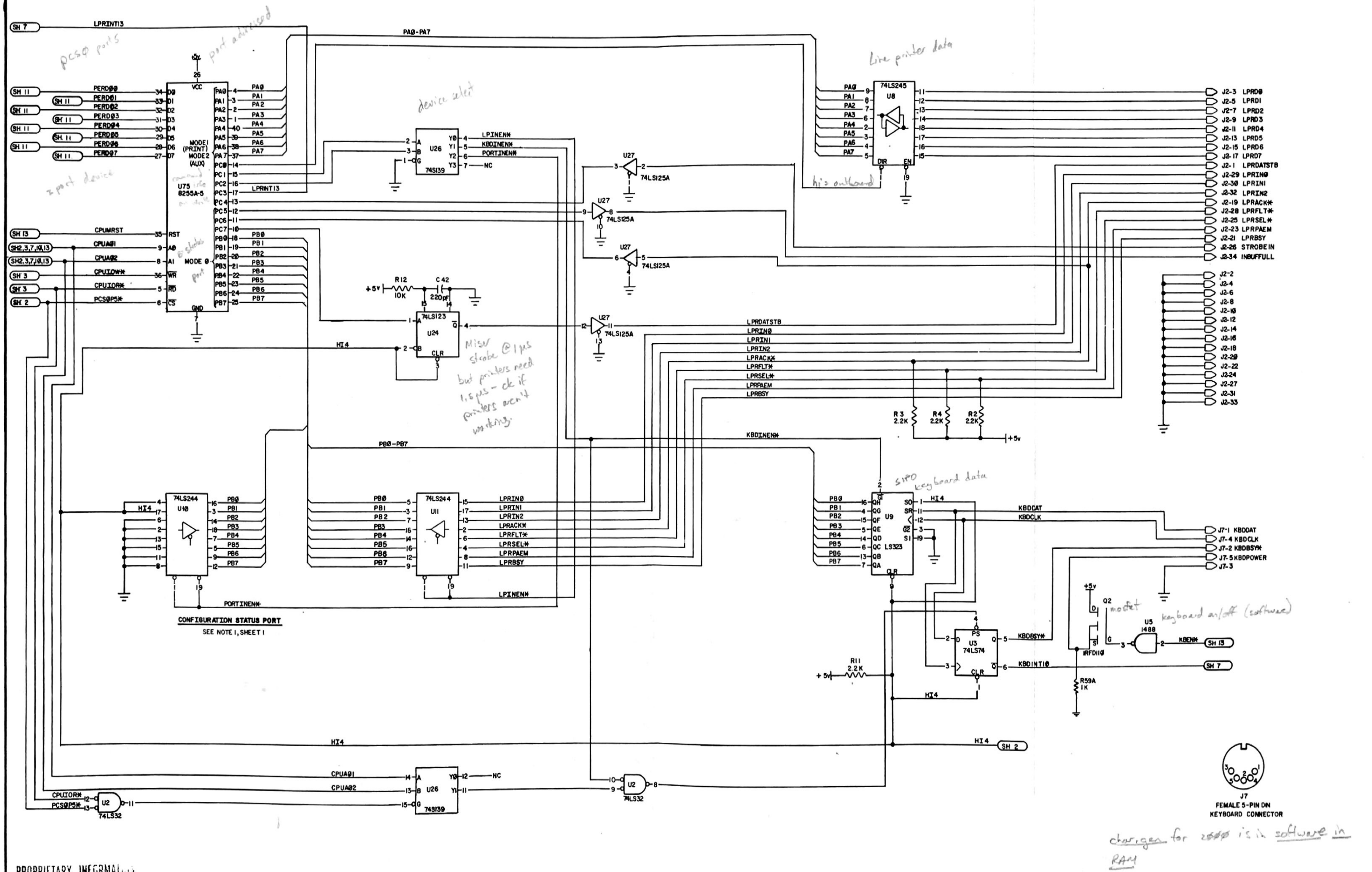
MEMORY CONTROL

DWG NO 8000203 SIZE D

SCALE N/A SHEET 10 OF 13



FLOPPY DISK CONTROLLER	DWG. NO. D- 8000203	REV
	SCALE: N/A	SHEET 11 OF 13



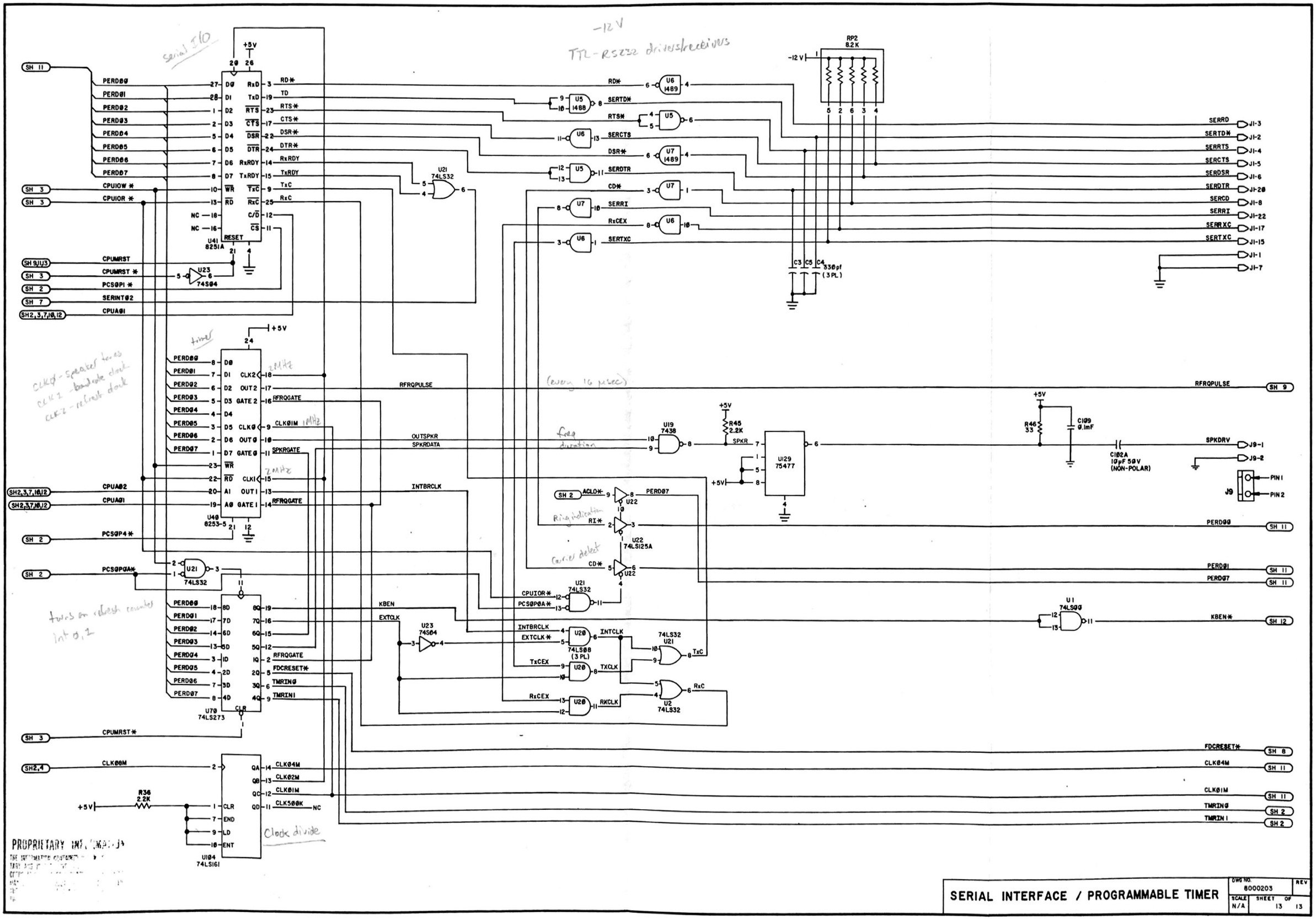
PROPRIETARY INFORMATION

THE INFORMATION CONTAINED HEREIN IS ... [illegible]

PARALLEL/KEYBOARD INTERFACE

DWG NO.	SIZE
8000203	D
SCALE N/A	SHEET 12 OF 13

K.N.


serial I/O
-12 V
TTL-RS232 drivers/receivers
RP2 8.2K
U41 8251A
U21 74LS32
U23 74S04
U40 8253-5
U79 74LS273
U104 74LS161
U19 7438
U129 75477
U1 74LS00
U20 74LS08 (3 PL)
U22 74LS125A
U2 74LS32
U5 1488
U6 1489
U7 1489
C3 C5 C4 330pf (3 PL)
C109 0.1mF
C102A 10µF 50V (NON-POLAR)
R45 2.2K
R46 33
R36 2.2K
timer
CLK0 - speaker tones
CLK2 - baudrate clock
CLK1 - refresh clock
(every 16 µsec)
freq duration
Ring indication
Carrier detect
turns on refresh counter
Int 0,1
Clock divide
RFRQPULSE
SPKRDATA
OUTSPKR
INTBRCLK
KBEN
EXTCLK
INTCLK
TXCLK
RXCLK
FDCRESET*
CLK04M
CLK02M
CLK01M
CLK500K
TMRIN0
TMRIN1
SERRD
SERTD*
SERRTS
SERCTS
SERDSR
SERDTR
SERCD
SERRI
SERRXC
SERTXC
SPKRDRV
PROPRIETARY INFORMATION
SERIAL INTERFACE / PROGRAMMABLE TIMER
DWG NO. 8000203
REV
SCALE N/A
SHEET OF 13 13