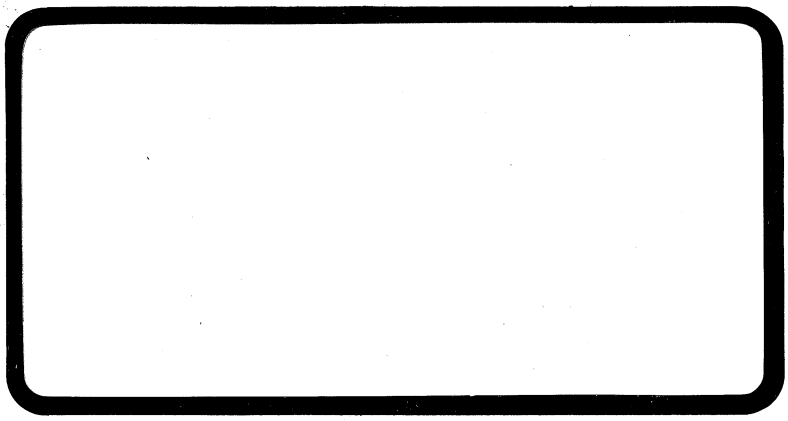

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PM-CTCV11A

PRELIMINARY

The product specifications, contained herein, shall not be construed as being any part of any contract, or contractual obligations, of Plessey, unless Plessey so agrees in writing, and specifically, Plessey makes no warranty as to their accuracy. These performance specifications are subject to change, from time-to-time , by Plessey.

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List of Effective Pages

Title: PM-CTCV11A User Manual

Manual Number: MA-703778

Date	Issue
February 1984	Preliminary Issue (2)

TABLES

PREFACE

This manual describes the PM-CTCV11A coupler manufactured by Plessey Peripheral Systems. This manual provides the basic information needed to install and operate the PM-CTCV11A.

SCOPE

This manual is intended to be used as an installation and reference guide by people knowledgeable of microcomputer systems.

RELATED DOCUMENTS

Plessey Customer Service offers other documents for additional information and guidance in the use of the PM-CTCV11A.

Document Title	Document Number
Maintenance Drawing Package (hard copy)	MD-703778

ORGANIZATION

Section 1 Introduction

This section describes the PM-CTCV11A coupler, including available models and physical and electrical specifications.

Section 2 Installation

This section details the steps to install the PM-CTCV11A coupler including typical cabling diagrams.

Section 3 Initial Start-up and Diagnostics

This section describes the inital start-up as it relates to the PM-CTCV11A.

Section 4 Functional Description

This sections provides the information necessary for a programmer, knowledgeable of QIC-02 interface drives, to write a back-up utility for a PM-CTCV11A subsytem.

1.0 Introduction

The PM-CTCV11A coupler is used with an intelligent tape drive for cost-effective system backup. The PM-CTCV11A couples quarter-inch streaming cartridge tape drives to the LSI-11* bus. The PM-CTCV11A drive interface is compatible with the industry-standard QIC-02 interface and QIC-24 format.

1.1 General Description

The PM-CTCV11A coupler is a single, dual-wide, multilayer board whichmay be installed in any DEC* LSI-11* compatible backplane. The PM-CTCV11A is available in two models as shown in Table 1-1.

Table 1-1. PM-CTCV11A Models

Model	Description
PM-CTCV11A-100 (703778-100)	Board Assembly (703755-100) Diagnostic Kit (PDD101PK1) Drawing Package - Microfiche (MD-703778) User Manual (MA-703778)
PM-CTCV11A-101 (703778-101)	Board Assembly (703755-100) 50-Pin Cable (703606-101) 10-Pin Cable (703788-101 LED Indicator Assembly (703790-100) LED Indicator Cable (703719-100) Diagnostic Kit (PDD101PK1) Drawing Package - Microfiche (MD-703778) User Manual (MA-703778)

The PM-CTCV11A is compatible with 1/4-inch streaming cartridge tape drives with the industry standard QIC-02 (Quarter-Inch Compatiblitly) interface and QIC-24 format. Data and commands are transferred on an eight bit bi-directional bus using asynchronous handshaking techniques.

* DEC and LSI-11 are registered trademarks of Digital Equipment Corporation.

The PM-CTCV11A coupler does not emulate any current DEC device and is not compatible with existing DEC handlers or drivers. However, to ensure compatibility with DEC's addressing parameters, the PM-CTCV11A uses register addresses previously assigned to the DEC TA11 and TC11. In the event one of these DEC devices is in the system, the PM-CTCV11A alternate register set may be used.

Software for system backup is available in Plessey's Cartridge Image Backup (CIB) off-line utility. The CIB utility supports the following devices: RL01/02, RK05, and RK06/07.

1.2 Features

Some of the features of the PM-CTCV11A coupler include:

- QIC-02 interface and QIC-24 format compatibility
- Jumper selectable alternate register set
- Data DMA operation for Read and Write
- Built-in self-test function
- On-board hardware boot capability
- Optional LED assembly indicates "Active" or "Write Protect"

1.3 Specifications

Table 1-2 lists the specifications for the PM-CTCV11A.

Table 1-2. PM-CTCV11A Specifications

Power	+5 V 5%@ 2.4 A 12 W
Temperature	+5 to 45 degrees Celsius
Humidity	0-95% without condensation
Transfer rate	Dependent upon drive
Size	5.2 inches X 8.9 inches (13.2 cm X 22.8 cm)
Environmental:	
Cooling requirement	Airflow of 25 cfm min
	Caution
	Damage may occur to the coupler if run without cooling air for a period in excess of thirty (30) minutes at maximum temperature.
Thermal shock	1 degree Celsius per minute
Altitude	-984 to +9840 ft. -300 to +3000 m
Vibration	5-100 Hz with 0.5 g acceleration
Mechanical shock	10 g for 6 milliseconds
Storage:	
Temperature range	-55 to +85 degrees Celsius
Relative humidity	0-95% without condensation
Thermal shock	10 degrees Celsuis per minute
Altitude	-984 to +52,493 ft. -300 to +16,000 m
Vibration	0-500 Hz with 2 g acceleration
Mechanical shock	20 g for 6 milliseconds

2.0 Installation

Installation for the PM-CTCV11A consists of three (3) basic steps:

1. Ensure the PM-CTCV11A is configured correctly for your system (Section 2.1).

2. Install the PM-CTCV11A board in a LSI-11 compatible backplane (Section 2.2).

3. Connect the cables (Section 2.3).

2.1 PM-CTCV11A Configurations

When you receive the PM-CTCV11A it will be configured to the factory standard. The factory standard configuration is specified in Table 2-1.

Table 2-1. Factory Standard Configuration

Option	Jumper Configuration
Primary Register Set (777500)	W1 IN, W2 OUT
On-board hardware boot enabled	W3 IN

For alternate PM-CTCV11A configurations, see Tables 2-2 and 2-3. Table 2-4 lists the functions of the jumpers on the PM-CTCV11A.

Table 2-2. Secondary Register Set Configuration

Option	Jumper Configuration
Secondary Register Set (777340)	W1 IN, W2 OUT

Note

If either the TC11 or TA11 is present in your system, use an alternate register set for the PM-CTCV11A. If both the TC11 and TA11 are present in the system, the PM-CTCV11A will **not** operate because both the primary and secondary register sets are already being used.

Table 2-3. On-board Hardware Boot Configuration

Option	Jumper Configuration
On-board hardware boot enable	W3 IN
On-board hardware boot disable	W3 OUT

Table 2-4. Jumper Functions

Jumper	Function
W1	Primary Register Set CSR 777500 REG 777502 Vector 000260
W2	Secondary Register Set CSR 777340 REG 777342 Vector 000214
W3	On-board Hardware Boot

Figure 2-1 represents the PM-CTCV11A amd shows approximate locations of the jumpers and cable connectors.

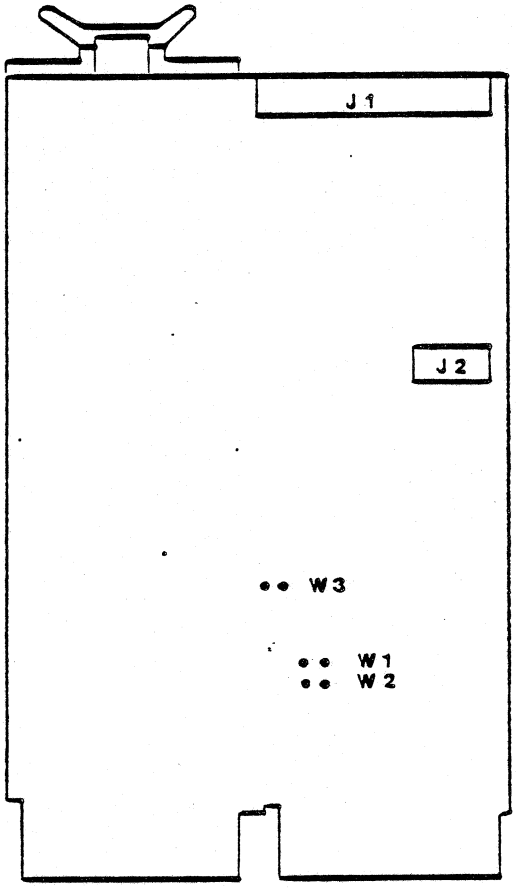

Figure 2-1. PM-CTCV11A Jumper and Connector Locations

2.2 Installing in Backplane

To install the PM-CTCV11A in a LSI-11 compatible backplane oberve the following:

1. Power down the system before installing the PM-CTCV11A in the backplane.

Caution

You must remove DC power from the backplane before module insertion or removal.

2. Install the PM-CTCV11A in any available dual-wide slot.

Note

It is preferable to install the PM-CTCV11A in the lowest priority dual-wide slot.

3. Install the PM-CTCV11A with the component side facing the same direction as the component side of the other boards in the backplane. The board, backplane, or both can be damaged if the board is installed backwards.

2.3 Cabling

After you have installed the PM-CTCV11A in the backplane, connect the cables observing the following:
(Reference Figure 2-2)

Note

If you are installing PM-CTCV11A-100, follow Steps 1 and 4 only.
If you are installing PM-CTCV11A-101, follow steps 1 through 4.

1. Connect a 50-pin flat ribbon drive I/O cable from PM-CTCV11A J1 to drive J1.

2. Connect a 10-pin flat ribbon status control cable from PM-CTCV11A J2 to LED assembly J1.

3. To connect the LED indicator cable (703719-100) from the LED indicator assembly to the drive:

   a. Connect one end of the cable to LED indicator assembly J2.

   b. Solder the other end of the cable to the tape drive. For example, with a Cipher Quarterback*:

      o Solder the black wire to IC 3B, Pin 4. This is the Cartridge Present line.

      o Solder white wire to IC 3B, Pin 2. This is the Write Protect line.

4. Ensure that all cables are installed and routed so they cannot be damaged.

Figure 2-2 shows cabling for a typical subsystem configuration using the PM-CTCV11A.

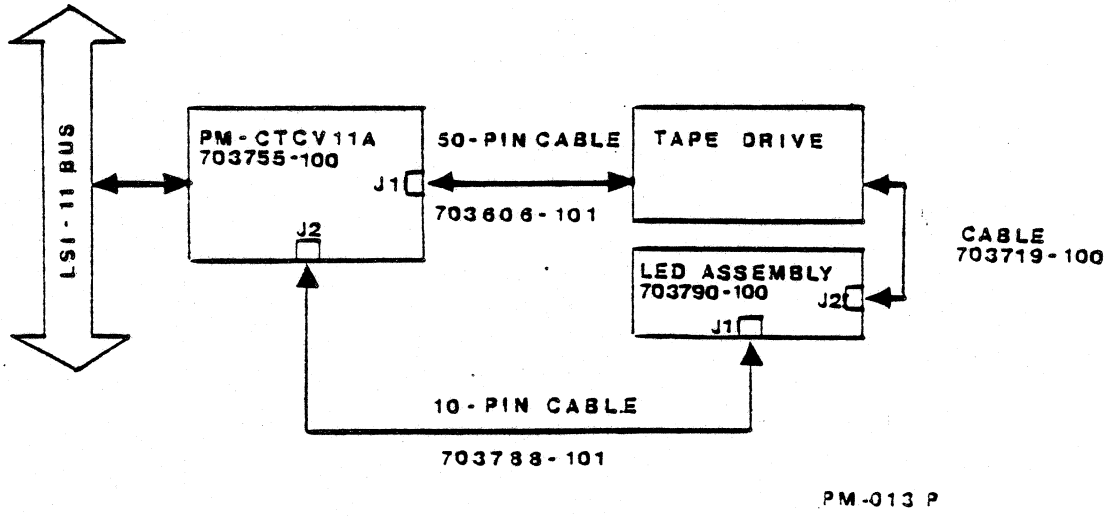

Figure 2-2. PM-CTCV11A Cabling

* Quarterback is a registered trademark of Cipher Data Products, Inc.

3.0 Initial Start-up and Diagnostics

After installing the PM-CTCV11A in your system, you must follow certain start-up procedures to ensure your coupler is operating with your equipment. Plessey also suggests that you run the supplied diagnostics.

3.1 Initial Start-up

To start-up your system using a PM-CTCV11A:

1. Power up the system.

2. Ensure that there is 4.95 to 5.05 VDC on the backplane.

3. If you are going to use the on-board hardware boot capablity, follow these steps.

   a. Insert bootable cartridge into tape drive.

   b. Disable the system line time clock (LTC).

   c. Enter the processor online debugging technique (ODT) mode.

   d. If you are using a Plessey subsystem, enter "BT" for automatic bootstrap.

      If you are using a system other than Plessey, enter "777100G" and type carriage return <CR>.

      Note

      This will cause the PM-CTCV11A coupler to read and execute the boot block of a bootable tape (SL 800157) which has been previously written in the bootable tape format as specified in Section 4.8 of this manual.

4. It is suggested that you run CPU diagnostics and memory diagnostics to ensure the system is in good working order.

5. Run the diagnostics supplied in the PM-CTCV11A Diagnostic Kit PDD101PK1. Section 3.2 guides you in running these Plessey diagnostics.

3.2 Diagnostics

The PM-CTCV11A coupler is supplied with Plessey diagnostics on cartridge tape. The Diagnostic Kit number is PDD101PK1. We suggest you run these diagnostics, as well as CPU and memory diagnostics, before operating the coupler in your subsystem.

The PM-CTCV11A Diagnostic Kit PDD101PK1 contains:

- SL 800157 XXDP- Monitor (Bootable Core Image)
- SL 800141-100 Basic Logic Test PBTDAC
- SL 800142-100 Data Reliability Test PBTDBC
- Program listings and descriptions on microfiche

3.2.1 Basic Logic Test PBTDAC

Plessey's Basic Logic Test PBTDAC checks all the functions of the PM-CTCV11A coupler.

To run PBTDAC:

1. Boot the system.

2. Load the BT cartridge tape (PDD101PK1).

3. At the "$", type "BT" <CR>. The system will print:

```
F<CR> TO SET THE FILL COUNT
D<CR> FOR DIRECTORY ON CONSOLE, OR
D/L<CR> FOR DIRECTORY ON LINE PRINTER, OR
R FILENAME <CR> TO RUN ANY OTHER PROGRAM
L FILENAME <CR> TO LOAD A PROGRAM ONLY
S <CR> TO START A PROGRAM AT SPECIFIC ADDRESS
```

4. In response to the "." on the monitor, enter:

```
.R PBTDAC <CR>
```

5. This message will appear on the operator console:

```
CSV11A BASIC LOGIC TEST (PBTDAC) DIAGNOSTIC SL 800141-100 REV C

ATP  Y  OR  N?
```

Note

If you have an 11/23 processor, go on to step 6. But if you have an 11/02 processor, first go to the special patch instructions on page 3-3.

6. Insert a scratch tape. Load the scratch tape BEFORE you enter "Y", or you will write over the diagnostic tape.

7. Enter "Y <CR>" at the operator console. This will cause all the subtests which do not require manual intervention to be performed.

Note

> Entering "N <CR>" will cause the program to output the executive prompt message "EX-", and wait for operator input. The executive commands are explained on the supplied microfiche.

8. When the diagnostic has finished, this message will appear on the operator console:

   END OF PASS XX ERR TOTAL XX

We suggest you run one successful pass of the Basic Logic Test PBTDAC.

11/02 Software Patch Instructions

To run the PBTDAC diagnostic with 11/02 systems, you must use this software patch. An 11/02 system will halt after the "CSV11A BASIC LOGIC TEST (PBTDAC) DIAGNOSTIC SL 800141-100 REV C" message. To run this diagnostic with and 11/02, use the following patch:

A. Enter <BREAK>.

B. Enter:

Location	Is	Should Be
7154 /	7352	7356
7350 /	401	5037
7352 /	22626	177572
7354 /	5537	401
7356 /	177572	22626

C. Enter @200G.

D. This message will appear on the operator console:

   CSV11 BASIC LOGIC TEST (PBTDAC) DIAGNOSTIC SL 800141-100 REV C

   ATP Y OR N ?

   At this point, go back to step 6 at the top of this page and continue.

3.2.2 Data Reliability Test PBTDBC

The Data Reliability Test PBTDBC is a data integrity test for the PM-CTCV11A coupler.

To run PBTDBC:

1. Load the BT cartridge tape (PDD101PK1).

2. At the "$", type "BT" <CR>. The system will print:

   F<CR> TO SET THE FILL COUNT
   D<CR> FOR DIRECTORY ON CONSOLE, OR
   D/L<CR> FOR DIRECTORY ON LINE PRINTER, OR
   R FILENAME <CR> TO RUN ANY OTHER PROGRAM
   L FILENAME <CR> TO LOAD A PROGRAM ONLY
   S <CR> TO START A PROGRAM AT SPECIFIC ADDRESS

3. In response to the "." on the monitor, enter:

   .R PBTDBC <CR>

4. This message will appear on the operator console:

   CSV11A DATA RELIABILITY TEST (PBTDBC) DIAGNOSTIC SL 800142-100 REV C

   ATP Y OR N?

5. Insert a scratch tape. Load the scratch tape BEFORE entering "Y", or you will write over the diagnostic tape.

6. Enter "Y <CR>" at the operator console. This will cause all the subtests which do not require manual intervention to be performed. During program execution, all hard or fatal errors will be displayed on the operator terminal.

Note

Entering "N <CR>" will cause the program to output the executive prompt message "EX-", and wait for operator input. The executive commands are explained on the supplied microfiche.

7. When the diagnostic has finished, this message will appear on the operator console:

END OF PASS XX ERR TOTAL XX

BYTES WRITTEN	HARD WRITE ERRORS	SOFT WRITE ERRORS	BYTES READ	HARD READ ERRORS	SOFT READ ERRORS	UNDER-RUN	DATA CMPR ERRORS
XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX

At the end of a program pass, the total number of program errors detected will be listed as well as the accumalated number of bytes written and read, and number of hard and soft read and write errors detected.

We suggest you run <u>three</u> successful passes of the Data Reliability Test PBTDBC. A "successful pass" should have no more than <u>three soft errrors</u>.

4.0 Functional Description

This section describes the PM-CTCV11A so that a programmer, knowledgeable of QIC-02 interface drives, can write a system backup utility. However, Plessey offers CIB, an off-line utility, to run system backup with the PM-CTCV11A.

4.1 General Description

The PM-CTCV11A coupler transfers commands from the LSI-11 system to the tape drive. Write and Read commands initiate DMA data transfer to or from the tape drive. A Read Status command interrogates the drive and coupler, and then leaves the status in memory using a DMA operation.

The PM-CTCV11A handles LSI-11 bus handshakes, DMA control, and interrupts. The PM-CTCV11A coupler will generate interrupts when a command is completed and when the Interrupt Enable Bit is set to 1. The coupler can send up to three (3) data blocks to the drive to be formatted. The drive also handles tape control and processes Read/Write data.

4.2 LSI-11 Bus Interface Registers

Information is processed between the coupler and LSI-11 system via the LSI-11 bus registers. Two (2) registers control operation of subsystem: the Control Status Register (CSR), and the Device Register (REG).

Primary and secondary device address and vector are selected by a single jumper on the PM-CTCV11A. Table 4-1 lists primary and secondary register set assignments.

Table 4-1. Primary and Secondary Register Sets

Register	Primary	Secondary
CSR	777500	777340
REG	777502	777342
Vector	000360	000214

To access a register in the Device Register, REG, that register must first be selected using SEL bits in CSR. For example, to access the Current Memory Address (CMA) register, set Bit 2 to 1, and Bit 1 to 0. The CMA register will now be presented in REG address.

Figure 4-1 shows the bit assignments for the registers.

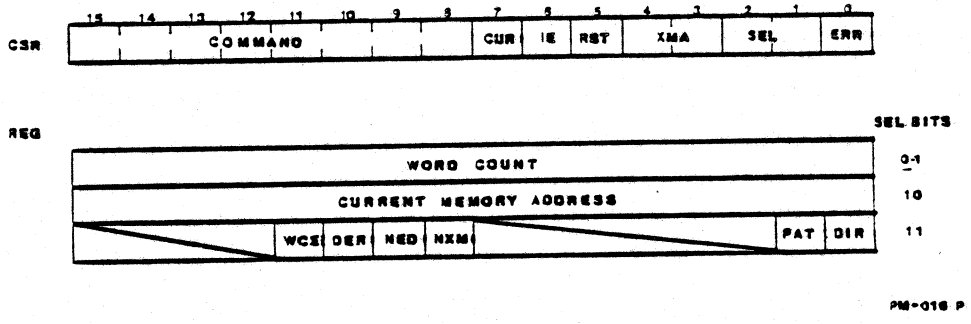

Figure 4-1. Register Bit Assignments

Table 4-2. Control Status Register Bit Assignments

Bit	Description
0 READ ONLY	ERROR (ERR) Set upon detection of any coupler error condition or when drive EXCEPTION line is active. BUS INIT or writing a 1 into Bit 5 of CSR (RESET) will cause ERR to set. Reset at beginning of any command.
1,2 READ/WRITE	SELECT REGISTER (SEL) These bits READ/WRITE select the register that will be accessed in REG location. Bit 2 Bit 1 1 1 Maintenance Reg. 1 0 Current Memory Address Reg. 0 1 Word Count Reg. 0 0 Undefined - This condition exists after INIT or RESET.
3,4 READ/WRITE	EXTENDED ADDRESS (XMA) These bits are used to address Bits 16 and 17 on the bus during a DMA operation. Reset by INIT or RESET.
5 WRITE ONLY	RESET (RST) When set to 1, coupler and drive will reset.
6 READ/WRITE	INTERRUPT (IE) When set to 1, the coupler will generate an interrupt to the CPU upon completion of a command. To disable interrupting, 0 must be written into the bit location. Bit will be reset by BUS INIT or RESET (CSR Bit 5 = 1).
7 READ ONLY	CONTROL UNIT READY (CUR) When set to 1, the coupler is ready to accept a command. Also, after a RESET or BUS INIT this bit will be 1. When this bit is 0, all other bits in either register are invalid.
8-15 WRITE ONLY	COMMAND (CMD) These bits accept the drive command from the CPU and transfer it to the drive. A command of 0 is NO-OP to the drive and will not cause any action. When a command is accepted, the CUR BIT (Bit 7) will be 0, and all other bits will be invalid until the command is complete. If the command encounters an error condition, Bit 0 (ERR) and Bit 7 (CUR) will be set to 1. A READ STATUS command must follow this condition. Command bits will always read back as 0.

Table 4-3. Maintenance Register (SEL =11) Bit Assignments

Bit	Description
0 READ ONLY	DRIVE DIRECTION ERROR (DIR) When set, indicates DIRECTION line was detected active by the Initialization Diagnostic. Reset only after corrective action at the drive and successful initialization.
1 READ ONLY	DRIVE BUS PATTERN ERROR (PAT) When set, indicates failure of the drive bus pattern test during Initialiation Diagnostic.
2-7	UNASSIGNED
8 READ ONLY	NON-EXISTANT MEMORY (NXM) When set, indicates a time-out (10 s) occured during a DMA operation. Reset by READ STATUS command, RESET or BUS INIT. This bit is duplicated in CEB.
9 READ ONLY	NON-EXISTANT DRIVE (NED) When set, indicates the EXCEPTION condition was not detected during Initalization. Therefore, it is assumed the drive does not exist. This bit is duplicated in CEB.
10 READ ONLY	DRIVE ERROR (DER) This bit is set when EXCEPTION is detected during procesing at a command. Reset by READ STATUS command. This bit is duplicated in CEB.
11 READ ONLY	WORD COUNT ERROR (WCE) When set, READ or WRITE operation was attempted with a non-256 multiple word in word count. Reset by READ STATUS command, RESET or BUS INIT.
12-15	UNASSIGNED

Table 4-4. Word Count Register (SEL=01) Bit Assignments

Bit	Description
0-15 READ/WRITE	WORD COUNT (WC) Must be loaded with the negative number of words to be transferred during a WRITE or READ command. NOTE: Only 256-word multiples are valid. Any other word count will cause ERROR (Bit 1, CSR) and WCE (Bit 2, CEB) to be set when a READ or WRITE command is issued. These bits remain unchanged following a BUS INIT or RESET, but will be set to 0 following a READ STATUS COMMAND.

Table 4-5. Current Memory Address Register (SEL=10) Bit Assignments

Bit	Description
0-15 READ/WRITE	CURRENT MEMORY ADDRESS (CMA) Must be loaded with the desired beginning memory address prior to READ, WRITE or READ STATUS Command. Will be incremented (by 2) for each word transferred during a DMA operation. Starting memory address must be on a word boundary. These bits remain unchanged following a RESET or BUS INIT.

4.3 Resets

Following a BUS INIT or coupler CLEAR, CUR (BIT 7, CSR) must be interrogated to determine when the PM-CTCV11A is ready to respond to bus operations.

4.4 On-board Hardware Boot Function

The PM-CTCV11A has an on-board hardware boot capability that is enabled by executing the command "777100G" using the on-line debugging technique (ODT). Reference Section 3.2 for operation procedure. During the on-board hardware boot function, the coupler reads and executes the boot block of a bootable tape. The bootable tape format is specified in Section 4.8.

4.5 Commands

A detailed description of command functions at the drive/formatter level can be obtained from your drive specification. Only system level functions will be discussed here.

A command is issued by writing the drive image of the command into the high byte (Bits 8-15) of the CSR. Commands requiring DMA operations (Read, Write and Read Status) must set up the beginning memory address in the CMA register. Additionally, Read and Write operations must set up the inverse number of words to be transferred in the Word Count register prior to issuing a command. If programming is to be interrupted upon completion of the command, the Interrupt Enable Bit must be set. If interrupt mode is not desired, the IE Bit must be reset.

When any non-zero data is written into the command byte of the CSR, a command is initiated in the PM-CTCV11A. The CUR bit of the CSR goes to 0. All other bits in the CSR and REG are invalid. Errors are cleared at the beginning of all but the Read Status command. If an error is encountered during command processing (i.e. EXCEPTION from the drive), error (Bit 0) and CUR (Bit 7) of CSR are set. If IE is set the coupler interrupts the processor and the command is complete. All bits in CSR and REG are valid when CUR = 1.

Normal command completion will generate an interrupt if IE is set in CSR. Completion status in CSR will indicate CUR - 1 ERR = 0.

4.6 System Status

The PM-CTCV11A coupler and drive status may be interrogated by issuing a Read Status command. A Read Status command is required following any error condition (ERR = 1).

The Read Status command loads four (4) status words into memory by a DMA operation. The CMA and extended address bits must be loaded with the desired memory first location. Figure 4-2 shows the order in which status is loaded into memory.

If an error is encountered during a Read Status command, CSR Bits 0 and 7 will be set, and an interrupt will be generated if enabled. If no error is encountered, only CUR bit (Bit 7) will be set and an interrupt will be generated if enabled.

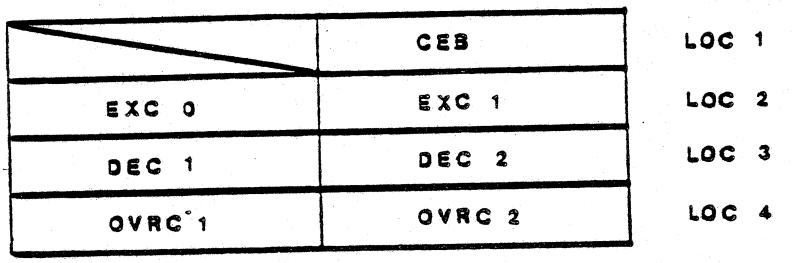

Figure 4-2. Status Map

Tables 4-6, 4-7, 4-8, 4-9, and 4-10 define the status bits. For a complete definition of drive status bits, refer to your drive specification.

Table 4-6. Coupler Error Byte (CEB)

Bit	Description
0	NON EXISTANT MEMORY (NXM) Defined in Maintenance Register Bit 8.
1	NON EXISTANT DRIVE (NED) Defined in Maintenance Register Bit 9.
2	DRIVE ERROR (DER) Defined in Maintenance Register Bit 10.
3	WORD COUNT ERROR (WCE) Defined in Maintenance Register Bit 11.

Table 4-7. Exception Byte 1 (EXC 1)

Bit	Description
0	Reset
1	Unused
2	Unused
3	Beginning of Media
4	Unused
5	No Data
6	Illegal Command
7	Exception Bits 1

Table 4-8. Exception Byte 0 (EXC0 0)

Bit	Description
8	File Mark Detected
9	BIE not Located
10	Unrecoverable Data Error
11	End of Tape
12	Write Protected
13	Drive not On-line
14	Cartridge not in Place
15	Exception Byte 0

Table 4-9. Data Error Counters (DEC 1, DEC 2)

Bit	Description
0-15	During Write operations: number of blocks rewritten. During Read Operations: number of soft read errors.

Table 4-10. Overrun Counter (OVRC 1, OVRC 2)

Bit	Description
0-15	During Write Operations: number of extended gaps. During Read Operations: number of read buffer underruns.

4.7 Drive/Formatter Interfaces

Any non-zero information in CMD byte (Bits 8-15) of CSR is transferred directly to the formatter from the PM-CTCV11A. All interface handshakes are accomplished by the coupler. If an EXCEPTION condition is generated by the formatter, the PM-CTCV11A sets ERR (CSR Bit 0) and aborts the operation. Only 256-word data blocks may be transferred between coupler and formatter. The word count is checked prior to a Read or Write operation to ensure that only 256 word multiples are attempted. If the word count is not a 256-word multiple, the command is aborted and ERR (Bit 0, CSR) is set.

4.8 Bootable Tape Format

The format for tape to be used with the PM-CTCV11A coupler is defined as follows:

1. The first 512-byte block of Track 0 of the bootable tape shall be designated the Tape Label Block. No format for this block is currently specified. This block contains information required to identify the tape. This information is currently unspecified.

2. The second 512-byte block of Track 0 of the bootable tape is the Boot Block and shall be a 512-byte core image of boot program to be loaded into physical memory addresses 0 - 377 octal. After loading, execution is started at memory address 0. Bytes are ordered in conventional PDP-11 right/left byte to word sequence.

3. The third 512-byte block of Track 0 of the bootable tape must not be the filemark block.

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ADDITIONAL COMMENTS: