4K RAM BOARD

DOCUMENTATION

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"Creative Electronics"

THEORY of OPERATION

88-4MCD 4K DYNAMIC RAM BOARD OPERATION

The 4K RAM Board provides 4,096 words of Dynamic Random Access Memory for the ALTAIR 8800. Each individual board contains memory protect circuitry, and address selection circuitry for any one of 16 starting address locations in increments of 4K. The maximum access time is 300 nanoseconds; thus, there is no "wait" requirement unless Refresh is occurring at the time of access.

Refresh

This memory board is designed around a dynamic integrated circuit, TMS 4030 or C2107A IC's. These dynamic IC's require each row within the chip to be accessed every 2 milliseconds or less. This is accomplished by accessing one of the 64 rows every 64 clock pulses (32 microseconds).

The ϕ2 clock is buffered through one gate of IC S and then inverted through one gate of IC A. It is then divided in half through flip-flop Ta, and divided again by 16 through a 4-bit counter (IC D). The final signal is fed to the clock input of flip-flop Ga. Thus, after 32 clock pulses Ga will toggle, and will toggle again after another 32 clock pulses. This will add one count to the 6-bit counter, IC's E & F, which sets up the refresh address at the inputs of IC O.

Ga is also used to trigger single-shot Ha. This partially enables IC K pin 11 and toggles flip-flop Gb, partially enabling IC K pin 3.

If the computer is in the run mode, a SYNC pulse, inverted through one gate of IC A, will occur within approximately 10 microseconds. This causes IC K pin 11 to go low for 500 nanoseconds and IC K pin 3 to go high for 500 nanoseconds. On the falling edge of this pulse, single-shot Ia is triggered. The pulse from IC Ia pin 13 disables the machine address and triggers IC Ib. The IC Ia pin 4 output is delayed less than 100 nanoseconds and fed to the chip-enable voltage level shift circuit (4 gates of IC Z, Q1, R1, R2, D1 & C1) and also clears flip-flop Gb.

The output of this circuit provides a 500 nanosecond, +12 volt pulse to the RAM IC's to accomplish the required access.

If the machine had been in a stop mode when the refresh pulse occured, there would have been no SYNC pulse. In this case refresh would have occured with the falling edge of the pulse from IC Ha, approximately 12 microseconds later.

The function of IC Ib is to disable the read-write single-shot, IC Hb, and to pull the Ready line active if the card is accessed during re-fresh. This puts the machine is a wait state until refresh has been accomplished. IC Hb is then triggered for a normal read or write.

Read

IC Hb is partially enabled by MEMR. When SYNC and ϕ1 occur, if re-fresh is not occuring keeping IC J pin 4 low, then IC K pin 8 goes low and pulls IC J pin 6 high. Approximately 90 nanoseconds later ϕ1 returns low, IC K pin 8 goes high and IC J pin 6 goes low trig-gering IC Hb. This pulls chip enable (CE) high for 500 nanoseconds.

After approximately 300 nanoseconds the data out of the RAM chips is valid. It is latched into the 8-bit latch (IC N) via the strobe in-put, IC N pin 11, by IC Hb pin 5.

The final requirement to place the data onto the bus is with the latch enable inputs, pins 1 & 13 of IC N. Pin 1 is pulled low by IC J pin 8 (card select) and pin 13 is pulled high by MEMR. This enables the latch outputs and presents the data to the bus.

Write

The write mode is identical to the read mode, except that the latch outputs are not enabled and the write inputs to the RAMS are activated.

The MWRITE signal partially enables the read-write single-shot, IC Hb, and is also gated with the output of Hb to IC L pins 9 & 10. When both signals are high (active) IC L pin 8 goes low. If memory is un-protected (IC M pin 6), IC M pin 4 goes high and IC A pin 4 goes low.

This pulls the write input of the memory chips to the low active write mode while at the same time chip enable is high (Hb pin 12) and the data (buffered and inverted through IC's R & Z) is present at the RAM data inputs.
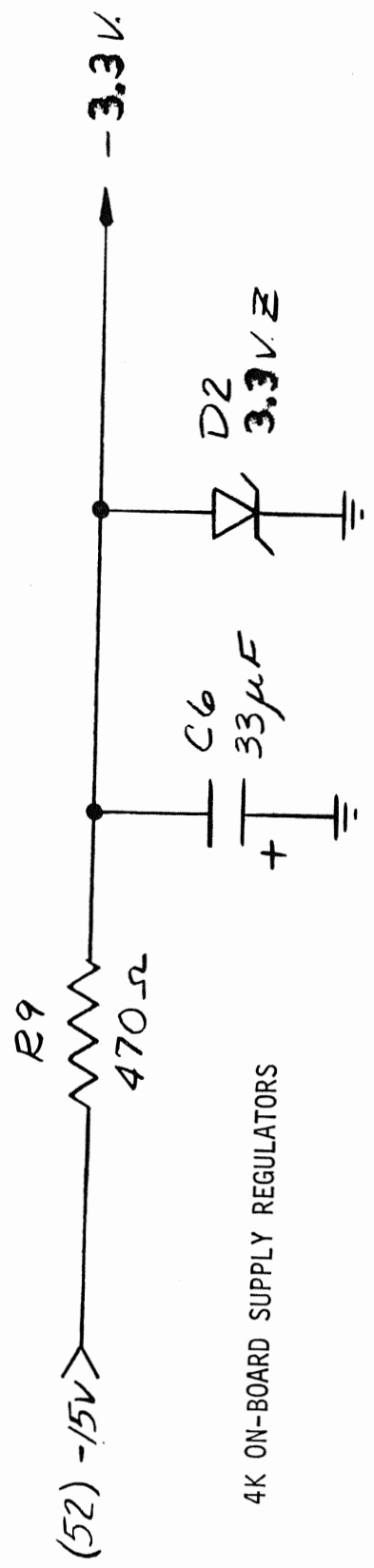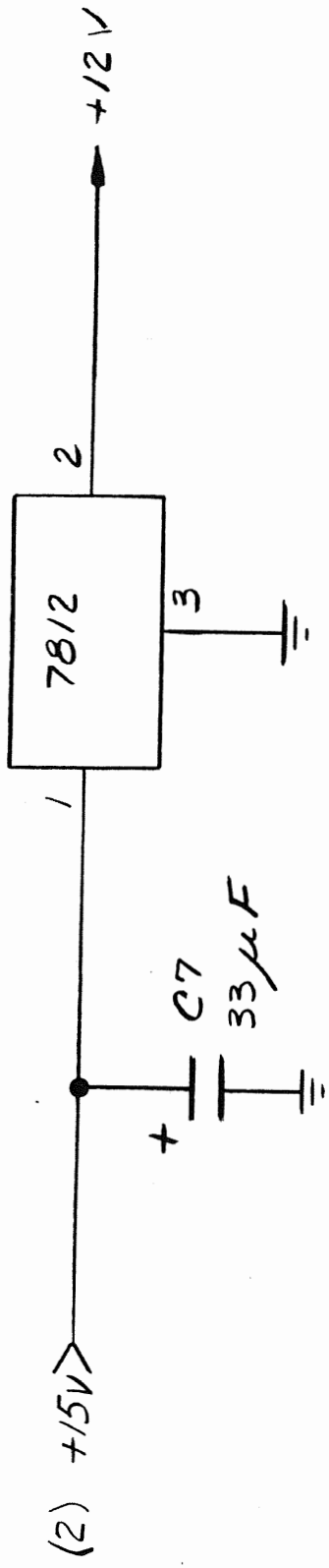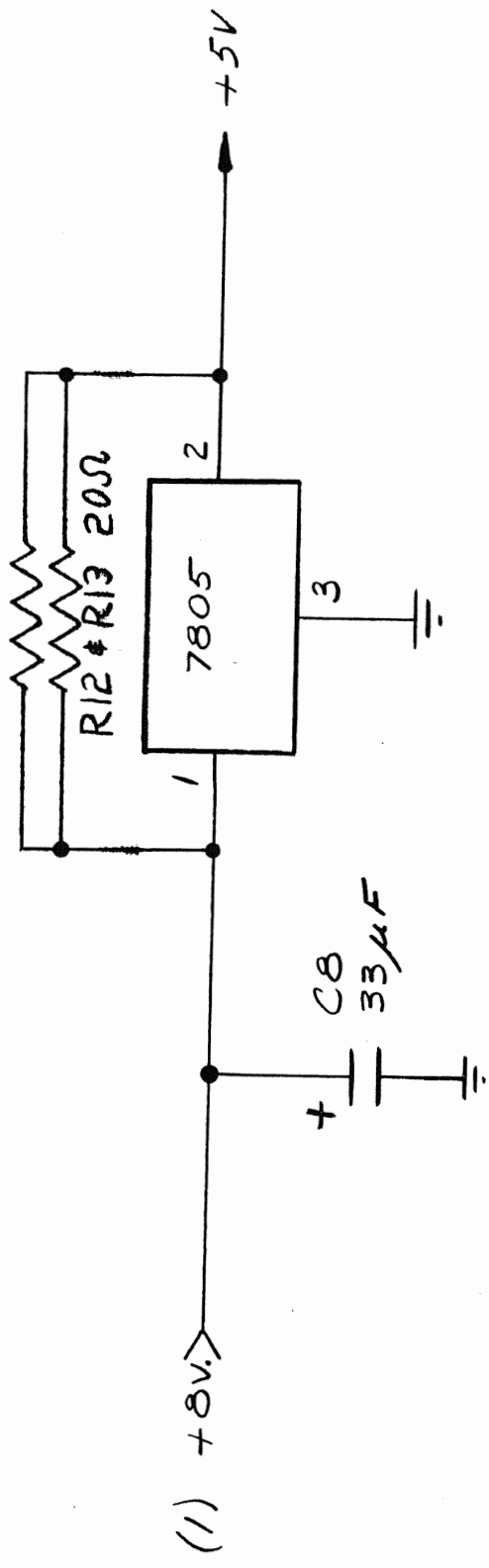
Protect

The entire 4,096 words of memory on the board can be protected via the front panel PROTECT switch.

When the card is selected (IC M pin 3) and the switch lifted to the PROTECT position (IC M pin 2), the output of IC M pin 1 toggles the flip-flop Tb. This pulls IC M pin 6 high to disable the write input to the RAMS, and pulls buffer IC S pins 13 & 14 low to light the PROTECT light on the front panel.

The memory will remain protected until power is turned off or the PROTECT switch is pushed to the UNPROTECT position.

When power is first applied to the unit the $\overline{POC}$ signal (Power On Clear) is pulled low for several milliseconds, insuring that the memory is unprotected.

+5V

R12 & R13 20Ω

7805

2

3

C8
33μF

(1) +8v.

+12 V

7812

2

3

C7
33μF

(2) +15V

−3.3 V.

D2
3.3V Z

C6
33μF

R9
470Ω

(52) −15V

4K ON-BOARD SUPPLY REGULATORS

DISPLAY/CONTROL BOARD CAPACITOR MODIFICATIONS

NOTE: THE FOLLOWING CAPACITOR VALUE SUBSTITUTIONS ARE CRITICAL IN THE
OPERATION OF AN ALTAIR SYSTEM USING 4K DYNAMIC MEMORY BOARDS.   THE
NECESSARY CAPACITORS WILL BE INCLUDED WITH EACH ALTAIR KIT AND WITH
EACH 4K MEMORY BOARD KIT, BUT THE SUBSTITUTIONS NEED BE PERFORMED ONLY
ONCE.   PERFORM THE SUBSTITUTIONS WHETHER YOU HAVE 4K BOARDS OR NOT.

THE FOLLOWING CAPACITORS ON THE DISPLAY/CONTROL BOARD ARE
TO BE CHANGED TO THE VALUES INDICATED BELOW:

C7 should now be 0.01µf

C8 should now be 0.1µf

THESE SUBSTITUTIONS ARE TO IMPROVE THE OPERATION OF THE ALTAIR'S
DEPOSIT CIRCUITRY.

THE FOLLOWING ADDITIONS AND CHANGES APPLY TO ALL "REV 0.2"
4K RAM BOARDS. BE SURE TO READ THESE OVER CAREFULLY BEFORE
BEGINNING CONSTRUCTION. WITH THESE EXCEPTIONS, THE REST OF
THE ASSEMBLY PROCEDURE IS AS STATED IN THE MANUAL.

There are four additional components to be added to the board
which are not shown on the silk-screen. These include a diode,
a resistor and two capacitors.

Refer to the component layout drawing on page 3 of this errata
and install the additional components in the positions shown.

NOTE: The .luf capacitor is not shown in the schematic.
       This capacitor is merely for noise suppression.

THE LEFT SIDE OF JUMPER J6 SHOULD NOT BE CONNECTED TO THE PAD
INDICATED BY THE SILK-SCREEN ON THE BOARD. IN THE DRAWING
YOU WILL NOTE THAT THE PAD FOR THE LEFT SIDE OF THIS JUMPER
IS NOW LOCATED JUST BELOW IC L.

The following information applies to specific pages of the
assembly manual:

OK PAGE 3:   IC B is now a 74LS04, IC L is now a 74LS00

   PAGES 8 & 9:   Diode D2, listed in the instructions as a 1N746A,
                  3.3v zener, will be so only if your kit contains
                  TMS 4030 memory IC's. If your kit is supplied
                  with the Intel C2107A's or TMS 4060-2's, then this
                  diode will be a 1N4733, 5v zener instead.

   PAGES 10 & 11: The markings on the silk-screen for two of the
                   jumper wire connections are incorrect. Just
                   beneath IC S, there are two pads next to each
                   other labeled J2 & J10. These two pads have
                   reverse markings; J2 should be J10, and J10
   should be J2. Connect them accordingly.

THERE HAVE BEEN IC SOCKETS ADDED TO YOUR KIT FOR MOUNTING SEVERAL OF THE INTEGRATED CIRCUITS.

A 24 PIN IC SOCKET HAS BEEN ADDED FOR IC N. THIS MAY BE ONE OF TWO TYPES. ONE TYPE IS A SINGLE UNIT AND WILL FIT DIRECTLY INTO THE HOLES ON THE BOARD FOR MOUNTING THE IC. THE OTHER TYPE IS ACTUALLY TWO HALVES JOINED TOGETHER BY SOME CROSS PIECES. USE WIRE CUTTERS TO RE-MOVE THE CROSS PIECES, SEPARATING THE HALVES. MOUNT THE SOCKET TO THE BOARD IN THE SAME MANNER AS YOU WOULD AN INTEGRATED CIRCUIT, THEN IN-STALL THE IC INTO THE SOCKET.

SOCKETS HAVE ALSO BEEN PROVIDED FOR THE MEMORY IC'S, MC-0 THROUGH MC-7. THESE SOCKETS MAY ALSO BE ONE OF TWO DIFFERENT TYPES. ONE TYPE WILL BE A SINGLE 22 PIN UNIT AND SHOULD BE INSTALLED IN THE SAME MANNER AS THE ONE MENTIONED ABOVE. THE OTHER TYPE IS EXACTLY LIKE THE TWO PIECE ONE MENTIONED ABOVE, AND SHOULD BE SEPARATED IN THE SAME MANNER. THIS ONE WILL ALSO REQUIRE A MODIFICATION IN ORDER TO ACCOMODATE THE 22 PIN IC'S. USE NEEDLE-NOSE PLIERS TO PULL ONE OF THE END PINS FROM EACH OF THE 16 SOCKET HALVES. WHEN MOUNTING THESE, KEEP THE HOLE WITH THE PIN MISSING TOWARDS THE BOTTOM OF THE BOARD. KEEP THE IC TOWARDS THE TOP OF THE BOARD WHEN INSTALLING IT SO THAT THE HOLE WITH THE MISSING PIN IS NOT USED.

PAGE 13:   Before installing IC MC-1, there is a track running close to one of the IC pads which should be inspected. On the side closest to capacitor C15 there is a PC land which runs between the pads for pins 7 & 8 of the IC. This land runs extremely close to the pad for pin 7.

Check this area of the board very closely, and be sure that the land does not touch the pad. If there is a short, or if you are not certain; use a small sharp knife and cut slightly into the board between the two, just enough to be sure that there is no connection.
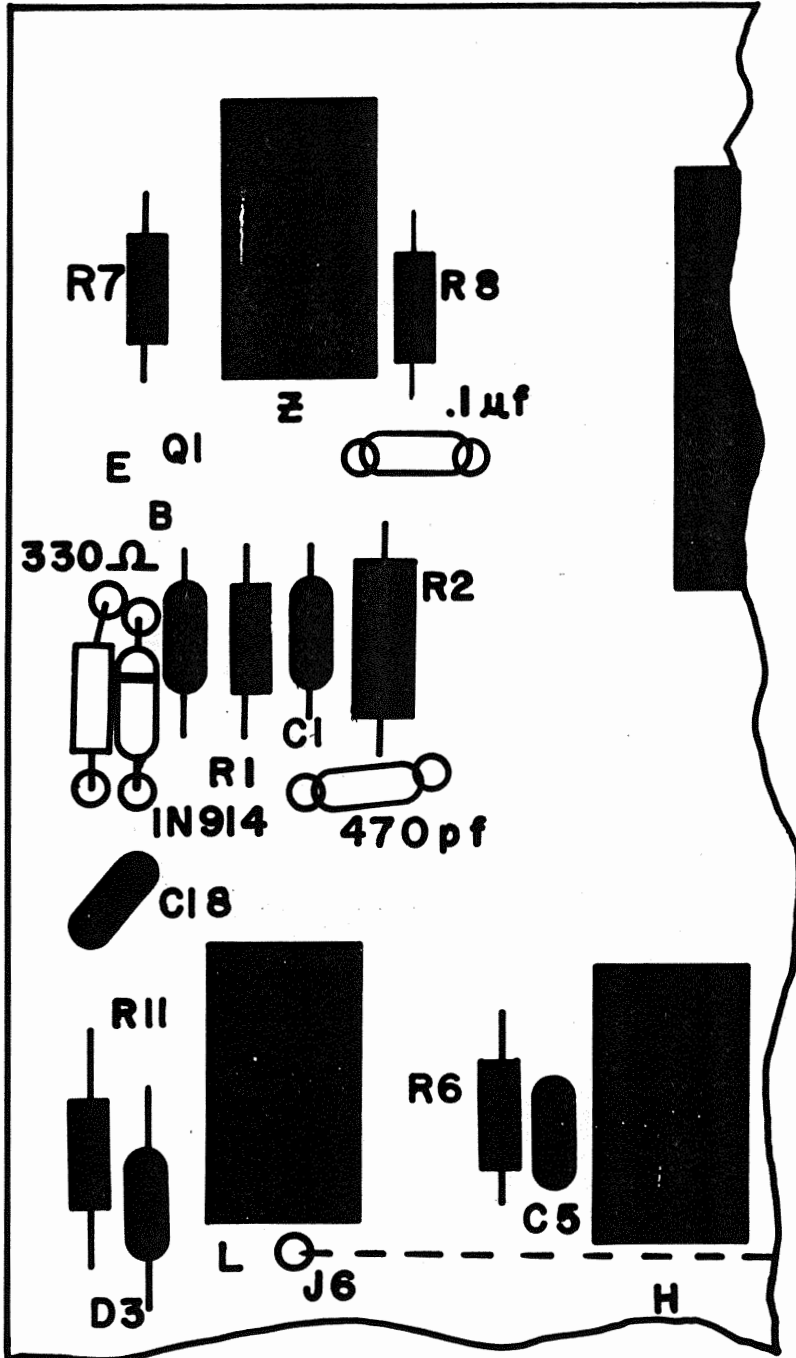
ORIGINAL COMPONENTS ARE SHOWN
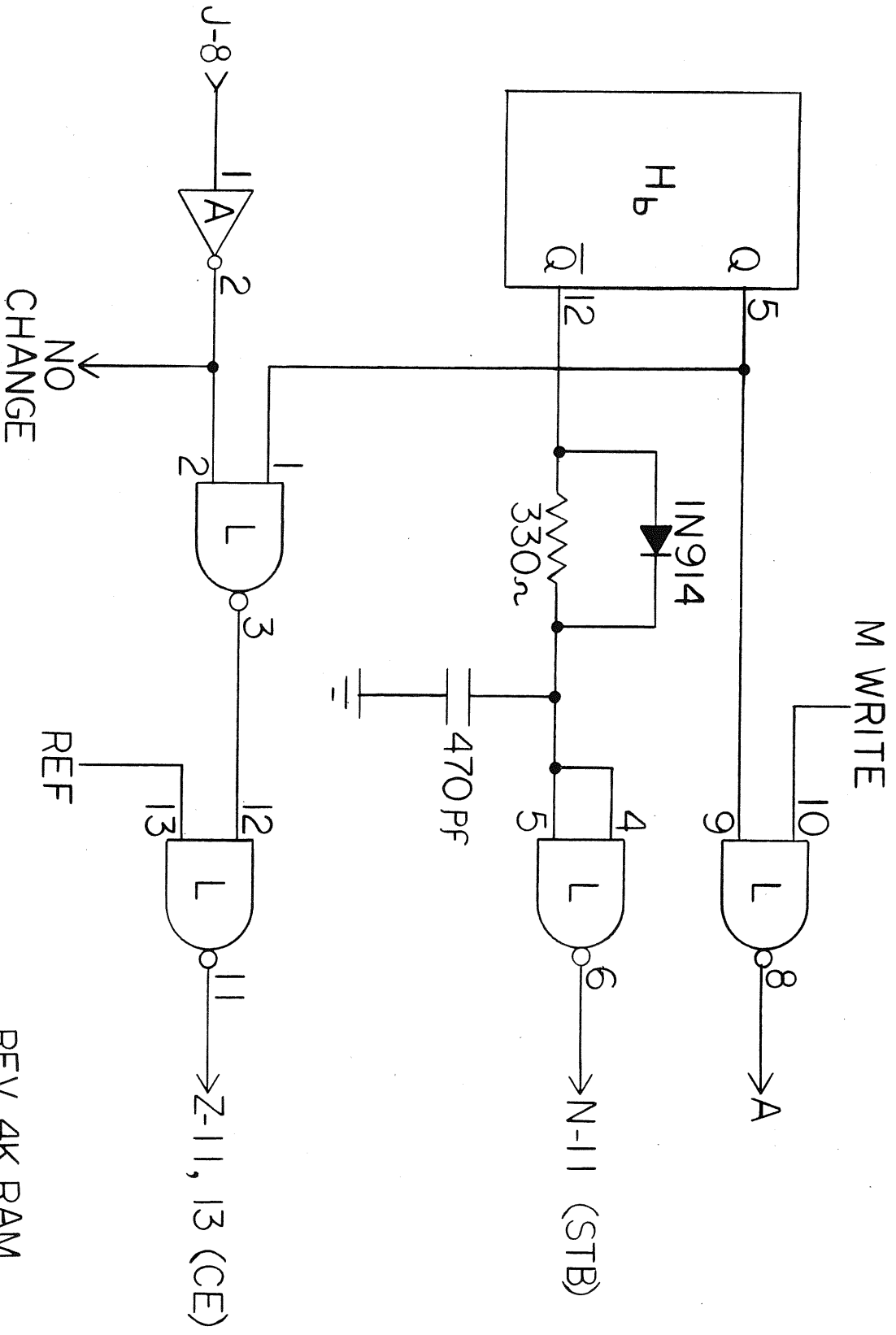IN SOLID BLACK, THE ADDITION-
AL COMPONENTS ARE THOSE SHOWN
OUTLINED.

THESE INCLUDE:

One .1uf capacitor

One 470pf capacitor

One 1N914 diode*

One 330 ohm (orange-
orange-brown) resistor

NOTE ALSO THE NEW LOCA-
TION FOR THE LEFT SIDE
OF JUMPER J6.

*Be sure to align the
band on the diode with
the band shown in the
drawing for the correct
orientation.

4K RAM

REV 0.2

J-8

IA
1
2
NO
CHANGE

Hb
Q
Q̄
12
5

2
1
3

330Ω
IN914
470pf
REF
13
12
11
Z-11, 13 (CE)

5
4
6
N-11 (STB)

M WRITE
9
10
8
A

REV 4K RAM
BOARD
9-23-75

4

88-4MCD
(4K Dynamic RAM)
Parts List
Sept. 1975

BAG 1

1	MC7805	101074
1	MC7812	101085
2	26L123	101066
1	74L00	101080
1	SN74L02	101072
1	74LS04	101042
1	SN7406	101054
1	74L20	101039
2	7473	101027
2	SN74L193	101087
1	SN74193	101037
4	N8T97	101040
2	74L04	101073
1	74LS00	101069

BAG 2

1	8212	101071
8	TI4060-2	101094
8	22 pin sockets	102108
1	24 pin socket	102105

BAG 3

2	.001mF 12v cer	100328
2	470pF 10v cer	100316
3	33mF 16v elec	100326
2	20pF 12v cer	100334
1	100pF 12v cer	100361
1	220pF 12v cer	100314
1	.01 16v	100321

BAG 4

17	.1mF 12v cer	100348

BAG 5

2	#6-32 nut	100933
2	6-32 lockwasher	100942
2	#6-32x1/2" screw	100918
1	Heat sink	101870
1	24" 20-gauge wire	103063
3	36" 26-gauge wire	103060
1	Edge connector	101864
2	Card guides	101714

BAG 6

1	EN2907	102804
5	IN914	100705
1	5.1v zener	100721

BAG 7

2	100 ohm 1/2w	101924
3	1K ohm 1/2w	101928
1	22K ohm 1/2w	101933
1	20K ohm 1/2w	101940
1	27K ohm 1/2w	101989
1	43K ohm 1/2w	101988
2	470 ohm 1/2w	101927
2	20 ohm 1/2w	102048
1	330 ohm 1/2w	101926

MISCELLANEOUS
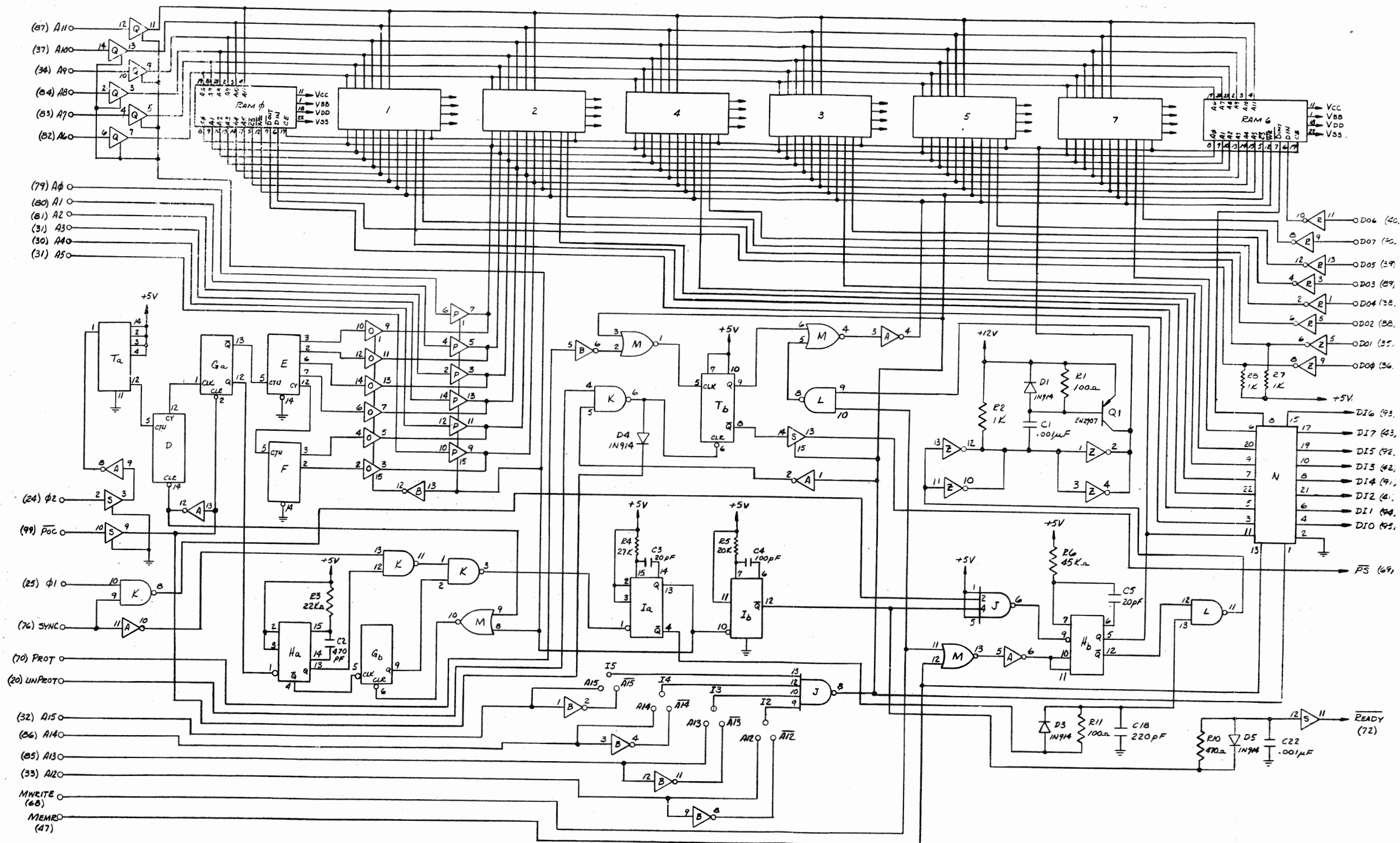
1	PC board	100100
	Manuals	101549

THE FOLLOWING APPLIES TO PAGE 3 OF THE ASSEMBLY MANUAL:

This is a corrected list of the integrated circuits
to be installed on all REVISION 0.2 4K Memory Boards.

(X)   IC's A & R are 74L04's — 9L04

(X)   IC B is a 74LS04

(X)   IC D is a 74193

(X   IC's F & E are 74L193's — 93L66

(X)   IC's G & T are 7473's

(X)   IC's H & I are AM26L123's

(X)   IC J is a 74L20

(X)   IC M is a 74L02

(X)   IC N is an 8212

(X)   IC's O, P, Q & S are 8T97's

(X)   IC K is a 74L00

(X)   IC L is a 74LS00

(X)   IC Z is a 7406

*NOTE: There are several errors in reference to this material,
including the current Parts & BAG lists. Disregard
all other instructions and references to these IC's.*

— 4K RAM BD. —