00	NOP		2B	DCX	H	56	MOV	D,M
01	LXI	B,D16	2C	INR	L	57	MOV	D,A
02	STAX	B	2D	DCR	L	58	MOV	E,B
03	INX	B	2E	MVI	L,D8	59	MOV	E,C
04	INR	B	2F	CMA		5A	MOV	E,D
05	DCR	B	30	- - -		5B	MOV	E,E
06	MVI	B,D8	31	LXI	SP,D16	5C	MOV	E,H
07	RLC		32	STA	Adr	5D	MOV	E,L
08	- - -		33	INX	SP	5E	MOV	E,M
09	DAD	B	34	INR	M	5F	MOV	E,A
0A	LDAX	B	35	DCR	M	60	MOV	H,B
0B	DCX	B	36	MVI	M,D8	61	MOV	H,C
0C	INR	C	37	STC		62	MOV	H,D
0D	DCR	C	38	- - -		63	MOV	H,E
0E	MVI	C,D8	39	DAD	SP	64	MOV	H,H
0F	RRC		3A	LDA	Adr	65	MOV	H,L
10	- - -		3B	DCX	SP	66	MOV	H,M
11	LXI	D,D16	3C	INR	A	67	MOV	H,A
12	STAX	D	3D	DCR	A	68	MOV	L,B
13	INX	D	3E	MVI	A,D8	69	MOV	L,C
14	INR	D	3F	CMC		6A	MOV	L,D
15	DCR	D	40	MOV	B,B	6B	MOV	L,E
16	MVI	D,D8	41	MOV	B,C	6C	MOV	L,H
17	RAL		42	MOV	B,D	6D	MOV	L,L
18	- - -		43	MOV	B,E	6E	MOV	L,M
19	DAD	D	44	MOV	B,H	6F	MOV	L,A
1A	LDAX	D	45	MOV	B,L	70	MOV	M,B
1B	DCX	D	46	MOV	B,M	71	MOV	M,C
1C	INR	E	47	MOV	B,A	72	MOV	M,D
1D	DCR	E	48	MOV	C,B	73	MOV	M,E
1E	MVI	E,D8	49	MOV	C,C	74	MOV	M,H
1F	RAR		4A	MOV	C,D	75	MOV	M,L
20	- - -		4B	MOV	C,E	76	HLT	
21	LXI	H,D16	4C	MOV	C,H	77	MOV	M,A
22	SHLD	Adr	4D	MOV	C,L	78	MOV	A,B
23	INX	H	4E	MOV	C,M	79	MOV	A,C
24	INR	H	4F	MOV	C,A	7A	MOV	A,D
25	DCR	H	50	MOV	D,B	7B	MOV	A,E
26	MVI	H,D8	51	MOV	D,C	7C	MOV	A,H
27	DAA		52	MOV	D,D	7D	MOV	A,L
28	- - -		53	MOV	D,E	7E	MOV	A,M
29	DAD	H	54	MOV	D,H	7F	MOV	A,A
2A	LHLD	Adr	55	MOV	D,L	80	ADD	B

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

81	ADD	C	AC	XRA	H	D7	RST	2
82	ADD	D	AD	XRA	L	D8	RC	
83	ADD	E	AE	XRA	M	D9	- - -	
84	ADD	H	AF	XRA	A	DA	JC	Adr
85	ADD	L	B0	ORA	B	DB	IN	D8
86	ADD	M	B1	ORA	C	DC	CC	Adr
87	ADD	A	B2	ORA	D	DD	- - -	
88	ADC	B	B3	ORA	E	DE	SBI	D8
89	ADC	C	B4	ORA	H	DF	RST	3
8A	ADC	D	B5	ORA	L	E0	RPO	
8B	ADC	E	B6	ORA	M	E1	POP	H
8C	ADC	H	B7	ORA	A	E2	JPO	Adr
8D	ADC	L	B8	CMP	B	E3	XTHL	
8E	ADC	M	B9	CMP	C	E4	CPO	Adr
8F	ADC	A	BA	CMP	D	E5	PUSH	H
90	SUB	B	BB	CMP	E	E6	ANI	D8
91	SUB	C	BC	CMP	H	E7	RST	4
92	SUB	D	BD	CMP	L	E8	RPE	
93	SUB	E	BE	CMP	M	E9	PCHL	
94	SUB	H	BF	CMP	A	EA	JPE	Adr
95	SUB	L	C0	RNZ		EB	XCHG	
96	SUB	M	C1	POP	B	EC	CPE	Adr
97	SUB	A	C2	JNZ	Adr	ED	- - -	
98	SBB	B	C3	JMP	Adr	EE	XRI	D8
99	SBB	C	C4	CNZ	Adr	EF	RST	5
9A	SBB	D	C5	PUSH	B	F0	RP	
9B	SBB	E	C6	ADI	D8	F1	POP	PSW
9C	SBB	H	C7	RST	0	F2	JP	Adr
9D	SBB	L	C8	RZ		F3	DI	
9E	SBB	M	C9	RET	Adr	F4	CP	Adr
9F	SBB	A	CA	JZ		F5	PUSH	PSW
A0	ANA	B	CB	- - -		F6	ORI	D8
A1	ANA	C	CC	CZ	Adr	F7	RST	6
A2	ANA	D	CD	CALL	Adr	F8	RM	
A3	ANA	E	CE	ACI	D8	F9	SPHL	
A4	ANA	H	CF	RST	1	FA	JM	Adr
A5	ANA	L	D0	RNC		FB	EI	
A6	ANA	M	D1	POP	D	FC	CM	Adr
A7	ANA	A	D2	JNC	Adr	FD	- - -	
A8	XRA	B	D3	OUT	D8	FE	CPI	D8
A9	XRA	C	D4	CNC	Adr	FF	RST	7
AA	XRA	D	D5	PUSH	D			
AB	XRA	E	D6	SUI	D8			

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

HEX-ASCII TABLE

00	NUL		2B	+		56	V	
01	SOH		2C	'		57	W	
02	STX		2D	–		58	X	
03	ETX		2E	.		59	Y	
04	EOT		2F	/		5A	Z	
05	ENQ		30	0		5B	[	
06	ACK		31	1		5C	\	
07	BEL		32	2		5D	]	
08	BS		33	3		5E	^	(↑)
09	HT		34	4		5F	—	(←)
0A	LF		35	5		60	`	
0B	VT		36	6		61	a	
0C	FF		37	7		62	b	
0D	CR		38	8		63	c	
0E	SO		39	9		64	d	
0F	SI		3A	:		65	e	
10	DLE		3B	;		66	f	
11	DC1	(X-ON)	3C	<		67	g	
12	DC2	(TAPE)	3D	=		68	h	
13	DC3	(X-OFF)	3E	>		69	i	
14	DC4	~~(TAPE)~~	3F	?		6A	j	
15	NAK		40	@		6B	k	
16	SYN		41	A		6C	l	
17	ETB		42	B		6D	m	
18	CAN		43	C		6E	n	
19	EM		44	D		6F	o	
1A	SUB		45	E		70	p	
1B	ESC		46	F		71	q	
1C	FS		47	G		72	r	
1D	GS		48	H		73	s	
1E	RS		49	I		74	t	
1F	US		4A	J		75	u	
20	SP		4B	K		76	v	
21	!		4C	L		77	w	
22	"		4D	M		78	x	
23	#		4E	N		79	y	
24	$		4F	O		7A	z	
25	%		50	P		7B	{	
26	&		51	Q		7C	|	
27	′		52	R		7D	}	(ALT MODE)
28	(		53	S		7E	~	
29	)		54	T		7F	DEL	(RUB OUT)
2A	*		55	U				

Adr = 16 bit address

intel

8080 Assembly Language Reference Card

March 1976

W.Z.

ZOLNEROVICH

98-005B

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Tokyo 101
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JUMP

C3	JMP	Adr
C2	JNZ	
CA	JZ	
D2	JNC	
DA	JC	
E2	JPO	
EA	JPE	
F2	JP	
FA	JM	
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	
CC	CZ	
D4	CNC	
DC	CC	
E4	CPO	
EC	CPE	
F4	CP	
FC	CM	

RETURN

C9	RET
C0	RNZ
C8	RZ
D0	RNC
D8	RC
E0	RPO
E8	RPE
F0	RP
F8	RM

MOVE IMMEDIATE

06	MVI B,	D8
0E	MVI C,	
16	MVI D,	
1E	MVI E,	
26	MVI H,	
2E	MVI L,	
36	MVI M,	
3E	MVI A,	

Acc IMMEDIATE*

C6	ADI	D8
CE	ACI	
D6	SUI	
DE	SBI	
E6	ANI	
EE	XRI	
F6	ORI	
FE	CPI	

LOAD IMMEDIATE

01	LXI B,	D16
11	LXI D,	
21	LXI H,	
31	LXI SP,	

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

* = all Flags (C, Z, S, P, AC) affected

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

SPECIALS

EB	XCHG
27	DAA*
2F	CMA
37	STC†
3F	CMC†

INPUT/OUTPUT

D3	OUT	D8
DB	IN	

ROTATE†

07	RLC
0F	RRC
17	RAL
1F	RAR

CONTROL

00	NOP
76	HLT
F3	DI
FB	EI

MOVE

40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
47	MOV	B,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
4F	MOV	C,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MOV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
57	MOV	D,A

MOVE (cont)

58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
5F	MOV	E,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
67	MOV	H,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
6F	MOV	L,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L
77	MOV	M,A
78	MOV	A,B
79	MOV	A,C
7A	MOV	A,D
7B	MOV	A,E
7C	MOV	A,H
7D	MOV	A,L
7E	MOV	A,M
7F	MOV	A,A

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

† = only CARRY affected

ACCUMULATOR*

80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
87	ADD	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
8F	ADC	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
97	SUB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
9F	SBB	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
A7	ANA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
AF	XRA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
B7	ORA	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
BF	CMP	A

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
SET	D16	
DS	D16	
DB	D8	[ ]
DW	D16	[ ]
IF	D16	
ENDIF		
MACRO		[ ]
ENDM		

CONSTANT DEFINITION

0BDH	Hex
1AH	
105D	Decimal
105	
72O	Octal
72Q	
11011B	Binary
00110B	
'TEST'	ASCII
'A' 'B'	

OPERATORS

(,)

* , / , MOD,SHL,SHR

+,−

NOT

AND

OR,XOR

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

FLAG BYTE STACK FORMAT

7	6	5	4	3	2	1	Ø
S	Z	Ø	AC	Ø	P	1	C

Adr = 16 bit address

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)