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# IBM 3090 Processor Complex Functional Characteristics

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## **Seventh Edition (April 1988)**

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## Preface

This manual is intended for management, programming, and operations personnel; it describes the components, functions, and models of the IBM 3090 Processor Complex.

Readers of this manual should be familiar with IBM System/370 (S/370), IBM System/370 extended architecture (370-XA), and IBM Enterprise Systems Architecture/370™ (ESA/370™) as defined in the *IBM System/370 Principles of Operation*, GA22-7000, the *IBM System/370 Extended Architecture Principles of Operation*, SA22-7085, and the *IBM Enterprise Systems Architecture/370 Principles of Operation* (to be available at a later date).

This manual contains information on the 3090 Processor Complex Models 120E, 150, 150E, 180, 180E, 200, 200E, 280E, 300E, 400, 400E, 500E, and 600E. This manual contains seven chapters, two appendixes, a glossary, and a bibliography.

- Chapter 1, "Introduction" summarizes the model configurations, design highlights, and programming support of the 3090 Processor Complex.
- Chapter 2, "3090 Processor Complex" describes the characteristics of the 3090 Processor Complex.
- Chapter 3, "3090 Processor Unit" describes the logical components of the processor unit.
- Chapter 4, "Consoles and Displays" describes the interactive consoles and displays in the 3090 Processor Complex and, in particular, the facilities provided by the system console.
- Chapter 5, "3092 Processor Controller" describes the processor controller.
- Chapter 6, "Error Handling" describes error recovery procedures that are performed automatically by the processor controller, the customer problem analysis procedures, and the remote support facility procedures.
- Chapter 7, "3090 Features" describes the standard and optional features provided by the 3090 Processor Complex.
- Appendix A, "3090 Architectural Deviations" contains exceptions to the *IBM System/370 Principles of Operation*, the *IBM System/370 Extended Architecture Principles of Operation*, and the *IBM Enterprise Systems Architecture/370 Principles of Operation*.

- **Appendix B, “Summary of 3090 Model Configurations” is a table that shows the 3090 Processor Complex model configurations.**
- **“Glossary of Terms and Abbreviations” defines the technical terms and abbreviations used in this manual.**
- **“Bibliography” lists the manuals that are recommended for use with this manual.**

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## Chapter 1. Introduction

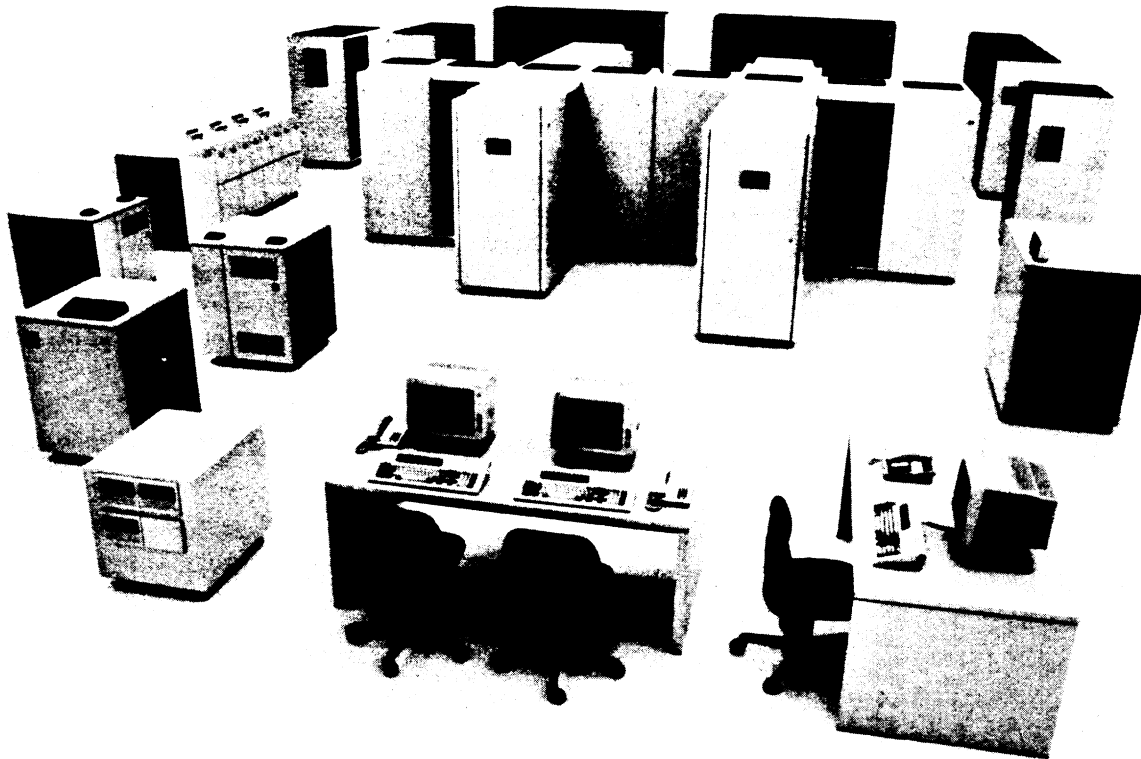
The IBM 3090 Processor Complex is a general-purpose data processing system. The IBM 3090 base models (Models 150, 180, 200, and 400) provide for operation in System/370 (S/370) mode or in System/370 extended architecture mode. The enhanced IBM 3090 Models 120E, 150E, 180E, 200E, 280E, 300E, 400E, 500E, and 600E are the most recent models of the IBM 3090 Processor Complex and can operate in S/370 mode or in Enterprise Systems Architecture/370 (ESA/370) mode. These systems provide reliability, performance, and ease of use for commercial, engineering, and scientific applications.

The 3090 is a compatible growth system for the IBM 3081, 3083, and 3084 Processor Complexes.

The enhanced Model 150E corresponds to the base Model 150, the enhanced Model 180E corresponds to the base Model 180, the enhanced Model 200E corresponds to the base Model 200, and the enhanced Model 400E corresponds to the base Model 400. Upgrade progression for the models is shown in the following table:

Model	Upgrade Progression
120E	150E
150	180 or 180E
150E	180E
180	200 or 200E or 280E
180E	200E or 280E
200	300E or 400 or 400E
200E	300E or 400E
280E	400E
300E	400E or 500E or 600E
400	600E
400E	500E or 600E
500E	600E

Figure 1-1 on page 1-2 shows a view of a 3090 Processor Complex Model 400.



**Figure 1-1. IBM 3090 Processor Complex Model 400 with Other Devices**

## Summary of 3090 Model Configurations

- The **3090 Model 120E** is a uniprocessor; it contains one central processor (CP). The CP has access to central storage, expanded storage, and channels. The 3090 Model 120E provides:
  - One CP
  - A vector facility feature (optional) for the CP
  - 32M bytes of central storage
  - Expanded storage (optional):
    - 64M bytes
    - 128M bytes
  - 16 or 24 integrated channels (16 are standard)
  - Logically partitioned operation (optional) with as many as four logical partitions
  
- The **3090 Model 150** is a uniprocessor; it contains one CP. The CP has access to central storage and channels. The 3090 Model 150 provides:
  - One CP
  - A vector facility feature (optional) for the CP
  - 32M or 64M bytes of central storage
  - 16 or 24 integrated channels (16 are standard)

- The **3090 Model 150E** is a uniprocessor; it contains one CP. The CP has access to central storage, expanded storage, and channels. The 3090 Model 150E provides:
  - One CP
  - A vector facility feature (optional) for the CP
  - 32M or 64M bytes of central storage
  - Expanded storage (optional):
    - 64M bytes
    - 128M bytes
  - 16 or 24 integrated channels (16 are standard)
  - Logically partitioned operation (optional) with as many as four logical partitions
  
- The **3090 Model 180** is a uniprocessor; it contains one CP. The CP has access to central storage, expanded storage, and channels. The 3090 Model 180 provides:
  - One CP
  - A vector facility feature (optional) for the CP
  - 32M or 64M bytes of central storage
  - Expanded storage (optional):
    - 64M bytes
    - 128M bytes
    - 192M bytes
    - 256M bytes
  - 16, 24, or 32 integrated channels (16 are standard)
  
- The **3090 Model 180E** is a uniprocessor; it contains one CP. The CP has access to central storage, expanded storage, and channels. The 3090 Model 180E provides:
  - One CP
  - A vector facility feature (optional) for the CP
  - 32M or 64M bytes of central storage
  - Expanded storage (optional):
    - 64M bytes
    - 128M bytes
    - 192M bytes
    - 256M bytes
  - 16, 24, or 32 integrated channels (16 are standard)
  - Logically partitioned operation (optional) with as many as four logical partitions
  
- The **3090 Model 200** is a two-way (dyadic) processor; it contains two integrated CPs, each having access to a common central storage, expanded storage, and channels. The 3090 Model 200 provides:
  - Two integrated CPs
  - A vector facility feature (optional) for each CP
  - 64M bytes of shared central storage
  - Shared expanded storage (optional):
    - 64M bytes
    - 128M bytes
    - 192M bytes

- 256M bytes
  - 32, 40, or 48 integrated channels (32 are standard)
- The **3090 Model 200E** is a two-way (dyadic) processor; it contains two integrated CPs, each having access to a common central storage, expanded storage, and channels. The 3090 Model 200E provides:
  - Two integrated CPs
  - A vector facility feature (optional) for each CP
  - 64M or 128M bytes of shared central storage
  - Shared expanded storage (optional):
    - 64M bytes
    - 128M bytes
    - 192M bytes
    - 256M bytes
    - 512M bytes
    - 1024M bytes
  - 32, 40, 48, or 64 integrated channels (32 are standard)
- The **3090 Model 280E** is a two-way processor; it contains two integrated CPs, each having access to a common central storage, expanded storage, and channels for single-image configuration or for physically partitioned configuration. The 3090 Model 280E provides:
  - Two integrated CPs
  - A vector facility feature (optional) for each CP
  - 64M or 128M bytes of shared central storage
  - Shared expanded storage (optional):
    - 128M bytes
    - 256M bytes
    - 384M bytes
    - 512M bytes
  - 32, 48, or 64 integrated channels (32 are standard)
  - Capability to be operated in a physically partitioned configuration as two uniprocessors similar to two Model 180Es
  - Logically partitioned operation (optional) with as many as four logical partitions (as many as eight when in a physically partitioned configuration)
- The **3090 Model 300E** is a three-way (triadic) processor; it contains three integrated CPs, each having access to a common central storage, expanded storage, and channels. The 3090 Model 300E provides:
  - Three integrated CPs
  - A vector facility feature (optional) for each CP
  - 64M or 128M bytes of shared central storage
  - Shared expanded storage (optional):
    - 64M bytes
    - 128M bytes
    - 192M bytes
    - 256M bytes
    - 512M bytes
    - 1024M bytes
  - 32, 40, 48, or 64 integrated channels (32 are standard)

- Logically partitioned operation (optional) with as many as four logical partitions
- The **3090 Model 400** is a four-way (dual-dyadic) processor; it contains four integrated CPs, each having access to a common central storage, expanded storage, and channels for single-image configuration or for physically partitioned configuration. The 3090 Model 400 provides:
  - Four integrated CPs
  - A vector facility feature (optional) for each CP
  - 128M bytes of shared central storage
  - Shared expanded storage (optional):
    - 128M bytes
    - 256M bytes
    - 384M bytes
    - 512M bytes
  - 64, 80, or 96 integrated channels (64 are standard)
  - Capability to be operated in a physically partitioned configuration as two dyadic processors similar to two Model 200s
- The **3090 Model 400E** is a four-way (dual-dyadic) processor; it contains four integrated CPs, each having access to a common central storage, expanded storage, and channels for single-image configuration or for physically partitioned configuration. The 3090 Model 400E provides:
  - Four integrated CPs
  - A vector facility feature (optional) for each CP
  - 128M or 256M bytes of shared central storage
  - Shared expanded storage (optional):
    - 128M bytes
    - 256M bytes
    - 384M bytes
    - 512M bytes
    - 1024M bytes
    - 2048M bytes
  - 64, 80, 96, or 128 integrated channels (64 are standard)
  - Capability to be operated in a physically partitioned configuration as two dyadic processors similar to two Model 200Es
  - Logically partitioned operation (optional) with as many as four logical partitions (as many as eight when in a physically partitioned configuration)
- The **3090 Model 500E** is a five-way (triadic-dyadic) processor; it contains five integrated CPs, each having access to a common central storage, expanded storage, and channels for single-image configuration or for physically partitioned configuration. The 3090 Model 500E provides:
  - Five integrated CPs
  - A vector facility feature (optional) for each CP
  - 128M or 256M bytes of shared central storage
  - Shared expanded storage (optional):
    - 128M bytes
    - 256M bytes
    - 384M bytes
    - 512M bytes

- 1024M bytes
  - 2048M bytes
  - 64, 80, 96, or 128 integrated channels (64 are standard)
  - Capability to be operated in a physically partitioned configuration as a triadic processor (similar to a Model 300E) and as a dyadic processor (similar to a Model 200E)
  - Logically partitioned operation (optional) with as many as four logical partitions (as many as eight when in a physically partitioned configuration)
- The **3090 Model 600E** is a six-way (dual-triadic) processor; it contains six integrated CPs, each having access to a common central storage, expanded storage, and channels for single-image configuration or for physically partitioned configuration. The 3090 Model 600E provides:
    - Six integrated CPs
    - A vector facility feature (optional) for each CP
    - 128M or 256M bytes of shared central storage
    - Shared expanded storage (optional):
      - 128M bytes
      - 256M bytes
      - 384M bytes
      - 512M bytes
      - 1024M bytes
      - 2048M bytes
    - 64, 80, 96, or 128 integrated channels (64 are standard)
    - Capability to be operated in a physically partitioned configuration as two triadic processors similar to two Model 300Es
    - Logically partitioned operation (optional) with as many as four logical partitions (as many as eight when in a physically partitioned configuration)

## Design Highlights

The 3090 provides high performance and flexibility of use with improved design and technology. The design of the 3090 incorporates:

- High-level performance
- Optional expanded storage (except on the Model 150)
- Improved technology
- Improved reliability, availability, and serviceability
- Choice of architectural modes of operation
- Optional logically partitioned operating mode (except on Models 150, 180, 200, and 400)
- Engineering and scientific capabilities



## ***High-Level Performance***

The 3090 achieves high-level performance by:

- A 17.2-nanosecond (ns) machine cycle time for Models 180E, 200E, 280E, 300E, 400E, 500E, and 600E.
- A 17.75-ns machine cycle time for Model 150E.
- An 18.5-ns machine cycle time for Models 120E, 150, 180, 200, and 400.
- A high-speed 64K-byte buffer in each CP.
- Buffer-to-buffer data paths.
- The use of emitter-coupled logic (ECL) in the thermal conduction modules (TCMs).
- Optional expanded storage (except Model 150) to extend central storage capacity, to reduce paging, and to improve response time for all 3090 models.
- Optional vector facility feature on each CP for improved performance of engineering and scientific applications.

## ***Optional Expanded Storage***

Optional high-speed, high-capacity expanded storage is available as an integrated part of the 3090 Processor Complex. Expanded storage improves system response and system performance balancing. Models 400E, 500E, and 600E offer as much as 2G bytes (2 147 483 648 bytes) of optional storage. Optional expanded storage for the 3090 models is shown in "Optional Machines and Features" on page 2-4.

## ***Improved Technology***

The 3090 uses large-scale integration that permits as many as 132 high-density silicon chips to be mounted on a multilayered ceramic substrate in a helium-filled module called a thermal conduction module (TCM). TCMs plug into a supporting multilayered circuit board. The use of TCMs and the boards significantly reduces requirements for power, space, cabling, and cooling, while enhancing reliability. Performance is improved because the TCMs use a faster-circuit family of emitter-coupled logic (ECL) instead of transistor-to-transistor logic (TTL).

## ***Improved Reliability, Availability, and Serviceability***

The 3090 offers improved reliability, availability, and serviceability (RAS) by providing:

- Additional online error detection and fault isolation techniques

- Deferred maintenance capability
- Enhanced remote support strategy

RAS improvements are implemented by the processor controller, which (except for the Model 120E) contains two integrated processor elements. The dual processor elements provide backup in single-image configuration for critical processor controller functions and for improved 3090 availability.

### ***Choice of Architectural Modes of Operation***

The 3090 base models (Models 150, 180, 200, and 400) can operate either in System/370 (S/370) mode or in System/370 extended architecture (370-XA) mode. The 3090 enhanced models (Models 120E, 150E, 180E, 200E, 280E, 300E, 400E, 500E, and 600E) can operate either in S/370 mode or in Enterprise Systems Architecture/370 (ESA/370) mode. The mode is selected when the 3090 is initialized. In S/370 mode, the 3090 has full compatibility with System/370. In 370-XA mode, the 3090 base models have the advantages of System/370 extended architecture and have problem-program compatibility with System/360, System/370, and 4300 processors. In ESA/370 mode (which includes the functions of 370-XA mode), the 3090 enhanced models can access virtual storage in multiple address spaces and data spaces. This significantly extends addressability for system, subsystem, and application functions that use ESA/370.

#### ***Notes:***

1. The 3090 Model 400 in single-image configuration operates only in 370-XA mode. The 3090 Models 280E and 400E in single-image configuration and the 3090 Models 300E, 500E, and 600E operate only in ESA/370 mode.
2. The 3090 Model 400 in a physically partitioned configuration is similar to two 3090 Model 200s, and each side independently can operate either in S/370 or 370-XA mode. The 3090 Models 280E and 400E in physically partitioned configuration are similar to two 3090 Model 180Es and 200Es, respectively, and each side independently can operate either in S/370 or ESA/370 mode, or be logically partitioned.

S/370 mode provides:

- System/370 extended facility
- 3033 extension
- Extended addressing
- As many as 16 channels for Multiple Virtual Storage/System Product (MVS/SP™) for each channel set or as many as 32 channels for Virtual

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MVS/SP is a trademark of the International Business Machines Corporation.

Machine/System Product High Performance Option (VM/SP HPO) for each channel set

370-XA mode provides:

- 31-bit addressing that provides a capability of a virtual address range of 2G bytes (2 147 483 648 bytes).
- Bimodal addressing that allows programs written with S/370 mode 24-bit addressing to execute and coexist with programs written with 370-XA mode 31-bit addressing.
- Channel path selection and I/O-busy-condition management as hardware functions (rather than system control program functions) that provide:
  - As many as four channel paths available to each I/O device.
  - Increased I/O device accessibility by allowing each central processor to initiate operations with any of the I/O devices and to handle any I/O interruption conditions.
- Support for the Start Interpretive Execution (SIE) instruction, allowing support of guest S/370 or 370-XA virtual machines.

ESA/370 mode provides:

- All of the functions of 370-XA mode
- A significantly extended addressability through access to multiple address spaces and data spaces while maintaining compatibility with existing 24-bit and 31-bit subsystems and user applications. Each address space can contain as many as 2G bytes of programs and data. Each data space can contain as many as 2G bytes of data.
- Support for the SIE instruction, allowing support of guest S/370 or ESA/370 virtual machines. On Models 120E, 150E, 180E, 200E, 280E, 300E, 400E, 500E, and 600E, the benefits of VM assist are provided to an interpretively executed S/370 mode guest virtual machine.

### ***Optional Logically Partitioned Operating Mode***

The optional Processor Resource/Systems Manager™ (PR/SM™) feature offers the capability to enable the event-driven, logical partitioning function of the 3090 Processor Complex. When the PR/SM feature is installed, three modes can be enabled: S/370, ESA/370 (which supports 370-XA and ESA/370 operating systems), and logically partitioned (LPAR) mode. When the logically partitioned mode of operation is chosen, the operator can define the resources that are to be allocated to each logical partition. Most resources can be reconfigured without requiring a power-on reset. After an S/370 or ESA/370 logical partition is defined and

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Processor Resource/Systems Manager and PR/SM are trademarks of the International Business Machines Corporation.

activated, a supporting operating system can be loaded into that logical partition. Central storage and optional expanded storage are defined to logical partitions before partition activation. When a logical partition is activated, the storage resources are allocated in 1M-byte contiguous blocks. These allocations are static upon activation. Sharing of allocated central storage or expanded storage among multiple logical partitions is not allowed.

Individual channel paths may be allocated to each logical partition. A channel path can be allocated only to one logical partition at a time. A device can be shared between logical partitions by using a separate channel path from each logical partition. Channel paths can be dynamically reconfigured between logical partitions.

CPs can be dedicated to a single logical partition or shared among multiple logical partitions. The allocation of CPs to a logical partition is made when the partition is activated. The use of CP resources shared between logical partitions can be modified by operator commands while the logical partitions are active.

An optional vector facility that is installed on a CP is available for use by all partitions that will perform on that CP. CPs that are dedicated to a logical partition (including associated vector facilities) are available only to that logical partition.

## ***Engineering and Scientific Capabilities***

Improved engineering and scientific computational performance in a general-purpose architecture are implemented by:

- Rapid floating-point arithmetic
- Very large storage
- High performance channels
- Improved availability
- A powerful instruction set
- Optional vector facility feature

### ***Vector Facility Feature***

The vector facility feature is optional for each of the central processors of the 3090 Processor Complex; the vector facility feature is available on all 3090 models. Central processors with the optional vector facility feature provide significantly increased levels of performance for many compute-intensive engineering and scientific applications.

## Programming Compatibility

The information in this topic applies to all 3090 models in single-image configuration, independently to each side of a 3090 in physically partitioned configuration, and to operation in a logical partition.

Any program (including its programming support) written for S/370 mode, 370-XA mode, or ESA/370 mode operates on a 3090 operating in that mode, provided that the program:

- Is not time dependent.
- Does not depend on the presence of system facilities (such as storage capacity, I/O equipment, or optional features) when the facilities are not included in the configuration.
- Does not depend on the absence of system facilities when the facilities are included in the configuration.
- Does not depend on results or functions that are defined in the appropriate *Principles of Operation* manual (see "Bibliography" on page X-7) as being unpredictable or model dependent.
- Does not depend on results or functions that are defined in this manual (or, for logically partitioned operation, in the *3090 Processor Complex: Processor Resource/Systems Manager Planning Guide*) as being differences or deviations from the appropriate *Principles of Operation* manual.
- Does not depend (for programs written for 370-XA mode) on the contents of instruction parameter fields B and C on interception of the SIE instruction. See *IBM System/370 Extended Architecture Interpretive Execution* for additional information.
- Does not depend (for S/370 mode) on the presence of the 2K-byte page size, or the presence of storage protection keys associated with 2K-byte blocks of storage.

Any program written for 370-XA mode operates in ESA/370 mode, any problem state program written for S/370 operates in ESA/370 mode or 370-XA mode, and any problem state program written for S/360 operates in ESA/370 mode, 370-XA mode, or S/370 mode, provided that the program:

- Observes the limitations in the preceding statements.
- Does not depend on any programming support facilities that are not provided or that have been modified.
- Takes into account other changes made that affect compatibility between modes. These changes are described in the *IBM System/370 Extended Architecture Principles of Operation*, in the *IBM System/370 Principles of Operation*, and in the *IBM Enterprise Systems Architecture/370 Principles of Operation*.

## Programming Support

Control program support is dependent on the mode in which the 3090 Processor Complex is operating. For example, a 3090 operating in 370-XA mode requires a control program for 370-XA mode.

*Note:* The term *basic modes* is used throughout this manual to refer to processor complex modes of operation other than logically partitioned mode. S/370, 370-XA, and ESA/370 are examples of basic modes.

### ***Control Programs for Basic Modes***

Control program support for the 3090 Processor Complex includes:

- S/370 control programs for operation in S/370 mode
  - MVS/SP Version 1 Release 3.5 (expanded storage and vectors are not supported; the maximum number of channels for each channel set is 16 and the maximum central storage supported is 64M bytes)
  - VM/SP High Performance Option Release 4.2 (the maximum central storage supported is 64M bytes)
  - TPF Version 2 Release 3
- 370-XA control programs for operation in ESA/370 mode or 370-XA mode
  - MVS/SP Version 2 Release 1.3 (supports Models 400 and 400E in physically partitioned configuration only; supports only the two-processor side (side 1) of Model 500E in a physically partitioned configuration; and does not support Model 300E or 600E)
  - MVS/SP Version 2 Release 1.7
  - VM/XA Systems Facility Release 1 (does not support vector facilities or Models 300E, 500E, and 600E; Models 280E, 400, and 400E are supported only in physically partitioned configuration)
  - VM/XA Systems Facility Release 2
  - VM/XA System Product (the Processor Resource/Systems Manager feature is a prerequisite for the VM/XA SP Enhancement for Multiple Preferred Guests)
  - TPF Version 2 Release 4
- ESA/370 control programs for operation in ESA/370 mode
  - MVS/SP Version 3

## **Guest Control Programs**

Start Interpretive Execution (SIE) support is provided by VM/XA for the following guest environments, when the 3090 is operating in ESA/370 mode or 370-XA mode:

- **Using VM/XA Systems Facility as host:**
  - MVS/SP Version 1 Release 1 with Release 1 Enhancement
  - MVS/SP Version 1 Release 3
  - MVS/SP Version 2 Release 1
  - VM/SP Release 2.1
  - VM/SP High Performance Option Release 3
  - VM/XA Migration Aid Release 1 (V = V only)
  - VM/XA Systems Facility (V = V only)
  - OS/VS1 Release 7 with Basic Programming Extensions Release 3
  - VSE/Advanced Function Release 3
- **Using VM/XA System Product as host:**
  - MVS/SP Version 1 Release 3.5
  - MVS/SP Version 2 Release 1.3
  - MVS/SP Version 3 (requires VM/XA System Product Release 2 and operation in ESA/370 mode)
  - VM/SP Release 4
  - VM/SP High Performance Option Release 4.2
  - OS/VS1 Release 7 with Basic Programming Extensions Release 4
  - VSE/Advanced Function Version 2
  - VSE/SP Version 2 and Version 3
  - VM/XA Systems Facility (V = V only)
  - VM/XA System Product (V = V only)
  - TPF Version 2 Release 3 (if TPF-specific processor and DASD control unit RPQs are not required; requires VM/XA SP Enhancement for Multiple Preferred Guests)

## ***Control Programs for Logically Partitioned Operation***

- **S/370 control programs for operation in S/370 mode in a logical partition.**

*Note:* When operating in a logical partition, an S/370 mode control program is limited to the use of a single channel set.

- MVS/SP Version 1 Release 3.5
  - VM/SP Release 5
  - VM/SP High Performance Option Release 5
  - VSE/Advanced Function Version 2
  - VSE/SP Version 2 and Version 3
  - TPF Version 2 Release 3 (if TPF-specific processor and DASD control unit RPQs are not required)
- **370-XA control programs for operation in ESA/370 mode in a logical partition:**
    - MVS/SP Version 2 Release 1.3
    - VM/XA System Product Release 2 (for test and development purposes only; V = V guests only)
    - TPF Version 2 Release 4 (if TPF-specific processor and DASD control unit RPQs are not required)
- **ESA/370 control program for operation in ESA/370 mode in a logical partition:**
    - MVS/SP Version 3



## **Chapter 2. 3090 Processor Complex**

The following 3090 characteristics are described in this chapter:

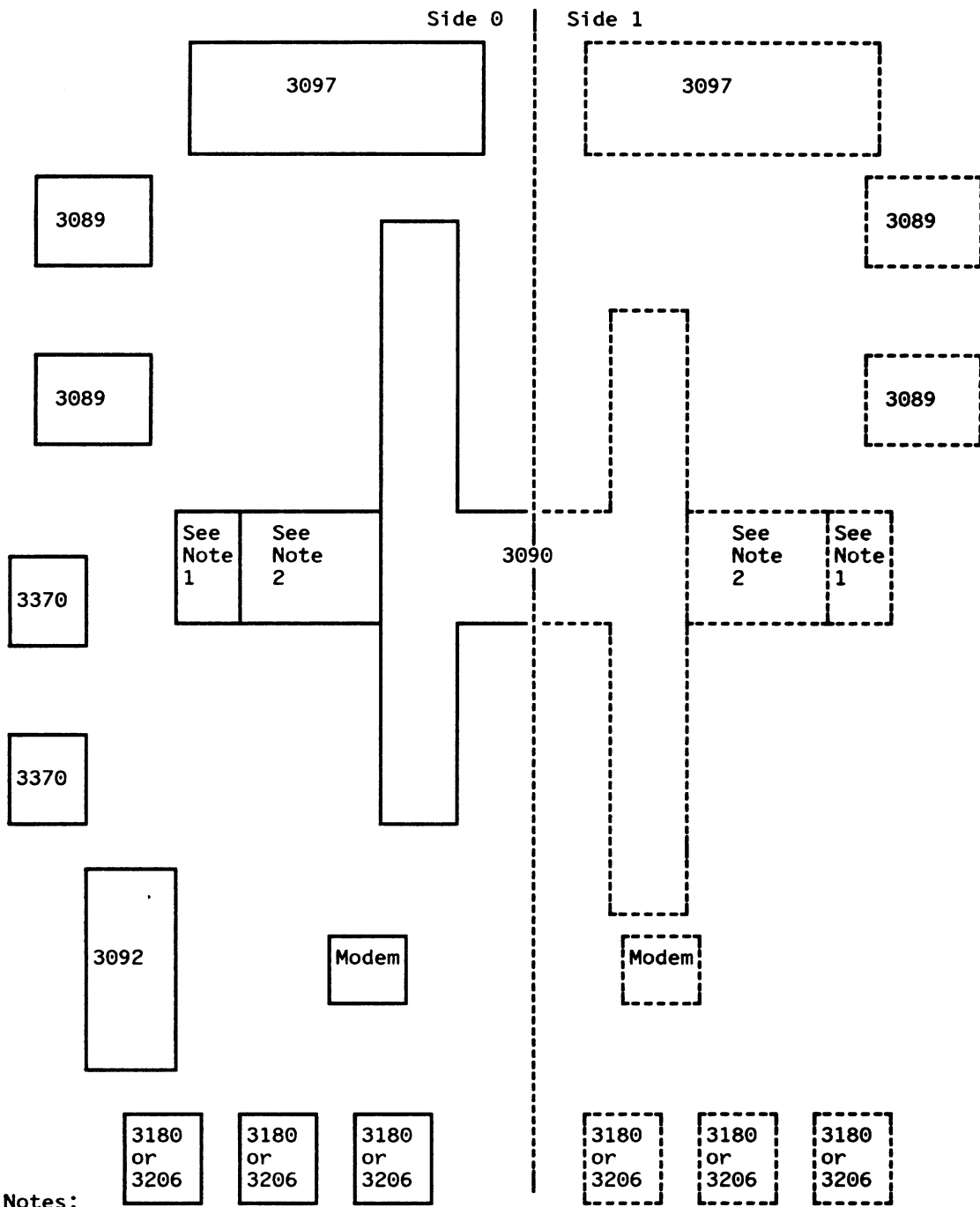
- Processor complex machine requirements
- Optional machines and features
- Console and display configuration
- Power and cooling
- I/O operations
- Storage operations
- Data representation
- System security
- Technology
- Processor controller
- RAS considerations

### **Processor Complex Machine Requirements**

The 3090 Processor Complex machine requirements fall into two categories:

- Standard machine requirements of the 3090 Processor Complex.
- Corequisite machine requirements for the operation and maintenance of the processor complex that are ordered separately.

See Figure 2-1 on page 2-2 for a plan view of 3090 Model 600E.



**Notes:**

1. This frame is present if 64 channels are installed on this side of the 3090.
2. This frame is present if any vector facility feature, or three CPs, or 64 channels are installed on this side of the 3090.
3. This drawing is not to scale.

**Figure 2-1. IBM 3090 Model 600E Plan View**

## ***Standard Machine Requirements***

The standard machine requirements for the 3090 Processor Complex are:

- One IBM 3090 Processor Unit Model 120E, 150, 150E, 180, 180E, 200, 200E, 280E, 300E, 400, 400E, 500E, or 600E.
- One IBM 3092 Processor Controller Model 1, 2, or 3. The 3092 Model 2 is for Models 280E, 400, 400E, 500E, or 600E; the 3092 Model 3 is for the Model 120E; all other 3090 models require the 3092 Model 1.
- One or two IBM 3097 Power and Coolant Distribution Units Model 1 or 2. Two 3097s are required for the 3090 Models 280E, 400, 400E, 500E, or 600E; one is required for the other 3090 models.
- Two or three IBM 3180 Display Stations Model 140 or IBM 3206 Display Stations Model 100. Three display stations are required for the 3090 Model 280E, 400, 400E, 500E, or 600E; two are required for the other 3090 models. See Chapter 4, "Consoles and Displays" on page 4-1 for more information.

## ***Corequisite Machine Requirements***

The corequisite machine requirements for the 3090 Processor Complex are:

- Two IBM 3370 Direct Access Storage Model A2 units (or equivalent), each with a string-switch feature, except for the 3090 Model 120E that requires one 3370 Direct Access Storage Model A2 (string-switch feature not required).
- Access to one of the following:
  - A path to one IBM 3803 Tape Control Unit Model 2 (or equivalent). The tape control unit must have an IBM 3420 Magnetic Tape Unit Model 4, 6, or 8 or an equivalent 6250 bit-per-inch tape unit with a maximum data rate of 1.25 megabytes per second. A 3090 Model 280E, 400, 400E, 500E, or 600E requires access to two channel paths to the magnetic tape unit.
  - A path to an IBM 3422 Magnetic Tape Subsystem. A 3090 Model 280E, 400, 400E, 500E, or 600E requires access to two channel paths to the magnetic tape subsystem.
  - A path to an IBM 3480 Magnetic Tape Unit Model B11 or Model B22 (or equivalent). A 3090 Model 280E, 400, 400E, 500E, or 600E requires access to two channel paths to the magnetic tape subsystem.
- One or two IBM 3864 Modems Model 2 (or equivalent) with an automatic calling unit feature. The 3090 Models 280E, 400, 400E, 500E, and 600E require two modems; all other 3090 models require one modem.

- One to four IBM 3089 Power Units Model 3 (or other 400-Hz power source):
  - 3090 Models 120E, 150, and 150E: one 3089 Power Unit is required.
  - 3090 Models 180 and 180E: two 3089 Power Units are required if the processor complex has both a vector facility feature and more than 128M bytes of expanded storage; otherwise, one 3089 Power Unit is required.
  - 3090 Models 200, 200E, and 300E: two 3089 Power Units are required.
  - 3090 Model 280E: four 3089 Power Units are required if the processor complex has two vector facility features and more than 256M bytes of expanded storage; three 3089 Power Units are required if the processor complex has one vector facility feature and more than 256M bytes of expanded storage; otherwise, two 3089 Power Units are required.
  - 3090 Models 400, 400E, 500E, and 600E: four 3089 Power Units are required.
  
- One or two channel-attached operator display stations for communication with the control program. Two display stations are required for 3090 Models 280E, 400, 400E, 500E, and 600E in physically partitioned configuration and one for all other models. See Chapter 4, “Consoles and Displays” on page 4-1 for more information.

### ***Optional Machines and Features***

Optional features for expanding the size, function, or performance of the system are ordered separately and are added to the processor complex at the customer's request.

Optional machines and features that may be included are shown in Figure 2-2.

To augment the standard machine requirement of two or three display stations, as many as three additional 3180 Display Stations Model 140 or 3206 Display Stations Model 100 may be attached to all 3090 models, except the 3090 Model 120E to which one additional display station may be attached. The 3180 Models 140 and 145 and the 3206 Models 100 and 110 can all be used interchangeably.

Optional Machines and Features	Model												
	120E	150	150E	180	180E	200	200E	280E	300E	400	400E	500E	600E
<b>Vector Facility:</b>													
VE0	-	-	-	-	-	-	-	-	Opt	-	-	Opt	Opt
VE1	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
VE2	-	-	-	-	-	Opt	Opt	-	Opt	Opt	Opt	Opt	Opt
VE3	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt
VE4	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	Opt
VE5	-	-	-	-	-	-	-	-	-	-	-	-	Opt
<b>Central Storage:</b>													
32M bytes	Std	Std	Std	Std	Std	-	-	-	-	-	-	-	-
64M bytes	-	Opt	Opt	Opt	Opt	Std	Std	-	Std	-	-	-	-
64M bytes (32M bytes/side)	-	-	-	-	-	-	-	Std	-	-	-	-	-
128M bytes	-	-	-	-	-	-	Opt	-	Opt	-	-	-	-
128M bytes (64M bytes/side)	-	-	-	-	-	-	-	Opt	-	Std	Std	Std	Std
256M bytes (128M bytes/side)	-	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt
<b>Expanded Storage:</b>													
64M bytes	Opt	Opt	Opt	Opt	Opt	Opt	Opt	-	Opt	-	-	-	-
128M bytes	Opt	-	Opt	Opt	Opt	Opt	Opt	-	Opt	-	-	-	-
128M bytes (64M bytes/side)	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt
192M bytes	-	-	-	Opt	Opt	Opt	Opt	-	Opt	-	-	-	-
256M bytes	-	-	-	Opt	Opt	Opt	Opt	-	Opt	-	-	-	-
256M bytes (128M bytes/side)	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt
384M bytes (192M bytes/side)	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt
512M bytes	-	-	-	-	-	-	Opt	-	Opt	-	-	-	-
512M bytes (256M bytes/side)	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt
1024M bytes	-	-	-	-	-	-	Opt	-	Opt	-	-	-	-
1024M bytes (512M bytes/side)	-	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt
2048M bytes (1024M bytes/side)	-	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt

**Legend:**

Opt Optional  
Std Standard  
- Not available

**Figure 2-2 (Part 1 of 2). Optional Machines and Features**

Optional Machines and Features	Model												
	120E	150	150E	180	180E	200	200E	280E	300E	400	400E	500E	600E
Processor Resource/Systems Manager Feature:	Opt	-	Opt	-	Opt	-	Opt	Opt	Opt	-	Opt	Opt	Opt
Channels:													
16	Std	Std	Std	Std	Std	-	-	-	-	-	-	-	-
24	Opt	Opt	Opt	Opt	Opt	-	-	-	-	-	-	-	-
32	-	-	-	Opt	Opt	Std	Std	-	Std	-	-	-	-
32 (16/side)	-	-	-	-	-	-	-	Std	-	-	-	-	-
40	-	-	-	-	-	Opt	Opt	-	Opt	-	-	-	-
48	-	-	-	-	-	Opt	Opt	-	Opt	-	-	-	-
48 (24/side)	-	-	-	-	-	-	-	Opt	-	-	-	-	-
64	-	-	-	-	-	-	Opt	-	Opt	-	-	-	-
64 (32/side)	-	-	-	-	-	-	-	Opt	-	Std	Std	Std	Std
80 (40/side)	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	Opt
96 (48/side)	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	Opt
128 (64/side)	-	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt
Printers: IBM 3287 Printer Model 1 or 2, or IBM 4224 Printer Model 201 or 202, or equivalent.													
First Printer	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
Second Printer	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt

**Legend:**

Opt Optional  
Std Standard  
- Not available

**Figure 2-2 (Part 2 of 2). Optional Machines and Features**

## Console and Display Configuration

A console is a logical device that performs logical functions. A display is a hardware device and is attached to particular ports of the processor controller. See "Standard Machine Requirements" on page 2-3 and "Optional Machines and Features" on page 2-4 for standard and optional consoles available for the 3090. See Chapter 4, "Consoles and Displays" on page 4-1 for more information.

The system and service support displays are controlled by the processor controller and the operator display is channel attached to the 3090 Processor Complex.

Optional displays are used for one or more of the following console functions:

- System console
- Service console
- Program mode console
- System monitor console

- Service monitor console

## **Power and Cooling**

Power and cooling are combined in one unit, the 3097 Power and Coolant Distribution Unit (PCDU) Model 1 or 2.

### ***Power***

The 3097 PCDU Model 1 or 2 distributes the 50-Hz or 60-Hz power and the 400-Hz power to the 3090 Processor Complex.

The 3097 PCDU Model 1 contains an I/O power sequence control. It can power on and off as many as 64 control units. With the optional, additional power sequence control, as many as 128 control units can be powered on and off. The 3097 PCDU Model 2 has reduced floor space requirements and does not include I/O power sequence control.

A Model 280E, 400, 400E, 500E, or 600E with two 3097 PCDUs Model 1 provides I/O power sequence control for 128, 192, or 256 control units.

### ***Cooling***

The cooling system consists of a closed-loop, distilled water circulating system. Most of the heat generated by the 3090 Processor Complex is removed by this cooling system. The coolant is circulated throughout the frames and is returned to the 3097 PCDU for cooling in a heat exchanger, where external connections to customer-supplied chilled water absorb the heat from the cooling system water loop.

The 3097 PCDU maintains a controlled temperature for the densely packed circuits in the 3090 Processor Complex. The 3097 PCDU contains the necessary controls to maintain the correct temperature within the processor complex. The correct temperature is maintained through use of the water system in the 3097, which is a self-contained closed-loop system, and the customer-supplied chilled-water system.

If a cooling problem occurs because of a malfunction in the operating pump, an alternate pump is switched automatically into the coolant circuit for continued operation.

## **Input/Output Operations**

The following information describes 3090 Models 200 and 200E I/O operations. The other 3090 models operate similarly, but the number of central processors and channels differs. For a summary of these differences, see "Summary of 3090 Model Configurations" on page 1-2.

I/O operations are handled by the channel subsystem in the processor complex. All channels can be configured for block multiplex mode of

operation and as many as four channels (eight on the Models 280E, 400, 400E, 500E, and 600E) can be configured for byte multiplex mode of operation. If the PR/SM feature is installed, as many as eight channels (16 on the Models 280E, 400E, 500E, and 600E) can be configured for byte multiplex mode of operation. Any channel not needed for byte multiplex mode of operation can be configured for block multiplex mode of operation.

Failing channels can be removed from the operating configuration. As many as eight control units can be physically attached to a channel, and each channel can address as many as 256 I/O devices. However, for any 3090 model, the total number of devices attached is 4096 minus the number of channels defined by using the I/O Configuration Program (IOCP). The way in which the channel subsystem performs I/O operations differs depending on the mode of operation (S/370, 370-XA, or ESA/370 mode). Models 300E, 500E, and 600E do not support the S/370 mode of operation, except when operating in a logical partition.

### ***S/370 Mode***

In S/370 mode, any channel may be assigned any valid channel address without concern for priority. Logically, channels are organized into two sets (one set for each central processor) with as many as 16 channels allowed in one set for MVS/SP operation and as many as 32 channels allowed in one set for VM/SP HPO operation. Channel-set switching is a standard feature. If one central processor fails, its channel set can be reassigned (under program control) to the other central processor. The other central processor can then use the two channel sets alternately to continue data processing (with some performance degradation).

*Note:* Operation in a logical partition is limited to the use of one channel set.

### ***ESA/370 and 370-XA Modes***

In ESA/370 mode or 370-XA mode, as many as four channel paths are available to any attached I/O device. During any I/O operation, one of the available channel paths to any specific I/O device is selected. Channel path selection is a hardware function rather than a function of the system control program.

At the start of an I/O operation, a central processor signals the channel subsystem (instead of a single channel, as in S/370 mode) that an I/O operation to a given I/O device is needed. An I/O request is posted to a queue; meanwhile, instruction execution in the central processor continues. Channel path management and the queuing of I/O requests eliminate all busy-condition I/O interruptions encountered in S/370-mode operations.



## **Channel-to-Channel Connection**

Channel-to-channel connection between multiple 3090 Processor Complexes is accomplished by using the IBM 3088 Multisystem Channel Communication Unit (MCCU) Model A1, 1, or 2. Channel-to-channel connection between 3090 Processor Complexes and other IBM processors can be accomplished by using the channel-to-channel adapter (CTCA) feature on those processors that offer it or by using the 3088 MCCU.

Both data-streaming and interlock modes are standard on the 3088 MCCU. Data-streaming mode provides for data transfers of as many as 4.5 megabytes per second, independent of cable length. Cable distances of 122 meters (400 feet) between the processor and the 3088 MCCU are supported in both data-streaming and interlock modes.

The 3088 MCCU Model A1 provides two-processor connectivity and as many as 63 logical CTCA links. The 3088 Model A1 can be field upgraded to a 3088 Model 1 or Model 2. The 3088 MCCU Model 1 can interconnect as many as four processor channels and can provide the equivalent function of as many as 126 CTCAs. The 3088 MCCU Model 2 can interconnect as many as eight processor channels and can provide the equivalent function of as many as 252 CTCAs.

## **Storage Operations**

A hierarchical storage structure increases performance and contributes to system reliability. Each central processor contains a 64K-byte high-speed buffer (cache) that handles instruction, operand, and data fetches.

Central storage provides storage capacity for the 3090 Processor Complex as shown in "Summary of 3090 Model Configurations" on page 1-2. Central storage is shared by all central processors. Expanded storage (an optional feature) is available for 3090 models as shown in the table in Appendix B, "Summary of 3090 Model Configurations" on page B-1.

Expanded storage is controlled by the control program and transfers 4K-byte pages to and from central storage. The control program can use expanded storage to reduce the paging and swapping load to channel-attached paging devices in a storage constrained environment and a heavy paging environment.

In ESA/370 mode and 370-XA mode, storage addressing is extended from 24 bits to 31 bits, which represents an address range of 2G bytes (2 147 483 648 bytes). In addition, these modes permit the use of either 24-bit or 31-bit addressing, under program control, and permits existing application programs to run with current control programs.

In ESA/370 mode and 370-XA mode, an additional channel command word (CCW) format is provided to permit direct addressing of storage of more than 16M bytes for I/O operations. With this format, channel programs may also reside in storage of more than 16M bytes.

## **Data Representation**

The basic addressable data unit is an 8-bit byte that may be used as one character, two decimal digits, or 8 binary bits. The 3090 provides the following data representation features:

- Efficient use of storage and effective I/O rates for decimal data
- Variable-length fields
- Broad and flexible code conversion
- Decimal arithmetic
- Fixed-point and floating-point arithmetic
- 32-bit words, 64-bit doublewords, and 128-bit extended words (for floating-point arithmetic)
- Instructions for functions such as translate, edit, convert, move, and compare

## **System Security**

Data integrity features and a two-level system access control contribute to a high level of system security. Customer planning and management are responsible for the implementation and adequacy of the following controls and for the use of the privileged operator controls such as display and alter storage.

### ***Data Integrity***

Data integrity is maintained through:

- Key-controlled storage protection (store and fetch)
- Low-address storage protection
- Storage error checking and correction
- Parity and other internal error checking
- Segment protection (S/370 mode only)
- Page protection (ESA/370 mode and 370-XA mode only)
- Block-multiplexer channel command retry
- Remote support authorization
- Clear reset of registers and main storage

## ***System Access Control***

System access control protects against inadvertent system damage by restricting commands and the use of display frames only to persons at specified authorization levels. System access control is implemented through a hierarchical structure such that a user will have access to functions at a specified level as well as all levels below the specified level. Access levels can be defined for the system console and the service console.

Also, the 3180 and 3206 Display Stations provide the following:

- A security keylock on the display that allows authorized access and that prevents unauthorized access.
- User authorization for remote access (remote support facility) necessitates the matching of a user-assigned access code, as well as enablement of automatic dialing.

## **Technology**

The 3090 Processor Complex uses several logic-circuit technologies. The central processor logic is implemented by using emitter-coupled logic (ECL) in thermal conduction modules (TCMs). However, central storage and the processor controller function are implemented by a mixture of monolithic technologies.

The TCM is a helium-filled, encapsulated module that is covered by a cold plate through which chilled water circulates to absorb heat. The TCM measures 125 by 134 by 35 millimeters (4.9 by 5.3 by 1.4 inches) and contains as many as 132 silicon chips mounted on a multilayered ceramic substrate that produces a package containing tens of thousands of logic circuits. TCMs plug into a multilayered circuit board that provides TCM powering and TCM-to-TCM connections. Each central processor consists of nine TCMs and the associated circuit board. Therefore, the major element of a processor complex is designed so that no external wiring or cabling is required.

## **Processor Controller**

The 3092 Processor Controller is a stand-alone support unit that includes dual processors, except for the 3092 Model 3 used with the 3090 Model 120E that has one processor. One processor is active and the other is backup in the Model 150, 150E, 180, 180E, 200, 200E, or 300E; or in the Model 280E, 400, 400E, 500E, or 600E in single-image configuration. Both processors are active in Models 280E, 400, 400E, 500E, and 600E in physically partitioned configuration. The backup processor monitors the active processor to provide a high level of availability.

All models of the 3092 continuously monitor the 3090 Processor Complex operation through direct communication with each component in the processor complex.

The 3092 initializes the system, distributes microcode to writable control storage at initialization, monitors voltage levels and coolant temperature, and provides the control unit function for the attached display stations.

The 3092 also provides extensive error recording, recovery, and diagnostic support for the processor complex.

**Microcode:** The 3090 microcode is a fundamental component of the 3090 Processor Complex and is copyrighted by IBM. Each 3090 processor is delivered with a set of microcode that is customized to the machine ordered. The microcode enables the 3090 to operate in accordance with its functional specifications, and is provided in accordance with the following procedures.

Customers who order a 3090 Processor Complex that includes two 3370-A2s plant merged with the 3090 Processor Complex will receive the 3090 microcode stored on each of the 3370 Model A2s (or on one 3370-A2 for the Model 120E).

If 3370-A2s are not plant merged with the 3090 Processor Complex, the customer must coordinate their availability with the 3090 for installation. The 3090 microcode is loaded on the 3370-A2s as part of the installation of the 3090.

Model upgrades, feature additions, and system engineering changes needed by the customer may require updated microcode for the 3090. The updated microcode replaces the existing microcode which must be returned to IBM or erased.

Relocation of the 3090 Processor Complex requires that the 3370-A2s containing the microcode will be reinstalled with the 3090 processor at the new location. The microcode may be shipped on the 3370-A2s, when they will be reinstalled with the 3090 processor at its new location. When the 3370-A2s will not be reinstalled with the 3090 processor at its new location, the microcode must be removed from the 3370-A2s and packaged on appropriate media for shipment with the 3090 processor. After the microcode has been removed and placed on the appropriate media, the 3370-A2s must be erased.

## **Reliability, Availability, and Serviceability Considerations**

Reliability, availability, and serviceability (RAS) are improved in the 3090 by the reduction of downtime and by using standard features.

### **Reliability:**

- ECL/TCM technology that provides a low intrinsic failure rate
- A dual processor controller (except for the 3090 Model 120E) that incorporates switchover and initialization of the functional side in single-image configuration
- Dual 3370 Direct Access Storage Model A2 units (except for the 3090 Model 120E) that support switchover in single-image configuration

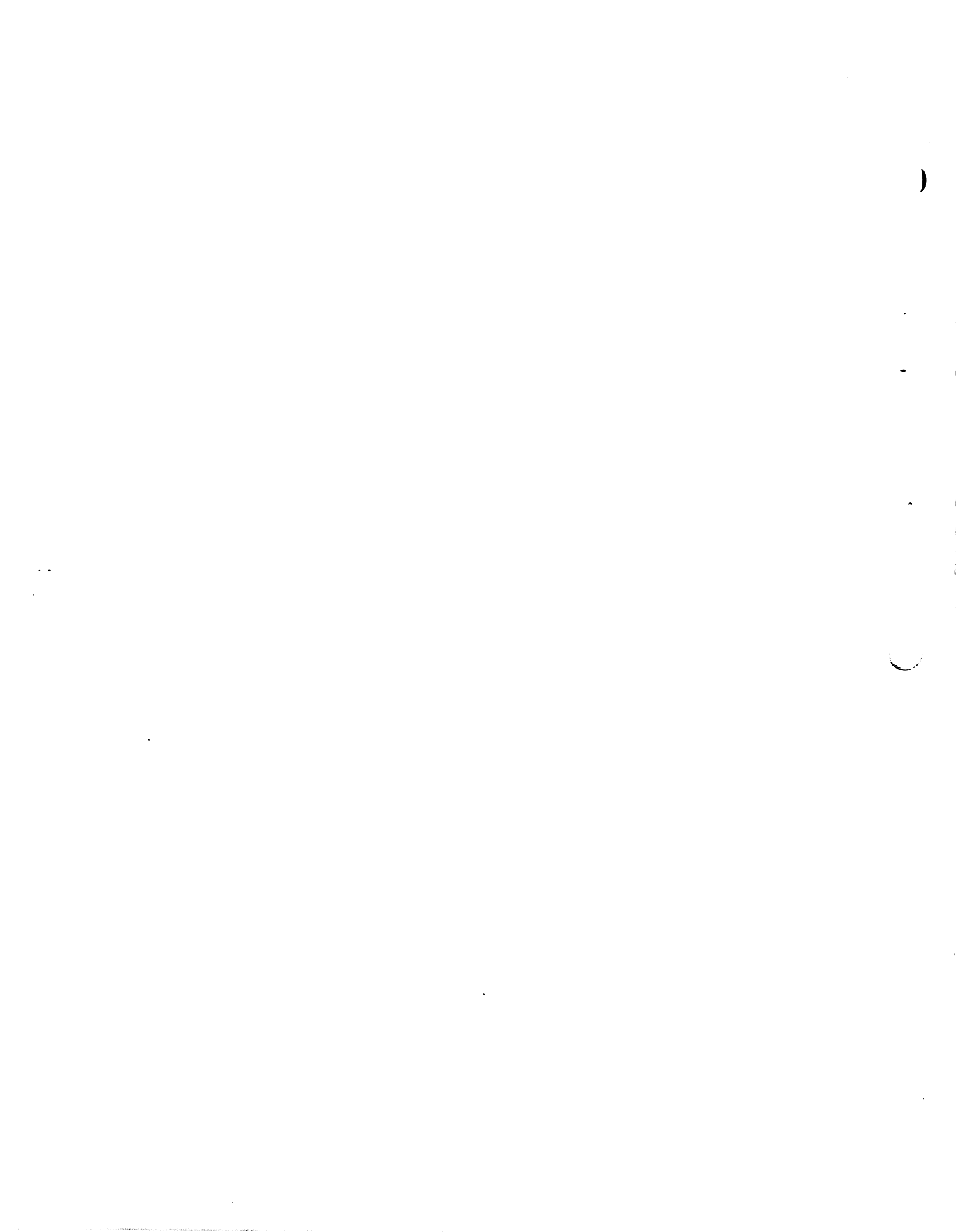
- Multiple consoles for monitoring functional console activity and for backup

**Availability:**

- Two or more central processors available on certain models
- Automatic error detection and correction in both central storage and expanded storage
  - Single-bit error correction and double-bit error detection in central storage
  - Single-bit and double-bit error correction and triple-bit error detection in expanded storage
- Storage deallocation
  - In 2M-byte increments under system program control for Models 120E, 150, 150E, 180, 200, and 400
  - In 4M-byte increments under system program control for Models 180E, 200E, 280E, 300E, 400E, 500E, and 600E
- The ability to vary channels offline in single channel increments
- Customer problem analysis to effect recovery without a service call

**Serviceability:**

- The location of many functional elements on power boundaries
- Automatic fault isolation (analysis routines) concurrent with operation
- Automatic remote support capability
- On-site problem isolation
  - Field-replaceable unit (FRU) isolation
  - Trace tables
  - Error logout recording



## Chapter 3. 3090 Processor Unit

The 3090 Processor Unit consists of logical components (see Figure 3-1 on page 3-2) that execute instructions and commands and that perform storage and channel operations. The 3090 logical components are:

- One or more central processors
- Central storage
- Optional expanded storage (except Model 150)
- One or two channel subsystems
- One or two system control elements

*Note:* For Models 280E, 400, 400E, 500E, and 600E, central storage, expanded storage, and channels are installed symmetrically, as shown in Figure 2-2 on page 2-5.

The vector facility feature is an optional feature that is available for each central processor.

The 3090 Models 120E, 150, 150E, 180, 180E, 200, 200E, and 300E have one processor unit. The central processors, central storage, and the channel subsystem are contained in the processor unit.

The 3090 Models 280E, 400, 400E, 500E, and 600E have one processor unit with two sides (side 0 and side 1). The central processors, processor storage, and the channel subsystems are each associated with either side 0 or side 1. In a single-image configuration, the two sides function as one. In a physically partitioned configuration, the two sides are logically and physically separate.

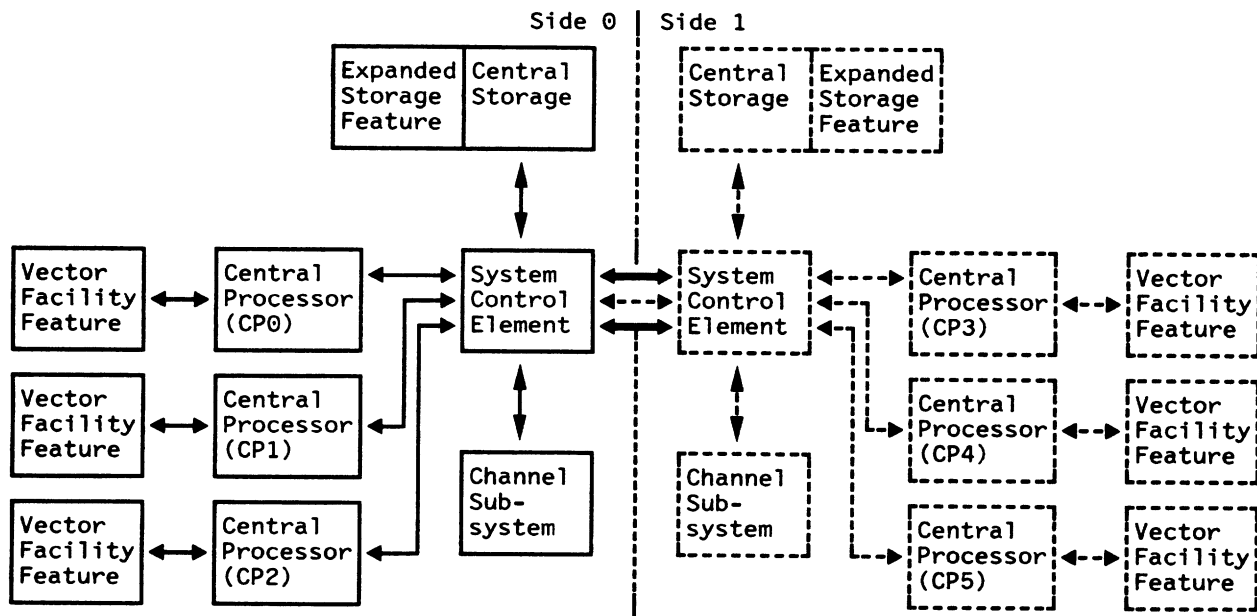


Figure 3-1. IBM 3090 Processor Unit Logical Components (Model 600E)

## CPU ID

A doubleword designated by the second operand address of the Store CPU ID (STIDP) instruction provides information about the 3090 Processor Complex. More information can be found in the *IBM System/370 Principles of Operation*, the *IBM System/370 Extended Architecture Principles of Operation*, and the *IBM Enterprise Systems Architecture/370 Principles of Operation*. A summary of the contents of the doubleword follows:

VV	A	SSSS	3090	0000
----	---	------	------	------

- VV is the version code (two hexadecimal digits):

- 03 (Model 120E)
- 05 (Model 150)
- 06 (Model 150E)
- 09 (Model 280E)
- 10 (Model 180)
- 11 (Model 180E)
- 20 (Model 200)



- 21 (Model 200E)
  - 31 (Model 300E)
  - 40 (Model 400)
  - 41 (Model 400E)
  - 51 (Model 500E)
  - 61 (Model 600E)
- ASSSSS is the central processor (CPU) identification number (six hexadecimal digits):
    - The first digit (A) is the central processor address, as stored by the Store CPU Address (STAP) instruction (see "CPU Address Identification" on page 7-13):

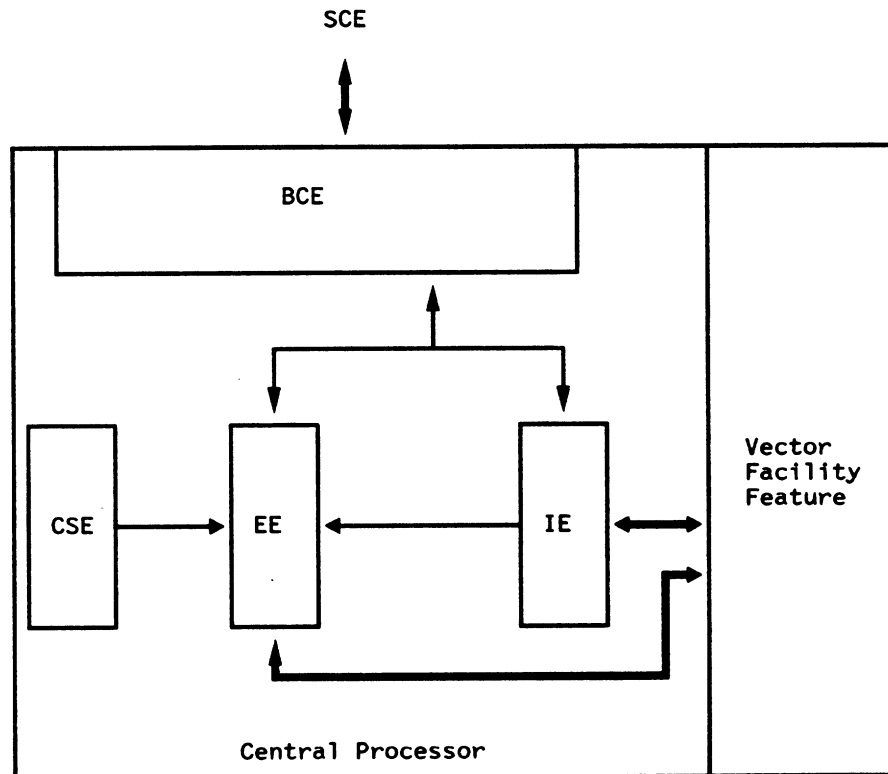
<u>Digit</u>	<u>Model</u>
1	120E
1	150
1	150E
1	180
1	180E
1 or 2	200
1 or 2	200E
1	280E (side 0)
3	280E (side 1)
0 or 1 or 2	300E
1 or 2	400 (side 0)
3 or 4	400 (side 1)
1 or 2	400E (side 0)
3 or 4	400E (side 1)
0 or 1 or 2	500E (side 0)
3 or 4	500E (side 1)
0 or 1 or 2	600E (side 0)
3 or 4 or 5	600E (side 1)

- The next five digits (SSSSS) are selected from the serial number of the 3090 Processor Unit.
- The next four digits are 3090 (for the processor complex).
  - The last four hexadecimal digits are 0000.

*Note:* When the processor complex is operating in a logical partition, the CPU ID presented to that logical partition is not the same as when the processor complex is operating in the S/370 or ESA/370 mode. See the *IBM 3090 Processor Complex: Processor Resource/Systems Manager Planning Guide* for more information.

## Central Processors

Each central processor (Figure 3-2) is microcode controlled and contains an instruction element (IE), execution element (EE), control storage element (CSE), and buffer control element (BCE). The CSE fetches microinstructions that control instruction execution in the IE and EE. The BCE controls the transfer of data between central storage and the central processor containing that BCE. Dynamic address translation is an automatic function of the BCE. Machine cycle times for the 3090 central processors are shown in Appendix B, "Summary of 3090 Model Configurations" on page B-1.



**Legend:**

- BCE Buffer control element
- CSE Control storage element
- EE Execution element
- IE Instruction element
- SCE System control element

**Figure 3-2. Elements of a Central Processor**

## ***Instruction Element***

The instruction element (IE) controls the sequencing of all instructions. The IE performs the following operations:

- Decodes instructions
- Calculates addresses
- Sends fetch requests to the BCE (for instructions and data) in central storage
- Determines fetch priority
- Controls storage requests
- Provides the EE with:
  - Operation codes
  - Operands
  - Operand addresses

The IE can process multiple instructions at the same time by handling the instructions in steps. As one instruction is fetched, decoded, and sent to a queue, the IE begins processing another instruction.

## ***Execution Element***

The execution element (EE) executes instructions set up by the IE and operates in parallel with the IE. The EE performs the following operations:

- Processes instructions
- Processes interruptions
- Overlaps operations with the IE
- Initiates control functions

The EE performs the logical decisions, arithmetic functions, and many control functions of S/370, 370-XA, and ESA/370 architecture instructions. Arithmetic results provided by the EE include the following:

- Fixed point
- Fixed-point multiply
- Convert to binary
- Convert to decimal
- Floating point
- Extended-precision floating point

## ***Control Storage Element***

The control storage element (CSE) is the logical element that controls microcode execution in the central processor and contains the supporting control storages and registers that are used by the central processors. The EE is primarily microcode controlled and the CSE contains the microcode that is used for controlling the EE operation.

## ***Buffer Control Element***

The buffer control element (BCE) handles all central processor references to and from central storage, performs dynamic address translation, and controls the high-speed buffer.

The BCE includes:

- A 64K-byte high-speed buffer
- A buffer directory
- A translation lookaside buffer (TLB)
- Dynamic address translation (DAT) hardware

**The high-speed buffer** provides much faster access to data than if the data were stored in central storage. The high-speed buffer is transparent to programs that are being executed. When data is referred to during instruction execution, the high-speed buffer, the buffer directory, and the TLB are accessed for address comparison.

**The buffer directory** contains the absolute addresses of central storage for data in the high-speed buffer.

**The translation lookaside buffer** stores the real address of the referenced page for a translated virtual address in central storage. Therefore, subsequent translations for the same virtual address are not required because the real address is immediately available in the TLB.

**Dynamic address translation** performs high-speed translation from virtual to real addresses for loading the TLB.

## ***Vector Facility Feature***

The vector facility feature is optional for each central processor of the 3090 Processor Complex and is available on all 3090 models.

Central processors with the optional vector facility feature provide significantly increased levels of performance for many numerically-intensive engineering and scientific applications. The vector facility feature is an extension of the instruction and execution elements of a central processor. Some of the vector facility feature characteristics follow:

- The vector facility feature performs vector arithmetic and logical operations on as many as 128 sets of operands with a single instruction.
- Arithmetic and logical units can produce a 32-bit or 64-bit sum, difference, or product each cycle.
- Compound operations can produce both a product and sum each cycle.

System/370 vector architecture provides:

- Sixty-three instructions with 171 new operation codes (104 operation codes are for floating point)
- Storage vector addressing
- Contiguous, noncontiguous, and indirect element selection
- Compound multiply-and-add instructions
- Vector results placed in vector registers
- Scalar results placed in scalar registers
- Logical, binary, short floating-point, and long floating-point operands

The vector facility feature is supported by:

- MVS/SP Versions 2 and 3, MVS/XA, VM/XA SF, VM/XA SP, and VM/SP HPO including automatic support for asymmetric configurations
- Multitasking facility (MTF) under MVS/SP Versions 2 and 3 for assignment of multiple processors to a job
- VS FORTRAN Version 2 with auto-vectoring capabilities
- APL2 Release 3: no modifications of existing APL2 application programs are required
- Engineering and Scientific Subroutine Library (ESSL): a set of high-performance mathematical routines compatible with the vector facility feature of the 3090 Processor Complex

Additional information on the vector facility feature is available in the *IBM System/370 Vector Operations*.

## Storage

Storage in the 3090 is implemented in monolithic and large-scale-integration technologies. The 3090 has three levels of storage: a high-speed buffer storage in each central processor, central storage, and optional expanded storage (the 3090 Model 150 is not available with expanded storage). The high-speed buffer is described under "Buffer Control Element" on page 3-6.

Also, see "Central Storage" on page 3-8 and "Expanded Storage" on page 3-9 for additional information.

## **Central Storage**

The central storage available for each model is shown in Appendix B, "Summary of 3090 Model Configurations" on page B-1. A hardware system area (HSA) is reserved within central storage for specific system information and cannot be addressed by user programs. The addressable portion of central storage is synonymous with main storage, as described in the *IBM System/370 Principles of Operation*, the *IBM System/370 Extended Architecture Principles of Operation*, and the *IBM Enterprise Systems Architecture/370 Principles of Operation*.

A central storage controller contains the logic for:

- Data storage and retrieval for the processor complex
- Central storage communication with the processor complex (by means of the system control element)
- Communication with and control of the optional expanded storage
- Error checking and correction (ECC)

## **Hardware System Area**

For Models 120E, 150, 150E, 180, 180E, 200, 200E, and 300E, during the initialization of the configuration, the hardware system area (HSA), which is unavailable for program use, selects at least 384K bytes (393 216 bytes) of central storage.

For Models 280E, 400, 400E, 500E, and 600E in physically partitioned configuration, the HSA selects at least 384K bytes of storage for each configuration; in single-image configuration, the HSA selects at least 432K bytes of storage.

The HSA contains copies of microcode, a unit control word (UCW) for each configured I/O device, message buffers, tables, directories, and trace information. The HSA cannot be accessed by conventional (program) storage references.

Depending on the number of UCWs required in the configuration, additional central storage may be required for the HSA. Expansion of the HSA occurs automatically as UCWs are added. HSA expansion for all purposes can be a maximum of 3M bytes (3 145 728 bytes) for each configuration, with the maximum number of devices supported equal to 4096 minus the number of channels defined by the I/O Configuration Program (IOCP).

## **Error Checking and Correction**

Error checking and correction (ECC) code bits are stored with data in central storage. Single-bit errors detected during data transfer are corrected. Certain multiple-bit errors are flagged for follow-on action.

Data paths from the central processors and the channels are checked for parity. Parity bits are included in each command or data word.

## **Frame Deallocation**

A dynamic page deallocation technique, under system program control, temporarily recovers some double-bit failures and allows the operating system to deallocate the failing page frame if the page is not fixed to that page frame. In these instances, the job is not terminated (abended) and processing continues normally. Central storage may be deallocated in 4K-byte increments under system program control. At the option of the customer, maintenance service may be deferred until a predetermined amount of central storage has been deallocated.

## **Key-Controlled Storage Protection**

Key-controlled storage protection provides both store and fetch protection. It prevents the unauthorized access or modification of information in central storage.

Each 4K-byte block of storage is protected by a 7-bit storage key. For processor-initiated store operations, access key bits 0-3 from the currently active program status word (PSW) are compared with bits 0-3 from the storage key associated with the pertinent 4K bytes of storage to be accessed. If the keys do not match, the central processor is notified of a protection violation, the data is not stored, and a program interruption occurs. The same protection is active for fetch operations if bit 4 of the storage key (the fetch protection bit) is on.

## ***Expanded Storage***

Expanded storage is an optional high-speed storage. The expanded storage available for the 3090 models is shown in Figure 2-2 on page 2-5.

Transfers to and from central storage are in 4K-byte pages. Data movement between central storage and expanded storage is controlled by the system control program. No data can be transferred to expanded storage without passing through central storage. Expanded storage reduces the paging and swapping load to channels.

## **Error Checking and Correction**

Error checking and correction (ECC) code bits within expanded storage are used to permit the following:

- Single-bit and double-bit error detection and correction
- Triple-bit error detection

- Some multiple-bit error detection

Unrecoverable errors are flagged.

## Channel Subsystem

Models 120E, 150, 150E, 180, 180E, 200, 200E, and 300E contain one channel subsystem (CSS). Models 280E, 400, 400E, 500E, and 600E contain two channel subsystems (one on each side). In a single-image configuration, the two channel subsystems of these models appear as a single dynamic channel subsystem to the control program.

A CSS consists of one channel control element (CCE) and as many as 64 channels. Each channel interface is controlled by a channel server (CHN), and each group of four CHNs is controlled by a channel element (CHE).

As many as four channels (four channels on each side for Models 280E, 400, 400E, 500E, and 600E) can be configured for byte multiplex mode of operation; all other channels can be configured for block multiplex mode of operation. If the PR/SM feature is installed, as many as eight channels (eight channels on each side for Models 280E, 400E, 500E, and 600E) can be configured for byte multiplex mode of operation.

In byte multiplex mode of operation, channels can be used either in byte multiplex mode or in burst mode. Byte multiplex mode permits the concurrent operation of several relatively slow-speed I/O devices.

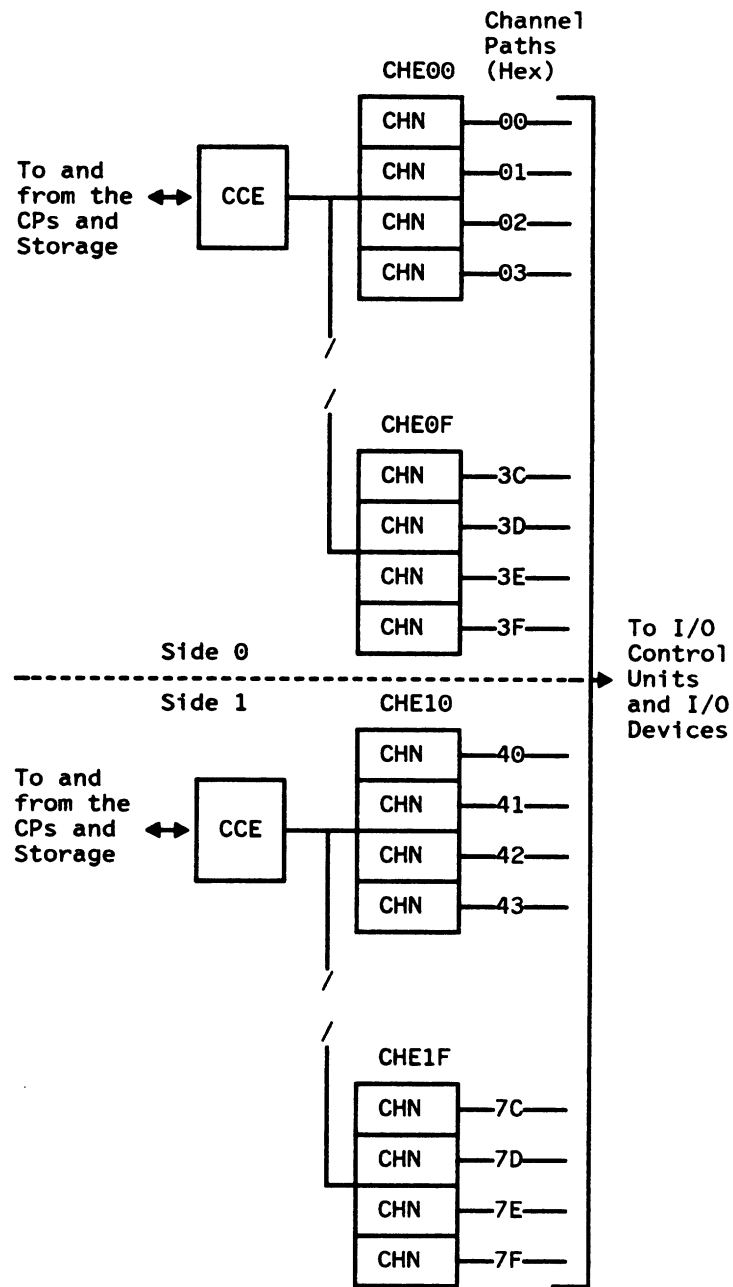
In block multiplex mode of operation, channels can operate either in interlocked (high-speed transfer) mode or in data-streaming mode. Data rates can be as high as 4.5 megabytes per second for data-streaming mode. All channels configured for block multiplex mode of operation may be attached to control units that can operate in high-speed transfer mode or in data-streaming mode.

Figure 3-3 on page 3-11 depicts the channel subsystem of a 3090 Model 600E maximum configuration.

The CSS handles all I/O operations for the central processors. The CSS controls communication between a configured channel and the control unit and device. The channel, control unit, and device configurations are defined to the channel subsystem by the I/O configuration data set (IOCDS) that is selected at system initialization. The IOCDS is created by the I/O Configuration Program (IOCP) and is stored on the 3370 Direct Access Storage devices that are attached to the processor controller.

At initialization, the IOCDS information is used to build necessary control blocks in the hardware system area (HSA) of central storage.





**Legend:**

- CCE Channel control element
- CHE Channel element
- CHN Channel
- CP Central processor

**Figure 3-3. Channel Subsystem for 3090 Model 600E**

## ***Channel Control Element***

The channel control element (CCE) interacts with central storage, the central processors, and the channels to:

- Initiate and end all channel operations
- Provide central storage access control
- Assign priorities for I/O operations

## ***Channels***

The channels control all data flow between the CCE and the control units by using the I/O interface sequences.

## ***System Control Element***

The system control element (SCE) accepts and processes storage requests from the central processors and the channel subsystem. The SCE analyzes each request and performs the following actions:

- Establishes request priority
- Performs cross-interrogation (to ensure that the requester receives the most recent copy of data that is shared)
- Processes requests
- Performs error checking
- Performs error reporting
- Handles request responses

## Chapter 4. Consoles and Displays

This chapter describes the required and optional consoles that support the various 3090 Processor Complex models, and also describes the system console interactive facilities.

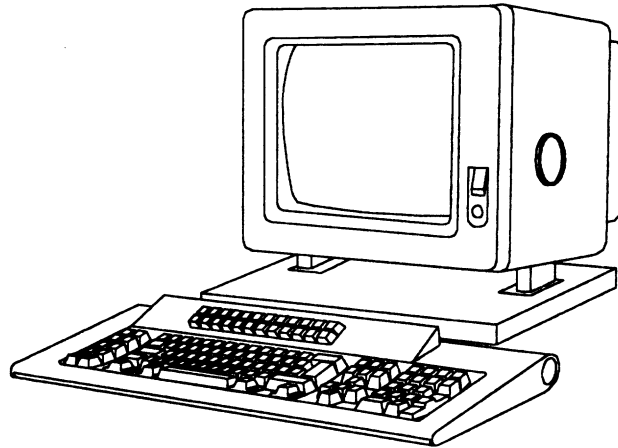
A console is a logical device that performs logical functions by means of a display. A display is an input/output device. The 3090 Processor Complex Models 120E, 150, 150E, 180, 180E, 200, 200E, and 300E require two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100: one as a system display that can be designated as a system console, and one as a service support display that can be designated as a service console. The operating system requires an additional channel-attached display for an operator console.

The 3090 Models 280E, 400, 400E, 500E, and 600E require three 3180 Display Stations Model 140 or three 3206 Display Stations Model 100: two as system displays that can be designated as system consoles and one as a service support display that can be designated as a service console. The operating system requires two additional channel-attached displays for operator consoles for operation in physically partitioned configuration.

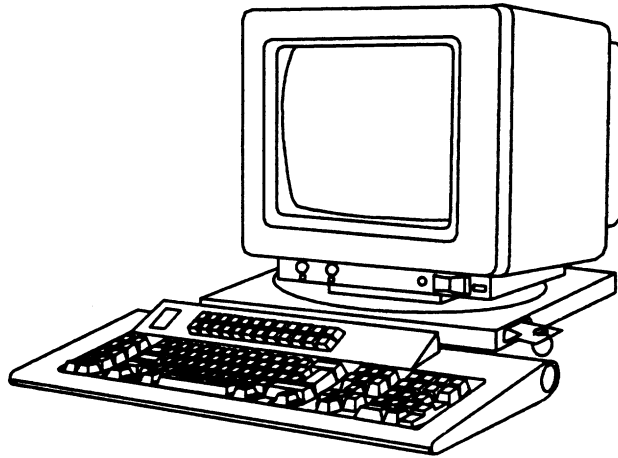
The 3092 Processor Controller Models 1 and 2 support as many as three additional (optional) 3180 Display Stations Model 140 or three 3206 Display Stations Model 100 for the 3090 Processor Complex. The 3092 Model 3 supports one additional (optional) 3180 Model 140 or 3206 Model 100. Each of these displays can be used as a:

- System console
- Service console
- Program mode console
- System monitor console
- Service monitor console

Any display that is attached to a 3092 Model 3, or attached to the active side of a 3092 Model 1 or 2, can be assigned as multiple logical consoles. A Console Assignment frame is provided for assigning selected logical consoles to specified displays. The Swap Cons function key on the display keyboard is used to reassign the logical consoles to a different display. The 3180 Models 140 (Figure 4-1) and 145 and the 3206 Models 100 (Figure 4-2) and 110 are all interchangeable.



**Figure 4-1. IBM 3180 Display Station Model 140**



**Figure 4-2. IBM 3206 Display Station Model 100**

## **System Console Interactive Facilities**

The following functions provide additional user control and flexibility in system operation:

- System definition
- System activity display (SAD)
- I/O configuration data set (IOCDs) content
- I/O problem determination (IOPD) information

## ***System Definition***

A system definition frame provides selections to:

- Supply a unique system name that is displayed on line 24 (system status line) of the screen
- Identify the frame that is to be displayed automatically after a power-on reset
- Enter initial program load (IPL) information (device identification and target central processor) for S/370, 370-XA, and ESA/370 modes of operation for automatic IPL following a power-on reset

## ***System Activity Display***

A maximum of 24 system activity display (SAD) frames can be defined to provide extensive flexibility in the different types of system activity that can be displayed. Frames can be defined to display central processor and channel activity pertinent to certain work shifts or types of jobs. SAD frame definition allows the customer to request that as many as 17 high-usage or low-usage channels or channel paths be dynamically identified and displayed.

A SAD index lists by number all defined SAD frames with their unique names (if specified when defined).

## ***I/O Configuration Data Set Content***

I/O configuration data sets (IOCDSs) are available to provide flexibility to change I/O configurations. A 3090 Model 120E, 150, 150E, 180, 180E, 200, 200E, or 300E has four IOCDSs. A 3090 Model 280E, 400, 400E, 500E, or 600E has four IOCDSs on each side in physically partitioned configuration and eight in single-image configuration.

Two IOCDS frames can be invoked that provide information about specified control units and devices in the I/O configuration that is defined for the IOCDS currently in effect. The two frames provide the following:

- Information about all control units (CUs) that are associated with a specified channel. The displayed information includes CU machine type, attached channel paths, protocol (data-streaming or interlock), and port addresses.
- Information about all devices that are accessible from a specified channel path.

## ***I/O Problem Determination Information***

| Two sets (one set for S/370 mode and one set for 370-XA mode or ESA/370  
| mode) of I/O problem determination (IOPD) frames are available to display  
| I/O status.

| Frames for 370-XA mode or ESA/370 mode include status information about  
| all installed channel paths, specified subchannel content, shared control  
| units, and device configuration.

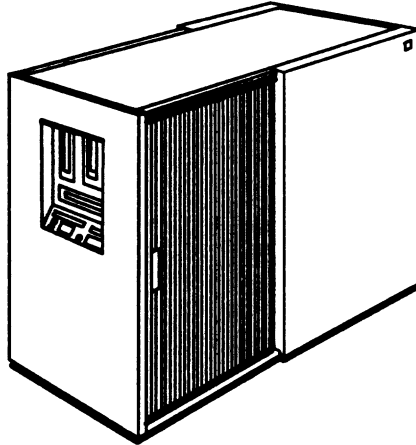
| Frames for S/370 mode include status information about all installed  
| channels by channel set, specified device address control block (DACB)  
| content, and I/O transaction area (IOTA) content.

| IOPD frames provide the user with extensive I/O information and can be  
| useful in identifying I/O problems.

| **Note:** The Model 400 in a single-image configuration does not support the  
| S/370 mode of operation. The Models 300E, 500E, and 600E, and the Models  
| 280E and 400E in a single-image configuration, do not support the S/370  
| mode of operation, except when logically partitioned.

## Chapter 5. 3092 Processor Controller

The 3092 Processor Controller Model 1 (Figure 5-1), Model 2, or Model 3 monitors and controls the status of all physical units within the 3090 Processor Complex.



**Figure 5-1. IBM 3092 Processor Controller Model 1**

The 3092 supports:

- Power on and power off (including I/O units)
- Customer selection of S/370, 370-XA, or ESA/370 mode of operation
- System initialization
- Control of the configuration of hardware elements
- Control unit function for required and optional consoles and optional printers
- Monitoring of power supplies, temperature, and the presence of water flow
- Control and assistance for error recovery
- Automatic analysis of data (analysis routines) for field-replaceable unit (FRU) isolation
- Collection and storage of error data (logout data) for later analysis
- Full processor complex remote support capability
- Problem analysis procedures for the customer
- Collection of information for system activity display (SAD) frames
- Collection of information for I/O problem determination (IOPD) frames

- Collection of status information for customer problem analysis (PA) frames

## Corequisites

The 3092 requires the following corequisites for full processor complex support:

- Two 3370 Direct Access Storage Model A2 units, each with a string-switch feature, except for the 3092 Model 3 that requires one 3370 Direct Access Storage Model A2 unit (string-switch feature not required). For a 3092 Model 1, and for a 3092 Model 2 in a single-image configuration:

- One 3370 is active and contains microcode for initialization, operation, and service
- One 3370 is for backup and is a duplicate of the active 3370

*Note:* For a 3092 Model 2 in a physically partitioned configuration, one 3370 is active for each side. For a 3092 Model 3, one 3370 is required.

- Access to one of the following:
  - A 3803 Tape Control Unit Model 2 (or equivalent) and its associated 3420 Magnetic Tape Unit Model 4, 6, or 8 (or equivalent 6250-bpi tape drive with a maximum data rate of 1.25 megabytes per second).
  - A 3422 Magnetic Tape Subsystem.
  - A 3480 Magnetic Tape Unit Model B11 or Model B22 (or equivalent).

The tape unit is used to install engineering changes and to load the 3370s if required. Valid device addresses for the tape unit are hexadecimal 00-9F and B0-FF.

*Note:* The 3092 Model 2 requires access to two channel paths to the tape unit.

- One 3864 Modem Model 2 with an automatic calling unit feature (or equivalent).
  - The modem is required to communicate with the remote support facility (RSF).
  - If the customer does not authorize automatic remote service, manual dial-up can be used.

*Note:* The 3092 Model 2 requires two 3864 Modems Model 2 (or equivalent).



## System Power Panel

The 3092 contains the System Power control panel that includes switches for power on, power off, and emergency power off; switches for system configuration (if applicable); and indicators for power status and service mode. Figure 5-2 shows a typical System Power panel; however, some panels may differ, depending on the model. For more information, see the *3090 Processor Complex: Operator Controls for the System Console*.

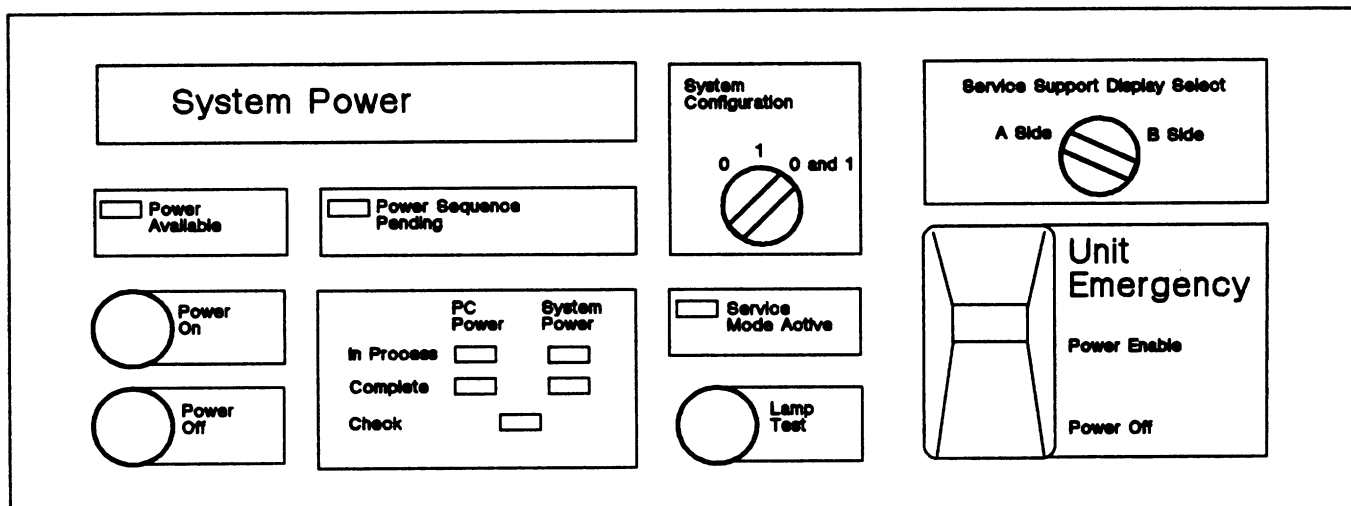


Figure 5-2. 3092 Model 1 or Model 2 System Power Panel

## Dual Support Processors

The 3092 Model 1 contains dual processors (A-side and B-side). The backup processor monitors the active processor to help maintain availability. In most situations, if the active processor fails, a switchover to the backup processor occurs.

When the Power On pushbutton is pressed, both A-side and B-side of the 3092 automatically power on and an IML and IPL occur. The battery-operated clock (BOC) is read and the processor controller time-of-day (TOD) clock is set. Each side communicates its state to the other side to set the active and backup sides. If both sides are functional, the A-side is made active and the B-side is backup. If both sides are functional but the state of the 3370s differ, the side with the most current 3370 is made active. If one side is not functional, the functioning side is made active.

The 3092 Model 2 operates in a similar fashion for a 3090 Processor Complex in a single-image configuration. For a physically partitioned configuration, both sides are active. The A-side of the 3092 controls side 0 of a 3090 Processor Complex in a physically partitioned configuration, and the B-side of the 3092 controls side 1 of a 3090 Processor Complex in a physically partitioned configuration.

The 3092 Model 3 contains a single processor that is always active. One 3370 is attached to the 3092 Model 3.

## **Operation Monitoring and Control**

The 3092 monitors and controls the operations of the 3090 Processor Complex. The 3092 initializes and sequences power to all 3090 components and to all interconnected I/O control units that are under power-sequence control. During initialization of the 3090 Processor Complex, the 3092 validates areas of central storage as error-free data locations, records failing storage locations, and assigns the hardware system area in central storage based on contiguous error-free storage locations. After power sequencing is complete, the processor controller performs an initial microprogram load (IML).

During processing, the 3092 monitors voltage levels and coolant flow. If the coolant flow rate significantly decreases or stops, the second pump in the 3097 is switched into the coolant circuit to avoid thermal shutdown.

## **Error Recovery**

The 3092 logs errors as they occur and then analyzes them for service personnel. Failure symptoms, saved at the time of a malfunction, are analyzed on a time-sharing basis with other processor controller functions; this operation is concurrent with operation of the processor complex.

The 3092 saves the symptoms of these errors, correlates multiple symptoms, performs error analysis, and isolates the failure to the failing FRU or group of FRUs. When automatic error-recovery attempts fail or the error occurs frequently, failure information is displayed on the system console, and an audible alarm is sounded to alert the operator of a problem requiring action. During IML, similar notification to the operator occurs when loss of storage exceeds a threshold that may degrade system performance.

## **Configuration**

The 3092 can be used to initiate configuration changes in:

- Central storage
- Central processors
- Online channels

However, operator-initiated action through the system control program is the preferred method of reconfiguration because it makes both hardware and software changes as a single, integrated action.

## **Remote Support Facility**

The remote support facility (RSF) consists of three parts:

- RSF configuration
- RSF authorization
- RSF call details

### ***RSF Configuration***

At installation, the RSF is tailored to the customer's requirements by the service representative. Two RSF configuration frames are available for the customer and the service organization to specify remote support facility information. These specifications include:

- As many as four telephone numbers for remote support access
- Type of access equipment available (for example, manual dialing, automatic dialing, automatic calling)
- Agreed-on service update schedule
- Allowance or disallowance of incoming and outgoing calls
- Unique RSF customer access code
- Customer and IBM information
  - Responsible customer personnel
  - Location of the system at the customer's installation
  - Customer's business, system console, and modem telephone numbers
  - IBM branch office number and telephone number
  - Prime shift and off-hour shift dispatcher's telephone numbers

The specified information can be changed at any time by invoking the frames and by entering the revised data.

### ***RSF Authorization***

No incoming or outgoing calls are allowed without customer authorization.

Customer authorization includes the following:

- Reason for call
- Type of call: outgoing, incoming, automatic call, manual dialing

- Name of the person at the customer location to be contacted
- Whether a service representative is on-site
- Whether the system is immediately available
- Whether RSF can be enabled, can be deferred, or is not authorized

### ***RSF Call Details***

Details of all RSF calls (both incoming and outgoing) are recorded and each call is listed on an RSF log index. The RSF log index can be displayed and any call that is listed can be selected from the index. The RSF log index shows the date, time, status, and reason for the call. When a call is selected, the first of a set of frames is displayed. The frames contain detailed information about the selected call.

See Chapter 6, "Error Handling" on page 6-1 for information about customer problem analysis and RSF procedures.

## **Chapter 6. Error Handling**

The 3092 Processor Controller automatically performs certain error recovery procedures. If automatic error recovery is not successful, a set of problem analysis frames and procedures is available to facilitate recovery by the user for certain types of failures, and remote support facility (RSF) procedures are available for all failures.

### **Automatic Error Recovery**

Error handling by the processor controller provides both automatic recovery from many hardware malfunctions and provides reporting by machine-check or channel-check interruption.

Error recovery functions are provided for errors in central storage and for channel errors. When an error is detected, the 3092 automatically performs error analysis procedures to isolate the malfunctioning area directly and to identify (if applicable) the field-replaceable unit (FRU) or group of FRUs. These procedures include problem recognition, recording, and diagnosis.

### ***Error Checking and Correction***

Error checking and correction in central storage provides automatic single-bit error detection and correction of all data read from central storage. Error checking also detects all double-bit errors and some multiple-bit errors of the data read from central storage, but does not correct the errors.

Some double-bit errors are temporarily recovered to allow the system control program an opportunity to deallocate the failing page frame.

Error checking and correction in expanded storage provides automatic single-bit and double-bit error detection and correction of all data read from expanded storage. Error checking also detects all triple-bit errors and some multiple-bit errors of the data read from expanded storage, but does not correct the errors.

Parity checking is used to verify other data in the processor complex that is not contained in central or expanded storage.

### ***Machine-Check Handling***

When a machine check occurs, the 3092 collects the error information and enters it in a log. The central processor then presents a machine-check interruption to the system control program.

All machine-check interruptions store a doubleword that contains a machine-check interruption code. Bits that are not assigned or are not implemented are stored as 0's. Certain bits in control register 14 are associated with machine-check handling. The 3090 uses bits 3 through 7 in ESA/370 and 370-XA modes, and bits 4 through 7 in S/370 mode. Model 400 in a single-image configuration does not support the S/370 mode of operation. Models 300E, 500E, and 600E, and Models 280E and 400E in a single-image configuration, do not support the S/370 mode of operation, except when logically partitioned.

When a malfunction makes it undesirable or impossible to continue processing, the central processor enters the check-stop state. The central processor always enters the check-stop state when any of the following occurs:

- PSW bit 13 is 0 and an exigent machine-check condition is generated
- Another exigent machine-check condition is detected during the execution of an interruption that was caused by an exigent machine-check condition
- The machine-check interruption code cannot be stored or the new PSW cannot be fetched during the execution of an interruption
- Invalid ECC is detected in the prefix register

The central processor is removed from the check-stop state by a CPU reset.

*Note:* When multiple central processors are part of the configuration, the processor controller generates a malfunction external interruption to all the configured central processors. If the processor controller cannot identify which central processor should be put into the check-stop state, all central processors are put into the check-stop state.

Figure 6-1 shows the machine-check interruption code (MCIC).

Mode			MCIC	Meaning
S/370	ESA/370 370-XA	Bit		
X	X	0		System damage
X	X	1		Instruction processing damage
X	X	2		System recovery
X	NA	3		Interval timer damage
X	X	4		Timing facility damage
X	NA	5		External damage
X	X	6		Vector facility failure
NA	X	9		Channel report pending
X	X	10		Service-processor damage
NA	X	11		Channel subsystem damage
X	X	13		Vector facility source
X	X	14		Backed up
X	X	16		Storage error uncorrected
X	X	17		Storage error corrected
X	X	18		Storage key error uncorrected
X	X	19		Storage degradation
X	X	20		PSW-EMWP validity
X	X	21		PSW mask and key validity
X	X	22		PSW program mask and condition code validity
X	X	23		PSW instruction address validity
X	X	24		Failing storage address validity
X	NA	26		External damage code validity
X	X	27		Floating-point register validity
X	X	28		General register validity
X	X	29		Control register validity
X	X	31		Storage logical validity
X	X	32		Indirect storage error
X	X	34		Delayed access exception
X	X	46		CPU timer validity
X	X	47		Clock comparator validity

**Legend:**

NA Not active for this mode of operation  
X Active for this mode of operation

**Figure 6-1. Machine-Check Interruption Code (MCIC)**

## I/O Operations

Errors detected by the channel subsystem are reported to the central processors as I/O interruptions or machine-check interruptions. I/O interruptions report the following hardware-related conditions:

- Interface control check (IFCC)
- Channel control check (CCC)
- Channel data check (CDC)

Machine-check interruptions include the following:

- Unrecoverable errors (retry attempts are unsuccessful)
- Persistent errors (retry attempts can be made, but the error threshold is exceeded)

- Serious channel errors that require immediate reporting or that cannot be reported as an IFCC or CCC with an I/O interruption

## **Problem Analysis**

To attempt recovery before initiating the remote support facility, the user can invoke problem analysis from the system console index frame. If the problem was caused by a power malfunction, the first of a set of power status problem analysis frames is displayed. If the problem was caused for some other reason, the first of a second set of problem analysis frames is displayed.

### ***Power Malfunction***

To assist recovery from a power malfunction, the first set of problem analysis frames displays this information:

- Power boundary errors with reason codes
- A list of suggested recovery actions
- Defined service action

For more information, see the *3090 Processor Complex: Operator Controls for the System Console*.

### ***Other Malfunctions***

Status information is displayed for the central processors, hardware, interface control checks, and channels or channel paths. Based on the status information, the customer can select any of a variety of problem analysis categories that include:

- Non-I/O hardware errors
- Unsuccessful IPL
- Enabled or disabled wait state
- Interface control checks (IFCCs)
- I/O device errors
- Operator console lockout

Each procedure provided by the problem analysis frames gives current status information for that type of malfunction, and then lists possible recovery actions. The IOPD frames may also be used for troubleshooting IFCC and I/O device problems. If the attempt at recovery fails and if remote support is required, a selection from the frame invokes the RSF authorization frame.



## **Remote Support Facility**

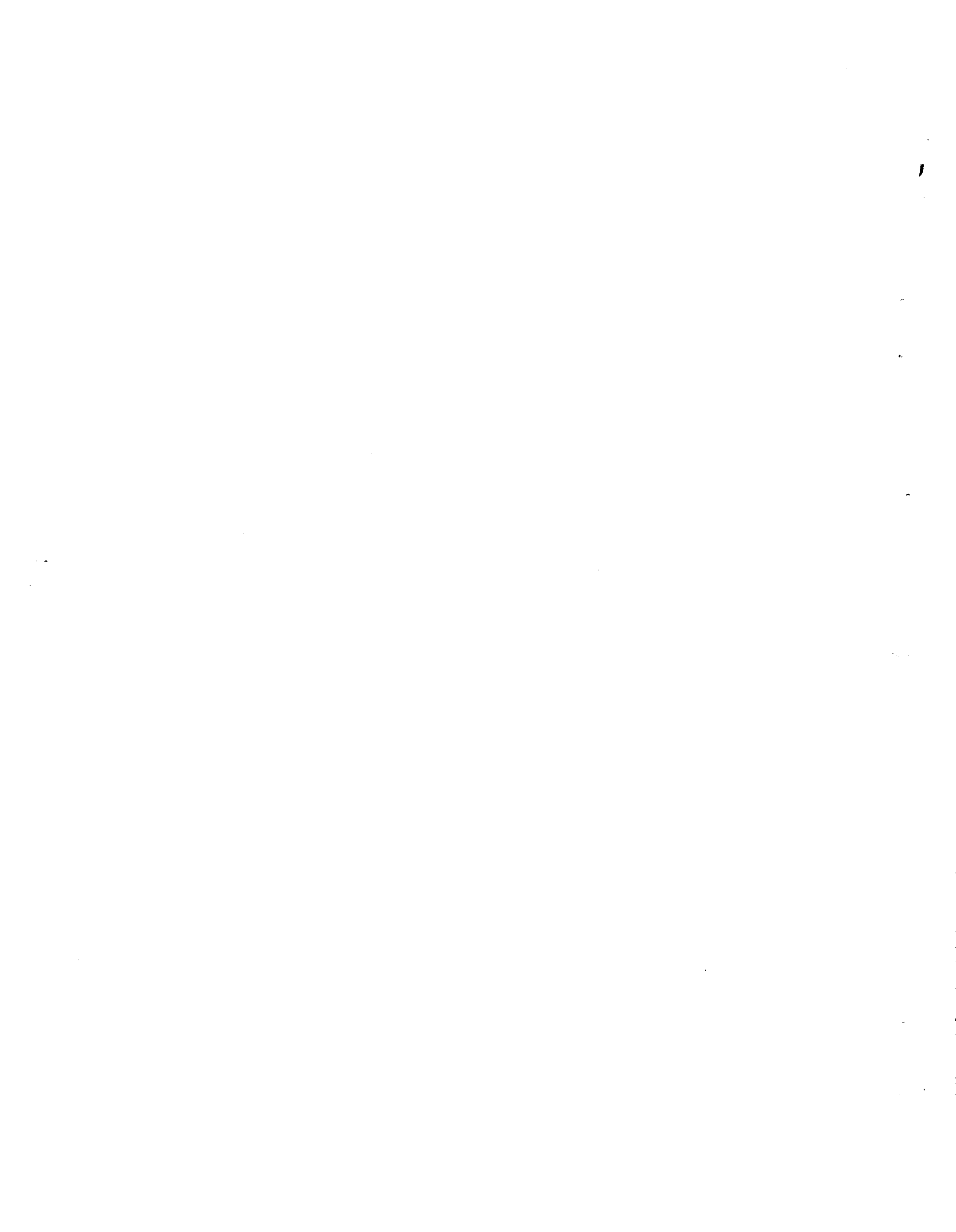
A priority message is displayed when:

- The processor controller detects a failure that requires service
- The remote support facility requires remote console control (from the remote support center)
- An automatic service update must be done

A customer can also initiate remote support from the problem analysis procedures or can invoke the RSF authorization frame and establish the remote connection.

After the service request is authorized, a telephone number is automatically dialed over the public switched network to establish a connection with a remote modem. The remote modem acknowledges the connection and the remote support facility is enabled.

When the remote support facility is connected by the data link, the remote support facility has access to the 3090. Control of the 3090 system can be passed to the remote support facility, and the 3090 Processor Complex can be manipulated by remote control.



## Chapter 7. 3090 Features

The 3090 features are listed under the following topics:

- “Features Dependent on Architectural Mode”

Additional information about the mode-dependent features can be found in the following manuals:

- *IBM System/370 Principles of Operation*, GA22-7000
- *IBM System/370 Extended Architecture Principles of Operation*, SA22-7085
- *IBM System/370 Extended Architecture Interpretive Execution*, SA22-7095
- *IBM System/370 Vector Operations*, SA22-7125
- *IBM Enterprise Systems Architecture/370 Principles of Operation* (to be available at a later date)

- “Programming Assists Dependent on Architectural Mode”

- “Features Not Dependent on Architectural Mode”

The brief descriptions of features in this chapter include an indication of whether the function is a standard or host-program feature of that mode on the 3090.

The column headings in the tables under “Features Dependent on Architectural Mode” and “Programming Assists Dependent on Architectural Mode” identify the architectural modes of the 3090 Processor Complex.

In both tables, the first three columns under 370-XA or ESA/370 Mode, apply when the 3090 Processor Complex (or a side of a physically partitioned 3090 Processor Complex, or a logical partition) has been initialized to operate in the 370-XA or ESA/370 architectural mode. These columns apply to all models of the 3090 Processor Complex. All 3090 base models can operate in 370-XA mode. All 3090 enhanced models can operate in ESA/370 mode.

- The first column, 370-XA or ESA/370, describes the features of the 3090 that are apparent to the control program (host). MVS/SP Version 2 and VM/XA SP are two typical control programs that may be used.
- The second column, 370-XA or ESA/370 Guest, describes the features of the 3090 that are apparent to a 370-XA or ESA/370 mode virtual machine, whose operation is initiated by means of a Start Interpretive Execution (SIE) instruction executed by the host.

- The third column, S/370 Guest, describes the features of the 3090 that are apparent to an S/370 mode virtual machine, whose operation is initiated by means of a Start Interpretive Execution (SIE) instruction executed by the host.

In both tables, the fourth column, S/370 Mode, applies when the 3090 Processor Complex (or a side of a physically partitioned 3090 Processor Complex, or a logical partition) has been initialized to operate in the S/370 architectural mode. This column does not apply to a 3090 Model 400 in a single-image configuration. (For 3090 Models 300E, 500E, and 600E, and the 3090 Models 280E and 400E in a single-image configuration, this column applies only to operation in a logical partition). MVS/SP Version 1 and VM/SP HPO are two typical control programs that may be used. Some S/370 mode control programs support the operation of virtual machines; the features of the 3090 that are apparent to those virtual machines are described in the publications associated with that control program and are not listed here.

## Features Dependent on Architectural Mode

Feature	370-XA or ESA/370 Mode			
	370-XA or ESA/370	370-XA or ESA/370 Guest	S/370 Guest	S/370 Mode
Basic control (BC) mode	-- (1)	-- (1)	Std	Std
Bimodal addressing	Std	Std	--	--
Branch and save	Std	Std	Std	Std
Byte-oriented operand	Std	Std	Std	Std
Channel indirect data addressing	Std	Std	Host	Std
Channel-set switching	-- (2)	-- (2)	Host	Std
Channel subsystem	Std	Std	--	--
Clear I/O	-- (2)	-- (2)	Host	Std
Command retry	Std	Std	Host	Std
Conditional swapping	Std	Std	Std	Std
CPU timer and clock comparator	Std	Std	Std	Std
Extended-precision divide	Std	Std	--	--
Extended-precision floating point	Std	Std	Std	Std
Extended real addressing (26 bit)	-- (3)	-- (3)	Std	Std
Fast release	-- (2)	-- (2)	Host	Std
Floating point	Std	Std	Std	Std
Halt device	-- (2)	-- (2)	Host	Std
Incorrect-length-indication suppression	Std	Std	--	--
Interpretive execution (SIE)	Std	Host	--	--
Interval timer	--	--	Std	Std
Key-controlled storage protection	Std (4)	Std (4)	Std	Std
Limited channel logout	-- (2)	-- (2)	Host	Std
Monitoring	Std	Std	Std	Std
Multiprocessing:				
- CPU address identification	Std	Std	Host	Std
- CPU signaling and response	Std	Std	Host	Std
- Prefixing	Std	Std	Host	Std
- Shared main storage	Std	Std	Host	Std
- TOD clock synchronization	Std	Host	Host	Std
Page protection	Std	Std	--	--
PSW-key handling	Std	Std	Std	Std
Recovery extensions	--	--	Host	Std
Segment protection	-- (5)	-- (5)	Std	Std
Service signal	Std	Host	Host	Std
Sorting instructions	Std	Std	--	--
Storage key instruction extensions	Std	Std	Std	Std
Storage key instructions (ISK, SSK)	-- (4)	-- (4)	Std	Std
Storage-key 4K-byte block:				
- Single-key 4K-byte blocks	Std	Std	Std	Std (6)
- Storage-key exception control	-- (4)	-- (4)	Std	Std
System/370 extended facility:				
Non-MVS-dependent portion	Std	Std	Std	Std
System/370 I/O instructions	-- (2)	-- (2)	Host	Std
Test block	Std	Std	Std	Std
Time-of-day (TOD) clock	Std	Std	Std	Std
Tracing (ASN, branch, and explicit)	Std	Std	--	--

370-XA or ESA/370 Mode

<u>Feature</u>	<u>370-XA or ESA/370</u>	<u>370-XA or ESA/370 Guest</u>	<u>S/370 Guest</u>	<u>S/370 Mode</u>
<b>Translation:</b>				
- Dynamic address translation:				
- 2K-byte page size	--	--	No	No
- 4K-byte page size	Std	Std	Std	Std
- 64K-byte segment size	--	--	Std	Std
- 1M-byte segment size	Std	Std	Std	Std
- Extended control (EC) mode	-- (1)	-- (1)	Std	Std
- Program-event recording (PER)	Std	Std	Std	Std
- Set-system-mask suppression	Std	Std	Std	Std
- Store status	Std	Std	Std	Std
Vector facility	Opt	Opt	Opt	Opt
<b>3033 extension:</b>				
- Dual-address space (DAS)	Std (7)	Std (7)	Std	Std
- SIOF queuing	-- (2)	-- (2)	Host	Std
- Suspend and resume	-- (2)	-- (2)	Host	Std
31-bit IDAWs	Std	Std	Host	Std
31-bit real addressing	Std	Std	--	--

**Notes:**

-- Not defined in the corresponding Principles of Operation manual for this architectural mode, and not implemented on the 3090.

Host The design of the host software determines whether or not this function is simulated for the guest; direct interpretive execution does not occur.

No Defined in the Principles of Operation manual for this architectural mode, but not implemented on the 3090.

Optional (Opt) Implemented as an optional feature of the 3090 when operating in this architectural mode.

Standard (Std) Implemented as a standard feature of the 3090 when operating in this architectural mode.

- 1 Operation in 370-XA or ESA/370 mode is comparable to operation in EC mode of System/370.
- 2 Replaced by standard functions of the channel subsystem operating in 370-XA or ESA/370 mode; channel program compatibility with System/370 is maintained.
- 3 Replaced by 31-bit real addressing.
- 4 The storage key instruction extensions provide the required function to manage the storage keys in 370-XA or ESA/370 mode; System/370 instructions ISK, RRB, and SSK are not in 370-XA or ESA/370 architecture.
- 5 Replaced by page protection.
- 6 Double-key 4K-byte blocks are not implemented.
- 7 Does not include dual-address space (DAS) tracing; address space number (ASN) tracing provides a comparable function.

## Programming Assists Dependent on Architectural Mode

Programming Assists	370-XA Mode or ESA/370			
	370-XA or ESA/370	370-XA or ESA/370 Guest	S/370 Guest	S/370 Mode
Control-switch assist	-- (1)	-- (1)	--	Std (2)
Preferred machine assist	-- (1)	-- (1)	--	Std (2)
SIE assist	Std (2)	--	--	--
System/370 extended facility				
- MVS-dependent portion:				
- Four lock-handling instructions	Std	Std	Std	Std
- Six tracing instructions	-- (3)	-- (3)	Std	Std
- Fix Page instruction	--	--	Std	Std
- SVC Assist instruction	Std	Std	Std	Std
- Add FRR instruction	Std	Std	Std	Std
- VM assist for MVS/370 assists	-- (1)	-- (1)	Std	Std
Virtual-machine assist	-- (1)	-- (1)	Std (4)	Std (5)
VM assists for CPU timer	-- (1)	-- (1)	--	Std (2)

### Notes:

- Not defined as a programming assist for this architectural mode, and not implemented on the 3090.
- Standard (Std) Implemented as a standard feature of the 3090 when operating in this architectural mode.
- 1 SIE provides an alternate means of supporting execution for one or more guest operating systems.
- 2 Not provided in a logical partition.
- 3 370-XA or ESA/370 tracing provides a comparable function.
- 4 Not provided on 3090 Models 150, 180, 200, and 400. On other models, does not include the shadow-table-validation function.
- 5 When operating in a logical partition, does not include the shadow-table-validation function.

## Features Not Dependent on Architectural Mode

<u>Feature</u>	<u>Optional or Standard</u>	<u>Model</u>
Channel group, 1st additional (8)	Optional	120E, 150, 150E, 180, 180E, 200, 200E, 300E
Channel group, 1st additional (16)	Optional	280E, 400, 400E, 500E, 600E
Channel group, 2nd additional (8)	Optional	180, 180E, 200, 200E, 300E
Channel group, 2nd additional (16)	Optional	280E, 400, 400E, 500E, 600E
Channel group, 3rd additional (16)	Optional	200E, 300E
Channel group, 3rd additional (32)	Optional	400E, 500E, 600E
Channels (16)	Standard	120E, 150, 150E, 180, 180E
Channels (32)	Standard	200, 200E, 280E, 300E
Channels (64)	Standard	400, 400E, 500E, 600E
CPU retry	Standard	All models
Data streaming	Standard	All models
Error checking and correction	Standard	All models
Expanded storage	Optional	All models (except 150)
High-speed buffer storage	Standard	All models
I/O error alert	Standard	All models
I/O power sequence control (for 1st to 64th control unit)	Optional	All models
I/O power sequence control (for 65th to 128th control unit)	Optional	All models
I/O power sequence control (for 129th to 192nd control unit)	Optional	280E, 400, 400E, 500E, 600E
I/O power sequence control (for 193rd to 256th control unit)	Optional	280E, 400, 400E, 500E, 600E
Processor Resource/Systems Manager	Optional	120E, 150E, 180E, 200E, 280E, 300E, 400E, 500E, 600E

## Feature Descriptions

This section describes the features and programming assists of the 3090 Processor Complex. These feature descriptions should be used together with the tables on pages 7-3, 7-5, and 7-6.

### *Basic Control Mode*

Basic control (BC) mode provides a PSW format that is compatible with the PSW format of System/360.



## ***Bimodal Addressing***

Bimodal addressing permits 31-bit logical addressing, yet allows users to continue running System/370 problem programs, which use 24-bit logical addresses.

## ***Branch and Save***

Branch and save provides the Branch and Save instruction (BAS and BASR).

## ***Byte-Oriented Operand***

Byte-oriented operand allows storage operands of most unprivileged instructions to appear on any byte boundary without causing a specification exception and a program interruption. This feature applies to fixed-point, floating-point, and logical operands. It does not apply to instruction addresses, privileged instructions, or channel command words (CCWs).

## ***Channel Indirect Data Addressing***

The addresses contained in channel command words (CCWs) in virtual storage must be translated by the system control program before execution. Channel indirect data addressing allows immediately adjacent areas of virtual storage to be mapped into nonadjacent areas of absolute storage.

## ***Channel-Set Switching***

Channel-set switching permits program-controlled switching of channel sets between two central processors so that if one central processor fails, either channel set may be assigned to the other central processor.

*Note:* When operating in a logical partition, an S/370-mode control program is limited to the use of a single channel set.

## ***Channel Subsystem***

The 370-XA and ESA/370 dynamic channel subsystems queue I/O requests, select from as many as four channel paths to any I/O device, and handle I/O busy conditions. Thirteen 370-XA and ESA/370 I/O instructions are associated with the channel subsystem.

Models 280E, 400, 400E, 500E, and 600E are configured with a channel subsystem on each side. However, when these models are in a single-image configuration, the two channel subsystems operate as one dynamic channel subsystem.

## ***Channels***

All channels can be assigned for block multiplex mode of operation. As many as eight channels in Models 280E, 400, 400E, 500E, and 600E (or four channels in other 3090 models) can be assigned for byte multiplex mode of operation. If the PR/SM feature is installed, as many as 16 channels in Models 280E, 400, 400E, and 500E (or eight channels in other 3090 models) can be assigned for byte multiplex mode of operation. See Appendix B, "Summary of 3090 Model Configurations" on page B-1 for standard and optional channels for each model.

## ***Clear I/O***

Clear I/O provides the clear I/O function in a channel when the privileged Clear I/O (CLRIO) instruction is executed. The clear I/O function causes a channel to discontinue its current I/O operation with an addressed I/O device by storing the status of the operation in the channel status word (CSW) and by making the associated subchannel available.

## ***Command Retry***

Command retry allows a subchannel to retry a command without causing an I/O interruption. The retry is initiated by a control unit.

## ***Conditional Swapping***

Conditional swapping makes available the Compare and Swap (CS) and Compare Double and Swap (CDS) instructions.

## ***Control-Switch Assist***

The control-switch assist enhances the functions of the preferred-machine assist by increasing the speed with which interruptions on central processor (CP) owned channels are presented to a preferred virtual machine, and by allowing a preferred virtual machine to access certain control program DIAGNOSE codes. VM/SP HPO Release 3.2 and later support control-switch assist.

## ***CPU Retry***

CPU retry automatically examines any instruction when an error occurs during the execution of the instruction. CPU retry usually attempts to reexecute the instruction.

## ***CPU Timer and Clock Comparator***

The CPU timer of each central processor is a high-resolution timer that causes an interruption whenever its value is negative. The interruption request is allowed by setting bit 21 in control register 0 and the external mask bit in the PSW.

The CPU timer measures central processor elapsed time and causes an interruption at the end of the period that is specified by the program. The timer is decremented when the central processor is executing instructions and during the wait state, but is not decremented when the central processor is in the stopped state. The program can initiate inspection of the CPU timer by using the Store CPU Timer (STPT) instruction and can set the timer to a specific value by using the Set CPU Timer (SPT) instruction. The contents of the CPU timer are reset to 0 by initial CPU reset.

*Note:* When the time-of-day (TOD) clock is in the stopped state or in the error state, the CPU timer is not decremented.

The clock comparator of each central processor provides for an interruption when the TOD clock reaches a value specified by the program. The interruption is allowed when the central processor sets bit 20 in control register 0 and the external mask bit in the PSW.

The format of the clock comparator is the same as that of the TOD clock. A clock-comparator interruption is an external interruption. The program can initiate inspection of the clock comparator by using the Store Clock Comparator (STCKC) instruction and can set it by using the Set Clock Comparator (SCKC) instruction. The contents of the clock comparator are reset to 0 by an initial CPU reset.

*Note:* When the TOD clock is in the stopped state or in the error state, the clock comparator is not operating.

## ***Data Streaming***

Data streaming is available on all block-multiplexer channels. It permits higher data rates (as many as 4.5 megabytes per second, depending on the control units attached) and longer cable lengths. Data streaming is initiated by the control unit. The channel subsystem permits the intermixed attachment of data-streaming and non-data-streaming devices on the same channel.

## ***Error Checking and Correction***

Data paths between expanded storage (if installed) and central storage, and between central storage and the channels and central processors are checked using either parity or error checking and correction.

Error checking and correction (ECC) code bits are stored with the data in the central storage and in the expanded storage data arrays. ECC codes apply to data stored in and fetched from central storage and expanded

storage; single-bit and multiple-bit error detection are performed in both central storage and expanded storage. Single-bit error correction takes place in central storage while both single-bit and double-bit error correction take place in expanded storage.

### ***Expanded Storage***

Expanded storage is an optional high-speed, high-capacity storage that transfers 4K-byte pages to and from central storage. See "Optional Machines and Features" on page 2-4 for the expanded storage available for the 3090 models.

### ***Extended-Precision Divide***

Extended-precision divide provides the Divide (DXR) instruction for extended-precision floating-point operands.

### ***Extended-Precision Floating Point***

Extended-precision floating point provides seven floating-point instructions that use the extended-precision format (a signed 7-bit characteristic and a 28-digit fraction).

### ***Extended Real Addressing***

Extended real addressing permits the addressing of real storage in excess of 16M bytes. The system control program uses extended real addressing for locating user programs and portions of the system control program in central storage at real addresses to 64M bytes. Extended real addressing does not affect virtual addressability, which may not exceed 16M bytes.

### ***Fast Release***

Fast release provides the start-I/O-fast-release function on a channel when the Start I/O Fast Release (SIOF) instruction is executed. This function provides for early release of the central processor that executes the instruction. Fast release occurs before the device-selection procedure is completed, thereby reducing the central processor delay associated with the operation.

### ***Floating Point***

Floating point provides the floating-point instructions and the floating-point registers. In System/370, floating point combined with the commercial instruction set is sometimes referred to as the System/370 universal instruction set.

## ***Halt Device***

Using the privileged Halt Device (HDV) instruction, the halt-device function signals the addressed I/O device to terminate its current I/O operation.

## ***High-Speed Buffer Storage***

High-speed buffer storage in each central processor satisfies many storage fetch requests, making the effective storage access time much shorter than the actual central storage cycle time. For more information, see "Buffer Control Element" on page 3-6.

## ***Incorrect-Length-Indication-Suppression Facility***

For format-1 channel programs, the incorrect-length-indication-suppression facility provides the incorrect-length-indication mode. The incorrect-length-indication-suppression facility includes the incorrect-length-suppression-mode control, bit 24 of word 1 of the operation request block (ORB).

## ***Interpretive Execution***

The interpretive execution facility is used by VM/XA SF and VM/XA SP and provides hardware support for several areas of virtual machine operation, such as interval timer operation, prefixing, address translation, and privileged instruction handling. This facility provides the Start Interpretive Execution (SIE) instruction (with interception format 2 installed), which is used to dispatch all virtual machines.

## ***Interval Timer***

The interval timer of each central processor provides external interruptions on a program-controlled basis. The value stored at a specified storage location is automatically decremented by 1 in bit position 23 every 3.33 milliseconds. The program receives an external interruption request when the interval timer decrements from 0 to a negative value. (Bit 7 of the PSW and bit 24 of control register 0 must be on.) The range of the interval timer is approximately 15.5 hours.

*Note:* When the TOD clock of a central processor is in the stopped or error state, the interval timer is not operating.

## ***I/O Error Alert***

I/O error alert permits a channel to be alerted when a malfunction affects the ability of a control unit to continue operating.

## ***I/O Power Sequence Control***

The 3097 Model 1 provides I/O power sequence control for any 3090 Processor Complex model; the 3097 Model 2 does not provide power sequence control. One I/O power sequence control on the 3097 Model 1 directs the sequence of power on or off for 64 control units. An option is available to extend the power sequence to 64 additional (128 total) control units.

The 3090 Models 280E, 400, 400E, 500E, and 600E require two 3097 Power and Coolant Distribution Units. If both 3097s are Model 1, power sequence control is available for 128, 192, or 256 control units.

## ***Key-Controlled Storage Protection***

Key-controlled storage protection prevents unauthorized access to information in central storage. Key-controlled storage protection includes both store protection and fetch protection. If store protection is violated, data is not stored into the protected area; if fetch protection is violated, data is not retrieved from the protected area. When a violation is recognized, a program interruption occurs. See "Central Storage" on page 3-8 for more information.

## ***Limited Channel Logout***

Limited channel logout provides 4 bytes of channel status information for model-independent recovery from channel errors.

## ***Monitoring***

Monitoring provides a means of selectively recording designated events in the execution of a program. This facility is implemented by the Monitor Call (MC) instruction.

## ***Processor Resource/Systems Manager***

The Processor Resource/Systems Manager (PR/SM) feature provides additional byte-multiplexer channel capability, enables logical partitioning of the processor complex, and supports the VM/XA System Product Enhancement for Multiple Preferred Guests.

### ***Additional Byte-Multiplexer Channels***

The PR/SM feature provides four additional byte-multiplexer-capable channels for 3090 Models 120E, 150E, 180E, 200E, and 300E, and eight additional byte-multiplexer-capable channels (four on each side) for 3090 Models 280E, 400E, 500E, and 600E.

## **Logical Partitioning**

When the PR/SM feature is installed, the 3090 Processor Complex (or side of a physically partitioned 3090 Processor Complex) can be initialized for logically partitioned operation. See “Optional Logically Partitioned Operating Mode” on page 1-8 for more information.

## **Multiple High Performance Guests**

The PR/SM feature is a prerequisite for support of the VM/XA System Product Enhancement for Multiple Preferred Guests. It allows the support of multiple high-performance guests running concurrent with other virtual machines. In addition to the V=R preferred guest virtual machine, as many as three V=F preferred guests are supported. The PR/SM feature supports devices dedicated to V=R and V=F guests. VMA, under SIE, supports V=R and V=F VM/SP and VM/SP HPO guests.

## ***Multiprocessing***

The multiprocessing feature permits a multiprocessing configuration. Multiprocessing provides CPU address identification, CPU signaling and response, prefixing, shared main storage, and TOD clock synchronization. See Appendix B, “Summary of 3090 Model Configurations” on page B-1 for the number of CPs for each model.

### **CPU Address Identification**

CPU address identification provides an address by which each of the central processors can be identified by the Signal Processor (SIGP) instruction. It also provides new external interruption conditions and the Store CPU Address (STAP) instruction by which the system control program can determine the address of a central processor. See “CPU ID” on page 3-2.

### **CPU Signaling and Response**

CPU signaling and response provides for communication among the central processors. This feature provides the Signal Processor (SIGP) instruction and the mechanism to interpret and to act on several order codes, such as sense, stop, and restart.

### **Prefixing**

For each central processor, prefixing provides a means of assigning real addresses 0 through 4095 to different 4K-byte blocks of central storage. One area of central storage (represented by a single contiguous range of absolute addresses) is assigned to each central processor.

## **Shared Main Storage**

Shared main storage permits all central processors to have access to common main storage locations.

## **TOD Clock Synchronization**

TOD clock synchronization provides a uniform appearance to a clock synchronization program in all 3090 Processor Complexes, allowing the program to be independent of the actual number of TOD clocks and central processors in a configuration. It includes a TOD clock synchronization control bit in control register 0.

## **Page Protection**

Page protection provides protection against improper storing by controlling access to virtual storage by using the page protection bit in each page table entry.

## **Preferred Machine Assist**

Preferred machine assist permits a single MVS/SP virtual-equals-real (V=R) virtual machine operating under VM/SP HPO to operate with a minimum of simulated instruction execution. This allows the MVS/SP virtual machine to achieve near basic performance. With preferred machine assist, any MVS/SP release that supports more than 16M bytes of real storage can use real storage above 16M bytes when MVS/SP is operating as a V=R virtual machine.

## **PSW-Key Handling**

PSW-key handling provides the Set PSW Key from Address (SPKA) and Insert PSW Key (IPK) instructions.

## **Recovery Extensions**

Recovery extensions consist of:

- The clear channel function in a channel, which can be used to perform an I/O system reset in a channel when the Clear Channel (CLRCH) instruction is executed.
- Machine-check extensions, which include a machine-check external damage-code validity bit and provide a detailed indication of the cause of external damage.
- Limited channel logout extensions, which consist of two additional logout bits, to indicate whether the I/O interface is operative and whether the logout is valid.



## ***Segment Protection***

Segment protection provides protection against improper storing by controlling access to virtual storage by using the segment protection bit in each segment-table entry.

## ***Service Signal***

Service signal provides an external interruption that is used by the 3092 Processor Controller to signal information to the system control program.

## ***SIE Assist***

The Start Interpretive Execution (SIE) assist improves the performance of a V = R preferred guest that is running under VM/XA SF or VM/XA SP. Certain I/O instructions and associated I/O interruptions can be handled in the interpretive execution mode for S/370, 370-XA, and ESA/370 guests if they are associated with devices dedicated to the guest.

*Note:* The PR/SM feature provides a similar performance improvement for both V = R and V = F guests when used with the VM/XA SP Enhancement for Multiple Preferred Guests.

## ***Sorting Instructions***

Sorting instructions are used by the IBM Program Product DFSORT (Data Facility Sort), Release 7 and later, running under MVS/SP Versions 2 and 3. The sorting instructions are used when sorting fixed-length records using the block-set sorting technique by the program DFSORT (Release 7 and later).

## ***Storage Key Instruction Extensions***

The storage key instruction extensions provide the Set Storage Key Extended (SSKE), Insert Storage Key Extended (ISKE), and Reset Reference Bit Extended (RRBE) instructions, which provide 31-bit addresses and operate on the storage key associated with each 4K-byte block of storage.

## ***Storage Key Instructions***

The storage key instructions Set Storage Key (SSK) and Insert Storage Key (ISK) allow initialization and inspection of the storage key associated with each block of storage that is available in the configuration.

## ***Storage-Key 4K-Byte Block***

Storage-key 4K-byte block allows a single key to be associated with each 4K-byte block of storage and, in S/370 mode, provides the storage-key exception control bit in control register 0.

## ***System/370 Extended Facility***

The non-MVS-dependent portion of the System/370 extended facility consists of:

- Low-address protection, which improves system integrity by providing special protection for storage (at fixed storage addresses 0 through 511) that is vital to the system control program.
- Invalidate Page Table Entry (IPTE) instruction and the common-segment bit, which increase the efficiency of dynamic address translation.
- Test Protection (TPROT) instruction, which performs tests for potential protection violations without causing program interruptions for protection exceptions.

The MVS-dependent portion of the System/370 extended facility consists of:

- Supervisor Call (SVC) Assist instruction, which improves central processor performance by reducing the time needed to enter MVS supervisory services
- Fix Page instruction, Add FRR (Add Functional Recovery Routine) instruction, six tracing instructions, and four lock-handling instructions, which improve central processor performance

## ***System/370 I/O Instructions***

The I/O instructions used in S/370 mode are:

- Clear Channel (CLRCH)
- Clear I/O (CLRIO)
- Halt Device (HDV)
- Halt I/O (HIO)
- Resume I/O (RIO)
- Start I/O (SIO)
- Start I/O Fast Release (SIOF)
- Store Channel ID (STIDC)
- Test Channel (TCH)
- Test I/O (TIO)

## ***Test Block***

Test block provides the Test Block (TB) instruction for testing the usability of a 4K-byte block of central storage.

## ***Time-of-Day Clock***

The time-of-day (TOD) clock for each central processor provides a consistent measurement of elapsed time that can be used for indicating the time of day. The TOD clock for each central processor is initialized by the Set Clock (SCK) instruction by a central processor.

- Bit 51 increments at 1-microsecond intervals.
- Bits 52-55 are monotonic to ensure 1-microsecond counting in bit 51.
- Bits 61-63 contain the central processor address.

## ***Tracing***

Tracing provides three aids for problem-program analysis:

- Address-space-number (ASN) tracing
- Branch tracing
- Explicit tracing

## ***Translation***

Translation includes the following features:

- Dynamic address translation
- Extended control (EC) mode
- Program-event recording (PER)
- Set-system-mask suppression
- Store status

As part of these features, translation also provides the following instructions:

- Load Read Address (LRA)
- Purge Translation Lookaside Buffer (PTLB)
- Reset Reference Bit (RRB)
- Store Then AND System Mask (STNSM)

- Store Then OR System Mask (STOSM)

### **Dynamic Address Translation**

Dynamic address translation (DAT) provides hardware translation of virtual addresses to real addresses during program execution. DAT supports real storage sizes according to the amount of storage available for each 3090 model. In S/370 mode, DAT supports as much as 64M bytes of real storage.

The 3090 uses 4K-byte pages and either 64K-byte segments or 1M-byte segments. S/370 mode uses both the 64K-byte and 1M-byte segment sizes; 370-XA and ESA/370 modes use only the 1M-byte segment size. An S/370 guest virtual machine under control of interpretive execution can use both segment sizes.

### **Extended Control Mode**

When the 3090 operates in extended control (EC) mode, virtual storage and high-speed DAT are available.

### **Program-Event Recording**

Program-event recording (PER) aids in debugging programs. During program execution, PER can monitor the following actions:

- Successful branches
- Alteration of general registers
- Instruction fetches from a specified storage area
- Alteration of a specified storage area

### **Set-System-Mask Suppression**

Set-system-mask suppression permits suppression of execution of the Set System Mask (SSM) instruction and provides the special-operation program interruption code.

### **Store Status**

Store status is an operator-initiated function that places the contents of the current PSW and the program-addressable registers in permanently assigned locations within the first 512 bytes of absolute storage. Store status also includes a non-initializing manual reset function.

### **Vector Facility Feature**

The vector facility feature is optional for each central processor in the 3090 Processor Complex. Central processors with the optional vector facility feature provide significantly increased levels of performance for many compute-intensive engineering and scientific applications. The section size is 128 and the partial-sum number is 4. For more information, see "Vector Facility Feature" on page 3-6 and *IBM System/370 Vector Operations*.

## ***Virtual-Machine Assist***

Virtual-machine assist (VMA), which is an assist for VM/SP, directly executes certain privileged virtual-machine instructions and validates page-table entries in the shadow tables. VMA improves performance on virtual-storage system operation under VM/SP by reducing the amount of time VM/SP spends in the real supervisor state. The reduction is achieved by emulation (instead of software simulation) of certain privileged operation codes used by the virtual-storage (guest) control program. Except on the 3090 Models 150, 180, 200, and 400, an interpretively-executed S/370-mode guest virtual machine also can benefit from the advantages offered by VMA.

## ***VM Assists for the CPU Timer***

VM assists for the CPU timer permit a central processor to execute directly the Set CPU Timer (SPT) and Store CPU Timer (STPT) instructions for a virtual machine operating under VM/SP.

## ***3033 Extension***

The 3033 extension provides the following facilities to the 3090:

- Dual-address space
- Start-I/O-fast queuing
- Suspend and resume

All three facilities are supported in S/370 mode by MVS/SP Version 1 Release 3; dual-address space is supported in 370-XA and ESA/370 modes by MVS/SP Version 2, and in ESA/370 mode by MVS/SP Version 3.

### **Dual-Address Space**

Dual-address space aids communication between virtual address spaces. It provides:

- Twelve additional instructions
- Two address spaces for immediate use by a program
- A means of changing to other virtual address spaces
- A table-based subroutine linkage
- The use of multiple access keys for key-controlled protection by problem programs
- Aids for problem-program analysis (S/370 mode only)

In 370-XA and ESA/370 modes, the tracing facility provides an alternative set of aids.

## **Start-I/O-Fast Queuing**

Start-I/O-fast queuing allows a Start I/O Fast Release (SIOF) instruction to complete execution independent of device selection or a channel-busy condition. Control unit or device busy conditions encountered before execution of a SIOF instruction cause the I/O operation to remain pending until facilities are available for initiation of the operation at the device.

## **Suspend and Resume**

Suspend and resume provides:

- The suspend flag in the channel command word (CCW), which indicates that execution of a channel program is to be suspended
- A channel address word (CAW) bit that controls whether the suspend flag of the CCW should cause suspension of execution of a channel program
- A channel status word (CSW) bit that indicates that execution of a channel program has been suspended
- The Resume I/O (RIO) instruction, which causes the execution of a suspended channel program to be resumed

## ***31-Bit Indirect Data Address Word***

The 31-bit indirect data address word (IDAW) extends the size of the address field in IDAWs to 31 bits.

## ***31-Bit Real Addressing***

Thirty-one bit real addressing ensures that certain fields contain 31-bit real addresses regardless of the setting of the addressing-mode control bits in the PSW.

## Appendix A. 3090 Architectural Deviations

The following information describes 3090 architectural deviations from the *IBM System/370 Principles of Operation*, the *IBM System/370 Extended Architecture Principles of Operation*, and the *IBM Enterprise Systems Architecture/370 Principles of Operation*.

### Concurrent Indication of PER Events with Operand-Access Exception

Storage alteration PER events may be indicated by the 3090 for execution of the instructions Edit, Edit and Mark, and Translate, even though an operand-access exception is encountered that nullifies or suppresses instruction execution.

### Protection Violation Instead of Delayed Access Exception

The S/370, 370-XA, and ESA/370 Principles of Operation permit considerable extent of unpredictability when a valid and attached dynamic address translation (DAT) table entry is changed and the entry is used for translation before the translation lookaside buffer (TLB) is cleared of copies of that entry. The definition permits changes to all of those result fields that are not protected. Changes can occur, for example, to the condition code, to operands due to be changed in registers, and to those portions of the operands due to be changed in storage for which no access exception exists.

The 3090 deviates from the architecture in that:

Protection exceptions due to key-controlled protection, page protection, and segment protection that occur after the initial pretest are ignored, the storing for a store-type reference takes place, and no interruption occurs.

### Fetch Protection Ignored

In certain situations when the fetch-protection-override control (bit 6 of control register 0) is 1 during operation in 370-XA or ESA/370 mode, fetch protection is ignored for locations at effective addresses 2048 through 2302.





## Appendix B. Summary of 3090 Model Configurations

Item	Model												
	120E	150	150E	180	180E	200	200E	280E	300E	400	400E	500E	600E
<b>Machine Cycle Time:</b>													
18.5 ns	Std	Std	-	Std	-	Std	-	-	-	Std	-	-	-
17.75 ns	-	-	Std	-	-	-	-	-	-	-	-	-	-
17.2 ns	-	-	-	-	Std	-	Std	Std	Std	-	Std	Std	Std
<b>Central Processor:</b>													
CP0	-	-	-	-	-	-	-	-	Std	-	-	Std	Std
CP1	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std
CP2	-	-	-	-	-	Std	Std	-	Std	Std	Std	Std	Std
CP3	-	-	-	-	-	-	-	Std	-	Std	Std	Std	Std
CP4	-	-	-	-	-	-	-	-	-	Std	Std	Std	Std
CP5	-	-	-	-	-	-	-	-	-	-	-	-	Std
<b>System Control Element:</b>													
SCE0	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std
SCE1	-	-	-	-	-	-	-	Std	-	Std	Std	Std	Std
<b>Channel Subsystem:</b>													
CSS0	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std	Std
CSS1	-	-	-	-	-	-	Std	Std	-	Std	Std	Std	Std
<b>Vector Facility:</b>													
VE0	-	-	-	-	-	-	-	-	Opt	-	-	Opt	Opt
VE1	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
VE2	-	-	-	-	-	Opt	Opt	-	Opt	Opt	Opt	Opt	Opt
VE3	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt
VE4	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	Opt
VE5	-	-	-	-	-	-	-	-	-	-	-	-	Opt
<b>Central Storage:</b>													
32M bytes	Std	Std	Std	Std	Std	-	-	-	-	-	-	-	-
64M bytes	-	Opt	Opt	Opt	Opt	Std	Std	-	Std	-	-	-	-
64M bytes (32M bytes/side)	-	-	-	-	-	-	-	Std	-	-	-	-	-
128M bytes	-	-	-	-	-	-	Opt	-	Opt	-	-	-	-
128M bytes (64M bytes/side)	-	-	-	-	-	-	-	Opt	-	Std	Std	Std	Std
256M bytes (128M bytes/side)	-	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt

Item	Model													
	120E	150	150E	180	180E	200	200E	280E	300E	400	400E	500E	600E	
<b>Expanded Storage:</b>														
64M bytes	Opt	-	Opt	Opt	Opt	Opt	Opt	-	Opt	-	-	-	-	
128M bytes	Opt	-	Opt	Opt	Opt	Opt	Opt	-	Opt	-	-	-	-	
128M bytes (64M bytes/side)	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt	
192M bytes	-	-	-	Opt	Opt	Opt	Opt	-	Opt	-	-	-	-	
256M bytes	-	-	-	Opt	Opt	Opt	Opt	-	Opt	-	-	-	-	
256M bytes (128M bytes/side)	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt	
384M bytes (192M bytes/side)	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt	
512M bytes	-	-	-	-	-	-	Opt	-	Opt	-	-	-	-	
512M bytes (256M bytes/side)	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt	
1024M bytes	-	-	-	-	-	-	Opt	-	Opt	-	-	-	-	
1024M bytes (512M bytes/side)	-	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	
2048M bytes (1024M bytes/side)	-	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	
<b>Processor Resource/Systems Manager:</b>														
	Opt	-	Opt	-	Opt	-	Opt	Opt	Opt	-	Opt	Opt	Opt	

Item	Model													
	120E	150	150E	180	180E	200	200E	280E	300E	400	400E	500E	600E	
<b>Channels:</b>														
16	Std	Std	Std	Std	Std	-	-	-	-	-	-	-	-	-
24	Opt	Opt	Opt	Opt	Opt	-	-	-	-	-	-	-	-	-
32	-	-	-	Opt	Opt	Std	Std	-	Std	-	-	-	-	-
32 (16/side)	-	-	-	-	-	-	-	Std	-	-	-	-	-	-
40	-	-	-	-	-	Opt	Opt	-	Opt	-	-	-	-	-
48	-	-	-	-	-	Opt	Opt	-	Opt	-	-	-	-	-
48 (24/side)	-	-	-	-	-	-	-	Opt	-	-	-	-	-	-
64	-	-	-	-	-	-	Opt	-	Opt	-	-	-	-	-
64 (32/side)	-	-	-	-	-	-	-	Opt	-	Std	Std	Std	Std	Std
80 (40/side)	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	Opt	Opt
96 (48/side)	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	Opt	Opt
128 (64/side)	-	-	-	-	-	-	-	-	-	-	Opt	Opt	Opt	Opt
<b>Processor Units:</b>														
3090	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req
<b>Processor Controller:</b>														
3092 Model 1	-	Req	Req	Req	Req	Req	Req	-	Req	-	-	-	-	-
3092 Model 2	-	-	-	-	-	-	-	Req	-	Req	Req	Req	Req	Req
3092 Model 3	Req	-	-	-	-	-	-	-	-	-	-	-	-	-
<b>Displays:</b> (IBM 3180 Display Station Model 140, IBM 3206 Display Station Model 100, or equivalent)														
First Display	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req
Second Display	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req
Third Display	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Req	Opt	Req	Req	Req	Req	Req
Fourth Display	-	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
Fifth Display	-	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
Sixth Display	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt	Opt
<b>Printers:</b> (IBM 3287 Printer Model 1 or 2, or IBM 4224 Printer Model 201 or 202, or equivalent)														
First Printer	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
Second Printer	-	-	-	-	-	-	-	Opt	-	Opt	Opt	Opt	Opt	Opt
<b>Direct Access Storage Device:</b> (IBM 3370 Model A2 with String-Switch Feature, or equivalent)														
First 3370	Req@	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req
Second 3370	-	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req
<b>Magnetic Tape Subsystem: (see Note)</b> (IBM 3420, 3422, or 3480, or equivalent)														
Tape Subsystem	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req

Item	Model												
	120E	150	150E	180	180E	200	200E	280E	300E	400	400E	500E	600E
<b>Modems:</b> (3864 Model 2 with automatic calling unit feature, or equivalent)													
First Modem	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req
Second Modem	-	-	-	-	-	-	-	Req	-	Req	Req	Req	Req
<b>Power and Coolant Distribution Units:</b> (IBM 3097 PCDU Model 1 or 2)													
First 3097	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req
Second 3097	-	-	-	-	-	-	-	Req	-	Req	Req	Req	Req
<b>Power Units:</b> (IBM 3089 Power Unit Model 3, or other 400-Hz power source)													
First 3089	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req	Req
Second 3089	-	-	-	*	*	Req	Req	Req	Req	Req	Req	Req	Req
Third 3089	-	-	-	-	-	-	-	**	-	Req	Req	Req	Req
Fourth 3089	-	-	-	-	-	-	-	**	-	Req	Req	Req	Req

\* Two 3089 Power Units are required if the processor complex has both a vector facility feature and more than 128M bytes of expanded storage; otherwise, one 3089 Power Unit is required.

\*\* Four 3089 Power Units are required if the processor complex has two vector facility features and more than 256M bytes of expanded storage; three 3089 Power Units are required if the processor complex has one vector facility feature and more than 256M bytes of expanded storage; otherwise, two 3089 Power Units are required.

@ String-switch feature is not required.

Note:

The 3090 Processor Complex requires access to one of the following:

- A path to one IBM 3803 Tape Control Unit Model 2 (or equivalent). The tape control unit must have an IBM 3420 Magnetic Tape Unit Model 4, 6, or 8 or an equivalent 6250 bit-per-inch tape drive with a maximum data rate of 1.25 megabytes per second. A 3090 Model 280E, 400, 400E, 500E, or 600E requires access to two channel paths to the tape control unit.
- A path to an IBM 3422 Magnetic Tape Subsystem (or equivalent). A 3090 Model 280E, 400, 400E, 500E, or 600E requires access to two channel paths to the magnetic tape subsystem.
- A path to an IBM 3480 Magnetic Tape Unit Model B11 or Model B22 (or equivalent). A 3090 Model 280E, 400, 400E, 500E, or 600E requires access to two channel paths to the magnetic tape subsystem.

Legend:

CP Central processor  
CSS Channel subsystem  
Opt Optional  
PCDU Power and coolant distribution unit  
Req Required  
SCE System control element  
Std Standard  
VE Vector  
- Not available

)

## Glossary of Terms and Abbreviations

See the Index or the *IBM Dictionary of Computing*, SC20-1699, for terms that do not appear in this glossary.

**abend.** Abnormal end of task or of processing.

**acronym.** A special type of abbreviation in which the characters chosen to abbreviate the word or words deliberately spell a word (as in RAM, COBOL, or BASIC).

**Add FRR.** Add Functional Recovery Routine instruction.

**address.** An identification of a storage location or an I/O device.

**address translation.** See *dynamic address translation*.

**analysis routine (AR).** A routine that uses error records to indicate the field-replaceable unit (FRU) or FRU group that probably caused the error.

**AR.** Analysis routine.

**ASN.** Address space number.

**auto-vectoring.** Occurs when VS FORTRAN Version 2 source code is automatically compiled to contain object code with vector instructions.

**BAS.** Branch and Save instruction.

**BASR.** Branch and Save instruction.

**BC.** Basic control mode.

**BCE.** Buffer control element.

**bit.** Binary digit.

**BOC.** Battery-operated clock.

**bpi.** Bits per inch.

**cache.** A high-speed buffer.

**CAW.** Channel address word (S/370).

**CC.** Condition code.

**CCC.** Channel control check.

**CCE.** Channel control element.

**CCW.** Channel command word.

**CDC.** Channel data check.

**CDS.** Compare Double and Swap instruction.

**central storage.** Includes both main storage (programs and data) and the hardware system area (not addressable by programming). Available to the channel subsystem and all central processors.

**channel.** Each channel in the channel subsystem controls an I/O interface between the channel control element and the attached control units.

**channel control element (CCE).** The channel control element in the channel subsystem.

**channel subsystem (CSS).** The channel subsystem is responsible for all I/O operations.

**CHE.** Channel element.

**CHN.** Channel.

**CHPID.** Channel path identifier.

**CLRCH.** Clear Channel (S/370 I/O instruction).

**CLRIO.** Clear I/O (S/370 I/O instruction).

**compute intensive.** Characterized by high central processor utilization.

**console.** A logical device that is used for communication between the user and the system. See *display station, monitor consoles, operator console, programming support console, service console, system console*.

**control, operator.** Any control (hardware or microcode) that can be used to communicate with the processor complex. Controls can include switches, pushbuttons, function keys, commands, and display frames.

**CP.** Central processor.

**CPU.** Central processing unit.

**CRW.** Channel report word (370-XA and ESA/370).

**CS.** Compare and Swap instruction.

**CSCH.** Clear Subchannel (370-XA and ESA/370 I/O instruction).

**CSE.** Control storage element (CP).

**CSS.** Channel subsystem.

**CSW.** Channel status word.

**CTCA.** Channel-to-channel adapter.

**CU.** Control unit.

**DACB.** Device address control block.

**DAS.** Dual-address space.

**DASD.** Direct-access storage device.

**DAT.** Dynamic address translation.

**display station.** A physical device that can be used as multiple logical consoles. See *console*.

**DXR.** Divide instruction.

**dyadic processor.** A two-way multiprocessor that uses two central processors for instruction execution while sharing central storage and channels.

**dynamic address translation (DAT).** The conversion of virtual addresses to real addresses immediately before the address is used, allowing the use of virtual addresses in instructions and commands.

**EC.** Extended control mode.

**ECC.** Error checking and correction.

**ECL.** Emitter-coupled logic.

**ECW.** Extended control word (370-XA and ESA/370).

**EE.** Execution element (CP).

**element.** A major part of a component (for example, the buffer control element) or a major part of the processor complex (for example, the system control element).

**error checking and correction (ECC).** Hardware that automatically corrects all single-bit errors and detects all double-bit errors and most triple-bit errors.

**ESA/370.** Enterprise Systems Architecture/370.

**ESSL.** Engineering and Scientific Subroutine Library.

**ESW.** Extended status word (370-XA and ESA/370).

**expanded storage.** Optional integrated high-speed storage that transfers 4K-byte pages to and from central storage.

**facility.** Hardware and software that provide useful capabilities for humans (as in an operator facility or a maintenance service facility).

**FCC.** Federal Communications Commission.

**FP.** Floating point.

**FPR.** Floating-point register.

**FRR.** Functional recovery routine.

**FRU.** Field-replaceable unit.

**ft.** (1) Foot. (2) Feet.

**G-byte.** 1 073 741 824 bytes.

**gigabyte.** 1 073 741 824 bytes.

**GR.** General register (CP).

**guest.** In interpretive execution mode, the interpreted or virtual machine as opposed to the real machine (host).

**hardware system area (HSA).** A logical area of central storage that is used to store microcode, instructions, and control information (not addressable by application programs).

**HDV.** Halt Device instruction (S/370).

**hex.** Hexadecimal.

**high-speed buffer.** A 64K-byte cache (one for each central processor).

**HIO.** Halt I/O (S/370 I/O instruction).

**host.** In interpretive execution mode, the real machine as opposed to the virtual or interpreted machine (the guest).

**HSA.** Hardware system area.

**HSCH.** Halt Subchannel (370-XA and ESA/370 I/O instruction).

**ID.** (1) Identifier. (2) Identification.

**IDAW.** Indirect data address word.

**IE.** Instruction element.

**IFCC.** Interface control check.

**IML.** Initial microprogram load.



**initialization.** To set counters, switches, addresses, latches, or storage contents to 0 or to other starting values at the beginning of, or at the prescribed points in, a computer program or process.

**I/O.** Input/output.

**I/O Configuration Program (IOCP).** Defines for the central processors all of the I/O devices and all of the available channel paths.

**I/O interface.** The I/O interface connects channels and control units for the exchange of signals and data.

**IOCDS.** I/O configuration data set.

**IOCP.** I/O Configuration Program.

**IOPD.** (1) I/O problem determination. (2) I/O Problem Determination frame.

**IOTA.** Input/output transaction area.

**IPK.** Insert PSW Key instruction.

**IPL.** Initial program load.

**IPTE.** Invalidate Page Table Entry instruction.

**ISK.** Insert Storage Key instruction.

**ISKE.** Insert Storage Key Extended instruction.

**K-byte.** 1024 bytes.

**kilobyte.** 1024 bytes.

**LCL.** Limited channel logout (S/370).

| **LCU.** Logical control unit (370-XA and ESA/370).

**limited channel logout (LCL).** An error record containing detailed information about an error affecting an I/O operation.

**logout.** Log data that has been collected, formatted, and recorded.

| **LPAR.** Logically partitioned.

**LRA.** Load Read Address instruction.

**M-byte.** 1 048 576 bytes.

**MC.** Monitor Call instruction.

**MCCU.** IBM 3088 Multisystem Channel Communication Unit.

**MCIC.** Machine-check interruption code.

**megabyte.** 1 048 576 bytes.

**MHz.** Megahertz.

**microsecond ( $\mu$ s).** One millionth of a second.

**modem.** Modulator-demodulator.

**monitor consoles.** Optional logical displays that are used to monitor the service or system consoles. Each monitor console can be assigned to any of the physical displays attached to the 3092.

$\mu$ s. Microsecond.

| **MSCH.** Modify Subchannel (370-XA and ESA/370 I/O instruction).

| **MTF.** Multitasking facility.

**multiplexing.** The ability of the channel and the device to disconnect and reconnect during an operation.

| **MVS/370.** MVS/SP Version 1.

**MVS/SP.** Multiple Virtual Storage/System Product.

| **MVS/XA.** MVS/SP Version 2.

**nanosecond (ns).** One thousandth of a microsecond.

**ns.** Nanosecond.

**operator console.** A required display that is channel attached to the processor unit to provide communication with the system control program.

**operator control.** Any control (hardware or microcode) that can be used to communicate with the processor complex. Controls can include switches, pushbuttons, function keys, commands, and frames.

| **ORB.** Operation request block.

| **PA.** Problem analysis.

**PCDU.** Power and coolant distribution unit.

**PER.** Program-event recording.

**port.** An access point for data entry or exit.

**processor complex.** A configuration comprising the:

- Processor unit
- Processor controller
- System display
- Service display
- Power and coolant distribution unit

- Power units

**processor controller.** Provides support and diagnostic functions for the central processors.

**processor storage.** The combination of central storage and expanded storage provided by a 3090 Processor Unit.

**program mode console.** Logical device that can be assigned to any of the physical displays attached to the 3092 Processor Controller.

**PR/SM.** Processor Resource/Systems Manager.

**PSW.** Program status word.

**PTLB.** Purge Translation Lookaside Buffer instruction.

**RAS.** Reliability, availability, and serviceability.

**RIO.** Resume I/O (S/370 I/O instruction).

**RPQ.** Request for price quotation.

**RRB.** Reset Reference Bit instruction.

**RRBE.** Reset Reference Bit Extended instruction.

**RSCH.** Resume Subchannel (370-XA and ESA/370 I/O instruction).

**RSF.** Remote support facility.

**S/370.** System/370 mode.

**SAD.** System activity display.

**SCE.** System control element.

**SCH.** Subchannel.

**SCK.** Set Clock instruction.

**SCKC.** Set Clock Comparator instruction.

**SCP.** System control program.

**service console.** A logical device used by service personnel to maintain the processor complex and to isolate failing field-replaceable units.

**service support display.** An IBM 3180 Display Station Model 140 or IBM 3206 Display Station Model 100 attached to a port of the processor controller, and that can be switched to a control unit on a channel of the 3090 Processor Complex for online test program use.

**SIE.** Start Interpretive Execution (370-XA and ESA/370 instruction).

**SIGP.** Signal Processor instruction.

**single channel service (SCS).** The capability of running diagnostic tests on a single channel while the other channels are being used by the customer.

**SIO.** Start I/O (S/370 I/O instruction).

**SIOF.** Start I/O Fast Release (S/370 I/O instruction).

**SPKA.** Set PSW Key from Address instruction.

**SPT.** Set CPU Timer instruction.

**SSCH.** Start Subchannel (370-XA and ESA/370 I/O instruction).

**SSK.** Set Storage Key instruction.

**SSKE.** Set Storage Key Extended instruction.

**SSM.** Set System Mask instruction.

**STAP.** Store CPU Address instruction.

**STCKC.** Store Clock Comparator instruction.

**STCPS.** Store Channel Path Status (370-XA or ESA/370 I/O instruction).

**STCRW.** Store Channel Report Word (370-XA or ESA/370 I/O instruction).

**std.** Standard.

**STIDC.** Store Channel ID (S/370 I/O instruction).

**STIDP.** Store CPU ID instruction.

**STNSM.** Store Then AND System Mask instruction.

**storage key.** A control field associated with a defined block of storage that protects that block of storage from unauthorized access and change.

**STOSM.** Store Then OR System Mask instruction.

**STPT.** Store CPU Timer instruction.

**subchannel.** The channel subsystem facilities required for sustaining a single I/O operation.

**SVC.** Supervisor Call instruction.

**system.** The processor complex and its attached and configured I/O and communication devices.

**system console.** A logical device used for the operation and control of hardware functions (for example, IPL, alter or display, and reconfiguration).

**system control element (SCE).** Handles the transfer of data and control information associated with storage requests between the elements of the processor complex.

**system display.** A required 3180 or 3206 Display Station that is attached to a port of the 3092 Processor Controller.

**TB.** Test Block instruction.

**TCH.** Test Channel (S/370 I/O instruction).

**TCM.** Thermal conduction module.

**thermal conduction module (TCM).** A field-replaceable unit containing multiple logic chips.

**TIO.** Test I/O (S/370 I/O instruction).

**TLB.** Translation lookaside buffer. (Directory lookaside table in the CP.)

**TOD.** Time of day.

**TPF.** Transaction Processing Facility.

**TPROT.** Test Protection instruction.

**triadic processor.** A three-way multiprocessor that uses three central processors for instruction execution while sharing central storage and channels.

**TSCH.** Test Subchannel (370-XA or ESA/370 I/O instruction).

**TTL.** Transistor-to-transistor logic.

**UCW.** Unit control word.

**V = F.** Virtual equals fixed.

**V = R.** Virtual equals real.

**V = V.** Virtual equals virtual.

**vector facility feature.** An optional feature for each central processor of the 3090 Processor Complex that provides the central processor with significantly increased levels of performance for many compute-intensive engineering and scientific applications.

**VF.** Vector facility feature.

**VMA.** Virtual-machine assist.

**VM/SP.** Virtual Machine/System Product.

**VM/SP HPO.** Virtual Machine/System Product High Performance Option.

**VM/XA.** Virtual machine/extended architecture.

**VM/XA SF.** Virtual Machine/Extended Architecture Systems Facility.

**VM/XA SP.** Virtual Machine/Extended Architecture System Product.

**VSE.** Virtual storage extended.

**370-XA.** System/370 extended architecture.

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IBM 3090 Processor Complex Functional Characteristics

Order No. SA22-7121-6

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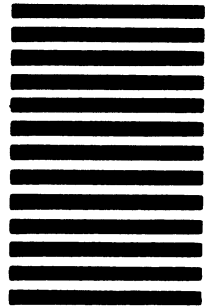
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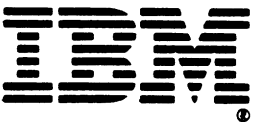
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