IBM 3090 Processor Complex Channel Characteristics and Configuration Guide

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Preface

This manual is intended to provide system engineers, system analysts, and system programmers with:

- Channel operation information on the IBM 3090 Processor Complex Models 120E, 150, 150E, 180, 180E, 200, 200E, 280E, 300E, 400, 400E, 500E, and 600E.
- A description of the channel operations, components, and functions of the IBM 3090 Processor Complex in System/370 (S/370) mode, System/370 extended architecture (370-XA) mode, and Enterprise Systems Architecture/370™ (ESA/370™) mode.
- Guidelines for configuring channel loads in an IBM 3090 Processor Complex (all models)

The reader should understand S/370, 370-XA, and ESA/370 input/output operations and be familiar with the content of the *IBM 3090 Processor Complex: Functional Characteristics*, SA22-7121, the *IBM System/370 Principles of Operation*, GA22-7000, the *IBM System/370 Extended Architecture Principles of Operation*, SA22-7085, and the *IBM Enterprise Systems Architecture/370 Principles of Operation* (to be available at a later date).

This manual contains four chapters, an appendix, a glossary of terms and abbreviations, and a bibliography:

- Chapter 1, "Introduction" provides an overview of the channels of the IBM 3090 Processor Complex Models 120E, 150, 150E, 180, 180E, 200, 200E, 280E, 300E, 400, 400E, 500E, and 600E.
- Chapter 2, "Channel Operation Characteristics" describes the characteristics, structure, and functions of the channels.
- Chapter 3, "Channel Performance Characteristics" describes channel performance concepts and characteristics, and the criteria for determining the sequence of attachment of input/output (I/O) devices.
- Chapter 4, "Channel Configuration Guidelines" describes how to configure I/O devices for operation on block-multiplexer or byte-multiplexer channels.
- Appendix, "Device Class and Critical Time for Byte-Multiplexer Channels" lists device classes and critical times.
- "Glossary of Terms and Abbreviations" defines the technical terms and abbreviations used in this manual.

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- "Bibliography" lists the manuals that are recommended for use with this manual.

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Chapter 1. Introduction

The IBM 3090 Processor Complex is a general-purpose data processing system. The IBM 3090 base models (Models 150, 180, 200, and 400) provide for operation in System/370 (S/370) mode or in System/370 extended architecture (370-XA) mode. The enhanced IBM 3090 Models 120E, 150E, 180E, 200E, 280E, 300E, 400E, 500E, and 600E are the most recent models of the 3090 Processor Complex and can operate in S/370 mode or in Enterprise Systems Architecture/370 (ESA/370) mode. These systems provide reliability, performance, and ease of use for commercial, engineering, and scientific applications.

The 3090 is a compatible growth system for the IBM 3081, 3083, and 3084 Processor Complexes.

Summary of 3090 Model Configurations

The **3090 Model 120E** contains one central processor with a vector facility feature (optional), a central storage, an expanded storage (optional), a system control element (SCE), and a channel subsystem (CSS). The IBM 3090 Processor Complex Model 120E includes the following:

- 3090 Processor Unit Model 120E
  - One central processor
  - 16 channels standard, 8 channels optional, for a maximum of 24 channels
- 3092 Processor Controller Model 3
- 3097 Power and Coolant Distribution Unit Model 1 or 2
- 3089 Power Unit Model 3 (or other appropriate 400-Hz power source)
- Two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100

The **3090 Model 150** contains one central processor with a vector facility feature (optional), a central storage, a system control element (SCE), and a channel subsystem (CSS). The IBM 3090 Processor Complex Model 150 includes the following:

- 3090 Processor Unit Model 150
  - One central processor
  - 16 channels standard, 8 channels optional, for a maximum of 24 channels
- 3092 Processor Controller Model 1
- 3097 Power and Coolant Distribution Unit Model 1 or 2

- 3089 Power Unit Model 3 (or other appropriate 400-Hz power source)
- Two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100

The **3090 Model 150E** contains one central processor with a vector facility feature (optional), a central storage, an expanded storage (optional), a system control element (SCE), and a channel subsystem (CSS). The IBM 3090 Processor Complex Model 150E includes the following:

- 3090 Processor Unit Model 150E
  - One central processor
  - 16 channels standard, 8 channels optional, for a maximum of 24 channels
- 3092 Processor Controller Model 1
- 3097 Power and Coolant Distribution Unit Model 1 or 2
- 3089 Power Unit Model 3 (or other appropriate 400-Hz power source)
- Two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100

The **3090 Model 180** contains one central processor with a vector facility feature (optional), a central storage, an expanded storage (optional), a system control element (SCE), and a channel subsystem (CSS). The IBM 3090 Processor Complex Model 180 includes the following:

- 3090 Processor Unit Model 180
  - One central processor
  - 16 channels standard, 16 channels optional (in increments of 8), for a maximum of 32 channels
- 3092 Processor Controller Model 1
- 3097 Power and Coolant Distribution Unit Model 1 or 2
- One or two 3089 Power Unit Model 3 (or other appropriate 400-Hz power source)
- Two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100

The **3090 Model 180E** contains one central processor with a vector facility feature (optional), a central storage, an expanded storage (optional), a system control element (SCE), and a channel subsystem (CSS). The IBM 3090 Processor Complex Model 180E includes the following:

- 3090 Processor Unit Model 180E
  - One central processor

  - 16 channels standard, 16 channels optional (in increments of 8), for a maximum of 32 channels

- 3092 Processor Controller Model 1
- 3097 Power and Coolant Distribution Unit Model 1 or 2
- One or two 3089 Power Units Model 3 (or other appropriate 400-Hz power source)
- Two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100

The **3090 Model 200** contains two central processors, each with a vector facility feature (optional), a shared central storage, a shared expanded storage (optional), a system control element (SCE), and a channel subsystem (CSS). The IBM 3090 Processor Complex Model 200 includes the following:

- 3090 Processor Unit Model 200
  - Two central processors
  - 32 channels standard, 16 channels optional (in increments of 8), for a maximum of 48 channels
- 3092 Processor Controller Model 1
- 3097 Power and Coolant Distribution Unit Model 1 or 2
- Two 3089 Power Units Model 3 (or other appropriate 400-Hz power source)
- Two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100

The **3090 Model 200E** contains two central processors, each with a vector facility feature (optional), a shared central storage, a shared expanded storage (optional), a system control element (SCE), and a channel subsystem (CSS). The IBM 3090 Processor Complex Model 200E includes the following:

- 3090 Processor Unit Model 200E
  - Two central processors
  - 32 channels standard, 32 channels optional (in increments of 8, 8, and 16), for a maximum of 64 channels
- 3092 Processor Controller Model 1
- 3097 Power and Coolant Distribution Unit Model 1 or 2
- Two 3089 Power Units Model 3 (or other appropriate 400-Hz power source)

- Two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100

The **3090 Model 280E** contains two central processors, each with a vector facility feature (optional), a shared central storage, a shared expanded storage (optional), two system control elements (SCEs), and two channel subsystems (CSSs).

When in single-image configuration, the two CSSs of the Model 280E coordinate activity and appear as a single dynamic channel subsystem to the control program. The Model 280E can operate in a physically partitioned configuration with operational characteristics similar to two Model 180Es. The IBM 3090 Processor Complex Model 280E includes the following:

- 3090 Processor Unit Model 280E
  - Two central processors
  - 32 channels standard (16 on each side); 32 channels (16 on each side) optional (in increments of 8 on each side) for a maximum of 64 channels
- 3092 Processor Controller Model 2
- Two 3097 Power and Coolant Distribution Units Model 1 or 2
- Two, three, or four 3089 Power Units Model 3 (or other appropriate 400-Hz power source)
- Three 3180 Display Stations Model 140 or three 3206 Display Stations Model 100

The **3090 Model 300E** contains three central processors, each with a vector facility feature (optional), a shared central storage, a shared expanded storage (optional), a system control element (SCE), and a channel subsystem (CSS). The IBM 3090 Processor Complex Model 300E includes the following:

- 3090 Processor Unit Model 300E
  - Three central processors
  - 32 channels standard, 32 channels optional (in increments of 8, 8, and 16), for a maximum of 64 channels
- 3092 Processor Controller Model 1
- 3097 Power and Coolant Distribution Unit Model 1 or 2
- Two 3089 Power Units Model 3 (or other appropriate 400-Hz power source)
- Two 3180 Display Stations Model 140 or two 3206 Display Stations Model 100

The **3090 Model 400** contains four central processors, each with a vector facility feature (optional), a shared central storage, a shared expanded storage (optional), two system control elements (SCEs), and two channel subsystems (CSSs).

When in single-image configuration, the two CSSs of the Model 400 coordinate activity and appear as a single dynamic channel subsystem to the control program. The Model 400 can operate in a physically partitioned configuration with operational characteristics similar to two Model 200s. The IBM 3090 Processor Complex Model 400 includes the following:

- 3090 Processor Unit Model 400
  - Four central processors
  - 64 channels standard (32 on each side), 32 channels optional (16 on each side, in increments of 8), for a maximum of 96 channels
- 3092 Processor Controller Model 2
- Two 3097 Power and Coolant Distribution Units Model 1 or 2
- Four 3089 Power Units Model 3 (or other appropriate 400-Hz power source)
- Three 3180 Display Stations Model 140 or three 3206 Display Stations Model 100

The **3090 Model 400E** contains four central processors, each with a vector facility feature (optional), a shared central storage, a shared expanded storage (optional), two system control elements (SCEs), and two channel subsystems (CSSs).

When in single-image configuration, the two CSSs of the Model 400E coordinate activity and appear as a single dynamic channel subsystem to the control program. The Model 400E can operate in a physically partitioned configuration with operational characteristics similar to two Model 200Es. The IBM 3090 Processor Complex Model 400E includes the following:

- 3090 Processor Unit Model 400E
  - Four central processors
  - 64 channels standard (32 on each side); 64 channels (32 on each side) optional (in increments of 8, 8, and 16 on each side), for a maximum of 128 channels
- 3092 Processor Controller Model 2
- Two 3097 Power and Coolant Distribution Unit Model 1 or 2
- Four 3089 Power Units Model 3 (or other appropriate 400-Hz power source)
- Three 3180 Display Stations Model 140 or three 3206 Display Stations Model 100

The **3090 Model 500E** contains five central processors, each with a vector facility feature (optional), a shared central storage, a shared expanded storage (optional), two system control elements (SCEs), and two channel subsystems (CSSs).

When in single-image configuration, the two CSSs of the Model 500E coordinate activity and appear as a single dynamic channel subsystem to the control program. The Model 500E can operate in a physically partitioned configuration with operational characteristics similar to a Model 300E and 200E, respectively. The IBM 3090 Processor Complex Model 500E includes the following:

- 3090 Processor Unit Model 500E
  - Five central processors
  - 64 channels standard (32 on each side); 64 channels (32 on each side) optional (in increments of 8, 8, and 16 on each side) for a maximum of 128 channels
- 3092 Processor Controller Model 2
- Two 3097 Power and Coolant Distribution Units Model 1 or 2
- Four 3089 Power Units Model 3 (or other appropriate 400-Hz power source)
- Three 3180 Display Stations Model 140 or three 3206 Display Stations Model 100

The **3090 Model 600E** contains six central processors, each with a vector facility feature (optional), a shared central storage, a shared expanded storage (optional), two system control elements (SCEs), and two channel subsystems (CSSs).

When in single-image configuration, the two CSSs of the Model 600E coordinate activity and appear as a single dynamic channel subsystem to the control program. The Model 600E can operate in a physically partitioned configuration with operational characteristics similar to two Model 300Es. The IBM 3090 Processor Complex Model 600E includes the following:

- 3090 Processor Unit Model 600E
  - Six central processors
  - 64 channels standard (32 on each side); 64 channels (32 on each side) optional (in increments of 8, 8, and 16 on each side) for a maximum of 128 channels
- 3092 Processor Controller Model 2
- Two 3097 Power and Coolant Distribution Units Model 1 or 2
- Four 3089 Power Units Model 3 (or other appropriate 400-Hz power source)

- Three 3180 Display Stations Model 140 or three 3206 Display Stations Model 100

Channel Subsystem

A channel subsystem consists of one channel control element (CCE) and a number of channels. Each side of a Model 280E, 400, 400E, 500E, and 600E has one channel subsystem. In single-image configuration, the two channel subsystems coordinate activity and appear to the control program as one dynamic channel subsystem. In logically partitioned operation, each logical partition appears to have a dynamic channel subsystem. Models 120E, 150, 150E, 180, 180E, 200, 200E, and 300E can have as many as four channels configured for byte multiplex mode of operation (with the Processor Resource/Systems Manager™ feature (PR/SM™) installed, as many as eight channels can be configured for byte multiplex mode of operation). Models 280E, 400, 400E, 500E, and 600E can have as many as eight channels configured for byte multiplex mode of operation (with the PR/SM feature installed, as many as 16 channels can be configured for byte multiplex mode of operation). All the other channels may be configured for block multiplex mode of operation.

The following information applies to a channel subsystem for a processor that is not operating in a physically partitioned configuration, to either the side 0 or side 1 channel subsystem of Models 280E, 400, 400E, 500E, and 600E in a physically partitioned configuration, and to each logical partition of a logically partitioned processor.

The channel subsystem handles all I/O operations for the central processors. The CSS controls communication between a configured channel and the control unit and device. The I/O configuration data set (IOCDS) that is selected at system initialization defines the channel paths on the processor complex, the control units attached to the channel paths, and the I/O devices assigned to the control units. The IOCDS is created by the I/O Configuration Program (IOCP) and is stored on a 3370 Direct Access Storage device associated with the processor controller. At system initialization, the IOCDS information is used to build the necessary control blocks in the hardware system area of central storage (which is not available for program use).

When logical partitioning is in effect, individual channel paths may be allocated to each logical partition. A channel path can be allocated only to one logical partition at a time. A device can be shared between logical partitions by using a separate channel path from each logical partition. Channel paths can be dynamically reconfigured between logical partitions, without requiring a power-on reset of the processor complex.

The channel subsystem logical organization is shown in Figure 1-1 on page 1-8.

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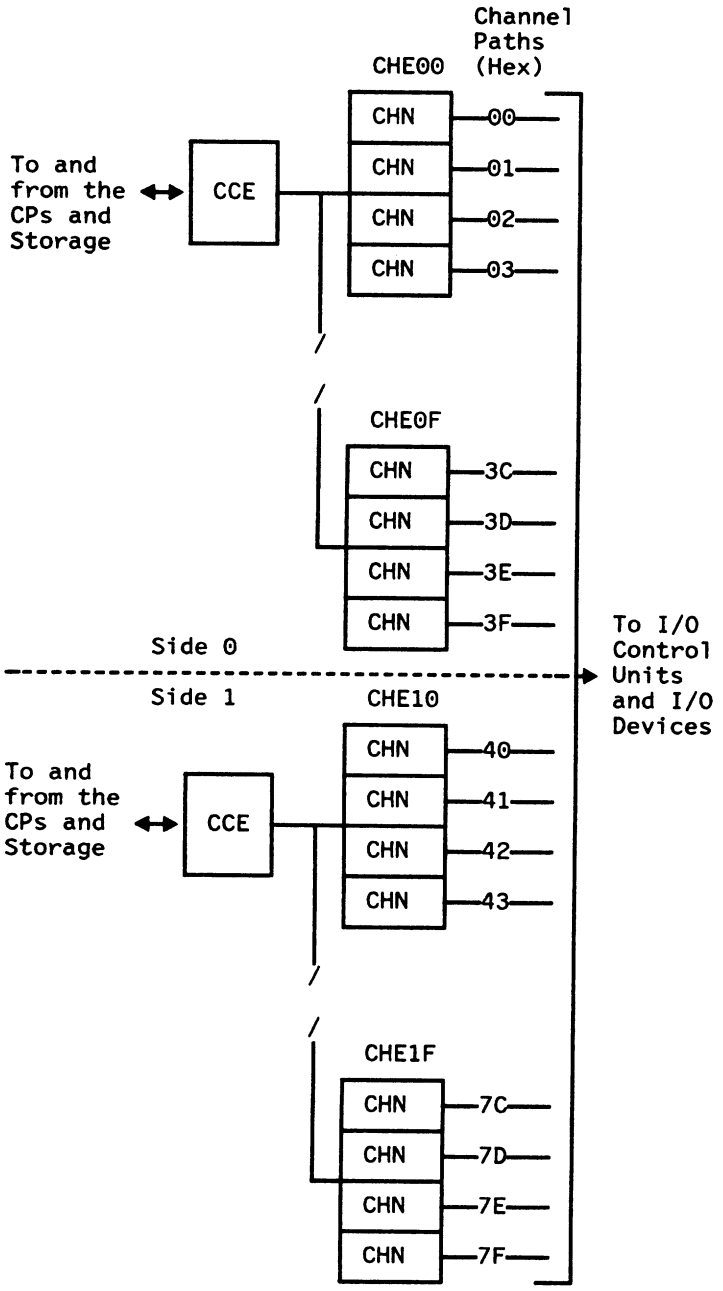

Legend:

CCE Channel control element
CHE Channel element
CHN Channel
CP Central processor

Figure 1-1. 3090 Model 600E (Maximum Configuration) Channel Subsystem

Channel Control Element

The channel control element (CCE) interacts with central storage, the central processors, and the channels to provide the following services:

- Initializing and terminating all channel operations
- Centralizing storage access control
- Prioritizing I/O operations
- Detecting and decoding central processor (CP) requests for I/O activity
- Fetching, updating, and restoring I/O control blocks

  Note: The S/370 control blocks represent channel sets and devices. The 370-XA and ESA/370 control blocks represent logical channel queues and subchannels (devices).

- Detecting and decoding channel requests for service
- Presenting I/O interruptions to the CPs

Channels

The channels control all data flow between the channel control element and the attached control units. Each channel operates independently to handle all interface sequences, CCW fetches, and data transfers.

Each channel is initialized at system initialization (or when assigned to a logical partition) for one of the following modes of operation:

- S/370 byte multiplex mode of operation
- S/370 block multiplex mode of operation
- 370-XA or ESA/370 byte multiplex mode of operation
- 370-XA or ESA/370 block multiplex mode of operation

Chapter 2. Channel Operation Characteristics

The channels in the channel subsystem permit transfer of data between central storage and I/O devices, under control of a channel program. The channels act independent of other operations being performed by a central processor. A central processor is therefore free to resume other operations after initiating an I/O operation.

The channel facility required to perform an I/O operation is called a subchannel. The control and implementation of I/O operations depend on the following:

- Architectural mode of operation
  - S/370
  - 370-XA (Models 150, 180, 200, and 400)
  - ESA/370 (Models 120E, 150E, 180E, 200E, 280E, 300E, 400E, 500E, and 600E)
- Data mode of operation
  - Byte multiplex
  - Block multiplex
- I/O interface protocol
  - Interlocked
  - Data streaming

Subchannels

One unit control word (UCW) is assigned to each subchannel. UCWs are stored in the hardware system area of central storage and are moved to a channel subsystem during execution of an I/O operation.

Each UCW contains the following control information:

- Protection key
- Data address
- Identity of the operation specified by the command code
- CCW flags
- Byte count

- Channel status
- Address of the next CCW
- Channel path identifiers for as many as four channel paths, which may be configured to an I/O device (370-XA and ESA/370 modes only)

The number of I/O devices supported is 4096 minus the number of channels defined by the Input/Output Configuration Program (IOCP). In 370-XA and ESA/370 modes, one UCW is assigned for each subchannel (device). In S/370 mode, UCW assignment can be either:

- Nonshared, each device is assigned a separate UCW
- Shared, several devices share one UCW

In S/370 mode, if more than one channel address is associated with an I/O device, a separate UCW is assigned for each channel address.

The 3090 provides two sets of I/O display frames (one for S/370 mode and one for 370-XA or ESA/370 mode) that display the contents of a specified subchannel or UCW.

The **architectural mode of operation** is determined by the central processor (CP) instruction set (S/370, 370-XA, or ESA/370) selected during initialization of a logical partition or of the processor complex (or for Models 280E, 400, and 400E, the initialization of a side of a processor complex operating in a physically partitioned configuration). Models 300E, 500E, and 600E offer only ESA/370 mode of operation, unless logically partitioned.

The **data mode of operation** is determined by the multiplex mode (byte or block) selected for specific channels during initialization of a logical partition or of the processor complex (or for Models 280E, 400, 400E, 500E, and 600E, the initialization of a side of a processor complex operating in a physically partitioned configuration).

The **I/O interface protocol** is determined by the interface sequencing operations selected for specific control units and their associated devices that are attached to the channel.

Channel Control

I/O operations over the interface are controlled by channel commands and mode-dependent I/O instructions, chaining operations, and I/O interruptions.

Channel Commands

Six basic channel commands can be specified by a CCW.

- *Write*, which initiates the transfer of data from central storage to an I/O device.
- *Read*, which initiates the transfer of data from an I/O device to central storage.
- *Read Backward*, which initiates the transfer of data from an I/O device to central storage, with the data bytes being stored in reverse order.
- *Control*, which specifies such operations as set tape density, rewind tape, advance paper in a printer, or sound an audible alarm.
- *Sense*, which requests information from a control unit. The information contains unusual conditions detected during the last I/O operation and detailed device status.
- *Transfer in Channel (TIC)*, which is executed by the channel subsystem and which specifies the location in central storage from which the next CCW in the channel program is to be fetched. The Transfer in Channel command provides branching between CCWs in noncontiguous storage areas. A Transfer in Channel command is not permitted to specify a CCW containing another Transfer in Channel command. Also, in S/370 mode, the channel address word (CAW) is not permitted to specify a CCW containing a Transfer in Channel command.

S/370 Mode

In S/370 mode, the I/O instruction set is an extension of the System/360 I/O instruction set. See "Channel Sets and Logical Channels" on page 2-4 for additional information.

The I/O instructions for operation in S/370 mode are:

- *Start I/O (SIO)*, which initiates an I/O operation if the addressed device is available and can be selected.
- *Start I/O Fast Release (SIOF)*, which allows an I/O operation to be enqueued independent of the status of a device. The operation is performed when the device is available.
- *Resume I/O (RIO)*, which causes a suspended channel program to be resumed.
- *Test Channel (TCH)*, which elicits information about the addressed channel.
- *Clear Channel (CLRCH)*, which performs an I/O system reset in the addressed channel, and signals a system reset on the associated I/O interface.

- *Test I/O (TIO)*, which elicits information about a channel and a particular I/O device.

- *Halt I/O (HIO)*, which terminates execution of the current I/O operation at the addressed channel, subchannel, or I/O device.

- *Clear I/O (CLRIO)*, which performs either the CLRIO function (causing discontinuance of the current operation with the addressed device) or the TIO function (described under Test I/O), depending on block-multiplexing control.

- *Halt Device (HDV)*, which terminates only operations associated with the addressed I/O device. When this instruction is issued to an I/O device on a block-multiplexer channel during data transfer, the subchannel remains in the working state until channel end is received.

- *Store Channel ID (STIDC)*, which places information identifying the designated channel in a specified storage location.

In S/370 mode, all I/O instructions set the program status word (PSW) condition code. Certain conditions also cause a channel status word (CSW) to be stored.

Channel Sets and Logical Channels

In S/370 mode, channels have a logical aspect and a physical aspect. Logically, the channels are organized into channel sets, two channel sets for Models 120E, 150, 150E, 180, 180E, 200, and 200E; and as many as four channel sets for Models 280E, 400, and 400E. In Models 120E, 150, 150E, 180, 180E, and each side of a Model 280E in a physically partitioned configuration, all channels are usually assigned to one channel set (channel set 0) of the single CP.

Note: In an S/370 logical partition, operation is restricted to the use of a single channel set.

A channel set is a group of channels associated with a specific central processor. When an I/O instruction is executed or an I/O interruption occurs, the assigned device address and channel address form a unique identifier (for the currently connected channel set). The unique identifier enables the central processors to select and recognize I/O devices.

In Models 120E, 150, 150E, 180, 180E, 200, and 200E (operating in S/370 mode), the channel set addresses are 0 and 1. Channel set 0 is usually assigned to central processor 1, and channel set 1 is usually assigned to central processor 2. A channel can be assigned to either channel set and is given a logical channel address that can range from 00 to 1F (hexadecimal).

Programming uses the assigned logical channel addresses and channel set addresses to activate any channel through a channel program.

The logical channel addresses in one channel set are independent of the logical channel addresses in the other set, but the addresses in both channel sets can be numerically the same. For example, for a Model 200

having 32 channels with 16 channels in each channel set, both channel sets can have logical channel addresses 00 through 0F.

Note: MVS/System Product (MVS/SP™) supports a maximum of 16 channels in a channel set. VM/System Product with the High Performance Option (VM/SP HPO) supports a maximum of 32 channels in a channel set.

Channel sets may be switched between central processors under program control. In a 3090, MVS/SP uses this switching capability to permit continued I/O operation with all channels in both channel sets if one of the central processors is disabled. VM/SP HPO uses channel sets to assign channels to each central processor, but does not support channel set switching.

If a central processor is removed from the configuration, both channel sets remain configured. However, if a central processor is offline, a reset causes channel set 0 to be connected to the remaining central processor, and channel set 1 to be disconnected. It is advisable to have critical asymmetrically attached devices (such as the operator console) assigned to channels in channel set 0.

At system initialization, a logical channel address is assigned to each physical channel, and each channel is assigned to a channel set through use of the Input/Output Configuration Program (IOCP). The IOCP defines the I/O configuration to the channel subsystem. The IOCP establishes the relationship between the logical channels and the channel path identifiers. For more information about IOCP, see the *IBM 3090 Processor Complex: Input/Output Configuration Program User's Guide and Reference.*

When a Model 400 is operating in a physically partitioned configuration, each side can operate in either S/370 or 370-XA mode. When Models 280E and 400E are operating in a physically partitioned configuration, each side can operate in either S/370 or ESA/370 mode, or can be logically partitioned. In a physically partitioned configuration, a model that is operating in S/370 mode on both sides has four channel sets, two channel sets on side 0 and two channel sets on side 1. Each side has a channel set 0 and a channel set 1:

- Side 0: Channel set 0 is usually assigned to CP1; and for Models 400 and 400E, channel set 1 is usually assigned to CP2.
- Side 1: Channel set 0 is usually assigned to CP3; and for Models 400 and 400E, channel set 1 is usually assigned to CP4.

A Model 400 in a single-image configuration can operate only in 370-XA mode and does not have channel sets. A Model 280E, 400E, 500E, or 600E in a single-image configuration can operate in ESA/370 mode or can be logically partitioned. One channel set is supported by each S/370 logical partition.

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370-XA and ESA/370 Modes

In 370-XA and ESA/370 modes, any CP can initiate I/O operations with any I/O device. Any CP can handle I/O interruptions from any I/O device. Each I/O device is assigned a unique device number, and each device is associated with one subchannel. The CPs communicate with devices by specifying the appropriate subchannel; the subchannel uses the assigned device address to communicate with the device over one or more channel paths. The device number provides a path-independent means to refer to a device for use in operator messages or at the time of IPL.

The I/O instructions for operation in 370-XA and ESA/370 modes are:

- *Start Subchannel (SSCH)*, which initiates execution of a channel program with the I/O device associated with the specified subchannel.
- *Test Subchannel (TSCH)*, which checks subchannel status and can clear the subchannel control bits.
- *Clear Subchannel (CSCH)*, which clears the subchannel and signals the channel subsystem to perform the clear function at the associated I/O device.
- *Halt Subchannel (HSCH)*, which terminates the current operation at the specified subchannel, and signals the channel subsystem to perform the halt function at the I/O device.
- *Resume Subchannel (RSCH)*, which signals the channel subsystem to resume execution of a suspended channel program with the I/O device associated with the specified subchannel.
- *Store Subchannel (STSCH)*, which stores control and status information about the specified subchannel.
- *Modify Subchannel (MSCH)*, which allows the control program to influence the execution of path management functions and some basic I/O functions.
- *Test Pending Interruption (TPI)*, which stores the interruption code for a pending I/O interruption and clears the interruption request.
- *Set Address Limit (SAL)*, which sets the address limit used in a comparison with the absolute storage address each time central storage is accessed for I/O data.
- *Reset Channel Path (RCHP)*, which initiates a reset of the specified channel path. deactivates the channel monitoring modes (measurement-block update and device-connect-time measurement).
- *Store Channel Path Status (STCPS)*, which identifies what channel paths are being used when STCPS is executed.
- *Store Channel Report Word (STCRW)*, which stores error-related information about a malfunction affecting the channel subsystem.

In 370-XA and ESA/370 modes, all I/O instructions except the SAL, SCHM, and STCPS instructions set the PSW condition code. These modes use interruption response blocks rather than channel status words for returning interruption status to the program.

The SSCH instruction specifies an operation request block, which designates the channel program.

Chaining

Following the transfer of information over a channel designated by a CCW, an operation initiated by the SIO or SIOF instruction (in S/370 mode) or by the SSCH instruction (in 370-XA or ESA/370 mode) can be continued by fetching a new CCW. Fetching a new CCW immediately following the completion of the previous CCW is called *chaining*. (Chaining is described in more detail in the *IBM System/370 Principles of Operation*, the *IBM System/370 Extended Architecture Principles of Operation* and the *IBM Enterprise Systems Architecture/370 Principles of Operation*.) CCWs located in contiguous areas of central storage (successive doubleword locations) can be chained. Chains of CCWs located in noncontiguous storage areas can be coupled for chaining purposes by using a Transfer in Channel command. All CCWs Interruptionsfer to the I/O device specified in the original instruction. The type of chaining (data or command) is specified by chain-data and chain-command flag bits in the CCW.

Data Chaining

When the data transfer specified by the current CCW is finished, data chaining causes the operation to continue by fetching a new CCW and using the storage area defined by the new CCW. Execution of the operation at the I/O device is not affected.

Command Chaining

Each time a new CCW is fetched during command chaining, a new I/O operation is specified. The new operation is initiated when the device end signal for the current operation is received, unless suspension is specified in the new CCW. When command chaining takes place, the completion of the current operation does not cause an I/O interruption.

I/O Interruptions

I/O interruptions report the completion of I/O operations to the CPs and also report error and time-out conditions.

Ending status information about the operation is available to the control program at the end of the I/O operation. When an I/O operation is completed, an I/O interruption request is sent to a central processor. When the request is honored, an I/O interruption occurs and places the central processor under control of the I/O new program status word (PSW). Until an I/O interruption condition is honored, it is called a pending I/O interruption.

Errors detected by the channel subsystem are reported to the CPs as I/O interruptions or machine-check interruptions. I/O interruptions report the following hardware-related conditions:

- Interface control check (IFCC); for example, interface tag errors and time-outs
- Channel control check (CCC); for example, parity, decode, or control errors
- Channel data check (CDC); for example, a parity error detected in central storage

Machine-check interruptions include the following:

- Unrecoverable errors (retry is unsuccessful)
- Persistent errors (retry can be attempted, but the error threshold is exceeded)
- Serious channel element errors that require immediate reporting or cannot be reported as an IFCC or CCC with an I/O interruption

Figure 2-1 shows the machine-check interruption code (MCIC).

Mode			
S/370	ESA/370 370-XA	MCIC Bit	Meaning
X	X	0	System damage
X	X	1	Instruction processing damage
X	X	2	System recovery
X	NA	3	Interval timer damage
X	X	4	Timing facility damage
X	NA	5	External damage
X	X	6	Vector facility failure
NA	X	9	Channel report pending
X	X	10	Service-processor damage
NA	X	11	Channel subsystem damage
X	X	13	Vector facility source
X	X	14	Backed up
X	X	16	Storage error uncorrected
X	X	17	Storage error corrected
X	X	18	Storage key error uncorrected
X	X	19	Storage degradation
X	X	20	PSW-EMWP validity
X	X	21	PSW mask and key validity
X	X	22	PSW program mask and condition code validity
X	X	23	PSW instruction address validity
X	X	24	Failing storage address validity
X	NA	26	External damage code validity
X	X	27	Floating-point register validity
X	X	28	General register validity
X	X	29	Control register validity
X	X	31	Storage logical validity
X	X	32	Indirect storage error
X	X	34	Delayed access exception
X	X	46	CPU timer validity
X	X	47	Clock comparator validity

Legend:

NA Not active for this mode of operation
X Active for this mode of operation

Figure 2-1. Machine-Check Interruption Code (MCIC)

Resets

An I/O system reset is issued to all channels, and the channels signal a system reset to all attached I/O devices. An I/O system reset:

- Stops all subchannel operations
- Resets interruptions and status in all subchannels

An I/O system reset occurs as part of:

- Channel subsystem power-on reset
- Initial program load
- Program reset (S/370 mode only); I/O system reset is performed only by channels currently connected to the CP performing the program reset)
- System reset

A channel issues a selective reset to a specific I/O device in response to an IFCC or CCC. The status of the specific device is reset.

Channel Implementation

Each I/O interface may attach as many as eight control units and can address as many as 256 I/O devices. As many as 16 control units can be attached to an I/O interface using a switching unit (such as an IBM 3814 Switching Management System).

Models 280E, 400, 400E, 500E, and 600E can have eight channels (four on each side) configured as byte-multiplexer channels. If the PR/SM feature is installed, Models 280E, 400E, 500E, and 600E can have as many as 16 channels (eight on each side) configured as byte-multiplexer channels. All other 3090 models can have four channels configured as byte-multiplexer channels. All other channels can be configured as block-multiplexer channels.

Multiplexing refers to the capability a channel and device have to disconnect and reconnect during an operation. Block multiplexing takes place between blocks of data, and byte multiplexing takes place between either bytes of data or groups of bytes of data.

Channel Time-Out

Each channel path has I/O interface time-out functions that time the control unit delays in completing the following I/O interface sequences:

- A 6-second time-out for all selection and status presentation sequences. A time-out occurs if the sequence is not complete within 6 seconds.
- A 30-second time-out for data transfer. A time-out occurs if a byte of data is not transferred within 30 seconds.

If a time-out occurs, the channel terminates the I/O request to the control unit and generates an IFCC interruption.

The time-out function detects malfunctions in control units and I/O devices that can cause the channel path to be unusable to other control units and I/O devices. The time-out function is specified as active or inactive for a device by the IOCP when the IOCDS is created.

Device Priority on a Channel

Device priority on the I/O interface of a channel is in the order of attachment. If the devices are connected to the 'select out' line, the first device has the highest priority. If the devices are attached to the 'select in' line, the priority sequence is reversed. Devices attached to the 'select out' line have priority over devices attached to the 'select in' line. (See Figure 2-2 on page 2-11.)

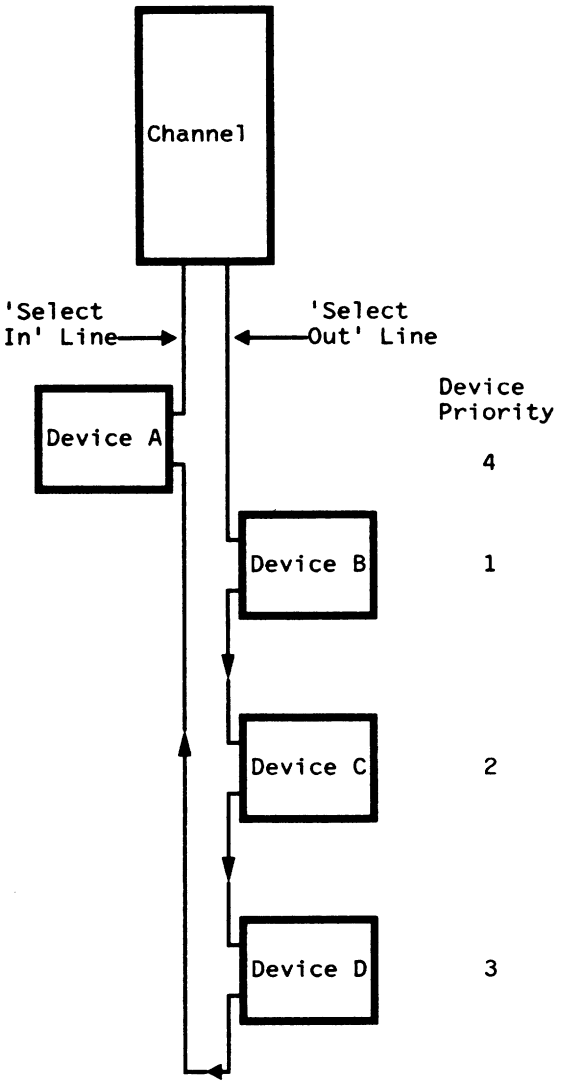

Figure 2-2. Device Priority on a Channel

Dynamic Reconnection

In 370-XA and ESA/370 modes, the channel subsystem permits dynamic reconnection of I/O devices that have the dynamic-reconnection feature installed and that are set up to operate in a multipath mode, such as the IBM 3380 Direct Access Storage Model AA4. Dynamic reconnection allows the device to reconnect and continue a chain of I/O operations using the first available channel path (one of as many as four possible channel paths defined in an IOCP parameter). The selected path is not necessarily the one used initially in the I/O operation.

Chapter 3. Channel Performance Characteristics

Maximizing channel subsystem performance is an important consideration in configuring I/O devices to a 3090 Processor Complex. Channel subsystem performance depends on the following factors:

- Attached device characteristics, such as data transfer rates, I/O interface control signal timings, byte-multiplexer channel burst sizes, channel utilization efficiency, device class, and device critical times
- Physical attachment configuration of the I/O control units to the I/O interfaces, including cable lengths
- Channel program characteristics, such as the number and type of chained commands, use of indirect data addressing, boundary alignment, block size, data chaining, and error-recovery programs
- Internal load, involving channel control element activity and the storage bus

Channel Performance Concepts

Performance-related factors that should be considered in configuring channels include:

- Elapsed time
- Deferred access
- Device class

Elapsed Time

The elapsed time to complete service for an I/O device connected to a channel consists of:

- Channel service time
- Higher priority time
- Lower priority time

Channel service time for the device includes the device tag time, the cable propagation time, the channel busy time to service the requested control sequence, and the wait time for channel resources.

Higher priority time is the wait time for service to a particular device because of the summation of channel service times of all higher priority devices requesting service and connected to the same channel.

Lower priority time is the wait time for service to a particular device because of the completion of the channel service time of a lower priority device connected to the same channel.

The sum of these three times is the elapsed time to service a device request. Conceptually, these elapsed time events occur in the following sequence: lower priority time, higher priority time, channel service time.

Figure 3-1 on page 3-3 illustrates elapsed time on a byte-multiplexer channel. This time includes service from the byte-multiplexer channel and contention delays for the channel. Contention delays for the byte-multiplexer channel are the lower priority time delays and the higher priority time delays. The lower priority time delay is the time that device 4 (a lower priority device or control unit) keeps the channel busy after requesting and receiving channel service just ahead of device 3. The higher priority time delay is the time that devices 1 and 2 (higher priority devices) can keep the channel busy. When device 4 releases the channel, devices 1 and 2 (if ready) receive service before a request by device 3 receives service. Also, if device 3 temporarily releases the path before the I/O operation is complete (disconnected command chaining or transfer of a portion of a buffer in byte multiplex mode of operation), devices 1 and 2 (if ready) can again receive service.

Critical Time

The time that an I/O device can wait for channel service without a negative impact on the performance of the device is called *critical time*. Each I/O device has limits on the elapsed times of various sequences between the device and the channel. When these time limits are not satisfied, device performance may be reduced.

For devices operating on block-multiplexer channels, the control sequences that have the most significant critical-time constraints are those related to chaining operations. For devices operating on byte-multiplexer channels, the time for connecting and disconnecting of the device to the channel for each byte or burst of data sent is the most critical sequence.

In some cases, the time limit is related to synchronized motion (for example, the time between columns on a card moving through an IBM 2501 Card Reader, or the time between the end of a Search ID Equal and the beginning of a Read or Write at an IBM 3380 Direct Access Storage). In each case, a control sequence must be completed within a time limit that relates directly to the physical motion of the device to sustain maximum I/O performance.

In other cases, no synchronized motion is involved; critical time is related to control-unit logic. For example, if a channel is busy when an IBM 3274 Control Unit (the control unit of an IBM 3278 Display Station) is ready to transfer data, the 3274 waits until the channel is ready to begin the data transfer.

Critical times for devices that may be attached to byte-multiplexer channels are listed in Appendix, "Device Class and Critical Time for Byte-Multiplexer Channels" on page A-1.

The critical time of a device can be exceeded because of other traffic on the channel or other traffic in the channel subsystem. Central storage loading can also contribute to the elapsed time, but not significantly. If the elapsed time is greater than the critical time, some performance degradation occurs. The result of exceeding critical time is described under "Deferred Access" and "Device Class" on page 3-4.

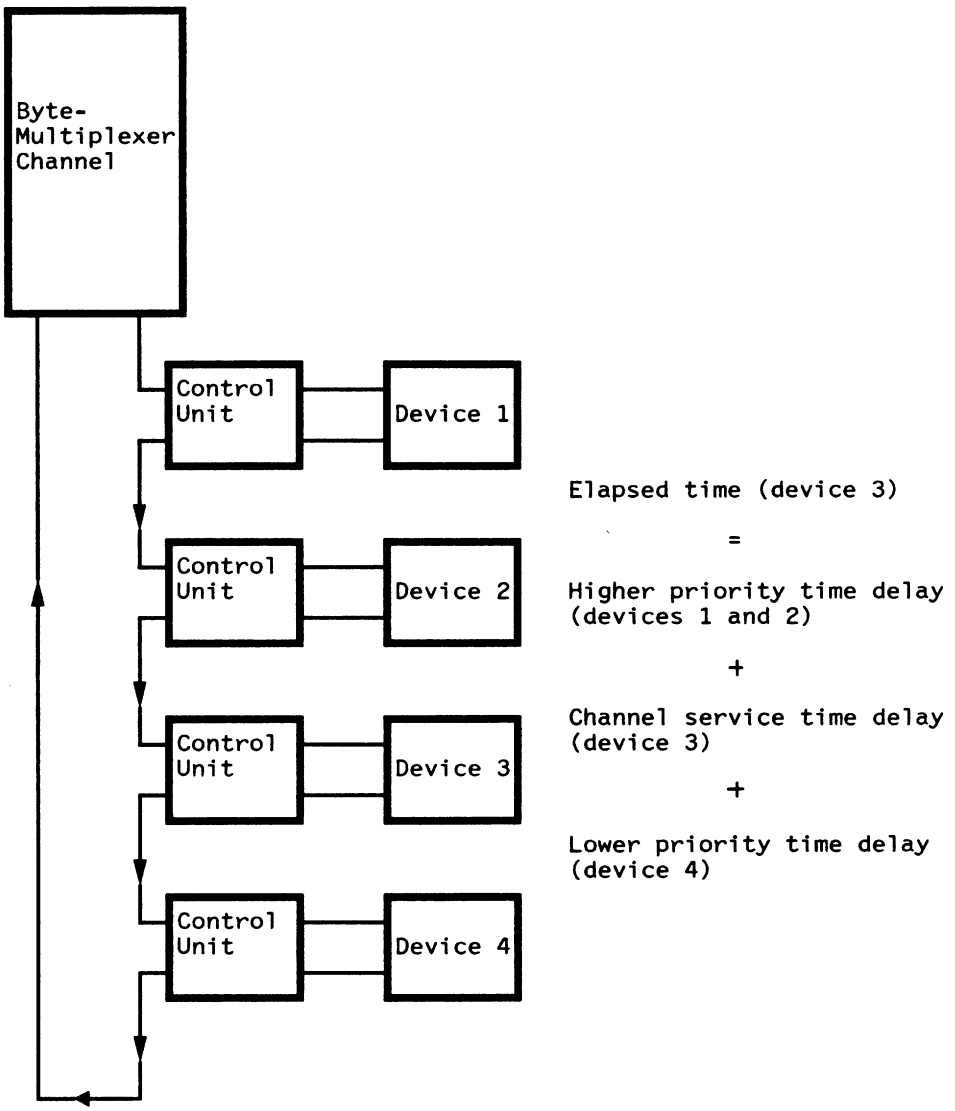

Figure 3-1. Example of Elapsed Time for Device 3

Deferred Access

A **data deferred access** is caused by the inability of the channel to transmit or accept data at the rate requested or transmitted by an I/O device.

A data deferred access is much less likely to occur on buffered devices than on unbuffered devices because buffered devices can wait for channel service. Unbuffered devices (such as start-stop terminals) may have data

deferred accesses when the time required for an error-recovery system logout exceeds the critical time.

Data-chaining operations involving the transfer of one or more blocks of data increase the probability of data deferred accesses with devices that do not respond to 'suppress out'. The probability of deferred accesses occurring during data chaining can be reduced by following the programming recommendations stated in "Data Chaining" on page 4-2.

A **chaining check** is an error detected in a channel when a channel accepts more data (in an input operation) than was specified by the count in the CCW. The check occurs when an I/O data rate is too high to be handled by the channel and storage.

A **command deferred access** is the inability of the channel to present the next command within the critical command-chaining time of a control unit.

Degradation (a loss in performance) can result from a deferred access. A deferred access that requires operator intervention can create significant degradation. In most cases, a deferred access that is handled automatically by retry does not significantly affect throughput.

Depending on the device and the type of deferred access, the operation may be halted when the need for a deferred access occurs, or it may continue transferring data until the end of the block is reached. A deferred access may cause a unit check to be presented to the channel. Any chaining is suppressed and an I/O interruption request is generated at the end of the operation. Certain control units, however, may initiate a command retry sequence without generating an I/O interruption request. See "I/O Interruptions" on page 2-8 for additional information.

Device Class

Devices that can operate in byte multiplex mode of operation are classified by what happens when a device is not serviced within the critical time for the requested control sequence for that device. Depending on how overall channel performance is impacted by the device critical time being exceeded, a device falls into one of three classes: 1, 2, or 3.

Device Class 1

When the critical time is exceeded, a deferred access occurs and the data is not transferred successfully. The consequent error indication causes an I/O interruption request, and program recovery action is required.

For example, data transfer for a 2501 Card Reader has a critical time of 0.462 millisecond (ms). If the 2501 does not receive service from the channel within that time, an error indication occurs, an I/O interruption request is generated, and the operator has to intervene and manually feed the card.

Device Class 2

When the critical time is exceeded, the device must be resynchronized. The additional delay results in performance degradation. The device performance is degraded by the combined delay of waiting for the channel and resynchronization.

For example, the card reader of an IBM 2540 Card Read Punch has a critical time of 6.5 ms. If the channel does not provide service during that time, an additional 20 ms of clutch access time occurs, causing performance degradation. Consequently, the 2540 operates at some speed less than its rated speed of 1000 cards per minute.

Device Class 3

When the critical time is exceeded, the device waits for channel service and causes performance degradation (the delay of waiting for the channel service).

For example, the IBM 4248 Printer can begin printing when its data buffer is full and line spacing is complete. The 4248 has a critical time of 5.2 ms. During this time, the buffer is filled and line spacing occurs. If the channel delays the completion of service past the critical time, performance degradation of the 4248 is limited to the excess of channel service delay over 5.2 ms.

Block Multiplex Mode of Operation

In block multiplex mode of operation, a device stays connected to a channel continuously during the transfer of a full block of data.

Block multiplex mode of operation allows a control unit to present channel end and to disconnect from a channel at the completion of a specified operation. Device end may be presented at a later point. During the interval between channel end and device end, another device attached to the same channel can be started or can complete an operation that is ready. However, if a second device does connect to the same channel during this interval, the first device may find the channel busy (because of the second device) when it tries to reconnect, and then the first device must wait for service.

A channel subsystem provides two modes for block multiplex mode of operation on the I/O interface: interlocked and data streaming.

Interlocked

Operating performance using the interlocked mode depends on overall tag timings (including channel subsystem service), cable length, and control unit service. Block multiplex mode of operation using the interlocked protocol can sustain a nominal data rate of 1.5 megabytes per second.

Data Streaming

The data-streaming protocol does not require interlocking of data transfer signals between the channel and the control unit; once data transfer is established over the interface, it continues at a rate governed by the control unit. Block multiplex mode of operation using the data-streaming protocol can sustain a nominal data rate of 4.5 megabytes per second.

Byte Multiplex Mode of Operation

Byte multiplex mode of operation allows the execution of multiple I/O operations concurrently. Each addressed device is selected, one at a time, for transfer of a byte or a group of bytes to or from central storage. Bytes from multiple devices are interleaved on the channel and routed to or from the desired locations in central storage.

The load that a byte-multiplexer channel can sustain is variable. It is governed by I/O device performance factors such as the data transfer rate, device buffers, number of bytes per data burst on the channel, channel program requirements, synchronized mechanical motion, and priority sequence position on the I/O interface. Byte-multiplexer channel operations are concurrent with block-multiplexer channel operations.

Byte Multiplex Mode and Burst Mode

A byte-multiplexer channel may be monopolized by one I/O device (burst mode) or shared by many I/O devices (byte multiplex mode). The number of bytes transferred at a time in byte multiplex mode may be one (single byte transfers) or more than one (multibyte transfers). Most control units that operate in byte multiplex mode can also operate in burst mode. A manually set switch at the control unit determines whether the control unit operates in burst mode or byte multiplex mode.

Some devices offer a choice of specifying how many bytes are transferred during a single data transfer sequence in byte multiplex mode. For example, an IBM 3211 Printer can specify either burst mode or byte multiplex mode with 1-byte or 6-byte transfers. Because most of the time spent in a data-transfer control sequence is for control, increasing the burst size (the number of bytes transferred per sequence) results in a relatively small increase in the total channel busy time for the sequence. Also, increasing the burst size reduces the number of data transfer sequences required (for example, by a factor of six for a 3211 Printer operating in byte multiplex mode with 6-byte transfers). The net effect is a significant improvement in channel efficiency and a higher allowable data rate.

Burst mode, although most effective in the use of channel resources, may cause another device on the byte-multiplexer channel to exceed its critical time. From the perspective of the control unit, burst mode occurs when the time contributed by the control unit in a transfer sequence is more than 32 microseconds. (See the *IBM System/360 and System/370 I/O Interface Channel to Control Unit OEMI.*) If the device configuration guidelines (in Chapter 4, "Channel Configuration Guidelines" on page 4-1) are followed

for byte-multiplexer channels of a 3090 Processor Complex, deferred accesses are minimized and data transfer sequences exceeding 32 microseconds are acceptable when large burst sizes are specified.

Note: Most class-2 and class-3 devices that can operate in burst mode should be attached to block-multiplexer channels for better performance.

Prospective devices for such attachment are listed in Appendix, "Device Class and Critical Time for Byte-Multiplexer Channels" on page A-1. Rules governing the placement of devices that can operate in byte multiplex or burst mode on one or more byte-multiplexer channels are discussed in Chapter 4, "Channel Configuration Guidelines" on page 4-1.

Buffered I/O Devices

For all configurations, buffered I/O devices are preferable to unbuffered I/O devices. Buffered I/O devices permit more efficient use of channels. A fully buffered device uses the channel when it needs the channel, and waits if the channel is busy. Such implementation provides data-deferred, access-free operation, and reduces the need for intervention by error routines or operators.

For example, the IBM 3505 Card Reader buffers 80 bytes and waits for the channel if the channel is busy. The 3505 is more desirable from a performance viewpoint than the 2501 Card Reader, which buffers only one byte, transfers one byte at a time, and cannot wait beyond critical time for service. Larger bursts of data from buffered devices promote more efficient channel operation.

Another example is the IBM 3705 Communications Controller. The 3705 has software-controlled buffers and can configure, for each communication line, a buffer that is large enough for the individual application.

Chapter 4. Channel Configuration Guidelines

This chapter is intended to assist in the physical placement of the control units connected to the I/O interface of a channel subsystem. The Input/Output Configuration Program (described in "Channel Sets and Logical Channels" on page 2-4) establishes the physical and logical addressing relationships of the I/O devices in the 3090 configuration.

General Device Considerations

In a channel subsystem, all channels have equal priority.

For positional placement of control units on a particular I/O interface, consider the service priority that is obtained from 'select out' or 'select in' tag propagation (see "Device Priority on a Channel" on page 2-10 for more information).

Device Sequence on Block-Multiplexer Channels

To establish the sequence of devices on any channel, consider the following factors.

Device Class. Class-2 devices should have higher priority for service than class-3 devices.

Total System Priorities. Attach the devices (control units) that are most important to system performance first (in the highest priority position).

Channel Service Time. Within a system priority, attach the devices with the shortest channel service time first.

Device Intermix

Although different devices (such as an IBM 3380 Direct Access Storage and an IBM 3800 Printing Subsystem) can share channels, the decision to intermix devices depends on the load imposed on the channel by each device.

Usually, different types of devices should be attached to different channels because of their design and use.

Reasons for separate channel requirements include:

- Type of channel
- Paging and response time
- Random versus sequential records (such as disk versus tape)

- Chained records (such as tape or disk)
- Logging
- Different critical times
- Number of devices
- Channel utilization

For example, to improve system performance, the following types of devices should be on separate block-multiplexer channels:

- Direct-access storage devices (such as the IBM 3380 Direct Access Storage)
- Tape devices (such as the IBM 3480 Magnetic Tape Subsystem)

Data Chaining

Data chaining can put a very heavy load on the channel. Factors affecting channel loading include:

- Data address alignment
- Low CCW byte counts
- High device-data rates
- Other channel activity within the channel subsystem
- Additional central storage accesses for CCWs during device data transfer

Because of these factors, data deferred accesses and chaining checks can occur when data is chained during data transfer sequences. Two programming recommendations help minimize the probability of these two problems:

- If the device or control unit responds to the suppress-out tag and suppresses data transfers, make the minimum CCW byte count greater than the number of bytes or byte requests in transit on the I/O interface cable. This number is variable; it depends on the cable length, the data transfer rate, and the protocol. With the interlocked protocol, no minimum byte count exists. With the data-streaming protocol, specifying a minimum byte count of 16 covers all combinations of local cable lengths and data transfer rates.

  Note: If a channel extender (using the IBM 3044 Fiber-Optic Channel Extender Link) is used, the minimum byte count is four times the cable length (measured in thousands of feet) times the data rate (measured in megabytes per second).

- If the device or control unit does not suppress data transfer, specify byte counts to be no less than 54 times the device instantaneous data rate (a maximum data rate of 4.5 megabytes per second) and put data addresses on doubleword or (preferably) quadword boundaries.

No minimum byte count restrictions exist for data chaining within gaps of a direct-access storage device record (that is, gaps between count, key, and data fields).

Byte-Multiplexer Channel Analysis

As stated in "Byte Multiplex Mode and Burst Mode" on page 3-6, many class-2 and class-3 devices can operate efficiently in burst mode on *block-multiplexer* channels. Before attempting to configure any such devices on byte-multiplexer channels, place as many of these devices as possible on block-multiplexer channels (see Appendix, "Device Class and Critical Time for Byte-Multiplexer Channels" on page A-1 for the list of devices). This reduces the contention of the devices remaining on byte-multiplexer channels. Next, ensure that devices with a variable burst size capability are set for large burst size. Finally, balance the device load across the available byte-multiplexer channels and sequence the devices within these channels (as described in "Balancing Device Load across Channels").

Balancing Device Load across Channels

To balance the device load across the channels, consider the following factors, in decreasing order of priority:

Burst Size. Try to configure I/O devices that are small burst devices (1, 2, 3, or 6 bytes per transfer) to one or more byte-multiplexer channels, and all large burst devices (16 or 32 bytes per transfer) to other byte-multiplexer channels. Class-1 devices should be distributed among the channels that attach small burst devices.

Critical Time. When possible, configure each byte-multiplexer channel with both short and long critical time devices.

For example, if two I/O devices have short critical times, put each device on a separate byte-multiplexer channel. If multiple devices (such as terminals) with different critical times attach to the same control unit, configure the control units according to the device with the shortest critical time.

Data Rate. Data rate balancing across multiple byte-multiplexer channels should be done where no conflict exists with class-1 and critical-time considerations.

Availability. Standard guidelines for availability, which provide for alternate paths, should be followed.

Sequencing Devices within a Channel

To sequence the devices (control units that have the most critical I/O devices) within a channel, consider the following factors.

Device Class. Attach class-1 devices first, class-2 devices next, and class-3 devices last. For information on:

- Class specifications, see "Device Class" on page 3-4.
- Device class by I/O device, see Appendix, "Device Class and Critical Time for Byte-Multiplexer Channels" on page A-1.

Increasing Critical Time. Within a class, the device with the shortest critical time has the highest priority. (See Appendix, "Device Class and Critical Time for Byte-Multiplexer Channels" on page A-1 for critical times.) For devices having the same critical time, attach the device with the smallest burst size first. A communications controller with several lines having short critical times should be ahead of a communications controller with one line having a short critical time. Devices operating in burst mode and connected to a byte-multiplexer channel should be given lowest attachment priority.

Appendix. Device Class and Critical Time for Byte-Multiplexer Channels

This appendix shows the device class and critical time for devices that may be attached to byte-multiplexer channels.

See "Critical Time" on page 3-2 for more information.

Device Class 1

Device	Critical Time (ms)
2501 Card Reader	0.462
2701 Data Adapter Unit	(See Note 1)
3704 Communication Controller	(See Note 2)
3705 Communication Controller	(See Note 2)
3720 Communication Controller	(See Note 2)
3725 Communication Controller	(See Note 2)

Notes:

1. See "Estimating Line Critical Time for a 2701" on page A-3.
2. See "Estimating Line Critical Time for a Communication Controller in Emulation Mode" on page A-3.

Device Class 2

Device	Critical Time (ms)
2540 Card Read Punch (Reader)[1]	6.50
2540 Card Read Punch (Punch)[1]	14.00
3525 Card Punch[1]	67.50 (Model P1) 33.20 (Model P2) 22.50 (Model P3)

[1]Recommended device for attachment to a block-multiplexer channel. Attaching devices that operate efficiently on block-multiplexer channels reduces contention of devices remaining on byte-multiplexer channels.

Device Class 3

Device	Critical Time (ms)
1403 Printer[1]	15.70
3174 Subsystem Control Unit Model 1L[1]	Not applicable
3203 Printer Model 5[1]	8.00
3211 Printer[1]	7.08
3262 Line Printer Model 5	60.00
3272 Control Unit[1]	Not applicable
3274 Control Unit[1]	Not applicable
3505 Card Reader[1]	9.00 (Model B1) 6.00 (Model B2)
3704 Communications Controller[1]	Not applicable (NCP mode)
3705 Communications Controller[1]	Not applicable (NCP mode)
3720 Communication Controller[1]	Not application (NCP mode)
3725 Communication Controller[1]	Not applicable (NCP mode)
3790 Communication System	Not applicable
3800 Printing Subsystem[1]	2.85 (12 lines per inch) 4.27 (8 lines per inch) 5.70 (6 lines per inch)
3851 Mass Storage Facility	Not applicable
3890 Document Processor[1]	360.0
4245 Line Printer	25.0
4248 Printer	5.2

[1]Recommended device for attachment to a block-multiplexer channel. Attaching devices that operate efficiently on block-multiplexer channels reduces contention of devices remaining on byte-multiplexer channels.

Estimating Line Critical Time for a 2701

The critical time for each line is determined as follows:

$$\text{Critical time (ms)} = \frac{\text{Buffer constant} \times 1000}{\text{Line speed (bps)}} \; E$$

where E is the emulation-program time in ms.

The buffer constant is determined according to the type of adapter used:

Adapter Type	Buffer Constant
IBM terminal adapter type I or II	8.5
Telegraph adapter type I	6.5
Telegraph adapter type II	9.5
Synchronous data adapter type I	7.0
Synchronous data adapter type II	
Six-bit with automatic polling	6.5
Six-bit without automatic polling	11.5
Eight-bit with automatic polling	8.5
Eight-bit without automatic polling	15.5

Estimating Line Critical Time for a Communication Controller in Emulation Mode

Critical time for a communication controller operating in emulation mode is developed on a per-line basis. In general, the attachment position chosen for a communication controller should follow standard guidelines for critical time. Choose the shortest critical time in each communication controller.

The steps for calculating an approximate critical time are:

1. For a 3704 or a 3705, determine the buffer constant for each line by the type of communication scanner (1, 2, or 3), the line speed, and the size of the emulation program (software) buffer.

   Notes:

   a. Using 167 assumes a BUILD macro specification of OPCSB2 = YES or a LINE macro specification of CHNPRI = HIGH with a type-4 channel adapter. Otherwise, use 39 or 43, as appropriate.

   b. In the algebraic expression 71 + 8S, S represents the size of the software buffer, which can be 4, 8, 16, 32, 64, 96, 128, 160, 192, or 224 bytes. For line speeds greater than 19200 bps, the default size of the buffer is 64 bytes; otherwise, it is 32 bytes. The size of the software buffer is chosen when the emulation program is generated.

For the 3720 or 3725, determine the buffer constant for each line using the line speed, the size of the emulation program (software) buffer, and the table that follows.

CSP Mode	Line Mode or Line Speeds	Buffer Constant (Note c)
Emulation	Bisynchronous	71
Emulation	Start/stop	80
Emulation	Start/stop burst mode	116
Emulation	High-speed start/stop	44 + 36S (Note a)
Emulation	High-speed start/stop burst mode	80 + 36S (Note a)
Normal	Bisynchronous <50 kb/s Synchronous	519 + 8S (Note b)
Normal	Bisynchronous 50 kb/s	2055 + 8S (Note b)

Notes:

a. For the 3720 or 3725, specifying BUFETTE=n for a value greater than n=2 causes the generation process to provide n*4-BYTE buffers, up to 255. For the purpose of this calculation S = n-1. If n = 2, use the value of 71, 80, or 116 instead of the algebraic equation. These values represent a 4-byte control program buffer plus the Communication Scanner Processor (CSP) buffering capability for the various line protocols.

b. For normal mode lines, S represents the BUFSIZE=parameter on the LINE statement at generation time. BUFSIZE may be specified in even numbers from 4 to 254. The default value is 64. The 512 and 2048 figures represent the capability of the CSP to buffer as many as 64 characters (256 characters, in the case of a high-speed line) for transfer to the control program, plus 7 bits of the next character from the line.

   If the data is received over a line for which a host Read command is not outstanding, the critical time is confined to the buffering capability of the CSP. The control program buffers are not used.

c. The buffer constant is a calculation of the maximum number of character bits that may be received over the line (assuming one buffer is allocated to the channel adapter and the rest of the buffers are available to the CSP) before an overrun occurs. The shortest character configuration (9/7 bits) was used for these figures.

2. Calculate the critical time (in ms) for each line.

$$\text{Critical time (ms)} = \frac{\text{Buffer constant} \times 1000}{\text{Line speed (bps)}} E$$

where E is the emulation-program time in ms.

For a 3704 and a 3705, the time taken by the emulation program depends on the type of communication scanner and the line speed, as follows:

Scanner Type	Line Speeds (bps)	Emulation Program Time (ms)
1	All	0.270
2 or 3	< 4800	0.402
2 or 3	4800 to 9600	0.306
2 or 3	> 9600	0.242

For the 3720 or 3725, use one of the following values for emulation program time:

Mode	ms
Normal	0.250
Emulation	0.210

Attach the communication controller with the shortest critical time communication line first (in the highest priority position).

A communication controller with several lines having short critical times should be placed ahead of a communication controller with one line having a short critical time.

Glossary of Terms and Abbreviations

See the Index or *IBM Dictionary of Computing*, SC20-1699, for terms that do not appear in this glossary.

acronym. A special type of abbreviation in which the characters chosen to abbreviate the word or words deliberately spell a word (as in RAM, COBOL, or BASIC.

address. An identification of a storage location or an I/O device.

bit. Binary digit.

bps. Bits per second.

BTAM. Basic telecommunications access method.

CAW. Channel address word (S/370).

CCC. Channel control check.

CCE. Channel control element.

CCW. Channel command word.

CDC. Channel data check.

central storage. Includes both main storage (programs and data) and the hardware system area (not addressable by programming).

chaining. The fetching of a new CCW immediately following the completion of the previous CCW.

channel. Each channel in the channel subsystem controls an I/O interface between the channel control element and the attached control units.

channel control element (CCE). The channel control element in the channel subsystem provides the interface between the channels and the rest of the 3090 system.

channel set. A group of channels that are assigned to a specific central processor in the 3090 Processor Complex. Channel sets apply only when the 3090 is operating in S/370 mode.

channel subsystem (CSS). The channel subsystem is responsible for all I/O operations.

CHE. Channel element.

CHN. Channel.

CHPID. Channel path identifier.

CLRCH. Clear Channel (S/370 I/O instruction).

CLRIO. Clear I/O (S/370 I/O instruction).

CP. Central processor (as in CP1, CP2).

CPU. Central processing unit.

| **CSCH.** Clear Subchannel (370-XA and ESA/370 I/O
| instruction).

CSS. Channel subsystem.

CSW. Channel status word.

CU. Control unit.

DASD. Direct-access storage device.

ECC. Error checking and correction.

| **ESA/370.** Enterprise Systems Architecture/370.

expanded storage. Optional integrated high-speed storage that transfers 4K-byte pages to and from central storage.

hardware system area (HSA). A logical area of central storage that is used to store microcode, instructions, and control information (not addressable by application programs).

HDV. Halt Device (S/370 I/O instruction).

hex. Hexadecimal.

HIO. Halt I/O (S/370 I/O instruction).

HSA. Hardware system area.

| **HSCH.** Halt Subchannel (370-XA and ESA/370 I/O
| instruction).

Hz. Hertz.

ID. (1) Identifier. (2) Identification.

IFCC. Interface control check.

IML. Initial microprogram load.

IMS. Information Management System.

initialization. To set counters, switches, addresses, latches, or storage contents to 0 or to other starting values at the beginning of, or at the prescribed points in, a computer program or process.

I/O. Input/output.

I/O Configuration Program (IOCP). Defines for the channel subsystem all of the I/O devices and all of the available channel paths.

I/O interface. The I/O interface connects channels and control units for the exchange of signals and data.

IOCDS. I/O configuration data set.

IOCP. I/O Configuration Program.

IPL. Initial program load.

JES. Job entry subsystem.

kb/s. Kilobytes per second.

M-byte. Megabyte; 1 048 576 bytes.

MCIC. Machine-check interruption code.

megabyte. 1 048 576 bytes.

ms. Millisecond.

MSCH. Modify Subchannel (370-XA and ESA/370 I/O instruction).

multiplexing. The ability of the channel and the device to disconnect and reconnect during an operation.

MVS/SP. Multiple Virtual Storage/System Product.

NCP. Network control program.

OEMI. Original equipment manufacturers' information.

offline. Pertains to resources with which the processor unit has no direct communication or control.

online. Pertains to resources with which the processor unit has direct communication or control.

PCDU. Power and coolant distribution unit.

port. An access point for data entry or exit.

processor complex. A configuration comprising the:

- Processor unit
- Processor controller
- System display
- Service support display
- Power and coolant distribution unit

processor controller. Provides support and diagnostic functions for the processor complex.

PR/SM. Processor Resource/Systems Manager.

PSW. Program status word.

RCHP. Reset Channel Path (370-XA and ESA/370 I/O instruction).

RIO. Resume I/O (S/370 I/O instruction).

RMF. Resource Management Facility.

RSCH. Resume Subchannel (370-XA and ESA/370 I/O instruction).

RTAM. Remote terminal access method.

S/370. System/370.

SAL. Set Address Limit (370-XA and ESA/370 I/O instruction).

SCE. System control element.

SCH. Subchannel.

SCHM. Set Channel Monitor (370-XA and ESA/370 instruction).

SIO. Start I/O (S/370 I/O instruction).

SIOF. Start I/O Fast Release (S/370 I/O instruction).

SSCH. Start Subchannel (370-XA and ESA/370 I/O instruction).

STCPS. Store Channel Path Status (370-XA and ESA/370 I/O instruction).

STCRW. Store Channel Report Word (370-XA and ESA/370 I/O instruction).

STIDC. Store Channel ID (S/370 I/O instruction).

storage key. A control field associated with a defined block of storage that protects that block of storage from unauthorized access and change.

STSCH. Store Subchannel (370-XA and ESA/370 I/O instruction).

subchannel (SCH). The channel facilities required to perform an I/O operation.

synchronous I/O operation. An I/O operation that requires the channel subsystem to signal a release to the central processor that initiated the operation.

system. Comprises the processor complex and all attached and configured I/O and communication devices.

system control element (SCE). Handles the transfer of data and control information associated with storage requests between the elements of the processor complex.

TCAM. Telecommunications access method.

TCH. Test Channel (S/370 I/O instruction).

TIC. Transfer in Channel command.

TIO. Test I/O (S/370 I/O instruction).

TPI. Test Pending Interruption (370-XA and ESA/370 I/O instruction).

TSCH. Test Subchannel (370-XA and ESA/370 I/O instruction).

UCW. Unit control word.

VM/SP. Virtual Machine/System Product.

VTAM. Virtual telecommunications access method.

370-XA. System/370 extended architecture.

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Bibliography

The following publications provide additional information about 3090 Processor Complex functions and operations:

GA22-6974 *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information*

GA22-7000 *IBM System/370 Principles of Operation*

GA22-7002 *IBM System/370 Input/Output Configurator*

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SC38-0038 *IBM 3090 Processor Complex: Input/Output Configuration Program User's Guide and Reference*

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| SC38-0062 *IBM 3090 Processor Complex Model 280E: Operator Tasks for the System Console*

| (to be available at a later date) *IBM Enterprise Systems Architecture/370 Principles of Operation*

| (to be available at a later date) *IBM 3090 Processor Complex: Processor Resource/Systems Manager Planning Guide*

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