System/370 Reference Summary

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This edition is a major revision and makes obsolete the previous edition, GX20-1850-4. Additions include new printer, tape, and DASD command codes. Minor technical and editorial revisions have been made throughout.

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PREFACE

This publication is intended primarily for use by S/370 assembler language application programmers. It contains basic machine information summarized from the *System/370 Principles of Operation* (GA22-7000) about System/370 Models 115 through 195; the 3031, 3032, 3033, 3081, 3083, and 3084 Processor Complexes; and the 4321, 4331, 4341, 4361, and 4381 Processors. It also contains frequently used information from the OS/VS, DOS/VSE, and VM/370 assembler language manual (GC33-4010), command codes for various I/O devices, and a multi-code translation table. This publication will be updated from time to time. However, the above manuals and others cited in this booklet are the authoritative reference sources and will be first to reflect changes.

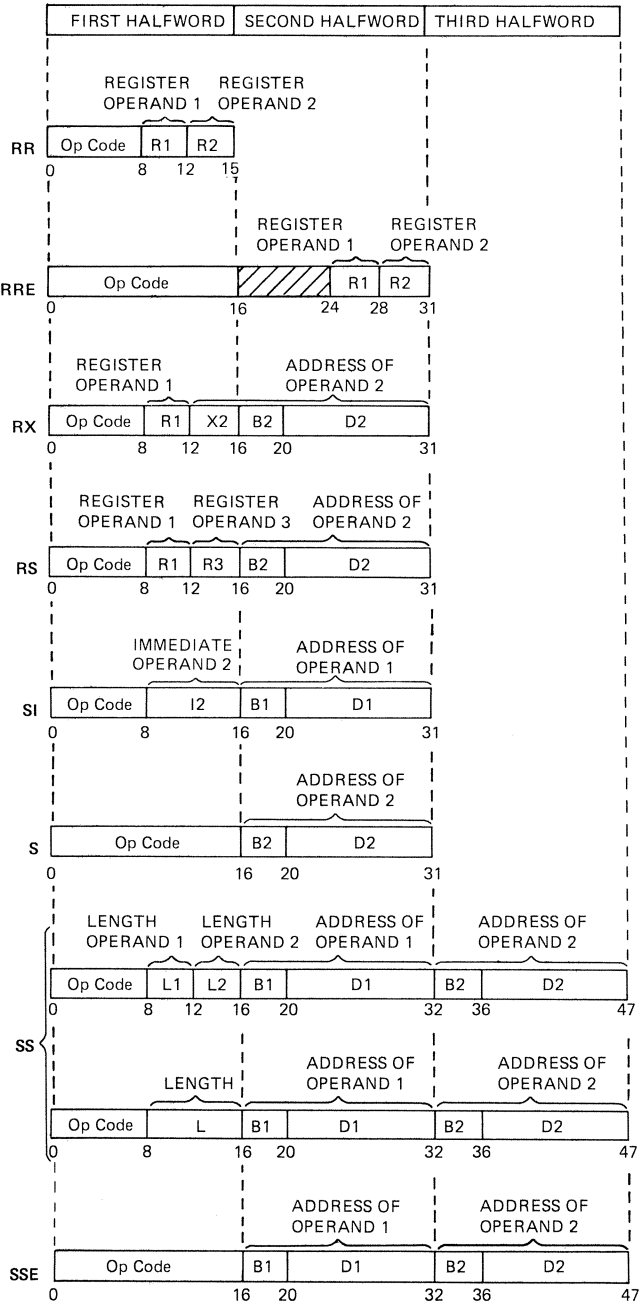
The floating-point and extended-precision floating-point instructions, as well as the instructions listed below, are not provided on every model. For instructions that are provided on a particular model, either as standard or optional features on that model, the user should refer to the appropriate System Library manual.

Facility	**Instructions**
Branch and save	BAS, BASR
Channel-set switching	CONCS, DISCS
Conditional swapping	CS, CDS
CPU timer and clock comparator	SCKC, SPT, STCKC, STPT
Direct control	RDD, WRD
Dual address space	EPAR, ESAR, IAC, IVSK, LASP, MVCP, MVCS, MVCK, PC, PT, SAC, SSAR
Extended facility	IPTE, TPROT
Move inverse	MVCIN
Multiprocessing	SPX, SIGP, STAP, STPX
PSW-key handling	IPK, SPKA
Storage-key-instruction extensions	ISKE, RRBE, SSKE
Suspend and resume	RIO
Test block	TB
Translation	LRA, PTLB, RRB, STNSM, STOSM

The operation of the following I/O instructions may differ depending on the model, the designated channel, and the installed facilities: CLRCH, CLRIO, HDV, and SIOF. To determine the operation, the user should refer to the appropriate System Library manual.

CONTENTS

MACHINE INSTRUCTION FORMATS



MACHINE INSTRUCTIONS

Name	Mnemonic	OP Code	For-mat	Operands
Add (c)	AR	1A	RR	R1,R2
Add (c)	A	5A	RX	R1,D2(X2,B2)
Add Decimal (c)	AP	FA	SS	D1(L1,B1),D2(L2,B2)
Add Halfword (c)	AH	4A	RX	R1,D2(X2,B2)
Add Logical (c)	ALR	1E	RR	R1,R2
Add Logical (c)	AL	5E	RX	R1,D2(X2,B2)
AND (c)	NR	14	RR	R1,R2
AND (c)	N	54	RX	R1,D2(X2,B2)
AND (c)	NI	94	SI	D1(B1),I2
AND (c)	NC	D4	SS	D1(L,B1),D2(B2)
Branch and Link	BALR	05	RR	R1,R2
Branch and Link	BAL	45	RX	R1,D2(X2,B2)
Branch and Save	BASR	0D	RR	R1,R2
Branch and Save	BAS	4D	RX	R1,D2(X2,B2)
Branch on Condition	BCR	07	RR	M1,R2
Branch on Condition	BC	47	RX	M1,D2(X2,B2)
Branch on Count	BCTR	06	RR	R1,R2
Branch on Count	BCT	46	RX	R1,D2(X2,B2)
Branch on Index High	BXH	86	RS	R1,R3,D2(B2)
Branch on Index Low or Equal	BXLE	87	RS	R1,R3,D2(B2)
Clear Channel (c,p)	CLRCH	9F01	S	D2(B2)
Clear I/O (c,p)	CLRIO	9D01	S	D2(B2)
Compare (c)	CR	19	RR	R1,R2
Compare (c)	C	59	RX	R1,D2(X2,B2)
Compare and Swap (c)	CS	BA	RS	R1,R3,D2(B2)
Compare Decimal (c)	CP	F9	SS	D1(L1,B1),D2(L2,B2)
Compare Double and Swap (c)	CDS	BB	RS	R1,R3,D2(B2)
Compare Halfword (c)	CH	49	RX	R1,D2(X2,B2)
Compare Logical (c)	CLR	15	RR	R1,R2
Compare Logical (c)	CL	55	RX	R1,D2(X2,B2)
Compare Logical (c)	CLI	95	SI	D1(B1),I2
Compare Logical (c)	CLC	D5	SS	D1(L,B1),D2(B2)
Compare Logical Characters under Mask (c)	CLM	BD	RS	R1,M3,D2(B2)
Compare Logical Long (c)	CLCL	0F	RR	R1,R2
Connect Channel Set (c,p)	CONCS	B200	S	D2(B2)
Convert to Binary	CVB	4F	RX	R1,D2(X2,B2)
Convert to Decimal	CVD	4E	RX	R1,D2(X2,B2)
Diagnose (p)		83		Model-dependent
Disconnect Channel Set (c,p)	DISCS	B201	S	D2(B2)
Divide	DR	1D	RR	R1,R2
Divide	D	5D	RX	R1,D2(X2,B2)
Divide Decimal	DP	FD	SS	D1(L1,B1),D2(L2,B2)
Edit (c)	ED	DE	SS	D1(L,B1),D2(B2)
Edit and Mark (c)	EDMK	DF	SS	D1(L,B1),D2(B2)
Exclusive OR (c)	XR	17	RR	R1,R2
Exclusive OR (c)	X	57	RX	R1,D2(X2,B2)
Exclusive OR (c)	XI	97	SI	D1(B1),I2
Exclusive OR (c)	XC	D7	SS	D1(L,B1),D2(B2)
Execute	EX	44	RX	R1,D2(X2,B2)
Extract Primary ASN (s)	EPAR	B226	RRE	R1
Extract Secondary ASN (s)	ESAR	B227	RRE	R1
Halt Device (c,p)	HDV	9E01	S	D2(B2)
Halt I/O (c,p)	HIO	9E00	S	D2(B2)
Insert Address Space Control (c,s)	IAC	B224	RRE	R1
Insert Character	IC	43	RX	R1,D2(X2,B2)
Insert Characters under Mask (c)	ICM	BF	RS	R1,M3,D2(B2)
Insert PSW Key (s)	IPK	B20B	S	
Insert Storage Key (p)	ISK	09	RR	R1,R2
Insert Storage Key Extended (p)	ISKE	B229	RRE	R1,R2

c. Condition code is set
n. New condition code is loaded
p. Privileged instruction
s. Semiprivileged instruction
x. Extended-precision floating-point

MACHINE INSTRUCTIONS (Cont'd)

Name	Mnemonic	OP Code	For-mat	Operands
Insert Virtual Storage Key (s)	IVSK	B223	RRE	R1,R2
Invalidate Page Table Entry (p)	IPTE	B221	RRE	R1,R2
Load	LR	18	RR	R1,R2
Load	L	58	RX	R1,D2(X2,B2)
Load Address	LA	41	RX	R1,D2(X2,B2)
Load Address Space Parameters (c,p)	LASP	E500	SSE	D1(B1),D2(B2)
Load and Test (c)	LTR	12	RR	R1,R2
Load Complement (c)	LCR	13	RR	R1,R2
Load Control (p)	LCTL	B7	RS	R1,R3,D2(B2)
Load Halfword	LH	48	RX	R1,D2(X2,B2)
Load Multiple	LM	98	RS	R1,R3,D2(B2)
Load Negative (c)	LNR	11	RR	R1,R2
Load Positive (c)	LPR	10	RR	R1,R2
Load PSW (n,p)	LPSW	82	S	D2(B2)
Load Real Address (c,p)	LRA	B1	RX	R1,D2(X2,B2)
Monitor Call	MC	AF	SI	D1(B1),I2
Move	MVI	92	SI	D1(B1),I2
Move	MVC	D2	SS	D1(L,B1),D2(B2)
Move Inverse	MVCIN	E8	SS	D1(L,B1),D2(B2)
Move Long (c)	MVCL	0E	RR	R1,R2
Move Numerics	MVN	D1	SS	D1(L,B1), D2(B2)
Move to Primary (c,s)	MVCP	DA	SS	D1(R1,B1),D2(B2),R3
Move to Secondary (c,s)	MVCS	DB	SS	D1(R1,B1),D2(B2),R3
Move with Key (c,s)	MVCK	D9	SS	D1(R1,B1),D2(B2),R3
Move with Offset	MVO	F1	SS	D1(L1,B1),D2(L2,B2)
Move Zones	MVZ	D3	SS	D1(L,B1),D2(B2)
Multiply	MR	1C	RR	R1,R2
Multiply	M	5C	RX	R1,D2(X2,B2)
Multiply Decimal	MP	FC	SS	D1(L1,B1),D2(L2,B2)
Multiply Halfword	MH	4C	RX	R1,D2(X2,B2)
OR (c)	OR	16	RR	R1,R2
OR (c)	O	56	RX	R1,D2(X2,B2)
OR (c)	OI	96	SI	D1(B1),I2
OR (c)	OC	D6	SS	D1(L,B1),D2(B2)
Pack	PACK	F2	SS	D1(L1,B1),D2(L2,B2)
Program Call (s)	PC	B218	S	D2(B2)
Program Transfer (s)	PT	B228	RRE	R1,R2
Purge TLB (p)	PTLB	B20D	S	
Read Direct (p)	RDD	85	SI	D1(B1),I2
Reset Reference Bit (c,p)	RRB	B213	S	D2(B2)
Reset Reference Bit Extended (c,p)	RRBE	B22A	RRE	R1,R2
Resume I/O (c,p)	RIO	9C02	S	D2(B2)
Set Address Space Control (s)	SAC	B219	S	D2(B2)
Set Clock (c,p)	SCK	B204	S	D2(B2)
Set Clock Comparator (p)	SCKC	B206	S	D2(B2)
Set CPU Timer (p)	SPT	B208	S	D2(B2)
Set Prefix (p)	SPX	B210	S	D2(B2)
Set Program Mask (n)	SPM	04	RR	R1
Set PSW Key from Address (s)	SPKA	B20A	S	D2(B2)
Set Secondary ASN (s)	SSAR	B225	RRE	R1
Set Storage Key (p)	SSK	08	RR	R1,R2
Set Storage Key Extended (p)	SSKE	B22B	RRE	R1,R2
Set System Mask (p)	SSM	80	S	D2(B2)
Shift and Round Decimal (c)	SRP	F0	SS	D1(L1,B1),D2(B2),I3
Shift Left Double (c)	SLDA	8F	RS	R1,D2(B2)
Shift Left Double Logical	SLDL	8D	RS	R1,D2(B2)
Shift Left Single (c)	SLA	8B	RS	R1,D2(B2)
Shift Left Single Logical	SLL	89	RS	R1,D2(B2)

c. Condition code is set
n. New condition code is loaded
p. Privileged instruction
s. Semiprivileged instruction
x. Extended-precision floating-point

Name	Mnemonic	OP Code	For-mat	Operands
Shift Right Double (c)	SRDA	8E	RS	R1,D2(B2)
Shift Right Double Logical	SRDL	8C	RS	R1,D2(B2)
Shift Right Single (c)	SRA	8A	RS	R1,D2(B2)
Shift Right Single Logical	SRL	88	RS	R1,D2(B2)
Signal Processor (c,p)	SIGP	AE	RS	R1,R3,D2(B2)
Start I/O (c,p)	SIO	9C00	S	D2(B2)
Start I/O Fast Release (c,p)	SIOF	9C01	S	D2(B2)
Store	ST	50	RX	R1,D2(X2,B2)
Store Channel ID (c,p)	STIDC	B203	S	D2(B2)
Store Character	STC	42	RX	R1,D2(X2,B2)
Store Characters under Mask	STCM	BE	RS	R1,M3,D2(B2)
Store Clock (c)	STCK	B205	S	D2(B2)
Store Clock Comparator (p)	STCKC	B207	S	D2(B2)
Store Control (p)	STCTL	B6	RS	R1,R3,D2(B2)
Store CPU Address (p)	STAP	B212	S	D2(B2)
Store CPU ID (p)	STIDP	B202	S	D2(B2)
Store CPU Timer (p)	STPT	B209	S	D2(B2)
Store Halfword	STH	40	RX	R1,D2(X2,B2)
Store Multiple	STM	90	RS	R1,R3,D2(B2)
Store Prefix (p)	STPX	B211	S	D2(B2)
Store Then AND System Mask (p)	STNSM	AC	SI	D1(B1),I2
Store Then OR System Mask (p)	STOSM	AD	SI	D1(B1),I2
Subtract (c)	SR	1B	RR	R1,R2
Subtract (c)	S	5B	RX	R1,D2(X2,B2)
Subtract Decimal (c)	SP	FB	SS	D1(L1,B1),D2(L2,B2)
Subtract Halfword (c)	SH	4B	RX	R1,D2(X2,B2)
Subtract Logical (c)	SLR	1F	RR	R1,R2
Subtract Logical (c)	SL	5F	RX	R1,D2(X2,B2)
Supervisor Call	SVC	0A	RR	I
Test and Set (c)	TS	93	S	D2(B2)
Test Block (c,p)	TB	B22C	RRE	R1,R2
Test Channel (c,p)	TCH	9F00	S	D2(B2)
Test I/O (c,p)	TIO	9D00	S	D2(B2)
Test Protection (c,p)	TPROT	E501	SSE	D1(B1),D2(B2)
Test under Mask (c)	TM	91	SI	D1(B1),I2
Translate	TR	DC	SS	D1(L,B1),D2(B2)
Translate and Test (c)	TRT	DD	SS	D1(L,B1),D2(B2)
Unpack	UNPK	F3	SS	D1(L1,B1),D2(L2,B2)
Write Direct (p)	WRD	84	SI	D1(B1),I2
Zero and Add (c)	ZAP	F8	SS	D1(L1,B1),D2(L2,B2)

Floating-Point Instructions

Name	Mnemonic	OP Code	For-mat	Operands
Add Normalized, Extended (c,x)	AXR	36	RR	R1,R2
Add Normalized, Long (c)	ADR	2A	RR	R1,R2
Add Normalized, Long (c)	AD	6A	RX	R1,D2(X2,B2)
Add Normalized, Short (c)	AER	3A	RR	R1,R2
Add Normalized, Short (c)	AE	7A	RX	R1,D2(X2,B2)
Add Unnormalized, Long (c)	AWR	2E	RR	R1,R2
Add Unnormalized, Long (c)	AW	6E	RX	R1,D2(X2,B2)
Add Unnormalized, Short (c)	AUR	3E	RR	R1,R2
Add Unnormalized, Short (c)	AU	7E	RX	R1,D2(X2,B2)
Compare, Long (c)	CDR	29	RR	R1,R2
Compare, Long (c)	CD	69	RX	R1,D2(X2,B2)
Compare, Short (c)	CER	39	RR	R1,R2
Compare, Short (c)	CE	79	RX	R1,D2(X2,B2)

c. Condition code is set
n. New condition code is loaded
p. Privileged instruction
s. Semiprivileged instruction
x. Extended-precision floating-point

Floating-Point Instructions (Cont'd)

Name	Mnemonic	OP Code	For-mat	Operands
Divide, Long	DDR	2D	RR	R1,R2
Divide, Long	DD	6D	RX	R1,D2(X2,B2)
Divide, Short	DER	3D	RR	R1,R2
Divide, Short	DE	7D	RX	R1,D2(X2,B2)
Halve, Long	HDR	24	RR	R1,R2
Halve, Short	HER	34	RR	R1,R2
Load, Long	LDR	28	RR	R1,R2
Load, Long	LD	68	RX	R1,D2(X2,B2)
Load, Short	LER	38	RR	R1,R2
Load, Short	LE	78	RX	R1,D2(X2,B2)
Load and Test, Long (c)	LTDR	22	RR	R1,R2
Load and Test, Short (c)	LTER	32	RR	R1,R2
Load Complement, Long (c)	LCDR	23	RR	R1,R2
Load Complement, Short (c)	LCER	33	RR	R1,R2
Load Negative, Long (c)	LNDR	21	RR	R1,R2
Load Negative, Short (c)	LNER	31	RR	R1,R2
Load Positive, Long (c)	LPDR	20	RR	R1,R2
Load Positive, Short (c)	LPER	30	RR	R1,R2
Load Rounded, Extended to Long (x)	LRDR	25	RR	R1,R2
Load Rounded, Long to Short (x)	LRER	35	RR	R1,R2
Multiply, Extended (x)	MXR	26	RR	R1,R2
Multiply, Long	MDR	2C	RR	R1,R2
Multiply, Long	MD	6C	RX	R1,D2(X2,B2)
Multiply, Long to Extended (x)	MXDR	27	RR	R1,R2
Multiply, Long to Extended (x)	MXD	67	RX	R1,D2(X2,B2)
Multiply, Short to Long	MER	3C	RR	R1,R2
Multiply, Short to Long	ME	7C	RX	R1,D2(X2,B2)
Store, Long	STD	60	RX	R1,D2(X2,B2)
Store, Short	STE	70	RX	R1,D2(X2,B2)
Subtract Normalized, Extended (c,x)	SXR	37	RR	R1,R2
Subtract Normalized, Long (c)	SDR	2B	RR	R1,R2
Subtract Normalized, Long (c)	SD	6B	RX	R1,D2(X2,B2)
Subtract Normalized, Short (c)	SER	3B	RR	R1,R2
Subtract Normalized, Short (c)	SE	7B	RX	R1,D2(X2,B2)
Subtract Unnormalized, Long (c)	SWR	2F	RR	R1,R2
Subtract Unnormalized, Long (c)	SW	6F	RX	R1,D2(X2,B2)
Subtract Unnormalized, Short (c)	SUR	3F	RR	R1,R2
Subtract Unnormalized, Short (c)	SU	7F	RX	R1,D2(X2,B2)

c. Condition code is set
n. New condition code is loaded
p. Privileged instruction
s. Semiprivileged instruction
x. Extended-precision floating-point

CONDITION CODES

Condition Code Setting	0	1	2	3
Mask Bit Value	8	4	2	1
General Instructions				
Add, Add Halfword	zero	<zero	>zero	overflow
Add Logical	zero, no carry	not zero, no carry	zero, carry	not zero, carry
AND	zero	not zero	—	—
Compare, Compare Halfword	equal	1st op low	1st op high	—
Compare and Swap/ Double	equal	not equal	—	—
Compare Logical	equal	1st op low	1st op high	—
Exclusive OR	zero	not zero	—	—
Insert Characters under Mask	all zeros	1st bit one	1st bit zero	—
Load and Test	zero	<zero	>zero	—
Load Complement	zero	<zero	>zero	overflow
Load Negative	zero	<zero	—	—
Load Positive	zero	—	>zero	overflow
Move Long	length equal	length low	length high	overlap
OR	zero	not zero	—	—
Shift Left Double/ Single	zero	<zero	>zero	overflow
Shift Right Double/ Single	zero	<zero	>zero	—
Store Clock	set	not set	error	not oper
Subtract, Subtract Halfword	zero	<zero	>zero	overflow
Subtract Logical	—	not zero, no carry	zero, carry	not zero, carry
Test and Set	1st bit zero	1st bit one	—	—
Test under Mask	all zeros	mixed	—	all ones
Translate and Test	all zeros	incomplete	complete	—
Decimal Instructions				
Add Decimal	zero	<zero	>zero	overflow
Compare Decimal	equal	1st op low	1st op high	—
Edit, Edit and Mark	zero	<zero	>zero	—
Shift and Round Decimal	zero	<zero	>zero	overflow
Subtract Decimal	zero	<zero	>zero	overflow
Zero and Add	zero	<zero	>zero	overflow
Floating-Point Instructions				
Add Normalized	zero	<zero	>zero	—
Add Unnormalized	zero	<zero	>zero	—
Compare	equal	1st op low	1st op high	—
Load and Test	zero	<zero	>zero	—
Load Complement	zero	<zero	>zero	—
Load Negative	zero	<zero	—	—
Load Positive	zero	—	>zero	—
Subtract Normalized	zero	<zero	>zero	—
Subtract Unnormalized	zero	<zero	>zero	—

CONDITION CODES (Cont'd)

Condition Code Setting	0	1	2	3
Mask Bit Value	8	4	2	1
I/O Instructions				
Clear Channel	reset signaled	–	chan busy	not oper
Clear I/O	no operation in progress	CSW stored	chan busy	not oper
Halt Device	interruption pending/busy	CSW stored	channel working	not oper
Halt I/O	interruption pending	CSW stored	burst op stopped	not oper
Resume I/O	successful	–	–	not oper
Start I/O, SIOF	successful	CSW stored	busy	not oper
Store Channel ID	ID stored	CSW stored	busy	not oper
Test Channel	available	interruption pending	burst mode	not oper
Test I/O	available	CSW stored	busy	not oper
Control Instructions				
Connect/Disconnect Channel Set	successful	connected to another CPU	–	not oper
Insert Address Space Control	zero	one	–	–
Load Address Space Parameters	parameters loaded	pri not available	sec not avail or not auth	space-sw event
Load Real Address	translation available	ST entry invalid	PT entry invalid	length violation
Move to Primary/ Secondary	len $\leq$ 256	–	–	len $>$ 256
Move with Key	len $\leq$ 256	–	–	len $>$ 256
Reset Reference Bit/Extended	R = 0,C = 0	R = 0, C = 1	R = 1, C = 0	R = 1, C = 1
Set Clock	set	secure	–	not oper
Signal Processor	accepted	stat stored	busy	not oper
Test Block	usable	not usable	–	–
Test Protection	can fetch, can store	can fetch, can't store	can't fetch, can't store	translation not avail

SOME EDIT AND EDMK PATTERN CHARACTERS (hex)

20 – digit selector
21 – start of significance
22 – field separator
40 – blank
4B – period
5B – dollar sign
5C – asterisk
6B – comma
C3D9 – CR

ASSEMBLER INSTRUCTIONS†

Function	Mnemonic	Meaning
Data definition	DC	Define constant
	DS	Define storage
	CCW	Define channel command word
Program sectioning and linking	START	Start assembly
	CSECT	Identify control section
	DSECT	Identify dummy section
	DXD*	Define external dummy section
	CXD*	Cumulative length of external dummy section
	COM	Identify blank common control section
	ENTRY	Identify entry-point symbol
	EXTRN	Identify external symbol
	WXTRN	Identify weak external symbol
Base register assignment	USING	Use base address register
	DROP	Drop base address register
Control of listings	TITLE	Identify assembly output
	EJECT	Start new page
	SPACE	Space listing
	PRINT	Print optional data
Program Control	ICTL	Input format control
	ISEQ	Input sequence checking
	PUNCH	Punch a card
	REPRO	Reproduce following card
	ORG	Set location counter
	EQU	Equate symbol
	OPSYN*	Equate operation code
	PUSH*	Save current PRINT or USING status
	POP*	Restore PRINT or USING status
	LTORG	Begin literal pool
	CNOP	Conditional no operation
	COPY	Copy predefined source coding
	END	End assembly
Macro definition	MACRO	Macro definition header
	MNOTE	Request for error message
	MEXIT	Macro definition exit
	MEND	Macro definition trailer
Conditional assembly	ACTR	Conditional assembly loop counter
	AGO	Unconditional branch
	AIF	Conditional branch
	ANOP	Assembly no operation
	GBLA	Define global SETA symbol
	GBLB	Define global SETB symbol
	GBLC	Define global SETC symbol
	LCLA	Define local SETA symbol
	LCLB	Define local SETB symbol
	LCLC	Define local SETC symbol
	SETA	Set arithmetic variable symbol
	SETB	Set binary variable symbol
	SETC	Set character variable symbol

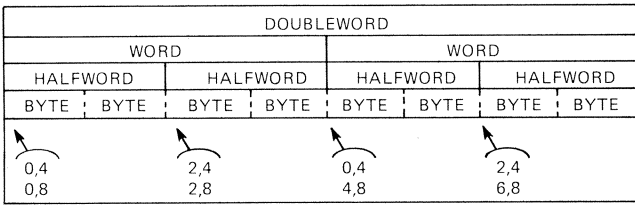
†Source: GC33-4010 for OS/VS, VM/370, and DOS/VSE.
*OS/VS and VM/370 only.

EXTENDED MNEMONIC INSTRUCTIONS†

Use	Extended Code* (RX or RR)	Meaning	Machine Instr.* (RX or RR)
General	B or BR	Unconditional Branch	BC or BCR 15,
	NOP or NOPR	No Operation	BC or BCR 0,
After Compare Instructions (A:B)	BH or BHR	Branch on A High	BC or BCR 2,
	BL or BLR	Branch on A Low	BC or BCR 4,
	BE or BER	Branch on A Equal B	BC or BCR 8,
	BNH or BNHR	Branch on A Not High	BC or BCR 13,
	BNL or BNLR	Branch on A Not Low	BC or BCR 11,
	BNE or BNER	Branch on A Not Equal B	BC or BCR 7,
After Arithmetic Instructions	BO or BOR	Branch on Overflow	BC or BCR 1,
	BNO or BNOR	Branch on No Overflow	BC or BCR 14,
	BP or BPR	Branch on Plus	BC or BCR 2,
	BM or BMR	Branch on Minus	BC or BCR 4,
	BNP or BNPR	Branch on Not Plus	BC or BCR 13,
	BNM or BNMR	Branch on Not Minus	BC or BCR 11,
	BNZ or BNZR	Branch on Not Zero	BC or BCR 7,
	BZ or BZR	Branch on Zero	BC or BCR 8,
After Test under Mask Instruction	BO or BOR	Branch if Ones	BC or BCR 1,
	BM or BMR	Branch if Mixed	BC or BCR 4,
	BZ or BZR	Branch if Zeros	BC or BCR 8,
	BNO or BNOR	Branch if Not Ones	BC or BCR 14,
	BNM or BNMR	Branch if Not Mixed	BC or BCR 11,
	BNZ or BNZR	Branch if Not Zeros	BC or BCR 7,

†Source: GC33-4010 for OS/VS, VM/370 and DOS/VSE.
*Second operand, not shown, is D2(X2,B2) for RX format and R2 for RR format.

CNOP ALIGNMENT



SUMMARY OF CONSTANTS†

Type	Implied Length, Bytes	Alignment	Format	Truncation/ Padding
C	—	byte	characters	right
X	—	byte	hexadecimal digits	left
B	—	byte	binary digits	left
F	4	word	fixed-point binary	left
H	2	halfword	fixed-point binary	left
E	4	word	short floating-point	right
D	8	doubleword	long floating-point	right
L	16	doubleword	extended floating-point	right
P	—	byte	packed decimal	left
Z	—	byte	zoned decimal	left
A	4	word	value of address	left
Y	2	halfword	value of address	left
S	2	halfword	address in base-displacement form	—
V	4	word	externally defined address value	left
Q*	4	word	symbol naming a DXD or DSECT	left

†Source: GC33-4010 for OS/VS, VM/370, and DOS/VSE.
*OS/VS and VM/370 only.

I/O COMMAND CODES

Standard Command-Code Assignments (CCW bits 0-7)

x x x x	0 0 0 0	Invalid Command	mmmm	0100	Sense
mmmm	mm01	Write	0 0 0 0	0100	— Basic Sense
mmmm	mm10	Read	1 1 1 0	0100	— Sense ID
0 0 0 0	0 0 1 0	—Read IPL	x x x x	1000	Transfer in Channel
mmmm	mm11	Control	mmmm	1100	Read Backward
0 0 0 0	0 0 1 1	— Control No Operation			

x — Bit ignored m — Modifier bit for specific type of I/O device

Standard Meanings of Bits of First Sense Byte

Bit	Designation	Bit	Designation
0	Command reject	4	Data check
1	Intervention required	5	Overrun
2	Bus-out check	6	(Device–dependent)
3	Equipment check	7	(Device–dependent)

Console Printer Channel Commands

Write, No Carrier Return	01	Sense	04
Write, Auto Carrier Return	09	Audible Alarm	0B
Read Inquiry	0A	No Operation	03

Direct Access Storage Devices

Use this chart to find the proper column in the DASD Channel Commands table (Page 11) and to find order numbers for DASD reference manuals. See DASD manuals for restrictions.

	CKD Devices						FBA Devices		
Controller	2305	3330 3333	3340 3344	3350	3375	3380	3310	3370	Controller Manual
DASD-A1							col6		GA26-1660
DASD-A4			col2						GA33-1526
DASD-A6			col2						GA33-1566
DASD-A7								col6	GA33-1539
DDA-30		col2							GA33-1510
DDA-40			col2						GA33-1506
IFA		col2	col2						GA24-3632
ISC		col2	col2	col2					GA26-1620
ISC-SA		col2		col2					GA32-0036
2835	col1								GA26-1589
3830-1		col2*							GA26-1592
3830-2		col2	col2	col2					GA26-1617
3830-3		col2		col2					GA32-0036
3880-1		col2	col2	col2	col4			col6	GA26-1661
3880-2		col2	col2	col2	col4	col4		col6	GA26-1661
3880-3						col4			GA26-1661
3880-4					col4			col6	GA26-1661
3880-11 (ND)		col2		col2					GA32-0061
3880-11 (PD)				col2					GA32-0061
3880-11 (PP)				col3					GA32-0061
3880-13						col5			GA32-0067
Device Manual	GA26 1589	GA26 1615	GA26 1619	GA26 1638	GA26 1666	GA26 1664	GA26 1660	GA26 1657	

DASD-A1 = 4321/4331/4361 DASD Adapter for 3310
DASD-A4 = 4321/4331 DASD Adapter for 3340/3344
DASD-A6 = 4361 DASD Adapter for 3340/3344
DASD-A7 = 4321/4331/4361 DASD Adapter for 3370
DDA-30 = S/370 125-0, -2 Direct Disk Attachment for 3330/3333
DDA-40 = S/370 115-0, -2, 125-0, -2 Direct Disk Attachment for 3340/3344
IFA = S/370 135, 135-3, 138 Integrated File Adapter
ISC = Integrated storage controller
ISC-SA = Integrated storage controller with staging adapter
ND = Nonpaging director
PD = Paging director, direct mode
PP = Paging director, paging mode
* = 3333 does not attach to 3830-1

I/O COMMAND CODES (Cont'd)

DASD Channel Commands

Channel Command	Hex Code	2305	3330 3340 3350	Page Swap 3350	3375 3380	Data Cache 3380	FBA 3310 3370	Typical Transfer Count
		1	2	3	4	5	6	
Control								
No Operation	03	X	X	X	X	X	X	None
Seek	07	X	X	X	X	X		6
Seek Cylinder	0B	X	X	X	X	X		6
Space Count	0F	X	X		X	X		3
Recalibrate (No-Op on 2305-1, -2)	13	X	X		X	X		None
Restore (executed as No-Op)	17	X	X		X	X		None
Seek Head	1B	X	X	X	X	X		6
Set File Mask	1F	X	X		X	X		1
Set Sector (3340 RPS is optional)	23	X	X	X	X	X		1
Vary Sensing	27	X						1
Orient (No-Op on 2305-2)	2B	X						None
Set High Performance Storage Limits	3B					X		10
Locate	43						X	8
Locate Record	47				(a)			16
Suspend Multipath Reconnection	5B				(b)	X		None
Define Extent	63				(a)	X	X	16
Set Subsystem Mode	87					X		2
Set Paging Parameters	8B			X				10
Discard Block	8F			X				2+(5×n)
Set Path Group ID	AF				(b)	X		12
Search								
Search Key Equal (*A9)	29	X	X		X	X		KL
Search ID Equal (*B1)	31	X	X	X	X	X		5
Search Home Address Equal (*B9)	39	X	X		X	X		4
Search Key High (*C9)	49	X	X		X	X		KL
Search ID High (*D1)	51	X	X		X	X		5
Search Key Equal or High (*E9)	69	X	X		X	X		KL
Search ID Equal or High (*F1)	71	X	X		X	X		5
Read								
Read Initial Program Load	02	X	X		X	X	X	DL or 512
Read Data (*86)	06	X	X	X	X	X		DL
Read Key & Data (*8E)	0E	X	X		X	X		KL+DL
Read Count (*92)	12	X	X		X	X		8
Read Record Zero (*96)	16	X	X		X	X		8+KL+DL
Read Home Address (*9A)	1A	X	X		X	X		5
Read Count Key & Data (*9E)	1E	X	X		X	X		8+KL+DL
Read Sector (3340 RPS is optional)	22	X	X		X	X		1
Read	42						X	512 × n
Read Multiple Count Key & Data	5E		(c,d)		X	X		n × (8 + KL + DL)
Write								
Write Special Count Key & Data	01	X	X					8+KL+DL
Write Data	05	X	X	X	X	X		DL
Write Key & Data	0D	X	X		X	X		KL+DL
Erase	11	X	X		X	X		8+KL+DL
Write Record Zero	15	X	X		X	X		8+KL+DL
Write Home Address	19	X	X		X	X		5, 7, or 11
Write Count Key & Data	1D	X	X		X	X		8+KL+DL
Write	41						X	512 × n
Write Update Data	85				(a)			DL
Write Update Key & Data	8D				(a)			KL+DL
Write Count Key & Data Next Track	9D				(a)			8+KL+DL
Sense								
Basic Sense	04	X	X	X	X	X	X	24
Unconditional Reserve (e,f,g)	14		(h,j)		(b,h,j)	X	(h,j)	24
Read Buffered Log	24	X						128
Sense Path Group ID	34				(b)	X		12
Sense Subsystem Status	54		(k)			X		40
Read Device Characteristics	64						X	32
Sense Subsystem Counts	74		(k)			X		80
Device Release (d,f)	94	(j)	(h,j)		(b,h,j)	X	(h,j)	24
Read and Reset Buffered Log (d)	A4		X		X	X	X	24 or 32
Device Reserve (d,f)	B4	(j)	(h,j)		(b,h,j)	X	(h,j)	24
Sense ID (c,d)	E4		X	X	X	X	X	7
Diagnostic								
Diagnostic Write Home Address	09				X	X		27 or 28
Diagnostic Read Home Address	0A				X	X		27 or 28
Diagnostic Sense # (g)	44	X	X					16 or 512
Diagnostic Load (g)	53	X	X					1
Diagnostic Write (g)	73	X	X					8 or 512
Diagnostic Sense/Read	C4		(m)		X	X	X	variable
Diagnostic Control	F3						X	4+n
		1	2	3	4	5	6	

a Speed-matching-buffer feature
b Dynamic path switching (3380-AA4 only)
c Not valid for 3330 or 3333 on ISC-SA or 3830-1; DDA-40, IFA, ISC and 3830-2, -3 require 3344/3350 microcode
d Not valid on DDA-30
e Not valid on IFA, ISC-SA, or 3330-1; not valid on 3330, 3333, 3340, or 3344 devices
f Without string-switch, executed as Basic Sense on DASD-A1, -A4, -A6, -A7 (for Unconditional Reserve, see note g)
g Not valid on DDA-30, DDA-40, DASD-A4, -A6
h String-switching feature
j Channel-switching feature
k Valid only for 3880-11 paging director
m Valid only for 3880-1, -2, -11
* Multi-track command codes (standard)
# Also called "Read Diagnostic Status 1"

I/O COMMAND CODES (Cont'd)

Card Reader and Card Punch Channel Commands

3504, 3505 Card Readers/3525 Card Punch (GA21-9124)

Command	Binary		Hex	Bit Meanings	
Sense	0000	0100	04	SS	Stacker
Feed, Select Stacker	SS10	F011		00	1
Read Only*	11D0	F010		01/10	2
Diagnostic Read (invalid for 3504)	1101	0010	D2	F	Format Mode
Read, Feed, Select Stacker*	SSD0	F010		0	Unformatted
Write RCE Format*	0001	0001	11	1	Formatted
3504, 3505 only				D	Data Mode
Write OMR Format†	0011	0001	31	0	1—EBCDIC
				1	2—Card image
3525 only					
Write, Feed, Select Stacker	SSD0	0001		L	Line Position
Print Line*	LLLL	L101		(5-bit binary value)	

*Special feature on 3525. †Special feature.

Magnetic-Tape Channel Commands

Use column A, B, C, D, or E.

A = 3410/3411 (GA32-0022)
B = 3420-3, -5, -7 (GA32-0020)
C = 3420-4, -6, -8 (GA32-0021)
D = 3430 (GA32-0076)
E = 8809 (GA26-1659)

		A	B	C	D	E
No Operation	03	X	X	X	X	X
Rewind	07	X	X	X	X	X
Rewind Unload	0F	X	X	X	X	X
Modeset-1 200/Odd/Y/N	→13	1	2	3	.	
Set Long Gap	↳13				.	X
Erase Gap	17	X	X	X	X	X
Request Track-In-Error	1B	X	X	X	X	.
Write Tape Mark	1F	X	X	X	X	X
Modeset-1 200/Evn/N/N	→23	1	2	3	.	
Set Normal Gap	↳23				.	X
Backspace Block	27	X	X	X	X	X
Modeset-1 200/Evn/N/Y	2B	1	2	3	.	.
Backspace File	2F	X	X	X	X	X
Modeset-1 200/Odd/N/N	→33	1	2	3	.	
Set High Spd/Norm Gap	↳33				.	X
Forward Space Block	37	X	X	X	X	X
Modeset-1 200/Odd/N/Y	3B	1	2	3	.	.
Forward Space File	3F	X	X	X	X	X
Modeset-1 556/Odd/Y/N	→53	1	1	3	.	
Set Low Spd/Long Gap	↳53				.	X
Modeset-1 556/Evn/N/N	→63	1	1	3	.	
Set Low Spd/Norm Gap	↳63				.	X
Modeset-1 556/Evn/N/Y	6B	1	1	3	.	.
Modeset-1 556/Odd/N/N	73	1	1	3	.	.
Modeset-1 556/Odd/N/Y	7B	1	1	3	.	.
Set Low Speed	83	.	.	.	.	X

		A	B	C	D	E
Modeset-1 800/Odd/Y/N	→93	1	1	3	.	
Set High Spd/Long Gap	↳93					. X
Data Security Erase	97	X	X	X	X	X
Modeset-1 800/Evn/N/N	A3	1	1	3	.	.
Modeset-1 800/Evn/N/Y	AB	1	1	3	.	.
Modeset-1 800/Odd/N/N	B3	1	1	3	.	.
Modeset-1 800/Odd/N/Y	BB	1	1	3	.	.
Modeset-2 1600 BPI PE	C3	4	4	5	X	3
Modeset-2 800 BPI NRZI	CB	4	4	3	.	.
Modeset-2 6250 BPI GCR	D3	.	.	5	X	.
Set High Speed	E3	.	.	.	.	X
Write	01	X	X	X	X	X
Read	02	X	X	X	X	X
Read Backward	0C	X	X	X	X	.
Basic Sense	04	X	X	X	X	X
Read/Reset Buffered Log	A4	.	.	.	.	X
Release	D4	.	6	6	.	.
Sense ID	E4	.	.	.	X	X
Reserve	F4	.	6	6	.	.
Diagnostic Mode Set	0B	.	X	X	.	.
Set Diagnose	4B	.	X	X	X	.
Loop Write-To-Read	8B	.	X	X	X	X

X = Valid command
. = Invalid command
Blank = N/A

1 = No action occurs unless the 7-track feature is installed.
2 = No action occurs unless the 7-track feature is installed; if installed, density is set to 200 BPI by 3803-2 Tape Control, 556 BPI by 3803-1.
3 = Valid command, but no action occurs.
4 = No action occurs unless the 800 BPI density feature is installed.
5 = No action occurs unless the 1600 BPI density feature is installed.
6 = Requires two-channel switch feature.

Modeset-1 sets: density (200/556/800 BPI)/parity (even/odd)/data converter (Y=on/N=off)/translator (Y=on/N=off) for 7-track drives.
Modeset-2 sets: density (800/1600/6250 BPI) for 9-track drives.

I/O COMMAND CODES (Cont'd)

Printer Channel Commands

COMMANDS VALID FOR ALL PRINTERS
(Except 3800-3 when in Page Mode)

No Operation	03
Space 1 Line Immediate	0B
Space 2 Lines Immediate	13
Space 3 Lines Immediate	1B
Block Data Check	73
Allow Data Check	7B
Skip to Channel 1 Immediate	8B
Skip to Channel 2 Immediate	93
Skip to Channel 3 Immediate	9B
Skip to Channel 4 immediate	A3
Skip to Channel 5 Immediate	AB
Skip to Channel 6 Immediate	B3
Skip to Channel 7 Immediate	BB
Skip to Channel 8 Immediate	C3
Skip to Channel 9 Immediate	CB
Skip to Channel 10 Immediate	D3
Skip to Channel 11 Immediate	DB
Skip to Channel 12 Immediate	E3
Write Without Spacing	01
Write and Space 1 Line	09
Write and Space 2 Lines	11
Write and Space 3 Lines	19
Write and Skip to Channel 1	89
Write and Skip to Channel 2	91
Write and Skip to Channel 3	99
Write and Skip to Channel 4	A1
Write and Skip to Channel 5	A9
Write and Skip to Channel 6	B1
Write and Skip to Channel 7	B9
Write and Skip to Channel 8	C1
Write and Skip to Channel 9	C9
Write and Skip to Channel 10	D1
Write and Skip to Channel 11	D9
Write and Skip to Channel 12	E1
Basic Sense	04

3800-3 PAGE MODE COMMANDS
(See Note X)

No Operation	03
Load Font Index	0F
Load Font Control	1F
Load Font	2F
Execute Order Any State	33
Load Font Equivalence	3F
Delete Font	4F
Begin Page Segment	5F
Delete Page Segment	6F
Include Page Segment	7F
Execute Order Home State	8F
Set Home State	97
Load Copy Control	9F
Begin Page	AF
End Page	BF
Load Page Description	CF
Begin Overlay	DF
Delete Overlay	EF
Write Factored Text Control	0D
Write Text	2D
Write Image Control	3D
Write Image	4D
End	5D
Load Page Position	6D
Basic Sense	04
Sense Intermediate Buffer	14
Sense Error Log	24
Sense ID	E4

3800-1 Reference: GA26-1635
3800-3 Reference: GA32-0050

Note X: Other 3800-3 commands are rejected with command retry; the retry will succeed because Page Mode will have been reset.

Note Y: For 3800-3 only, the Set Home State (97) command will be rejected with command retry; the retry will succeed because Page Mode will have been set.

IMPACT PRINTERS – ADDITIONAL COMMANDS

Printer	Column	Reference
1403-N1	A	GA24-3312
3203-1, -2	B	GA33-1515
3203-4	C	GA33-1515
3203-5	C	GA33-1529
3211	C	GA24-3543
4248 <3211 mode>	C	GA24-3927
3262-1, -11	D	GA24-3733
3262-5 <3262-1 mode>	D	GA24-3936
4245	D	GA33-1541
3262-5 <4248 mode>	E	GA24-3936
4248 <native mode>	E	GA24-3927

Use column A, B, C, D, or E.		A	B	C	D	E
Unfold	23	.	.	X	X	X
Execute Order	33	.	.	.	.	X
Fold	43	.	.	X	X	X
Advance to End of Sheet	5B	.	X	.	.	.
Load Forms Control Buffer	63	.	X	X	X	X
Raise Cover	6B	.	.	1	2	
Signal Attention	6B	.	.			3
Skip to Channel 0 Immediate	83	.	.	4	.	2
Clear Printer	87	.	.	.	X	X
UCS Gate Load	EB	X	2	.	.	.
Load UCS Buffer and Fold	F3	X	X	.	.	
Verify Band ID	F3	.	.	.		X
Load UCS Buffer (No Fold)	FB	X	X	X	X	
Verify Band ID	FB					X
Release CU and Device	14	5	.	.	.	
Sense Intermediate Buffer	14	.	.	.		X
Release CU, Reserve Device	34	5	.	.	.	
Reserve CU, Release Device	54	5	.	.	.	
Reserve CU and Device	74	5	.	.	.	
Release Device	94	5	.	.	.	
Reserve Device	B4	5	.	.	.	
Release CU	D4	5	.	.	.	
Sense ID	E4	.	X	.	X	X
Reserve CU	F4	5	.	.	.	
Read Band ID	0A	.	.			X
Diagnostic Read PLB	02	X	.	X	6	2
Diagnostic Write	05	7	.	8	6	2
Diagnostic Check Read	06	X	.	X	X	2
Diagnostic Gate	07	.	.	X	X	2
Diagnostic Read UCS Buffer	0A	.	.	X	X	
Diagnostic Read FCB	12	.	.	X	X	X

X = Valid; . = Invalid; Blank = N/A
1 = No action occurs (except 3211).
2 = No action occurs.
3 = No action occurs (except 4248).
4 = 3211 only (no action occurs on 4248 <3211 mode> and 3203-4).
5 = Two-channel switch feature only.
6 = No action occurs (except 4245).
7 = 1403-N1 also uses command codes 0D, 15, 1D, 8D, 95, 9D, A5, AD, B5, BD, C5, CD, D5, DD, and E5.
8 = 3211 and 4248 <3211 mode> only.

3800-1, -3 – ADDITIONAL COMMANDS
(Except 3800-3 when in Page Mode; see Note Y)

End of Transmission	07
Mark Form	17
Load Copy Number	23
Execute Order Any State	33
Initialize Printer	37
Load Forms Overlay Seq Control	43
Select Translate Table 0	47
Load Writable Char Gen Module	53
Select Translate Table 1	57
Load Forms Control Buffer	63
Select Translate Table 2	67
Select Translate Table 3	77
Load Translate Table	83
Clear Printer	87
Load Graphic Char Modification	25
Load Copy Modification	35
Sense Intermediate Buffer	14
Sense Error Log	24
Sense ID	E4

CODE TABLES

Dec.	Hex	Inst. (RR)	Graphics and Controls BCDIC	EBCDIC(1)	ASCII	7-Track Tape BCDIC(2)	Card Code EBCDIC	Binary
0	00			NUL	NUL		12-0-1-8-9	0000 0000
1	01			SOH	SOH		12-1-9	0000 0001
2	02			STX	STX		12-2-9	0000 0010
3	03			ETX	ETX		12-3-9	0000 0011
4	04	SPM		SEL	EOT		12-4-9	0000 0100
5	05	BALR		HT	ENQ		12-5-9	0000 0101
6	06	BCTR		RNL	ACK		12-6-9	0000 0110
7	07	BCR		DEL	BEL		12-7-9	0000 0111
8	08	SSK		GE	BS		12-8-9	0000 1000
9	09	ISK		SPS	HT		12-1-8-9	0000 1001
10	0A	SVC		RPT	LF		12-2-8-9	0000 1010
11	0B			VT	VT		12-3-8-9	0000 1011
12	0C			FF	FF		12-4-8-9	0000 1100
13	0D	BASR		CR	CR		12-5-8-9	0000 1101
14	0E	MVCL		SO	SO		12-6-8-9	0000 1110
15	0F	CLCL		SI	SI		12-7-8-9	0000 1111
16	10	LPR		DLE	DLE		12-11-1-8-9	0001 0000
17	11	LNR		DC1	DC1		11-1-9	0001 0001
18	12	LTR		DC2	DC2		11-2-9	0001 0010
19	13	LCR		DC3	DC3		11-3-9	0001 0011
20	14	NR		RES/ENP	DC4		11-4-9	0001 0100
21	15	CLR		NL	NAK		11-5-9	0001 0101
22	16	OR		BS	SYN		11-6-9	0001 0110
23	17	XR		POC	ETB		11-7-9	0001 0111
24	18	LR		CAN	CAN		11-8-9	0001 1000
25	19	CR		EM	EM		11-1-8-9	0001 1001
26	1A	AR		UBS	SUB		11-2-8-9	0001 1010
27	1B	SR		CU1	ESC		11-3-8-9	0001 1011
28	1C	MR		IFS	FS		11-4-8-9	0001 1100
29	1D	DR		IGS	GS		11-5-8-9	0001 1101
30	1E	ALR		IRS	RS		11-6-8-9	0001 1110
31	1F	SLR		ITB/IUS	US		11-7-8-9	0001 1111
32	20	LPDR		DS	SP		11-0-1-8-9	0010 0000
33	21	LNDR		SOS	!		0-1-9	0010 0001
34	22	LTDR		FS	"		0-2-9	0010 0010
35	23	LCDR		WUS	#		0-3-9	0010 0011
36	24	HDR		BYP/INP	$		0-4-9	0010 0100
37	25	LRDR		LF	%		0-5-9	0010 0101
38	26	MXR		ETB	&		0-6-9	0010 0110
39	27	MXDR		ESC	'		0-7-9	0010 0111
40	28	LDR		SA	(		0-8-9	0010 1000
41	29	CDR		SFE	)		0-1-8-9	0010 1001
42	2A	ADR		SM/SW	*		0-2-8-9	0010 1010
43	2B	SDR		CSP	+		0-3-8-9	0010 1011
44	2C	MDR		MFA	,		0-4-8-9	0010 1100
45	2D	DDR		ENQ	-		0-5-8-9	0010 1101
46	2E	AWR		ACK	.		0-6-8-9	0010 1110
47	2F	SWR		BEL	/		0-7-8-9	0010 1111
48	30	LPER			0		12-11-0-1-8-9	0011 0000
49	31	LNER			1		1-9	0011 0001
50	32	LTER		SYN	2		2-9	0011 0010
51	33	LCER		IR	3		3-9	0011 0011
52	34	HER		PP	4		4-9	0011 0100
53	35	LRER		TRN	5		5-9	0011 0101
54	36	AXR		NBS	6		6-9	0011 0110
55	37	SXR		EOT	7		7-9	0011 0111
56	38	LER		SBS	8		8-9	0011 1000
57	39	CER		IT	9		1-8-9	0011 1001
58	3A	AER		RFF	:		2-8-9	0011 1010
59	3B	SER		CU3	;		3-8-9	0011 1011
60	3C	MER		DC4	<		4-8-9	0011 1100
61	3D	DER		NAK	=		5-8-9	0011 1101
62	3E	AUR			>		6-8-9	0011 1110
63	3F	SUR		SUB	?		7-8-9	0011 1111

1. Two columns of EBCDIC graphics are shown. The first gives IBM standard U.S. bit pattern assignments. The second shows the T-11 and TN text printing chains (120 graphics.)
2. Add C (check bit) for odd or even parity as needed, except as noted.
3. For even parity use CA.

TWO-CHARACTER BSC DATA LINK CONTROLS

Function	EBCDIC	ASCII
ACK-0	DLE,X'70'	DLE,0
ACK-1	DLE,X'61'	DLE,1
WACK	DLE,X'6B'	DLE,;
RVI	DLE,X'7C'	DLE,<

CODE TABLES (Cont'd)

Dec.	Hex	Inst. (RX)	Graphics and Controls BCDIC	EBCDIC(1)		ASCII	7-Track Tape BCDIC(2)	Card Code EBCDIC	Binary
64	40	STH	SP	SP	SP	@	(3)	no punches	0100 0000
65	41	LA		RSP		A		12-0-1-9	0100 0001
66	42	STC				B		12-0-2-9	0100 0010
67	43	IC				C		12-0-3-9	0100 0011
68	44	EX				D		12-0-4-9	0100 0100
69	45	BAL				E		12-0-5-9	0100 0101
70	46	BCT				F		12-0-6-9	0100 0110
71	47	BC				G		12-0-7-9	0100 0111
72	48	LH				H		12-0-8-9	0100 1000
73	49	CH				I		12-1-8	0100 1001
74	4A	AH		¢	¢	J		12-2-8	0100 1010
75	4B	SH	.	.	.	K	B A 8 2 1	12-3-8	0100 1011
76	4C	MH	¤)	<	<	L	B A 8 4	12-4-8	0100 1100
77	4D	BAS	[	(	(	M	B A 8 4 1	12-5-8	0100 1101
78	4E	CVD	<	+	+	N	B A 8 4 2	12-6-8	0100 1110
79	4F	CVB	╪	|	|	O	B A 8 4 2 1	12-7-8	0100 1111
80	50	ST	&+	&	&	P	B A	12	0101 0000
81	51					Q		12-11-1-9	0101 0001
82	52					R		12-11-2-9	0101 0010
83	53					S		12-11-3-9	0101 0011
84	54	N				T		12-11-4-9	0101 0100
85	55	CL				U		12-11-5-9	0101 0101
86	56	O				V		12-11-6-9	0101 0110
87	57	X				W		12-11-7-9	0101 0111
88	58	L				X		12-11-8-9	0101 1000
89	59	C				Y		11-1-8	0101 1001
90	5A	A		!	!	Z		11-2-8	0101 1010
91	5B	S	$	$	$	[	B 8 2 1	11-3-8	0101 1011
92	5C	M	*	*	*	\	B 8 4	11-4-8	0101 1100
93	5D	D	]	)	)	]	B 8 4 1	11-5-8	0101 1101
94	5E	AL	;	;	;	^	B 8 4 2	11-6-8	0101 1110
95	5F	SL	△	¬	¬	_	B 8 4 2 1	11-7-8	0101 1111
96	60	STD	–	–	–	`	B	11	0110 0000
97	61		/	/	/	a	A 1	0-1	0110 0001
98	62					b		11-0-2-9	0110 0010
99	63					c		11-0-3-9	0110 0011
100	64					d		11-0-4-9	0110 0100
101	65					e		11-0-5-9	0110 0101
102	66					f		11-0-6-9	0110 0110
103	67	MXD				g		11-0-7-9	0110 0111
104	68	LD				h		11-0-8-9	0110 1000
105	69	CD				i		0-1-8	0110 1001
106	6A	AD		¦		j		12-11	0110 1010
107	6B	SD	,	,	,	k	A 8 2 1	0-3-8	0110 1011
108	6C	MD	%(	%	%	l	A 8 4	0-4-8	0110 1100
109	6D	DD	¬	_	_	m	A 8 4 1	0-5-8	0110 1101
110	6E	AW	\	>	>	n	A 8 4 2	0-6-8	0110 1110
111	6F	SW	✱	?	?	o	A 8 4 2 1	0-7-8	0110 1111
112	70	STE				p		12-11-0	0111 0000
113	71					q		12-11-0-1-9	0111 0001
114	72					r		12-11-0-2-9	0111 0010
115	73					s		12-11-0-3-9	0111 0011
116	74					t		12-11-0-4-9	0111 0100
117	75					u		12-11-0-5-9	0111 0101
118	76					v		12-11-0-6-9	0111 0110
119	77					w		12-11-0-7-9	0111 0111
120	78	LE				x		12-11-0-8-9	0111 1000
121	79	CE		`		y		1-8	0111 1001
122	7A	AE	ъ	:	:	z	A	2-8	0111 1010
123	7B	SE	#=	#	#	¦	8 2 1	3-8	0111 1011
124	7C	ME	@'	@	@	¦	8 4	4-8	0111 1100
125	7D	DE	:	'	'	¦	8 4 1	5-8	0111 1101
126	7E	AU	>	=	=	~	8 4 2	6-8	0111 1110
127	7F	SU	✓	"	"	DEL	8 4 2 1	7-8	0111 1111

CODE TABLES (Cont'd)

Dec.	Hex	Instruction and Format		Graphics and Controls BCDIC	EBCDIC(1)	ASCII	7-Track Tape BCDIC(2)	Card Code EBCDIC	Binary
128	80	SSM	S					12-0-1-8	1000 0000
129	81				a	a		12-0-1	1000 0001
130	82	LPSW	S		b	b		12-0-2	1000 0010
131	83	Diagnose			c	c		12-0-3	1000 0011
132	84	WRD	SI		d	d		12-0-4	1000 0100
133	85	RDD	SI		e	e		12-0-5	1000 0101
134	86	BXH	RS		f	f		12-0-6	1000 0110
135	87	BXLE	RS		g	g		12-0-7	1000 0111
136	88	SRL	RS		h	h		12-0-8	1000 1000
137	89	SLL	RS		i	i		12-0-9	1000 1001
138	8A	SRA	RS					12-0-2-8	1000 1010
139	8B	SLA	RS			¦		12-0-3-8	1000 1011
140	8C	SRDL	RS			≤		12-0-4-8	1000 1100
141	8D	SLDL	RS			(See Note		12-0-5-8	1000 1101
142	8E	SRDA	RS			+ See Note		12-0-6-8	1000 1110
143	8F	SLDA	RS			+		12-0-7-8	1000 1111
144	90	STM	RS					12-11-1-8	1001 0000
145	91	TM	SI		j	j		12-11-1	1001 0001
146	92	MVI	SI		k	k		12-11-2	1001 0010
147	93	TS	S		l	l		12-11-3	1001 0011
148	94	NI	SI		m	m		12-11-4	1001 0100
149	95	CLI	SI		n	n		12-11-5	1001 0101
150	96	OI	SI		o	o		12-11-6	1001 0110
151	97	XI	SI		p	p		12-11-7	1001 0111
152	98	LM	RS		q	q		12-11-8	1001 1000
153	99				r	r		12-11-9	1001 1001
154	9A							12-11-2-8	1001 1010
155	9B					¦		12-11-3-8	1001 1011
156	9C	See below				¤		12-11-4-8	1001 1100
157	9D	See below				) See Note		12-11-5-8	1001 1101
158	9E	See below				±		12-11-6-8	1001 1110
159	9F	See below				■		12-11-7-8	1001 1111
160	A0					¬ See Note		11-0-1-8	1010 0000
161	A1				~	°		11-0-1	1010 0001
162	A2				s	s		11-0-2	1010 0010
163	A3				t	t		11-0-3	1010 0011
164	A4				u	u		11-0-4	1010 0100
165	A5				v	v		11-0-5	1010 0101
166	A6				w	w		11-0-6	1010 0110
167	A7				x	x		11-0-7	1010 0111
168	A8				y	y		11-0-8	1010 1000
169	A9				z	z		11-0-9	1010 1001
170	AA							11-0-2-8	1010 1010
171	AB					∟		11-0-3-8	1010 1011
172	AC	STNSM	SI			⌐		11-0-4-8	1010 1100
173	AD	STOSM	SI			[		11-0-5-8	1010 1101
174	AE	SIGP	RS			≥		11-0-6-8	1010 1110
175	AF	MC	SI			•		11-0-7-8	1010 1111
176	B0					[0] See Note		12-11-0-1-8	1011 0000
177	B1	LRA	RX			[1] See Note		12-11-0-1	1011 0001
178	B2	See below				[2] See Note		12-11-0-2	1011 0010
179	B3					[3] See Note		12-11-0-3	1011 0011
180	B4					[4] See Note		12-11-0-4	1011 0100
181	B5					[5] See Note		12-11-0-5	1011 0101
182	B6	STCTL	RS			[6] See Note		12-11-0-6	1011 0110
183	B7	LCTL	RS			[7] See Note		12-11-0-7	1011 0111
184	B8					[8] See Note		12-11-0-8	1011 1000
185	B9					[9] See Note		12-11-0-9	1011 1001
186	BA	CS	RS					12-11-0-2-8	1011 1010
187	BB	CDS	RS			⌟		12-11-0-3-8	1011 1011
188	BC					¬		12-11-0-4-8	1011 1100
189	BD	CLM	RS			]		12-11-0-5-8	1011 1101
190	BE	STCM	RS			≠		12-11-0-6-8	1011 1110
191	BF	ICM	RS			¬		12-11-0-7-8	1011 1111

S Format

9C00 – SIO	9E01 – HDV	B203 – STIDC	B209 – STPT	B212 – STAP
9C01 – SIOF	9F00 – TCH	B204 – SCK	B20A – SPKA	B213 – RRB
9C02 – RIO	9F01 – CLRCH	B205 – STCK	B20B – IPK	B218 – PC
9D00 – TIO	B200 – CONCS	B206 – SCKC	B20D – PTLB	B219 – SAC
9D01 – CLRIO	B201 – DISCS	B207 – STCKC	B210 – SPX	
9E00 – HIO	B202 – STIDP	B208 – SPT	B211 – STPX	

RRE Format

B221 – IPTE	B224 – IAC	B226 – EPAR	B228 – PT	B22A – RRBE
B223 – IVSK	B225 – SSAR	B227 – ESAR	B229 – ISKE	B22B – SSKE
				B22C – TB

Note: This character is an EBCDIC superscript character.

CODE TABLES (Cont'd)

Dec.	Hex	Inst. (SS)	Graphics and Controls BCDIC	EBCDIC(1)	ASCII	7-Track Tape BCDIC(2)	Card Code EBCDIC	Binary
192	C0		?	{		B A 8 2	12-0	1100 0000
193	C1		A	A	A	B A 1	12-1	1100 0001
194	C2		B	B	B	B A 2	12-2	1100 0010
195	C3		C	C	C	B A 2 1	12-3	1100 0011
196	C4		D	D	D	B A 4	12-4	1100 0100
197	C5		E	E	E	B A 4 1	12-5	1100 0101
198	C6		F	F	F	B A 4 2	12-6	1100 0110
199	C7		G	G	G	B A 4 2 1	12-7	1100 0111
200	C8		H	H	H	B A 8	12-8	1100 1000
201	C9		I	I	I	B A 8 1	12-9	1100 1001
202	CA			SHY			12-0-2-8-9	1100 1010
203	CB						12-0-3-8-9	1100 1011
204	CC			⌐			12-0-4-8-9	1100 1100
205	CD						12-0-5-8-9	1100 1101
206	CE			┬			12-0-6-8-9	1100 1110
207	CF						12-0-7-8-9	1100 1111
208	D0		!	}		B 8 2	11-0	1101 0000
209	D1	MVN	J	J	J	B 1	11-1	1101 0001
210	D2	MVC	K	K	K	B 2	11-2	1101-0010
211	D3	MVZ	L	L	L	B 2 1	11-3	1101 0011
212	D4	NC	M	M	M	B 4	11-4	1101 0100
213	D5	CLC	N	N	N	B 4 1	11-5	1101 0101
214	D6	OC	O	O	O	B 4 2	11-6	1101 0110
215	D7	XC	P	P	P	B 4 2 1	11-7	1101 0111
216	D8		Q	Q	Q	B 8	11-8	1101 1000
217	D9	MVCK	R	R	R	B 8 1	11-9	1101 1001
218	DA	MVCP					12-11-2-8-9	1101 1010
219	DB	MVCS					12-11-3-8-9	1101 1011
220	DC	TR					12-11-4-8-9	1101 1100
221	DD	TRT					12-11-5-8-9	1101 1101
222	DE	ED					12-11-6-8-9	1101 1110
223	DF	EDMK					12-11-7-8-9	1101 1111
224	E0		∔	\		A 8 2	0-2-8	1110 0000
225	E1			NSP			11-0-1-9	1110 0001
226	E2		S	S	S	A 2	0-2	1110 0010
227	E3		T	T	T	A 2 1	0-3	1110 0011
228	E4		U	U	U	A 4	0-4	1110 0100
229	E5	See below	V	V	V	A 4 1	0-5	1110 0101
230	E6		W	W	W	A 4 2	0-6	1110 0110
231	E7		X	X	X	A 4 2 1	0-7	1110 0111
232	E8	MVCIN	Y	Y	Y	A 8	0-8	1110 1000
233	E9		Z	Z	Z	A 8 1	0-9	1110 1001
234	EA						11-0-2-8-9	1110 1010
235	EB						11-0-3-8-9	1110 1011
236	EC			⊣			11-0-4-8-9	1110 1100
237	ED						11-0-5-8-9	1110 1101
238	EE						11-0-6-8-9	1110 1110
239	EF						11-0-7-8-9	1110 1111
240	F0	SRP	0	0	0	8 2	0	1111 0000
241	F1	MVO	1	1	1	1	1	1111 0001
242	F2	PACK	2	2	2	2	2	1111 0010
243	F3	UNPK	3	3	3	2 1	3	1111 0011
244	F4		4	4	4	4	4	1111 0100
245	F5		5	5	5	4 1	5	1111 0101
246	F6		6	6	6	4 2	6	1111 0110
247	F7		7	7	7	4 2 1	7	1111 0111
248	F8	ZAP	8	8	8	8	8	1111 1000
249	F9	CP	9	9	9	8 1	9	1111 1001
250	FA	AP		|		12-11-0-2-8-9	1111 1010
251	FB	SP					12-11-0-3-8-9	1111 1011
252	FC	MP					12-11-0-4-8-9	1111 1100
253	FD	DP					12-11-0-5-8-9	1111 1101
254	FE						12-11-0-6-8-9	1111 1110
255	FF			EO			12-11-0-7-8-9	1111 1111

SSE Format
E500 – LASP
E501 – TPROT

ANSI-DEFINED PRINTER CONTROL CHARACTERS
(A in RECFM field of DCB)

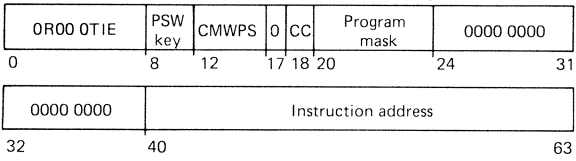
Code	Action before printing record
blank	Space 1 line
0	Space 2 lines
–	Space 3 lines
+	Suppress space
1	Skip to line 1 on new page

CONTROL REGISTERS

CR	Bits	Name of field	Associated with	Init.*
0	0	Block-multiplexing control	Block-multiplexing	0
	1	SSM-suppression control	SSM instruction	0
	2	TOD-clock-sync control	Multiprocessing	0
	3	Low-addr-protection control	Low-address protection	0
	4	Extraction-authority control	Dual address space	0
	5	Secondary-space control		0
	7	Storage-key exception control	Storage-key 4K-byte block	0
	8-12	Translation format	Dynamic address trans	0
	13	Page-fault-assist control	MVS assists	0
	16	Malfunc-alert subclass mask	Multiprocessing	0
	17	Emergency-signal subcl mask		0
	18	External-call subclass mask		0
	19	TOD-clk sync-chk subcl mask		0
	20	Clk-comparator subclass mask	Clock comparator	0
	21	CPU-timer subclass mask	CPU timer	0
	22	Service-signal subclass mask	Service signal	0
	24	Interval-timer subclass mask	Interval timer	1
	25	Interrupt-key subclass mask	Interrupt key	1
	26	External-signal subcl mask	External signal	1
1	0-7	Primary segment-table length	Dynamic address trans	0
	8-25	Primary segment-table origin		0
	31	Space-switch-event control	Dual address space	0
2	0-31	Channel masks	Channels	1
3	0-15	PSW-key mask	Dual address space	0
	16-31	Secondary ASN		0
4	0-15	Authorization index	Dual address space	0
	16-31	Primary ASN		0
5	0	Subsystem-linkage control	Dual address space	0
	8-24	Linkage-table origin		0
	25-31	Linkage-table length		0
6	0	VM assists	VM assists	0
	1	Virtual problem state	Extended facility	0
	2	ISK-SSK inhibit	VM assists	0
	3	S/360 operations only		0
	4	SVC inhibit		0
	5	Shadow-tbl-valid'n inhibit		0
	6	Expanded VM and CP		0
	7	Virtual interval timer		0
	8-28	Virtual-machine param list		0
	29	VM assists for MVS	Extended facility	0
7	0-7	Secondary segment-tbl length	Dual address space	0
	8-25	Secondary segment-tbl origin		0
8	16-31	Monitor masks	MC instruction	0
9	0	Successful-branching-event mask	Program-event recording	0
	1	Instruction-fetching-event mask		0
	2	Storage-alteration-event mask		0
	3	GR-alteration-event mask		0
	16-31	PER general-register masks		0
10	8-31	PER starting address	Program-event recording	0
11	8-31	PER ending address	Program-event recording	0
14	0	Check-stop control	Machine-check handling	1
	1	Synch.-MCEL control		1
	2	I/O-extended-logout control	I/O extended logout	0
	4	Recovery-report subclass mask	Machine-check handling	0
	5	Degradation-report subclass mask		0
	6	Ext.-damage report subclass mask		1
	7	Warning subclass mask		0
	8	Asynch.-MCEL control		0
	9	Asynch.- fixed-log control		0
	12	ASN-translation control	Dual address space	0
	20-31	ASN-first-table origin		0
15	8-28	MCEL address	Machine-check handling	512

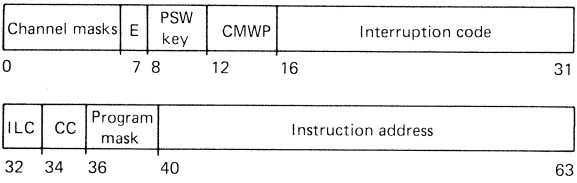
*Value after initial CPU reset.

PROGRAM-STATUS WORD (EC Mode)



1 (R) Program-event-recording mask
5 (T = 1) DAT mode
6 (I) Input/output mask
7 (E) External mask
12 (C = 1) Extended-control mode
13 (M) Machine-check mask
14 (W = 1) Wait state
15 (P = 1) Problem state
16 (S = 1) Address-space control
18-19 (CC) Condition code
20 Fixed-point-overflow mask
21 Decimal-overflow mask
22 Exponent-underflow mask
23 Significance mask

PROGRAM-STATUS WORD (BC Mode)



0-5 Channel 0 to 5 masks
6 Mask for channel 6 and up
7 (E) External mask
12 (C = 0) Basic-control mode
13 (M) Machine-check mask
14 (W = 1) Wait state
15 (P = 1) Problem state
32-33 (ILC) Instruction-length code
34-35 (CC) Condition code
36 Fixed-point-overflow mask
37 Decimal-overflow mask
38 Exponent-underflow mask
39 Significance mask

PROGRAM INTERRUPTION CODES

0001	Operation exception	0010	Segment translation excp
0002	Privileged operation excp	0011	Page translation exception
0003	Execute exception	0012	Translation specification excp
0004	Protection exception	0013	Special operation exception
0005	Addressing exception	0017	ASN-translation spec excp
0006	Specification exception	001C	Space-switch event
0007	Data exception	001F	PC-translation spec excp
0008	Fixed-point overflow excp	0020	AFX translation excp
0009	Fixed-point divide excp	0021	ASX translation excp
000A	Decimal overflow exception	0022	LX translation excp
000B	Decimal divide exception	0023	EX translation excp
000C	Exponent overflow excp	0024	Primary authority excp
000D	Exponent underflow excp	0025	Secondary authority excp
000E	Significance exception	0040	Monitor event
000F	Floating-point divide excp	0080	PER event (code may be combined with another code)

EXTERNAL INTERRUPTION CODES

Code (binary)	Condition	Code (binary)	Condition
00000000 1eeeeeee	Interval timer	00010010 00000000	Malfunction alert
00000000 e1eeeeee	Interrupt key	00010010 00000001	Emergency signal
00000000 ee1eeeee	External sig 2	00010010 00000010	External call
00000000 eee1eeee	External sig 3	00010000 00000011	TOD-clock-sync check
00000000 eeee1eee	External sig 4	00010000 00000100	Clock comparator
00000000 eeeee1ee	External sig 5	00010000 00000101	CPU timer
00000000 eeeeee1e	External sig 6	00100100 00000001	Service signal
00000000 eeeeeee1	External sig 7		

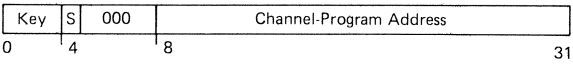
e- if 1, the bit indicates a concurrent external interruption condition.

FIXED STORAGE LOCATIONS

Area, dec.	Addr type	Hex addr	EC only	Function
0- 7	A	0		Initial-program-loading PSW
0- 7	R	0		Restart new PSW
8- 15	A	8		Initial-program-loading CCW1
8- 15	R	8		Restart old PSW
16- 23	A	10		Initial-program-loading CCW2
24- 31	R	18		External old PSW
32- 39	R	20		Supervisor-call old PSW
40- 47	R	28		Program old PSW
48- 55	R	30		Machine-check old PSW
56- 63	R	38		Input/output old PSW
64- 71	R	40		Channel-status word (see diagram)
72- 75	R	48		Channel-address word (see diagram)
80- 83	R	50		Interval timer
84- 87	L	54		Trace-table designation (0 control, 8-31 address)
88- 95	R	58		External new PSW
96-103	R	60		Supervisor-call new PSW
104-111	R	68		Program new PSW
112-119	R	70		Machine-check new PSW
120-127	R	78		Input/output new PSW
128-131	R	80		External-interruption parameter for service signal
132-133	R	84		CPU address associated with external interruption, or unchanged
132-133	R	84	X	CPU address associated with external interruption, or zeros
134-135	R	86	X	External-interruption code (see table)
136-139	R	88	X	SVC interruption (0-12 zeros, 13-14 ILC, 15:0, 16-31 code)
140-143	R	8C	X	Program interrupt (0-12 zeros, 13-14 ILC, 15:0, 16-31 code)
144-147	R	90	X	Translation-exception ID (see table)
148-149	R	94		Monitor class (0-7 zeros, 8-15 class number)
150-151	R	96	X	PER code (0-3 code, 4-15 zeros)
152-155	R	98	X	PER address (0-7 zeros, 8-31 address)
156-159	R	9C		Monitor code (0-7 zeros, 8-31 code)
164-167	L	A4		MVS-assist parameter list (MAPL) address
168-171	R	A8		Channel ID (0-3 type, 4-15 model, 16-31 max. IOEL length)
172-175	R	AC		I/O-extended-logout address (0-7 unused, 8-31 address)
176-179	R	B0		Limited channel logout (see diagram)
185	R	B9	X	Measurement byte (0-1 delay, 2-4 count, 5-7 zeros)
186-187	R	BA	X	I/O address
216-223	A	D8		Store-status CPU-timer save area
216-223	R	D8		Machine-check CPU-timer save area
224-231	A	E0		Store-status clock-comparator save area
224-231	R	E0		Machine-check clock-comparator save area
232-239	R	E8		Machine-check-interruption code (see diagram)
244-247	R	F4		External-damage code (see table)
248-251	R	F8		Failing-storage address (0-5 zeros, 6-31 address)
252-255	R	FC		Region code*
256-263	A	100		Store-status PSW save area
256-351	R	100		Fixed-logout area*
264-267	A	108		Store-status prefix save area
268-271	A	10C		Store-status model-dependent save area*
352-383	A	160		Store-status floating-point-register save area
352-383	R	160		Machine-check floating-point-register save area
384-447	A	180		Store-status general-register save area
384-447	R	180		Machine-check general-register save area
448-511	A	1C0		Store-status control-register save area
448-511	R	1C0		Machine-check control-register save area
795	L	31B		CPU identity for DAS tracing

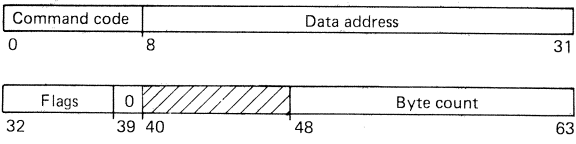
*May vary among models; see System Library manuals for specific model.
A = Absolute address
L = Logical address
R = Real address

CHANNEL-ADDRESS WORD (hex 48)



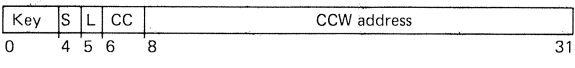
4(S) Suspend-control bit

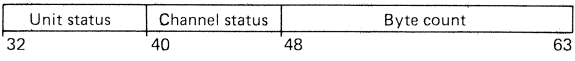
CHANNEL-COMMAND WORD



CD – bit 32 (80) causes use of data-address portion of next CCW.
CC – bit 33 (40) causes use of command code and data address of next CCW.
SLI – bit 34 (20) causes suppression of possible incorrect-length indication.
Skip – bit 35 (10) suppresses transfer of information to main storage.
PCI – bit 36 (08) causes a channel-program-controlled interruption.
IDA – bit 37 (04) causes bits 8-31 of CCW to specify location of first IDAW.
Suspend – bit 38 (02) causes suspension before execution of this CCW.

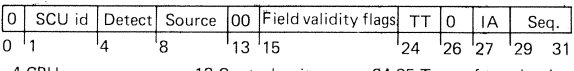
CHANNEL-STATUS WORD (hex 40)





4 Suspended (only in CCW stored by PCI)
5 Logout pending
6-7 Deferred condition code
32 (80) Attention
33 (40) Status modifier
34 (20) Control-unit end
35 (10) Busy
36 (08) Channel end
37 (04) Device end
38 (02) Unit check
39 (01) Unit exception
40 (80) Program-controlled interruption
41 (40) Incorrect length
42 (20) Program check
43 (10) Protection check
44 (08) Channel-data check
45 (04) Channel-control check
46 (02) Interface-control check
47 (01) Chaining check
48-63 Residual byte count for the last CCW used

LIMITED CHANNEL LOGOUT (hex B0)



4 CPU
5 Channel
6 Main-storage control
7 Main storage
8 CPU
9 Channel
10 Main-storage control
11 Main storage
12 Control unit
15 Full chan logout
16-18 Reserved (000)
19 Sequence code
20 Unit status
21 CCW addr. and key
22 Channel address
23 Device address
24-25 Type of termination
00 Interface disconnect
01 Stop, stack or normal
10 Selective reset
11 System reset
27 (I) Interface inoperative
28(A) I/O-error alert
29-31 Sequence code

EXTERNAL DAMAGE CODE (hex F4)

Bits	Meaning
0-1	Reserved (zeros)
2	External secondary report
3	Channel not operational
4	Channel-control failure
5	I/O-instruction timeout
6	I/O-interruption timeout
7-31	Reserved (zeros)

MACHINE-CHECK INTERRUPTION CODE (hex E8)

MC conditions	000 00	Time	Stg. error	0	Validity indicators
0	9	14	16	19	20 31

0000 0000 0000 00	Val.	MCEL length
32	46	48 63

0 System damage
1 Inst.-proc'g damage
2 System recovery
3 Intvl-timer damage
4 Timing-facil. damage
5 External damage
6 Not assigned (0)
7 Degradation
8 Warning
14 Backed up
15 Delayed
16 Uncorrected
17 Corrected
18 Key uncorrected
20 PSW bits 12-15
21 PSW mask and key
22 Prog. mask and CC
23 Instruction address
24 Failing-stg. address
25 Region code
26 External-damage code
27 Floating-pt registers
28 General registers
29 Control registers
30 Logout
31 Storage logical
46 CPU timer
47 Clock comparator

DYNAMIC ADDRESS TRANSLATION

Dynamic Address Translation Format

			Virtual -Address Fields			
Cntl Reg 0 Bits 8 - 12	Segment Size	Page Size		Segment Index	Page Index	Byte Index
0 1 0 0 0	64K	2K	Bits 0-7 are ignored	8-15	16-20	21-31
0 1 0 1 0	1M	2K		8-11	12-20	21-31
1 0 0 0 0	64K	4K		8-15	16-19	20-31
1 0 0 1 0	1M	4K		8-11	12-19	20-31

Any other combination of bits 8-12 of control register 0 is invalid for translation. 1M-byte segments are not provided on some models; 2K-byte pages are not provided on some models.

Segment-Table Entry

PT length	0000*	Page-table origin	P	C	I
0	4	8	29	30	31

*Normally zeros; ignored on some models.
29 (P) Segment protection
30 (C) Common segment
31 (I) Segment-invalid bit

Page-Table Entry (4K)

Page-frame real address	I	EA	
0	12	13	15

12 (I) Page-invalid bit
13-14 (EA) Extended-address bits

Page-Table Entry (2K)

Page-frame real address	I	0	
0	13	14	15

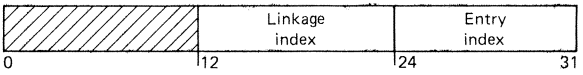
13 (I) Page-invalid bit

TRANSLATION-EXCEPTION ID (hex 90)

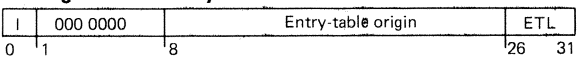
Interruption Code	ID
0010,0011	0 secondary address, 1-7 zeros, 8-31 address
001C	0 old space-sw-event ctl bit, 1-15 zeros, 16-31 old PASN
0020,0021,0024,0025	0-15 zeros, 16-31 ASN
0022,0023	0-11 zeros, 12-31 PC number

DUAL-ADDRESS-SPACE CONTROL

Program-Call Number



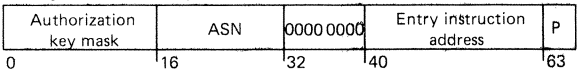
Linkage-Table Entry

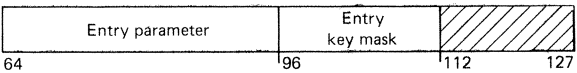


0 (I) LX-invalid bit

26-31 (ETL) Entry-table length

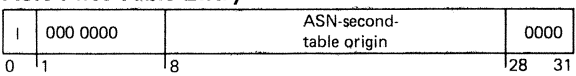
Entry-Table Entry





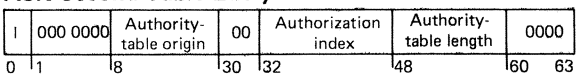
63(P) Entry problem state

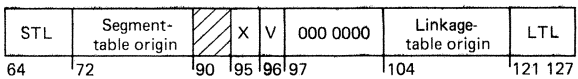
ASN-First-Table Entry



0 (I) AFX-invalid bit

ASN-Second-Table Entry





0 (I) ASX-invalid bit

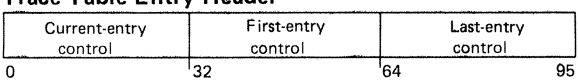
64-71 (STL) Segment-table length

95 (X) Space-switch-event bit

96 (V) Subsystem-linkage control

121-127 (LTL) Linkage-table length

Trace-Table-Entry Header



HEXADECIMAL AND DECIMAL CONVERSION

From hex: locate each hex digit in its corresponding column position and note the decimal equivalents. Add these to obtain the decimal value.

From decimal: (1) locate the largest decimal value in the table that will fit into the decimal number to be converted, and (2) note its hex equivalent and hex column position. (3) Find the decimal remainder. Repeat the process on this and subsequent remainders.

Note: Decimal, hexadecimal, and binary equivalents of all numbers from 0 to 255 are listed in the code tables.

HEXADECIMAL COLUMNS											
6		5		4		3		2		1	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,069	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
0 1 2 3		4 5 6 7		0 1 2 3		4 5 6 7		0 1 2 3		4 5 6 7	
BYTE				BYTE				BYTE			

POWERS OF 2

2^n	n
256	8
512	9
1 024	10
2 048	11
4 096	12
8 192	13
16 384	14
32 768	15
65 536	16
131 072	17
262 144	18
524 288	19
1 048 576	20
2 097 152	21
4 194 304	22
8 388 608	23
16 777 216	24
33 554 432	25
67 108 864	26

$2^0 = 16^0$
$2^4 = 16^1$
$2^8 = 16^2$
$2^{12} = 16^3$
$2^{16} = 16^4$
$2^{20} = 16^5$
$2^{24} = 16^6$
$2^{28} = 16^7$
$2^{32} = 16^8$
$2^{36} = 16^9$
$2^{40} = 16^{10}$
$2^{44} = 16^{11}$
$2^{48} = 16^{12}$
$2^{52} = 16^{13}$
$2^{56} = 16^{14}$
$2^{60} = 16^{15}$

POWERS OF 16

16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

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