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IBM System/370 Model 158 Functional Characteristics

This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

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37, 38	61, Back cover
39 (added), 40 (added)	

Pages 35 through 43.3 have been renumbered to incorporate revised material from former pages 39 through 43. It is suggested that this material be read in its entirety.

All pages to which a change has been made carry a revision notice in the upper margin. A technical change to the text is indicated by a vertical line to the left of the change.

Summary of Amendments

This newsletter adds information about the IBM System/370 Model 158 attached processor system.

Note: *Please file this cover letter at the back of the manual to provide a record of changes.*

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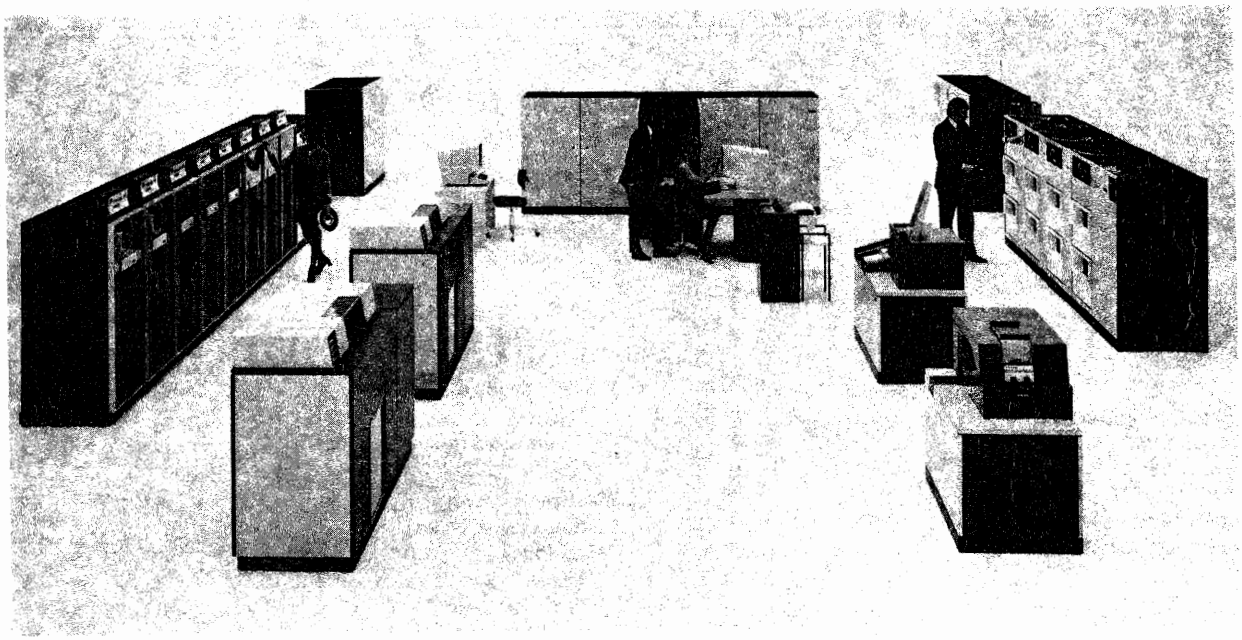


IBM System/370 Model 158 (Representative Uniprocessor Configuration)

The IBM System/370 Model 158 is a medium-size, high-performance data processing system that extends and enhances the basic System/370 concept. The Model 158 incorporates many advanced features such as integrated monolithic main storage, virtual storage capability, enhanced timing facilities, integrated storage controls, and a display console. These improvided functional capabilities encourage expanded applications for all large-scale users.

The basic components of the System/370 Model 158 are the CPU (the IBM 3158 or 3158-3 Processing Unit), the display console, and an optional console printer. Included within the 3158 and 3158-3 are the processor, main storage, buffer storage, at least one byte-multiplexer channel, and two block-multiplexer channels. Input/output (I/O) devices are attached to the channels via control units.

The 3158 and 3158-3 are available in eight main storage capacities:

3158	*3158-3*	*Main Storage Capacity*
I, AP1, MP1	U31, A31, M31	524,288 bytes (512K)
J, AP2, MP2	U32, A32, M32	1,048,576 bytes (1,024K)
JI, AP3, MP3	U33, A33, M33	1,572,864 bytes (1,536K)
K, AP4, MP4	U34, A34, M34	2,097,152 bytes (2,048K)
KJ, AP5, MP5	U35, A35, M35	3,145,728 bytes (3,072K)
L, AP6, MP6	U36, A36, M36	4,194,304 bytes (4,096K)
LJ, AP7	U37, A37, M37	5,242,880 bytes (5,120K)
LK, AP8	U38, A38, M38	6,291,456 bytes (6,144K)

A high-speed buffer is standard; its storage capacity is 8,192 bytes (8K) in the 3158, and 16,384 bytes (16K) in the 3158-3.

The 3158-3 is an advanced version of the 3158, which can be converted to a 3158-3. Information within this manual applies to both models unless noted otherwise. Differences between the two are discussed where relevant.

For input/output operations, one byte-multiplexer channel (channel 0) and two block-multiplexer channels (channels 1 and 2) are standard. Optional features provide for up to three additional block-multiplexer channels (channels 3, 4, and 5). Alternatively, with channel 3 installed, channel 4 may be used as a second byte-multiplexer channel. For details, see Figure 1.

VIRTUAL STORAGE

Regardless of the real storage capacity, when the Model 158 is operating in extended control (EC) mode with dynamic address translation invoked, all logical addresses within the 24-bit addressing scheme of System/370 are available. Therefore, the maximum logical (virtual) address is 16,777,215. System/370 Model 158 is designed primarily to support this virtual storage environment; it is not subject to restraints normally imposed on programming applications by the amount of available storage, and the operational flexibility of the installation is enhanced.

MULTIPROCESSOR SYSTEM

Multiprocessing is a logical extension of multiprogramming. A Model 158 multiprocessor (MP) system uses two multiprocessing versions of the 3158 or 3158-3, joined by an IBM 3058 Multisystem Unit. The CPUs can execute programs simultaneously while sharing total system resources, including data. Benefits derived from multiprocessing include operational efficiency and flexibility and improved system availability. The most critical component of the MP system is the control program. CPUs are considered to be system resources as are I/O devices and storage.

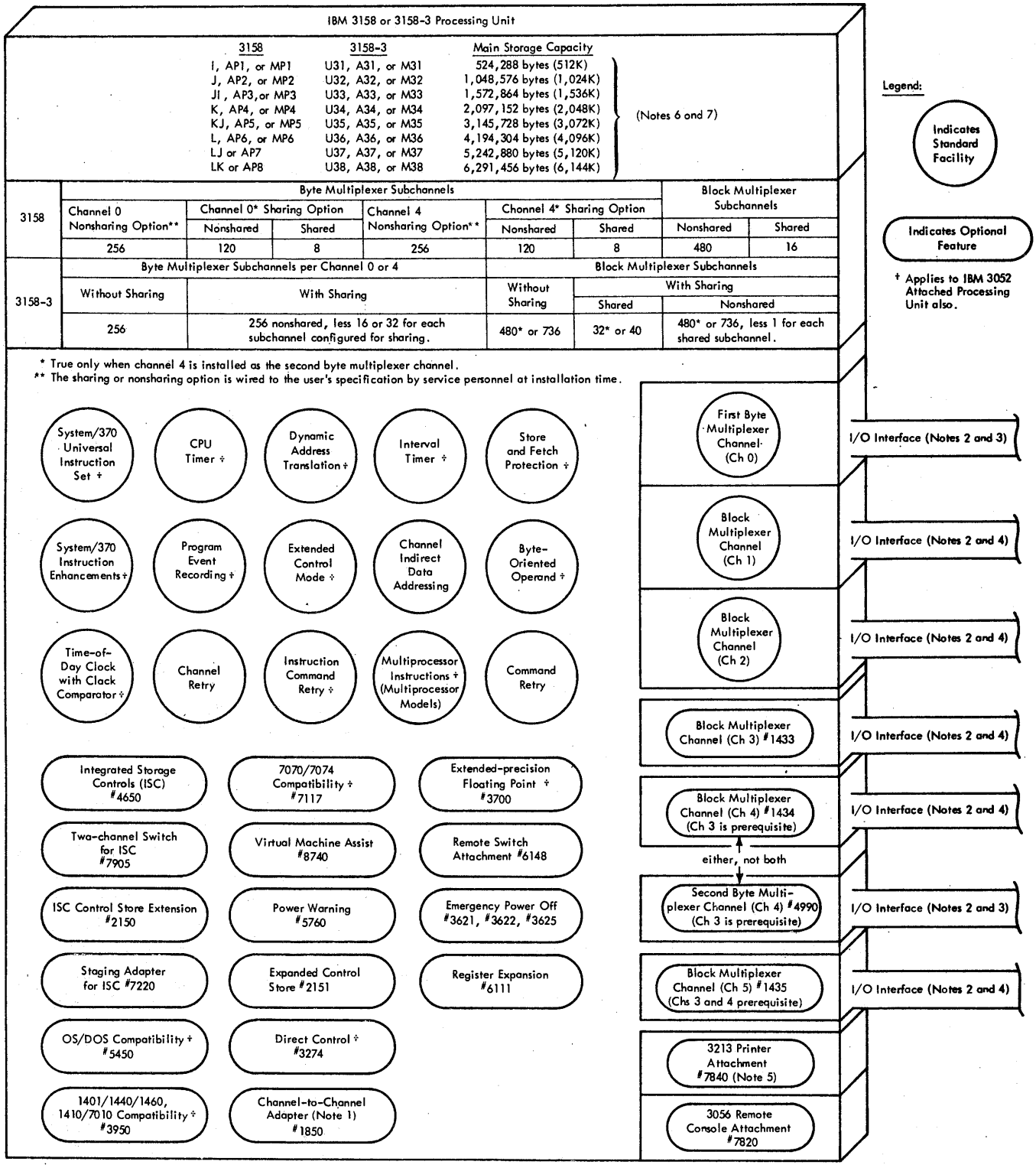
ATTACHED PROCESSOR SYSTEM

The instruction-processing capabilities of a Model 158 can be significantly increased by adding an IBM 3052 Attached Processing Unit (APU) Model 1 to an upgraded 3158 or 3158-3 Processing Unit (CPU). The APU executes programs concurrently with the CPU and shares the CPU's main storage, channels, and input/output facilities. This tightly coupled configuration, called the Model 158 attached processor (AP) system, is designed for the user who requires instruction execution capability beyond that available with the uniprocessor system but whose needs do not presently justify a Model 158 multiprocessor system. The attached processor system can provide internal performance that is generally 50 to 80% greater than that of a uniprocessor Model 158.

PROGRAMMING SUPPORT

Extended control (EC) mode with dynamic address translation (DAT) is supported by OS/VS1, OS/VS2, VM/370, and DOS/VS. Multiprocessing is supported by OS/VS2 (MVS). Attached processing is supported by the AP first-customer-shipment release level of OS/VS2 (MVS) modified by a selectable unit. Extended storage (5,120K and 6,144K) is supported by OS/VS2 for both uniprocessor and attached processor systems and by VM/370 and OS/MVT for uniprocessor systems only.

In addition, OS/360 and DOS/360 (in hardstop mode) provide support in System/370 basic control (BC) mode.



Notes:
1. The channel-to-channel adapter (one per system, attached to byte or block multiplexer channel) permits interconnection of two channels. One control unit position on the Model 158 channel can connect to one control unit position on any other System/370 or System/360 channel. Only one adapter is needed per connection; it counts as one control unit on both channels.
2. Attaches as many as eight control units; available subchannels are shown on chart.
3. Operates in either burst mode or byte mode; multiplexing capability on bytes, groups of bytes, or blocks.
4. Operates in burst mode only; multiplexing capability on blocks or multiple blocks. Available subchannels are shown on chart.
5. The 3213-1 Printer is optional in display mode, mandatory in printer-keyboard mode.
6. A multiprocessor system consists of two multiprocessing models of 3158 or 3158-3 connected by a 3058 Multisystem Unit. The storage capacities of both CPUs must be equal and no more than 4,096K in any system using two 3158s; they need not be equal in a system using two 3158-3's if the main storage of each CPU is other than 512K or 1,536K. Maximum main storage capacity is 8,192K.
7. An attached processor system consists of an IBM 3052 Attached Processing Unit (with an IBM 3056 Remote System Console) connected to a Model A-series 3158. The 3052 contains no main storage or channels.

Figure 1. Model 158 Configurator

COMPATIBILITY

The Model 158 is upward program compatible with models of IBM System/360 and System/370. All programs written for System/360 and System/370 will operate on the Model 158 with the following exceptions:

1. Time-dependent programs.
2. Programs written to cause program checks deliberately.
3. Programs using machine-dependent data (for example, machine logs).
4. Programs using the ASCII bit.
5. Programs that depend on the contents of the extended logout area (decimal 128-1152 for the Model 158).
6. Programs that depend on devices or architecture not implemented in the Model 158.
7. Programs using any other model-dependent functions as specified in *IBM System/370 Principles of Operation*, GA22-7000.
8. In EC mode, programs that modify CCWs during channel program execution.

REMOTE SUPPORT FACILITY

If the system malfunctions, this facility provides the customer with the combined expertise of local and remote IBM System/370 Model 158 support specialists. This is achieved by linking the system, via a teleprocessing network, to the field technical support center. The advantages of this support technique are evident; however, the customer's data security and privacy are subject to some exposure while the remote support facility is in use.

The security measures enlisted to ensure minimal exposure are as follows:

1. The customer's security (console) key is required in order to display the teleprocessing link frame.
2. The teleprocessing link is established only after thorough verification of the identity of both the customer and the remote support center.
3. Each mode of remote support (remote program, remote monitor, and remote control dedicated) is initiated and identified at the customer's installation. When the teleprocessing link is established for remote monitor or remote control dedicated mode, a header message containing the maintenance strategy level for the customer is displayed onsite and at the remote support center. These levels, which are determined by the customer and altered only at his request, are:
   a. Customer allows concurrent maintenance.
   b. Customer allows stand-alone maintenance only.
   c. Security account: the system must be cleared of all customer data prior to remote support, including making devices that contain security data not-ready.
4. Every operation initiated at the remote center can be monitored by the customer.
5. The teleprocessing link can be disconnected at any time at the customer's installation by pressing the remote pushbutton on the control panel.

One of three modes of operation can be selected at the discretion of the service representative and with the customer's approval.

1. *Remote Program*: This mode is identical to the RETAIN/370 link and provides all of the online test executive program (OLTEP) security facilities. For example, to protect against accidental modification of customer data, OLT(S)EP diagnostic programs restrict writing to noncustomer volumes or to designated areas of customer volumes. Also, to protect against disclosure, OLT(S)EP diagnostic programs read/transmit the smallest amount of data that permits satisfactory diagnosis.
2. *Remote Monitor*: This mode allows the remote center to monitor the data being displayed on the console display. The monitoring may take place concurrently with the customer's operation, which therefore displays customer data to the remote center.
3. *Remote Control Dedicated*: In this mode, all console functions, both service and operational, are available to the remote center. The customer console is inoperative; however, it is possible for the customer to terminate the operation by pressing the remote pushbutton. It should be noted that all data sets on the system could be accessed by the remote center; however, every operation initiated at the remote center can be customer-monitored. This mode will normally be used with the system dedicated to the service personnel, although it is possible to use it concurrently with customer operation.

All modes of operation are independent of operating system release levels. This facility is not dependent on the CPU, I/O, or channels being operational.

STANDARD FACILITIES AND OPTIONAL FEATURES

For a description of the standard facilities and optional features for the Model 158, see "Facilities and Features Summary."

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The following are 3158 characteristics that are different from the 3158-3:

- Buffer storage contains two 4K compartments, rather than four.
- Space is reserved on a halfblock (16-byte) basis, rather than on a block basis.
- The buffer assignment algorithm uses a single least recently used (LRU) bit rather than six algorithm bits.
- There is one LRU bit for every block and halfblock address (two entries), rather than six bits for every block address (four entries).

The index array is interrogated during each CPU storage reference to determine if the referenced data is in the buffer. The index array is cycled at the referenced block address (both block and halfblock addresses on the 3158), and the four entries (two on the 3158) read out are compared to the referenced row and valid bit. An equal comparison of the entries (row and validity) determines that the buffer compartment contains the wanted data. An initial program reset or initial program load (IPL) sets the index array row addresses to valid parity, turns off all valid bits, and turns on the OK bits.

The system can continue to operate even when a component in the buffer fails. When a failure is detected, the OK bit for that block is turned off, and all subsequent fetches for that block are made directly to main storage. A machine check occurs when a block in the buffer is deleted for error-recording purposes.

Virtual Storage

Virtual storage is an image of 16,384K (16,777,216 bytes) created by the control program. It is functionally equivalent to the real or main storage of the system, and its contents are physically located in main storage or auxiliary disk storage.

Storage Allocation

Real (main) storage is allocated by the system control program on a dynamic paging basis. An entire program need not be resident in main storage throughout its execution. Instead, page size (2K or 4K) portions are transferred into main storage (in any available location) only as needed. Each page of main storage becomes available for reallocation to another job or task upon completion of the task, when the task is no longer using that page, or upon request for that storage space by a higher priority task.

Translation Lookaside Buffer (TLB)

Needless retranslations are avoided because the translation lookaside buffer (TLB) stores up to 128 logical-to-real pairs of address translations. Each entry in the TLB represents either a 2K or a 4K area, depending on the page size specified.

CPU storage references requiring translation are first compared with the TLB to determine whether a current translation exists. If one exists, the corresponding real address in the TLB is used, as described in "Buffer Storage and Index Array." If no translation exists, translation is performed and the result is stored in the TLB.

Translation generates real addresses for the segment and page table entries. The fetching of these entries interacts with the buffer storage and index array like any other CPU storage reference. A new translation replaces a previous translation at that entry.

The TLB is purged of all entries:

1. When a purge TLB (PTLB) instruction is executed.
2. When a load control (LCTL) instruction modifying a segment or page size in control register 0 (CR0) is executed.
3. When the enter key on the keyboard is pressed.
4. When the store control character is touched with the light pen.
5. When a machine check occurs.
6. When a program reset is executed.
7. When an initial program reset is executed.

A partial purge of the TLB occurs if an LCTL instruction modifies CR1.

Reference and Change Recording

Three bit positions are added to the storage protection key associated with each 2K block of real storage. Two of the bits provide for reference and change recording; the third is used as a parity bit.

For complete details on the use, setting, and resetting of bits, see *IBM System/370 Principles of Operation*, GA22-7000.

Channel Operations

The channels share control storage and data flow paths with CPU functions to perform I/O operations. Many channel functions are performed by the shared hardware, using a break-in technique to service I/O requests for the CPU and main storage.

The channels store and fetch all data to and from main storage, using real addresses. Channel data does not enter the buffer (see Figure 3). When a channel stores data in main storage, the index array is interrogated; if the data corresponding to that storage address is in the buffer, the valid bit for the buffer entry is turned off.

Since the channels do not implement dynamic address translation, CCWs in virtual storage must be translated by the control program before they are executed. To allow the designation of contiguous areas of virtual storage to be mapped into noncontiguous areas of real storage, indirect data addressing is provided. For complete channel information, see *IBM System/370 Model 158 Channel Characteristics*, GA22-7012, and *IBM System/370 Principles of Operation*, GA22-7000.

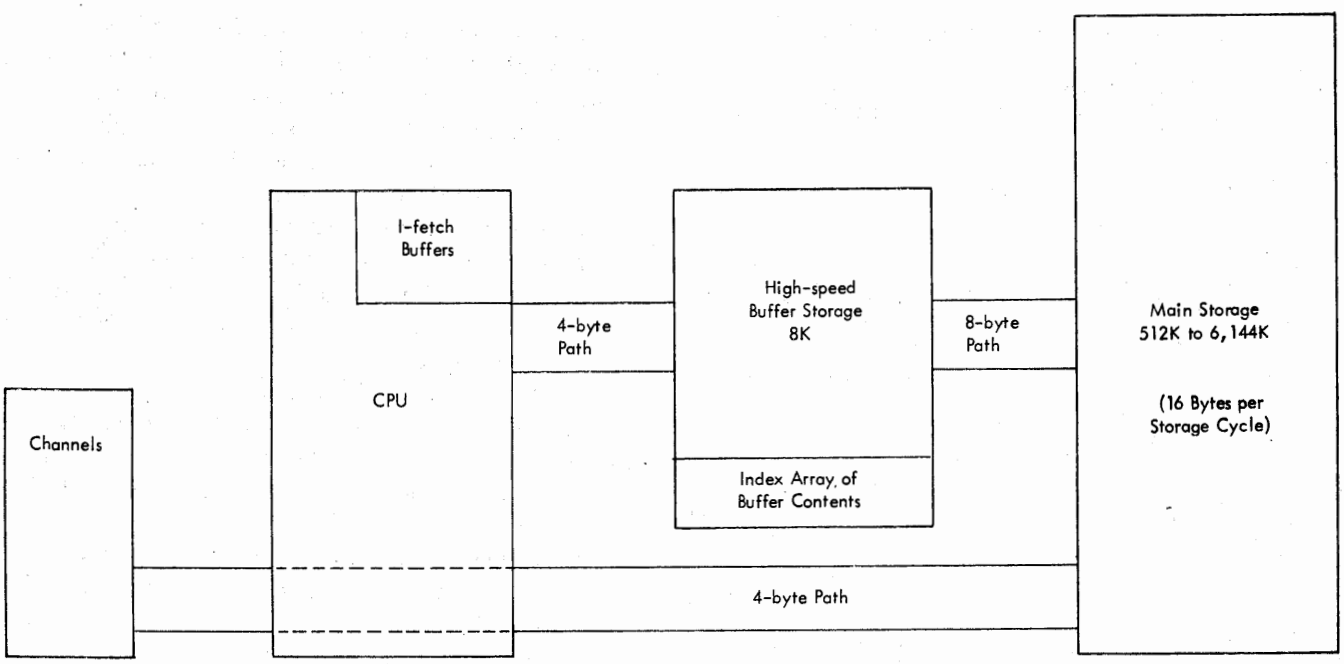

Figure 3. Conceptual Data Flow in Model 158

Program Event Recording

Program event recording (PER) is a valuable program debugging aid. PER is enabled by turning on bit 1 of the EC mode program status word (PSW). Control registers 9-11 control the selection of registers and storage locations. For details concerning PER, see *IBM System/370 Principles of Operation*, GA22-7000.

Store Status Facility

The store status facility allows control information to be preserved and stored after a reset operation. The facility may be selected by touching the light pen to the Store Status control character on the manual frame immediately following the reset function.

System Mask Changes

Two new instructions, store then AND system mask (STNSM) and store then OR system mask (STOSM), selectively enable or disable system mask bits in the PSW. The original value of the system mask is stored for later restoration. When the set system mask (SSM) instruction is executed and the SSM control bit (bit 1 of control register 0) is 1, a special operation exception is caused.

For a complete discussion of these changes, see *IBM System/370 Principles of Operation*, GA22-7000.

The system console of the Model 158 provides facilities for operating and controlling the system and for displaying system status. A small control panel, a keyboard, a cathode-ray tube (CRT) display, and a console disk file constitute the major operational components of the console. A console printer is available.

Most of the switches and pushbuttons normally associated with an operator's console are replaced by appropriate designations that are selectively displayed on the console screen. The entire system status cannot be displayed at one time; information is grouped logically into various frames (display categories), which are displayed on the CRT one at a time. Most of these frames are used as service aids by service personnel; only four (configuration, manual, program and alter/display) are used by the operator. Thus, advanced system maintenance and diagnostic procedures are combined with ease of operation to provide a high degree of efficiency.

The system console functions in one of two modes, depending on the operating system console support mode selected at initial microprogram load (IMPL) time. In systems providing device independent display operator console support (DIDOCS), the console can operate as a graphics display console with keyboard and selector (light) pen input and CRT output. The optional 3213 Printer provides hard-copy output. Alternatively, printer-keyboard mode may be selected with or without DIDOCS support, and the console then functions as a console I/O device similar to a 3215 Printer-Keyboard. When the console is operating in printer-keyboard mode, system-operator messages appear on the display screen but they can be displaced by subsequent messages before being acknowledged by the operator. The primary means of system communication in printer-keyboard mode are the 3213 Printer and the console keyboard.

The console file, located adjacent to the kneespace under the console keyboard, provides the microprograms required for the initial microprogram load (IMPL) of the reloadable control storage (RCS) of both the CPU and the console processor. A similar file, located in the rear of the console, is used for service and diagnostic purposes. Switches for the channel-to-channel adapter (CTCA) and for the integrated storage controls (ISC) are also located in the console file enclosure. An integrated data adapter for remote support of the Model 158 is standard on the console (see "Remote Support Facility" in the Introduction).

REMOTE SYSTEM CONSOLE

Another console, the IBM 3056 Remote System Console, is available as a special feature. It allows users to have operator control of a Model 158 from as much as 150 feet from the CPU. This enables users to have CPUs away from the center of activity, and thus permits more flexible organization of space for increased efficiency and convenience. For example, the 3056 can be located closer to the other system components which require attention. This console can be particularly worthwhile to users with multiple System/370s, enabling them to centralize operations.

The 3056, mounted on a standalone base, contains a CRT display and keyboard, identical to those on the main console. However, it has no light pen or printer. This console provides the operator with remote operational control over the system, including the ability to IPL, display the maintenance frames, and use the alter/display function. Controls not provided at the remote system console include those for system power on, IMPL, TOD clock, lamp test, and system power off.

The 3056 does not connect to a channel, but instead is a slave to the main console, and operates in parallel with it. The CRTs show the same displays, and responses can be made from either keyboard.

The remote system console has a disable key switch similar to that on the main console. When the main console key is locked and the remote system console key is unlocked, the remote operator has unrestricted access to all frames. When the remote system console key is locked, the remote operator has access only to the program frame, and is prohibited from performing an IPL or from altering programs or data. When the main console key is unlocked, the remote system console is inoperative.

CONSOLE SUPPORT

Device independent display operator console support (DIDOCS) for the CRT is the same as that provided for the IBM 3277 Display Station Model 2 supported by OS Release 21. This includes the selector pen (also referred to in this manual as the light pen), the keyboard, and the display area of twenty-four 80-character lines (the twenty-fifth line is used by system functions and is independent of DIDOCS).

The 3213 Console Printer is supported as an output-only console under multiple console support (MCS) or its equivalent.

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The Model 158 offers two multiple-processor systems: the Model 158 multiprocessor (MP) system and the Model 158 attached processor (AP) system.

MULTIPROCESSOR SYSTEM

Multiprocessing permits two Model 158 systems to function with a single operating system in a shared main-storage environment, and provides shared I/O and floating storage-addressing capabilities.

The Model 158 MP system consists of two 3158 or 3158-3 Processing Units (both multiprocessor models), an IBM 3058 Multisystem Unit, and I/O devices with shared and nonshared control units. The system has shared main storage, as well as configuration, partitioning, and synchronization facilities.

Each CPU can function independently when in the uniprocessor (UP) mode.

System availability is increased through better use of resources. Required maintenance may be performed with reduced effect on the system operations. When servicing is required on the MP system, a maintenance subsystem consisting of a processor, channels, adequate storage, and I/O can be configured to perform the maintenance function. In general, this is accomplished by use of manual reconfiguration and vary offline facilities.

Both CPUs of an MP system must be either 3158s or 3158-3s. If two 3158s are used, their main storage capacities must be equal. If two 3158-3s are used, their storage capacities can be unequal. All features announced for the Model 158 are available for installation on both CPUs. Channels are dedicated to the CPUs to which they are attached; devices on the CPUs may be shared if the two-channel switch feature is installed.

The Model 158 multiprocessor system is available in eight storage capacities. Six symmetric (equal) storage configurations are as follows:

	Multiprocessors	*Units*	*Logical Units of Floating Storage Addressing*
1,024K	2 Model MP1s or M31s	4 –	256K logical units with 512K physical partitioning
2,048K	2 Model MP2s or M32s	4 –	512K logical units with 1,024K physical partitioning
3,072K	2 Model MP3s or M33s	6 –	512K logical units with 1,536K physical partitioning
4,096K	2 Model MP4s or M34s	8 –	512K logical units with 2,048K physical partitioning
6,144K	2 Model MP5s or M35s	6 –	1,024K logical units with 3,072K physical partitioning
8,192K	2 Model MP6s or M36s	8 –	1,024K logical units with 4,096K physical partitioning

Asymmetric (unequal) storage configurations can be put together with any two-unit combination of M32 (1,024K), M34 (2,048K), M35 (3,072K), and M36 (4,096K) models.

The physical dimensions of the Model 158 multiprocessor system are equivalent to two uniprocessor systems and the 3058 Multisystem Unit on which the configuration control panel is mounted (Figure 19.1).

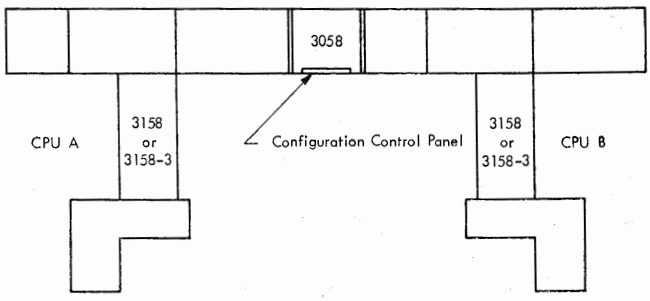

Figure 19.1. Example of a Model 158 Multiprocessor System (Plan View)

The following items discuss various areas in which multiprocessing differs from uniprocessing, both architecturally and in hardware implementation.

Prefixing

Each CPU in a shared-storage multiprocessing environment requires an area of storage to be used for permanently assigned locations and logout areas. Since there is only one set of storage locations with these addresses in shared main storage, a means of assigning them to two different storage areas, one for each CPU, is necessary. Prefixing is the technique used.

Prefixing in the Model 158 provides the means of assigning real addresses 0 to 4095 to any storage area, starting at an address that is a multiple of 4096. Each CPU has a private page frame allocated to it in virtual queue space for use as a permanent storage area (PSA). The real storage address for each CPU is placed in bits 8-19 of the prefix register located in the storage control unit (SCU) of that CPU. *Note: Real* addresses 0 to 4095 for each CPU are used by the nucleus initialization program and other CPU functions. The prefix register may be altered or displayed by use of the alter/display function (see "Alter/Display Frame").

Prefixing operates as follows: Whenever a CPU refers to a storage address in the range of 0 to 4095 (the high-order 12 bits, 8-19, of the effective storage address are 0's), the contents of the prefix register for that CPU replace bits

8-19 of the effective address. The new address will then point to a location in the PSA of that CPU. This is forward prefixing. When a CPU refers to an address in the 4K block that is pointed to by its prefix register (that is, an address in its own PSA), 0's are substituted for bits 8-19 of the effective address so that an address range of 0 to 4095 results. This is reverse prefixing. The prefix is applied to references made by the CPU including hardware-generated addresses such as the interval timer and PSWs. References made by a channel to channel command words and I/O data are not prefixed.

Signaling and Response between CPUs

Signaling and response between CPUs is provided by use of the signal processor (SIGP) instruction and appropriate hardware between the CPUs. The CPU receiving the signal decodes the order, performs the specified operation, and responds to the signaling CPU. (Note that a CPU may signal itself by inserting its own address in the instruction.) Nine orders are used for communication between CPUs. They are specified in bit positions 24-31 of the second operand address of the SIGP instruction and are encoded as follows:

Code	*Order*
(00)	(Invalid)
01	Sense
02	External call
03	Emergency signal
04	Start
05	Stop
06	Restart
07	Initial program reset
08	Program reset
09	Stop and store status
(0A-FF)	(Invalid)

Refer to *IBM System/370 Principles of Operation*, GA22-7000, for details concerning the signal processor instruction.

Shared Storage

Communication between CPUs becomes active when both CPUs have read a valid shared-storage configuration from the configuration control panel. This ensures that all references to shared storage access the most current data.

Malfunction Alert

When either CPU enters the check-stop state, a malfunction alert signal is sent to the other CPU. This signal generates a request for an external interruption. The interruption request remains pending until the interruption is taken or until the system is reset. If the interruption is taken, the address of the failing CPU is stored in locations 132-133, with an interruption code of hex 1200 stored in locations 134-135.

Time-of-Day (TOD) Clock

When the system is in MP mode, the oscillator in CPU A (hex address 0000) sends a pulse to CPU B (hex address 0001) to enable both clocks to run as one. To facilitate the programming-dependent synchronization of the time-of-day clocks, a sync pulse is transmitted each second between storage control units. This pulse can be used during synchronization to restart the TOD clock. In UP mode, the clocks run independently.

Configuration Control Panel

The configuration control panel located on the configuration control unit controls the system mode, main storage and I/O unit allocation, floating storage addressing, and system configuration. The panel contains the system mode switch, valid configuration lights, the enter configuration (ENTER CONFIG) pushbutton, a floating address switch and two storage allocation switches for each storage unit, and I/O unit allocation switches. (See Figure 19.2.)

System Mode Switch

The system mode switch is used to allow or disallow communication between CPUs in conjunction with the enter configuration pushbutton. If the ENTER CONFIG pushbutton is pressed when the switch is in the MP position, the signals associated with communication between CPUs can be transmitted. If the switch is set to UP, no signals can be transmitted between CPUs.

Storage Allocation Switches

Two storage allocation switches, one per CPU, are associated with each floating storage address rotary switch. Each storage allocation switch enables or disables the operation of the associated CPU with the storage unit when the ENTER CONFIG pushbutton is pressed.

Floating Storage Addressing

There is one floating storage address rotary switch per storage range assignment. Address ranges in increments of 256K, 512K, or 1,024K may be assigned, depending on the total storage capacity.

Enter Configuration (ENTER CONFIG) Pushbutton

The enter configuration pushbutton is used to enter the states of the system mode switch, the storage allocation switches, and the floating storage allocation switches into the CPUs.

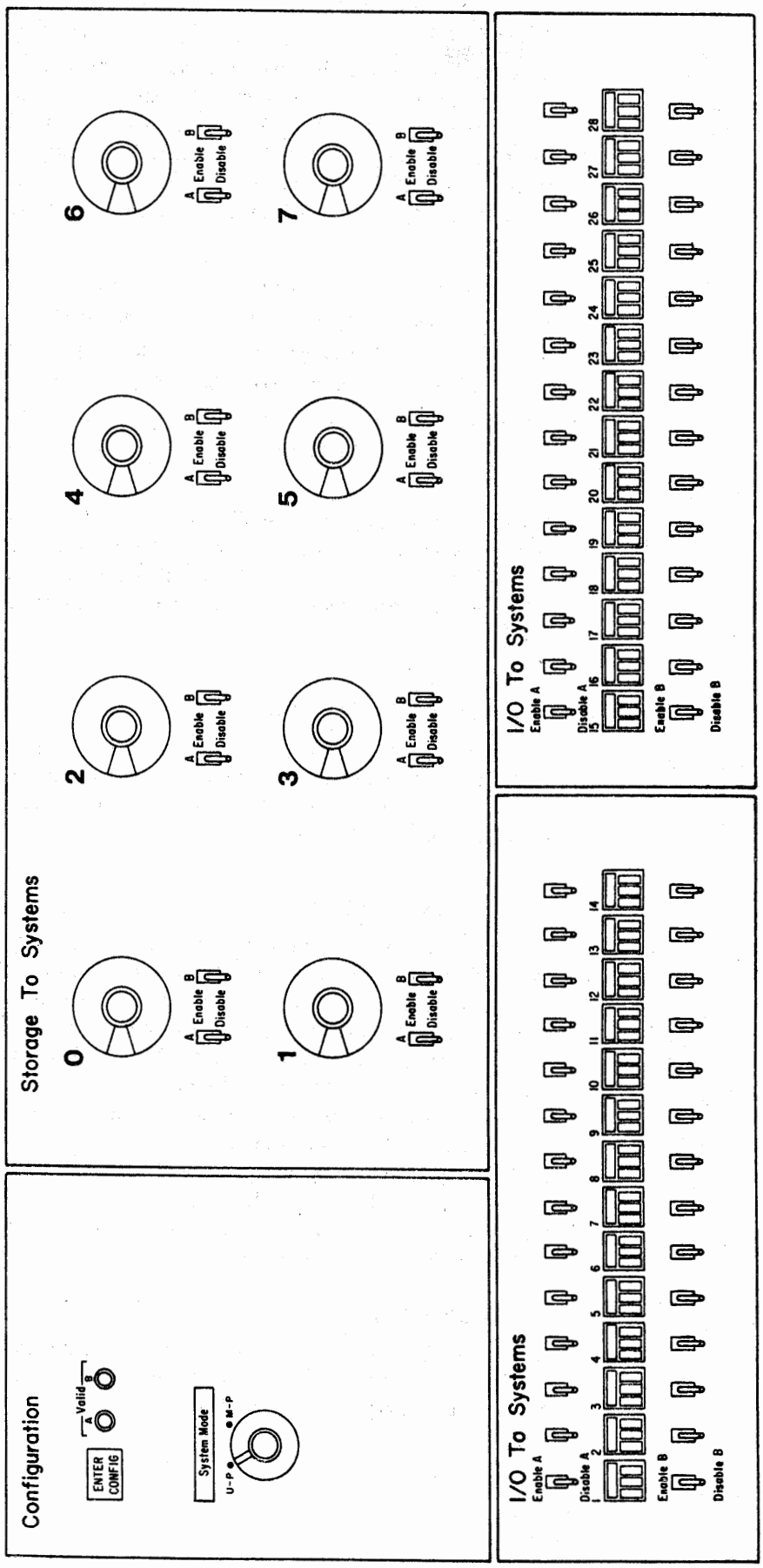

Figure 19.2. Model 158 MP Configuration Control Panel

Valid Configuration Indicators

Two valid configuration indicator lights, one for each CPU, are located on the configuration control panel. They indicate whether a valid system configuration has been set on the panel. Pressing the ENTER CONFIG pushbutton has no effect on a CPU whose valid indicator is off.

The indicators are turned off if:

- The system mode switch is set to MP and more than one floating storage address switch is set to one address range.
- Power is off on one CPU (that CPU's indicator will be turned off).
- A system is configured with storage but without a storage unit 0.
- The system mode switch is set to UP and a storage unit is assigned to both CPUs.
- The system mode switch is set to MP and a storage unit is assigned to one CPU but not to the other.

I/O Allocation Switches

Up to 28 pairs of I/O allocation switches are available; of these, 14 pairs are optionally available. With the two-channel switch and remote switch attachment features installed, these switches provide for the sharing of control units. They operate independently of the enter configuration pushbutton in enabling or disabling the control units for the particular CPU and channel.

Configuration Restrictions

Before configuring a CPU into the system, the CPU being brought into the running system must have had the reset/clear function invoked manually.

To vary a CPU online, a SIGP initial program reset function must be issued by the operating system before restarting the "varied-on" CPU. This must be done to synchronize the storage protection keys.

Failure to observe these restrictions will cause unpredictable results.

In addition, when performing the vary online function of a storage range, the operating system must validate that storage increment before using the new storage. Otherwise, residual errors may result in system damage. Set key instructions must be issued for the storage range varied online before using the new storage.

Manual Controls

All manual controls of the multiprocessor system function as in the uniprocessor system except system reset, clear control switch, load, and clock security switch. When the system is operating in MP mode, the signals are propagated to the other CPU. The following table summarizes the effects of reset, reset clear, load, and load clear functions:

	Effect	
Function	*Local*	*Remote*
System reset (normal)	Program reset	Program reset
System reset (clear)	System clear	Initial program reset
Load (normal)	Initial program reset	Program reset
Load (clear)	System clear	Initial program reset
PSW restart	Initial program reset	Program reset

When the system is operating in MP mode, the TOD clock is secure only when the clock security switches are secure on both CPUs. Both TOD clocks are enabled for setting if either of the clock security switches is in the enable set position.

System Control Panel Features

The system control panel (Figure 5) in a 3158-3 multiprocessing system provides additional capability, through the use of the remote/local clock switch and the remote clock indicator.

Remote/Local Clock Switch

This two-position lever switch allows main storage of the local CPU to be synchronized and timed with the clocks of the remote CPU. (The terms *local* and *remote* are relative. The local CPU, for example, is the one whose control panel is actually being operated; the remote CPU is, at that time, the other CPU.) The switch in the remote position (up) enables the remote CPU (and a segment of the local CPU's main storage, if desired) to stay online. The local CPU and console may then be powered-down for maintenance, while main storage of the local CPU remains powered-up and available to the remote CPU. In normal operation, this switch is in the local position (down).

Remote Clock Indicator

Used in conjunction with the remote/local clock switch, this indicator lights when the remote clocks are being used to time main storage of the local CPU.

ATTACHED PROCESSOR SYSTEM

The Model 158 attached processor (AP) system (Figure 19.3) consists of an IBM 3052 Attached Processing Unit (APU), a Model A-series 3158 or 3158-3 Processing Unit (CPU), and an IBM 3056 Remote System Console. The system operates under a single system-control program and can increase internal performance by 50 to 80% over that of the uniprocessor system.

The 3052 APU shares the CPU's main storage, channels, and I/O devices.

A Model A-series CPU permits attachment of the APU and its control lines to the CPU. An installed 3158 or 3158-3 may be upgraded to a Model A-series version.

The 3056 console attaches to the service processor of the APU and provides the display and keyboard for APU diagnostic and maintenance purposes. If the user wants a remote console for system use, another 3056 can be attached to the CPU.

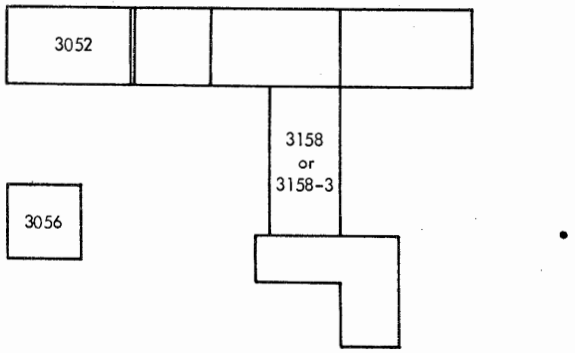

Figure 19.3. Example of a Model 158 Attached Processor System (Plan View)

The AP system is supported by OS/VS2 (MVS) with a selectable unit designed for the AP system. This system can be loosely coupled with other System/370s (either uniprocessor or multiprocessor) to better meet user needs.

The calculated 50 to 80% improvement capability in the internal performance of the AP system is based on both systems having identical features, I/O facilities, and multiprogram job streams running under MVS. Each AP system's ability to achieve its throughput potential depends on the degree that the user's applications are oriented toward multiprogram job streams.

The service processors of the CPU and APU (one each) operate independently of each other. Both are designed to retain important operation information under error conditions for later evaluation, either locally or at a remote site.

The current standard and optional features of the CPU in a uniprocessor system apply also to the CPU in an attached processor system.

3052 Attached Processing Unit

The 3052 Attached Processing Unit (APU) provides processing capabilities similar to those of the CPU. The APU uses monolithic circuitry and contains an instruction execution unit and a 16K (16,384-byte) buffer. The buffer can satisfy many requests for processor storage, making the effective storage access time much less than processor storage cycle time. The APU is metered and can be taken offline during periods of low use or for certain maintenance activities.

Optional features for the APU include direct control, extended-precision floating point, and all the Model 158 emulator features except virtual machine assist (VMA).

The APU is not attachable to the Model 158 multiprocessor system or any other System/370.

Prefixing

Prefixing is standard in an attached processor system; it is essentially the same as in an MP system. Both the CPU and APU have prefix-value registers to enable them to assign addresses 0 to 4095 to any 4K storage area, starting with any address that is a multiple of 4,096. The 12-bit prefix value in a CPU or APU can be set by execution of the set prefix (SPX) instruction and can be inspected by the store prefix (STPX) instruction. The contents of the prefix value register are set to 0 by an initial program load, an initial program reset, and by a signal processor instruction specifying either initial CPU reset or initial program reset. The prefix value register is indicated on the CRT when the CE mode of operation is selected. Application of prefixing is described in *IBM System/370 Principles of Operation*, GA22-7000.

Signaling and Response between the CPU and APU

The signal processor (SIGP) instruction provides communication between the CPU (addressed as processor 0001) and the APU (addressed as processor 0000) in an attached processor system. Nine orders are implemented for interprocessor communication. They are specified in bit positions 24 to 31 of the second operand address of the SIGP instruction and are encoded as follows:

Code	*Order*
(00)	(Invalid)
01	Sense
02	External call
03	Emergency signal
04	Start
05	Stop
06	Restart
07	Initial program reset
08	Program reset
09	Stop and store status
(0A-FF)	(Invalid)

Details concerning the SIGP instruction can be found in *IBM System/370 Principles of Operation*, GA22-7000.

CPU and APU Addresses

The store CPU address (STAP) instruction returns an ID of 0000 when executed by the APU and returns an ID of 0001 when executed by the CPU.

Details concerning the STAP instruction can be found in *IBM System/370 Principles of Operation*, GA22-7000.

Storage Control

Main storage is located in the CPU and its use is shared with the APU. Storage references are handled on a first-come, first-served basis.

Malfunction Alert

When either processing unit (CPU or APU) enters the check-stop state, a malfunction alert signal is sent to the other processing unit. This generates a request for an external interruption. The interruption request remains pending until the interruption is taken or until the system is reset. If the interruption is taken, the address of the failing processing unit is stored in locations 132-133, with an interruption code of hex 1200 stored in locations 134-135.

Time-of-Day (TOD) Clock

In AP mode, the oscillator in the APU (hex address 0000) sends a pulse to the CPU (hex address 0001) to enable both the APU and CPU TOD clocks to run as one. To facilitate the programming-dependent synchronization of the TOD clocks, a sync pulse is transmitted each second between the CPU and APU. This pulse can be used during synchronization to restart a clock.

Power Control

Power must be on to both the CPU and APU to operate as an attached processor system, but the power needs to be on only to the CPU to operate as a uniprocessor system. EPO removes power from both the CPU and APU.

STANDARD FACILITIES

Standard facilities for the Model 158 include:

System/370 Universal Instruction Set
Dynamic Address Translation
Clock Comparator
CPU Timer
Command Retry
Channel Retry
First Byte and Block Multiplexer Channels (Channels 0–2)

System/370 Universal Instruction Set

The System/370 universal instruction set includes the following enhancement instructions. They are discussed in *IBM System/370 Principles of Operation*, GA22-7000.

Compare Logical Characters under Mask (CLM)
Compare Logical Long (CLCL)
Insert Characters under Mask (ICM)
Load Control (LCTL)
Load Real Address (LRA)
Monitor Call (MC)
Move Long (MVCL)
Purge TLB (PTLB)
Reset Reference Bit (RRB)
Set Clock (SCK)
Set Clock Comparator (SCKC)
Set CPU Timer (SCT)
Shift and Round Decimal (SRP)
Store Channel ID (STIDC)
Store Characters under Mask (STCM)
Store Clock (STCK)
Store Clock Comparator (STCKC)
Store Control (STCTL)
Store CPU ID (STIDP)
Store CPU Timer (STCT)
Store then AND System Mask (STNSM)
Store then OR System Mask (STOSM)

Dynamic Address Translation

The method used to convert virtual (logical) addresses to real storage addresses is called dynamic address translation (DAT). DAT is invoked by turning on bit 5 of the PSW while the CPU is operating in extended control mode. (The user may select the extended control mode by turning on bit 12 of the PSW.) With bit 12 off, the system runs in the basic control mode, and dynamic address translation is not used. For complete information on dynamic address translation, see *IBM System/370 Principles of Operation*, GA22-7000.

Clock Comparator

The clock comparator can be used to cause an external interruption after the TOD clock passes a time specified in the executing program. The clock comparator is set by the set clock comparator (SCKC) instruction and inspected by the store clock comparator (STCKC) instruction.

CPU Timer

The CPU timer measures elapsed CPU time, and can be used to cause an external interruption after a specified amount of time has elapsed. The CPU timer is set by the set CPU timer (SCT) instruction and inspected by the store CPU timer (STCT) instruction.

Command Retry

Command retry is a control-unit-initiated procedure between the channel and the control unit. No I/O interruption is required. The number of retries is device-dependent.

Channel Retry

Channel retry is performed by machine-logic CPU retry procedures plus program-logic recovery action. Where possible, channel instructions are retried using the existing CPU retry machine logic, provided that the error occurs before the I/O command is issued to the I/O device. When the device receives the command, the channel presents a limited channel logout (LCL) to the program if an error occurs. The LCL contains information for retry of the channel instruction by programs using modified error recovery procedures. When a channel-only or channel-CPU error occurs, the entire CPU and all channels perform a logout, and CPU retry is entered. Channels affected by the error provide a channel status word (CSW) and limited channel logout (LCL) via an interruption or a condition code 1 CSW store operation.

First Byte and Block Multiplexer Channels

Channels 0-2, the first byte multiplexer channel and the first two block multiplexer channels, are provided with the basic Model 158.

OPTIONAL FEATURES

The optional features for the CPU include:

- Direct control
- Channel-to-channel adapter
- Emergency power-off control (multisystem)
- Block multiplexer channels (channels 3, 4, and 5)*
- Second byte multiplexer channel (channel 4)*
- Extended-precision floating point
- OS/DOS compatibility
- 1401/1440/1460 and 1410/7010 compatibility
- 7070/7074 compatibility
- Virtual machine assist
- Power warning
- Main storage options (1,024K, 1,536K, 2,048K, 3,072K, 4,096K, 5,120K, or 6,144K)*
- Integrated storage controls and two-channel switch for ISC
- 3213 printer attachment
- Staging adapter
- 3056 remote console attachment

*Refer to the configurator (Figure 1) for details on channel and main storage options.

Direct Control

The direct control feature provides two instructions, read direct and write direct, and six external interruption lines. The read and write instructions provide for the transfer of a single byte of information between an external device and the main storage of the system. Each of the six external signal lines, when active, sets up the conditions for an external interruption. Additional details are in *IBM System/360 and System/370 Direct Control and External Interruption Features, OEMI,* GA22-6845.

Channel-to-Channel Adapter

The channel-to-channel adapter feature allows the establishment of a loosely coupled multisystem via one control-unit position on the respective channels of the individual systems. Only one adapter may be installed on the Model 158; the attachment may be on either the byte or the block multiplexer channel.

Under program control, the channel-to-channel adapter can operate as two independent control units. Five commands, in addition to those supplied on System/360, are available to the programmer. Expanded checking facilities are also provided. Programs written for the System/360 adapter may be run if the additional features are not enabled.

Emergency Power-Off Control (Multisystem)

Emergency power-off control is required on only one of the processing units, normally the largest, in any installation composed of more than one cable-connected processing unit and/or cable-connected units that can be operated offline.

Optionally, from two to as many as twelve EPO switches can be installed (refer to Figure 1). The emergency power-off feature interconnects EPO switches to provide, in effect, a single EPO switch.

Extended-Precision Floating Point

Extended-precision floating point includes instructions designed to handle extended-precision (28-hex-digit) floating-point operands. Extended-precision operands may also be rounded to long-precision format, and long-precision operands may be rounded to short-precision format. For additional details, see *IBM System/370 Principles of Operation*, GA22-7000.

OS/DOS Compatibility

The OS/DOS compatibility feature allows the user to run System/360 Disk Operating System (DOS) control programs (including multiprogramming) under control of the System/360 Operating System (OS) in a multiprogramming environment. Refer to *Emulating DOS Under OS on IBM System/370*, GC26-3777.

1401/1440/1460 and 1410/7010 Compatibility

The 1401/1440/1460 and 1410/7010 integrated emulator programs allow the Model 158 to execute programs and programming systems originally written for 14XX or 7010 systems. The compatibility feature adds special instructions and internal logic to the Model 158. The integrated emulator programs use these facilities and the available instruction sets to execute 14XX-type instructions in a multiprogramming environment. Unlike stand-alone emulators, integrated emulators must share the CPU and I/O devices with the operating system. In a system with multiprogramming capability, however, the time lost waiting for a shared resource is much less (on the average) than the time lost by a stand-alone emulator waiting for its I/O operations to be completed. This reduction in system wait time increases total system throughput.

7070/7074 Compatibility

The 7070/7074 emulation allows the Model 158 to execute programs and programming systems originally written for the IBM 7070 and 7074 Systems.

Virtual Machine Assist

The virtual machine assist (VMA) feature improves performance on the Model 158 that is using virtual storage systems running under VM/370. This improvement is achieved by significantly reducing the amount of time VM/370 spends in the real supervisor state. This reduction is accomplished by emulation (instead of software simulation) of certain privileged operation codes used by the VS system supervisor. Emulation is also used for shadow page table maintenance and for SVC interruption handling.

The VMA feature may not operate concurrently with the 7070/7074 compatibility feature. The system operator must determine at IMPL time whether VMA or 7070/7074 compatibility is to be loaded.

Release 2 of VM/370 provides programming support.

Power Warning

The power warning feature, on the Model 158 supported by an uninterruptible power system, permits the use of controlled shutdown and recovery procedures following power line disturbances. When utility power drops 18 ± 2% below rated voltage, the feature provides an automatic interruption to the control program. Combined with OS/VS or OS/MVT programming, the power warning feature provides support for:

- Turning on the power warning bit
- Time delay before interruption
- User intercept option
- Main storage dump/restore

The uninterruptible power system provides a power reserve to take over the task of powering either the complete system, or critical components of the system, during line disturbances including complete loss of utility-furnished power. With an uninterruptible power system supporting the complete processing system, operation may continue during power failures as long as the interruption does not exceed the buffering capacity of the uninterruptible power system. The user intercept option permits the user to program (via an exit) procedures tailored to his operation.

The CPU, all channels, and control units and devices on only one channel are powered by a partial uninterruptible power system, and use of the user intercept option may be less attractive.

The elements of the power warning feature, which is field installable, are:

1. A vendor-supplied uninterruptible power system for maintaining power to the entire or critical components of the system, and a sensor to detect power line disturbances and generate a power warning signal.
2. Hardware modifications to the Model 158 to support the power warning machine-check interruption architecture.
3. Software support for the power warning machine-check interruption handler, including the dump and restore programs and the user intercept option.

Operational Characteristics: The power warning is issued when utility voltage is reduced by 18 ± 2% for a duration greater than one-half cycle. The uninterruptible power system sensor signal remains active as long as the undervoltage condition exists, and causes the CPU to generate a soft machine-check interruption. This interruption is under the control of PSW bit 13 (Machine Check Interruption Mask), and bit 7 of control register 14 (Power Warning Sub-Mask).

If the user provides an uninterruptible power system for his complete computing system, the following events will then occur:

1. The interruption will branch to a timing routine to determine if the power disturbance is transient. The duration of this timing activity is a customer option and is limited by the uninterruptible power system capacity.
2. If the disturbance is transient, control can be returned to the machine-check handler and the system continues operation.
3. If the disturbance is determined to be non-transient, control is passed to either the dump routine or to the user intercept option.
4. If the dump routine is selected, when normal power is restored, system storage can be refreshed from the dump device. This storage information is then available to assist the user in recovery and restart procedures.
5. If the user intercept option is selected, the user is able to:
   a. Ride through the power line disturbance if it is of short duration.
   b. Assess the reserve time left in his uninterruptible power system to justify continued processing.
   c. Initiate his system quiesce procedures to terminate operations within the limits of his UPS reserves. Such procedures must be developed by the user.
   d. Transfer to the dump routine which terminates all processing and preserves the contents of storage for subsequent restart procedures.

If the user has a partial uninterruptible power system, during the processing of the power warning interruption, all channels are set to the channel interruption pending state. The channel on which the storage dump is to be performed must process the microcode-initiated channel error interruption. Interruptions are allowed from that channel only. Normal error retry procedures are used. The entire contents of storage are dumped, at which time the uninterruptible power system may be turned off to conserve reserve power. When full utility power is returned to the system, the main storage contents can be restored from the dump device.

Multiprocessing: In a tightly coupled multiprocessing system, the power warning signal is sent to both CPUs. Masking in the individual CPUs determines if the interruption is processed or held pending. In MP mode all shared storage can be dumped by either CPU, depending on which one processes the interruption.

In uniprocessor mode, each CPU must process its own interruption. Only that storage configured to a CPU can be dumped by that CPU. If both CPUs require data retention in the uniprocessor environment, they must *both* have a control unit configured that has uninterruptible power system support.

Physical Planning: Installation of either a partial or full uninterruptible power system requires a significant amount of pre-installation planning. Specialists are required to determine uninterruptible power system specifications, space requirements, cable layout, etc. Users should allow six months to a year lead time prior to the desired installation date.

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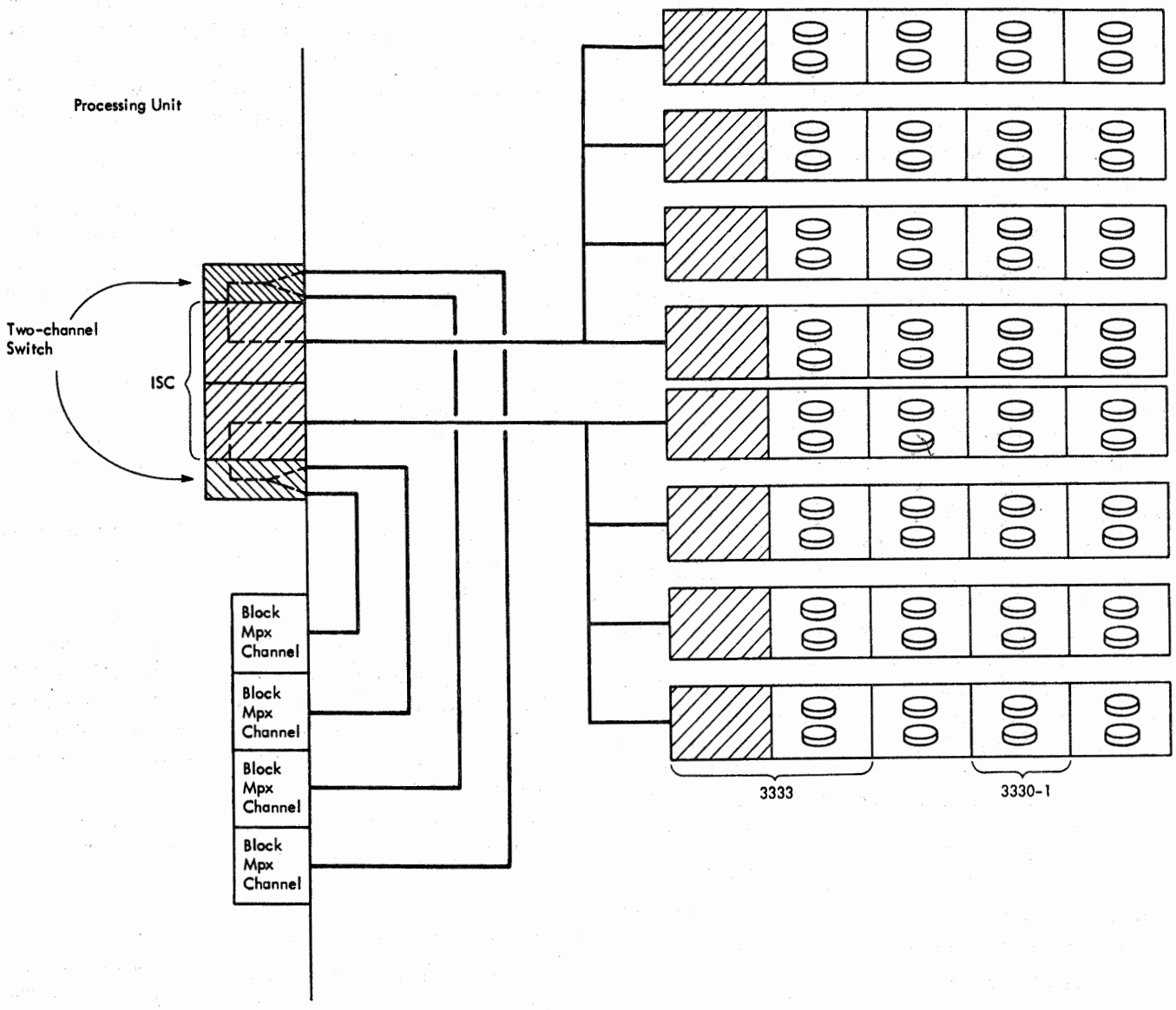

* The second data path from each half of the two-channel switch may be logically connected to a channel on the host CPU or on another CPU.

Figure 20. Integrated Storage Controls and Two-channel Switch Showing Logical Maximum Configuration

Integrated Storage Controls (ISC)

The Model 158 integrated storage controls (ISC) feature provides for the attachment of up to eight IBM 3333 Disk Storage and Control Model 1's. The IBM 3330 Disk Storage Model 1 can be attached to provide a maximum of 64 disk drives, when the 32-drive expansion feature is attached.

The integrated storage controls execute DASD commands; the feature is program compatible with IBM 3830 Storage Control and IBM 3330 Disk Storage in the areas of data format, channel commands, permissible command sequences, and error recovery procedures.

The ISC contains two data and control paths, each of which is capable of attaching up to 32 disk drives (see Figure 20). The two paths are logically independent, with completely overlapped operation, and each can attach to separate block multiplexer channels. There is some commonality for the two data and control paths. One kind of failure may cause both data and control paths to be inoperative.

The ISC is dependent on the 3158 Processing Unit and is clocked on the CPU meter.

Two-channel Switch

A two-channel switch feature is available that provides for attachment to an additional block multiplexer channel (see Figure 20). The paths may be attached to channels on

either the same or different CPUs. Channel switching and device reservation are controlled by the channel program. Two special commands are associated with two-channel switch operation: device reserve and device release. Individual drives attached to the ISC may be reserved for the exclusive use of either of the two channels attached to the given ISC path.

32-Drive Expansion

This feature permits the attachment of two additional 3333 Disk Storage and Control Model 1s and their associated 3330 Disk Storage Model 1 disk drives on each path of the integrated storage controls feature (see Figure 20). This doubles the number of available disk drives on the ISC, making a maximum of 64. A prerequisite for 32-drive expansion is the control store extension feature, which provides additional control storage for microprogram use.

Staging Adapter for ISC

This optional feature for the ISC permits expansion of the addressing capability of each ISC path to a maximum of 64 unique addresses. The adapter allows direct attachment of the IBM 3850 Mass Storage System to a Model 158, and provides the same functions as the IBM 3830 Storage Control Model 3. The expanded capability that the adapter provides is independent of the number of 3330 Disk Storage drives attached to the ISC. Attachment of the staging adapter requires attachment of the ISC control store extension, and precludes attachment of 3340 Disk Storage drives to the ISC.

Facilities

The integrated storage controls provide or support the following standard facilities:

- Command Retry
- Multiple Requesting
- Multiple Track Operation
- Record Overflow
- End-of-File

Command Retry: Command retry is a channel-storage control procedure that causes an improperly executed command in a channel program to be automatically retried. The reexecution does not cause an I/O interruption, and programmed error-recovery procedures are not required.

Multiple Requesting: Use of block multiplexer channels and disk drives with rotational position-sensing capabilities allows the ISC and attached disk drives to disconnect from the channel during mechanical delays resulting from execution of arm-positioning seek sector or set sector commands. Reconnection is attempted when the access mechanism is positioned at the desired track, or when the specified rotational position has been reached.

During the time the channel and the ISC are disconnected, the CPU is free to initiate I/O operations on other drives attached to the ISC even though the disconnected channel program is not completed. Thus, separate channel programs may be operating simultaneously on each drive attached to the storage control.

Multiple Track (MT) Operation: On all search and most read commands, the ISC can automatically select the next sequentially numbered head on a disk drive. This eliminates the need for seek head commands in a chain of read or search commands.

Record Overflow: The record overflow function provides a means of processing logical records that exceed the capacity of a track. When the system is using overflow records, the cylinder boundary is the factor limiting the size of the record.

A special channel command (Write Special Count, Key, and Data) is used to format the disk pack for record overflow operation.

End-of-File: An end-of-file record, used to define the end of a logical group of records, is written by executing a Write Count, Key, and Data command with a data length of zero. Execution of this command causes the ISC to direct the addressed drive to write a data area consisting of one byte of zeros.

When the end-of-file record is processed, detection of the zero data length causes unit exception status to be generated.

Statistical Usage/Error Recording

The ISC maintains a statistical data record of usage and error information for each attached logical device. The usage information provides an accumulated count of the total number of access motions, and the total number of seek errors, correctable data errors, and uncorrectable data errors that were recovered by the ISC retry procedure. Also included in the error information is the total number of command and data overrun conditions that were retried by the ISC.

The usage/error information is sent to the system logout area periodically. The transfer takes place on the next start I/O issued to the device having outstanding usage/error information. Each of the usage/error counters is reset to zero after the counter information is transferred to the channel.

Storage Control Diagnostics

To provide maximum facility availability, the ISC can execute diagnostic tests on a drive concurrently with normal system operation on the remaining disk drives. This mode of operation allows servicing personnel to diagnose

and repair most disk drive failures while the facility continues to operate other attached drives. The ISC provides a transient block of 512 bytes (128 words) of control storage to allow temporary residence for a specific diagnostic test.

The transient area is loaded by the system under control of the online test executive program (OLTEP). A special command (diagnostic write) loads a selected test into control storage and instructs the storage control to execute the test. This loading and execution may also be initiated from the service frame.

After the test, error-message information or test results are transferred from the ISC to main storage by a read diagnostic status 1 command. If the service frame is used, the test results are displayed on the service frame indicators.

Configuration Control

Operator-accessible switches are provided for configuration control of each ISC data and control path (see Figure 21). The ISC can operate with a given channel only when the respective interface switch is set to ON. The multitag switches determine how the device end (generated by the drive in a not-ready-to-ready sequence) is provided to the channel.

When the multitag switch is set to ON, a disk drive is available to a channel after the channel clears the device end generated by the drive on a not-ready-to-ready sequence. Before any other channel can use the disk drive, it must also accept the not-ready-to-ready sequence device end.

When the multitag switch is set to OFF, a disk drive is made available to all channels after one of the channels clears the device end generated by the drive in a not-ready-to-ready sequence.

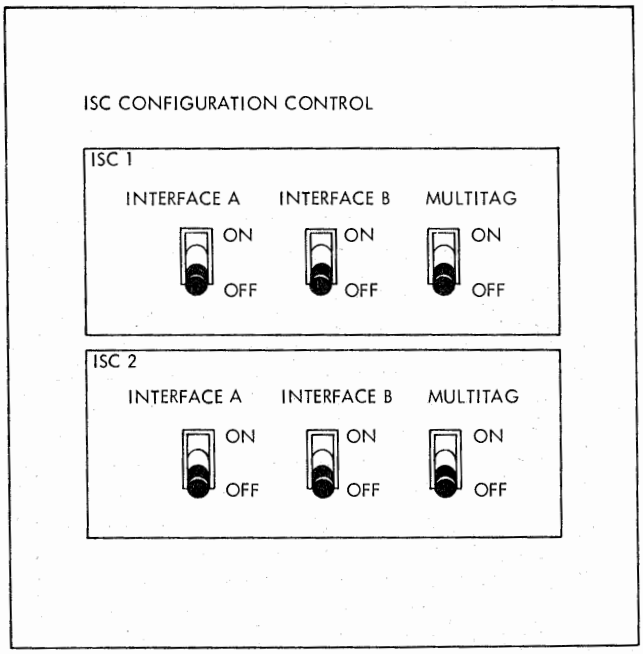

Figure 21. Configuration Control Switches with Two-channel Switch Feature

Input/Output Operations

The following text contains a general description of I/O operations related to the ISC and its attached disk storage units. For detailed information regarding the central processing unit and channel program control of I/O operations, refer to *IBM System/370 Principles of Operation*, GA22-7000.

Unit Selection and Device Addressing: The I/O address of each ISC data and control path and its attached drives is designated by an eight-bit binary number in an I/O instruction. These addresses consist of three parts: (1) The ISC data and control path address (determined by service personnel at installation time) in bits 0, 1, 2, and 3; (2) the address of the 3333 Disk Storage and Control specified in bit 4; and (3) the addresses of the attached 3330s specified in bits 5, 6, and 7. With 32 drives installed on each path, bits 0, 1, and 2 are used to designate the ISC data and control path address. The 3333 Disk Storage and Control address is specified in bits 3 and 4; bits 5, 6, and 7 retain their same function.

The ISC accepts any drive address from 000 to 111. If the specified drive is either offline or not attached, the attempted operation is terminated with unit check status. Multiple responses to an address owing to duplicate logical address plugs or hardware failures also cause the operation to be terminated.

Channel Commands: The command set used to perform operations with the ISC is identical to that used with the 3330 Disk Storage and 3830 Storage Control Model 1.

Refer to *Reference Manual for IBM Integrated Storage Control*, GA26-1620, for a description of commands and sense data.

Appendix A. EBCDIC Interface Code

Bits 4 5 6 7	Hex 1	00				01				10				11				← Bits 0, 1
		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11	← Bits 2, 3
	↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	← Hex 0
0 0 0 0	0					SP	&	-									0	
0 0 0 1	1							/		a	j			A	J		1	
0 0 1 0	2									b	k	s		B	K	S	2	
0 0 1 1	3									c	l	t		C	L	T	3	
0 1 0 0	4									d	m	u		D	M	U	4	
0 1 0 1	5		NL							e	n	v		E	N	V	5	
0 1 1 0	6									f	o	w		F	O	W	6	
0 1 1 1	7									g	p	x		G	P	X	7	
1 0 0 0	8									h	q	y		H	Q	Y	8	
1 0 0 1	9		EM							i	r	z		I	R	Z	9	
1 0 1 0	A					¢	!		:									
1 0 1 1	B					.	$	,	#									
1 1 0 0	C		DUP			<	*	%	@									
1 1 0 1	D					(	)	_	'									
1 1 1 0	E		FM			+	;	>	=									
1 1 1 1	F					|	¬	?	"									

Table 1. I/O Interface Code–EBCDIC

Appendix C. Glossary and Abbreviations

If the term you are seeking does not appear in this glossary, refer to *IBM Data Processing Glossary*, GC20-1699.

Address: An identification of a storage location or an I/O device.

Address Compare: A technique to stop the CPU at a specific address.

Address Modification: The process of changing the address part of a machine instruction via coded instructions.

Address Translation: The process of changing the address of an item of data or an instruction from its virtual address to its real storage address.

Alphameric: Pertaining to a character set that contains letters, digits, and special characters.

Attention Identifier (AID): A character that is set by the console in display mode when the operator presses ENTER or CANCEL, or detects a field with the light pen.

Attribute Character: A character that describes the characteristics of the data field that follows it.

Basic Control (BC) Mode: A mode in which the features of a System/360 computing system and additional System/370 features, such as new machine instructions, are operational on a System/370 computing system.

CCW: Channel command word.

Control Registers: A set of registers used for operating system control of relocation, priority interruption, program event recording, error recovery, and masking operations.

CPU: Central processing unit.

CRT: Cathode-ray tube.

CSW: Channel status word.

CTCA: Channel-to-channel adapter.

Cursor Symbol: A short line (underscore) displayed on the CRT to indicate where the next character entered will be positioned.

DIDOCS: Device independent display operator console support.

DOS/VS: Disk operating system/virtual storage.

Dynamic Address Translation (DAT): (1) The change of a virtual storage address to a real storage address during execution of an instruction. (2) A hardware feature that performs the translation.

EBCDIC: Extended binary-coded decimal interchange code.

EPO: Emergency power off.

Extended Control (EC) Mode: A mode in which all the features of a System/370 computing system, including dynamic address translation, are operational.

Hardstop: Faulty machine condition in which CPU ceases operation.

Hex: Denoted in the hexadecimal (base 16) number system.

HMS: Hierarchical monitoring system.

IAR: Instruction address register.

IMPL: Initial microprogram load.

Initialize: To set counters, switches, address, etc., to zero or other starting values at the beginning of, or at prescribed points in, a computer program.

IPL: Initial program load.

ISC: Integrated storage controls.

k: 1,000.

K: 1,024 bytes of storage capacity.

LCL: Limited channel logout.

Loosely Coupled: Pertaining to processing units that are connected by channel-to-channel adapters that are used to pass control information between the processors.

MCS: Multiple console support.

MP: Multiprocessor *or* the multiprocessor mode of operation.

Multiprocessor: A computer system having two processing units under a single control program.

MVS: Multiple virtual storage.

Offline: Pertaining to resources with which the central processing unit has no direct communication or control.

OLT(S)EP: Online test (standalone) executive program.

Online: Pertaining to resources with which the central processing unit has direct communication or control.

OS/VS: Operating system/virtual storage.

Page: (1) A fixed-length block of instructions, data, or both that can be transferred between real storage and external page storage. (2) To transfer instructions, data, or both between real storage and external page storage.

Page Table: A table that indicates whether a page is in real storage, and correlates virtual addresses with real storage addresses.

PER: Program event recording.

PFK: Program function key.

PSW: Program status word.

PTLB: Purge translation lookaside buffer.

RAS: Reliability and serviceability.

RCS: Reloadable control storage.

Real Address: The address of a location in real storage.

SAR: Storage address register.

SCU: Storage control unit.

Segment: A continuous 64K area of virtual storage, which is allocated to a job or system task.

Segment Table: A table used in dynamic address translation to control user access to virtual storage segments. Each entry indicates the length, location, and availability of a corresponding page table.

Selectable Unit: A collection of macro instructions and modules that provides added program function or hardware support for MVS.

SF: Start field.

Softstop: Stop condition in which CPU clock continues to run.

SVP: Service processor.

Tightly Coupled: Pertaining to processing units that share main storage, are controlled by the same control program, and can communicate with each other.

TOD: Time of day.

UCW: Unit control word.

Uniprocessor: A computer system having a single processing unit.

UP: In an MP system, the uniprocessor mode of operation.

UPS: Uninterruptible power system.

Virtual Address: An address that refers to virtual storage and must, therefore, be translated into a real storage address when it is used.

Wait State: The state of the system when no instructions are being processed, but the system is not fully stopped. The system can accept I/O and external interruptions, and can be put through the IPL procedure.

Word: Predetermined group of bytes whose address is the first byte-address, located in storage by boundary limits; halfword = two bytes, location divisible by 2; fullword = four bytes, location divisible by 4; doubleword = eight bytes, location divisible by 8.

Write: To transfer data from main storage to an I/O device.

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