GA24-3672-4
File No. 4300-01

Systems

# IBM 4341 Processor Model Group 1 Functional Characteristics and Processor Complex Configurator

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**Fifth Edition, November 1981**

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# Preface

This reference publication is for system analysts and programmers who require information about processor features, input/output characteristics, timings, machine instructions, and the functions of integrated I/O devices.

The reader is assumed to have a working knowledge of the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode,* Order No. GA22-7070, and the *IBM System/370 Principles of Operation,* GA22-7000, and to have had programming experience with System/360, System/370, or other 4300 Processors.

The main chapters cover:

- Introduction to the IBM 4341 Processor Model Group 1
- Input/Output Channel Characteristics
- Support Subsystem
- Display Console
- Facilities Descriptions
- Instruction Timings
- IBM 4341 Processor Model Group 1 Complex Configurator

**Prerequisite Publications**

- *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode,* GA22-7070
- *IBM System/370 Principles of Operation,* GA22-7000
- *IBM 4300 Processors Summary and Input/Output & Data Communications Configurator,* GA33-1523.

**Associated Publications**

- *IBM 4341 Processsor Model Group 1 Channel Characteristics,* GA24-3671
- *IBM 4341 Processors Operator's Guide,* GA24-3669
- *IBM 4300 Processors Installation Manual–Physical Planning,* GA24-3667
- *IBM Input/Output Equipment Installation Manual–Physical Planning for System/360, System/370, and 4300 Processors,* GA22-7064
- *IBM 3268 Printer Model 2 Planning and Site Preparation Guide,* GA27-3266
- *IBM 3270 Information Display System Component Description,* GA27-2749
- *Introduction to Programming the IBM 3270,* GC27-6999
- *IBM Disk Pack and Cartridge Handling Procedures,* GA26-5756
- *IBM Diskette–General Information Manual,* GA21-9182
- *IBM 3270 Information Display System Color and Programmed Symbols,* GA33-3056.

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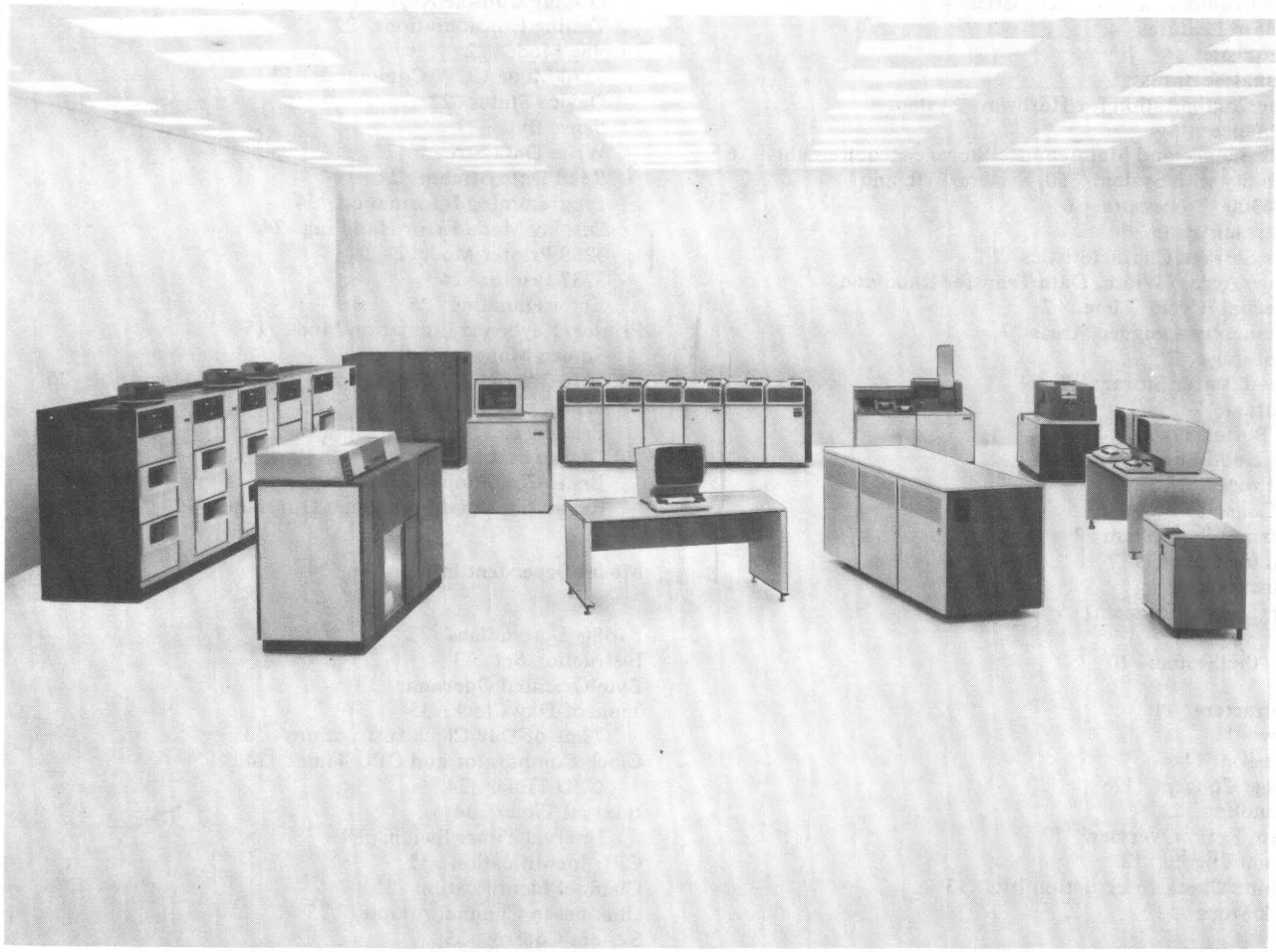


**Figure 1. IBM 4341 Processor with Typical I/O Configuration**

# IBM 4341 Process Model Group 1 Functional Characteristics

This publication is a reference for users of the 4341 Model Group 1; only items that are unique to the 4341 Processor are discussed in detail. Effective use of this manual requires a comprehensive understanding of the information in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode,* GA22-7070, as well as the *IBM System/370 Principles of Operation,* GA22-7000.

The 4341 Processor (Figure 1) is a high-availability data processing system that provides the reliability, performance, and convenience demanded by both business and scientific users. The 4341 Model Group 1 is compatible with other 4300 Processors and is capable of running under current program operating systems.

> **Note:** *Hereinafter, references to 4341 are to 4341 Model Group 1.*

## *Highlights*

The 4341 offers Virtual Storage, System Control Program (SCP) support, and System/370 compatibility, implemented by using Large Scale Integrated technology and large processor storage.

The 4341 Complex consists of the 4341 and the IBM 3278 Model 2A Display Console or the IBM 3279-2C Color Display Console. The processor provides arithmetic, logic and control functions, storage, channels, and system diskette drive.

Other significant 4341 characteristics are:

- Ease of installation, with minimum disturbance of existing input/output configuration.
- DOS/VSE, OS/VS1, OS/VS2-MVS, and VM/370 program support.
- Balanced performance of decimal, commercial, and scientific instructions.
- Processor cycle time of 150 to 300 nanoseconds. The data path to storage is eight bytes wide. A high-speed buffer storage is standard.
- Processor storage of 2 or 4 megabytes. (Some of this storage is required by the system, as described under "System Storage Requirements.")
- Improved reliability, availability, and serviceability (RAS), including instruction retry, error checking and correction (ECC) to provide single-bit error correction and double-bit error detection in processor storage. Error recording by the hardware itself and the Remote Support Facility (RSF) for remote maintenance are also provided.
- Six channels available:
  - Group 1 (standard): One byte-multiplexer channel and two block-multiplexer channels.
  - Group 2 (optional): Three additional block-multiplexer channels. (Channel 4 can be selected as a second byte-multiplexer channel.)

    The channels are capable of overlapped operation from the Instruction Execution function of the 4341.

    The block-multiplexer channels "appear" as selector channels to I/O devices that do not block multiplex.

    An optional Channel-to-Channel Adapter is also available.

- Two modes of operation selectable at Initial Microcode Load (IML) time:
  - Extended Control Program Support VSE (ECPS:VSE) Mode – allows operation of an appropriately generated DOS/VSE for enhanced performance.
  - System/370 Mode – allows operation of any program written for the System/360 or System/370 that does not violate the exceptions noted in the "Compatibility" section below. For those System Control Programs (SCPs) that contain 4341 support, see "Programming Support."

    In this mode, three mutually exclusive performance options are available:

    ECPS:VS1 Assist – provides a hardware assist that reduces the processor time needed to execute certain frequently used supervisor functions in VS1, Release 7 or later. In this mode, other supported SCPs operate but without enhanced performance.

ECPS:VM/370 Assist – reduces the processor time needed to execute certain frequently used supervisor functions in VM/370, Release 6 or later. In this mode, other supported SCPs operate but without enhanced performance.

ECPS:MVS – allows the 4341 processor to operate with compatibility support of the System/370 Extended Facility while running in System/370 mode. This selection provides the System/370 facilities that are a prerequisite for operation in the MVS/SP environment.

- The IBM 3278 Model 2A Display Console or 3279-2C Color Display Console required for interaction with the 4341 for both operation and maintenance. The Operator Console Keyboard with its Operator Control Panel (OCP) is used for turning power on and off, for Initial Microcode Load (IML), and for starting and stopping processor operations.

  Both the Display mode and the Printer- Keyboard Emulation mode are supported. In Display mode, the keyboard is used for input, and the display is used for the output of up to 20 lines of up to 80 characters each.

  In Printer-Keyboard mode, the keyboard is used for input. The display and a recommended 3268 Printer Model 2 or 3287 Printer Model 1, 2, 1C, or 2C are used for output. The display console and the printer appear to the system as a console printer-keyboard. This allows using an operating system that has been generated for a System/360 with a 1052 Printer-Keyboard or a System/370 with a 3210 or 3215 Console Printer-Keyboard. An optional alternate console (with one display-keyboard and one printer) can also be configured.

  The console also provides for *normal* versus *instruction step* processing, for address compare stopping, for altering certain registers and storage areas, and for displaying processor status.

  For maintenance and service support, the console can display and store the status of the 4341 complex and other pertinent servicing information. It also provides a means for using diagnostic tools.

  Up to three optional 3278 Model 2A Display Consoles or 3279-2C Color Display Consoles or 3268 Model 2 or 3287 Model 1 or 2 Printers can be configured (for a total of four). The optional printer has a separate address in display mode and requires Multiple Console Support (MCS).

  **Note:** The procedures for configuring 3268-2 or 3287 Printers depend on the operating system being used. For OS/VS1, for example, the 3287 is supported by specifying either a 3286 or 3210 Printer.

  The 3278-2A and 3279-2C features other than those basic to the primary display console are not supported.

- The Support Processor for automatic analysis of failure symptoms. The result of this "self diagnosis" is a processor-generated *reference code* that contains information to guide the service representative to the failing unit. This reference code is logged on the system diskette, and displayed to alert the operator of possible machine malfunction.

- The System Diskette Drive for both IML of microcode and recording of errors for later diagnosis. The removable diskettes provide all the microcode required for initializing basic processor features (and optional features, when ordered), as well as diagnostics for the service representative.

- The Remote Support Facility (RSF) for use (when installed and authorized by the customer) to enhance hardware maintenance.

- The Remote Operator Console Facility (ROCF) for assisting the operation of a 4341 in a Distributed Data Processing (DDP) environment.

## Channel Configurations

The input/output channel configurations available for the 4341 are:

- Channel Group 1 (standard): One byte-multiplexer channel (1-megabyte/second data rate) and two block-multiplexer channels. In *byte mode,* simultaneous operation of several low-speed devices is permitted. Data transfer can be interleaved.

**Note:** I/O devices that are subject to data overrun (that is, the possibility of data loss), such as magnetic tape units, are not supported in burst mode on the byte-multiplexer channel.

The two block-multiplexer channels permit simultaneous operation of high-speed devices. Block-multiplexer channels are for relatively high-speed burst operations. They can multiplex complete blocks of data, and thereby permit a device to disconnect only after channel end, or after a halt instruction has been executed. This facility allows the interleaved execution of several channel programs by one channel.

The actual data rates depend on the types of devices being serviced and the effect of concurrent processor and channel activity. For channel data rates, see "Input/Output Channel Characteristics."

- Channel Group 2 (optional): This feature provides three additional block-multiplexer channels. Channel 4 can be selected as a byte-multiplexer channel having a 2-megabyte/second data rate. With this option, the configuration includes two byte-multiplexer channels, one 1-Mb block-multiplexer channel, one 2-Mb block-multiplexer channel, and two 3-Mb block-multiplexer channels.

Most input/output devices that can be attached to IBM System/360 and IBM System/370 can be attached to the 4341 processor. See *IBM 4300 Processors Summary and Input/Output & Data Communications Configurator,* GA33-1523.

## Modes of Operation

The 4341 executes all the processing and input/output functions described in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode,* as well as those functions described in the *IBM System/370 Principles of Operation.* The major difference between the mutually exclusive System/370 and ECPS:VSE modes is in the handling of virtual addresses.

- ECPS:VSE mode uses internal address translation for both processor and channel addresses. All storage addresses are virtual addresses.

- System/370 mode uses segment and page tables for processor Dynamic Address Translation (DAT). Channel addresses are real addresses that are translated by the System Control Program (assisted by the Channel Indirect Data Addressing facility).

## Programming Support

Programming support for the 4341 in ECPS:VSE mode is provided by DOS/VSE. In System/370 mode, programming support is provided by DOS/VSE, OS/VS1, OS/VS2-MVS, and VM/370.

Brief descriptions of these program support packages (and references to the publications that describe them in detail) are available from your IBM representative. Additional information about 4341 processing and input/output functions, and Basic Control (BC) and Extended Control (EC) modes, is presented in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* or, for System/370 mode, in the *IBM System/370 Principles of Operation.*

## Remote Support Facility (RSF)

This facility (when installed and with customer authorization) provides the capability of remotely controlling the 4341 from an IBM RETAIN/370 site, and allows the on-site service representative to access the IBM RETAIN data bank for the latest service aids and information.

While in this mode, the IBM Remote Support personnel can perform online diagnosis as though he were at the customer's site. Logout data stored on the system diskette drive can be saved in RETAIN during the Data Link (DL) operation for later offline analysis. Microcode patches may also be applied remotely.

The remote connection is via a customer-supplied Data Access Arrangement (DAA). For connection information, refer to the *IBM 4300 Processors Installation Manual–Physical Planning,* Order No. GA24-3667. Remote console operation from any IBM RETAIN terminal is through the Data Link facility of RETAIN.

The 3278-2A is used to monitor RSF data transmission. The DISC key can be used to terminate data transmission at any time.

In customer installations where the IBM RETAIN facilities cannot be used, remote control is possible via an IBM 3275 Display Station (using a dial-up, 1200-baud, bisynchronous, switched line).

## Remote Operator Console Facility

The Remote Operator Console Facility (optional feature) is an extension of the Remote Support Facility (RSF). When installed and enabled, the Remote Operator Console Facility is active in the support processor when 4341 power is on.

In a distributed data processing environment, Remote Operator Console Facility allows personnel at the host site to dial-up the remote 4341 and control the remote system from the host site. This control is accomplished through such system operation functions as IML/IPL, Reset, Restart, Compare/Trace, and Display/Alter.

To use the Remote Operator Console Facility, the remote 4341 system must be equipped with a customer-supplied auto-answer modem and Data Access Arrangement. For details, refer to the *IBM 4300 Processor Installation Manual–Physical Planning*. Communication with the Remote Operator Console Facility is by an IBM 3275 Display Station, and by programming support (provided by IBM Program Products) designed to allow remote console communication.

In Remote Operator Console Facility mode, the optional Security Keylock feature on the 4341 system console (if installed) allows the host site to control the remote 4341 without interference from unauthorized personnel at the remote site.

Password verification is also part of the Remote Operator Console Facility, and protects against unauthorized access to the remote 4341. If a higher level of data security is required, an external encryption device may be attached to the dial-up link.

After the remote 4341 system is successfully initialized, normal transfer of data and control information between the host and the remote system should be handled through a standard communication network, such as the 270x or 370x Communication Controllers).

## Processor Features and Characteristics

The 4341 features and characteristics listed here are explained in detail in other sections of this manual (or in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* or the *IBM System/370 Principles of Operation).*

### *Standard Features*

Standard features on the 4341 Model Group 1 are:

| *Model* | *Processor Storage (Note 1)* |
|---|---|
| K1 | 2,097,152 bytes |
| L1 | 4,194,304 bytes |

Basic Control (BC) Mode
Byte-Oriented Operands
Channel Group 1 (Note 2): One Byte-Multiplexer Channel
Two Block-Multiplexer Channels
Channel Command Retry
Clock Comparator and Processor Timer
Control Registers
Decimal Instructions
Dynamic Address Translation (in System/370 Mode Only)
Eight-Byte Parallel Data Flow within Processor (as well as eight-byte data path among processor, storage, and channels)
150- to 300-Nanosecond Processor Cycle
Error Checking and Correction (ECC) in Processor Storage
Extended Control (EC) Mode
Extended Control-Program Support (ECPS:VSE) Mode
Extended Precision Floating Point
External Signal
Floating-Point Instructions
High-Speed Buffer Storage
Instruction Retry
Interval Timer
Limited Channel Logout
Machine Check Handling
Move Inverse Instruction
Program-Event Recording (PER)
PSW Key Handling
Reloadable Control Storage
Storage Protection (Store and Fetch)
Store Status (System/370 Mode) or Save (ECPS:VSE Mode)
Subchannels (128 to 1024, Note 2)
Support Processor
System/370 Mode (Note 3) ECPS:VS1 Assist
ECPS:VM/370 Assist
ECPS:MVS
System/370 Universal Instruction Set
System Diskette Drive
Time-of-Day Clock
Virtual Storage

**Notes:**

1. The actual processor storage available for application programs depends on the number of UCWs, and so forth. Refer to "System Storage Requirements."
2. From 128 to 1024 subchannels can be configured. Refer to "Input/Output Channel Characteristics."
3. BC mode and EC mode are submodes of both System/370 mode and ECPS:VSE mode.

### *Prerequisites*

3278 Model 2A Display Console or 3279-2C Color Display Console (both with Operator Control Panel)

## *Optional Features*

Optional features on the 4341 are:

Channel Group 2:
Three Additional Block-Multiplexer Channels
(or One Byte- and Two Block-Multiplexer Channels)
Channel-to-Channel Adapter
Additional Channel Control Unit Positions
Remote Support Facility
Remote Operator Console Facility
3279-2C Color Display Console and 3287-1C
or 2C Color Printer

**Note:** Any combination of three 3278-2A, 3279-2C, 3268-2, and/or 3287 devices is optional on the 4341 (in addition to the 3278-2A or 3279-2C Display Console). These devices are ordered separately.

# Minimum Configuration for Hardware System Maintenance

The following minimum configuration is required for hardware maintenance. The individual System Control Programs (SCPs) have their own minimum requirements depending on the SCP type and release level.

### Minimum Configuration with Demountable Direct Access Storage

- 4341 Processor
- 3278-2A Display Console or 3279-2C Color Display Console
- Access to one of the following groups of devices:
  - 1 Card Image I/O device* and
  - 2 Direct Access devices** and
  - 1 Hard-Copy Output device,

  or:

  - 1 Card Image I/O device* and
  - 1 Direct Access device** and
  - 2 Magnetic Tape devices*** and
  - 1 Hard-Copy Output device,

  or:

  - 1 Card Image I/O device* and
  - 3 Magnetic Tape devices*** and
  - 1 Hard-Copy Output device.

* *Card Image* is defined as:
- Any supported Card Reader, or
- An addressable diskette input/output unit (such as a 3540) and key-to-diskette capability, or
- A magnetic tape drive and provisions for entering card-image formatted records onto magnetic tape, or
- Capability provided by the customer through his operating system facilities to create card-image format on either tape or diskette. The customer must supply an operator to key the card images at the direction of the service representative.

** Must be demountable Direct Access Storage Device (DASD).

*** If 2400 Series, seven-track, magnetic tapes are used, Data Conversion features (No. 3228 and 3236) must be installed on the 2803 or 2804 Tape Control unit.

### Minimum Configuration with Nondemountable Direct Access Storage

For configurations with nonremovable direct access storage devices (DASD), the following devices constitute the minimum configuration for hardware maintenance, provided that the first forty cylinders on a nonremovable drive (other than the System Residence drive) are made available for the generation and maintenance of service programs. This space must be allocated for initial installation, for modifications to the configuration, and for the application of maintenance facility updates.

- IBM 4341 Processor
- IBM 3278-2A Display Console or 3279-2C Color Display Console
- Card Image I/O Device (See * above)
- Nonremovable DASD:
  IBM 3350 – The first 40 cylinders of a drive dedicated when required.
  IBM 3370 – The first 64K blocks dedicated during maintenance.

  **Note:** After use of the 3350 or 3370 by the service representative, this drive may need to be reformatted by the customer for customer use.
- Magnetic Tape Device
- Hard-Copy Output Device

### Additional Requirements for Installation and Operational Maintainability

In all configurations, each processor must use IBM programs (or equivalent) that provide for error recording, with elements for handling machine-check interruptions and for recording status of the processor when a failure is detected. Routines for error recording are contained in some releases of DOS/VSE, OS/VS1, OS/VS2-MVS, and VM/370. The ability of IBM to service configurations that do not meet the above requirements may be impaired with an effect on system availability. Making provisions for the Remote Support Facility (RSF) is recommended to further enhance maintainability and availability.

## System Residence and Maintenance Storage Requirements

Optimum performance and maximum availability are obtained when a disk-storage facility is provided. The DOS, VS1, MVS, and VM/370 operating systems *require* a disk storage facility. These storage requirements are assumed to be attached through a block-multiplexer channel.

### System Storage Requirements

A portion of processor storage is required for dynamic tables. This reduces the amount of processor storage available for user programming. Depending on the processor configuration, the reduction of available processor storage may be from 14K bytes to 108K bytes. The reduction is the sum of the requirements of user selectable options:

- Installed storage size (processor model), plus
- Number of unit control words (UCWs) selected, plus
- Mode of operation, as shown below:

| *Mode of Operation* | *Model K1 (2 Megabytes) Processor Storage Required* | *Model L1 (4 Megabytes) Processor Storage Required* |
|---|---|---|
| ECPS:VSE | 43,008 Bytes | 45,056 Bytes |
| System/370 | 6,144 Bytes | 6,144 Bytes |

| *Number of UCWs* | *Processor Storage Required* |
|---|---|
| 128 | 8,192 Bytes |
| next 32 | +2,048 Bytes |
| next 32 | +2,048 Bytes |
| etc., | etc., |
| up to: | up to: |
| 1024 | 65,536 Bytes |

## Compatibility with System/360, System/370, and other 4300 Processors

An important difference between the System/370 and the 4300 Processors when operated in ECPS:VSE mode is the concept of virtual storage being mapped to real storage under hardware and microcode control. *Real storage* is the amount of storage that is physically installed. The apparent storage (called *virtual storage*) can be any amount of storage that an application requires, up to 16,777,216 bytes.

Any program written for IBM System/370 can operate on the 4341 Processor in System/370 mode, provided that it:

1. Is not time-dependent.
2. Does not depend on system facilities (storage size, I/O equipment, optional features, etc.) being present when the facilities are not included in the configuration.
3. Does not depend on system facilities (such as interruptions, and operation codes) being absent when the facilities are included in the 4341.
4. Does not depend on results or functions that are defined in the *Principles of Operation* to be unpredictable or model-dependent.

Any program written for the 4300 processors in ECPS:VSE mode operates on the 4341 Processor if it follows the above rules.

Any program written for the System/360 can operate on the 4341 if it follows the above rules and does not depend on functions that differ between System/360 and System/370. The System/370 functions that differ from System/360 functions are described in an appendix of the *IBM System/370 Principles of Operation.*

For additional information about compatibility, see *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode,* GA22-7070.

An important aspect of compatibility is the disk data format. With System/360 and System/370, the Count-Key-Data (CKD) architecture is used. The 4341 supports disk units with both the CKD format and Fixed-Block Architecture (FBA) formats. Existing disk volumes can be mapped onto system disk devices.

## Data Representation

The 4341 is both character- and word-oriented. The basic addressable unit is an eight-bit byte (a character, two decimal digits, or eight bits). This provides for efficient use of storage and for high effective input/output rates for decimal data, variable field lengths, broad and flexible code conversion, decimal arithmetic, 32-bit words and 16-bit halfwords for fixed-point arithmetic, 32-bit words and 64-bit doublewords for floating-point arithmetic, and for instructions for such functions as translate and edit.

## Processor Storage Characteristics

The 4341 is available in two processor storage sizes:

Model K1: 2,097,152 bytes (2 megabytes)
Model L1: 4,194,304 bytes (4 megabytes)

Virtual storage capability is provided to increase the effective use of processor storage.

**Note:** The contents of this storage is not saved when power is removed.

### *Storage Access Width, Data Transfer Rate, and Internal Cycle Time*

The storage access width is eight bytes. The high-speed buffer storage cycle time for reading or writing of data already in the buffer is 0.225 microseconds.

Detailed timings of the 4341 instruction set are given in "Instruction Timing Information."

### *Permanently Assigned Areas*

All byte locations of processor storage are available for programming functions except the permanently assigned processor storage areas (storage locations 0 through 511, as described in the *IBM System/370 Principles of Operation* and the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode*).

## Control Storage

Reloadable control storage, not available to the user, accommodates the microcode for controlling all standard and installed optional features.

## High-Speed Buffer Storage

The high-speed buffer storage functions as a smaller and faster subset of processor storage to improve performance. This 8K-byte buffer is not part of user-addressable storage.

## Local Storage

This 1K-byte area contains the general registers, floating-point registers, channel unit control word (UCW) directory, etc.

## Channel Buffer Storage

A data buffer of 256 bytes per channel facilitates data transfer operations between processor storage and the channel I/O interfaces.

## Arithmetic and Logic Unit (ALU)

The ALU has an access width of eight bytes and provides for binary and decimal addition and subtraction operations, as well as for logical AND, OR, and EXCLUSIVE OR operations.

## Support Processor

The support processor (SP) controls processor initialization (initial microcode loading), instruction retry, error analysis and logging, and supports the display console and related equipment.

## Display Console

The IBM 3278 Model 2A Display Console or 3279-2C Color Display Console serves as the online input/output device for operator-system communications. The display console is used to enter or display programming-system control parameters, responses to system messages, and for the display or alteration of application data, general and floating-point registers, etc.

### *Operating the System*

The 4341 is operated, monitored, and controlled from the display console. For detailed information about the basic display console, optional display consoles and printer configurations, and system operation, refer to "Display Console."

### *Operator Controls*

The operator is made aware of processor status via the displays described below and can invoke the described functions from the keyboard.

Normally, the display/keyboard communicates with an application program. Twenty lines of the screen are reserved for this purpose. The bottom lines on the screen are reserved to show processor status (operating, wait, manual, test, and load, and the address and data fields) and the setting of the rate control, check control, and address compare controls.

The functions that can be invoked by pressing a function key are:

- Start
- Stop
- Mode Selection
- Change Display
- Copy
- Page
- External Interruption
- Cursor Controls (left, right, insert, delete, erase EOF, erase IPT)
- Request (PA1)
- Cancel (PA2)

When the Mode or Change Display keys are pressed, the operator is able to set controls or invoke functions via the keyboard, either with or without menu prompting, as follows:

- Alter/Display
- Address Compare
- Interval Timer Enable/Disable
- Check Control
- Program Load
- Operation Rate
- Restart
- System Reset (Program or Clear)
- Store Status (in System/370 mode) or Save (in ECPS:VSE mode)
- Time-of-Day Clock Enable-Set

**System and Control Status**

The indicator fields displayed are:

***Operating Indicator*** is on when the processor is not in stopped state.

***Wait Indicator*** is displayed when the processor is in wait state.

***Manual Indicator*** is on when the processor is in the stopped state.

***Test Indicator*** is on when a control is not in its normal state or when a maintenance function is being performed.

***Load Indicator*** is on during program load. It goes off when the new PSW is successfully loaded.

***Save Indicator*** is turned on upon successful completion of Machine Save (in ECPS:VSE mode) or Store Status (in System/370 mode).

***Addressing Indicator*** displays the address of the next instruction to be executed.

*V-ADDR* indicates that the machine is in System/370 mode and that it is operating with virtual addresses.

*R-ADDR* indicates that the machine is in System/370 mode and that it is operating with real addresses.

*ADDR* indicates that the machine is in ECPS:VSE mode and that it is operating with virtual addresses.

Depending on the dynamic address translation (DAT) setting, either 'V' or 'R' can appear in System/370 mode.

***Data Indicator*** displays the contents of the next address to be executed when the machine is in stopped state. While the machine is operating the display is blank.

***Timer Indicator*** is displayed in both System/370 mode and ECPS:VSE mode and shows the setting of the Interval Timer control.

***Rate Indicator*** is displayed when the Rate control is set to Instruction Step.

***Check Control Indicator*** is displayed when the Check Control control is set to Stop After Log-Switch, Channel Log, Hardstop, No Retry, or Disable.

***Address Compare Indicator:***
*Control* is displayed when the Address Compare control is set to Stop, Trace Stop, or Trace Wrap.

*Type* displays the setting of the way in which an address compare is made: any reference, a data store reference, an I/O reference, or a reference to fetch an instruction.

*Addr/data* displays the address for the compare or the data contents of that address if Address Compare is on Data.

***Check Stop Indicator*** is on when the machine is in check-stopped state after an error.

**Manual Controls**

***System Reset:***
*Program* clears all equipment check indications and sets the processor to such a state that operation may be resumed. An I/O reset is also performed.

*Clear* issues Program Reset and clears processor storage, the general purpose registers, control registers, and the floating-point registers.

> **Note:** These functions can be automatic if selected from the program load screen.

***Start key*** causes the processor to enter the operating state.

***Stop key*** causes the processor to enter the stopped state when the current processing step is completed and any pending interruptions are handled.

***Address Compare:*** The processor enters the stopped state, or traces when an address set by the address compare function matches an address used in a storage reference. An address compare stop/trace can occur on any reference, a data store reference, an I/O reference, or a reference to fetch an instruction.

***Data Compare:*** The processor enters the stopped state, or traces when data established by the data compare function for an address matches data in a storage reference at that address. A stop can occur on any reference, a data store reference, an I/O reference, or a reference to fetch an instruction.

***Interval Timer:*** When the interval timer is activated, processor storage location 80 is decremented every 1/300 of a second. When the location goes negative, an interruption is generated. If Interval Timer is off, location 80 is available for other uses.

***Check Control:***
*Normal*: On an error, the processor may perform retry. If successful, system recovery is reported. If unsuccessful, instruction processing damage or system damage is reported.

*Hardstop*: No machine-check handling is permitted, and no reference code is generated.

*No Retry*: Retry is disabled.

*Disable*: On a CPU or channel error, the processor ignores the error and attempts to continue processing.

*Stop After Log - Switch*: On a CPU or channel error, the processor performs a logout and check-stops, or performs a retry operation and, if unsuccessful, performs a logout and enters the check-stop state.

***Program Load:*** After an Initial Program reset or a Clear reset (a user choice), the processor loads 24 bytes from the load unit addressed, continues until the Initial Program Load (IPL) chaining sequence is complete, and starts the processor under control of the new PSW.

***Operation Rate:***
*Normal* operates the machine at normal speed when start control is activated.

*Instruction Step* performs one unit of execution, takes all pending allowed interruptions, and returns to the stopped state.

***Restart*** stores the old PSW at location 8, fetches the new PSW from location 0, and enters the operating state.

***Interrupt Key*** raises an interruption to the processor. The pending request is cleared when it causes an interruption or by a program reset.

***Time-of-Day Enable/Disable*** allows the operator to change the status of the machine to allow, or disallow, Set Clock instructions (TOD Clock Enabled).

The delay from the time that the control is activated to the time the clock is enabled is about 25 ms. TOD secure selection delay is normally 3 seconds.

## Basic Functions

### *Alter/Display (System)*

Several facilities can be displayed, some of which can be altered. Any of the selections described below cause the processor to enter the manual state. A return to the operating state is required for processor operations to continue.

**Display**

Registers, processor storage, and certain other facilities can be displayed.

These facilities can be displayed in two ways. One way is to go through the mode selection frame to the alter/display frame and then use the menu to fill in the required information. The other way is to use "fast-selection," that is, by keying in a command indicating the function desired, including any required information, such as storage address.

**Alter**

Registers, current PSW, and processor storage can be altered in two ways: menu selection or fast-selection (see "Display" above).

During menu selection, the facility is displayed as it exists in the processor. The operator can then change part or all of it by moving the cursor to the characters to be changed and entering the new data. After the change is entered, the display console shows the change.

For fast-selection, data is entered with the command line. The facility is only displayed after the change.

**Facilities**

The facilities displayed are:

G General Registers
C Control Registers
F Floating-Point Registers
P Current PSW
K Storage Key (in System/370 mode), or Block Description (in ECPS:VSE mode)
V Processor Storage-Virtual
M Processor Storage-Real (available only in System/370 mode)
T Trace Area

***General Registers, Control Registers, and Floating-Point Registers*** can be both displayed and altered. For an alter operation, if the new data is included in the command, any byte of a register can be addressed. Several registers can be altered at a time. When the cursor is used, any hexadecimal digit can be changed.

***Current PSW*** can be both displayed and altered. When displayed, the entire PSW is shown in hexadecimal. Certain fields in the PSW are also formatted.

***Storage Key*** can be both displayed and altered. When altered, the entire key must be entered.

The display is in the same format that is required for the input. Certain fields in the Storage Key are also formatted.

***Processor Storage-Virtual*** can be displayed or altered. A page ability is included. If the Dynamic Address Translation (DAT) bit is off (System/370 mode), the message ADDRESS NOT AVAILABLE is issued.

***Processor Storage-Real/Machine*** functions like Processor Storage-Virtual.

***Trace Area*** displays the addresses in the trace area.

**Page**

The page function displays processor storage. The appropriate display routine fills in the next required address to the previous command. The two page keys allow for either page forward or backward. These keys can be used any time a facility, such as processor storage, cannot be fully displayed on one screen.

### *Mode*

These keys and controls are described in more detail in "Display Console."

**Mode Sel Key**

When the MODE SEL key is pressed, the general selection frame shows on the screen and the operator can select an additional frame.

**Chg Dply Key**

The CHG DPLY key changes the screen between display mode and manual control mode.

**Copy Key**

The Copy key is only operational when in manual control mode and a 3268-2 or 3287 Printer installed. Pressing the Copy key causes the screen image to be printed on the printer that is attached to the adapter. This can be used to save displays, etc.

## Checking the System

The 4341 can be checked by using the System Test programs that are available from IBM on magnetic tape or external disk storage. These programs test and report the condition of the processor and I/O devices made available.

# System Structure

This section describes the major 4341 components to provide an overview of machine and program interrelationships.

## Data Flow

In Figure 2, the simplified data flow of the processor describes the 4341 operation. Microinstructions from the system diskette drive are loaded into control storage during the initial microcode load (IML) procedure. The microcode controls data transfer operations to or from both processor storage and control storage. Work storage is used as a source or destination for this data. During I/O operations, data is transferred between storage and the I/O interface via the channel data buffer. The dotted lines represent optional features.

For an understanding of logical and physical channel relationships, refer to "Input/Output Channel Characteristics."

## *Processor*

The processor contains processor storage, control storage, the system control panel, and other facilities necessary to perform arithmetic functions and logical processing of data. The processor also contains the input/output channel circuitry for control of data transfers between the processor and I/O devices.

The manner in which the various data-flow elements interact depends on the microcode loaded into control storage. The processor executes the instructions defined in *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* and the *IBM System/370 Principles of Operation,* including input/output instructions and commands.

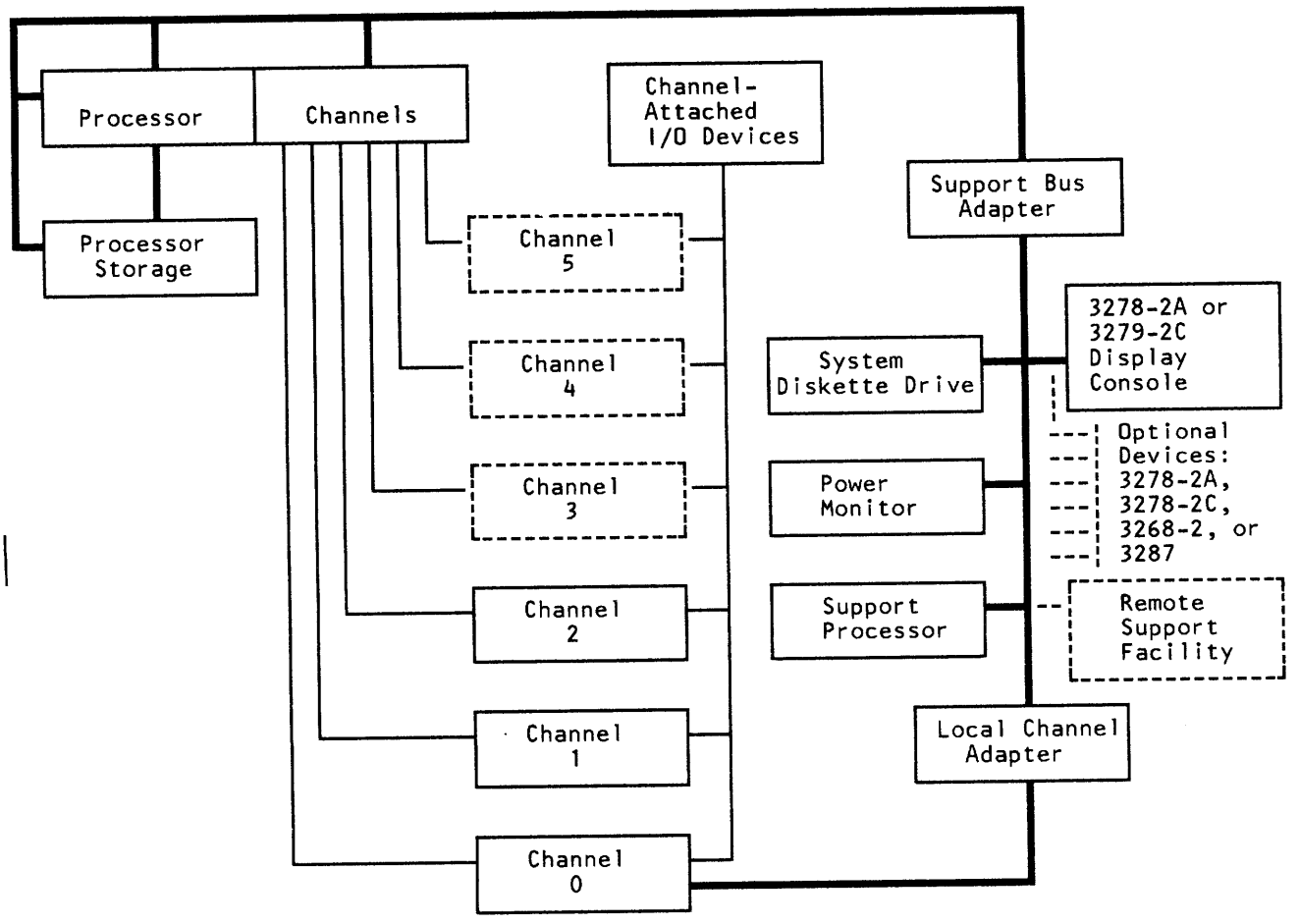



**Figure 2. Simplified 4341 Data Flow**

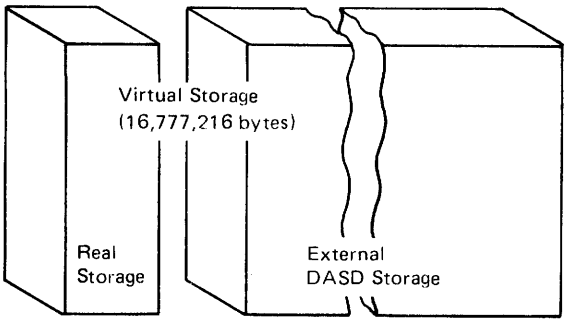



**Figure 3. Storage Concept**

### *Storage Concept*

The storage concept (Figure 3) consists of real storage (up to 4 megabytes) and virtual storage (16 megabytes).

## Error Handling

The error handling function provides both automatic recovery from many hardware malfunctions and reporting by a machine-check interruption to assist in program damage assessment and recovery.

### *System Retry Overview*

The Retry function makes intermittent, processor detected, hardware failures logically transparent to processing. Retry is, in general, done on a machine instruction basis. The data in certain machine facilities is saved during instruction execution. To perform retry when a malfunction occurs, this data is restored in those machine facilities, and the instruction is reexecuted.

Because operand addressability is not verified by pretesting, the retry mechanism can also be invoked when an operand crosses a storage page boundary and an access exception occurs. This has the effect of logically backing up the processor to the state preceding the instruction so that a program interruption can be taken as if the instruction had been nullified.

No retry is performed on malfunctions affecting channel operations (these result in channel control checks).

For both retriable and unretriable errors, the support processor performs an internal logout of hardware latches for analysis. Several logouts are retained on the system diskette.

#### Machine Check Handling

The 4341 error recovery facilities and machine-check interruption procedures comply with the general definitions in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* and the *IBM System/370 Principles of Operation.*

The error handling function can perform any of the following:

1. Re-execute an instruction or interruption that failed because of an intermittent hardware malfunction
2. Post a machine-check interruption for uncorrectable malfunctions and alert conditions
3. Enter check-stop state when a malfunction makes it undesirable or impossible to continue operation.

If application-program errors occur, the operating system attempts to handle the exception and to provide any necessary operator messages. Refer to the applicable programming publications for the operating system you use.

If a failure occurs within the processor or an I/O unit, provisions have been made to retry the failing operation. Facilities are incorporated to record any such failures. (This is in addition to any provisions made by the operating system for error retry and error logging.)

Instruction retry, limited channel logout, storage validation (error checking and correction–ECC) for processor storage, and other error-detection and error-handling provisions are standard.

#### Error Checking and Correction (ECC)

Error checking and correction on processor storage provides automatic, single-bit error detection and correction. ECC also detects all double-bit errors and most multiple-bit storage errors but does not correct them. Parity checking is used to verify other data that is not contained in processor storage.

### Channel Command Retry

Channel command retry is a control-unit initiated procedure between the channel and the control unit. (Not all control units have this capability.) No I/O interruption is required. The number of retries is device-dependent.

## *Internal Logout*

Each machine check normally leads to an internal logout. Because the data flow area and microcode are used for the control of channels and integrated adapters as well as for processor control, the logout buffer contents can relate to either a machine-check condition or a channel-control check. Thus, the interruption may relate to either a processor error or a channel error.

For a hardware error other than corrected single-bit errors, the processor generates an internal logout as a preliminary action to error analysis.

## *Machine Check Interruption Bits*

The machine-check interruption code (MCIC) bits are described in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* and the *IBM System/370 Principles of Operation.*

## *Check Stops*

The processor enters the check-stop condition if any one of the following situations occurs:

- Invalid microcode is executed.
- Certain severe hardware failures.
- A storage error in the system storage (aux) area which cannot be corrected.
- A malfunction occurs during IML/IPL.
- PSW bit 13 is set to 1, and an error occurs during a machine-check interruption that is attempting to report system damage or instruction processing damage.
- PSW bit 13 is set to 0, and an error occurs that causes the system damage bit or the instruction processing damage bit to be set to 1 in the MCIC buffer.
- An error occurs, a successful retry was not performed, and the Stop After Log switch is active.

# System Operation

Operation is initiated when the operator presses the Power On key. After the power-on sequence is completed, the microcode is loaded (under operator control) from the system diskette drive into the control storage of the processor. Normally the operating system is then loaded from the system disk by a program-load command from the display console. The customer's application programs are read into processor storage from an appropriate input device.

Program execution follows the normal System/370 pattern. The processor executes the machine instructions in sequence under control of the current PSW and the mask bits in the control registers. The normal sequential execution of instructions can be changed by branching.

During ECPS:VSE mode operation, processor storage is always addressed by designating one of 16-megabyte locations. Locations that are "addressable" according to the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* are automatically mapped to their corresponding physical storage locations.

Interruptions of six different classes (machine check, supervisor call, program, external, input/output, and restart) can occur during operation. An interruption involves storing the current PSW as the old PSW, storing a code identifying the cause of the interruption, and fetching a new PSW. Processing is resumed according to the new PSW.

## Support Processor

The support processor (SP) maximizes the total system availability and provides for rapid isolation and repair of failures, whenever possible, by automating and simplifying failure diagnosis.

The support processor provides the services necessary for initialization, monitoring, and maintenance. Integrated adapters and a logic element communicate with console I/O devices and other elements of the processor to provide for microcode loading, messenger, and routine checking facilities. The system diskette drive is used for loading microcode that controls processor and channel operations, and for residence areas for error log and analysis data.

The support processor is connected to the 4341 through the local channel adapter (LCA) and the support bus adapter (SBA).

The common communications adapter (CCA) and the remote support facility (RSF) included in the support processor are used by IBM personnel for maintenance.

## System Diskette Drive

The system diskette drive is the initial microcode load (IML) device and provides, by means of removable diskettes, the microcode for initialization, system operations, diagnostics, and so forth. Data loaded into control storage is not accessible to the programmer.

### *Diskette Wear*

Diskettes provide for ease of media handling and storage, etc. Note, however, that during recording and reading, the read/write head is in contact with the media causing wear over time. Care in storage, use, and handling can also affect diskette life. (See guidelines in *IBM Diskette–General Information Manual,* GA21-9182.)

### *Initial Microcode Loading (IML)*

Initial microcode loading is executed in two phases: the support processor, and the main processor. When the appropriate controls on the console are activated, disk reading starts, and the load routine transfers microcode from the system diskette drive into the support processor. Then, optionally, the main processor microcode is loaded into control storage. When loading is completed, the system-reset microcode is executed. After system reset, the processor stops until an external action is taken, such as initial program load (IPL).

# Input/Output Channel Characteristics

The 4341 I/O channels, with a few variations, are like those of System/370. When in ECPS:VSE mode, *virtual addressing* is used. When in System/370 mode, *channel indirect data addressing* can be used. The description of I/O channels that follows describes System/370 mode. For additional information about channel operations, refer to the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* and the *IBM System/370 Principles of Operation.*

For information about I/O devices attaching to the 4341 Processor interface, refer to the *IBM 4300 Processors Summary and Input/Output & Data Communications configurator.*

This section covers the basic characteristics and defines the limitations of the I/O channels.

The following channel configurations are available:

- One byte-multiplexer channel, logical address 0.

  The support processor is internally attached to this channel. The 3278-2A or 3279-2C (and any optional 3268-2 or 3287 printers or additional 3278-2A or 3279-2C devices) are internally connected to the support processor, and are addressed via channel 0.

  Addresses 0F0 through 0FF are reserved for natively attached I/O devices and the support processor, and are not available for I/O devices attached to channel 0.

- Two standard block-multiplexer channels, logical addresses 1 and 2.
- Optionally, three block-multiplexer channels, logical addresses 3, 4, and 5. (Service personnel can connect Channel 4 as a byte-multiplexer channel, if so selected.)

The standard channel configuration is:

Channel 0 - Byte Multiplexer
Channel 1 - Block Multiplexer
Channel 2 - Block Multiplexer

When the additional channels are installed, the channel configuration is:

Channel 0 - Byte Multiplexer
Channel 1 - Block Multiplexer
Channel 2 - Block Multiplexer
Channel 3 - Block Multiplexer
Channel 4 - Block (or Byte) Multiplexer
Channel 5 - Block Multiplexer

The byte-multiplexer channels can operate in either byte mode or burst mode. This is determined by the characteristics of the device operating on the channel. When a device forces burst mode, no other device can operate with that channel until the burst-mode operation is completed.

In byte mode, the single data path of the byte-multiplexer channel can be shared by several low-speed I/O devices operating simultaneously. The channel multiplexes data to or from these devices (one device at a time) in groups of bytes as required by the I/O device being serviced.

The block-multiplexer channel is optimized for relatively high-speed burst operations and can multiplex complete blocks of data. This channel is particularly suited to buffered or cyclic devices with high data rates (such as disk-storage devices). The multiplexing facility of the block-multiplexer channel allows the interleaved execution of several channel programs by the same channel.

> **Note:** The block-multiplexer channels "appear" as selector channels to I/O devices that do not block multiplex.

Block-multiplexing control (defined in *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* and the *IBM System/370 Principles of Operation)* allows operation of the block-multiplexer channel as a selector channel.

The byte-multiplexer and block-multiplexer channels operate from the same I/O instruction and command formats used for System/370.

## Standard Input/Output Interface

The standard System/370 I/O interface is used to connect the channels to I/O devices or control units.

### High-Speed Transfer

This facility enables data transfer to take place (on block-multiplexer channels) faster than the data rates that can be obtained with service-in and service-out alone. Because of the higher-speed

data transfer, this facility can also be used to permit locating a control unit at a greater distance from the channel than would otherwise be possible. This facility includes two additional tag lines: data-in and data-out.

Data-in can be alternated with service-in tag line to enable transfer of data at a higher rate than is possible if service-in alone is used. In this case, data-out is alternated with service-out as the response to data-in. Data-out is the response to data-in as service-out is the response to service-in.

### I/O Error Alert

An additional selection (formerly tag) line, called *disconnect-in* provides (on block-multiplexer and byte-multiplexer channels) control units with the ability to alert the processor of a malfunction that prevents the control unit from signaling correctly over the I/O interface.

Disconnect-in can be activated by a control unit only when it is connected to the channel (has operational-in up). The channel performs a selective reset in response to disconnect-in and indicates to the operating system the occurrence of disconnect-in by causing an I/O interruption and posting an interface control check in the channel status word (CSW).

### Channel Command Retry

Command retry is a combined channel-control unit procedure that can cause a command to be retried without requiring an I/O interruption.

Based on such factors as whether operator intervention or program reorientation is required before retry, the control unit determines if the last command can be retried.

Command retry applies only to block-multiplexer channels and requires an additional interface line called *mark 0-in.*

## Channel Data Rates

Each channel operates on a time sharing basis. Each channel is assigned a certain time slot to minimize the impact on each channel's throughput relative to other channel loading. Each channel's data rate is not affected by the other channels.

Channel configurations and maximum data rates are shown in Figure 4.

**Basic Channel Set (3 Channels)**

| *Channel* | *Data Rate* |
|---|---|
| Byte-Multiplexer Channel 0* | (See Table Below) |
| Block-Multiplexer Channel 1 | 3 Megabytes/Second |
| Block-Multiplexer Channel 2 | 3 Megabytes/Second |

**Full Channel Set (6 Channels)**

| *Channel* | *Data Rate* |
|---|---|
| Byte-Multiplexer Channel 0* | (See Table Below) |
| Block-Multiplexer Channel 1 | 3 Megabytes/Second |
| Block-Multiplexer Channel 2 | 3 Megabytes/Second |
| Block-Multiplexer Channel 3 | 2 Megabytes/Second |
| Block-Multiplexer Channel 4 | 2 Megabytes/Second |
| (or Byte-Multiplexer Channel 4) | (See Table Below) |
| Block-Multiplexer Channel 5 | 1 Megabyte/Second |

* These devices attached natively to the Support Processor are addressed from the IPU through addresses on the byte-multiplexer channel 0.

**Note:** The aggregate data rate for two block-multiplexer channels operating concurrently is up to 6 megabytes per second. When five block-multiplexer channels are operating concurrently, the aggregate data rate is up to 11 megabytes per second.

**Byte-Mode Operation (Channels 0 and 4)**

These data rates are with no other channel activity. For data rates with other channel activity, see *4341 Processor Channel Characteristics.*

| *Byte-Mode Type* | *Byte Channel 0 Data Rate* | *Byte Channel 4 Data Rate* |
|---|---|---|
| Single-Byte Transfer | 16 kb/Second | 22 kb/Second |
| Four-Byte Transfer | 64 kb/Second | 88 kb/Second |

| **Burst-Mode Operation** | **(Channel 0)** | **(Channel 4)** |
|---|---|---|
| *Device Type* | *Channel Data Rate* | |
| Buffered Input: | 1000 kb/Second | 2000 kb/Second |
| Output: | Average kb/Second = (1000 x device rate in kb) divided by (1000 + device rate in kb) | |

For device rates equal to or less than 1000 kb.

**Note:** These data rates assume small interface-cable and control-unit generated delays.

**Figure 4. Channel Configurations and Data Rates**

## Input/Output Interruptions

The 4341 input/output interruptions are described in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode,* GA22-7070.

## Byte-Multiplexer Channel(s)

For byte-multiplexer channel operations, the status, data, or control communication with a device is coordinated by the standard-interface signal sequences between the device and the byte-multiplexer channel.

Every device attached to the byte-multiplexer channel must have a unit control word (UCW) assigned to it. When a byte-multiplexer channel operation requires using the information in a UCW, that UCW is read from system (auxiliary) storage into channel local storage. The operation specified by the UCW is then performed, and the UCW is updated and returned to auxiliary storage when the operation is completed. The UCW carries a dynamic record of the operation for the I/O device assigned.

> **Note:** I/O devices, such as magnetic tape units, that operate in burst mode and are subject to data overrun (that is, the possibility of data loss) are not supported on the byte-multiplexer channel.

## Block-Multiplexer Channels

Up to five block-multiplexer channels (two standard plus up to three optional) are available on the 4341. The block-multiplexing capability allows concurrent operation of many I/O devices on the channel's single data path.

Although only one device may actually be transmitting data at any given instant, multiple channel programs can be concurrently active.

Block multiplexing involves temporarily disconnecting an operation in a sequence of chained channel commands. This frees the channel during nondata transfer activity of the device, and allows other devices access to the channel during this time.

The multiplexing facility of the block-multiplexer channel allows interleaved execution of several channel programs by the same channel.

I/O equipment with high data rates is normally attached to block-multiplexer channels. Non-multiplexing devices attached to these channels operate in selector-channel mode.

## Subchannels and UCWs

A maximum of 256 I/O unit addresses is available on each channel. An exception is channel 0 which can have a maximum of 240 I/O unit addresses because addresses 0F0-0FF are reserved. However, the maximum number of UCWs is 1,024, which are assigned to I/O devices as required. Each control unit or device requires a subchannel (UCW). With a shared control unit, several different I/O devices may share one UCW. Examples are:

1. A single control unit that controls one I/O unit. For example, the 1443 Printer Model N1 requires one subchannel (UCW).
2. A single unit that contains several control units. For example, the 2821 Control Unit that handles functions for each attached 1403 Printer, the 2540 Reader section, and for the 2540 Punch section, requires three subchannels (UCWs).
3. A single control unit that services the requirements of several devices at once. For example, the 3830 Storage Control (used with 3330 Disk Storage devices) requires a subchannel for each device.
4. A single control unit that services the requirements of several I/O units (one at a time). For example, each 3272 Control Unit requires an exclusive UCW, but all 3277 Displays serviced by that control unit share the UCW assigned to the 3272.

### *UCW Pool*

From 128 to 1,024 subchannels (UCWs) can be configured. If more than 128 UCWs are required, additional groups of 32 UCWs are allocated, up to the maximum of 1,024.

Each of the minimum allocation of 128 UCWs occupies 64 bytes of user storage (for a total of 8,192 bytes). Additional UCWs (in groups of 32, up to a maximum of 1,024) can be assigned by trained service personnel.

Each group of 32 additional UCWs reduces the usable processor storage by 2,048 bytes. For example, 128 UCWs require 8K of storage, and

1,024 UCWs require 64K of storage. For each increase in the number of UCWs, the additional UCW storage requirement limits the high address boundary.

Sixteen UCWs (000 through 00F) are reserved for natively attached I/O and for internal functions.

The UCW contains all control information necessary for a channel to perform I/O operations to an attached device.

Each channel has a UCW through which all unassigned I/O devices can present asynchronous interruptions.

Each device attached to a channel must have a UCW associated with its address.

### *Channel UCW Directory*

Each channel has a channel directory. Each directory has 256 entries, one for each possible device address (00-FF) on the channel.

Each directory entry contains the reference number of its associated UCW.

### *UCW Assignment*

UCWs for natively attached I/O devices (such as the 3278-2A) are preassigned. The logical addresses for these devices are assigned by the user. All other I/O devices must be described to the processor by the service representative at the user's request. This information is kept in the UCW directory tables for automatic assignment of UCWs by the processor.

All UCW assignments are written onto the system diskette and become effective after subsequent IMLs. Note, however, that UCWs reassignments for natively attached equipment become effective immediately (without a re-IML).

### *Device Considerations*

Devices that share a control unit and operate in selector mode can use one common shared UCW on the channel. The SEL mode bit must be on in the directory entry.

Devices capable of running in block-multiplexer mode may use an *unshared* UCW for each actual device attached, or one *shared* UCW for all devices attached to the control unit. Normally, UCWs for the block-multiplexer channel are unshared, with SEL mode off.

Devices, such as the IBM 3272 Control Unit, require one exclusive UCW for each control unit on the channel. Each 3277 attached to that control unit then shares that control unit's UCW. The shared bit must be on in the directory entry for that UCW.

Magnetic tape devices use a shared UCW and operate in selector mode.

Channel-to-channel adapters are treated as control units, and require one UCW for each interface attached to the processor.

## Channel Operation

Initial selection, interruptions, and channel status are controlled by microcode and hardware circuits. When the channel operation is set up, hardware controls the data transfer. Each channel has 256 bytes of channel data buffer. Depending on the data length and address boundary, hardware controls the transfer of data to processor storage:

- in 64-byte blocks
- in a partial block to line up to a 64-byte address boundary
- in a partial block to complete a data transfer
- in a partial block for short records
- in a partial block for byte-multiplexer operation.

# Display Console

The IBM 3278 Model 2A Display Console or the IBM 3279-2C Color Display Console is the principal device provided for the operator to communicate with the system. The operator can use the keyboard and the display console to control system operation and to display system status. The display consoles and printers are attached to the 4341 via the support processor.

The minimum 4341 configuration requires one 3278-2A Display Console or 3729-2C Color Display Console.

Depending on the mode of operations, three additional devices may be attached to the support processor ports:

| *Port* | *Devices* |
|---|---|
| 0 | 3278-2A or 3279-2C |
| 1 | 3278-2A or 3279-2C or 3268-2 or 3287 |
| 2 | 3278-2A or 3279-2C or 3268-2 or 3287 |
| 3 | 3278-2A or 3279-2C or 3268-2 or 3287 |

Two operating modes are described in this section: Display mode and Printer/Keyboard Emulation mode.

## *Display Consoles*

The display console can be a 3278 Model 2A Display Console or a 3279 Model 2C color Display console with their keyboard. Both uppercase and lowercase characters can be entered and displayed.

The 3278-2A or 3279-2C has a total screen size of 2000 characters (25 lines of 80 characters each). The character positions on line 25 are used exclusively for indicating display console status. The remaining display screen is partitioned into two regions. The upper 20-line region is used and managed by the operating system. Lines 21 through 24 are reserved for displaying system status. Lines 21 through 25 are not available to the user.

## *Printers*

The 3268 Printer Model 2 or a 3287 Printer, matrix printers, can be attached as a console printer. The 3268 Printer Model 2 can operate at up to 340 characters per second. The operator can select 10 or 16.7 characters per inch, and 3, 4, 6, or 8 lines per inch.

The 3287 Printer has a nominal print speed of 80 characters per second (Models 1 and 1C) or 120 characters per second (Models 2 and 2C). A print operation can be initiated by application programs or by the operator using the Copy key. The Models 1C and 2C can print in color.

## *Operator Control Panel*

The operator control panel (OCP), used with the display console, controls and monitors 4341 operation. With the OCP, the operator can:

- Power the system on and off
- Load the support processor microcode
- Observe system status.

## 3278-2A or 3279-2C Display Console

The display console provides communication between the operator and the system. The operating system uses the display to pass messages to the operator, to present operating modes for selection and further definition, and to display information accessed or entered at the keyboard. The 3279-2C Color Display Console can display information in up to four colors (red, green, blue, and white) for improved readability.

| | | |
|---|---|---|
| ▶DISPLAY MODE | INSERT MODE | INHIBITED |
| ▶PTR/KYBD MODE | (or blank) | PTR-BUSY |
| ▶MANUAL CONTROL | | PTR-INTV REQD |
| ▶DISCONNECTED | | PTR-CHECK |
| ▶ | | USAGE CONFLICT |

**Figure 5. Display Console Status Indicator Layout (Line 25)**

### 4341 Display Console Indicators

Messages on line 25 of the 3278-2A or 3279-2C Display Console screen indicate the status of the device (Figure 5). Except when in Test mode, the indicator line is identified by the ▶ symbol when the display console 'power on response' is accepted. Only one indicator in each field is active at any given time.

***Display Mode*** indicates that the display console is available to the host operating system, using 3272 control unit interface or equivalent support.

***Ptr/Kybd Mode*** (printer/keyboard emulation mode) indicates that the display console is available to the host operating system, using 1052, 3210, or 3215 Console Printer/Keyboard interface support.

***Manual Control*** indicates that the display console is under the manual functions control and is not available to the operating system. In this mode, a Start I/O (SIO) to the display console is accepted but is held pending until the device is available to the operating system. If an SIO is enqueued, the audible alarm sounds and SYSTEM MESSAGE WAITING is displayed on line 23.

***Disconnected*** indicates that the device is not logically connected to the 4341, is not available to the operating system, and is not in use for manual functions. This condition exists when no unit address has been assigned to the display console.

***Insert Mode*** (keyboard insert mode) is displayed after the Insert key has been pressed and is reset by pressing the Reset key.

***Inhibited*** indicates that the keyboard input is inhibited because:

1. An Attention key (a PF key, ENTER, CNCL (PA2), REQ (PA1), MODE SEL, CHG DPLY, or DIAG) was pressed.
2. The operator attempted to alter a protected field.
3. The operator attempted to insert a character into a field that had no nulls.
4. Keyboard overrun (caused by multiple simultaneous key entries) occurred.
5. The Start, Stop, INTR, MODE SEL, CHG DPLY, or DIAG keys were pressed when *another* display console was already in Manual Control mode, or when a previous request had not been completed.

   When the keyboard is locked, the Inhibited indication is displayed. Certain functions, such as the Reset key, are accepted and processed when the keyboard is locked.

This indicator is reset by:

1. Pressing the Reset key, or
2. When the application program issues a Write command which specifies 'keyboard restore.' (This also resets the PTR-Busy, PTR-INTV REQD, and PTR-Check indicators.)

***Ptr-Busy*** (hard-copy printer busy) is displayed when a Copy request is issued to a hard-copy printer that is busy with a previous Copy request or with an SIO from the operating system. The Copy request is ignored.

This indicator is reset by pressing the Reset key.

***Ptr-Intv Reqd*** (hard-copy printer intervention required) is displayed if a Copy request is rejected because of an error condition from which the operator can recover, such as:

1. End of forms
2. Power off or in Test mode
3. No hard-copy device assigned.

This indicator is reset by pressing the Reset key.

***Ptr-Check*** (hard-copy printer equipment check) appears when an equipment check condition is detected while attempting to perform a Copy request.

This indicator is reset by pressing the Reset key.

***Usage Conflict*** appears when a function is not allowed at the present time. This occurs if the START, STOP, INTR, MODE SEL, CHG DPLY, or DIAG key, and so forth is pressed when another display console is already in manual functions control mode or when a previous request has not been completed.

This indicator is reset by pressing the RESET key.

## *3278-2A Switches and Controls*

The switches located on the 3278-2A Display Console control the operation of the unit.

***Power On/Off and Normal/Test Switches*** can be used to make the device ready (On and Normal positions) or not ready (Off or Test positions). In the not ready case, intervention required in the sense byte is set and Start I/O instructions to the device are rejected. When a not-ready-to-ready transition occurs, a device-end status is presented. Whenever the device is made not ready in this fashion, the current display console image is lost and is not recoverable. The top 20 lines of the screen are blank when the device is made ready.

***Mono/Dual Switch*** determines whether lowercase alphabetic characters are displayed in lowercase or uppercase. When the switch is set to Mono, all alphabetic characters are entered and displayed in uppercase. When set to Dual, both uppercase and lowercase characters are displayed.

***Contrast/Brightness and Alarm-Volume Controls*** are used to set up display console and alarm conditions appropriate to the operating environment or operator preference. These controls have no effect on the operation of the device and cause no error conditions.

## *3297-2C Switches and Controls*

- Power on/off
- Test/Normal
- Mono/Dual
- Brightness
- Volume
- Two Color/Four Color

The 3279-2C switches and controls function the same as those on the 3278-2A. The Two Color/Four Color switch (00/0000) enables the display to change from a base four-color presentation to a two-color (green/white) presentation which duplicates the 3278-2A mono-color presentation with intensification display.

## *Display Console Keyboard*

The display console keyboard is the operator's primary input device to the system. The keyboard controls the display console and provides a means of signaling the program. The keyboard allows operator communication with the processor to:

- Enter data
- Answer program generated requests
- Perform manual functions
- Enter system configuration.

The functional key groups are: Shift keys, alphameric and graphic keys, cursor control keys, input control keys, Program Attention keys, system function keys, and the Copy key.

1. Shift keys generate unique codes that are interpreted and acted on accordingly.
2. Alphameric and graphic keys are interpreted as data and displayed on the screen. Alphameric data characters appear on the display console screen at the cursor location, unless the cursor is in a protected field or in an attribute character location. The Enter or Program Function keys are used to indicate that data entry is complete. The alphabetic characters are displayed on the screen in either uppercase or lowercase.
3. Cursor control keys reposition the cursor on the screen.
4. Input control keys cause the character(s) in the input field(s) to be inserted, deleted, or erased.
5. Program Attention (PA) keys generate an attention interruption to notify the application program. An attention identification (AID) character is generated at the time of interruption to identify which Program Attention key caused the interruption.

| *Normal/Shift Mode* | | *Alternate Mode* | |
|---|---|---|---|
| *Function* | *AID* | *Function* | *AID* |
| CANCEL (PA2) | 6E | PF1 | F1 |
| REQUEST (PA1) | 6C | PF2 | F2 |
| ENTER | 7D | PF3 | F3 |
| | | PF4 | F4 |
| | | PF5 | F5 |
| | | PF6 | F6 |
| | | PF7 | F7 |
| | | PF8 | F8 |
| | | PF9 | F9 |
| | | PF10 | 7A |
| | | PF11 | 7B |
| | | PF12 | 7C |

6. System function keys (such as Start, Stop, and INTR) are used to control the 4341 processor, and are transparent to the user program.
7. Copy key performs a print operation, and is active only when the manual functions screen is in use. The data printed on the printer appears in the same characters and format that appears on the display console screen.

### *Testing Considerations*

The 3278-2A or 3279-2C Display Console has facilities to test the refresh buffer, keyboard, and execution of device Write commands.

***Test Mode 1*** is entered by powering on the 3278-2A or 3279-2C with the Test/Normal key in the Test position. The 3278-2A or 3279-2C automatically ripples the low-order eight bits of the I/O address counter into the refresh buffer. This displays the character set to verify that the 3278-2A or 3279-2C refresh buffer operation and the character generator are functioning correctly.

***Test Mode 2*** is entered automatically following test mode 1. In this mode, an operator can press any keyboard key (except the Reset key) and cause the unique code of that key to be written into the refresh buffer at the current I/O address counter address (appearing in row 1, column 1). After the data is written, the I/O address counter is incremented to the next sequential address. The operator can verify the operation of all keyboard keys with displayable key codes and the proper functioning of the data path from the keyboard to the refresh buffer.

***Test Mode 3*** is entered by pressing the keyboard Reset key. In this mode, the operator can execute any 3278-2A or 3279-2C command by pressing the appropriate key. If the command executed requires data to follow it, any key(s) except the Reset key can be pressed to provide the byte(s) of data. The Reset key must be pressed before another command is executed after data has been transferred from the keyboard.

## Display Mode

Display mode supports the 3278-2A Display Console or 3279-2C Color Display Console and an optional printer.

The user screen size is limited to 20 lines; only 1600 bytes of the 3278-2A or 3279-2C Display Console device buffer is available to the operating system. For the printer, 24 lines (1920 bytes) are available.

The display consoles and printers have unique unit addresses and are treated as independent devices. The device addresses (X'000'-X'0EF') on channel 0 can be selected by the operator at any time.

When the operating system or application program requires the display console for service, it issues an SIO to the channel. The channel starts the display console operation by issuing a 3270-mode CCW commands (see below). For more detailed information about 3270 commands, see the *IBM 3270 Information Display System Component Description,* GA27-2749.

### *3270-Mode CCW Commands*

| *Code* | *CCW Command* | *Initial Status* | *Ending Status* | *Async. Status* |
|---|---|---|---|---|
| 01 | Write | 00 | CE | DE |
| 05 | Erase/Write | 00 | CE | DE |
| 02 | Read Buffer | 00 | CE,DE | |
| 06 | Read Modified | 00 | CE,DE | |
| 0B | Select | CE | | DE |
| 0F | Erase All Unprotected | CE | | DE |
| 03 | No Operation | CE,DE | | |
| 04 | Sense | 00 | CE,DE | |
| E4 | Sense I/O | 00 | CE,DE | |

### *Device Status*

The display console status byte presented to the operating system can be generated synchronously or asynchronously. Synchronous status is passed to the host channel as ending status to a command.

| *Bit* | *Status* |
|---|---|
| 0 | Attention |
| 1 | Not used |
| 2 | Not used |
| 3 | Busy |
| 4 | Channel end |
| 5 | Device end |
| 6 | Unit check |
| 7 | Unit exception |

***Initial Status*** reflects the condition of the selected device on receipt of a command, and indicates to the channel whether or not the command can be executed.

***Ending Status*** reflects the condition of the selected device after all channel interface operations of a nonimmediate command are completed.

***Asynchronous Status*** reflects ending status for an immediate command (other than no operation), a second ending status for a Write or Erase/Write command, or an equipment condition or operator action (attention) not associated with command execution.

## Sense Byte

When an error is detected, the appropriate bit(s) are set as follows to describe the condition that caused the error. This sense byte is sent to the host channel when a Sense command is executed. Sense data is reset by every command except NOP.

| *Bit* | *Sense* |
|---|---|
| 0 | Command reject |
| 1 | Intervention required |
| 2 | Bus-out check |
| 3 | Equipment check |
| 4 | Data check |
| 5 | Unit specify |
| 6 | Control check |
| 7 | Operation check |

## Write Data Stream

Programming for a display console differs from most other I/O devices in that the CCW commands for a display console are fairly elementary, and the detailed data positioning and control attributes are imbedded within the data stream that is transferred by the CCW.

To control the information displayed on a display console, the application program must provide a write data stream that includes a write control character (WCC), buffer control orders, buffer address, attribute, and data. Only the attribute and data are stored into the device buffer. Invalid or undefined data (EBCDIC) in the data stream is displayed as a hyphen.

| *Bit* | *Write Control Character (WCC)* |
|---|---|
| 0 | Not used |
| 1 | 1 |
| 2,3* | Printout format<br>00=the NL order in the data stream; determines print line length<br>01=specifies 40-character print line<br>10=specifies 64-character print line<br>11=specifies 80-character print line |
| 4* | Start print |
| 5 | Sound alarm |
| 6 | Restore keyboard |
| 7 | Reset MDT |

* Used only when the Write is directed to the 3287 Printer.

| *Code* | *Buffer Control Orders* |
|---|---|
| 1D | Start field (SF) |
| 11 | Set buffer address (SBA) |
| 13 | Insert cursor (IC) |
| 05 | Program tab (PT) |
| 3C | Repeat to address (RA) |
| 12 | Erase unprotected to address (EUA) |

| *Bit* | *Attribute Character* |
|---|---|
| 0 | Determined by the contents of bits 2-7 |
| 1 | 1 |
| 2 | 0=Unprotected<br>1=Protected field |
| 3 | Bits 2,3=11 cause an automatic skip |
| 4,5 | 00=Normal display<br>01=Normal display<br>10=Intensified display<br>11=Nondisplay, nonprint |
| 6 | 0 |
| 7 | Modified data tag (MDT)<br>0=Field has not been modified<br>1=Field has not been modified by the operator or set by program in the data stream |

If a buffer address is specified past the end of the user buffer area (20 lines for the 3278-2A and 3279-2C, 24 lines for the 3268-2 and 3287), operation check sense is set. The command is aborted with device end and unit check status. When the operation check occurs because of an invalid buffer address, channel end may have been sent before the operation check was detected. The residual count filed is unpredictable in this case, and cannot be used to precisely determine the location of the error in the write data stream. The CCW address stored in the CSW may also be past the CCW pointing to the invalid data if data chaining is specified for the write command. The write data stream must be inspected to locate the invalid address specification.

## Color Console and Printer

The colors presented on the color console and printer are determined by the existing protection and intensification attribute bits of the displayed field.

The attribute bits, their field characteristics, and colors presented are:

| *Bits* | *Attribute Characteristic* | *Color* |
|---|---|---|
| 0 0 | Unprotected, Unintensified | Green* |
| 0 1 | Unprotected, Intensified | Red |
| 1 0 | Protected, Unintensified | Blue |
| 1 1 | Protected, Intensified | White<br>Black* (3287-1C,2C) |

*Green and black may be interchanged on the 3287-1C or 2C at the time the feature is ordered.

## *Read Data Stream*

Depending on the command, these types of Read data streams are generated:

1. Read Buffer data stream: In response to the Read Buffer command, the read data stream is generated with a three-character read heading that consists of the Attention Identification (AID) character followed by a two-character cursor address.

   The contents of all device buffer locations (lines 1-20 for 3278-2A or 3279-2C, lines 1-24 for 3268-2 and 3287) are transferred, including nulls. Start field (SF) order codes are inserted before each attribute character to identify the beginning of each field.

2. Read Modified data stream: In response to the attention interruption from pressing the Enter key or a Program Function key, the application program issues a Read Modified command to the display console. The first three-byte read heading of the read data stream are always the AID code and the two-byte cursor address.

   Following the read heading is the data of each modified field (lines 1-20 for 3278-2A or 3279-2C, lines 1-24 for 3268-2 and 3287). The data for each field is preceded in the data stream by a Set Buffer Address (SBA) order code followed by the two-byte buffer address of the first character position in that field (the attribute address +1).

## *Programming Information*

The concepts of protected or unprotected data, and the modified data tag function are basic to the modes of operation.

**Protected Data Autolock**

A program-controlled facility of the display console allows fields to be defined as *protected* or *unprotected.* A protected field is a field that the operator may not alter in any way. If an attempt is made to enter an alphameric character when the cursor is located in a protected field, the keyboard becomes disabled by the autolock function.

In an unprotected field, the operator can enter, modify, and erase alphameric data.

**Modified Data Tag**

To identify data fields that have been modified, the modified data tag (MDT) bit (bit 7 of the attribute character) is set to a 1. This process is called *tagging* the field.

Data in protected or unprotected fields can be tagged as having been modified. In protected fields, the tags are set under program control. In unprotected fields, modified data tags are also set by keyboard operation. These tagged fields are the only fields transferred on execution of a Read Modified command.

## *Display Mode Error Handling*

When attempting any recovery after a unit check is reported to the operating system, use error recovery procedures in the *IBM 3270 Information Display System Component Description,* order no. GA27-2749.

## *3268 Model 2 and 3287 Printers*

These optional printers provide a hard copy of the information that is displayed on a 3278-2A or 3279-2C Display Console, or of information written from the application program.

All 3270-mode CCW commands and data stream to the 3278-2A or 3279-2C Display Console can be issued to the printer. Printouts can be formatted in the same manner as a display image. Cursor information is ignored by the printer.

When a print operation is specified by a Write command addressed to the printer, the print line format in which the data is to be printed can be specified as part of the command in one of three printer formats. These formats simply define the print line length: 40, 64, or 80 character positions per line. If a format is not specified, the print line length is set to the default for the printer.

Printer control orders (NL, EM, and FF) are transferred as part of the data stream from the application program. They are stored in the printer buffer as data.

> **Note:** If a write buffer has been issued but the buffer not printed, the printer appears busy to a Copy key request.

### *Error Handling*

The recovery procedures for errors detected by the 3287 are categorized in three ways:

1. Automatic recovery – The Alphameric Readout (ANR) may or may not be used to indicate the reason code.

2. Manual intervention recovery – Printer check light is turned on and ANR indicates the reason code.

3. Machine stop – Printer check light is turned on and ANR indicates the reason code.

## Printer/Keyboard Emulation Mode

The printer/keyboard emulation mode allows the processor to run operating systems and programs designed for devices such as the 1052, 3210, or 3215. Although physically different, these devices accept the same commands and respond similarly. They are emulated on a 3278-2A or 3279-2C Display Console with a recommended optional printer coupled as a hard-copy device.

Printer/keyboard emulation mode requires one 3278-2A or 3279-2C Display Console. Options allow three additional 3278-2A, 3279-2C, 3268-2 or 3287 devices to be attached to the support processor and configured as needed.

In *coupled* mode, all data read from or written to the device is printed on the printer. In *uncoupled* mode, only up to the last 18 lines of data are displayed on the 3278-2A or 3279-2C. No hard-copy record is made. To couple, assign the same device address to a display console and printer by using the console functions program load (L) screen.

Both the display console and the printer appear to the operating system as one device. The device addresses used are selected by the operator and can be modified at any time. A maximum of two printer/keyboard devices can be configured at a time.

In printer/keyboard emulation mode, the display console accepts printer/keyboard commands and responds with status and sense information. The data received or sent with the commands is formatted to appear on the display console and optional printer like the actual devices being emulated.

Indicators and keys to emulate printer/keyboard functions are displayed on the 3278-2A or 3279-2C Display Console to allow the functions to be performed by the operator.

### *Screen Management*

When the display console is in printer/keyboard emulation mode, the whole screen is controlled by the emulation facility. The screen is initialized the first time printer/keyboard emulation mode is entered, either via operator action (Attention keys or making device ready) or by channel action (SIO or reset). After the screen is initialized, the operator can only enter data on the screen when a Read command is issued. At all other times, the whole display is protected from operator alteration.

The screen is divided into three areas. Lines 1-18 are the message area for displaying the operator input and host program output messages. Lines 19-20 are the operator input area. Up to 126 characters are allowed for each read operation. Part of line 20 displays 1052 keyboard indicators (Request, Proceed, Alarm, and INTV REQD). Lines 21-24 display the system status. The character positions on line 25 are exclusively for indicating display console status.

A message in the input area transferred to the host program is also displayed in the message area. Input and output messages are displayed sequentially starting from the top (line 1) as if they were printed on the printer/keyboard device.

When the display message reaches the bottom (line 18), scrolling takes place. The top six lines (lines 1-6) are rolled off the screen and the bottom six lines (lines 13-18) are made available for later input.

#### Display Area

The display area starts in line 1, column 1, and ends on line 18, column 79. The display area is protected by an attribute at line 20, column 80. This area shows the last 18 lines of data that has been read or written to the device. The data is organized into lines corresponding to lines of printer/keyboard output, with each new line beginning in column 1 of a display area line. A line longer than 80 characters (the display area line length) wraps to the next line in the display area, to a maximum of 126 characters.

To allow the maximum amount of data to be displayed, multiple new line characters (NL = X'15') in a write data stream result in only one blank line on the display console. This prevents data from being scrolled off the screen when new line characters are added to space the printer output. The new line suppression only applies within a command; each new command is treated separately. Therefore, multiple blank lines caused by two or more commands are not suppressed.

**Input Area**

The input area is defined by an attribute at line 18, column 80, and contains 126 characters on lines 19 and 20. This area is unprotected only when a Read command is in progress (Proceed indicator displayed) to permit data entry or modification. At all other times, it is protected from operator alteration.

Pressing the Enter or Cancel key transfers the data in the input area across the channel. Data accepted by the channel for a Read command is then moved to the display area and printed. If the channel terminates data transfer before all data entered by the operator was sent, only that data accepted appears in the display area.

The field initially contains all nulls (X'00') that are compressed out of the Read data and not transferred to the channel. If a space (X'40') is desired in the response, the Space key must be used to enter it. Cursor movement keys leave nulls in the input area. These nulls are compressed from the data.

**Indicator Area**

The indicator area is a brightened field defined by an attribute on line 20, column 47, and is 32 characters in length. This area contains the following visual indicators:

***Proceed*** appears whenever a Read command is in progress for entry of data in the input area. Proceed is cleared when the Read command is ended by any of the following conditions:

- Normal ending caused by Enter or Cancel key
- A system or selective reset
- A Halt Device or Halt I/O instruction issued to the device.

***Request*** indicates that a REQ (Request) key attention status has been stacked because the device is busy executing a command. When the current operation completes, the attention status is presented to the channel, and the Request indicator is reset. A system or selective reset also resets the Request indicator.

***Alarm*** appears, and the audible alarm sounds, whenever an Alarm command is received. The indicator is reset by any of the following:

- Pressing a Program Function (PF) key
- Pressing the Enter or Cancel key when Proceed is not displayed
- System or selective reset occurs.

***Intervention Required (INTV-REQD)*** appears if the 3268-2 or 3287 Printer coupled as a hard-copy device becomes Not Ready. This condition occurs when end-of-forms, power off, or other check conditions are present. A Start I/O is not accepted. When the check condition is cleared, the indicator is erased, and device-end status is presented to the channel.

## *3278-2A and 3279-2C Console Keyboard Operation*

The 3278-2A or 3279-2C Display Console keyboard is used to communicate with the processor. In printer/keyboard emulation mode, the display console always contains a formatted screen defining protected and unprotected fields. The response for the different keys is:

***Alphameric and Special Character Keys*** can only be used when an unprotected field is present, which is only during a Read command (Proceed indicator displayed). Such use causes the character to appear and the cursor to advance. At all other times, or if the cursor is not in the input area, using these keys causes the Inhibited message to appear on line 25 of the display console. The inhibited condition can be cleared with the Reset key.

***Request (REQ) Key*** initiates communication with the operating system by sending an attention status (X'80'). If the request status cannot be sent immediately because of a busy condition, the Request indicator appears, and the attention is stacked. When the device becomes not busy, the attention is sent, and the Request indicator is reset.

Note: Do not confuse the REQ and INTR keys: the red INTR key causes an External Interrupt and is not used with printer/keyboard emulation mode operation.

***Enter Key*** is used during a Read operation when data entry is complete. The data is read, and the input area is cleared and protected. This key is equivalent to the End-of-Block (EOB) or End keys on the emulated device. If no Read is in progress, the Alarm indicator is reset, and the keyboard is unlocked.

***Cancel (CNCL) Key*** serves the same function as the printer/keyboard Cancel key. During a Read operation, this key sends a cancel response to the channel. The cancel response is a channel end with unit exception (X'09'). The input area is cleared and protected, and an asterisk (*) is written in the display area. No data is transferred. If no Read is in progress, the Alarm indicator is reset and the keyboard unlocked.

***Program Function Keys (PF1-PF12)*** reset the Alarm indicator and unlock the keyboard.

***Cursor Movement Keys*** move the cursor without causing any modifications to the screen. They may be used at any time and cause no errors. The cursor is positioned at the start of the input area when a Read command is initiated. The cursor must be in the input area to enter data. The Tab and Backtab keys always position the cursor at the beginning of the input area if a Read is in progress. Pressing the New-Line key places the cursor in the first column of either line 19 or 20.

***Erase Input and Erase EOF Keys*** clear the input area when a Read is in progress. The Erase Input key clears the whole field and repositions the cursor. The Erase EOF (End-Of-Field) key clears the field from the current cursor position to the end of the input area.

***Insert and Delete Keys*** selectively add and delete characters when entering and altering data in the input area.

## *3268 Model 2 and 3287 Printers*

A 3268-2 or 3287 (optionally coupled as a hard-copy device in printer/keyboard emulation mode) can print all data that has been transferred. The data is arranged in lines of 126 or fewer characters, as they would appear on the emulated printer. Each line is printed when it is completed; that is, when any of the following conditions occurs:

- 126 bytes of data have been received since the beginning of the line.
- A New-Line character (X'15') is found in a Write or Write-ACR command data stream.
- All data has been received on a Write-ACR command.
- After a Read command is executed.
- A system or selective reset occurs.

Note that, after a Write command (X'01') is executed but a complete line has not been accumulated, the last partial line is not printed. The data is accumulated in the printer buffer and is printed when the line is completed by succeeding commands. During this time, the printer is busy to a Copy key request.

A system or selective reset causes a line feed to be performed if no data is present in the buffer.

### *Printer/Keyboard Commands*

Printer/keyboard emulation mode accepts and executes all commands that are valid for the emulated device. The valid commands and the normal status responses received are:

| *Code* | *Command* | *Initial Status* | *Ending Status* | *Async. Status* |
|---|---|---|---|---|
| 01 | Write | 00 | CE | DE |
| 09 | Write ACR | 00 | CE | DE |
| 0A | Read Inquiry | 00 | CE | DE |
| 04 | Sense | 00 | CE,DE | – |
| 03 | NOP | CE,DE | – | – |
| 0B | Alarm | CE,DE | – | – |
| E4 | Sense I/O | 00 | CE,DE | – |

It is assumed that an alternate console printer has been coupled as a hard-copy device. If not, ending status for a command is presented to the channel after the data has been placed in the display console area.

#### Write

The Write command transfers data from the channel to an internal buffer, and then processes a line at a time to the display area on the 3278-2A or 3279-2C and prints it on the printer. When all the data has been received, channel-end status is returned and the last line is processed. If the last line is not

complete (ended with New-Line character or exactly 126 bytes), device-end status is sent after the data has been placed in the display area and saved in the printer buffer without printing. If the command ends with a complete line, device-end status is sent when printing is finished. The Write command continues requesting data from the channel until the channel stops data transfer (when the CCW count reaches zero). Therefore, Incorrect Length channel status is always indicated with a zero residual count unless the Suppress Incorrect Length Indicator (SILI) CCW flag is on.

**Write-ACR (Automatic Carriage Return)**

This command is similar to the Write command except that at the end of processing, printing of the last line is started and an automatic carriage return (ACR) is performed.

**Read-Inquiry**

When the Read-Inquiry command is received, the input area is unprotected and the Proceed indicator is turned on. The command then waits until the operator signals that data entry is complete (by pressing the Enter or Cancel key).

If the Enter key is pressed, the data is read from the input area and transferred to the channel. (Channel end is presented after data transfer.) Then any data the channel accepted is written to the display area and printed on the printer.

If the Cancel key is pressed, a channel end with unit exception is presented to the channel, and an asterisk (*) is written to the display area and printed.

After printing is completed, a device end is sent to terminate the command.

**Sense**

The Sense command transfers one byte of sense information. After the sense byte is accepted, channel end and device end are presented as ending status. The sense byte is reset at the initiation of any command except Sense. The sense byte is defined as:

| *Bit* | *Code* | *Sense Information* |
|---|---|---|
| 0 | CR | Command Reject |
| 1 | IR | Intervention Required |
| 2 | BOC | Bus-Out Check |
| 3 | EC | Equipment Check |
| 4 | — | Unused; always 0 |
| 5 | — | Unused; always 0 |
| 6 | — | Unused; always 0 |
| 7 | — | Unused; always 0 |

**Sense I/O**

This command is used for device type identification. If the device is not busy or not ready, seven bytes of fixed data are presented:

| | |
|---|---|
| *Printer/Keyboard Mode* | |
| PTR/KBD | X'FF434100105200' |
| *Display Mode* | |
| 3278-2A | X'FF43410032782A' |
| 3279-2C | X'FF43410032792C' |
| 3287 | X'FF434100328700' |
| 3268-2 | X'FF434100328700' |

**No Operation (NOP)**

This control command results in an immediate channel end and device end. No action is performed in the device. This command can be used to clear any outstanding status or to cause a command chain to end with a channel end and device end together.

**Alarm**

This control command sounds the audible alarm on the display console and displays the Alarm indicator. If the display is Not Ready, the command functions as a NOP. Immediate channel end and device end are presented as initial status. The command is accepted even if an intervention required condition exists.

## *Device Status*

The following status bits are set:

| *Bit* | *Status* |
|---|---|
| 0 | Attention |
| 1 | Unused |
| 2 | Unused |
| 3 | Busy |
| 4 | Channel end |
| 5 | Device end |
| 6 | Unit check |
| 7 | Unit exception |

Unlike the display console, the following interfaces are specific for the printer/keyboard Read operation:

- The attention bit is set to one when the Request key is pressed. This attention status is presented to the channel when no other operation is in progress. The host program should react to the attention interruption by issuing a Read command.
- No AID is generated for an attention interruption.

## *Error Conditions*

The following error conditions can occur while operating in printer/keyboard emulation mode:

**3278-2A or 3279-2C Display Console Not Ready**

When the 3278-2A or 3279-2C is not ready because of any of the following conditions, a Write, Write-ACR, Read, or NOP command is rejected. The Sense and Alarm commands are always accepted.

***Power Off:*** When the display console is not powered on, an intervention required condition exists and is reported to a Sense command.

***Test Mode:*** When the 3278-2A or 3279-2C is in test mode (Test/Normal switch in Test position), an intervention required condition exists and is reported to a Sense command.

***Device Not Functional:*** If the 3278-2A or 3279-2C hardware is failing, or the device is incorrectly configured or not connected, an intervention required or equipment check condition exists and is reported to a Sense command.

**Console Printer Not Ready**

The 3268-2 or 3287 Printer is in a not ready state because of any of the following conditions:

***Power Off:*** When power is off to the printer, an intervention required condition exists and is reported to a Sense command.

***Test Mode:*** When the printer is in test mode (by pressing the Test switch), an intervention required condition exists and is reported to a Sense command.

***End-of-Forms:*** When the End-of-Forms switch indicates that no paper is in the printer and a one-minute timeout occurs, an intervention required condition exists and is reported to a Sense command. The INTV-REQD indicator is displayed only after the timeout condition occurs. This delay allows the operator to correct the end-of-forms condition and have the printer continue printing with no errors reported or software retry required. The end-of-forms condition causes the audible alarm to sound until the HOLD PRINT switch is pressed. The end-of-forms condition is cleared by pressing the HOLD PRINT switch, replacing the forms, then pressing the ENABLE PRINT switch.

***Hold Print Timeout:*** When the HOLD PRINT condition lasts longer than ten minutes, an intervention required condition exists and is reported to a Sense command. The INTV-REQD indicator is displayed only after the ten-minute timeout occurs.

***Device Not Functional:*** When the console printer is not operating because of error conditions, incorrect connection, or invalid configuration, an intervention required or equipment check condition exists.

## *Restrictions and Functional Differences*

When operating in printer/keyboard emulation mode, consider the following:

**Timing**

The length of time taken to execute a command may differ from the emulated devices. Typically, the time from Start I/O until the associated channel end is much shorter, and the time from channel end to device end is longer due to buffering because printing is not started until a complete line is received.

The printing speed of the 3287 or 3268-2 is much faster than the 1052 and the other emulated devices. Using printer/keyboard emulation mode results in a considerable gain in throughput.

When running in uncoupled mode (3278-2A or 3279-2C without a printer), a timing delay of 0.5 seconds per line is added to improve display console readability.

**Keyboard Differences**

The 3278-2A or 3279-2C and emulated keyboards differ in both the number of keys and the keyboard layout. Because all the keys on the 3278-2A or 3279-2C can be used even if the emulated printer/keyboard has no corresponding key, it is possible to read and write characters that are not implemented on the emulated device.

Note that the Carriage Return key on the emulated keyboard is not implemented. Programs that require the use of this key are not supported in printer/keyboard emulation mode.

# Model-Dependent Information

This section addresses the 4341 implementation of certain 4300 Processors facilities and functions. (The terms used here are defined elsewhere in this manual, or in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* or in the *IBM System/370 Principles of Operation.)*

***Addressing of Natively Attached I/O Devices:*** Addresses F2 through F5 are for the 3278-2A and 3279-2C Display Consoles or 3268-2 and 3287 Printers. (Address F0 and F1 are spares.)

***Condition Code Setting:*** The nullification of the NC, CLC, OC, XC, TRT, and ZAP instruction execution does not cause the instruction to be executed as if it were specified as a no operation. The Condition Code may be altered by any of these six instructions even though the instruction has been nullified.

***Detection of a PSW Loop:*** A continuous string of interruptions (PSW loop) may be indicated if pressing the Stop key does not stop processing. Under this condition, a system reset may be necessary to stop.

***Segment Table Entry:*** The 4341 does not check bits 4-7, 29, and 30 of the segment table entry for zeros.

***Timing Facility Damage:*** The 4341 does not distinguish between the failure of the three timing facilities: TOD clock, CPU timer, and clock comparator. Any failure of hardware timing facilities causes all three facilities to enter the error state.

***Storage Size and Page Capacity Count (PCC):*** When in ECPS:VSE mode, the virtual storage size is 16,777,216 bytes and cannot be altered (as described in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode).* No *storage size control* is on the display console. The value of the page capacity count (PCC) is always 8192.

***Timer and Clock Resolution:*** The interval timer is updated every 3.328 milliseconds. The processor skips one update every 625 updates to derive the average of 3.333 milliseconds. The conditions of losing a decrement update are:

- When the Interval Timer control on the display console is set to Off
- When the processor is not in the operating state
- When the Rate Control on the display console is set to Instruction Step.

The time-of-day clock resolution is one microsecond. The 1-MHz oscillator has a tolerance of 0.0027 percent.

The CPU timer and clock comparator have the same resolution as the time-of-day clock. Time-of-day clock updates that are interrupted during an instruction retry are readjusted following the retry.

***Reference and Change Recording:*** The recording of reference and change bits is accurate with the following exceptions:

- The reference bit may be set because of storage operand fetching of a nullified or suppressed instruction.
- The reference bit may be set because of prefetching of an instruction (instruction buffering). Prefetching can be a minimum of one instruction up to a maximum of four instructions ahead. This can be a minimum of two bytes and, up to a maximum of eight bytes in advance.
- The reference bit may be set because of channel prefetching of CCW, IDAW, or data during an output operation.
- Change bits may be set for the operands of a unit of operation that is nullified because of a page translation exception. For example, the destination operand of a Move instruction may cross a page boundary and encounter a page translation exception at the boundary. In this case, the instruction is nullified so that the portion of the operand up to the boundary is restored to its original value, but change bits may remain set after the nullification of the instruction.

***Nontransparent Suppression and Nullification:*** The channel may observe the effect of temporary storage change of a partially executed, but nullified or suppressed, instruction. This can occur because of an operand access exception, access retry (lack of pretest), and instruction retry.

***Machine Check Handling:*** Machine check handling is implemented in the 4341 as follows:

- CR14 Machine Check Control Bits:

  Bit 4: Recovery Report Mask
  Bit 6: External Damage Report Mask

- Machine Check Interruption Code (MCIC):

  Bit 0: System Damage
  Bit 1: Instruction Processing Damage
  Bit 2: System Recovery
  Bit 3: Interval Timer Damage
  Bit 4: Timing Facility Damage
  Bit 15: Delayed
  Bit 16: Storage Error
  Bit 18: Storage Key Error Uncorrected
  Bit 20: PSW EMWP Validity
  Bit 21: PSW Mask and Key Validity
  Bit 22: PSW Program Mask and Condition Code Validity
  Bit 23: PSW Instruction Address Validity
  Bit 24: Failing Storage Address Validity
  Bit 27: Floating-Point Register Validity
  Bit 28: General Register Validity
  Bit 29: Control Register Validity
  Bit 31: Storage Logical Validity
  Bit 46: CPU Timer Validity
  Bit 47: Clock Comparator Validity

- Other CR14 and MCIC bits are not set by the 4341.

***Machine Check Interruptions:*** Machine check interruptions do not report failures detected during channel operations. A machine check interruption can occur when the malfunction also causes an IPU operation to be retried or terminated.

***CCW Prefetch:*** The channels do not prefetch a CCW for data chaining on input operation.

***Power-On State:*** Before the operator control panel (OCP) indicates power-on complete, the following components must have completed power-on in the sequence:

1. Support Processor
   System Diskette Drive
   Adapters
   Display Console
2. Processor
3. Channel-to-Channel Adapter
4. Channel Attached I/O Devices

Power to these components is controlled by the OCP power control.

The optional 3278-2A or 3279-2C Display Consoles (alternate console) and console printers enter the power-on state by the operator activating their power-on switches.

# Facility Descriptions

This section describes some of the significant 4341 facilities.

## *Instruction Set*

The universal instruction set is implemented in the 4341. For details on instruction word formats and definitions, refer to the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* or the *IBM System/370 Principles of Operation.*

## *Byte-Oriented Operands*

The byte-oriented operand facility allows the processor storage operands of unprivileged instructions to appear on any byte boundary without causing a specification exception and a program interruption.

This facility applies to fixed-point operands, floating-point operands, and logical operands. It does not apply to instruction addresses, privileged instructions, and channel command words (CCWs). 0.8 For the definition and limitations of boundary alignment operations, refer to the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* or the *IBM System/370 Principles of Operation.*

> **Note:** Optimum performance for RS and RX format instructions occurs only when operands are aligned.

## *Time-of-Day Clock*

The time-of-day clock provides a consistent measurement of elapsed times that can be used for indicating the time of day. The facility consists of a 64-bit binary counter with bit positions that correspond to those of a fixed-point number in doubleword format. Time is measured by the clock increasing its value incrementally, according to the rules of fixed-point arithmetic. Bit position 51 of the counter is incremented at 1-microsecond intervals.

The instructions included are: Store Clock and Set Clock. The Store Clock instruction allows the clock to be inspected and causes bits 0 through 51 of the current clock value to be placed in processor storage; bits 51 through 63 are stored as zero. The Set Clock instruction allows the clock to be set to a specific value and replaces bits 0 through 51 of the current clock value by an operand that is designated by the instruction; bits 52 through 63 are not used.

The clock value stored by a Store Clock instruction may be affected by I/O interference.

When system power is turned off, the clock value is lost.

Some check stops lose the value of the time-of-day clock.

Once the time-of-day clock has been enabled, and made operational with the Set Clock instruction, it maintains a constant rate of increase. The full cycle of the clock is about 143 years. This timing operation is *not* affected by:

- Any normal activity or event in the system
- Wait state
- Stopped state
- Instruction-step mode
- Single-cycle mode
- Test mode*
- System reset
- Initial Program Load (IPL) procedure
- Initial Microcode Load (IML) procedure

* The clock value is lost when the time-of-day clock microdiagnostic tests are performed.

## *Time-of-Day Clock Instructions*

The clock value can be accessed by the Store Clock instruction. This causes the current clock value to be stored in a processor storage location specified by the instruction.

The clock can be set to a specific value by the privileged Set Clock instruction. This causes the current clock value to be replaced by the value specified in the instruction. The Set Clock instruction changes the clock value only when the TOD CLK setting is ENABLE SET.

## *Clock Comparator and CPU Timer*

The clock comparator provides for an inter- ruption when the time-of-day clock reaches a value specified by the programmer. The interruption is allowed by setting bit 20 in control register 0 and the external mask bit in the PSW.

The clock comparator has the same format as the time-of-day clock. It consists of bits 0 through 47, which are compared with the corresponding bits of the time-of-day clock. A clock comparator interruption is indicated as an external interruption with an interruption code of 1004 (hex).

The programmer can inspect the clock comparator by using the Store Clock Comparator instruction and can set the comparator by using the Set Clock Comparator instruction. The contents of the clock comparator are reset to 0 by initial program reset.

## *CPU Timer*

The CPU timer provides a high-resolution (1-microsecond) timer that causes an interruption whenever its value is zero or negative. The timer value is set by using the Set CPU Timer instruction. The interruption is allowed by setting bit 21 in control register 0 and the external mask bit in the PSW.

The timer measures processor elapsed time and causes an interruption at the end of the period that has been specified by the programmer. This interruption is indicated as an external interruption with an interruption code of 1005 (hex).

The CPU timer has a format similar to bits 0 through 47 of the time-of-day clock, except that bit 0 is regarded as a sign bit. The CPU timer is decremented when the processor is executing instructions and during the wait state, but is not decremented when the processor is in the stopped state.

The programmer can inspect the CPU timer by using the Store CPU Timer instruction and can set the timer to a specific value by using the Set CPU Timer instruction. The contents of the CPU timer are reset to 0 by initial program reset.

Four instructions are provided:

Set Clock Comparator
Store Clock Comparator
Set CPU Timer
Store CPU Timer.

Further details of these instructions are found in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* or the *IBM System/370 Principles of Operation.*

## *Interval Timer*

The interval timer provides external interruption on a program-controlled time basis. The storage word at processor storage locations 80 through 83 (decimal) is reserved for the interval timer. Any value stored at this location is automatically reduced by decrementing bit 23 every 3.333 milliseconds, provided the Interval Timer switch is in the ON position.

The program in process can be automatically interrupted by an external interruption (if PSW system-mask bit 7 and bit 24 in control register 0 are ones) when the interval timer word goes from a positive to a negative value. The interruption is identified by setting the appropriate bit on in the interruption code.

The high-order 24 bits of the interval timer word provide a full cycle of about 15.5 hours.

Uses of the interval timer include:

- Job accounting
- Monitoring for perpetual program loops
- Time stamping
- Polling at timed intervals.

## *Interval Timer Switch*

When the Interval Timer switch is set to ON, the value stored in the interval timer word is automatically decremented immediately.

When the Interval Timer switch is set to OFF, no decrementing of the interval timer word takes place. The four bytes can be used for normal program applications. Displaying processor storage locations 80-83 (decimal) under this condition displays the last information stored. This information could be either the interval timer setting or other program information.

### *CPU Identification*

Information identifying the processor is stored in an eight-byte field of processor storage that is designated by the operand address of the Store CPU ID instruction. The format of the stored information is:

| | |
|---|---|
| Bits 0-7 | Version code (zeros) |
| Bits 8-31 | Processor serial number |
| Bits 32-47 | Processor model number |
| Bits 48-63 | All zeros |

### *Channel Identification*

Information that identifies a designated channel is stored in processor storage at location 168 (decimal) as described in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode.* Bits 16 through 23 of the sum that is formed by adding the contents of register B1 and the contents of the D1 field of the Store Channel ID instruction identifies the channel to which the instruction applies.

**Note:** The block-multiplexer channels appear as selector channels to I/O devices that do not block multiplex.

### *Channel-to-Channel Adapter*

The channel-to-channel adapter provides a path for operations to take place between two channels and synchronizes those operations. The adapter uses one control unit position on each of the two channels, but only one of the two connected channels requires the adapter to be installed. The adapter is attached to a block-multiplexer channel on the 4341. The other system can be any System/360, System/370, or 4300 processor.

The adapter operates in burst mode and transmits data at the rate of the lower-speed channel. The adapter is selected and responds the same as any control unit. The adapter accepts and decodes commands from the channel; however, it differs from a control unit in that it does not use these commands to operate and control input/output devices. The adapter instead uses the commands to open a path between the two channels it connects and then synchronizes the operations performed between the two channels.

### *System Control*

The basic control (BC) and extended control (EC) modes are submodes of both System/370 and ECPS:VSE mode, under the control of the current PSW and control registers. (BC and EC modes are described in detail in the *IBM 4300 Processors Principles of Operation for ECPS:VSE Mode* and the *IBM System/370 Principles of Operation.)* The current PSW is loaded from processor storage by the Load PSW instruction, and is stored in various permanently assigned areas of processor storage when an interruption is accepted.

### *PSW Format*

Bit 12 of the PSW controls the use of EC mode, which can be selected when a new PSW is obtained; that is:

- After an interrupt
- When the Load PSW instruction is used
- After initial program loading
- When a PSW restart operation is performed.

When the programmer selects EC mode, the PSW format changes by the removal of channel mask bits, instruction length code, and interruption code, and by the insertion of mode and mask bits for control of the additional functions. Permanent processor storage allocation is extended by placing the interruption code (and its extensions) and the instruction length code in locations higher than 128 (decimal).

### *Program-Event Recording*

Program-event recording (PER) aids in debugging programs. It permits the program to be alerted to:

- Execution of a successful branch instruction
- Alterations of the contents of designated general registers
- Fetching of an instruction from designated processor storage locations
- Alterations of the contents of designated processor storage locations.

The program has control over the conditions that are considered events for recording purposes and that can specify selectively one or more events to be monitored. Information about a program event is provided to the program by a program interruption. The cause of the interruption is identified in the interruption code.

Information for controlling program-event recording resides in control registers 9, 10, and 11. Control register 9 specifies which events are to be monitored.

Control register 10 designates the beginning of the monitored processor storage area. Control register 11 designates the end of the monitored processor storage area.

Program-event recording is available only in EC mode and is under the control of PSW bit 1, the PER mask. When the mask is 0, no program event can cause an interruption. When the mask is 1, interruptions are permitted subject to the PER control bits in control register 9. In BC mode, the PER mask has, in effect, a value of zero and program-event recording is disabled.

When a designated program event occurs with the processor enabled for program-event recording, a program interruption occurs. The cause of the interruption is identified by setting bit 8 of the interruption code to 1 and by the information placed in locations 150-155 of processor storage. (If a PER interruption occurs simultaneously with another program interruption, the interruption code indicates both conditions.)

This facility should be used only for program debugging purposes because PER causes significant internal performance degradation.

## *Store Status and Machine Save*

The System/370 mode includes an operator initiated function called *store status.* This function places the contents of the programmable registers in fixed locations within the first 512 bytes of processor storage. The programmable registers are stored in absolute locations as shown in the following table:

| *Register* | *Length in Bytes* | *Absolute Address of First Byte Stored* | |
|---|---|---|---|
| | | *Decimal* | *Hex* |
| CPU Timer | 8 | 216 | D8 |
| Clock Comparator | 8 | 224 | E0 |
| Current PSW | 8 | 256 | 100 |
| Floating-Point Registers 0-6 | 32 | 352 | 160 |
| General Registers 0-15 | 64 | 384 | 180 |
| Control Registers 0-15 | 64 | 448 | 1C0 |

The similar function in ECPS:VSE mode is called *machine save.* This function saves the above data as well as page 0 (address 0-2000) in auxiliary storage for subsequent retrieval.

# Instruction Timing Information

This section describes the basic 4341 instruction timings and storage cycle times.

## *Processor Instruction Timings*

Listed below are the formulas for determining the instruction execution times in nanoseconds. These formulas do not include any allowance for high-speed buffer storage misses, TLB misses, or processor interference because of I/O operations, processor storage refresh, or interval timer updates. These factors must be considered separately.

Each access to processor storage for a doubleword or less requires 225 nanoseconds. The timing formulas assume that the storage operands are aligned on doubleword boundaries. If a storage operand is not aligned on a doubleword boundary, additional access(es) may be needed. For each such access, add 225 nanoseconds to the instruction time obtained by using the appropriate formula.

For indexing operations in RX instructions that use a nonzero index register, add 150 nanoseconds.

***Accuracy Codes:*** Formulas with no identified accuracy code yield instruction execution times accurately.

Formulas with Accuracy Code I may not yield exact instruction times, but represent *average* execution times that can be expected in representative instruction sequences.

Formulas with Accuracy Code II yield instruction timing values given below, within 5 percent.

## *4341 Model Group 1 Instruction Timing List*

| *Instruction Name* | *Format* | *Mnemonic* | *Op-Code* | *Accuracy Code* | *Formula and Comments* |
|---|---|---|---|---|---|
| Add | RR | AR | 1A | | 375 |
| Add | RX | A | 5A | | 600 |
| Add Decimal | SS | AP | FA | | 1275+RC•1125+ZR•1050 (for L1≤8 and L2≤8) |
| | | | | | 1950+RC•1275+ZR•1050 (for L1≤8 and L2>8) |
| | | | | | 2625+RC•1275+ZR•1050 (for L1>8 and L2≤8) |
| | | | | | 2700+RC•1275+ZR•1050 (for L1>8 and L2>8) |
| Add Halfword | RX | AH | 4A | | 600 |
| Add Logical | RR | ALR | 1E | | 375 |
| Add Logical | RX | AL | 5E | | 600 |
| Add Normalized (Extended) | RR | AXR | 36 | I | 3834 |
| Add Normalized (Long) | RR | ADR | 2A | I | 1050 |
| Add Normalized (Long) | RX | AD | 6A | I | 1425 |
| Add Normalized (Short) | RR | AER | 3A | I | 1134 |
| Add Normalized (Short) | RX | AE | 7A | I | 1472 |
| Add Unnormalized (Long) | RR | AWR | 2E | I | 986 |
| Add Unnormalized (Long) | RX | AW | 6E | I | 1511 |
| Add Unnormalized (Short) | RR | AUR | 3E | I | 1166 |
| Add Unnormalized (Short) | RX | AU | 7E | I | 1689 |
| And | RR | NR | 14 | | 375 |
| And | RX | N | 54 | | 600 |
| And (Character) | SS | NC | D4 | | 1275 (for L≤8) |
| | | | | | 900+L8•825 +LZ8•75 (for L>8) |
| | | | | | 900+L•825+LZ•75 (for operands overlap) |
| And (Immediate) | SI | NI | 94 | | 825 |
| Branch And Link | RR | BALR | 05 | I | 750+S•675 |
| Branch and Link | RX | BAL | 45 | I | 1275 |

| *Instruction Name* | *Format* | *Mnemonic* | *Op-Code* | *Accuracy Code* | *Formula and Comments* |
|---|---|---|---|---|---|
| Branch on Condition | RR | BCR | 07 | I | 150+S•675 |
| | | | | | 1125 (for serialization case) |
| Branch on Condition | RX | BC | 47 | I | 150+S•525 |
| Branch on Count | RR | BCTR | 06 | I | 525+S•525 (for R2≠0) |
| | | | | | 300 (for R2=0) |
| Branch on Count | RX | BCT | 46 | I | 375+S•525 |
| Branch on Index High | RS | BXH | 86 | I | 750+S•525 |
| Branch on Index Low or Equal | RS | BXLE | 87 | I | 750+S•525 |
| Clear I/O | S | CLRIO | 9D01 | | See "I/O Instruction Timing Information." |
| Clear Page | S | CLRP | B215 | | 102750 |
| Compare | RR | CR | 19 | | 375 |
| Compare | RX | C | 59 | | 600 |
| Compare (long) | RR | CDR | 29 | | 450 (for E1=E2) |
| | | | | | 825 (for E1≠E2) |
| Compare (long) | RX | CD | 69 | | 825 (for E1=E2) |
| | | | | | 1200 (for E1≠E2) |
| Compare (short) | RR | CER | 39 | | 450 (for E1=E2) |
| | | | | | 1125 (for E1≠E2) |
| Compare (short) | RX | CE | 79 | | 825 (for E1=E2) |
| | | | | | 1500 (for E1<E2) |
| | | | | | 1350 (for E1>E2) |
| Compare and Swap | RS | CS | BA | | 975 (for OP1≠OP2) |
| | | | | | 1050 (for OP1=OP2) |
| Compare Decimal | SS | CP | F9 | | 1275 (for L1≤8, L2≤8) |
| | | | | | 2025 (for L1≤8, L2>8) |
| | | | | | 2175 (for L1>8, L2≤8) |
| | | | | | 2475 (for L1>8, L2>8) |
| Compare Double and Swap | RS | CDS | BB | | 1650 (for OP1≠OP2) |
| | | | | | 1875 (for OP1=OP2) |
| Compare Halfword | RX | CH | 49 | | 600 |
| Compare Logical | RR | CLR | 15 | | 375 |
| Compare Logical | RX | CL | 55 | | 600 |
| Compare Logical (character) | SS | CLC | D5 | | 975 (for L≤8) |
| | | | | | 600+L8•525-P•75 (for L>8) |
| Compare Logical (immediate) | SI | CLI | 95 | | 600 |
| Compare Logical Characters under Mask | RS | CLM | BD | I | 1059+M•75 |
| Compare Logical Long | RR | CLCL | 0F | II | 675+C256•6750+L8C•675 |
| | | | | | (for C256>0 and F256=0) |
| | | | | | 675+F256•(7650+(L1>0)•300)+L8F•600 |
| | | | | | (for C256=0 and F256>0) |
| | | | | | -2225+F256(7650+(L1>L2)•300)+C256•6750 |
| | | | | | +L8F•600+L8C•675 |
| | | | | | (for C256>0 and F256>0) |
| Connect Page | RS | CTP | B0 | | 5325-C•3075 |
| Convert to Binary | RX | CVB | 4F | | 1350+NDD2•750 |
| Convert to Decimal | RX | CVD | 4E | | 1275•(1+NHD)+K•150 |
| Deconfigure Page | S | DEP | B21B | | 13650 |
| Diagnose | — | — | 83 | | — |
| Disconnect Page | S | DCTP | B21C | | 3375+C•14425 |
| Divide | RR | DR | 1D | | 6525+N2•150+N1•375 |

| *Instruction Name* | *Format* | *Mnemonic* | *Op-Code* | *Accuracy Code* | *Formula and Comments* |
|---|---|---|---|---|---|
| Divide | RX | D | 5D | | 7425+N1•375+N2•150 |
| Divide (long) | RR | DDR | 2D | | 10425+PN•225 |
| Divide (long) | RX | DD | 6D | | 10950+PN•225 |
| Divide (short) | RR | DER | 3D | | 5550+PN•225 |
| Divide (short) | RX | DE | 7D | | 6300+PN•225 |
| Divide Decimal | SS | DP | FD | II | 7350+(L1>8)•1500-(L1=16)•300<br>-(NDD1=0)•150+DWR•225<br>(for NDD1<NDD2)<br>11800+(NDD1-NDD2)•1350<br>(for NDD1≥NDD2 and L1≤8)<br>13300+(1350+LC•150)•(NDD1-NDD2)<br>+(NDD1>15)•825-(L1=16)•300+(DWQ+DWR)•225<br>(for NDD1≥NDD2 and L1>8)<br>**Note:** For cases with NDD1≥NDD2 times assume equal probability of digits 0 through 9. |
| Edit | SS | ED | DE | II | 975+(Cond.Code≠0)•225+Sum(EB+SA)<br>(Where the sum is taken over all pattern characters. Refer Figure 6) |
| Edit and Mark | SS | EDMK | DF | II | 1425+(Cond.Code≠0)•225+Sum(EB+SA+EMK)<br>(Where the sum is taken over all pattern characters. Refer Figure 6) |
| Exclusive OR | RR | XR | 17 | | 375 |
| Exclusive OR | RX | X | 57 | | 600 |
| Exclusive OR (character) | SS | XC | D7 | | 1275 (for L≤8)<br>1200+L8•825+LZ8•75 (for L>8)<br>900+L•825+LZ•75 (for operands overlap)<br>1350+L8•225 [for L>8 and ADDR(OP1)=ADDR(OP2)] |
| Exclusive OR (immediate) | SI | XI | 97 | | 825 |
| Execute | RX | EX | 44 | | 1125+SI+R•3300 (for R1=0)<br>1425+SI+R•3300 (for R1≠0) |
| Halt Device | S | HDV | 9E01 | | See "I/O Instruction Timing Information." |
| Halt I/O | S | HIO | 9E00 | | See "I/O Instruction Timing Information." |
| Halve (long) | RR | HDR | 24 | | 1125+PN•225 |
| Halve (short) | RR | HER | 34 | | 975+PN•225 |
| Insert Character | RX | IC | 43 | | 375 |
| Insert Characters under Mask | RS | ICM | BF | I | 1125 |
| Insert Page Bits | RS | IPB | B4 | | 2250+C•525 |
| Insert PSW Key | S | IPK | B20B | | 1350 |
| Insert Storage Key | RR | ISK | 09 | | 1425 (for BC, S/370 mode)<br>1575 (for EC, S/370 mode)<br>1725 (for BC, ECPS:VSE mode)<br>2475 (for EC, ECPS:VSE mode) |
| Invalidate Page Table Entry | S | IPTE | B221 | | 6075 (2K Page Size)<br>6375 (4K Page Size) |
| Load | RR | LR | 18 | | 300 |
| Load | RX | L | 58 | | 375 |
| Load (long) | RR | LDR | 28 | | 300 |
| Load (long) | RX | LD | 68 | | 375 |
| Load (short) | RR | LER | 38 | | 300 |
| Load (short) | RX | LE | 78 | | 375 |

| *Instruction Name* | *Format* | *Mnemonic* | *Op-Code* | *Accuracy Code* | *Formula and Comments* |
|---|---|---|---|---|---|
| Load Address | RX | LA | 41 | | 300 |
| Load and Complement (long) | RR | LCDR | 23 | | 675 |
| Load and Test | RR | LTR | 12 | | 375 |
| Load and Test (long) | RR | LTDR | 22 | | 525 |
| Load and Test (short) | RR | LTER | 32 | | 525 |
| Load Complement | RR | LCR | 13 | | 375 |
| Load Complement (short) | RR | LCER | 33 | | 675 |
| Load Control | RS | LCTL | B7 | | 12750+PU•5400 (for S/370 mode, load all Regs) |
| | | | | | 12000 (for ECPS:VSE, load all Regs) |
| | | | | | 5025+PU•5400 (for S/370 mode, load Regs 0,1) |
| | | | | | 3825 (for ECPS:VSE, load Regs 0,1) |
| Load Frame Index | RS | LFI | B8 | | 2175 |
| Load Halfword | RX | LH | 48 | | 375 |
| Load Multiple | RS | LM | 98 | | 150+N•225 |
| Load Negative | RR | LNR | 11 | | 525-N2•150 |
| Load Negative (long) | RR | LNDR | 21 | | 525 |
| Load Negative (short) | RR | LNER | 31 | | 675 |
| Load Positive | RR | LPR | 10 | | 375+N2•225 |
| Load Positive (long) | RR | LPDR | 20 | | 675 |
| Load Positive (short) | RR | LPER | 30 | | 675 |
| Load PSW | S | LPSW | 82 | | 5250 (for BC/BC) |
| | | | | | 5550 (for EC/BC) |
| | | | | | 6075 (for BC-EC/EC) |
| Load Real Address | RX | LRA | B1 | | 4800 (for 1M segment) |
| | | | | | 5100 (for 64K segment) |
| Load Rounded (extended to long) | RR | LRDR | 25 | | 750 |
| Load Rounded (long to short) | RR | LRER | 35 | | 900 |
| Make Addressable | S | MAD | B21D | | 3075-A•150 |
| Make Unaddressable | S | MUN | B21E | | 2925+A•450 |
| Monitor Call | SI | MC | AF | | 4200 |
| | | | | | 1200 (for NO-OP case) |
| Move (character) | SS | MVC | D2 | | 825 (for L≤8) |
| | | | | | 675+L8•450 (for L>8) |
| | | | | | 900+L•450 (for L≤8 and operands overlap) |
| | | | | | 750+L•450 (for L>8 and operands overlap) |
| Move (immediate) | SI | MVI | 92 | | 375 |
| Move Inverse | SS | MVCIN | E8 | | 750+L•750 |
| Move Long | RR | MVCL | 0E | II | 375+M256•6863+P256•7688-MEOB•5738 +L8M•375 |
| | | | | | +L8P•225 |
| | | | | | (for M256>0 and P256>0) |
| | | | | | 375+M256•6863+MEOB•150+L8M•375 |
| | | | | | (for M256>0 and P256=0) |
| | | | | | -600+P256•7688+L8P•225 |
| | | | | | (for M256=0 and P256>0) |
| Move Numerics | SS | MVN | D1 | | 1800 (for L≤8) |
| | | | | | (L8+1)•1125 (for L>8) |
| | | | | | 825+L•1125 (for L≤8 and operands overlap) |
| | | | | | 825+L•1125 (for L>8 and operands overlap) |

| *Instruction Name* | *Format* | *Mnemonic* | *Op-Code* | *Accuracy Code* | *Formula and Comments* |
|---|---|---|---|---|---|
| Move with Offset | SS | MVO | F1 | | 2400+(A2<A1+L1)•375<br>(for L1≤8,L2≤8)<br>2850+(A2<A1+L1)•375<br>(for L1≤8,L2>8)<br>3600+(A2<A1+L1)•375<br>(for L1>8,L2≤8)<br>3900+(A2<A1+L1)•375<br>(for L1>8,L2>8)<br>3900+min(L1,L2)•1050+(L1>L2)•525+<br>[(L1>L2+8)+(L1>8)+(L2>8)]•225 (for overlapping case) |
| Move Zones | SS | MVZ | D3 | | 1800 (for L≤8)<br>(L8+1)•1125 (for L>8)<br>825+L•1125 (for operands overlap) |
| Multiply | RR | MR | 1C | | 3600+N2•450<br>1050 (for VP=0) |
| Multiply | RX | M | 5C | | 3900+N2•450 |
| Multiply (extended) | RR | MXR | 26 | | 15675+PN•75 |
| Multiply (long to extended) | RR | MXDR | 27 | | 5850+PN•75 |
| Multiply (long to extended) | RX | MXD | 67 | | 6375+PN•75 |
| Multiply (short to long) | RR | MER | 3C | | 3825+PN•225 |
| Multiply (short to long) | RX | ME | 7C | | 4350+PN•225 |
| Multiply (long) | RR | MDR | 2C | | 4875+PN•225 |
| Multiply (long) | RX | MD | 6C | | 5400+PN•225 |
| Multiply Decimal | SS | MP | FC | | 4875+(L1>8)•375-(NDD2=0)•150<br>(for NDD1=0)<br>5700<br>(for NDD1>15 and NDD2=0)<br>5100+(L1>8)•825-CLZ•525<br>(for NDD1≤15 and NDD2=0)<br>8175+NDD2•150+(L1>8)•675-CLZ•525<br>(for NDD1<15 and NDD2>0)<br>11625+(L1>8)•675-CLZ•525<br>(for NDD1=15 and NDD2<15)<br>18600-CLZ•525<br>(for NDD1=NDD2=15)<br>14275+300•NDD2<br>(for NDD1>15 and NDD2>0)<br>6150+VP•600<br>(for NDD1=29 and NDD2=1) |
| Multiply Halfword | RX | MH | 4C | | 3075+N2•150 |
| OR | RR | OR | 16 | | 375 |
| OR | RX | O | 56 | | 600 |
| OR (character) | SS | OC | D6 | | 1275 (for L≤8)<br>900+L8•825+LZ8•75 (for L>8)<br>900+L•825+LZ•75 (for operands overlap) |
| OR (immediate) | SI | OI | 96 | | 825 |
| Pack | SS | PACK | F2 | | 1725 (for L1≤8, L2≤8)<br>2100 (for L1>8, L2≤8)<br>2400 (for L1≤8, L2>8)<br>3000 (for L1>8, L2>8) |
| Purge TLB | S | PTLB | B20D | | 6750 |

| Instruction Name | Format | Mnemonic | Op-Code | Accuracy Code | Formula and Comments |
|---|---|---|---|---|---|
| Reset Reference Bit | S | RRB | B213 | | 3225+C•150 (for ECPS:VSE mode)<br>1800 (for S/370 mode) |
| Retrieve Status and Page | SS | RSP | D8 | | 133425 |
| Set Clock | S | SCK | B204 | | 7650 (for Enable ON)<br>1950 (for Enable OFF) |
| Set Clock Comparator | S | SCKC | B206 | | 5325 |
| Set CPU Timer | S | SPT | B208 | | 11175 |
| Set Page Bits | RS | SPB | B5 | | 3675 |
| Set Program Mask | RR | SPM | 04 | | 750 |
| Set PSW Key from Address | S | SPKA | B20A | | 2325 |
| Set Storage Key | RR | SSK | 08 | | 7650 (for S/370 mode)<br>4725 (for ECPS:VSE mode) |
| Set System Mask | S | SSM | 80 | | 1725 (for BC; S/370 mode or ECPS:VSE mode)<br>5475 (for EC; ECPS:VSE mode)<br>5850 (for EC; S/370 mode) |
| Shift and Round Decimal | SS | SRP | F0 | | 3600-ZR•225 (for L≤8, shift left and amount<16)<br>3300-ZR•150 (for L≤8, shift right and amount<16)<br>2400 (for L≤8, shift left and amount≥16)<br>2175 (for L≤8, shift right and amount>16)<br>2400 (for L≤8, shift right and amount=16)<br>5850-ZR•150 (for L>8, shift left)<br>5175-ZR•150 (for L>8, shift right and amount<16)<br>4875-ZR•150 (for L>8, shift right and amount=16)<br>5025-ZR•150 (for L>8, shift right and 16<amount<32)<br>4725-ZR•150 (for L>8, shift right and amount=32) |
| Shift Left Double | RS | SLDA | 8F | | 1500+N1•150 |
| Shift Left Double Logical | RS | SLDL | 8D | | 1200 |
| Shift Left Single | RS | SLA | 8B | | 1050+N1•150 |
| Shift Left Single Logical | RS | SLL | 89 | | 600 |
| Shift Right Double | RS | SRDA | 8E | | 1275 |
| Shift Right Double Logical | RS | SRDL | 8C | | 1200 |
| Shift Right Single | RS | SRA | 8A | | 825 |
| Shift Right Single Logical | RS | SRL | 88 | | 600 |
| Start I/O | S | SIO | 9C00 | | See "I/O Instruction Timing Information." |
| Start I/O Fast Release | S | SIOF | 9C01 | | See "I/O Instruction Timing Information." |
| Store | RX | ST | 50 | | 375 |
| Store (long) | RX | STD | 60 | | 375 |
| Store (short) | RX | STE | 70 | | 375 |
| Store Capacity Counts | S | STCAP | B21F | | 2025 |
| Store Channel ID | S | STIDC | B203 | | See "I/O Instruction Timing Information." |
| Store Character | RX | STC | 42 | | 375 |
| Store Characters Under Mask | RS | STCM | BE | I | 909 |
| Store Clock | S | STCK | B205 | | 2175 |
| Store Clock Comparator | S | STCKC | B207 | | 1575 |
| Store Control | RS | STCTL | B6 | | 900+[ORS+!(N-ORS)/2]•450<br>+[floor of((N-ORS)/2)]•RSA•225 |
| Store CPU ID | S | STIDP | B202 | | 1500 |
| Store CPU Timer | S | STPT | B209 | | 2550 |
| Store Halfword | RX | STH | 40 | | 375 |
| Store Multiple | RS | STM | 90 | | 150+N•225 |

| *Instruction Name* | *Format* | *Mnemonic* | *Op-Code* | *Accuracy Code* | *Formula and Comments* |
|---|---|---|---|---|---|
| Store then AND System Mask | SI | STNSM | AC | | 1650 (for BC; S/370 mode or ECPS:VSE mode)<br>5400 (for EC; ECPS:VSE mode)<br>5550 (for EC; S/370 mode) |
| Store then OR System Mask | SI | STOSM | AD | | 1650 (for BC; S/370 mode or ECPS:VSE mode)<br>5400 (for EC; ECPS:VSE mode)<br>5550 (for EC; S/370 mode) |
| Subtract | RR | SR | 1B | | 375 |
| Subtract | RX | S | 5B | | 600 |
| Subtract Decimal | SS | SP | FB | | 1275+RC•1125+ZR•1050<br>(for L1≤8 and L2≤8)<br>1950+RC•1275+ZR•1050<br>(for L1≤8 and L2>8)<br>2625+RC•1275+ZR•1050<br>(for L1>8 and L2≤8)<br>2700+RC•1275+ZR•1050<br>(for L1>8 and L2>8) |
| Subtract Halfword | RX | SH | 4B | | 600 |
| Subtract Logical | RR | SLR | 1F | | 375 |
| Subtract Logical | RX | SL | 5F | | 600 |
| Subtract Normalized (extended) | RR | SXR | 37 | I | 3834 |
| Subtract Normalized (long) | RR | SDR | 2B | I | 1050 |
| Subtract Normalized (long) | RX | SD | 6B | I | 1425 |
| Subtract Normalized (short) | RR | SER | 3B | I | 1134 |
| Subtract Normalized (short) | RX | SE | 7B | I | 1472 |
| Subtract Unnormalized (long) | RR | SWR | 2F | I | 986 |
| Subtract Unnormalized (long) | RX | SW | 6F | I | 1511 |
| Subtract Unnormalized (short) | RR | SUR | 3F | I | 1166 |
| Subtract Unnormalized (short) | RX | SU | 7F | I | 1689 |
| Supervisor Call | RR | SVC | 0A | I | 6075 (for BC/BC)<br>6675 (for EC/BC)<br>6787 (for BC-EC/EC) |
| Test and Set | S | TS | 93 | | 1125 |
| Test Channel | S | TCH | 9F00 | | See "I/O Instruction Timing Information." |
| Test I/O | S | TIO | 9D00 | | See "I/O Instruction Timing Information." |
| Test Protect | SS | TPRT | E501 | | 8400 Condition Code 0, 1Meg Seg.<br>(add 300 ns for 64K Seg.)<br>9000 Condition Code 1, 1Meg Seg.<br>(add 300 ns for 64K Seg.)<br>9000 Condition Code 2, 1Meg Seg.<br>(add 300 ns for 64K Seg.)<br>8400 Condition Code 3, 1Meg Seg.<br>(add 300 ns for 64K Seg.) |
| Test under Mask | SI | TM | 91 | | 450 |
| Translate | SS | TR | DC | | 600+L•975 |
| Translate and Test | SS | TRT | DD | | 600+NP•975+CCV•150 |
| Unpack | SS | UNPK | F3 | | 2175 (for L1≤8, L2≤8)<br>2700 (for L1>8, L2≤8)<br>2550 (for L1≤8, L2>8)<br>3225 (for L1>8, L2>8) |

| Instruction Name | Format | Mnemonic | Op-Code | Accuracy Code | Formula and Comments |
|---|---|---|---|---|---|
| Zero and Add | SS | ZAP | F8 | | 2475+RC•1125+ZR•1050 +(A2<A1+L1)•375 (for L1≤8 and L2≤8)<br>3150+RC•1275+ZR•1050 +(A2<A1+L1)•375 (for L1≤8 and L2>8)<br>3150+RC•1275+ZR•1050 +(A2<A1+L1)•375 (for L1>8 and L2≤8)<br>3225+RC•1275+ZR•1050 +(A2<A1+L1)•375 (for L1>8 and L2>8) |

## *Legend for Timing Formulas*

A = 1 if block is addressable; otherwise 0.
A1 = address of operand 1.
A2 = address of operand 2.
C = 1 if block is connected; otherwise 0.
CCV = 0 if condition code (CC) is 0; 5 if CC is 1; 6 if CC is 2.
CEOB = 1 if C256>0 and that portion of the longer operand that is compared to the shorter operand compares equal and the right end of the last longer operand doubleword thus compared is not on a 256-byte boundary. If operands have equal length, this refers to operand 1. Otherwise CEOB =0.
CLZ = 1 if multiplicand has 8 bytes or more of leading zeros; otherwise 0.
C256 = number of 256-byte blocks, on 256-byte boundaries, spanned by that portion of the longer operand that is compared to the shorter operand, extending through the first doubleword, if any, that compares unequal. If operands have equal length, this refers to operand 1 alignment.
DWQ = 1 if the quotient crosses a doubleword boundary; otherwise 0.
DWR = 1 if the remainder crosses a doubleword boundary; otherwise 0.
EB = ED, EDMK base value. Refer Figure 6.
EMK = EDMK adjustment. Refer Figure 6.
E1 = exponent corresponding to operand 1.
E2 = exponent corresponding to operand 2.
FEOB = 1 if (F256>0) and (CC=0) and the right end of the last longer operand doubleword is not on a 256-byte boundary. Otherwise FEOB=0.
F256 = number of 256-byte blocks, on 256-byte boundaries, spanned by that portion of the longer operand that is compared to the pad character, extending through the first doubleword, if any, that compares unequal.
K = number of hex digits with value greater than 9.
L = length of the operand in bytes.
LC = 0 if NDD1 ≤ 15
LC = 1 if NDD1 > 15 and NDD1-NDD2 > 14
LC = 2 if NDD1 > 15 and NDD1-NDD2 ≤ 14
LZ = number of contiguous zero result bytes starting from the beginning of the result.
LZ8 = number of contiguous zero result doublewords starting from the beginning of the result.
L1 = length of operand 1 in bytes.
L2 = length of operand 2 in bytes.
L8 = number of operand 1 doublewords spanned by processing.
L8C = number of doublewords in the longer operand that is compared to the shorter operand. If operands have equal length, this refers to operand 1.
L8F = number of doublewords in the longer operand that is compared to the pad character.
L8M = number of doublewords spanned by move in operand 1.
L8P = number of doublewords spanned by pad in operand 1.
M = 0 if all mask bits selected are 0; otherwise 1.
MEOB = 1 if move ends on other than a 256-byte boundary in operand 1; otherwise 0.
M256 = number of 256-byte blocks, on 256-byte boundaries, spanned by move in operand 1.
N = number of registers in LM, STM.
N1 = 1 if operand 1 is negative; otherwise 0.
N2 = 1 if operand 2 is negative; otherwise 0.
NDD1 = number of significant decimal digits in operand 1.
NDD2 = number of significant decimal digits in operand 2.
NHD = number of significant hex digits.
NP = number of bytes processed.
ORS = 1 if starting register number is odd, otherwise 0.
P = 0 if processing halts before the last doubleword is reached; 1 if the last doubleword is processed.
PN = 1 if post normalization is required; otherwise 0.
PU = 1 if translation lookaside buffer purge is required; otherwise 0.
P256 = number of 256-byte blocks, on 256-byte boundaries, spanned by the pad in operand 1.
R = 1 if returned to the instruction following the execute instruction after completing the subject instruction; otherwise 0.
RC = 1 if recomplementation is required; otherwise 0.
RMN = 1 if remainder is negative; otherwise 0.

RSA = 1 if starting register number is even and operand 2 is off doubleword boundary or if starting register number is odd and operand 2 is on a doubleword boundary; otherwise 0.
S = 1 if successful branch; otherwise 0.
SA = sign adjustment. Refer Figure 6.
SI = time to execute the subject instruction.
VP = value of the operand 2.
X = 1 if index register number is not zero; otherwise 0.
ZR = 1 if result is zero; otherwise 0.
• = multiply.
! = ceiling function.
( ) = 1 if the logical condition within ( ) is satisfied; otherwise 0.

Use Figure 6 to determine the processing time for each pattern character occurring in ED and EDMK instructions. For each such pattern character, determine the EB value and add it to the instruction time. If the pattern character is a digit selector or a significance starter, and if the source digit is the lowest-order digit in its field, add in also the sign adjustment (SA). If the instruction is EDMK and a nonzero source digit is encountered with the significance indicator off, add the EMK adjustment to the instruction time.

## *High-Speed Buffer Storage and TLB Miss Service Times*

These timings (in microseconds) are added to the instruction execution time for each miss in the high-speed buffer storage.

| | |
|---|---|
| 2.36 μs | High-speed buffer storage miss where page to be replaced has not been altered. |
| 3.75 to 6.45 μs | High-speed buffer storage miss where page to be replaced has been altered (castout case). |

For typical workloads, the average high-speed buffer storage miss time is about 2.85 microseconds. The frequency depends on the addressing pattern of the program being executed.

For each miss in the Translation Lookaside Buffer (TLB), these times are added:

| | |
|---|---|
| 1.43 μs | TLB miss for S/370 mode, BC mode or EC DAT off. |
| 1.43 μs | TLB miss for ECPS:VSE mode. |
| 5.80 μs | TLB miss for S/370 mode, EC mode DAT on. |
| 0.15 μs | Add for TLB miss if S/370 mode with DAT on if 64K segment. |

| *Pattern Character Type* | *Significance Indicator* | *Source Digit* | *EB Value* | *SA - Sign Adjustment Add if digit is the last before:* | | | *EMK Adjustment* |
|---|---|---|---|---|---|---|---|
| | | | | *Sign B* | *Sign D* | *+Sign* | *add if EDMK* |
| Digit Selector | Off | 0 | 1838 | 487 | 487 | 487 | 0 |
| | Off | 1-9 | 2138 | 712 | 937 | 937 | 300 |
| | On | 0 | 1838 | 712 | 937 | 1087 | 0 |
| | On | 1-9 | 1988 | 712 | 937 | 1087 | 0 |
| Significance Starter | Off | 0 | 2513 | 712 | 937 | 782 | 0 |
| | Off | 1-9 | 2663 | 712 | 937 | 937 | 300 |
| | On | 0 | 2288 | 637 | 862 | 1012 | 0 |
| | On | 1-9 | 2438 | 637 | 862 | 1012 | 0 |
| | | *First Byte of Pattern* | | | | | |
| Field Separator | | Yes | 900 | | | | |
| | | No | 1275 | | | | |
| Message Char. | Off | Yes | 900 | | | | |
| | Off | No | 1275 | | | | |
| | On | --- | 1050 | | | | |

**FIgure 6. ED and EDMK Pattern Character Timings**

These times assume that the necessary translation table entries are found in the high-speed buffer storage. The TLB miss frequency depends on the addressing pattern of the program being executed. Values outside the ranges given are possible.

**Performance Degradation of PER Mask Setting**

With bit 1 of the PSW, EC mode turned on, and the PER mask nonzero, the performance degradation (time in addition to the normal time) is:

110 percent with no masked event selected
242 percent with successful branch event selected only
337 percent with instruction fetch event selected only
391 percent with storage alteration event selected only
362 percent with general register alteration event selected only.

The accumulative degradation with more than one event selected is not an addition of the above figures.

## *Effect of Hardware-Assist Features on Performance*

The ECPS:VM/370 Assist and ECPS:VS1 Assist facilities simulate certain frequently used functions in hardware. The effect that these have on performance depends on the workload being executed and the frequency with which it requests services that are assisted.

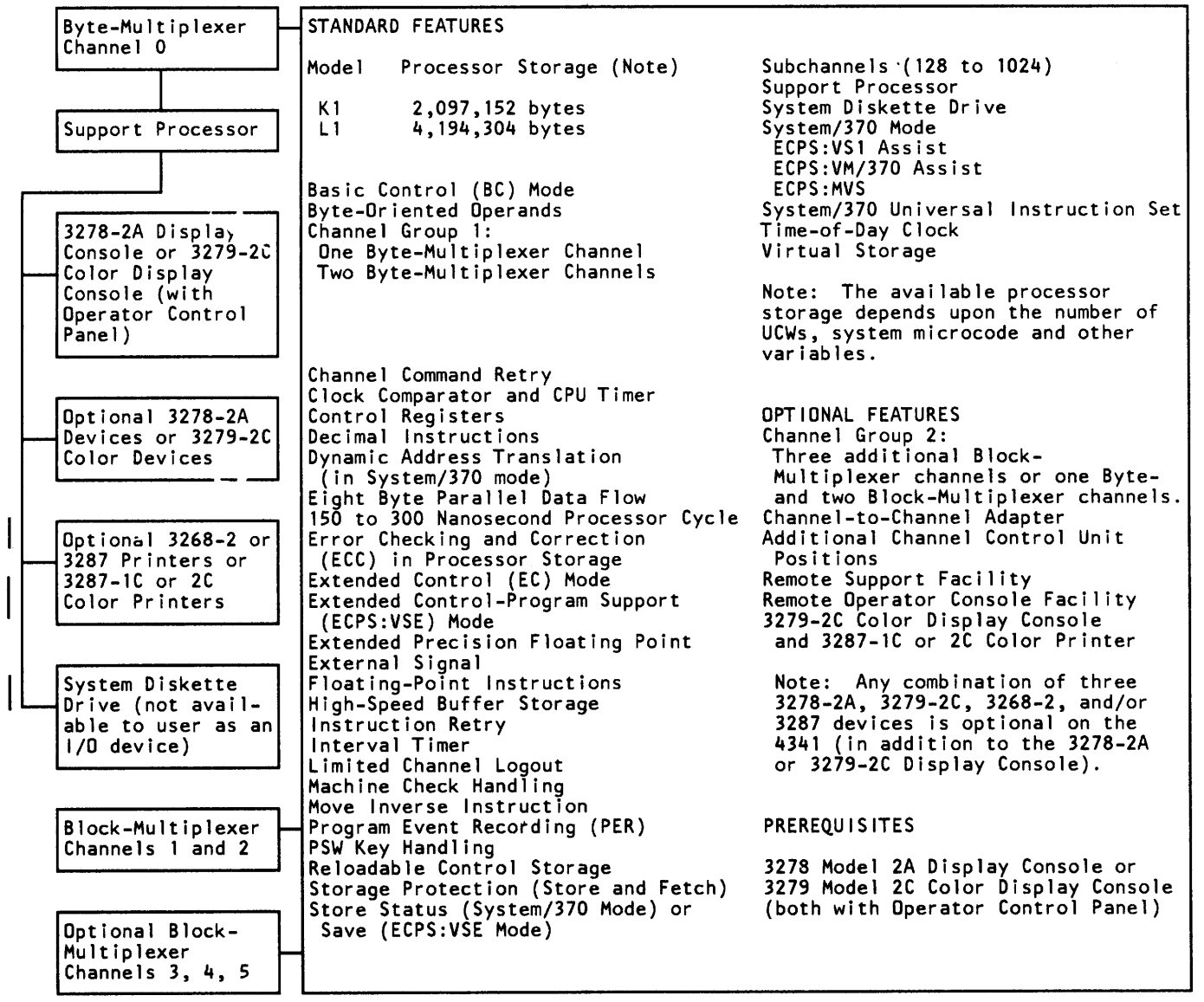
As an approximate indication of magnitude, the following are given: ECPS:VM/370 Assist reduces the VM/370 hypervision overhead by about 83 percent of its value without the assist when running VS/1 under VM/370 with the batch jobstream PACE.

When running CMS alone under VM/370 with ECPS:VM/370 Assist, the hypervision overhead is reduced by approximately 35 percent of its value without the assist.

ECPS:VS1 Assist reduces the supervisor state time for VS/1 running the PACE jobstream by about 14 percent.

ECPS:VM/370 Assist and ECPS:VS1 Assist are mutually exclusive facilities. Also, ECPS:VM/370 Assist and ECPS:MVS are mutually exclusive facilities.

# 4341 Processor Model Group 1 Complex Configurator



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International Business Machines Corporation
Data Processing Division
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IBM World Trade Americas/Far East Corporation
Town of Mount Pleasant, Route 9, North Tarrytown, N. Y., U. S. A. 10591

IBM World Trade Europe/Middle East/Africa Corporation
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