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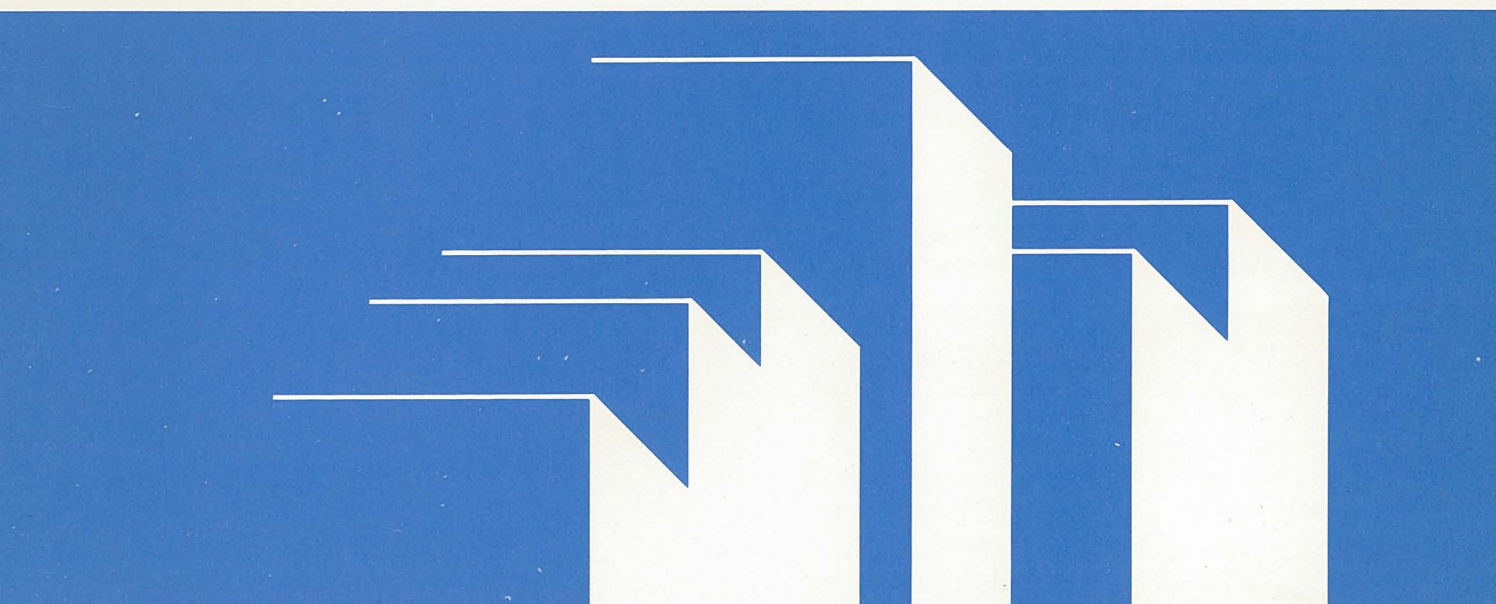
IBM 3084

Functional Characteristics



IBM 3084

Functional Characteristics

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Fifth Edition (February 1986)

This major revision obsoletes GA22-7088-3. This edition includes changes to the following information about the IBM 3084 Processor Complex:

- Programming support
- Features available
- Operation of the features in System/370 (S/370) or System/370 extended architecture (370-XA) mode
- Glossary of terms and abbreviations
- Bibliography

Changes or additions to the text and illustrations are indicated by a vertical line to the left of the change.

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Preface

This manual, which is intended for management, programming, and operations personnel, describes the components and functions of the IBM 3084 Processor Complex base model (Q) and improved model (QX).

Readers of this manual should:

- Be familiar with System/370 architecture as defined in the *IBM System/370 Principles of Operation,* GA22-7000, and the *IBM System/370 Extended Architecture Principles of Operation,* SA22-7085.
- Have a knowledge of virtual-storage and virtual-machine concepts. Other manuals that should be used in addition to this manual are listed in the "Bibliography."

This manual contains the following five chapters and one appendix:

Chapter 1 introduces and summarizes the IBM 3084 Processor Complex.

Chapter 2 describes the structure and implementation of the 3084 Processor Complex.

Chapter 3 describes the functions of the IBM 3084 Processor Unit components.

Chapter 4 describes the IBM 3082 Processor Controller Models Q48 and X48.

Chapter 5 describes the standard and optional features.

Appendix A contains deviations from the *IBM System/370 Principles of Operation,* GA22-7000, the *IBM System/370 Extended Architecture Principles of Operation,* SA22-7085, and the *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information,* GA22-6974.

This manual also contains a glossary of terms and abbreviations and a bibliography.

In this manual, all references to the IBM 3084 Processor Complex, the IBM 3084 Processor Unit, and the IBM 3082 Processor Controller apply to both the base model and the improved model, unless indicated otherwise.

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Chapter 1. Introduction

The IBM 3084 Processor Complex (Figure 1-1) is a four-way multiprocessor that provides twice the hardware resources of an IBM 3081 Processor Complex.

Design Highlights

The design of this high-performance processor complex incorporates:

- Two physical modes of operation
- System/370 extended architecture
- Two architectural modes of operation
- External data controllers
- Thermal conduction modules

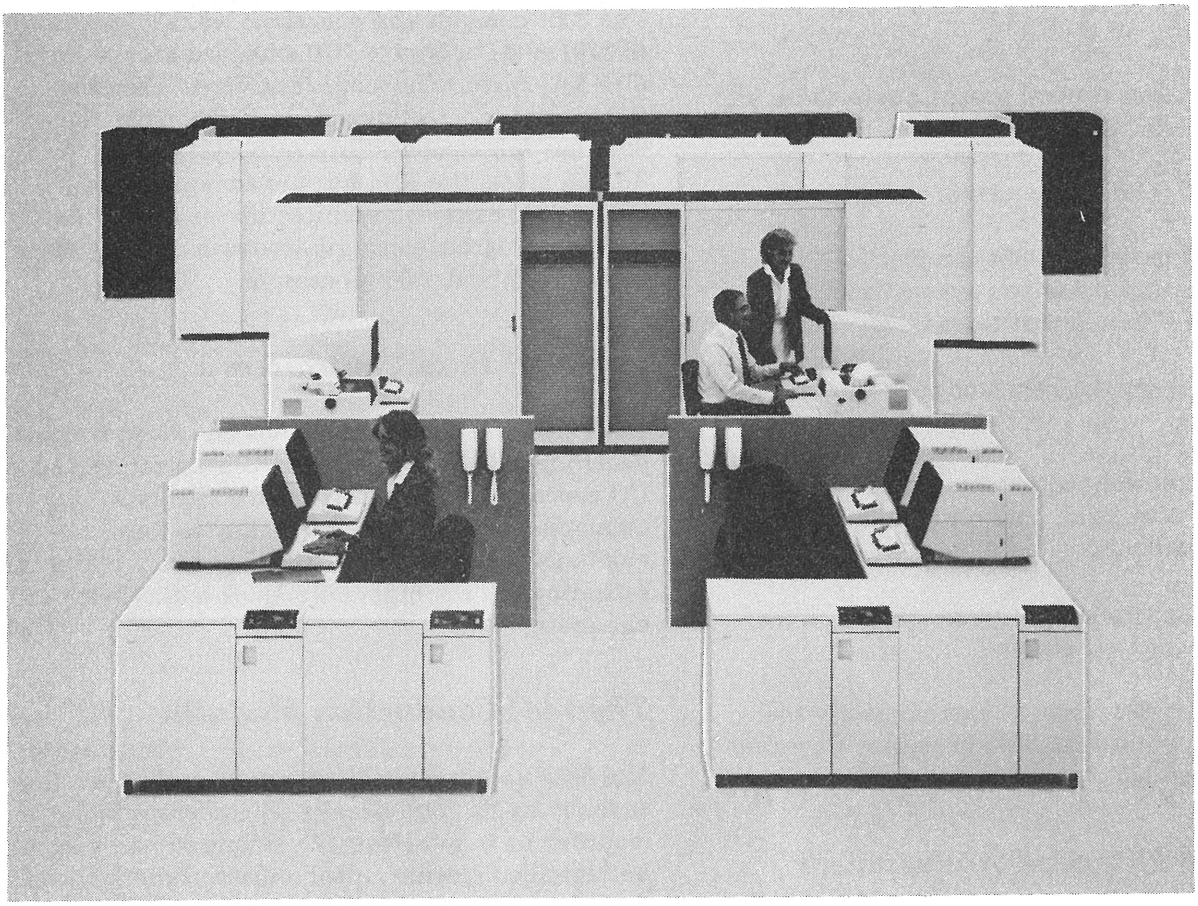


Figure 1-1. IBM 3084 Processor Complex, with Other Devices (Design Models)

Two Physical Modes of Operation

The 3084 complex has two physical modes of operation: single-image (single-system) mode and partitioned mode. In single-image mode, the 3084 complex:

- Operates as a single system under a single control program
- Makes its maximum hardware resources available. Most prominent among them are:
  - Four central processors
  - 48 channels
  - 32M, 48M, 64M, 96M, or 128M bytes of central storage (1M byte equals 1,048,576 bytes)
- Allows all four central processors to share all of central storage
- Generally permits concurrent maintenance

In partitioned mode, the 3084 complex is partitioned so that it has two symmetric sides (A and B). Each side of a partitioned 3084 complex:

- Operates independently, under its own control program
- Provides two central processors; 24 channels; and 16M, 24M, 32M, 48M, or 64M bytes of central storage
- Permits the two central processors to share that side's central storage
- Executes instructions at approximately the same rate as an IBM 3081 Processor Complex Model K or KX.

System/370 Extended Architecture (370-XA)

An evolutionary extension of System/370 architecture, 370-XA adds a number of functional enhancements. For example:

- It permits 31-bit addressing, yet allows users to continue running System/370 problem programs, which use 24-bit addresses.
- It makes channel-path selection and I/O-busy-condition management a hardware function rather than a control-program function.
- It makes as many as four channel paths available to each I/O device.
- It increases I/O-device accessibility by allowing any of the central processors to initiate operations with any of the devices and to handle any I/O interruptions.

Two Architectural Modes of Operation

The 3084 complex can operate in either System/370 (S/370) mode or System/370 extended architecture (370-XA) mode. The mode is selected when the 3084 complex is initialized. In S/370 mode, the 3084 has full compatibility with System/370. In 370-XA mode, the 3084 has the advantages of System/370 extended architecture and has problem-program compatibility with System/360, System/370, and 4300 processors.

External Data Controllers

Each side of a 3084 complex has an external data controller (EXDC). Each EXDC is an integrated I/O processor that contains and controls 24 channels. In each EXDC, as many as four channels can be configured for byte-multiplexer operation; all the others are block-multiplexer channels.

Thermal Conduction Modules

The 3084 uses large-scale integration that permits as many as 133 high-density silicon chips to be mounted on a multilayered ceramic substrate in a helium-filled module called a *thermal conduction module* (TCM). TCMs plug into a supporting multilayered circuit board. The use of TCMs and the boards, which are designed to eliminate module-to-module external wiring, significantly reduces requirements for power, space, cabling, and cooling, while enhancing reliability.

Other Highlights

The basic machine cycle time (24 nanoseconds in Model QX, 24.5 nanoseconds in Model Q with the optional performance feature installed, and 26 nanoseconds in Model Q without the optional performance feature installed) and having four central processors for instruction execution permit the 3084 to achieve a high level of internal performance.

Other significant characteristics and features include:

- A stand-alone support processor that monitors and supervises the entire processor complex
- Dedicated service support consoles, which facilitate maintenance operations and provide backup for the system consoles
- The System/370 extended facility, 3033 extension, extended addressing, virtual machine assist, and preferred machine assist, which are all standard features of a 3084 operating in S/370 mode

The 3084 complex may operate as either a stand-alone configuration or loosely coupled with other IBM processors (including System/360, System/370, 30xx, and 4300).

A single-image 3084 complex operates in 370-XA mode only. In addition, operation in 370-XA mode permits any of the central processors to initiate an operation with any attached I/O device without regard to which channel or EXDC the device is attached.

Many of the preceding characteristics and features, as well as a number of others, are described in more detail in the following chapters.

Programming Support

Programming support is mode dependent. For example, to operate in 370-XA mode, a 3084 complex requires a 370-XA-mode control program.

A single-image 3084 complex operates in 370-XA mode only and is supported by MVS/SP Version 2.

Programming support for each side of a partitioned 3084 complex includes:

Control Programs	In S/370 Mode	In 370-XA Mode
MVS/SP Version 1 Release 1 Enhancement	All models	-
MVS/SP Version 2	-	All models
VM/SP with VM/SP High Performance Option (VM/SP-HPO) Release 3	All models	-
VM/XA Migration Aid	-	All models
VM/XA Systems Facility	-	All models

Most existing S/370-mode application (problem) programs can operate without alteration under 370-XA mode control programs. This ability is primarily due to:

- The System/370 unprivileged instructions being a subset of the 370-XA instruction set
- Addressing in 370-XA mode providing for use of either 24-bit or 31-bit addresses, as determined by the control program

Only one license is required for IBM licensed programs used with the 3084 complex, as opposed to the two licenses required for such programs used with earlier IBM multiprocessors.

Compatibility

Any program written to run in 370-XA mode or S/370 mode can run on a 3084 operating in that mode, if the program:

- Is not time dependent.
- Does not depend on system facilities (such as storage capacity, I/O equipment, or optional features) being present when the facilities are not included in the 3084 configuration.
- Does not depend on system facilities being absent when the facilities are included in the 3084 configuration. For example, the program must not depend on interruptions caused by

invalid operation codes for instructions that are not on some models but are present on the 3084.

- Does not depend on results or functions that are defined in the appropriate principles-of-operation manual as being unpredictable or model dependent, or as affecting compatibility.

- Does not depend on results or functions that are defined in this manual as being deviations from the appropriate principles-of-operation manual. (See Appendix A for descriptions of the deviations.)

Any 3084 operating in 370-XA mode can run any problem program written for System/360, System/370 (including the 3031, 3032, and 3033 processors), or 4300 processors if the program:

- Does not violate the first four of the preceding conditions

- Does not depend on control-program facilities that are not available on the 3084

In S/370 mode, two functions of a partitioned 3084 complex differ somewhat from those of some earlier IBM processors:

- In dynamic address translation, the 3084 uses only 64K-byte segments and 4K-byte pages, not 1M-byte segments or 2K-byte pages.

  Note: An S/370-mode interpretively executed guest virtual machine can use 1M-byte segments. See Chapter 5 for additional information.

- In key-controlled storage protection, the 3084 uses only 4K-byte storage keys, not 2K-byte storage keys.

For more details about compatibility, see the appropriate principles-of-operation manual.

Chapter 2. 3084 Structure and Implementation

Each 3084 Processor Complex (Figure 2-1) has:

- One IBM 3084 Processor Unit
- One IBM 3082 Processor Controller Model Q48 or X48
- Two IBM 3087 Coolant Distribution Units Model 1 or 2
- Two IBM 3089 Power Units or other appropriate sources of 400-Hz power
- Two IBM 3278 Display Consoles Model 2A (as system consoles)

Additional console devices are required (as operator consoles) to communicate with the control program.

Other requirements for full operation and maintenance include:

- Customer-supplied telephones to provide data links to remote support locations.
- Access to an appropriate model of an IBM 3274 Control Unit attached by a channel to each side of the 3084 Processor Unit so that IBM service personnel, using an integrated service support console of the processor controller, can run error-isolation or maintenance programs concurrent with ongoing operations.

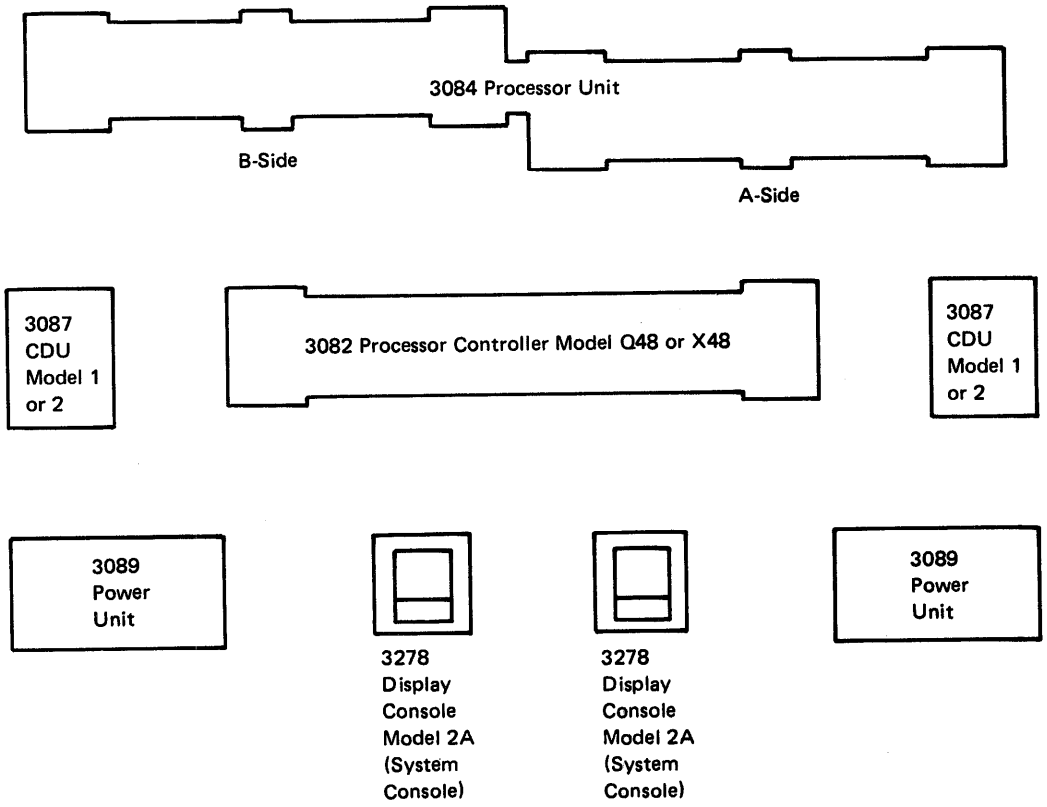


Figure 2-1. IBM 3084 Processor Complex Plan View

Each 3084 complex should also include:

- One or two printers for hard-copy output
- Access to a card reader
- Access to supporting direct-access storage devices or magnetic tape units

The 3084 must use IBM programs (or equivalents) that provide system error recording to handle machine-check interruptions and the recording of detailed system status when a failure is detected.

IBM's ability to provide service may be affected if configurations do not meet the preceding requirements. Therefore, the availability of the 3084 complex may be affected.

Upgrading

At a customer's location, a 3081 Processor Complex Model K or KX can be upgraded to a 3084 Processor Complex Model Q or QX, respectively, as follows:

- For a 3084 Processor Complex Model Q, upgrade an IBM 3081 Processor Unit Model K to an IBM 3084 Processor Unit Model Q, and an IBM 3082 Processor Controller Model 16 or 24 to a 3082 Model Q48.
- For a 3084 Processor Complex Model QX, upgrade an IBM 3081 Processor Unit Model KX to an IBM 3084 Processor Unit Model QX, and an IBM 3082 Processor Controller Model X16 or X24 to a 3082 Model X48.

In addition, a 3084 complex requires a second set of the other units of a 3081 complex (3087 Coolant Distribution Unit, 3089 Power Unit [or another source of 400-Hz power], and the consoles).

Consoles

Each side of a 3084 uses at least three consoles:

- A system console, which interacts directly with other components of the 3084 complex. (See Chapter 4, "3082 Processor Controller" for more information.)
- A service support console, which interacts with the service and support microcode. (See Chapter 4, "3082 Processor Controller" for more information.)
- An operator console, which interacts with the control program and communicates with it through one of the channels. In a single-image 3084 complex, only one operator console is required for communication with the control program.

  The choice of consoles typically includes the IBM 3277 and 3278 Display Stations and the IBM 3279 Color Display Station. An operator console can be backed up by an alternative console defined at system generation. A printer can be attached to the control unit to provide a printed record of operator-console display images.

A fourth console, the programming support console, is optional.

Store-In-Buffer Concept

Each central processor contains a high-speed buffer (cache) that is transparent to programs. The use of the buffer reduces effective access time for both instructions and operand data. All instruction and operand fetches and all modifications to central storage made by a central processor take place in the buffer. Data transfers to and from I/O devices take place directly in central storage. Data retrieval synchronization and data integrity are maintained by the use of a directory of each buffer. (See "System Controller" in Chapter 3 for more information.) The buffers use a least-recently-used (LRU) algorithm for efficient data replacement. (See Chapter 3, "3084 Processor Unit" for more information.)

Modes of Operation

The 3084 complex operates in either S/370 mode or 370-XA mode. The S/370 mode conforms with System/370 architecture as described in the *IBM System/370 Principles of Operation*. The 370-XA mode conforms with System/370 extended architecture as described in the *IBM System/370*

Extended Architecture Principles of Operation. The mode is selected during initial microprogram load (IML).

A single-image 3084 complex operates only in 370-XA mode, but each side of a partitioned complex can operate in either 370-XA mode or S/370 mode. In a partitioned 3084 complex, the choice of mode on one side does not affect the choice of mode on the other.

S/370 mode and 370-XA mode differ in a number of respects. The two major areas of difference are in input/output (I/O) operations and in storage addressing.

Input/Output Operations

In both S/370 mode and 370-XA mode, the 3084 complex provides 48 channels (24 on each side). All the channels can be assigned for block-multiplexer operation, or as many as four channels of each EXDC can be assigned for byte-multiplexer operation. Any channel not needed for byte-multiplexer operation can be reconfigured for block-multiplexer operation.

Physically, the channels are organized into groups of eight. If one (or more) of the channels of a channel group fails, it can be removed from the operating configuration, to permit continued operation. (For more information about channels, see "External Data Controller" in Chapter 3.)

As many as eight control units can be physically attached to each channel, and each channel can address as many as 256 I/O devices. A single-image 3084 complex can control as many as 4,080 devices, and a partitioned 3084 complex can control as many as 4,080 devices on each side.

S/370 Mode

In S/370 mode, any channel may be assigned any valid channel address without concern for priority. Channel operation is based on a random, time-sliced approach that gives each channel equal opportunity to request service.

Logically, channels are organized into two sets on each EXDC (one set for each central processor) with as many as 16 channels allowed in one set. Channel-set switching is a standard feature. If one central processor fails, its set of channels (a channel set) can be reassigned (under program control) to the other central processor on the same side. This permits continued data processing, but with some performance degradation. The other central processor on the same side may use the sets of channels alternately.

370-XA Mode

In 370-XA mode, as many as four channel paths are available to any attached I/O device. During any I/O operation, the *channel subsystem* selects one of the available channel paths to any specific I/O device.

The 370-XA mode improves system efficiency by making channel-path selection a hardware function rather than a control-program function. System efficiency is also improved by the queuing of pending I/O requests, thereby eliminating any control-program delays in reinstructing the I/O device.

At the start of an I/O operation, a central processor signals the channel subsystem (instead of a single channel, as in S/370 mode) that an I/O operation to a given I/O device is needed and that an I/O request is posted to a queue; meanwhile, instruction execution in the central processor continues. Channel-path management and the queuing of I/O requests eliminate all of the busy-condition I/O interruptions encountered in S/370-mode operations.

In 370-XA mode, byte-multiplexer and block-multiplexer operation and attachment methods are unchanged, and existing channel programs (CCWs) continue to function without any changes. However, in 370-XA mode, channel paths are not logically organized into channel sets.

When a device is dynamically reconnected to the system, the first available channel path (of the several channel paths attaching the control unit) may be selected, if the control unit has the dynamic reconnection feature.

Storage Operations

In 370-XA mode, storage addressing is extended from 24 bits to 31 bits, which represents an address range of 2G bytes (2,147,483,648 bytes). In addition, 370-XA mode permits the use of either 24-bit or 31-bit addressing, under program control. This facilitates the running of existing application (problem) programs with 370-XA-mode control programs.

In 370-XA mode, an additional CCW format is provided to permit direct addressing of storage above 16M bytes for I/O operations. With this format, channel programs may also reside above 16M bytes.

Support Unit

The 3082 Processor Controller Model Q48 or X48 is a stand-alone support unit that continuously monitors 3084 complex operation through direct communication with each component in the 3084 complex.

The 3082 initializes the system, distributes microcode to control storage during initial microprogram load (IML), monitors voltage levels and coolant temperature, and provides the control-unit function for both the system console and service support console.

The 3082 also provides extensive error recording, recovery, and diagnostic support (described in "Processor Controller" under "Reliability, Availability, and Serviceability" in this chapter).

The 3082 is described in more detail in Chapter 4.

Technology

The 3084 complex uses several logic-circuit technologies. The processor-unit logic is implemented in a new technology (TCM and its associated circuit board), but central storage and the processor controller function are implemented in a mixture of monolithic technologies.

A TCM (Figure 2-2) is a helium-filled, encapsulated module that is covered by a cold plate through which chilled water circulates to absorb heat. The TCM measures 125 by 134 by 35 millimeters (4.9 by 5.3 by 1.4 inches) and contains as many as 133 silicon chips mounted on a multilayered ceramic substrate that produces a package containing tens of thousands of logic circuits. The TCMs are plugged into a multilayered circuit board that provides TCM powering and TCM-to-TCM connection. Each central processor consists of eight TCMs and the associated board. Therefore, the major element of a processor unit is designed so that no external wiring or cabling is required.

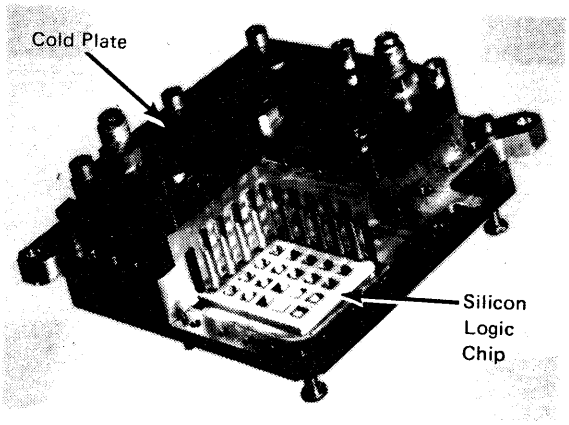


Figure 2-2. Thermal Conduction Module with a Cold Plate (Cutaway View)

Power

Each side of a 3084 complex requires a source of 400-Hz power. The 3089 Power Unit is designed to be the standard source of 400-Hz power for each side of the 3084 complex. The 3089 meets IBM machine-room environmental standards, and therefore can be located in the machine room.

Cooling

The 3084 Processor Unit uses both air cooling and water cooling. The water cooling is provided by two 3087 Coolant Distribution Units (one for each side).

The 3087 is available in two models: the water-cooled Model 1 and the air-cooled Model 2. The 3087-1 uses a water-to-water heat exchanger, which transfers the 3084's heat to the customer's chilled-water supply. The 3087-2 uses a water-to-air heat exchanger, which transfers the

3084's heat to the air in the computer room. The 3087-1 is more efficient and shorter in length, whereas the 3087-2 may be more convenient for users who have limited cooling requirements. Both 3087s must be either Model 1's or Model 2's.

The 3087 conditions and controls chilled water in a closed loop to maintain controlled temperature and flow rates to the densely packed circuits in the processor unit. The 3087 contains both the necessary controls to maintain the proper temperature within the self-contained closed loop and an automatic valve to adjust the flow of the chilled water.

The 3087 includes two pumps. If a cooling problem occurs as the result of a malfunction in the operating pump, the alternate pump is switched automatically into the coolant circuit for continued operation.

Data Representation

The basic addressable data unit is an eight-bit byte that may be used as one character, two decimal digits, or eight binary bits. The 3084 provides the following data representation features:

- Efficient use of storage and effective I/O rates for decimal data
- Variable-length fields
- Broad and flexible code conversion
- Decimal arithmetic
- Fixed- and floating-point arithmetic
- 32-bit words, 64-bit doublewords, and 128-bit extended words (for floating-point arithmetic)
- Instructions for functions such as translate, edit, convert, move, and compare

Error Handling

The 3084 contains comprehensive, automatic error-handling procedures that are often assisted by the 3082 Processor Controller. Error correction and recovery are attempted as a first

step by using one of the following procedures (depending on where the error is detected):

- Processor checkpoint retry for the central processors
- Error handling for the external data controller (EXDC)
- Error checking and correction for central storage

When an error is detected, the 3082 automatically performs error-analysis procedures to isolate the malfunctioning area of the processor complex directly and therefore identify the field-replaceable unit (FRU) or group of units. These procedures also include problem recognition, recording, and diagnosis.

Error analysis includes data scanout that consists of serialized bit-by-bit transfer of the data contained in the TCMs into the processor controller for analysis (to isolate the problem). Therefore, to isolate a FRU (for example, a TCM) or a group of FRUs, the error analysis uses all data scanned out at the time of the error. Errors are analyzed by the processor controller concurrent with the operation of the 3084 complex.

If the error is repeated frequently or is unrecoverable, the analysis information is displayed on the system console. The operator can provide the information to IBM service personnel.

Processor Checkpoint Retry

Processor checkpoint retry (CPU retry) is an improved, more inclusive recovery mechanism than the instruction retry used on earlier IBM systems because it generally involves the retry of a series of instructions, rather than the retry of a single instruction. It can correct intermittent errors beyond those associated with a single instruction.

Processor checkpoint retry is implemented by using a series of error-detection circuits and a set of backup facilities (for example, a program status word [PSW] and general registers). The error-detection circuits within each central processor are continuously active.

Periodically, a checkpoint is taken by the central processor during the execution of instruction sequences. A checkpoint saves information in the backup facilities about the state of the central processor so that this processor can return to a point at which all processing was known to be correct, and can reexecute any failing instruction sequence.

If an error is detected in a central processor, instruction execution stops. The processor controller saves information about the failure (that is, it initiates a logout of the central processor) and directs the central processor to return to the last checkpoint. The central processor uses the data saved in the backup facilities to restore itself to the state that existed at the time the checkpoint was established. Instruction processing is restarted from that point.

A central processor performs retry as many as eight times. If the error has not been corrected by the eighth retry, the central processor either performs a machine-check interruption or enters the check-stop state. If the error is corrected on or before the eighth retry, system recovery is reported by a repressible machine-check interruption and processing continues.

Most, but not all, operations can be retried; for example, the Signal Processor instruction cannot be retried after it has signaled another central processor. Before execution of a nonretryable operation is attempted, correct operation of the instruction sequence to that point is verified. If an error occurs during execution of a nonretryable operation, the central processor either performs a machine-check interruption or enters the check-stop state. A new checkpoint is established and processing continues when correct execution of a nonretryable operation has been verified.

Figure 2-3 shows the bits of the machine-check interruption codes supported by the 3084.

Certain bits in control register 14 are associated with machine-check handling. Of these bits, the 3084 supports the use of bits 3 through 7 in 370-XA mode, and bits 0 and 4 through 7 (but not 1, 8, or 9) in S/370 mode.

S/370 Mode

```
SPSTCE  W      BDS K WMPIF EFGC S
DDRDDD00 00000  E0E0PSMAA0CPRR0T
0                              31

                CC
00000000000000TC0000000000000000
32                             63
```

370-XA Mode

```
SPS C   WCSC  B S K WMPIF  FGC S
DDR0D000 PPK00 0E0E0PSMAA00PRR0T
0                              31

                CC
00000000000000TC0000000000000000
32                             63
```

Legend:

```
B   Backed up
CC  Clock-comparator validity
CD  Timing-facility damage
CK  Channel-subsystem damage
CP  Channel report pending
CR  Control-register validity
CT  CPU-timer validity
D   Delayed
EC  External-damage-code validity
ED  External damage
FA  Failing-storage-address validity
FP  Floating-point-register validity
GR  General-register validity
IA  PSW-instruction-address validity
KE  Storage-key error uncorrected
MS  PSW mask and key validity
PD  Instruction-processing damage
PM  PSW program-mask and condition-
      code validity
SD  System damage
SE  Storage error uncorrected
SP  Service-processor damage
SR  System recovery
ST  Storage logical validity
TD  Interval-timer damage
W   Warning
WP  PSW-EMWP validity
```

Figure 2-3. 3084 Machine-Check-Interruption Code Formats

EXDC Error Handling

Errors detected within an EXDC are handled in one of two ways:

- An interface-control check indicates that an error occurred in a control unit or on the I/O interface and causes posting of an interruption and invoking of software error recovery.

- For an error occurring within an EXDC, the 3082 Processor Controller may temporarily stop all EXDC operations by stopping the clocks to scan out, for analysis, the status of certain facilities where the error was detected. All channel operations in process at the time of a channel-control check may be reinitiated under software control. (For more information about the EXDCs, see "External Data Controller" in Chapter 3.)

Error Checking and Correction for Central Storage

Error checking and correction (ECC) for central storage provides automatic, single-bit error detection and correction. ECC also detects all double-bit errors and most multiple-bit errors but does not correct them. ECC takes place in the system controller and in central storage. (See Chapter 3, "3084 Processor Unit" for more information.)

CPU ID

The doubleword whose address is designated by the second operand of the Store CPU ID (STIDP) instruction contains the following information:

- The version code (two hexadecimal digits: 26 for Model Q, 66 for Model Q with the performance feature, and A6 for Model QX)

- The CPU identification number (six hexadecimal digits):

  - The first digit is the central-processor address: 0, 1, 2, or 3

  - The next five digits are selected from the processor-unit serial number

- The model (processor-complex) number (four digits: 3084)

The last four hexadecimal digits are 0000.

Reliability, Availability, and Serviceability

Concurrent maintenance and duplication of hardware, use of the highly integrated TCM for logic implementation, the processor controller, and remote servicing contribute to the reliability, availability, and serviceability of the 3084 complex.

Concurrent Maintenance and Duplication of Hardware

The duplication of all critical hardware helps ensure continued operation under a variety of conditions, most of which permit concurrent maintenance; that is, maintenance performed while at least part of the complex continues processing.

In a single-image 3084 complex, concurrent maintenance is usually allowed for failing components. If a component fails, the side having the failing component generally can be reconfigured into a maintenance subsystem while the other side continues operating. After being repaired and tested, the component can be returned to the operating configuration without need for another initial program load (IPL) or IML.

Some hardware failures preclude continued operation. Such failures may be:

- In the hardware system area of central storage
- In processor-controller monitoring and control circuitry in the 3084 Processor Unit
- In either system controller
- Concurrent multiple failures on both sides

In both single-image and partitioned 3084 complexes, concurrent maintenance is permitted for central storage. Part of central storage can be isolated and repaired while the 3084 complex or side continues processing, using the rest of central storage.

Also, for both single-image and partitioned 3084 complexes, maintenance can be deferred:

- In a single-image 3084 complex, certain components (such as an EXDC or as many as three central processors) can be isolated for deferred maintenance while the rest of the 3084 complex continues operating.
- In a partitioned 3084 complex, each side is serviced independent of the other. If a duplicate component (a central processor, one or two channel groups, or one or more channels) fails on one side, that component can be isolated for deferred maintenance while the side continues operating. All other failures preclude continued operation of the side having the failing component.

TCMs

A single central processor (consisting of eight TCMs and the associated board) is an interconnected component that requires no external wires or TCM-to-TCM cabling, because all power and signal conductors are embedded in the basic structure of the TCM and its board. This high degree of integration improves 3084 reliability.

Processor Controller

The 3082 Processor Controller provides the following extensive error recording, recovery, and diagnostic support for IBM service personnel:

- Assisting the processor unit in error recovery
- Monitoring and logging all hardware failures
- Analyzing logout data and identifying failing parts
- Communicating with remote support locations

If automatic error recovery fails, the processor controller performs error analysis to identify the failing FRU or group of FRUs. Information about any failing FRU is displayed on the system console, and the operator can include this

information when notifying IBM service personnel so that replacement parts can be obtained for the service call.

More extensive error analysis can be performed by IBM service personnel through the use of dedicated diagnostic microcode. However, the dedicated use of one side of the 3084 complex is required to run such microcode.

The central storage controller interacts with the 3082 to permit concurrent maintenance and repair of central storage, without regard to how the 3084 is configured. Information about previously logged errors (logged as they occurred during operation) is used with diagnostic microcode to locate storage failures. Failing cards can be replaced, and the repair can be verified. After being serviced, that element can be tested by rerunning the diagnostic microcode.

If local diagnostic methods fail to determine the problem conclusively or to isolate the failure, the processor controller provides a data link to the IBM Large Systems Support Center for the assistance of highly trained service specialists.

Remote Servicing

The data link to a remote support console is established manually (with user authorization) from the user's site. The Remote Support Active indicator (on the operator control panel of the system console) lights and remains lighted during the data link. These procedures permit customers to monitor use of the data link.

When a remote support console is connected by the data link, IBM Large Systems Support Center personnel have access to the same information that is available to local IBM service personnel through the service support console. Control of the system can be passed to a remote support console so that scan data and the contents of a wide range of arrays, latches, triggers, and registers can be examined and analyzed. The 3084 Processor Unit can be controlled remotely (for example, for starting, stopping, and address comparing).

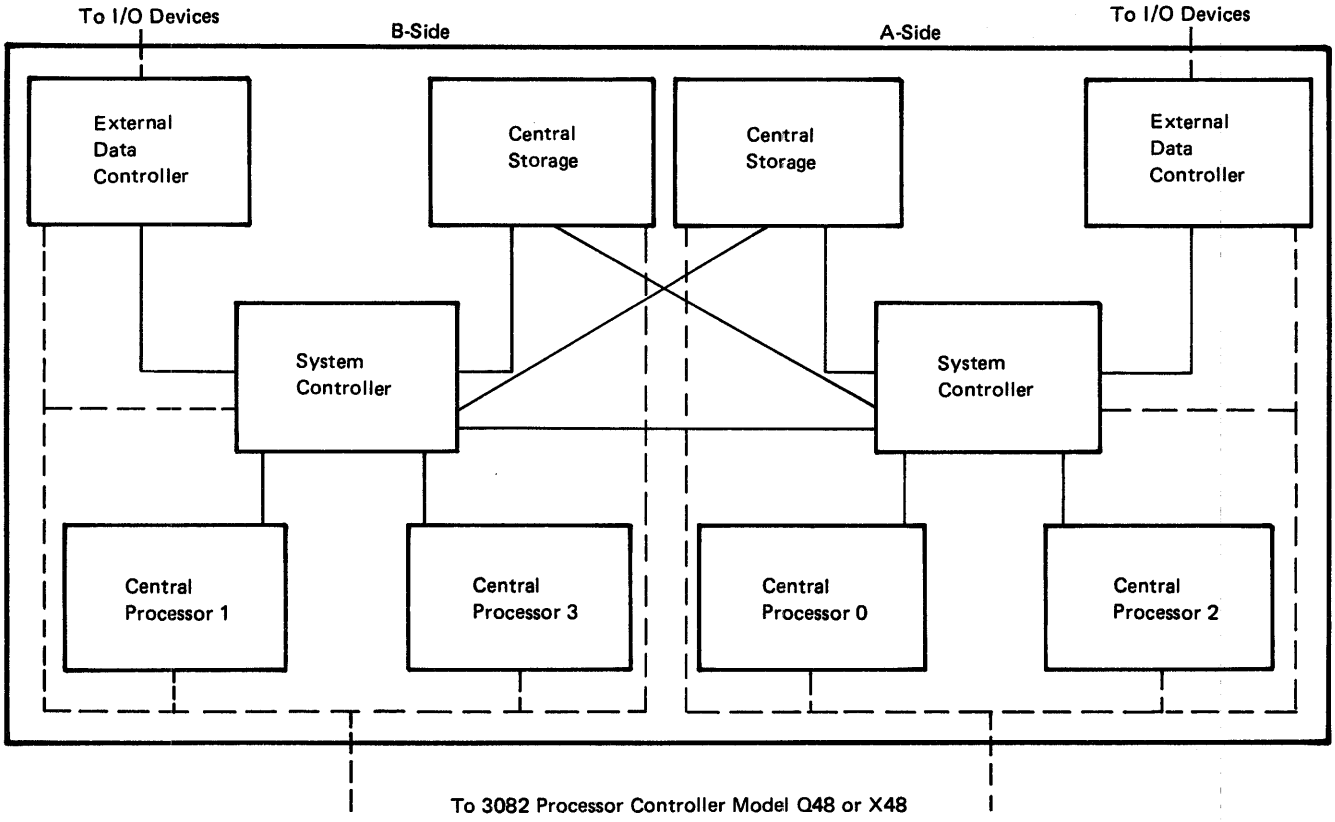
Chapter 3. 3084 Processor Unit

The 3084 Processor Unit consists of the following logical components (Figure 3-1) that execute instructions and commands, and perform storage and channel functions:

- Four integrated central processors
- Shared central storage (one-half of central storage residing on each side)
- Two external data controllers (one on each side, each with 24 channels)
- Two system controllers (one on each side)

The 3084 Processor Unit provides the following central storage capacities:

3084 Model	Bytes of Central Storage
Q32, QX3	33,554,432 (32M)
Q48, QX4	50,331,648 (48M)
Q64, QX6	67,108,864 (64M)
Q96, QX9	100,663,296 (96M)
QC8, QXC	134,217,728 (128M)



Legend:

——— Data and control lines
– – – Monitoring lines

Figure 3-1. Logical Components of the IBM 3084 Processor Unit

The 3084-QX differs from the 3084-Q in that the 3084-QX has a central-processor cycle time of 24 ns instead of 26 ns.

Note: If the optional performance improvement feature is installed on Model Q, the basic machine cycle time is 24.5 ns instead of 26 ns.

Each central processor has a high-speed buffer with a two-cycle access time (48 ns in Model QX, 49 ns in Model Q with the optional performance feature installed, and 52 ns in Model Q without the performance feature installed).

The access time to central storage from a central processor is 312 ns, and data transfers between central storage and a buffer occur in 128-byte increments. Data transfers across the channels between central storage and the external data controllers (EXDCs) take place directly, bypassing the buffers. Modification of data by a central processor occurs in its buffer.

Central Processors

Each central processor is microcode controlled and contains an instruction element (IE), variable field element (VFE), execution element (EE), control storage element (CSE), and buffer control element (BCE). The CSE fetches microinstructions that control instruction execution in the IE, VFE, and EE. The BCE controls the transfer of data between central storage and the central processor containing that BCE. Dynamic address translation is an automatic function of the BCE.

Instruction Element

The instruction element (IE) controls the sequencing of all instructions. It generates all addresses for instruction requests and initiates all central storage requests (both fetch and store). The IE includes its own buffers, registers, and hardware to handle instructions other than those executed in the VFE and EE. Execution of most instructions in the RR, RRE, RX, RS, S, SI, and SSE formats takes place in the IE.

Variable Field Element

The variable field element (VFE) executes SS-format instructions. It contains a decimal adder, two input registers, and two output registers. While using the data in one input register, the IE can be filling the other. The output registers work in the same way. Output goes to the storage data register in the IE. While the VFE is operating, the IE continues to fetch and store additional operand data.

Execution Element

The execution element (EE) provides the arithmetic results in the following operations:

- Fixed-point divide
- Fixed-point multiply
- Convert to binary
- Convert to decimal
- Floating point
- Extended-precision floating point

The EE contains various adders and registers to execute the instructions, and a local working storage to retain register contents during a checkpoint.

Control Storage Element

The control storage element (CSE) is the logical element that controls microcode execution in the central processor and contains the supporting control storages and registers that are used by the central processors.

Part of control storage is dynamically loadable. The dynamically loadable part permits infrequently used microcode to be loaded (from the hardware system area in central storage) as required. A lookaside directory, which is associated with the dynamically loadable part of control storage, permits immediate execution of in-place microinstructions and initiates the fetching of the appropriate microinstructions when they are not present in the CSE. When newly referenced microinstructions are loaded,

they overlay the least recently used (LRU) microcode.

Buffer Control Element

The buffer control element (BCE) handles all central processor references to and from central storage, performs dynamic address translation, and controls the high-speed buffer.

The BCE includes:

- A 64K-byte high-speed buffer
- A buffer directory
- A translation lookaside buffer (TLB)
- Dynamic address translation (DAT) hardware
- A store-back array

The High-Speed Buffer provides much faster access to instructions than if they were stored in central storage. The buffer is transparent to executing programs. It is a store-in buffer that has a two-cycle access time for eight bytes of data with address translation done in parallel. The buffer is logically partitioned into 512 blocks. Each block contains 128 bytes. The blocks of data in the buffer are replaced by using a least recently used (LRU) algorithm.

When data is referred to during instruction execution, the buffer, the directory, and the TLB are accessed at the same time for address comparison.

The Buffer Directory contains the central-storage absolute addresses for the 128-byte blocks of data in the buffer. The directory entries contain bits that indicate:

- A block of data has been modified.
- The area in central storage that contains a specified block has been modified.
- The buffer has the only valid copy of the block. This bit must be on before a block can be stored into central storage.
- The block has been modified during a checkpoint interval and cannot be replaced until the end of the interval.

The TLB contains as many as 128 virtual-real address pairs. When a virtual address is translated, the real address of the referenced page in central storage is stored in the TLB. Therefore, subsequent translations for the same virtual address are not required because the real address is immediately available in the TLB.

A least-recently-used (LRU) algorithm is used for the replacement of TLB entries. The TLB can be cleared by a reset or by the Purge TLB (PTLB) instruction. Under certain conditions, the TLB or selected entries in it may also be cleared by the Invalidate Page Table Entry (IPTE) instruction.

Dynamic Address Translation performs high-speed translation from virtual to real addresses for loading the TLB. Translation is overlapped so that if referenced data (real address) is in either central storage or the buffer, the data is directly available.

In S/370 mode, the 3084 uses 4K-byte pages and 64K-byte segments. In 370-XA mode, the 3084 uses 4K-byte pages and 1M-byte segments. An S/370-mode interpretively executed guest virtual machine can additionally use the 1M-byte segment size.

The Store-Back Array stores original copies of data that were modified in the high-speed buffer since the last checkpoint. If an error condition causes a processor checkpoint retry, this data is returned to the buffer before reexecution of the failing instruction sequence. The store-back array is reset at each checkpoint if no errors are detected within the checked instruction sequence.

Central Storage

The 3084 Processor Unit has two levels of storage (central storage and a high-speed buffer in each central processor) implemented in monolithic and large-scale-integration technologies. (The buffer is described under "Buffer Control Element" in this chapter.)

Central storage can have a total storage capacity of 32M, 48M, 64M, 96M, or 128M bytes (16M, 24M,

32M, 48M, or 64M bytes on each side). Depending on how the 3084 is configured and operated, all of central storage can be shared by the four central processors, or each half can be shared by the two central processors of that side. The two halves are symmetric.

A hardware system area is reserved within central storage for specific system information and cannot be addressed by user programs. The addressable portion of central storage is synonymous with main storage, as described in the *IBM System/370 Principles of Operation* and the *IBM System/370 Extended Architecture Principles of Operation.*

Each side of central storage is structured into two basic storage elements (BSEs). The BSEs, which have a storage capacity of 8M, 16M, or 32M bytes, contain the logic for fetching doublewords from (or storing doublewords into) the data arrays in each BSE. The data arrays are divided into two or four basic storage modules (BSMs). Central storage has two- or four-way interleaving of contiguously addressed 2K-byte blocks of storage. Interleaving, which is determined during initialization, permits the simultaneous accessing of separate BSMs. Therefore, access by any central processor or either EXDC to different physical BSMs can occur simultaneously.

The BSE logic performs the following functions:

- Data storage and retrieval for the processor complex
- Central storage communication with the processor complex (by means of the system controller)
- ECC
- Storage regeneration control

Note: Because 3084 storage is volatile, power failure results in the loss of data in central storage.

Hardware System Area

As part of the initial microprogram load (IML), at least 320K (327,680) bytes of central storage are selected for use as the hardware system area. This storage, which is unavailable for program use, contains:

- Copies of microcode
- A unit control word (UCW) for each configured I/O device
- Message buffers
- Tables
- Directories

The hardware system area cannot be accessed by conventional (program) storage references.

In a single-image 3084 complex, one hardware system area is shared by all four central processors. In a partitioned 3084 complex, each side has its own hardware system area.

If more than 512 control units and I/O devices are required, the hardware system area is automatically expanded in increments of 64K bytes to as much as 576K (589,824) bytes. Storage in the hardware system area (to a total of 1,024K [1,048,576] bytes for all purposes) may be reserved optionally during an IML for IBM service personnel to trace I/O operations.

Error Checking and Correction

Error checking and correction (ECC) code bits are stored with data in the central storage data arrays. Single-bit errors detected during data transfer are corrected. Multiple-bit errors are flagged for follow-on action.

Data paths from the central processors and the channels are checked for parity. Parity bits are included in each command or data word.

Key-Controlled Storage Protection

Key-controlled storage protection provides both store and fetch protection. It prevents the unauthorized access or modification of information in central storage.

Each 4K-byte block of storage is protected by a seven-bit storage key. For processor-initiated store operations, access-key bits 0-3 from the currently active program status word (PSW) are compared with bits 0-3 from the storage key associated with the pertinent 4K bytes of storage to be accessed. If the keys do not match, then that central processor is notified of a protection violation, the data is not stored, and an interruption occurs. The same protection is active for fetch operations if bit 4 of the storage key (the fetch-protection bit) is on.

Storage protection is regulated by each system controller.

External Data Controller

Each of the two external data controllers (EXDCs) is an integrated I/O processor that contains and controls 24 channels. A 3084 therefore has 48 channels. As many as four channels in each EXDC can be configured for byte-multiplexer operation; all the others must be configured for block-multiplexer operation.

In byte-multiplexer operation, channels can be used in either byte-multiplex mode or burst mode. Byte-multiplex mode permits the concurrent operation of several relatively slow-speed I/O devices.

In block-multiplexer operation, channels can operate in either interlock mode (the standard mode) or data-streaming mode (for data-streaming control units). Data rates can be as high as 1.5 megabytes per second in interlock mode, and as high as 3.0 megabytes per second in data-streaming mode. All channels configured for block-multiplexer operation may be attached to control units that can operate in interlock mode or in data-streaming mode.

In a 3084 complex, channels are organized physically into three groups for each EXDC (eight channels for each group). In a partitioned 3084 complex, channels are also organized logically into two channel sets on each side that is operating in S/370 mode. As many as 16 channels are allowed in one channel set.

Channel organization is described in more detail in Chapter 2 under "Input/Output Operations."

In S/370 mode, any physical channel may be assigned any valid channel address, but channel addresses must be contiguous within each channel set.

In a partitioned 3084 complex, the EXDC of each side that is operating in 370-XA mode operates as a channel subsystem having 24 channel paths.

In a single-image 3084 complex, the resources of the EXDCs are combined into a single channel subsystem having 48 channels.

EXDC operation in 370-XA mode has several advantages:

- When an I/O request is made of any I/O device, the request is posted to the channel subsystem, which selects the channel path.
- The channel subsystem manages as many as four channel paths to any device and handles any I/O-busy conditions.
- If any of the central processors of the 3084 are taken offline, channel recovery is not impacted, because interruptions may be handled by any of the remaining central processors.
- The channel subsystem permits dynamic reconnection of certain I/O devices, such as the IBM 3380 Direct Access Storage Model AA4. Dynamic reconnection allows such an I/O device to use the first available channel path (of as many as four) when the device reconnects to a channel, without regard to which channel path was used initially.

Each EXDC consists of the following logical elements:

- One channel processing element (CPE)
- Three data server elements (DSEs)

- Twenty-four interface adapter elements (IAEs)

Channel Processing Element

Each EXDC has one microcode-controlled channel processing element (CPE) that interacts with three data server elements (DSEs) to do the following:

- Fetch channel command words (CCWs)
- Perform queuing and dequeuing for queued I/O requests
- Analyze status
- Post interruptions
- Start and end DSE operations
- Assist DSEs in command chaining and indirect addressing
- Manage channel-path selection (in 370-XA mode)

Data Server Elements

Each EXDC has three data server elements (DSEs)—one for each channel group (eight channels). Each microcode-controlled DSE provides a port to each of eight channels. The DSE uses a time-slicing technique to service all ports equally. Time slicing removes channel priority considerations.

The DSE controls channel functions by:

- Accepting and acting on commands from the CPE
- Controlling the transfer of data between the I/O devices and central storage
- Analyzing the ending status of a data transfer and sending it to the CPE

Interface Adapter Elements

The interface adapter elements (IAEs), which are *physically* located in the 3082 Processor Controller, control the I/O interfaces; therefore, each DSE port has an IAE. In S/370 mode, the microcode of the EXDC provides the flexibility to assign a physical interface to any valid channel designation.

The IAE controls channel functions by:

- Performing I/O-interface tag sequences
- Interpreting control signals sent from the DSE

System Controller

Each side of the 3084 Processor Unit has a system controller. Each system controller acts as a switching device among all other logical components of one side of the processor unit by interconnecting the two central processors and the external data controller with central storage.

The two system controllers coordinate the use of processor-unit resources, with each managing the hardware resources on its side of the 3084 complex. In a single-image 3084 complex, the system controllers operate together in:

- Permitting the resources of the two EXDCs to function as a single channel subsystem
- Assigning the storage locations of the two sides of central storage to a single absolute address space
- Coordinating the use of the high-speed buffers of the central processors on opposite sides of the 3084 complex

In a single-image 3084 complex, each system controller has direct access to both sides of central storage. If central storage receives an access request from each of the two system controllers simultaneously, central storage determines which request is honored first.

On each side, the system controller:

- Controls data transfers to and from central storage
- Is the key switching element in the data flow between processor-unit components (the central processors, the EXDC, and central storage)
- Controls storage protection
- Contains a time-of-day (TOD) clock

Each system controller includes hardware for ECC, storage protection, directories (similar to the BCE directories), a queue array, and I/O interruptions.

Because the central processors have store-in buffers, central storage may not be at the latest level. To ensure valid data, the system controller blocks access by any subsequent requesting central processor until the using (first requesting) central processor ensures that a transfer of valid changed data from the high-speed buffer to central storage has occurred. Exact copies of each buffer directory that resides in the system controller are referred to each time a central processor requests data from central storage.

The system controller also keeps track of central storage requests and assigns priorities to them. When two components on the same side (for example, an EXDC and a central processor or two central processors) require access to the same storage module at the same time, the system controller establishes the priority. The system controller also designates which component can use specified data when contention exists.

Chapter 4. 3082 Processor Controller

The 3082 Processor Controller Model Q48 or X48 (Figure 4-1) provides and performs a variety of functions for the entire 3084 complex. Among them are:

- Monitoring and supervising all operations in the 3084 complex
- Providing the control-unit functions for all the consoles other than the operator consoles
- Providing two remote support facility modems and two processor controller files
- Providing an operator-controlled, two-position switch that determines whether the 3084 complex is in single-image mode or partitioned mode
- Providing the interface adapter elements for 48 channels

A 3082 Model Q48 or X48 is used with a 3084 as follows:

3082 Model	Used with 3084 Model
Q48	Q32, Q48, Q64, Q96, QC8
X48	QX3, QX4, QX6, QX9, QXC

The 3082 Models Q and X have two sides (A and B). The 3082 Model Q48 or X48 has twice the resources of the 3082 Model 24 or X24, which is part of the 3081-K or -KX complex, respectively.

A 3082 Model X16 or X24 (for the 3081) can be upgraded to a 3082 Model X48 (for the 3084), just as a 3082 Model 16 or 24 (for the 3081) can be upgraded to a 3082 Model Q 48 (for the 3084).

Note: When the optional performance feature is installed on the 3084 Model Q, the performance feature must also be installed on both sides of the associated 3082 Processor Controller.

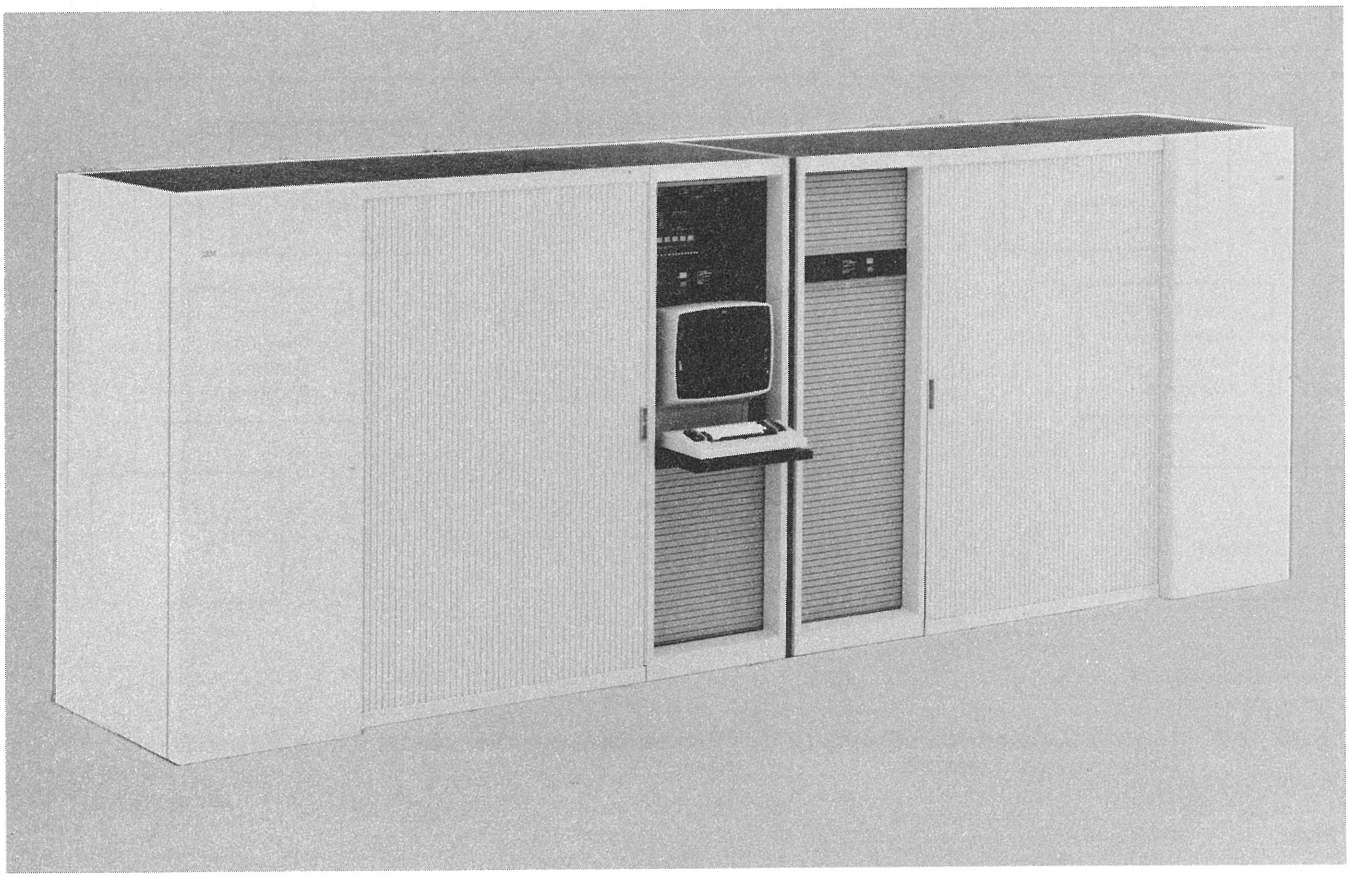
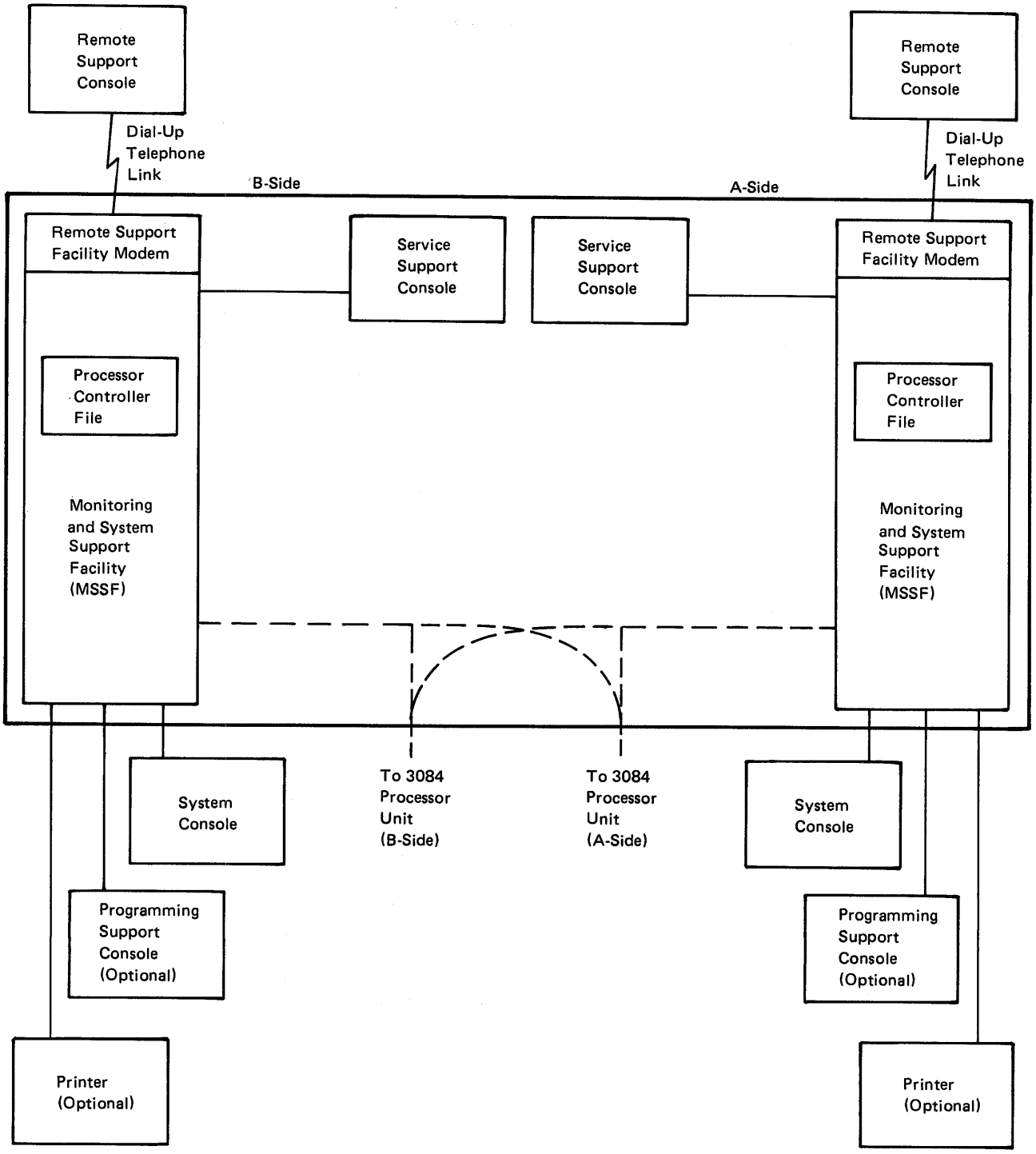


Figure 4-1. IBM 3082 Processor Controller Model Q48 or X48 (Design Model)



Legend:

——— Data and control lines
– – – – – Monitoring lines

Figure 4-2. Logical Components of an IBM 3082 Processor Controller Model Q48 or X48 with Consoles and Printers

Monitoring and Supervisory Functions

The monitoring and supervisory functions of the 3082 are performed by one or both of the monitoring and system support facilities (MSSFs), depending on the physical mode. Through the use of one or both MSSFs, the 3082 performs the following functions:

- Monitoring and control of system operation
- Display of channel and central-processor activity
- Recovery from processor-unit errors

Also, the 3082 is used to initiate configuration changes.

In a single-image 3084 complex, one MSSF supports the operation of the 3084 complex while the other MSSF stands ready as the backup. In a partitioned 3084 complex, each MSSF supports the operation of its respective side of the 3084 complex.

Monitoring and Control of System Operation

The 3082 monitors and controls the operations of the 3084 complex. It begins with initialization and proceeds through the sequencing of power to all the 3084 components and to all interconnected I/O control units that are under power-sequence control. During initialization of the 3084 complex, the 3082 validates areas of central storage as error-free data locations, records failing storage locations, and assigns the hardware system area in central storage based on contiguous error-free storage. The assignment of absolute address 0 is also made on the basis that the first 2M (2,097,152) bytes of a storage element are error free. This procedure ensures that this critical location for control-program residency is error free. After power sequencing, the 3082 performs an IML.

During processing, the 3082 monitors voltage levels and coolant flow. If coolant flow in a 3087 decreases or stops, the second pump in that 3087 is switched into the coolant circuit to avoid thermal shutdown. If voltage adjustments are needed, IBM service personnel can use the 3082 to perform the required adjustment.

Channel and Central-Processor Activity Display

The 3082 provides the capability to sample and display channel and central processor activity.

Using the SYSTEM ACTIVITY DISPLAY (SAD) frame, the operator can choose options that specifically set up the sampling to suit the situation. Variables include target elements, sample time periods, operating states, and range parameters. Once a SAD frame is defined, it remains cataloged and can be recalled and invoked.

As many as four user-defined SAD frames are permitted. They can be displayed on the system console. In a single-image 3084 complex, the other system console can also be used to display SAD frames.

Processor-Unit Error Recovery

The 3082 assists the processor unit in error recovery. When an error occurs within the processor unit, the 3082 assists in checkpoint retry or channel error correction.

The 3082 logs errors as they occur and then analyzes them for IBM service personnel. Failure symptoms, saved at the time of a malfunction, are analyzed on a time-shared basis with other processor controller functions; this operation is concurrent with operation of the 3084 Processor Unit in either physical mode.

The 3082 saves the symptoms of these errors, correlates multiple symptoms, performs error analysis, and isolates the failure to the failing FRU or group of FRUs. This procedure is done automatically and is concurrent with continuing operation of the 3084 Processor Unit. When automatic error-recovery attempts fail or the error occurs frequently, failure information is displayed on a system console, and an audible alarm is sounded to alert the operator of a problem requiring action. During IML, similar notification to the operator occurs when loss of storage exceeds a threshold that may degrade performance.

Configuration Changes

Through use of a service support console or system console (discussed later in this chapter), the 3082 can be used to initiate changes in the configuration of the 3084 Processor Unit to one or more of the following components or elements:

- Central storage arrays
- Central processors
- Interface adapter elements

However, operator-initiated action through the control program is the preferred method of reconfiguring, because it makes both hardware and software changes as a single integrated action.

Such action adds or removes components or elements from the configuration in preparation for either concurrent or deferred maintenance.

Control Unit Functions

The processor controller (see Figure 4-2) provides control-unit functions for the following devices:

- Two system consoles
- Two service support consoles
- One or two optional printers
- One or two optional programming support consoles

In a single-image 3084 complex, the attached devices of one side are operational while the attached devices of the other side stand ready as backup. In a partitioned 3084 complex, each of the attached devices operates with its respective side. Additionally, each service support console can be associated with either MSSF under switch control so that either console can be used with either side or with the entire 3084 complex.

System Consoles

Depending on the physical mode, one or both system consoles interact directly with the system through the processor controller and display system status and system activity. They also perform the following console functions: address compare, alter, display, start, stop, reset, restart, external interruption, and initial program loading (IPL).

Each system console (Figure 4-3) is a stand-alone IBM 3278 Display Console Model 2A. The display screen contains 25 lines. Lines 1 through 21 are used for formatted function frames. Lines 22 through 25 display system and console status, messages, and operator input. The display console also has switches, controls, and indicators for contrast and brightness, alarm volume, status conditions, and error conditions. The keyboard resembles a typewriter keyboard but includes special function keys. The operator control panel, containing system indicators, is located immediately above the keyboard.

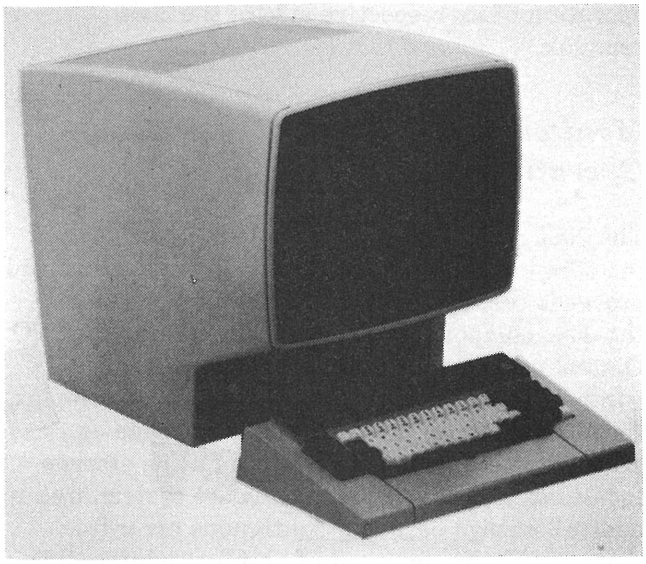


Figure 4-3. IBM 3278 Display Console Model 2A, the System Console

Service Support Consoles

Depending on the physical mode, one or both service support consoles (see Figure 4-1), which are similar to a 3278, are used by IBM service personnel for interaction with the service and support microcode. Each console, which can be used independent of and concurrent with user

operations, can also be used as a backup system console. Each can be attached to a channel (by means of an appropriate model of an IBM 3274 Control Unit) for running service and support programs such as the online test executive program (OLTEP).

A service control panel, located above each console, contains error indicators, system activation controls, and data entry and display facilities for IBM service personnel use. Each panel is used with the console to analyze and isolate malfunctions within the 3082 Processor Controller.

Optional Printers

One or two optional printers (IBM 3230 Printer Model 2, 3268 Printer Model 2, or 3287 Printer Model 1 or 2) can be attached to the 3082 for hard-copy output of complete display frames on either a service support console or a system console. For example, 3084 complex status, processor unit activity, error logs, or other diagnostic results can be printed. Each printer can be activated by function keys on either a service support console or a system console.

Optional Programming Support Console

One or two optional IBM 3278 Display Stations Model 2 can be attached to the processor controller as programming support consoles. If a console has the switch-control-unit feature and the switch is set for 3082 control, the 3278 may be used by IBM service personnel to access IBM FE RETAIN through an integrated remote support facility modem. When the switch is set for processor-unit control, the 3278 can be connected to a 3274 Control Unit and may be used as any other online display console that is attached by means of a channel.

Remote Support Facility Modems

The 3082 contains two integrated modems (one for each side) that provide data links used by IBM service personnel to communicate with the IBM Large Systems Support Center for remote maintenance assistance. For more information, see "Remote Servicing" under "Reliability, Availability, and Serviceability" in Chapter 2.

Integrated Processor Controller Files

The integrated processor controller files contain libraries essential to the function of the 3084 complex; the files include microcode libraries, UCWs, I/O-configuration and channel-path parameters, the Input/Output Configuration Program (IOCP), and error logs.

Chapter 5. 3084 Feature Descriptions

The features described in this chapter are organized into the following three groups:

- Features that depend on architectural mode (Figure 5-1)
- Features that provide programming assists (Figure 5-2)
- Features that do not depend on architectural mode (Figure 5-3)

Figures 5-1 and 5-2 indicate whether the feature is standard for the architectural mode, is a host-program feature, or is not implemented in the 3084. Additional information about the mode-dependent features (Figure 5-1) can be found in the following manuals:

- *IBM System/370 Principles of Operation,* GA22-7000
- *IBM System/370 Extended Architecture Principles of Operation,* SA22-7085
- *IBM System/370 Extended Architecture Interpretive Execution,* SA22-7095

Basic Control (BC) Mode

BC mode provides a PSW format that is compatible with the PSW format of System/360.

Bimodal Addressing

Bimodal addressing permits 31-bit logical addressing, yet allows users to continue running System/370 problem programs, which use 24-bit logical addresses.

Branch and Save

Branch and save provides the Branch and Save instruction (BAS and BASR).

Byte-Oriented Operand

Byte-oriented operand allows storage operands of most unprivileged instructions to appear on any byte boundary without causing a specification exception and a program interruption. This feature applies to fixed-point, floating-point, and logical operands. It does not apply to instruction addresses, privileged instructions, or channel command words (CCWs).

Channel Indirect Data Addressing

The addresses contained in channel command words (CCWs) in virtual storage must be translated by the control program before execution. Channel indirect data addressing allows immediately adjacent areas of virtual storage to be mapped into nonadjacent areas of absolute storage.

Feature	S/370 Native	S/370 (SIE) Guest	370-XA Native (Host)	370-XA (SIE) Guest
Basic-control (BC) mode	Standard	Standard	-, 1	-, 1
Bimodal addressing	-	-	Standard	Standard
Branch and save	Standard	Standard	Standard	Standard
Byte-oriented operand	Standard	Standard	Standard	Standard
Channel indirect data addressing	Standard	Host	Standard	Standard
Channel-set switching	Standard	Host	-, 2	-, 2
Channel subsystem	-	-	Standard	Standard
Clear I/O	Standard	Host	-, 2	-, 2
Command retry	Standard	Host	Standard	Standard
Conditional swapping	Standard	Standard	Standard	Standard
CPU timer and clock comparator	Standard	Standard	Standard	Standard
Extended-precision divide	-	-	Standard	Standard
Extended-precision floating point	Standard	Standard	Standard	Standard
Extended real addressing (26 bit)	Standard	Standard	-, 3	-, 3
Fast release	Standard	Host	-, 2	-, 2
Floating point	Standard	Standard	Standard	Standard
Halt device	Standard	Host	-, 2	-, 2
Interpretive execution (SIE)	-	-	Standard	Host
Interval timer	Standard	Standard	-	-
I/O extended logout	Standard	Host	-	-
Key-controlled storage protection	Standard	Standard	Standard, 4	Standard, 4
Limited channel logout	Standard	Host	-, 2	-, 2
Monitoring	Standard	Standard	Standard	Standard
Multiprocessing				
CPU-address identification	Standard	Host	Standard	Standard
CPU-signaling and response	Standard	Host	Standard	Standard
Prefixing	Standard	Host	Standard	Standard
TOD-clock synchronization	Standard	Host	Standard	Host
Page protection	-	-	Standard	Standard
PSW-key handling	Standard	Standard	Standard	Standard
Recovery extensions	Standard	Host	-	-
Segment protection	Standard	Standard	-, 5	-, 5
Service signal	Standard	Host	Standard	Host
Sorting instructions	-	-	Standard	Standard
Storage-key-instruction extensions	Standard	Standard	Standard	Standard
Storage-key instructions (ISK, SSK)	Standard	Standard	-, 4	-, 4
Storage-key 4K-byte block:				
Single-key 4K-byte blocks	Standard, 6	Standard	Standard	Standard
Storage-key exception control	Standard	Standard	-, 4	-, 4
System/370 extended:				
Non-MVS-dependent portion	Standard	Standard	Standard	Standard
System/370 I/O instructions (8)	Standard	Host	-, 2	-, 2
Test block	Standard	Standard	Standard	Standard
Time-of-day (TOD) clock	Standard	Standard	Standard	Standard
Tracing (ASN, branch, and explicit)	-	-	Standard	Standard
Translation:				
Dynamic address translation:				
2K-byte page size	No	No	-, 4	-, 4
4K-byte page size	Standard	Standard	Standard	Standard
64K-byte segment size	Standard	Standard	-	-
1M-byte segment size	No	Standard	Standard	Standard
Extended control (EC) mode	Standard	Standard	-, 1	-, 1
Program-event recording (PER)	Standard	Standard	Standard	Standard
Set-system-mask suppression	Standard	Standard	Standard	Standard
Store status	Standard	Standard	Standard	Standard
3033 extension:				
Dual-address space (DAS)	Standard	Standard	Standard, 8	Standard, 8
SIOF queuing	Standard	Host	-, 2	-, 2
Suspend and resume (9)	Standard	Host	-, 2	-, 2
31-bit IDAWs	Standard	Host	Standard	Standard
31-bit real addressing	-	-	Standard	Standard

Notes:

-	Not defined in the principles-of-operation manual for this architectural mode and therefore not implemented on the 3084.
Host	Host software determines whether or not this native function is simulated for the guest; direct interpretive execution does not occur.
No	Defined in the principles-of-operation manual for this architectural mode but not implemented on the 3084.
Standard	Implemented as a standard feature of the 3084 when operating in this architectural mode.
1	Operation in 370-XA mode is comparable to operation in EC mode of System/370.
2	Replaced by basic functions of the channel subsystem: channel-program compatibility with System/370 is maintained.
3	Replaced by 31-bit real addressing.
4	The storate-key instruction extensions provide the required function to manage the storage keys in 370-XA mode; System/370 instructions ISK, RRB, and SSK are not in 370-XA architecture.
5	Replaced by page protection.
6	Double-key 4K-byte blocks are not implemented on the 3084.
7	Does not include the Resume I/O instruction.
8	Does not include dual-address-space tracing; address-space-number (ASN) tracing provides a comparable function.
9	Includes the Resume I/O instruction.

Figure 5-1. Features That Depend On Architectural Mode

Feature	S/370 Native	370-XA (SIE) Guest	370-XA Native (Host)	370-XA (SIE) Guest
Control-switch assist	Standard	-	-, 1	-, 1
Preferred machine assist (PMA)	Standard	-	-, 1	-, 1
SIE assist	-	-	Standard	Host
System/370 extended facility				
MVS-dependent portion:				
4 lock-handling instructions	Standard	Standard	Standard	Standard
6 tracing instructions	Standard	Standard	-, 2	-, 2
Fix Page	Standard	Standard	-	-
SVC Assist	Standard	Standard	Standard	Standard
Add FRR	Standard	Standard	Standard	Standard
Page-fault assist	Standard	Standard, 3	-	-
VM assist for MVS/370 assists	Standard	Standard	-, 1	-, 1
Virtual-machine assist (VMA)	Standard	-	-, 1	-, 1
VM assists for CPU timer	Standard	-	-, 1	-, 1

Notes:

- Not defined in the principles-of-operation manual as a programming assist for this architectural mode and therefore not implemented on the 3084.

Host Host software determines whether or not this native function is simulated for the guest; direct interpretive execution does not occur.

Standard Implemented as a standard feature of the 3084 when operating in this architectural mode.

1 Interpretive execution (SIE) provides an alternative means of supporting execution of one or more guest operating systems.

2 370-XA tracing provides a comparable function.

3 Standard for preferred-storage-mode S/370 guest; not implemented for pageable-storage-mode S/370 guest.

Figure 5-2. Features That Provide Programming Assists

Feature	Availability
Channel-to-channel adapters, A-side	Optional (As many as two)
Channel-to-channel adapters, B-side	Optional (As many as two)
Channels (six groups)	Standard
Data streaming	Standard
Error checking and correction	Standard
High-speed buffer storage	Standard
I/O error alert	Standard
I/O power sequence control (each side)	Standard (For 1st to 32nd control unit)
I/O power sequence control, A-side	Optional (For 33rd to 64th control unit)
I/O power sequence control, B-side	Optional (For 33rd to 64th control unit)
Performance improvement	Optional (On Model Q)
Processor checkpoint retry	Standard
Storage configuration control	Standard

Figure 5-3. Features That Do Not Depend On Architectural Mode

Channel-Set Switching

Channel-set switching permits program-controlled switching of channel sets between two central processors on the A-side or B-side of a partitioned 3084 complex so that if one processor fails, either channel set may be assigned to the other processor.

Channel Subsystem

The 370-XA channel subsystem queues I/O requests, selects from as many as four channel paths to any I/O device, and handles I/O-busy conditions. In a partitioned 3084 complex, each external data controller (EXDC) operates as a channel subsystem having as many as 24 channel paths. In a single-image 3084 complex, both EXDCs operate as one channel subsystem having 48 channels. Thirteen 370-XA I/O instructions are associated with the channel subsystem.

Channel-to-Channel Adapters (A-Side and B-Side)

A channel-to-channel adapter provides the control-unit function for two loosely coupled processors. To interconnect two processors, one adapter is required. The data transfer rate is at the speed of the slower of the two attached channels. One or two A-side and B-side channel-to-channel adapters are available as optional features for the A-side and the B-side, respectively, of the 3082 Model Q48 or X48.

Channels (Six Groups)

The 3084 has 48 integrated channels (six groups)—24 in each external data controller (EXDC). All the channels can be assigned for block-multiplexer operation, or as many as eight channels (four in each EXDC) can be assigned for byte-multiplexer operation. (See "External Data Controller" in Chapter 3 for more information about channels.)

Clear I/O

Clear I/O provides the clear I/O function in a channel when the privileged Clear I/O (CLRIO) instruction is executed. The clear I/O function causes a channel to discontinue its current I/O operation with an addressed I/O device by storing the status of the operation in the channel status word (CSW) and by making the associated subchannel available.

Command Retry

Command retry allows a subchannel to retry a command without causing an I/O interruption. The retry is initiated by a control unit.

Conditional Swapping

Conditional swapping makes available the instructions Compare and Swap (CS) and Compare Double and Swap (CDS).

Control-Switch Assist

Control-switch assist (CSA), an extension for preferred-machine assist, increases the speed with which interruptions on CP-owned channels are presented to a preferred virtual machine and adds several functions, including the use of the virtual machine communication facility (VMCF).

CPU Timer and Clock Comparator

The CPU timer of each central processor is a high-resolution timer that causes an interruption whenever its value is negative. The interruption request is allowed by setting bit 21 in control register 0 and the external mask bit in the PSW.

The timer measures central-processor elapsed time and causes an interruption at the end of the period that is specified by the program. The timer is decremented when the central processor is executing instructions and during the wait state but is not decremented when the central processor is in the stopped state. The program can initiate inspection of the CPU timer by using the Store CPU Timer (STPT) instruction and can set the timer to a specific value by using the Set CPU Timer (SPT) instruction. The contents of the CPU timer are reset to 0 by an initial CPU reset.

Note: When the TOD clock is in the stopped or error state, the CPU timer is not decremented.

The clock comparator of each central processor provides for an interruption when the time-of-day (TOD) clock reaches a value specified by the program. The interruption is allowed when the central processor sets bit 20 in control register 0 and the external mask bit in the PSW.

The format of the clock comparator is the same as that of the TOD clock. A clock-comparator interruption is an external interruption. The program can initiate inspection of the clock comparator by using the Store Clock Comparator (STCKC) instruction and can set it by using the Set Clock Comparator (SCKC) instruction. The contents of the clock comparator are reset to 0 by an initial CPU reset.

Note: When the TOD clock is in the stopped or error state, the clock comparator is not operating.

Data Streaming

Data streaming is available on all block-multiplexer channels. It permits higher data rates (up to 3 megabytes per second) and longer cable lengths. For control units that operate in data-streaming mode, the cable between the 3082 and a control unit can be as long as 122 meters (400 feet). Data streaming is initiated by the control unit. The EXDC permits the intermixed attachment of data-streaming and non-data-streaming devices on the same channel.

Error Checking and Correction

Data paths between central storage and the channels and central processors are checked for parity.

Error checking and correction (ECC) code bits are stored with the data in the central storage data arrays. ECC codes apply to data stored in and fetched from central storage; single- and multiple-bit error detection and single-bit error correction are performed.

Extended-Precision Divide

Extended-precision divide provides the Divide (DXR) instruction for extended-precision floating-point operands.

Extended-Precision Floating Point

Extended-precision floating point provides the seven floating-point instructions that use the extended-precision format (a signed seven-bit characteristic and a 28-digit fraction).

Extended Real Addressing

Extended real addressing permits the addressing of real storage in excess of 16M bytes. MVS/SP and VM/SP-HPO use extended real addressing for locating user programs and portions of the control program in central storage at real addresses up to 32M bytes (with MVS/SP Version 1 Release 3) or 64M bytes (with VM/SP-HPO Release 2.5). Extended real addressing does not affect virtual addressability, which may not exceed 16M bytes.

Fast Release

Fast release provides the start-I/O-fast-release function on a channel when the Start I/O Fast Release (SIOF) instruction is executed. This function provides for early release of the central processor that executes the instruction. Fast release occurs before the delay-selection procedure is completed, thereby reducing the central-processor delay associated with the operation.

Floating Point

Floating point provides the floating-point instructions and the floating-point registers. In System/370, floating point combined with the commercial instruction set is sometimes referred to as the System/370 universal instruction set.

Halt Device

Using the privileged Halt Device (HDV) instruction, the halt-device function signals the addressed I/O device to terminate its current I/O operation.

High-Speed Buffer Storage

High-speed buffer storage in each central processor satisfies many storage fetch requests, making the effective storage access time much shorter than the actual central storage cycle time. (For more information, see "Buffer Control Element" in Chapter 3.)

Interpretive Execution

The interpretive execution facility is used by the VM/XA Migration Aid and provides hardware support for several areas of virtual machine operation, such as interval timer operation, prefixing, address translation, and privileged instruction handling. This facility provides the Start Interpretive Execution (SIE) instruction, which the VM/XA Migration Aid uses to dispatch all virtual machines. (For more information, see *IBM System/370 Extended Architecture Interpretive Execution,* SA22-7095.)

Interval Timer

The interval timer of each central processor provides external interruptions on a program-controlled basis. The value stored at a specified storage location is automatically decremented by 1 in bit-position 23 every 3.33 milliseconds. The program receives an external interruption request when the interval timer decrements from 0 to a negative value. (Bit 7 of the PSW and bit 24 of control register 0 must be on.) The range of the interval timer is approximately 15.5 hours.

Note: When the TOD clock is in the stopped or error state, the interval timer is not operating.

I/O Error Alert

I/O error alert permits a channel to be alerted when a malfunction affects the ability of a control unit to continue operating.

I/O Extended Logout

I/O extended logout provides for the storing of detailed channel-error information in a storage area designated by a pointer.

I/O Power Sequence Control (A-Side and B-Side)

I/O power sequence control permits the 3084 to sequence power (for power on or power off) for as many as 32 control units. If more control units are needed, a second I/O power sequence control is optionally available to provide power-on and power-off control for as many as 32 more control units on the A-side and B-side, respectively, of a 3084 complex.

Key-Controlled Storage Protection

Key-controlled storage protection prevents unauthorized access to information in central storage. Both store protection and fetch protection are included. If store protection is violated, data is not stored into the protected area; if fetch protection is violated, data is not retrieved from the protected area. When a violation is recognized, a program interruption occurs. (See "Central Storage" in Chapter 3 for more information.)

Limited Channel Logout

Limited channel logout provides four bytes of channel-status information for model-independent recovery from channel errors.

Monitoring

Monitoring provides a means of selectively recording designated events in the execution of a program. This facility is implemented by the use of the Monitor Call (MC) instruction.

Multiprocessing

With the four central processors in a 3084, multiprocessing permits a multiprocessing configuration. Multiprocessing includes the following:

- CPU-address identification
- CPU signaling and response
- Prefixing
- Shared main storage
- TOD-clock synchronization

CPU-Address Identification

CPU-address identification provides an address by which each of the four central processors can be identified by the Signal Processor (SIGP) instruction. It also provides new external-interruption conditions and the Store CPU Address (STAP) instruction, by which the control program can determine the address of a central processor.

CPU Signaling and Response

CPU signaling and response provides for communication between the four central processors. This feature provides the Signal Processor (SIGP) instruction and the mechanism to interpret and act on several order codes, such as sense, stop, and restart.

Prefixing

For each central processor, prefixing provides a means of assigning real addresses 0 through 4095 to two or more different 4K-byte blocks of central storage. In a 3084, in which as many as four central processors share central storage (represented by a single contiguous range of absolute addresses), one area is assigned to each central processor.

Shared Main Storage

Shared main storage permits as many as four central processors to have access to common main-storage locations.

TOD-Clock Synchronization

TOD-clock synchronization provides a uniform appearance to a clock-synchronization program in all 3081, 3083, and 3084 Processor Complexes, allowing the program to be independent of the actual number of TOD clocks and central processors in a configuration. The feature includes a TOD-clock-synchronization control bit in control register 0.

Page Protection

Page protection provides protection against improper storing by controlling access to virtual storage through the use of the page protection bit in each page table entry.

Performance Improvement

Performance improvement (optional) provides a 24.5-ns basic machine cycle time (instead of 26 ns) for 3084 Model Q. The performance improvement feature must be installed on both sides of the 3084 Processor Unit Model Q and on both sides of the associated 3082 Processor Controller.

Preferred Machine Assist

Preferred machine assist permits a single MVS/SP virtual-equals-real (V=R) virtual machine operating under VM/SP-HPO to operate with a minimum of simulated instruction execution, thereby allowing it to achieve near native performance. With preferred machine assist, any MVS/SP release that supports more than 16M bytes of real storage can use real storage above 16M bytes when operating as a V=R virtual machine.

Processor Checkpoint Retry

Processor checkpoint retry (CPU retry) is an error recovery procedure that corrects intermittent central-processor errors by saving pertinent data between predetermined checkpoints. If an error occurs, reexecution of the instruction sequence from the last checkpoint is performed. (For more information about this feature, see "Processor Checkpoint Retry" in Chapter 2.)

PSW-Key Handling

PSW-key handling provides the instructions Set PSW Key from Address (SPKA) and Insert PSW Key (IPK).

Recovery Extensions

Recovery extensions consist of:

- The clear channel function in a channel, which can be used to perform an I/O-system reset in a channel when the Clear Channel (CLRCH) instruction is executed.
- Machine-check extensions, which include a machine-check external damage-code validity bit and which provide a detailed indication of the cause of external damage.
- Limited channel logout extensions, which consist of two additional logout bits, to indicate whether the I/O interface is operative and whether the logout is valid.

Segment Protection

Segment protection provides protection against improper storing by controlling access to virtual storage through the use of the segment protection bit in each segment-table entry.

Service Signal

Service signal provides an external interruption that is used by the 3082 Processor Controller to signal information to the control program.

SIE Assist

Start interpretive execution (SIE) assist improves the performance of virtual equals real (V=R) guests. Most I/O instructions and associated interruptions are handled without leaving interpretive execution mode.

Sorting Instructions

The sorting instructions are designed to improve sort performance. These instructions are used by the IBM Program Product Data Facility Sort (DFSORT) Release 7 and later releases running under MVS/XA when sorting fixed-length records by means of the blockset sort method.

Storage Configuration Control

The address ranges of the data arrays in a basic storage module are assigned as part of system initialization. If a storage module has an error after processor-unit initialization, the module can be removed from the operational configuration.

Storage-Key Instruction Extensions

The storage-key instruction extensions provide the Set Storage Key Extended (SSKE), Insert Storage Key Extended (ISKE), and Reset Reference Bit Extended (RRBE) instructions, which provide 31-bit addresses and operate on the storage key associated with each 4K-byte block of storage.

Storage-Key Instructions

The storage-key instructions Set Storage Key (SSK) and Insert Storage Key (ISK) allow initialization and inspection of the storage key associated with each block of storage that is available in the configuration.

Storage-Key 4K-Byte Block

Storage-key 4K-byte block allows a single key to be associated with each 4K-byte block of storage and, in S/370 mode, provides the storage-key exception control bit in control register 0.

System/370 Extended Facility (MVS-Dependent Portion)

The MVS-dependent portion of the System/370 extended facility consists of:

- SVC Assist instruction, which improves central processor performance by reducing the time needed to enter MVS supervisory services
- Fix Page instruction, Add FRR instruction, six tracing instructions, and four lock-handling instructions, which improve central-processor performance
- Page-fault assist, which improves MVS performance by directly assigning and initializing a page frame when a page-translation exception is recognized on first reference to certain virtual pages

In addition, in S/370 mode, the System/370 extended facility provides VM assists for MVS/370 assists. For virtual machines, these VM assists perform functions that are identical to functions of corresponding MVS assists for real machines.

System/370 Extended Facility (Non-MVS-Dependent Portion)

The non-MVS-dependent portion of the System/370 extended facility consists of:

- Low-address protection, which improves system integrity by providing special protection for storage (at effective addresses 0 through 511) that is vital to the control program
- Invalidate Page Table Entry (IPTE) instruction and the common-segment bit, which increase the efficiency of dynamic address translation

- Test Protection (TPROT) instruction, which performs tests for potential protection violations without causing program interruptions for protection exceptions

System/370 I/O Instructions

The I/O instructions used in S/370 mode are:

- Clear Channel (CLRCH)
- Clear I/O (CLRIO)
- Halt Device (HDV)
- Halt I/O (HIO)
- Start I/O (SIO)
- Start I/O Fast Release (SIOF)
- Store Channel ID (STIDC)
- Test Channel (TCH)
- Test I/O (TIO)

Another I/O instruction, Resume I/O (RIO), is provided by suspend and resume, which is described under "3033 Extension" in this chapter.

Test Block

Test block provides the Test Block (TB) instruction for testing the usability of a 4K-byte block of central storage.

Time-of-Day Clock

The time-of-day (TOD) clocks provide a consistent measurement of elapsed time that can be used for indicating the time of day.

Each TOD clock is initialized by execution of the Set Clock (SCK) instruction by a central processor. The clock is incremented every 125 nanoseconds by an 8-MHz clock line. It provides resolution to a single machine cycle with additional low-order bits, and has a nominal oscillator tolerance of ± 160 Hz.

Bit assignments are:

- Bits 0-54 increment at an 8-MHz rate.
- Bits 56-58 increment every machine cycle to provide cycle-by-cycle resolution.
- Bit 59 is 0 for the A-side clock and 1 for the B-side clock.
- Bit 61 is on for the first Store Clock (STCK) instruction after initialization of the TOD clock by the control program.
- Bits 62 and 63 show the TOD-clock state.

In a 3084, bits 55 and 60 are 0.

Tracing

Tracing provides three aids for problem-program analysis:

- Address-space-number (ASN) tracing
- Branch tracing
- Explicit tracing

Translation

Translation includes the following five features:

- Dynamic address translation
- Extended control mode
- Program-event recording
- Set-system-mask suppression
- Store status

As part of these features, translation also provides the following instructions:

- Load Real Address (LRA)
- Purge TLB (PTLB)

- Reset Reference Bit (RRB)
- Store Then AND System Mask (STNSM)
- Store Then OR System Mask (STOSM)

Dynamic Address Translation

Dynamic address translation (DAT) provides hardware translation of virtual addresses to real addresses during program execution. DAT supports real storage sizes up to 64M bytes in S/370 mode and 128M bytes in 370-XA mode. The 3084 uses 4K-byte pages and either 64K-byte segments (in S/370 mode) or 1M-byte segments (in 370-XA mode).

An S/370-mode interpretively executed guest virtual machine can additionally use the 1M-byte segment size.

Extended Control (EC) Mode

When the 3084 operates in EC mode, virtual storage and high-speed DAT are available. (See "Central Processor" in Chapter 3 for more information.)

Program-Event Recording

Program-event recording (PER) assists in debugging programs. During program execution, PER can monitor the following actions:

- Successful branches
- Alteration of general registers
- Instruction fetches from a specified storage area
- Alteration of a specified storage area

Set-System-Mask Suppression

Set-system-mask suppression permits suppression of execution of the Set System Mask (SSM) instruction and provides the special-operation program interruption code.

Store Status

Store status is an operator-initiated function that places the contents of the current PSW and the program-addressable registers in permanently assigned, real-address locations within the first 512 bytes of central storage. Store status also includes a noninitializing manual reset function.

Virtual-Machine Assist

Virtual-machine assist (VMA), which is a programming assist for Virtual Machine/System Product-High Performance Option (VM/SP-HPO), directly executes 15 virtual-machine instructions (including the ISKE, SSKE, and RRBE instructions) and validates page-table entries in the shadow tables. VMA improves performance on virtual-storage systems operating under VM/SP-HPO by reducing the amount of time VM/SP-HPO spends in the real supervisor state. The reduction is achieved by emulation (instead of software simulation) of certain privileged operation codes used by the virtual-storage (guest) control program.

VM Assists for the CPU Timer

VM assists for the CPU timer permit a central processor to directly execute the Set CPU Timer (SPT) and Store CPU Timer (STPT) instructions for a virtual machine operating under VM/SP-HPO.

3033 Extension

The 3033 extension provides:

- Dual-address space
- Start-I/O-fast queuing
- Suspend and resume

All three are supported in S/370 mode by MVS/SP Version 1 Release 3; dual-address space is also supported in 370-XA mode by MVS/SP Version 2.

Dual-Address Space

Dual-address space aids communication between virtual address spaces. It provides:

- Twelve additional instructions
- Two address spaces for immediate use by a program
- A means of changing to other spaces
- A table-based subroutine linkage
- The use of multiple access keys for key-controlled protection by problem programs
- Aids for problem-program analysis (S/370 mode only)

In 370-XA mode, the tracing facility provides an alternative set of aids.

Start-I/O-Fast Queuing

Start-I/O-fast queuing allows a Start I/O Fast Release (SIOF) instruction to complete execution independent of device selection or a channel-busy condition. Control-unit or device busy conditions encountered subsequent to execution of an SIOF instruction cause the I/O operation to remain pending until facilities are available for initiation of the operation at the device.

Suspend and Resume

Suspend and resume provides:

- The suspend flag in the channel command word (CCW), which indicates that execution of a channel program is to be suspended
- A channel-address-word (CAW) bit that controls whether the CCW's suspend flag should cause suspension of execution of a channel program
- A channel-status-word (CSW) bit that indicates that execution of a channel program has been suspended
- The Resume I/O (RIO) instruction, which causes resumption of execution of a suspended channel program

31-Bit Indirect-Data-Address Word

The 31-bit indirect-data-address word (IDAW) extends the size of the address field in IDAWs to 31 bits.

31-Bit Real Addressing

Thirty-one-bit real addressing ensures that certain fields contain 31-bit real addresses regardless of the setting of the addressing-mode control bit in the PSW.

Appendix A. 3084 Deviations

The following information describes 3084 deviations from the *IBM System/370 Principles of Operation,* the *IBM System/370 Extended Architecture Principles of Operation,* and the *IBM System/360 and System/370 I/O Interface Channel to Control Unit OEMI.*

Change Bit

(Both Principles of Operation)

When a 3084 Processor Unit performs a store access, it always turns on the change bit in the associated key concurrent with the access. The 3084 is granted a deviation that permits it to turn on a change bit without storing, provided that no store-access exceptions would have occurred if the store had taken place.

Channel-to-Channel Adapter Internal Resistance

(I/O Interface OEMI)

The maximum allowable internal resistance contributed by a control unit for every signal line of the I/O interface is 1.0 ohm. The 3084 deviates from this requirement in that the resistance contributed to an I/O interface by a channel-to-channel adapter feature may be up to 3.0 ohms.

Connect Channel Set Condition Code

(System/370 Principles of Operation)

When a channel set is connected to a central processor and the central processor becomes not operational because of program reconfiguration, a subsequent Connect Channel Set (CONCS) instruction which addresses that channel set sets condition code 1 (channel set connected to another central processor), giving the appearance of connection to a not-operational central processor, which is a deviation from the *System/370 Principles of Operation.* The Disconnect Channel Set (DISCS) instruction executed under the same circumstances sets condition code 3 (channel set not operational), as allowed by the *System/370 Principles of Operation.*

Delayed Bit

(System/370 Principles of Operation)

The *IBM System/370 Principles of Operation* specifies that the delayed bit is set to 1 when a machine-check condition is delayed in being reported because the CPU is disabled for machine-check interruptions at the time the condition occurs. The 3084 deviates from this by always turning on the delayed bit in the machine-check interruption code for repressible machine-check interruptions even though the CPU is enabled for that type of interruption at the time the condition occurs.

Multiple Copies of Storage Keys

(Both Principles of Operation)

Multiple copies of each storage key can be maintained if the following conventions (which limit the effects these copies may have on a program) are observed:

- Many copies of a storage key may appear to be associated with a particular 4K-byte block of storage; the copies are not associated with a particular central processor or with a particular address within the block.
- A central processor or channel program accessing central storage chooses one of the copies of the storage key and uses it.
- The Set Storage Key (SSK) and Set Storage Key Extended (SSKE) instructions place the operand into *each* copy of the designated storage key. The changes to the various copies are not necessarily performed concurrently, as viewed by channel programs and other central processors. However, all bits of a particular copy of the key are updated

concurrently, as viewed by channel programs and other central processors. The changes to the key obey the same sequencing conventions that are applicable to storage-operand store references. If more than one central processor executes an SSK or SSKE to the same block at the same time, one central processor completes the SSK or SSKE operation before any other begins.

- The Insert Storage Key (ISK) and Insert Storage Key Extended (ISKE) instructions fetch bits 0-4 of any one of the copies of the designated storage key and places them into bit positions 24-28 of the register designated by the R_1 field. In EC mode, the logical OR of the reference bits and the logical OR of the change bits from each copy of the storage key are placed into bit positions 29 and 30, respectively.

  If an SSK or SSKE is in progress on another central processor at the same time, ISK or ISKE obtains the values of bits 0-4 of the storage key existing at one time, either before or after the SSK or SSKE. However, the reference and change bits, bits 29 and 30, may appear to be fetched at different times, either before or after the SSK or SSKE, independent of each other and of the fetching of bits 24-28.

- If an ISK or ISKE is executed concurrent with a Reset Reference Bit (RRB) or a Reset Reference Bit Extended (RRBE) to the same block, bit position 29 appears to be set with the value of the reference bit before the RRB or RRBE, or 0.

- The RRB and RRBE instructions set the condition code as follows:

  0 All reference bits 0, all change bits 0
  1 All reference bits 0, at least one change bit 1
  2 At least one reference bit 1, all change bits 0
  3 At least one reference bit 1, at least one change bit 1

  For each copy of the designated storage key, RRB and RRBE fetch the reference and change bits (to determine the condition-code setting) and sets the reference bit to 0. The operations on the various copies are not necessarily performed concurrently, as viewed by channel programs and other central processors. For example, another central processor may concurrently execute an SSK or SSKE, causing the final value of each reference bit to be either that from the SSK or SSKE, or 0 (but not necessarily all the same). When the final values of the reference bits are from the SSK or SSKE, or are 0, the condition-code setting by RRB or RRBE appears to be derived from the values of the change and reference bits before or after the SSK or SSKE.

- The Test Protection (TPROT) instruction and the Insert Virtual Storage Key (IVSK) instruction provide information by fetching any one of the copies of the designated storage key.

In each of the preceding examples, the access to a copy of a storage key follows the same sequencing conventions applicable to a storage operand of the same type.

Nonzero Bus-Out during Stop Sequence Control

(I/O Interface OEMI)

During a stop sequence control, 3084 channels do not ensure that bus-out contains all 0's.

Prefixing of DAT Table Entries

(System/370 Principles of Operation)

Dynamic-address-translation table entries can be accessed in the process of dynamic address translation without applying prefixing and reverse prefixing to the storage addresses of the table entries.

Test Channel Condition Code

(System/370 Principles of Operation)

A byte-multiplexer channel operating in burst mode responds available (condition code 0) to a Test Channel (TCH) instruction.

Glossary of Terms and Abbreviations

Refer to *IBM Vocabulary for Data Processing, Telecommunications, and Office Systems,* GC20-1699, for terms that do not appear in this glossary.

absolute address. An address that identifies a storage location without the use of any intermediate reference.

address. An identification of a storage location or an I/O device.

address translation. See *dynamic address translation.*

ASN. Address-space number.

BC mode. Basic control mode.

BCE. Buffer control element.

BSE. Basic storage element.

BSM. Basic storage module.

CAW. Channel address word.

CCW. Channel command word.

CDU. Coolant distribution unit.

central storage. In the 3084 complex, central storage consists of shared main storage and a hardware system area. In a partitioned 3084 complex, central storage is divided into two equal parts, each of which has a hardware system area.

CPE. Channel processing element.

CPU. Central processing unit.

CSE. Control storage element.

CSW. Channel status word.

DAT. See *dynamic address translation.*

DSE. Data server element.

dynamic address translation (DAT). (1) The process of changing a virtual storage address to a real storage address during execution of an instruction. (2) A hardware feature that performs the translation.

EC mode. See *extended control mode.*

ECC. Error checking and correction.

EE. Execution element.

EXDC. External data controller.

extended control mode. A mode in which all the features of a System/370 model, including dynamic address translation, are operational.

FCC. Federal Communications Commission.

FE. Field Engineering.

FE RETAIN. A remote technical assistance and information network that provides data base and data link support for the IBM Field Engineering (FE) Division.

FRU. Field-replaceable unit.

G-byte. 1,073,741,824 bytes of storage capacity.

guest. In interpretive execution mode, the interpreted or virtual machine as opposed to the real machine (the host).

hardware system area. That part of central storage that is reserved for system usage and is not program addressable.

high-speed buffer. A 64K-byte high-speed store-in buffer (one for each central processor).

host. In interpretive execution mode, the real machine as opposed to the virtual or interpreted machine (the guest).

Hz. Hertz.

IAE. Interface adapter element.

ID. Identifier.

IE. Instruction element.

IML. Initial microprogram load.

in. inch.

initialization. To set counters, switches, addresses, latches, or storage contents to 0 or to other starting values at the beginning of, or at the prescribed points in, a computer program or process.

I/O. Input/output.

IOCP. Input/Output Configuration Program, which defines I/O configuration parameters needed for the EXDC to function.

IPL. Initial program load.

K-byte. 1,024 bytes of storage capacity.

LRU. Least recently used.

main storage. That part of central storage that is program addressable.

M-byte. 1,048,576 bytes of storage capacity.

MHz. Megahertz.

microsecond. One millionth of a second.

mm. Millimeter.

MSSF. Monitoring and system support facility.

MVS/SP. Multiple Virtual Storage/System Product.

nanosecond. One thousandth of a microsecond.

ns. Nanosecond.

OEMI. Original equipment manufacturers' information.

OLTEP. Online test executive program.

PER. Program event recording.

port. An access point for data entry or exit.

PSW. Program status word.

RAS. Reliability, availability, and serviceability.

real address. The address of a location in real storage.

RETAIN. See *FE RETAIN.*

RR. Register-and-register operation.

RRE. Register-and-register operation having an extended operation-code field.

RS. Register-and-storage operation.

RX. Register-and-indexed-storage operation.

S. Storage operation using an implied operand and storage.

SAD frame. SYSTEM ACTIVITY DISPLAY frame.

SI. Storage-and-immediate operation.

SIE. Start interpretive execution.

SS. Storage-and-storage operation.

SSE. Storage-to-storage operation having an extended operation-code field.

S/370. System/370

TCM. Thermal conduction module.

thermal conduction module (TCM). Helium-filled, encapsulated module containing multiple logic chips mounted on a multilayered ceramic substrate; used to implement the logic circuitry of the 3084 Processor Unit.

TLB. Translation lookaside buffer (sometimes referred to as a directory lookaside table, or DLAT).

TOD clock. Time-of-day clock.

UCW. Unit control word.

V = R. Virtual equals real.

VFE. Variable field element.

virtual address. An address that refers to virtual storage and that must be translated into a real storage address when it is to be used.

VMA. Virtual machine assist.

VM/SP. Virtual Machine/System Product

VM/SP-HPO. Virtual Machine/System Product - High Performance Option.

VM/XA. Virtual Machine/Extended Architecture.

volatile storage. Storage that does not retain stored data after power is removed.

| **370-XA.** System/370 extended architecture.

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Bibliography

The following publications provide additional information about 3084 Processor Complex functions and operation:

GA22-6974 *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information*

GA22-7000 *IBM System/370 Principles of Operation*

GA22-7001 *IBM System/370 System Summary: Processors*

GA22-7002 *IBM System/370 Input/Output Configurator*

GA22-7077 *IBM 3081, 3083, and 3084 Channel Characteristics and Configuration Guide*

SA22-7085 *IBM System/370 Extended Architecture Principles of Operation*

SA22-7095 *IBM System/370 Extended Architecture Interpretive Execution*

GA32-0039 *IBM Input/Output Device Summary*

GC22-7004 *IBM System/370 Installation Manual—Physical Planning*

GC28-1027 *Input/Output Configuration Program User's Guide and Reference*

GC38-0037 *IBM 3084 Operator's Guide for the System Console* (for 3084 operation in single-image mode)

GC38-0035 *IBM 3081, 3083, and 3084 Messages for the System Console*

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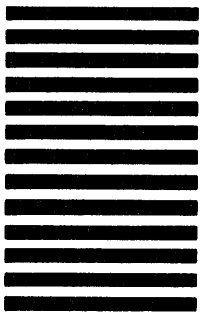

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