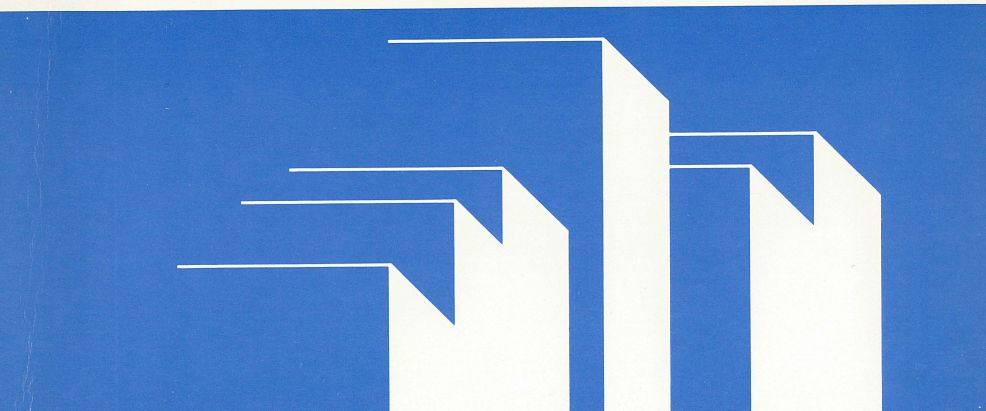
Publication Number
GA22-7083-3

IBM 3083

Functional Characteristics



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Publication Number
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Fourth Edition (May 1984)

This major revision obsoletes GA22-7083-2. This edition adds information about the performance feature for the IBM 3083 Processor Unit Models E, B, and J. Changes or additions to the text and illustrations are indicated by a vertical line to the left of the change.

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Preface

This manual, which is intended for management, programming, and operations personnel, describes the components and functions of the IBM 3083 Processor Complex improved models (EX, BX, and JX) and base models (E, B, and J). Readers of this manual should:

- Be familiar with system architecture as defined in the *IBM System/370 Principles of Operation,* GA22-7000, and the *IBM System/370 Extended Architecture Principles of Operation,* SA22-7085.
- Have a knowledge of virtual-storage and virtual-machine concepts. Other publications that should be used in addition to this manual are listed in the "Bibliography."

This manual contains five chapters and one appendix.

Chapter 1 introduces and summarizes the IBM 3083 Processor Complex.

Chapter 2 describes the structure and implementation of the 3083 Processor Complex.

Chapter 3 describes the functions of the IBM 3083 Processor Unit components.

Chapter 4 describes the IBM 3082 Processor Controller.

Chapter 5 describes the basic, standard, and optional features.

Appendix A contains deviations from the *IBM System/370 Principles of Operation,* the *IBM System/370 Extended Architecture Principles of Operation,* and the *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information,*GA22-6974.

This manual also contains a glossary of terms and abbreviations and a bibliography.

In this manual, all references to the 3083 Processor Complex, 3083 Processor Unit, or 3082 Processor Controller apply to both the improved models and the base models, unless indicated otherwise.

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Contents

Chapter 1. Introduction

The IBM 3083 Processor Complex (Figure 1-1) is an upward extension of System/370 for high-speed, large-scale, general-purpose computation.

Design Highlights

The design of this high-performance processor complex incorporates:

- System/370 extended architecture (370-XA)
- Two architectural modes of operation
- An external data controller (EXDC)
- Thermal conduction modules (TCMs)

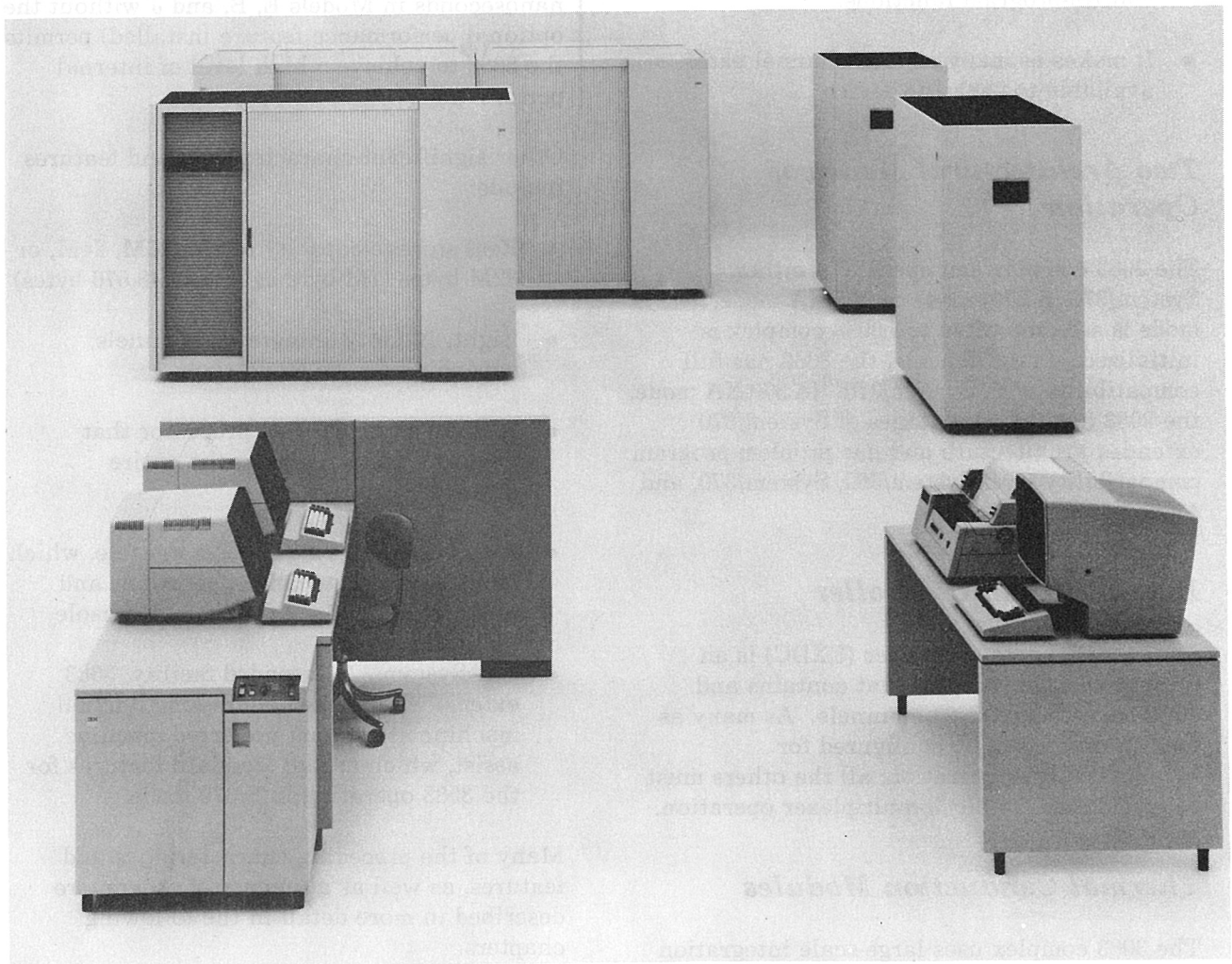


Figure 1-1. IBM 3083 Processor Complex with Other Devices (Design Models)

System/370 Extended Architecture (370-XA)

An evolutionary extension of System/370 architecture, 370-XA adds a number of functional enhancements. For example:

- It permits 31-bit addressing, yet allows users to continue running System/370 problem programs, which use 24-bit addresses.
- It makes channel-path selection and I/O-busy-condition management be hardware functions rather than control-program functions.
- It makes as many as four channel paths available to each I/O device.

Two Architectural Modes of Operation

The 3083 complex can operate in either System/370 (S/370) mode or 370-XA mode. The mode is selected when the 3083 complex is initialized. In S/370 mode, the 3083 has full compatibility with System/370. In 370-XA mode, the 3083 has the advantages of System/370 extended architecture and has problem-program compatibility with System/360, System/370, and 4300 processors.

External Data Controller

The external data controller (EXDC) is an integrated I/O processor that contains and controls as many as 24 channels. As many as four channels can be configured for byte-multiplexer operation; all the others must be configured for block-multiplexer operation.

Thermal Conduction Modules

The 3083 complex uses large-scale integration that permits as many as 133 high-density silicon chips to be mounted on a multilayered ceramic substrate in a helium-filled module called a *thermal conduction module* (TCM). TCMs plug into a supporting multilayered circuit board. The use of TCMs and the boards, which are designed to eliminate module-to-module external wiring, significantly reduces requirements for cabling, power, space, and cooling, while enhancing reliability.

Other Highlights

The basic machine cycle time (24 nanoseconds in Models EX, BX, and JX, 24.5 nanoseconds in Models E, B, and J with the optional performance feature installed, and 26 nanoseconds in Models E, B, and J without the optional performance feature installed) permits the 3083 to achieve a high level of internal performance.

Other significant characteristics and features include:

- Real storage capacity of 8M, 16M, 24M, or 32M bytes (1M byte equals 1,048,576 bytes)
- Eight, 16, or 24 integrated channels, depending on the model
- A stand-alone support processor that monitors and supervises the entire processor complex
- A dedicated service support console, which facilitates maintenance operations and provides backup for the system console
- The System/370 extended facility, 3033 extension, extended addressing, virtual machine assist, and preferred machine assist, which are all standard features for the 3083 operating in S/370 mode.

Many of the preceding characteristics and features, as well as a number of others, are described in more detail in the following chapters.

The 3083 complex may operate in either a stand-alone configuration or loosely coupled with other IBM processors (including System/360, System/370, 308X, and 4300).

Programming Support

Programming support is mode dependent. For example, to operate in 370-XA mode, a 3083 requires a 370-XA-mode control program.

Programming support for the 3083 complex includes:

Control Programs	In S/370 Mode	In 370-XA Mode
MVS/SP Version 1 Release 1 Enhancement	All models	–
MVS/SP Version 2	–	All models
VM/SP with VM/SP High Performance Option (VM/SP-HPO) Release 2	All models	–
VM/XA Migration Aid	–	All models

Most existing S/370-mode application (problem) programs can operate without alteration under 370-XA-mode control programs. This ability is primarily due to:

- The System/370 nonprivileged instructions being a subset of the 370-XA instruction set
- Addressing in 370-XA mode providing for use of either 24-bit or 31-bit addresses, as determined by the control program

Compatibility

Any program written to operate in S/370 mode or 370-XA mode can run on any 3083 operating in that mode, if the program:

- Is not time dependent
- Does not depend on the presence of system facilities (such as storage capacity, I/O equipment, or optional facilities) when the facilities are not included in the configuration
- Does not depend on the absence of system facilities when the facilities are included in the configuration. For example, the program must not depend on interruptions caused by invalid operation codes for instructions that are not present on some models but are present on the 3083
- Does not depend on results or functions that are defined in the appropriate principles-of-operation manual as being unpredictable or model dependent, or as affecting compatibility
- Does not depend on results or functions that are defined in this manual as deviations from the appropriate principles-of-operation manual. (See Appendix A for descriptions of deviations.)

Any 3083 operating in 370-XA mode can run any problem program written for System/360, System/370, or 4300 processors if the program:

- Does not violate the first four of the preceding conditions
- Does not depend on control-program facilities that are not available on the 3083

In S/370 mode, two functions of the 3083 differ somewhat from those of some earlier IBM processors:

- In dynamic address translation, the 3083 uses only 64K-byte segments and 4K-byte pages (not 1M-byte segments or 2K-byte pages)

  Note: A S/370-mode interpretively executed guest virtual machine can use the 1M-byte segments. See Chapter 5 for additional information.

- In key-controlled storage protection, the 3083 uses only 4K-byte keys (not 2K-byte keys)

For more details about compatibility, see the appropriate principles-of-operation manual.

Chapter 2. 3083 Structure and Implementation

Each 3083 Processor Complex (Figure 2-1) includes:

- An IBM 3083 Processor Unit
- An IBM 3082 Processor Controller
- An IBM 3087 Coolant Distribution Unit (CDU) Model 1 or 2
- An IBM 3089 Power Unit or other appropriate source of 400-Hz power
- An IBM 3278 Display Console Model 2A (as a system console)

An additional console device is required (as an operator console) to communicate with the control program.

Other requirements for full operation and maintenance include:

- A customer-supplied telephone to provide a data link to remote support locations.
- Access to an appropriate model of an IBM 3274 Control Unit attached by a channel to the 3083 Processor Unit so that a customer engineer, using the integrated service support console of the processor controller, can run error-isolation or maintenance programs concurrent with ongoing operations.

Each 3083 complex should also include:

- A printer for hard-copy output
- Access to a card reader
- Access to supporting direct-access storage devices or magnetic tape units

A 3083 can also include an optional programming support console.

The 3083 must use IBM programs (or equivalents) that provide system error recording to handle machine-check interruptions and the recording of detailed system status when a failure is detected.

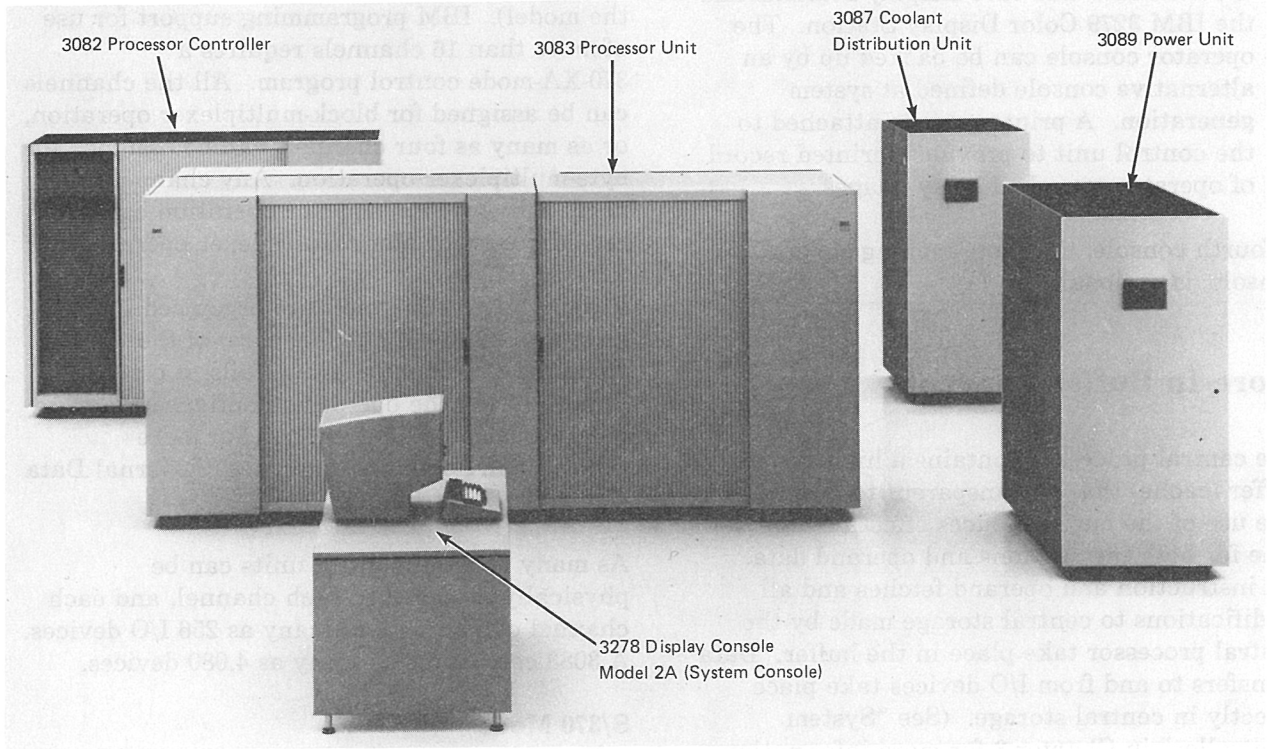


Figure 2-1. IBM 3083 Processor Complex (Design Model)

IBM's ability to provide service may be impacted if configurations do not meet the preceding requirements. Therefore, the availability of the 3083 complex may be affected.

Consoles

The 3083 uses at least three consoles:

- The system console, which interacts directly with other components of the 3083 complex. (See Chapter 4, "3082 Processor Controller" for more information.)
- The service support console, which interacts with the service and support microcode. (See Chapter 4, "3082 Processor Controller" for more information.)
- The operator console, which interacts with the control program and communicates with it through one of the channels.

  The choice of consoles typically includes the IBM 3277 and 3278 Display Stations and the IBM 3279 Color Display Station. The operator console can be backed up by an alternative console defined at system generation. A printer can be attached to the control unit to provide a printed record of operator-console display images.

A fourth console, the programming support console, is optional.

Store-In Buffer Concept

The central processor contains a high-speed buffer (cache) that is transparent to programs. The use of the buffer reduces effective access time for both instructions and operand data. All instruction and operand fetches and all modifications to central storage made by the central processor take place in the buffer. Data transfers to and from I/O devices take place directly in central storage. (See "System Controller" in Chapter 3 for more information.) The buffer uses a least-recently-used (LRU) algorithm for efficient data replacement. (See Chapter 3, "3083 Processor Unit," for more information.)

Modes of Operation

The 3083 Processor Complex operates in either System/370 (S/370) mode or System/370 extended architecture (370-XA) mode. S/370 mode conforms with System/370 architecture as described in the *IBM System/370 Principles of Operation.* The 370-XA mode conforms with System/370 extended architecture as described in the *IBM System/370 Extended Architecture Principles of Operation.* The mode is selected during initial microprogram load (IML).

S/370 mode and 370-XA mode differ in a number of respects. The two major areas of difference are in input/output (I/O) operations and in storage addressing.

Input/Output Operations

The 3083 complex provides 8, 16, or 24 channels (8 standard and 8 or 16 optional, depending on the model). IBM programming support for use of more than 16 channels requires a 370-XA-mode control program. All the channels can be assigned for block-multiplexer operation, or as many as four channels can be assigned for byte-multiplexer operation. Any channel not needed for byte-multiplexer operation can be reconfigured for block-multiplexer operation.

Physically, the channels are organized into groups of eight. If one (or more) of the channels of a channel group fails, it can be removed from the operating configuration to permit continued operation. (For more information about channels, see "External Data Controller" in Chapter 3.)

As many as eight control units can be physically attached to each channel, and each channel can address as many as 256 I/O devices. A 3083 can attach as many as 4,080 devices.

S/370 Mode

In S/370 mode, any channel may be assigned any valid channel address without concern for priority. Channel operation is based on a

random time-sliced approach that gives each channel equal opportunity to request service.

370-XA Mode

In 370-XA mode, as many as four channel paths are available to any attached I/O device. During any I/O operation, the *channel subsystem* selects one of the available channel paths to any specific I/O device.

The 370-XA mode improves system efficiency by making channel-path selection a hardware function rather than a control-program function. System efficiency is also improved by the queuing of pending I/O requests, thereby eliminating any control-program delays in reinstructing the I/O device.

At the start of an I/O operation, the central processor signals the channel subsystem (instead of a single channel, as in S/370 mode) that an I/O operation with a given I/O device is needed and an I/O request is posted to a queue; meanwhile, instruction execution in the central processor continues. Channel-path management and the queuing of I/O requests eliminate all busy-condition I/O interruptions encountered in S/370-mode operations.

In 370-XA mode, byte-multiplexer and block-multiplexer operation and attachment methods are unchanged, and existing channel programs (CCWs) continue to function without any changes.

When a device is dynamically reconnected to the system, the first available channel path (of the several channel paths attaching the control unit) may be selected, if the control unit has the dynamic reconnection feature.

Storage Operations

In 370-XA mode, storage addressing is extended from 24 bits to 31 bits, which represents an address range of 2G bytes (2,147,483,648 bytes). In addition, 370-XA mode permits the use of either 24-bit or 31-bit addressing, under program control. This facilitates the running of existing application (problem) programs with 370-XA-mode control programs.

In 370-XA mode, an additional CCW format is provided to permit direct addressing of storage above 16M bytes for I/O operations. With this format, channel programs may also reside above 16M bytes.

Support Unit

The 3082 Processor Controller is a stand-alone support unit that continuously monitors 3083 complex operation through direct communication with each component in the 3083 complex.

The 3082 initializes the system, inserts information in control storage at the time of IML, monitors voltage levels and coolant temperature, and provides the control-unit function for both the system console and service support console.

The 3082 also provides extensive error recording, recovery, and diagnostic support (described in "Processor Controller" under "Reliability, Availability, and Serviceability" in this chapter.)

(The 3082 is described in more detail in Chapter 4.)

Technology

The 3083 Processor Complex uses several logic-circuit technologies. The processor-unit logic is implemented in the new technology (TCM and its associated circuit board), but central storage and the processor controller function are implemented in a mixture of monolithic technologies.

The TCM (Figure 2-2) is a helium-filled, encapsulated module that is covered by a cold plate through which chilled water circulates to absorb heat. The TCM measures 125 by 134 by 35 millimeters (4.9 by 5.3 by 1.4 inches) and contains as many as 133 silicon chips mounted on a multilayered ceramic substrate that produces a package containing tens of thousands of logic circuits. The TCMs are plugged into a multilayered circuit board that provides TCM powering and TCM-to-TCM

connections. The central processor consists of eight TCMs and the associated board. Therefore, the major element of a processor unit is designed so that no external wiring or cabling is required.

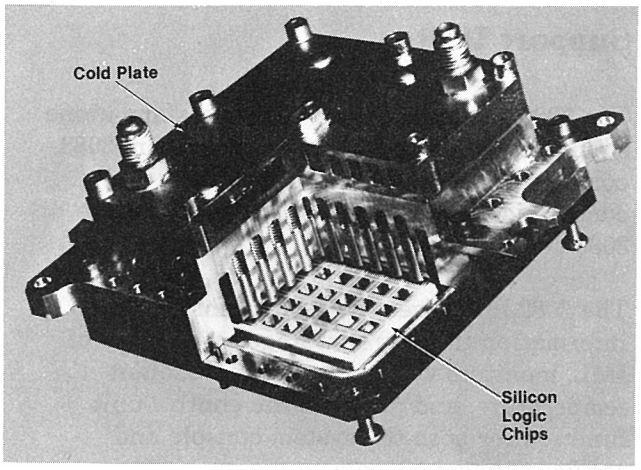


Figure 2-2. Thermal Conduction Module with a Cold Plate (Cutaway View)

Power

The 3089 Power Unit is designed to be the standard source of 400-Hz power for the 3083 complex. The 3089 meets IBM machine-room environmental standards, and therefore can be located in a machine room.

Cooling

The 3083 Processor Unit uses both air cooling and water cooling. The water cooling is provided by the 3087 Coolant Distribution Unit.

The 3087 is available in two models: the water-cooled Model 1 and the air-cooled Model 2. The Model 1 uses a water-to-water heat exchanger, which transfers the 3083's heat to the customer's chilled-water supply. The Model 2 uses a water-to-air heat exchanger, which transfers the 3083's heat to the air in the computer room. The 3087-1 is more efficient and shorter in length, whereas the 3087-2 may be more convenient for users who have limited cooling requirements.

The 3087 conditions and controls chilled water in a closed loop to maintain controlled temperature and flow rates to the densely packed circuits in the processor unit. The 3087 contains both the necessary controls to maintain the proper temperature within the self-contained closed loop and an automatic valve to adjust the flow of the chilled water.

The 3087 includes two pumps. If a cooling problem occurs as the result of a malfunction in the operating pump, the alternate pump is switched automatically into the coolant circuit for continued operation.

Data Representation

The basic addressable data unit is an eight-bit byte that may be used as one character, two decimal digits, or eight binary bits. The 3083 provides the following data representation features:

- Efficient use of storage and effective I/O rates for decimal data
- Variable-length fields
- Broad and flexible code conversion
- Decimal arithmetic
- Fixed- and floating-point arithmetic
- 32-bit words, 64-bit doublewords, and 128-bit extended words (for floating-point arithmetic)
- Instructions for functions such as translate, edit, convert, move, and compare

Error Handling

The 3083 contains comprehensive, automatic error-handling procedures that are often assisted by the 3082 Processor Controller. Error correction and recovery are attempted as a first step by using one of the following procedures (depending on where the error is detected):

- Processor checkpoint retry for the central processor
- Error detection and recovery for the external data controller (EXDC)
- Error checking and correction for central storage

When an error is detected, the 3082 automatically performs error-analysis procedures to isolate the malfunctioning area of the processor complex directly and therefore to identify the field-replaceable unit (FRU) or group of units. These procedures also include problem recognition, recording, and diagnosis.

Error analysis includes data scanout that consists of serialized bit-by-bit transfer of the data contained in the TCMs into the processor controller for analysis (to isolate the problem). Therefore, to isolate a FRU (for example, a TCM) or a group of FRUs, the error analysis uses all data scanned out at the time of the error. Errors are analyzed by the processor controller concurrent with the operation of the 3083 complex.

If the error is repeated frequently or is unrecoverable, analysis information is displayed on the system console. The operator can provide that information to the customer engineer who is contacted for assistance and who can then bring the necessary parts for the repair.

Processor Checkpoint Retry

Processor checkpoint retry (CPU retry) is an improved, more inclusive recovery mechanism than the instruction retry used on earlier IBM systems because it generally involves the retry of a series of instructions, rather than the retry of a single instruction. It can correct intermittent errors beyond those associated with a single instruction.

Processor checkpoint retry is implemented by using a series of error-detection circuits and a set of backup facilities (for example, a program status word [PSW] and general registers). The error-detection circuits within the central processor are continuously monitored.

Periodically, a checkpoint is taken by the central processor during the execution of instruction sequences. A checkpoint saves information in the backup facilities about the state of the central processor so that the processor can return to a point at which all processing was known to be correct, and can reexecute any failing instruction sequence.

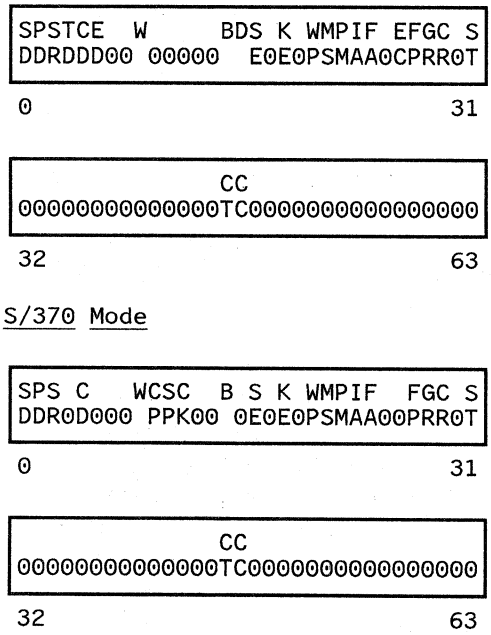
If an error is detected in the central processor, instruction execution stops. The processor controller saves information about the failure (that is, it initiates a logout of the central processor) and directs the central processor to return to the last checkpoint. The central processor uses the data saved in the backup facilities to restore itself to the state that existed at the time the checkpoint was established. Instruction processing is restarted from that point.

The central processor performs retry as many as eight times. If the error has not been corrected by the eighth retry, the central processor either performs a machine-check interruption or enters the check-stop state. If the error is corrected on or before the eighth retry, system recovery is reported by a repressible machine-check interruption, and processing continues.

Most, but not all, operations can be retried. Before execution of a nonretryable operation is attempted, correct operation of the instruction sequence to that point is verified. If an error occurs during execution of a nonretryable operation, the central processor either performs a machine-check interruption or enters the check-stop state. A new checkpoint is established and processing continues when correct execution of a nonretryable operation has been verified.

Figure 2-3 shows the bits of the machine-check interruption codes supported by the 3083.

Certain bits in control register 14 are associated with machine-check handling. Of these bits, the 3083 supports the use of bits 3 through 7 in 370-XA mode, and bits 0 and 4 through 7 (but not 1, 8, or 9) in S/370 mode.



Legend:

```
 B  Backed up
CC  Clock-comparator validity
CD  Timing-facility damage
CK  Channel-subsystem damage
CP  Channel report pending
CR  Control-register validity
CT  CPU-timer validity
 D  Delayed
EC  External-damage-code validity
ED  External damage
FA  Failing-storage-address validity
FP  Floating-point-register validity
GR  General-register validity
IA  PSW-instruction-address validity
KE  Storage-key error uncorrected
MS  PSW mask and key validity
PD  Instruction-processing damage
PM  PSW program-mask and condition-
    code validity
SD  System damage
SE  Storage error uncorrected
SP  Service-processor damage
SR  System recovery
ST  Storage logical validity
TD  Interval-timer damage
 W  Warning
WP  PSW-EMWP validity
```

Figure 2-3. 3083 Machine-Check-Interruption Code Formats

EXDC Error Handling

Errors detected within the EXDC are handled in one of two ways:

- An interface-control check indicates that an error occurred in a control unit or on the I/O interface, and causes posting of an interruption and invoking of software error recovery.

- For an error occurring within the EXDC, the 3082 Processor Controller may temporarily stop all EXDC operations by stopping the clocks to scan out, for analysis, the status of certain facilities where the error was detected. All channel operations in process at the time of a channel-control check are reinitiated under software control. (For more information about the EXDC, see "External Data Controller" in Chapter 3.)

Error Checking and Correction for Central Storage

Error checking and correction (ECC) for central storage provides automatic, single-bit error detection and correction. ECC also detects all double-bit errors and most multiple-bit errors but does not correct them. ECC takes place in the system controller and in central storage. (See Chapter 3, "3083 Processor Unit" for more information.)

CPU ID

The doubleword whose address is designated by the second operand of the Store CPU ID (STIDP) instruction contains the following information:

- The version code (two hexadecimal digits):
  - 01 for Model E
  - 11 for Model B
  - 21 for Model J
  - 81 for Model EX
  - 91 for Model BX
  - A1 for Model JX

- The CPU identification number (six hexadecimal digits):
  - The first digit is 2 (the central-processor address)
  - The next five digits are selected from the processor-unit serial number
- The model (processor-complex) number (four digits: 3083)

The last four hexadecimal digits are 0000.

Reliability, Availability, and Serviceability

Use of highly integrated TCMs for logic implementation, the processor controller, and the remote servicing contribute to the reliability, availability, and serviceability of the 3083 Processor Complex.

TCMs

The central processor (consisting of eight TCMs and the associated board) is an interconnected component that requires no external wires or TCM-to-TCM cabling, because all power and signal conductors are embedded in the basic structure of the TCM and its board. This high degree of integration improves 3083 reliability.

Processor Controller

The 3082 Processor Controller provides the following extensive error recording, recovery, and diagnostic support for customer engineers:

- Assisting the processor unit in error recovery
- Monitoring and logging all hardware failures
- Analyzing logout data and identifying failing parts
- Communicating with remote support locations

If automatic error recovery fails, the processor controller performs error analysis to identify the failing FRU or group of FRUs. Information about any failing FRU is displayed on the system console, and the operator can include this information when notifying service personnel so that replacement parts can be obtained for the service call.

More extensive error analysis can be performed by customer engineers through the use of dedicated diagnostic microcode. However, the dedicated use of the 3083 complex is required to run such microcode.

The central storage controller interacts with the 3082 to permit the concurrent maintenance and repair of central storage (16M bytes or larger). Part of storage (one basic storage element) can be taken offline while the rest of the complex continues operation. Information about previously logged errors (logged as they occurred during operation) is used with integrated diagnostic microcode to locate storage failures. Failing cards can be replaced, and the repair can be verified. After being serviced, that element can be tested by running integrated diagnostic microcode.

If local diagnostic methods fail to determine the problem conclusively or to isolate the failure, the processor controller provides a data link to the IBM Large Systems Support Center for the assistance of highly trained service specialists.

Remote Servicing

The data link to a remote support console is established manually (with user authorization) from the user's site. The Remote Support Active indicator lights on the operator control panel of the system console and remains lighted throughout linkup. These procedures permit customers to monitor use of the data link.

When a remote support console is connected by the data link, IBM Field Support Center personnel have access to the same information that is available to a local customer engineer through the service support console. Control of the system can be passed to a remote support console so that scan data and the contents of a wide range of arrays, latches, triggers, and registers can be examined and analyzed. The 3083 Processor Unit can be manipulated remotely (for example, for starting, stopping, and address comparing).

Chapter 3. 3083 Processor Unit

The 3083 Processor Unit consists of the following logical components (Figure 3-1) that execute instructions and commands, and perform storage and channel functions:

- A central processor
- Central storage
- An external data controller (with 8, 16, or 24 channels, depending on the model)
- A system controller

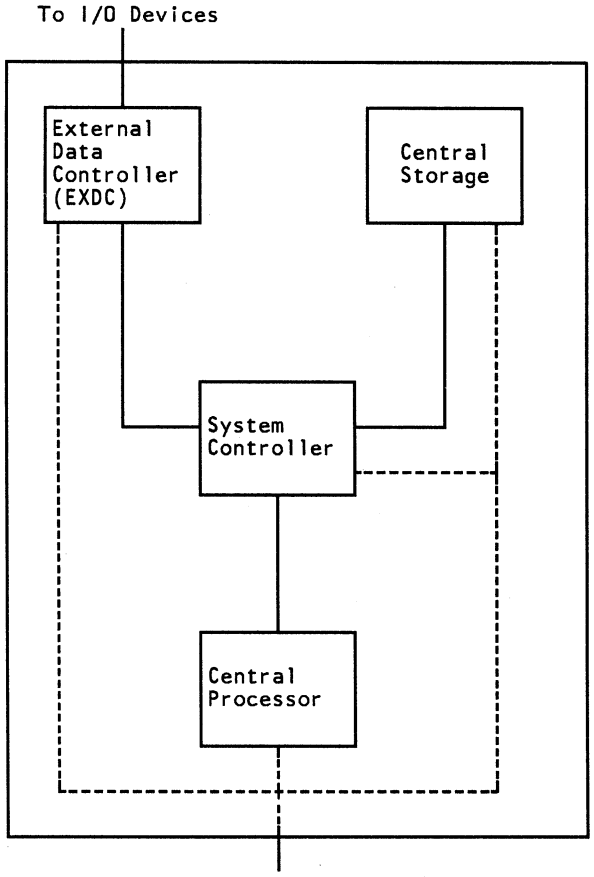


Figure 3-1. Logical Components of the IBM 3083 Processor Unit

The 3083 Processor Unit provides the following central storage capacities:

3083 Model	Bytes of Central Storage
E8, B8, J8, EX0, BX0, JX0	8,388,608 (8M)
E16, B16, J16, EX1, BX1, JX1	16,777,216 (16M)
E24, B24, J24, EX2, BX2, JX2	25,165,824 (24M)
E32, B32, J32, EX3, BX3, JX3	33,554,432 (32M)

The improved models (EX, BX, and JX) differ from the base models (E, B, and J) in that the improved models have a basic machine cycle time of 24 ns instead of 26 ns.

Note: If the optional performance feature is installed on base Models E, B, and J, the basic machine cycle time is 24.5 ns instead of 26 ns.

Models E and EX represent the lower end of the performance range, Models B and BX the midrange, and Models J and JX the higher end.

A 3083 Processor Unit can be upgraded at a customer's location as follows:

From	To
3083-E	3083-B or -J
3083-B	3083-J or 3081-G or -K
3083-J	3081-K
3083-EX	3083-BX
3083-BX	3083-JX or 3081-GX
3083-JX	3081-KX

The central processor has a high-speed buffer with a two-cycle access time (48 ns in Models EX, BX, and JX, 49 ns in Models E, B, and J with the optional performance feature installed, and 52 ns in Models E, B, and J without the optional performance feature installed). The access time to central storage is 312 ns, and data transfers between central storage and the buffer occur in 128-byte increments. Data transfers across the channels between central storage and the external data controller (EXDC) take place directly, bypassing the buffer. Modification of data by the central processor occurs in the buffer.

Central Processor

The central processor is microcode controlled and contains an instruction element (IE), variable field element (VFE), execution element (EE), control storage element (CSE), and buffer control element (BCE). The CSE fetches microinstructions that control instruction execution in the IE, VFE, and EE. The BCE controls the transfer of data between central storage and the central processor. Dynamic address translation is an automatic function of the BCE.

Instruction Element

The instruction element (IE) controls the sequencing of all instructions. It generates all addresses for instruction requests and initiates all central storage requests (both fetch and store). The IE includes its own buffers, registers, and hardware to handle instructions other than those executed in the VFE and EE. Execution of most instructions in the RR, RRE, RX, RS, S, SSE, and SI formats takes place in the IE.

Variable Field Element

The variable field element (VFE) executes SS-format instructions. It contains a decimal adder, two input registers, and two output registers. While using the data in one input register, the IE can be filling the other. The output registers work in the same way. Output goes to the storage data register in the IE. While the VFE is operating, the IE continues to fetch and store additional operand data.

Execution Element

The execution element (EE) provides the arithmetic results of the following operations:

- Fixed-point divide
- Fixed-point multiply
- Convert to binary
- Convert to decimal
- Floating point
- Extended-precision floating point

The EE contains various adders and registers to execute the instructions, and a local working storage to retain register contents during a checkpoint.

Control Storage Element

The control storage element (CSE) is the logical element that controls microcode execution in the central processor and contains the supporting control storage and registers that are used by the central processor.

Part of control storage is dynamically loadable. The dynamically loadable part permits infrequently used microcode to be loaded (from the hardware system area in central storage) as required. A lookaside directory, which is associated with the dynamically loadable part of control storage, permits immediate execution of in-place microinstructions and initiates the fetching of the appropriate microinstructions when they are not present in the CSE. When newly referenced microinstructions are loaded, they overlay the least-recently-used (LRU) microcode.

Buffer Control Element

The buffer control element (BCE) handles all central processor references to and from central storage, performs virtual-to-real address translation, and controls the high-speed buffer.

The BCE includes:

- A high-speed buffer
- A buffer directory
- A translation lookaside buffer (TLB)
- Dynamic address translation (DAT) hardware
- A store-back array

The High-Speed Buffer provides much faster access to instructions than if they were stored

in central storage. The buffer is transparent to executing programs. It is a store-in buffer that has a two-cycle access time for eight bytes of data with address translation done in parallel. The buffer stores data in 128-byte blocks. The blocks of data in the buffer are replaced by using a least-recently-used (LRU) algorithm.

When data is referred to during instruction execution, the buffer, the directory, and the TLB are accessed at the same time for address comparison.

The Buffer Directory contains the central-storage absolute addresses for the 128-byte blocks of data in the buffer. The directory entries contain bits that indicate:

- A block of data has been modified.
- The area in central storage that contains a specified block has been modified.
- The block has been modified during a checkpoint interval and cannot be replaced until the end of the interval.

The TLB contains as many as 128 virtual-real address pairs. When a virtual address is translated, the real address of the referenced page in central storage is stored in the TLB. Therefore, subsequent translations for the same virtual address are not required because the real address is immediately available in the TLB.

A least-recently-used (LRU) algorithm is used for the replacement of TLB entries. The TLB can be cleared by a reset or by the Purge TLB (PTLB) instruction. Under certain conditions, the TLB or selected entries in it may also be cleared by the Invalidate Page Table Entry (IPTE) instruction.

Dynamic Address Translation performs high-speed translation from virtual to real addresses for loading the TLB. Translation is overlapped so that if referenced data (real address) is in either central storage or the buffer, the data is directly available.

In S/370 mode, the 3083 uses 4K-byte pages and 64K-byte segments. In 370-XA mode, the 3083 uses 4K-byte pages and 1M-byte segments. A S/370-mode interpretively executed guest virtual machine can additionally use the 1M-byte segment size.

The Store-Back Array stores original copies of data that were modified in the high-speed buffer since the last checkpoint. If an error condition causes a processor checkpoint retry, this data is returned to the buffer before reexecution of the failing instruction sequence. The store-back array is reset at each checkpoint if no errors are detected within the checked instruction sequence.

Central Storage

The 3083 Processor Unit has two levels of storage (central storage and a high-speed buffer in the central processor) implemented in monolithic and large-scale-integration technologies. (The buffer is described under "Buffer Control Element" in this chapter.) Central storage is available in 8M-, 16M-, 24M-, or 32M-byte capacities. A hardware system area is reserved within central storage for specific system information and cannot be addressed by user programs. The addressable portion of central storage is synonymous with main storage, as described in the *IBM System/370 Principles of Operation* and the *IBM System/370 Extended Architecture Principles of Operation.*

Central storage is structured into basic storage elements (BSEs). The BSEs, which have either 8M or 16M bytes of central storage, contain the logic for fetching doublewords from or storing doublewords into the data arrays in each BSE. The data arrays are divided into basic storage modules (BSMs). Central storage has two-way interleaving of contiguously addressed 2K-byte blocks of storage. Interleaving permits the simultaneous accessing of separate BSMs. Therefore, access by the central processor or the EXDC to different physical BSMs can occur simultaneously.

The BSE logic performs the following functions:

- Data storage and retrieval for the processor complex

- Central storage communication with the processor complex (by means of the system controller)
- ECC
- Storage regeneration control

Note: Because 3083 storage is volatile, power failure results in the loss of data in central storage.

Hardware System Area

As part of the initial microprogram load (IML), at least 320K (327,680) bytes of central storage are selected for use as the hardware system area. This storage, which is unavailable for program use, contains:

- Copies of microcode
- A unit control word (UCW) for each configured I/O device
- Message buffers
- Tables
- Directories

The hardware system area cannot be accessed by conventional (program) storage references.

If channel attachment requirements for I/O devices exceed 512, the hardware system area is automatically expanded in increments of 32K bytes (in Models E, B, and J) or 64K bytes (in Models EX, BX, and JX) to as many as 576K (589,824) bytes.

Storage in the hardware system area (up to a total allocation of 800K [819,200] bytes in Models E, B, and J and 1,024K [1,048,576] bytes in Models EX, BX, and JX for all purposes) may be optionally reserved at IML for a customer engineer to trace I/O operations.

Error Checking and Correction

Error checking and correction (ECC) code bits are stored with data in the central storage data arrays. Single-bit errors detected during data transfer are corrected. Multiple-bit errors are flagged for follow-on action.

Data paths from the central processor and the channels are checked for parity. Parity bits are included in each command or data word.

Key-Controlled Storage Protection

Key-controlled storage protection provides both store and fetch protection. It prevents the unauthorized access or modification of information in central storage.

Each 4K-byte block of storage is protected by a seven-bit storage key. For processor-initiated store operations, access-key bits 0-3 from the currently active program status word (PSW) are compared with bits 0-3 from the storage key associated with the pertinent 4K bytes of storage to be accessed. If the keys do not match, the central processor is notified of a protection violation, the data is not stored, and an interruption occurs. The same protection is active for fetch operations if bit 4 of the storage key (the fetch-protection bit) is on.

Storage protection is regulated by the system controller.

External Data Controller

The external data controller (EXDC) is an integrated I/O processor that contains and controls channels. The number of channels is model dependent, as follows:

Model	Standard Channels	Optional Channels	Maximum No. of Channels
E and EX	8	8	16
B and BX	8	8 or 16	24
J and JX	8	8 or 16	24

IBM programming support for use of more than 16 channels requires a control program that operates in 370-XA mode. As many as four channels can be configured for byte-multiplexer operation; all the others must be configured for block-multiplexer operation.

In byte-multiplexer operation, channels can be used in either byte-multiplex mode or burst

mode. Byte-multiplex mode permits the concurrent operation of several relatively slow-speed I/O devices.

In block-multiplexer operation, channels can operate in either interlock mode (the standard mode) or data-streaming mode (for data-streaming control units). Data rates can be as high as 1.5 megabytes per second in interlock mode, and as high as 3.0 megabytes per second in data-streaming mode. All channels configured for block-multiplexer operation may be attached to control units that can operate in interlock mode or in data-streaming mode.

Channels are physically organized into one, two, or three groups of eight, depending on the model. (Channel organization is described in more detail in Chapter 2 under "Input/Output Operations.")

In S/370 mode, any physical channel may be assigned any valid channel address, but channel addresses must be contiguous.

When a 3083 is operating in 370-XA mode, the EXDC operates as a channel subsystem having 8, 16, or 24 channel paths, depending on the model. EXDC operation in 370-XA mode has several advantages:

- When an I/O request is made of any I/O device, the request is posted to the channel subsystem's work queue and the channel subsystem selects the channel path.
- The channel subsystem manages as many as four channel paths to any device, and handles any I/O-busy conditions.
- The channel subsystem permits dynamic reconnection of certain I/O devices, such as the IBM 3380 Direct Access Storage Model AA4. Dynamic reconnection allows such an I/O device to use the first available channel path (of as many as four) when the device reconnects to a channel without regard to which channel path was used initially.

The EXDC consists of the following logical elements:

- Channel processing element (CPE)
- Data server elements (DSEs)
- Interface adapter elements (IAEs)

Channel Processing Element

The EXDC has one microcode-controlled channel processing element (CPE) that interacts with as many as three data server elements (DSEs) to:

- Fetch channel command words (CCWs)
- Perform queuing and dequeuing for queued I/O requests
- Analyze status
- Post interruptions
- Start and end DSE operations
- Assist DSEs in command chaining and indirect addressing
- Manage channel-path selection (in 370-XA mode)

Data Server Elements

An EXDC may have as many as three data server elements (DSEs)—one per channel group (eight channels). Each microcode-controlled DSE provides a port to each of eight channels. The DSE uses a time-slicing technique to service all ports equally. Time slicing removes channel priority considerations.

The DSE controls channel functions by:

- Accepting and acting on commands from the CPE
- Controlling the transfer of data between the I/O
  devices and central storage
- Analyzing the ending status of a data transfer and passing it to the CPE

Interface Adapter Elements

The interface adapter elements (IAEs), which are *physically* located in the 3082 Processor Controller, control the I/O interfaces; therefore, each DSE port has an IAE. In S/370 mode, the microcode of the EXDC provides the flexibility to assign a physical interface to any valid channel designation.

The IAE controls channel functions by:

- Performing I/O interface tag sequences
- Interpreting control signals sent from the DSE

System Controller

The system controller acts as a switching device among all other logical components of the processor unit by interconnecting the central processor, the external data controller, and central storage.

The system controller:

- Controls data transfers to and from central storage
- Is the key switching element in the data flow between processor-unit components (the central processor, the EXDC, and central storage)
- Controls storage protection
- Contains a time-of-day (TOD) clock

The system controller includes hardware for ECC, storage protection, directories (similar to the BCE directories), a queue array, and channel interruptions.

The system controller also keeps track of central storage requests and assigns priorities to them. When two components (for example, the EXDC and the central processor) require access to the same storage module at the same time, the system controller establishes the priority. The system controller also designates which component can use specified data if contention exists.

Chapter 4. 3082 Processor Controller

The 3082 Processor Controller (Figure 4-1) provides and performs a variety of functions for the entire 3083 complex. They include:

- Monitoring and supervising all operations in the 3083 complex
- Providing the control-unit functions for all the consoles other than the operator console
- Providing the remote support facility modem and the processor controller file

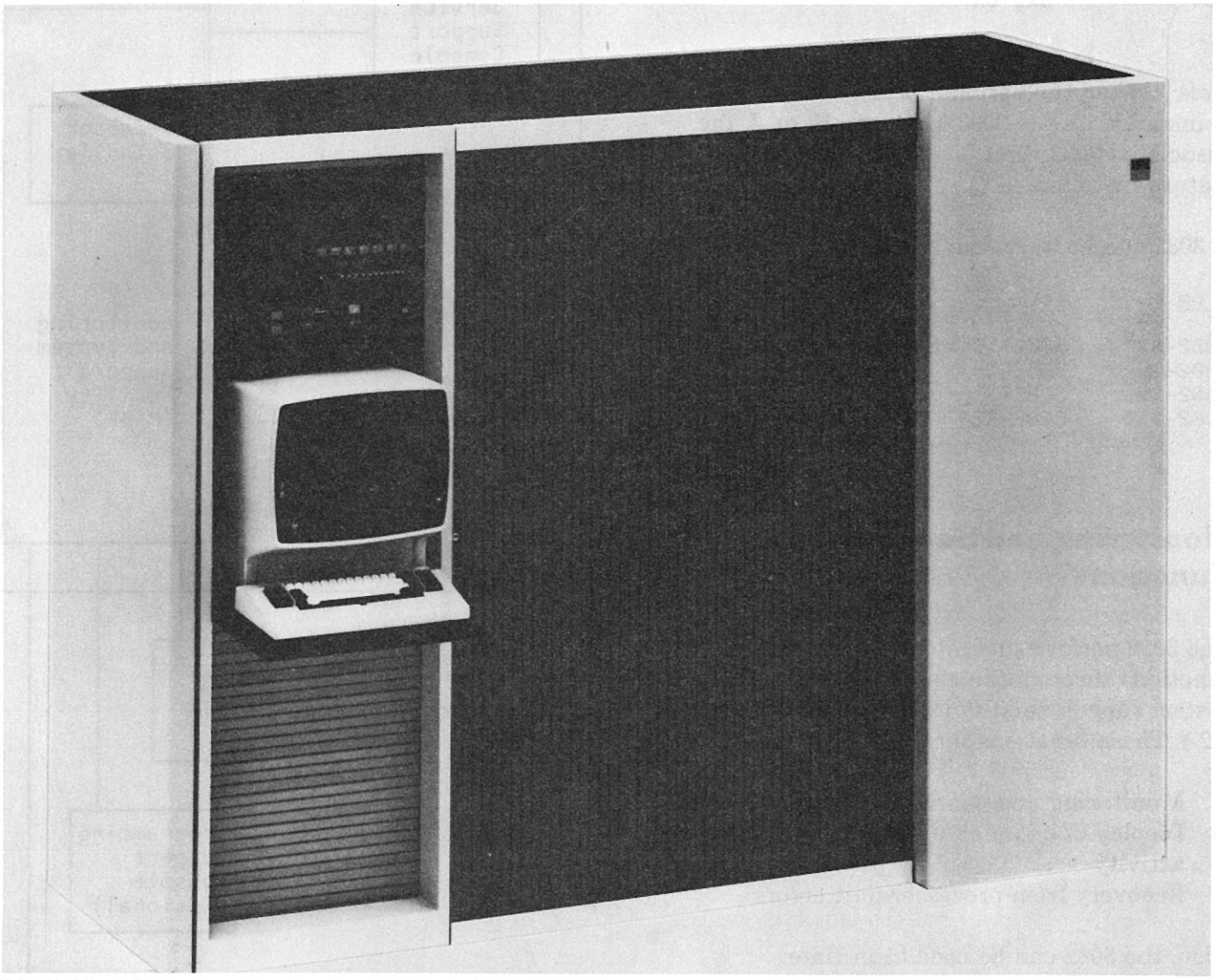


Figure 4-1. IBM 3082 Processor Controller, Showing the Integrated Service Support Console (Design Model)

The 3082 also physically houses the interface adapter elements (IAEs) for 8 channels (with a Model 8 or X8), 16 channels (with a Model 16 or X16), and 24 channels (with a Model 24 or X24).

A 3082 is used with a 3083 as follows:

3082 Model	Used with 3083 Model
8, 16	E, B, J
24	B, J
X8, X16	EX, BX, JX
X24	BX, JX

Note: When the optional performance feature is installed on the 3083 Model E, B, or J, the associated 3082 must have the performance feature installed.

A 3082 can be upgraded as follows:

From	To
3082-8	3082-16 or -24
3082-16	3082-24
3082-X8	3082-X16 or -X24
3082-X16	3082-X24

Monitoring and Supervisory Functions

The 3082 performs monitoring and supervisory functions through the use of its monitoring and system support facility (MSSF). (See Figure 4-2.) These functions include:

- Monitoring and control of system operation
- Display of channel and central-processor activity
- Recovery from processor-unit errors

Also, the 3082 can be used to initiate configuration changes.

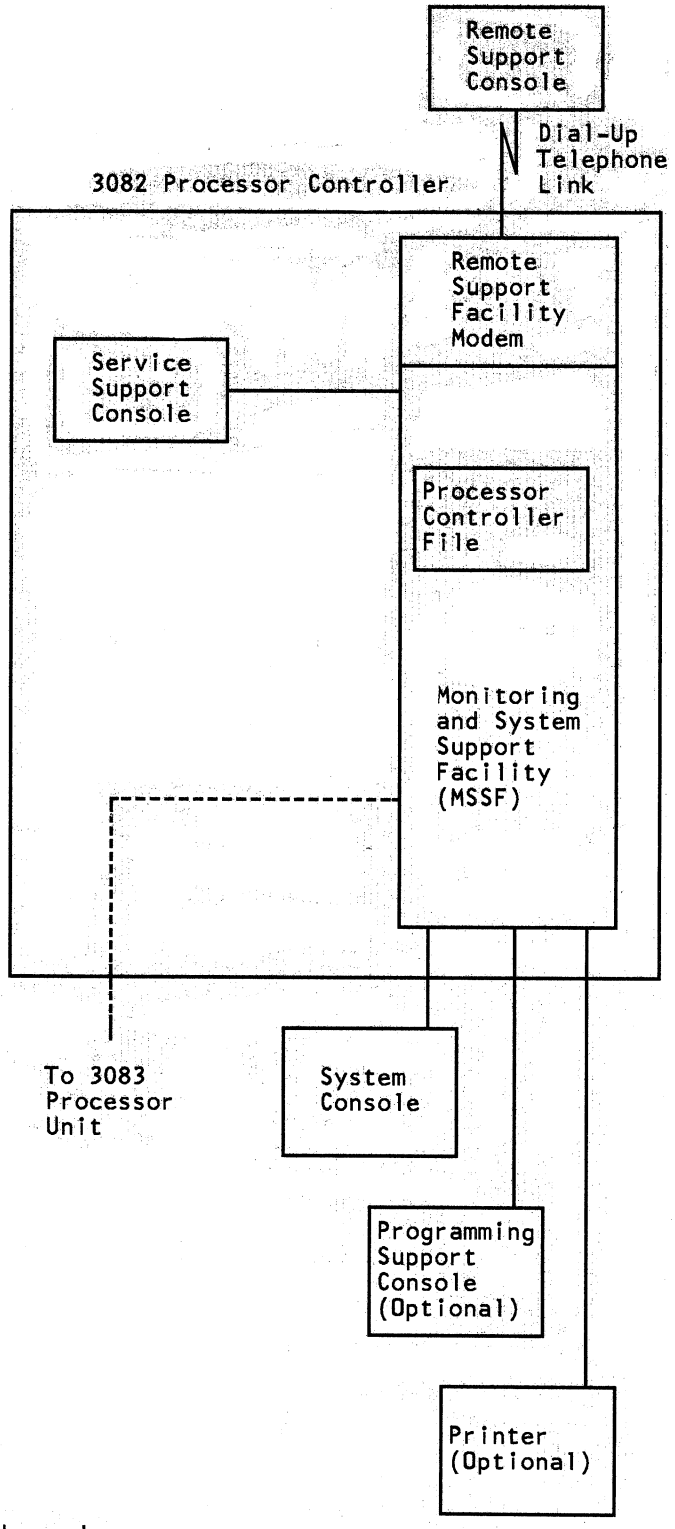


Figure 4-2. IBM Logical Components of an IBM 3082 Processor Controller with Consoles and a Printer

Operation Monitoring and Control

The 3082 monitors and controls the operations of the 3083 complex. It begins with initialization and proceeds through the sequencing of power to all the 3083 components and to all interconnected I/O control units that are under power-sequence control. During initialization of the 3083 complex, the 3082 validates areas of central storage as error-free data locations, records failing storage locations, and assigns the hardware system area in central storage based on contiguous error-free storage. The assignment of absolute address 0 is also made on the basis that the first 2M (2,097,152) bytes of a storage element is error free. This procedure ensures that this critical location for control-program residency is error free. After power sequencing, the 3082 performs IML.

During processing, the 3082 monitors voltage levels and coolant flow. If coolant flow decreases or stops, the second pump is switched into the coolant circuit to avoid thermal shutdown. If voltage adjustments are needed, a customer engineer can use the 3082 to perform the required adjustment.

Channel and Central-Processor Activity Display

The 3082 provides the ability to sample and display channel and central-processor activity.

Using the SYSTEM ACTIVITY DISPLAY (SAD) frame, the operator can choose options that specifically set up the sampling to suit the situation. Variables include target elements, sample time periods, operating states, and range parameters. Once a SAD frame is defined, it remains cataloged and can be recalled and reinvoked.

Processor-Unit Error Recovery

The 3082 assists the processor unit in error recovery. When an error occurs within the processor unit, the 3082 assists in checkpoint retry or channel-error correction.

The 3082 logs errors as they occur and then analyzes them for customer engineers. Failure symptoms, saved at the time of a malfunction, are analyzed on a time-sharing basis with other 3082 functions; this operation is concurrent with operation of the processor unit.

The 3082 saves the symptoms of these errors, correlates multiple symptoms, performs error analysis, and isolates the failure to the failing FRU or group of FRUs. This procedure is done automatically and is concurrent with continuing operation of the processor unit. When automatic error recovery attempts fail or the error occurs frequently, failure information is displayed on the system console, and an audible alarm is sounded to alert the operator of a problem requiring action. During IML, similar notification to the operator occurs when loss of storage exceeds a threshold that may degrade performance.

Configuration Changes

Through use of the service support console or system console (described later in this chapter), the 3082 can be used to initiate configuration changes in:

- Central storage arrays (for storage greater than 8M bytes)
- Interface adapter elements

However, operator-initiated action through the control program is the preferred method of reconfiguration because it makes both hardware and software changes as a single integrated action.

Control Unit Functions

The processor controller provides control-unit functions for the following devices:

- The system console
- The service support console
- An optional printer
- An optional programming support console

System Console

The system console interacts directly with the system through the processor controller and displays system status and system activity; it also performs the console functions of address compare, alter, display, start, stop, reset, restart, external interruption, and initial program loading (IPL).

The system console (Figure 4-3) is a stand-alone IBM 3278 Display Console Model 2A. The display screen contains 25 lines. Lines 1 through 21 are used for formatted function frames. Lines 22 through 25 display system and console status, messages, and operator input. The display console also has switches, controls, and indicators for contrast and brightness, alarm volume, status conditions, and error conditions. The keyboard resembles a typewriter keyboard but includes special function keys. The operator control panel, containing system indicators, is located immediately above the keyboard.

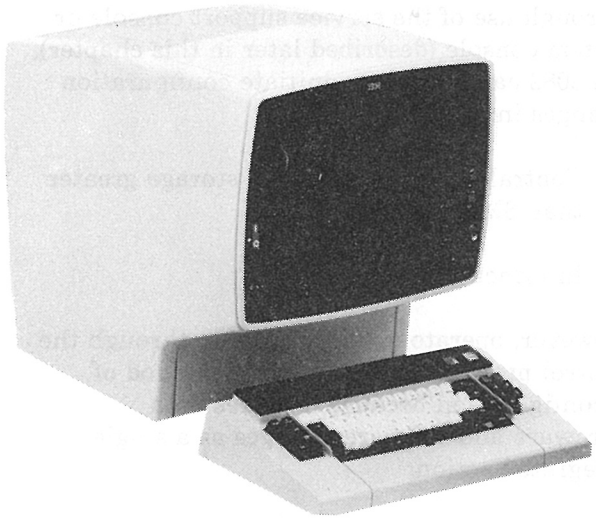


Figure 4-3. IBM 3278 Display Console Model 2A (Design Model), the System Console

Service Support Console

The service support console (Figure 4-1), which is similar to a 3278, is used by customer engineers for interaction with the service and support microcode. The console, which can be used independent of and concurrent with user operations, can also be used as a backup system console and attaches to a channel (by means of an appropriate model of an IBM 3274 Control Unit) for running service and support programs such as the online test executive program (OLTEP).

The service control panel, located above the console, contains error indicators, system activation controls, and data entry and display facilities for customer engineer use. The panel is used with the console to analyze and isolate malfunctions within the 3082 Processor Controller.

Optional Printer

An optional IBM 3230 Printer Model 2, 3268 Printer Model 2, or 3287 Printer Model 1 or 2 can be attached to the 3082 for hard-copy output of complete display frames on either the service support console or the system console. For example, 3083-complex status, processor-unit activity, error logs, or other diagnostic results can be printed. The printer is activated by function keys on either the service support console or the system console.

Optional Programming Support Console

An optional IBM 3278 Display Station Model 2 can be attached to the processor controller as a programming support console. If the console has the switch-control-unit feature and the switch is set for 3082 control, the 3278 may be used by a customer engineer to access IBM FE RETAIN through an integrated remote support facility modem. When the switch is set for processor-unit control, the 3278 can be connected to a 3274 Control Unit and may be used as any other online display console that is attached by means of a channel.

Remote Support Facility Modem

The 3082 contains an integrated modem that provides the data link used by a customer engineer for communicating with the IBM Large Systems Support Center for remote maintenance assistance. (See "Reliability, Availability, and Serviceability" in Chapter 2 for additional information.)

Integrated Processor Controller File

The integrated processor controller file contains libraries essential to the function of the 3083 complex; the file includes microcode libraries, UCWs, I/O-configuration and channel pathing parameters, the Input/Output Configuration Program (IOCP), and error logs.

Chapter 5. 3083 Feature Descriptions

The 3083 Processor Complex has many features. Some features are not part of the basic function of an architectural mode, and are thus classed as standard or optional features of that mode. Many features which are standard or optional features of the S/370 mode are part of the basic function of the 370-XA mode, or of the guest operation under interpretive execution (SIE) in the 370-XA mode, and are, therefore, provided by all processors capable of that mode. The features described in this chapter can be categorized into the following three groups (Figure 5-1):

- Features dependent on architectural mode (Figure 5-1, Part 1)
- Features that provide programming assists (Figure 5-1, Part 2)
- Features not dependent on architectural mode (Figure 5-1, Part 3)

The brief descriptions of features in this chapter include an indication of whether the function is basic in all implementations of the architectural mode of operation, or a standard or host-program feature of that mode on the 3083. Additional information about the mode-dependent features (Figure 5-1, Part 1) can be found in the following manuals:

- *IBM System/370 Principles of Operation,* GA22-7000
- *IBM System/370 Extended Architecture Principles of Operation,* SA22-7085

Additional information about programming assists (Figure 5-1, Part 2) can be found in the following manuals:

- *Virtual-Machine Assist and Shadow-Table-Bypass Assist,* GA22-7074
- *IBM System/370 Assists for MVS,* GA22-7079
- *IBM Assists for MVS/XA,* SA22-7092
- *IBM System/370 Extended Architecture Interpretive Execution,* SA22-7095

Basic Control (BC) Mode

BC mode provides a PSW format that is compatible with the PSW format of System/360.

Bimodal Addressing

Bimodal addressing permits 31-bit logical addressing, yet allows users to continue running System/370 problem programs, which use 24-bit logical addresses.

Branch and Save

Branch and save provides the Branch and Save instruction (BAS and BASR).

Byte-Oriented Operand

Byte-oriented operand allows storage operands of most unprivileged instructions to appear on any byte boundary without causing a specification exception and a program interruption. This feature applies to fixed-point, floating-point, and logical operands. It does not apply to instruction addresses, privileged instructions, or channel command words (CCWs).

Channel Group, First Additional and Second Additional

In addition to the one standard channel group (described in this chapter under "Channels") and depending on the 3083 model, one or two additional channel groups are optionally available. They provide 8 or 16 more channels for a total of 16 or 24 channels. (See "External Data Controller" in Chapter 3 for more information about channel groups.)

Feature	S/370 Native	S/370 (SIE) Guest	370-XA Native (Host)	370-XA (SIE) Guest
Basic-control (BC) mode	Basic	Basic	-- (1)	-- (1)
Bimodal addressing	--	--	Basic	Basic
Branch and save	Std	Basic	Basic	Basic
Byte-oriented operands	Basic	Basic	Basic	Basic
Channel indirect data addressing	Std	Host	Basic	Basic
Channel subsystem	--	--	Basic	Basic
Clear I/O	Std	Host	-- (2)	-- (2)
Command retry	Std	Host	Basic	Basic
Conditional swapping	Std	Basic	Basic	Basic
CPU timer and clock comparator	Std	Basic	Basic	Basic
Extended-precision divide	--	--	Basic	Basic
Extended-precision floating point	Std	Basic	Basic	Basic
Extended real addressing (26 bit)	Std	Basic	-- (3)	-- (3)
Fast release	Std	Host	-- (2)	-- (2)
Floating point	Std	Basic	Basic	Basic
Halt device	Std	Host	-- (2)	-- (2)
Interval timer	Basic	Basic	--	--
I/O extended logout	Std	Host	--	--
Key-controlled storage protection	Basic	Basic	Basic (4)	Basic(4)
Limited channel logout	Std	Host	-- (2)	-- (2)
Monitoring	Basic	Basic	Basic	Basic
Multiprocessing (5)				
CPU address identification	Std	Host	Basic	Basic
CPU signaling and response	Std	Host	Basic	Basic
Prefixing	Std	Host	Basic	Basic
TOD-clock synchronization	Std	Host	Basic	Host
Page protection	--	--	Basic	Basic
PSW-key handling	Std	Basic	Basic	Basic
Recovery extensions	Std	Host	--	--
Segment protection	Std	Basic	-- (6)	-- (6)
Service signal	Std	Host	Basic	Host
Storage-key instructions (ISK, SSK)	Basic	Basic	-- (4)	-- (4)
Storage-key-instruction extensions	Std	Basic	Basic	Basic
Storage-key 4K-byte block:				
Single-key 4K-byte blocks	Std (7)	Basic	Basic	Basic
Storage-key exception control	Std	Basic	-- (4)	-- (4)
System/370 extended:				
Non-MVS-dependent portion	Std	Basic	Basic	Basic
System/370 I/O instructions (8)	Basic	Host	-- (2)	-- (2)
Test block	Std	Basic	Basic	Basic
Time-of-day (TOD) clock	Basic	Basic	Basic	Basic
Tracing (ASN, branch, and explicit)	--	--	Basic	Basic
Translation:				
Dynamic address translation:				
2K-byte page size	No	No	-- (4)	-- (4)
4K-byte page size	Std	Basic	Basic	Basic
64K-byte segment size	Std	Basic	--	--
1M-byte segment size	No	Std	Basic	Basic
Extended-control (EC) mode	Std	Basic	-- (1)	-- (1)
Program-event recording (PER)	Std	Basic	Basic	Basic
Set-system-mask suppression	Std	Basic	Basic	Basic
Store status	Std	Basic	Basic	Basic
3033 Extension:				
Dual address space (DAS)	Std	Basic	Basic (9)	Basic(9)
SIOF queuing	Std	Host	-- (2)	-- (2)
Suspend and resume (10)	Std	Host	-- (2)	-- (2)
31-bit IDAWs	Std	Host	Basic	Basic
31-bit real addressing	--	--	Basic	Basic

Notes:

--	Not defined in the principles-of-operation manual for this architectural mode and therefore not implemented on the 3083.
Basic	Basic function of all processors operating in this architectural mode.
Host	The design of the host programming determines whether or not this native function is provided to the guest.
No	Defined in the principles-of-operation manual for this architectural mode but not implemented on the 3083.
Standard (Std)	Implemented as a standard feature of the 3083 when operating in this architectural mode.
1	Operation in 370-XA mode is comparable to operation in EC mode of System/370.
2	Replaced by basic functions of the channel subsystem; channel-program compatibility with System/370 is maintained.
3	Replaced by 31-bit real addressing.
4	The storage-key instruction extensions provide the required function to manage the storage keys in 370-XA mode; System/370 instructions ISK, RRB, and SSK are not in 370-XA architecture.
5	Multiple central processors and shared main storage are not provided on the 3083. Malfunction alerts and TOD-clock-sync checks do not occur on the 3083.
6	Replaced by page protection.
7	Double-key 4K-byte blocks are not implemented on the 3083.
8	Does not include the Resume I/O instruction.
9	Does not include DAS tracing; ASN tracing provides a comparable function.
10	Includes the Resume I/O instruction.

Figure 5-1 (Part 1 of 3). 3083 Features

Assist	S/370 Native	S/370 (SIE) Guest	370-XA Native (Host)	370-XA (SIE) Guest
Interpretive execution (SIE)	--	--	Std	Host
Preferred-machine assist (PMA)	Std	--	-- (1)	-- (1)
System/370 extended facility				
MVS-dependent portion:				
4 lock-handling instructions	Std	Basic	Basic	Basic
6 tracing instructions	Std	Basic	-- (2)	-- (2)
FIX PAGE	Std	Basic	--	--
SVC ASSIST	Std	Basic	Basic	Basic
ADD FRR	Std	Std	Std	Std
Page-fault assist	Std	Std (3)	--	--
VM assist for MVS/370 assists	Std	Basic	-- (1)	-- (1)
Virtual-machine assist (VMA)	Std	--	-- (1)	-- (1)
VM assists for CPU timer	Std	--	-- (1)	-- (1)

Notes:

--	Not defined as a programming assist for this architectural mode and therefore not implemented on the 3083.
Basic	Basic function of all processors operating in this architectural mode.
Host	The design of the host programming determines whether or not this native function is provided to the guest.
Standard (Std)	Implemented as a standard feature of the 3083 when operating in this architectural mode.
1	Interpretive execution (SIE) provides an alternative means of supporting execution of one or more guest operating systems.
2	Explicit tracing provides a comparable function.
3	Standard for preferred-storage-mode S/370 guest; not implemented for pageable-storage-mode S/370 guest.

Figure 5-1 (Part 2 of 3). 3083 Features

Features Not Dependent on Architectural Mode

Channel group, first additional	Optional
Channel group, second additional	Optional (On Models B, J, BX, and JX)
Channel-to-channel adapters	Optional (As many as two)
Channels (one group)	Standard
Data streaming	Standard
Error checking and correction	Standard
High-speed buffer storage	Standard
I/O error alert	Standard
I/O power sequence control	Standard (For 1st to 32nd control unit)
I/O power sequence control	Optional (For 33rd to 64th control unit)
Performance	Optional (On Models E, B, and J)
Processor checkpoint retry	Standard
Storage configuration control	Standard

Figure 5-1 (Part 3 of 3). 3083 Features

Channel Indirect Data Addressing

The addresses contained in channel command words (CCWs) in virtual storage must be translated by the control program before execution. Channel indirect data addressing allows immediately adjacent areas of virtual storage to be mapped into nonadjacent areas of absolute storage.

Channel Subsystem

The 370-XA channel subsystem queues I/O requests, selects from as many as four channel paths to any I/O device, and handles I/O-busy conditions. The external data controller (EXDC) operates as a channel subsystem having as many as 24 channel paths (depending on the 3083 model). Thirteen 370-XA I/O instructions are associated with the channel subsystem.

Channel-to-Channel Adapters

A channel-to-channel adapter provides the control-unit function for two loosely coupled processors. To interconnect two processors, one adapter is required. The data transfer rate is at the speed of the slower of the two attached channels. One or two adapters are available as optional features.

Channels (One Group)

One group of eight channels is standard and is integrated in the external data controller (EXDC). All the channels can be assigned for block-multiplexer operation, or as many as four channels can be assigned for byte-multiplexer operation. (See "External Data Controller" in Chapter 3 for more information about channels. See also "Channel Group, First Additional and Second Additional" in this chapter for information about additional channels.)

Clear I/O

Clear I/O provides the clear I/O function in a channel when the privileged Clear I/O (CLRIO) instruction is executed. The clear-I/O function causes a channel to discontinue its current I/O operation with an addressed I/O device by storing the status of the operation in the channel status word (CSW) and by making the associated subchannel available.

Command Retry

Command retry allows a subchannel to retry a command without causing an I/O interruption. The retry is initiated by a control unit.

Conditional Swapping

Conditional swapping makes available the Compare and Swap (CS) and Compare Double and Swap (CDS) instructions.

CPU Timer and Clock Comparator

The CPU timer is a high-resolution timer that causes an interruption whenever its value is negative. The interruption request is allowed by setting bit 21 in control register 0 and the external mask bit in the PSW.

The timer measures central processor elapsed time and causes an interruption at the end of the period that is specified by the program. The timer is decremented when the central processor is executing instructions and during the wait state but is not decremented when the central processor is in the stopped state. The program can initiate inspection of the CPU timer by using the Store CPU Timer (STPT) instruction and can set the timer to a specific value by using the Set CPU Timer (SPT) instruction. The contents of the CPU timer are reset to 0 by an initial CPU reset.

Note: When the TOD clock is in the stopped or error state, the CPU timer is not decremented.

The clock comparator provides for an interruption when the time-of-day (TOD) clock reaches a value specified by the program. The interruption is allowed when the central processor sets bit 20 in control register 0 and the external mask bit in the PSW.

The format of the clock comparator is the same as that of the TOD clock. A clock-comparator interruption is an external interruption. The program can initiate inspection of the clock comparator by using the Store Clock Comparator (STCKC) instruction and can set it by using the Set Clock Comparator (SCKC) instruction. The contents of the clock comparator are reset to 0 by an initial CPU reset.

Note: When the TOD clock is in the stopped or error state, the clock comparator is not operating.

Data Streaming

Data streaming is available on all block-multiplexer channels. It permits higher data rates (up to 3 megabytes per second) and longer cable lengths. For control units that operate in data-streaming mode, the cable between the 3082 and a control unit can be as long as 122 meters (400 feet). Data streaming is initiated by the control unit. The EXDC permits the intermixed attachment of data-streaming and non-data-streaming devices on the same channel.

Error Checking and Correction

Data paths between central storage and the channels and central processor are checked for parity.

Error checking and correction (ECC) code bits are stored with the data in the central storage data arrays. ECC codes apply to data stored in and fetched from central storage; single- and multiple-bit error detection and single-bit error correction are performed.

Extended-Precision Divide

Extended-precision divide provides the Divide (DXR) instruction for extended-precision floating-point operands.

Extended-Precision Floating Point

Extended-precision floating point provides the seven floating-point instructions that use the extended-precision format (a signed seven-bit characteristic and a 28-digit fraction).

Extended Real Addressing

Extended real addressing permits the addressing of real storage in excess of 16M bytes. The control program uses extended real addressing for locating user programs and portions of the control program in central storage at real addresses up to 32M bytes. Extended real addressing does not affect virtual addressability, which may not exceed 16M bytes.

Fast Release

Fast release provides the start-I/O-fast-release function on a channel when the Start I/O Fast Release (SIOF) instruction is executed. This function provides for early release of the central processor which executes the instruction. The fast release occurs before the device-selection procedure is completed, thereby reducing the central-processor delay associated with the operation.

Floating Point

Floating point provides the floating-point instructions and the floating-point registers. In System/370, floating point combined with the commercial instruction set is sometimes referred to as the System/370 universal instruction set.

Halt Device

Using the privileged Halt Device (HDV) instruction, the halt-device function signals the addressed I/O device to terminate its current I/O operation.

High-Speed Buffer Storage

High-speed buffer storage in the central processor satisfies many storage fetch requests, making the effective storage access time much shorter than the actual central storage cycle time. (For more information, see "Buffer Control Element" in Chapter 3.)

Interpretive Execution

The interpretive execution facility is used by the VM/XA Migration Aid and provides hardware support for several areas of virtual machine operation, such as interval timer operation, prefixing, address translation, and privileged instruction handling. This facility provides the Start Interpretive Execution (SIE) instruction, which the VM/XA Migration Aid uses to dispatch all virtual machines. (For more information, see *IBM System/370 Extended Architecture Interpretive Execution*, SA22-7095.)

Interval Timer

The interval timer provides external interruptions on a program-controlled basis. The value stored at a specified storage location is automatically decremented by 1 in bit-position 23 every 3.33 milliseconds. The program receives an external interruption request when the interval timer decrements from 0 to a negative value. (Bit 7 of the PSW and bit 24 of control-register 0 must be on.) The range of the interval timer is approximately 15.5 hours.

Note: When the TOD clock is in the stopped or error state, the interval timer is not operating.

I/O Error Alert

I/O error alert permits a channel to be alerted when a malfunction affects the ability of a control unit to continue operating.

I/O Extended Logout

I/O extended logout provides for the storing of detailed channel-error information in a storage area designated by a pointer.

I/O Power Sequence Control

I/O power sequence control permits the 3083 to sequence power (for power on or power off) for as many as 32 control units. If more control units are needed, a second I/O power sequence control is optionally available to provide power-on and power-off control for as many as 32 more control units.

Key-Controlled Storage Protection

Key-controlled storage protection prevents unauthorized access to information in central storage. Both store protection and fetch protection are included. If store protection is violated, data is not stored into the protected area; if fetch protection is violated, data is not retrieved from the protected area. When a violation is recognized, a program interruption occurs. (See "Central Storage" in Chapter 3 for more information.)

Limited Channel Logout

Limited channel logout provides four bytes of channel-status information for model-independent recovery from channel errors.

Monitoring

Monitoring provides a means of selectively recording designated events in the execution of a program. This facility is implemented by the use of the Monitor Call (MC) instruction.

Multiprocessing

In a 3083, multiprocessing provides CPU-address identification, CPU signaling and response, prefixing, and TOD-clock synchronization; it does not provide more than one central processor or shared main storage.

CPU-Address Identification

CPU-address identification provides an address by which the central processor may be identified by the Signal Processor (SIGP) instruction. CPU-address identification also provides new external-interruption conditions and the Store CPU Address (STAP) instruction.

CPU Signaling and Response

CPU signaling and response provides the Signal Processor (SIGP) instruction and the mechanism to interpret and act on several order codes, such as sense, stop, and restart.

Prefixing

Prefixing provides a means of assigning real addresses 0 through 4095 to any 4K-byte block in main storage.

TOD-Clock Synchronization

TOD-clock synchronization provides a uniform appearance to a clock-synchronization program in all 3081, 3083, and 3084 Processor Complexes, allowing the program to be independent of the actual number of TOD clocks and central processors in a configuration. TOD-clock synchronization includes a TOD-clock-synchronization control bit in control register 0.

Page Protection

Page protection provides protection against improper storing by controlling access to virtual storage through the use of the page protection bit in each page table entry.

Performance

The optional performance feature provides a 24.5-ns basic machine cycle time (instead of 26 ns) for 3083 Models E, B, and J. The performance feature must be installed on the associated 3082 Processor Controller.

Preferred Machine Assist

Preferred machine assist permits a single MVS/SP virtual-equals-real (V=R) virtual machine operating under VM/SP-HPO to operate with a minimum of simulated instruction execution, thereby allowing it to achieve near native performance. With preferred machine assist, any MVS/SP release that supports more than 16M bytes of real storage can use real storage above 16M bytes when operating as a V=R virtual machine.

Processor Checkpoint Retry

Processor checkpoint retry (CPU retry) is an error recovery procedure that corrects intermittent central-processor errors by saving pertinent data between predetermined checkpoints. If an error occurs, reexecution of the instruction sequence from the last checkpoint is performed. (For more information about this feature, see "Processor Checkpoint Retry" in Chapter 2.)

PSW-Key Handling

PSW-key handling provides the Set PSW Key from Address (SPKA) and Insert PSW Key (IPK) instructions.

Recovery Extensions

Recovery extensions consist of:

- The clear channel function in a channel, which can be used to perform an I/O-system reset in a channel when the Clear Channel (CLRCH) instruction is executed.
- Machine-check extensions, which include a machine-check external damage-code validity bit and which provide a detailed indication of the cause of external damage.
- Limited channel logout extensions, which consist of two additional logout bits, to indicate whether the I/O interface is operative and whether the logout is valid.

Segment Protection

Segment protection provides protection against improper storing by controlling access to virtual storage through the use of the segment protection bit in each segment-table entry.

Service Signal

Service signal provides an external interruption that is used by the 3082 Processor Controller to signal information to the control program.

Storage Configuration Control

The address ranges of the data arrays in a basic storage module are assigned as part of system initialization. In a 3083 with more than 8M bytes of central storage, a storage module can be removed from the operational configuration if the module malfunctions after processor-unit initialization.

Storage-Key Instruction Extensions

The storage-key instruction extensions provide the Set Storage Key Extended (SSKE), Insert Storage Key Extended (ISKE), and Reset Reference Bit Extended (RRBE) instructions, which provide 31-bit addresses and operate on the storage key associated with each 4K-byte block of storage.

Storage-Key Instructions

The storage-key instructions, Set Storage Key (SSK) and Insert Storage Key (ISK), allow initialization and inspection of the storage key associated with each block of storage that is available in the configuration.

Storage-Key 4K-Byte Block

Storage-key 4K-byte block allows a single key to be associated with each 4K-byte block of storage and, in S/370 mode, provides the storage-key exception control bit in control register 0.

System/370 Extended Facility (MVS-Dependent Portion)

The MVS-dependent portion of the System/370 extended facility consists of:

- SVC Assist instruction, which improves central processor performance by reducing the time needed to enter MVS supervisory services
- Fix Page instruction, Add FRR instruction, six tracing instructions, and four lock-handling instructions, which improve central-processor performance
- Page-fault assist, which improves MVS performance by directly assigning and initializing a page frame when a page-translation exception is recognized on first reference to certain virtual pages

In addition, in S/370 mode, System/370 extended facility provides VM assists for MVS assists. For virtual machines, these VM assists perform functions that are identical to functions of corresponding MVS assists for real machines.

System/370 Extended Facility (MVS-Non-Dependent Portion)

The MVS-non-dependent portion of the System/370 extended facility consists of:

- Low-address protection, which improves system integrity by providing special protection for storage (at effective addresses 0 through 511) that is vital to the control program
- Invalidate Page Table Entry (IPTE) instruction and the common-segment bit, which increase the efficiency of dynamic address translation
- Test Protection (TPROT) instruction, which performs tests for potential protection violations without causing program interruptions for protection exceptions

System/370 I/O Instructions

The I/O instructions used in S/370 mode are:

- Clear Channel (CLRCH)
- Clear I/O (CLRIO)
- Halt Device (HDV)
- Halt I/O (HIO)
- Start I/O (SIO)
- Start I/O Fast Release (SIOF)
- Store Channel ID (STIDC)
- Test Channel (TCH)
- Test I/O (TIO)

Another I/O instruction, Resume I/O (RIO), is provided by suspend and resume, which is described under "3033 Extension" in this chapter.

Test Block

Test block provides the Test Block (TB) instruction for testing the usability of a 4K-byte block of central storage.

Time-of-Day Clock

The time-of-day (TOD) clock provides a consistent measurement of elapsed time that can be used for indicating the time of day.

The TOD clock is initialized by execution of the Set Clock (SCK) instruction by the central processor. The clock is incremented every 125 nanoseconds by an 8-MHz clock line. It provides resolution to a single machine cycle with additional low-order bits, and has a nominal oscillator tolerance of ± 160 Hz.

Bit assignments are:

- Bits 0-54 increment at an 8-MHz rate.

- Bits 56-58 increment every machine cycle to provide cycle-by-cycle resolution.
- Bit 61 is on for the first Store Clock (STCK) instruction after initialization of the TOD clock by the control program.
- Bits 62 and 63 show the TOD-clock state.

In a 3083, bits 55, 59, and 60 are 0.

Tracing

Tracing provides three aids for problem-program analysis:

- Address-space number (ASN) tracing
- Branch tracing
- Explicit tracing

Translation

Translation includes the following five features:

- Dynamic address translation
- Extended control mode
- Program event recording
- Set-system-mask suppression
- Store status

As part of these features, translation also provides the following instructions:

- Load Real Address (LRA)
- Purge TLB (PTLB)
- Reset Reference Bit (RRB)
- Store Then AND System Mask (STNSM)
- Store Then OR System Mask (STOSM)

Dynamic Address Translation

Dynamic address translation (DAT) provides hardware translation of virtual addresses to real addresses during program execution. DAT supports real storage sizes up to 32M bytes. The 3083 uses 4K-byte pages and either 64K-byte segments (in S/370 mode) or 1M-byte segments (in 370-XA mode). A S/370-mode interpretively executed guest virtual machine can additionally use the 1M-byte segment size.

Extended Control (EC) Mode

When the 3083 operates in EC mode, virtual storage and high-speed DAT are available. (See "Central Processor" in Chapter 3 for more information.)

Program Event Recording

Program event recording (PER) assists in debugging programs. During program execution, PER can monitor the following actions:

- Successful branches
- Alteration of general registers
- Instruction fetches from a specified storage area
- Alteration of a specified storage area

Set-System-Mask Suppression

Set-system-mask suppression permits suppression of execution of the Set System Mask (SSM) instruction and provides the special-operation program interruption code.

Store Status

Store status is an operator-initiated function that places the contents of the current PSW and the program-addressable registers in permanently assigned, real-address locations within the first 512 bytes of central storage. Store status also includes a noninitializing manual reset function.

Virtual-Machine Assist

Virtual-machine assist (VMA), which is a programming assist for VM/SP-HPO, directly executes 15 virtual-machine instructions (including the ISKE, SSKE, and RRBE instructions), and validates page-table entries in the shadow tables. VMA improves performance on virtual-storage systems operating under VM/SP-HPO by reducing the amount of time VM/SP-HPO spends in the real supervisor state. The reduction is achieved by emulation (instead of software simulation) of certain privileged operation codes used by the virtual-storage (guest) control program.

VM Assists for the CPU Timer

VM assists for the CPU timer permit a central processor to directly execute the Set CPU Timer (SPT) and Store CPU Timer (STPT) instructions for a virtual machine operating under VM/SP HPO.

3033 Extension

The 3033 extension provides:

- Dual-address space
- Start-I/O-fast queuing
- Suspend and resume

All three are supported in S/370 mode by MVS/SP Version 1 Release 3; dual-address space is also supported in 370-XA mode by MVS/SP Version 2.

Dual-Address Space

Dual-address space aids communication between virtual address spaces. It provides:

- Twelve additional instructions
- Two address spaces for immediate use by a program
- Means of changing to other spaces
- A table-based subroutine linkage
- The use of multiple access keys for key-controlled protection by problem programs
- Aids for problem-program analysis (S/370 mode only)

In 370-XA mode, the tracing facility provides an alternative set of aids.

Start-I/O-Fast Queuing

Start-I/O-fast queuing allows a Start I/O Fast Release (SIOF) instruction to complete execution independent of device selection or a channel-busy condition. Control-unit or device busy conditions encountered subsequent to execution of an SIOF instruction cause the I/O operation to remain pending until facilities are available for initiation of the operation at the device.

Suspend and Resume

Suspend and resume provides:

- The suspend flag in the channel command word (CCW), which indicates that execution of a channel program is to be suspended.
- A channel-address-word (CAW) bit that controls whether the CCW's suspend flag should cause suspension of execution of a channel program.
- A channel-status-word (CSW) bit that indicates that execution of a channel program has been suspended
- The Resume I/O (RIO) instruction, which causes resumption of execution of a suspended channel program

31-Bit Indirect-Data-Address Word

The 31-bit indirect-data-address word (IDAW) extends the size of the address field in indirect-data-address words to 31 bits.

31-Bit Real Addressing

Thirty-one-bit real addressing ensures that certain fields contain 31-bit real addresses regardless of the setting of the addressing-mode control bit in the PSW.

Appendix A. 3083 Deviations

The following information describes 3083 deviations from the *IBM System/370 Principles of Operation,* the *IBM System/370 Extended Architecture Principles of Operation,* and the *IBM System/360 and System/370 I/O Interface Channel to Control Unit OEMI.*

Change Bit

(Both Principles of Operation)

When a 3083 Processor Unit performs a store access, it always turns on the change bit in the associated key concurrent with the access. The 3083 is granted a deviation that permits it to turn on a change bit without storing, provided that no store-access exceptions would have occurred if the store had taken place.

Channel-to-Channel Adapter Internal Resistance

(I/O Interface OEMI)

The maximum allowable internal resistance contributed by a control unit for every signal line of the I/O interface is 1.0 ohm. The 3083 deviates from this requirement in that the resistance contributed to an I/O interface by a channel-to-channel adapter feature may be up to 3.0 ohms.

Delayed Bit

(System/370 Principles of Operation)

The *IBM System/370 Principles of Operation* specifies that the delayed bit is set to 1 when a machine-check condition is delayed in being reported because the central processor is disabled for machine-check interruptions at the time the condition occurs. The 3083 deviates from this by always turning on the delayed bit in the machine-check interruption code for repressible machine-check interruptions even though the central processor is enabled for that type of interruption at the time the condition occurs.

Nonzero Bus-Out during Stop Sequence Control

(I/O Interface OEMI)

During a stop sequence control, 3083 channels do not ensure that bus-out contains all 0's.

Prefixing DAT Table Entries

(System/370 Principles of Operation)

Dynamic-address-translation (DAT) entries can be accessed in the DAT process without applying prefixing and reverse prefixing to the storage addresses of the table entries.

Test Channel Condition Code

(System/370 Principles of Operation)

A byte-multiplexer channel operating in burst mode responds available (condition code 0) to a Test Channel (TCH) instruction.

Glossary of Terms and Abbreviations

Refer to *IBM Vocabulary for Data Processing, Telecommunications, and Office Systems,* GC20-1699, for terms that do not appear in this glossary.

absolute address. An address that identifies a storage location without the use of any intermediate reference.

address. An identification of a storage location or an I/O device.

address translation. See *dynamic address translation.*

BCE. Buffer control element.

BSE. Basic storage element.

BSM. Basic storage module.

CAW. Channel address word.

CCW. Channel command word.

CDU. Coolant distribution unit.

central storage. In the 3083, includes both main storage (programs and data) and the hardware system area (not addressable by programming); it is available to the central processor and the EXDC.

CPE. Channel processing element.

CPU. Central processing unit.

CSE. Control storage element.

DAT. See *dynamic address translation.*

DSE. Data server element.

dynamic address translation (DAT). (1) The process of changing a virtual storage address to a real storage address during execution of an instruction. (2) A hardware feature that performs the translation.

EC mode. See *extended control mode.*

ECC. Error checking and correction.

EE. Execution element.

EXDC. External data controller.

extended control mode. A mode in which all the features of a System/370 model, including dynamic address translation, are operational.

FE. Field Engineering.

FE RETAIN. A remote technical assistance and information network that provides data base and data link support for the IBM Field Engineering (FE) Division.

FRU. Field-replaceable unit.

G-byte. 1,073,741,824 bytes of storage capacity.

guest. In interpretive execution mode, the interpreted or virtual machine as opposed to the real machine (the host).

hardware system area. That part of central storage that is reserved for system usage and is not program addressable.

high-speed buffer. A high-speed store-in buffer.

host. In interpretive execution mode, the real machine as opposed to the virtual or interpretive machine (the guest).

Hz. Hertz.

IAE. Interface adapter element.

ID. Identifier.

IE. Instruction element.

IML. Initial microprogram load.

initialization. To set counters, switches, addresses, latches, or storage contents to 0 or to other starting values at the beginning of, or at the prescribed points in, a computer program or process.

I/O. Input/output.

IOCP. Input/Output Configuration Program, which defines I/O configuration parameters needed for the EXDC to function.

IPL. Initial program load.

K-byte. 1,024 bytes of storage capacity.

latch. A hardware logic device that denotes a condition. In this manual, the word is applied to error conditions.

LRU. Least recently used.

main storage. That part of central storage that is program addressable.

M-byte. 1,048,576 bytes of storage capacity.

MHz. Megahertz.

microsecond. One millionth of a second.

MSSF. Monitoring and system support facility.

MVS. Multiple virtual storage.

nanosecond. One thousandth of a microsecond.

ns. Nanosecond.

offline. Pertaining to resources with which the processor unit has no direct communication or control.

OLTEP. Online test executive program.

online. Pertaining to resources with which the processor unit has direct communication or control.

PER. Program event recording.

port. An access point for data entry or exit.

PSW. Program status word.

RAS. Reliability, availability, and serviceability.

real address. The address of a location in real storage.

RETAIN. See *FE RETAIN.*

RR. Register-and-register operation.

RRE. Register-and-register operation having an extended operation-code field.

RS. Register-and-storage operation.

RX. Register-and-indexed-storage operation.

S. Storage operation using an implied operand and storage.

SAD. System activity display.

SI. Storage-and-immediate operation.

SIE. Start interpretive execution.

SS. Storage-and-storage operation.

SSE. Storage-to-storage operation having an extended operation-code field.

S/370. System/370.

TCM. See *thermal conduction module.*

thermal conduction module (TCM). Helium-filled, encapsulated module containing multiple logic chips mounted on a multilayered ceramic substrate; used to implement 3083 Processor Unit technology.

TLB. Translation lookaside buffer (sometimes referred to as a directory lookaside table, or DLAT).

TOD clock. Time-of-day clock.

UCW. Unit control word.

V=R. Virtual equals real.

VFE. Variable field element.

virtual address. An address that refers to virtual storage and that must be translated into a real storage address when it is to be used.

VMA. Virtual machine assist.

volatile storage. Storage that must be regenerated (refreshed) for permanent valid data retention.

VM/SP-HPO. Virtual Machine Facility/System Product High Performance Option.

370-XA. System/370 extended architecture.

Bibliography

The following publications provide additional information about 3083 Processor Complex functions and operation:

GA22-6974 *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information*

GA22-7000 *IBM System/370 Principles of Operation*

GA22-7001 *IBM System/370 System Summary: Processors*

GA22-7002 *IBM System/370 Input/Output Configurator*

GA22-7074 *Virtual-Machine Assist and Shadow-Table-Bypass Assist*

GA22-7077 *IBM 3081, 3083, and 3084 Channel Characteristics and Configuration Guide*

GA22-7079 *IBM System/370 Assists for MVS*

SA22-7085 *IBM System/370 Extended Architecture Principles of Operation*

SA22-7092 *IBM Assists for MVS/XA*

SA22-7095 *IBM System/370 Extended Architecture Interpretive Execution*

GA32-0039 *IBM Input/Output Device Summary*

GC22-7004 *IBM System/370 Installation Manual—Physical Planning*

GC28-1027 *Input/Output Configuration Program User's Guide and Reference*

GC38-0035 *IBM 3081, 3083, and 3084 Messages for the System Console*

GC38-0036 *IBM 3083 Operator's Guide for the System Console*

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