IFTE89P500100-01 18 September 1990

INTEGRATED FAMILY OF TEST EQUIPMENT (IFTE)

COMMERCIAL EQUIVALENT EQUIPMENT

CEE HANDBOOK

CONTRACT NO. DAAB07-89-C-N001

CDRL SEQUENCE NO. 5001

Prepared for:

PM-TMDE

US ARMY COMMUNICATIONS-ELECTRONICS COMMAND

FT. MONMOUTH, NJ 07703-5008

Prepared by:

GRUMMAN CORPORATION

ELECTRONICS SYSTEMS DIVISION

BETHPAGE, NY 11714

		REVISION SHEET
REV	DATE	REVISION DESCRIPTION
01	9-18-90	This document has been revised to incorporate various changes in paragraphs 4.1.4, 4.3.2, 4.6.3 and 4.7. A vertical bar-mark is used in the right-hand margin of this document to indicate the approximate location in the text where a change was made.

TABLE OF CONTENTS

1. GENERAL INFORMATION

1.1 CEE HANDBOOK PURPOSE & SCOPE

The purpose of this handbook is to assist test program set developers in the application and use of the IFTE CEE. For this purpose, the handbook has been divided into the following major sections:

A. General Information - A summary of the physical characteristics and requirements of a fully-configured CEE.

B. CEE Applications - A discussion of the various configurations of the CEE that can be used to meet the requirements of particular application. This includes the identification of the various elements present in each configuration.

C. Operating Instructions - Specific instructions for system initialization, turn on, turn off, and program execution.

D. Operational Characteristics - Detailed characteristics of CEE resources, organized by major subsystem.

E. System Interface - Application and use of the various UUT and user interfaces of the CEE.

F. TPS Implementation Tools - A summary description of the TPS tools presently available with the ATSE.

G. Testing and Troubleshooting - Description and use of the preventative maintenance, self test and self alignment capabilities of the CEE.

1.2 CEE GENERAL DESCRIPTION

The CEE is designed for use in developing and validating Test Program Sets (TPSs) capable of performing end-to-end (performance) testing and fault isolation of LRUs, WRAs, SRUs, SRAs, etc.

In addition, the CEE is used for factory and depot-level testing in lieu of the militarized BSTS ATE.

The approach to CEE design and configuration stresses maximum commonality to the BSTS through the observation of the following guidelines:

A. It utilizes software common to the BSTS.

B. It utilizes TPS tools common to the BSTS (ATSE).

C. It contains features that are the exact equivalent of the BSTS:

- UUT Interface

- Operator Interface

- Test Capability

This approach allows a contractor to perform TPS development and to implement a factory and depot test capability that is functionally, and in software capability, the same as the full militarized version that will host the TPS in the field.

1.3 PHYSICAL CHARACTERISTICS

1.3.1 Major Components List

The following list of major components shall comprise all of the CEE configurations, unless otherwise noted. (Reference Figures 1.1 through 1.6)

A. System Controller and Peripherals

(1) Peripheral Interface Controller (System Controller)

(2) Printer

(3) Disc Drive

(4) Display terminal

(5) Touch Screen

B. Power Subsystem

(1) Programmable DC Load

(2) AC Power Supply

(3) Programmable DC Power Supply #1, #2 (CEE -103, -109 only)

(4) 28 VDC Supply

C. RF Instruments

(1) RF Interface Unit (RFIU) (CEE -101, -103, -107, -109 only)

(2) RF Generator 1 (RFG1) (CEE -103, -109 only)

(3) RF Generator 2 (RFG2) (CEE -101, -103, -107, -109 only)

(4) RF Generator 3 (RFG3) (CEE -101, -107 only)

(5) Spectrum Analyzer and Display (CEE -101, -103, -107, -109 only)

(6) RF Power Meter (CEE -101, -103, -107, -109 only)

(7) Rubidium Frequency Reference

(8) RF Millivoltmeter (CEE -103, -109 only)

D. Miscellaneous Units

(1) Power Control Unit

(2) High Frequency Probe for DMM

(3) Self-Alignment ICD

(4) Self-Test ICD

E. Analog VIC Assembly

(1) Resource Controller

(2) Signal Distribution System (SDS)

(3) Arbitrary Function Generator

(4) Synchro/Resolver Simulator-Indicator

(5) Digitizer

(6) Counter-Timer

(7) Digital Multimeter

(8) Display Analyzer-Simulator

F. Digital VIC Assembly

(1) Resource Controller

(2) Digital I/O

(3) BUS Test Unit

(4) Wizard Probe System

G. VIC Power Supply

H. Interface Panels

(1) Gold Dot Interface Panel

(2) Auxiliary Interface Panel

I. Mechanical

(1) Racks to house electronic equipment and drawers of the CEE.

(2) CEE Work Surfaces

J. Software

(1) Executive Software

(2) Maintenance Software

a. Self Test

b. Self Alignment

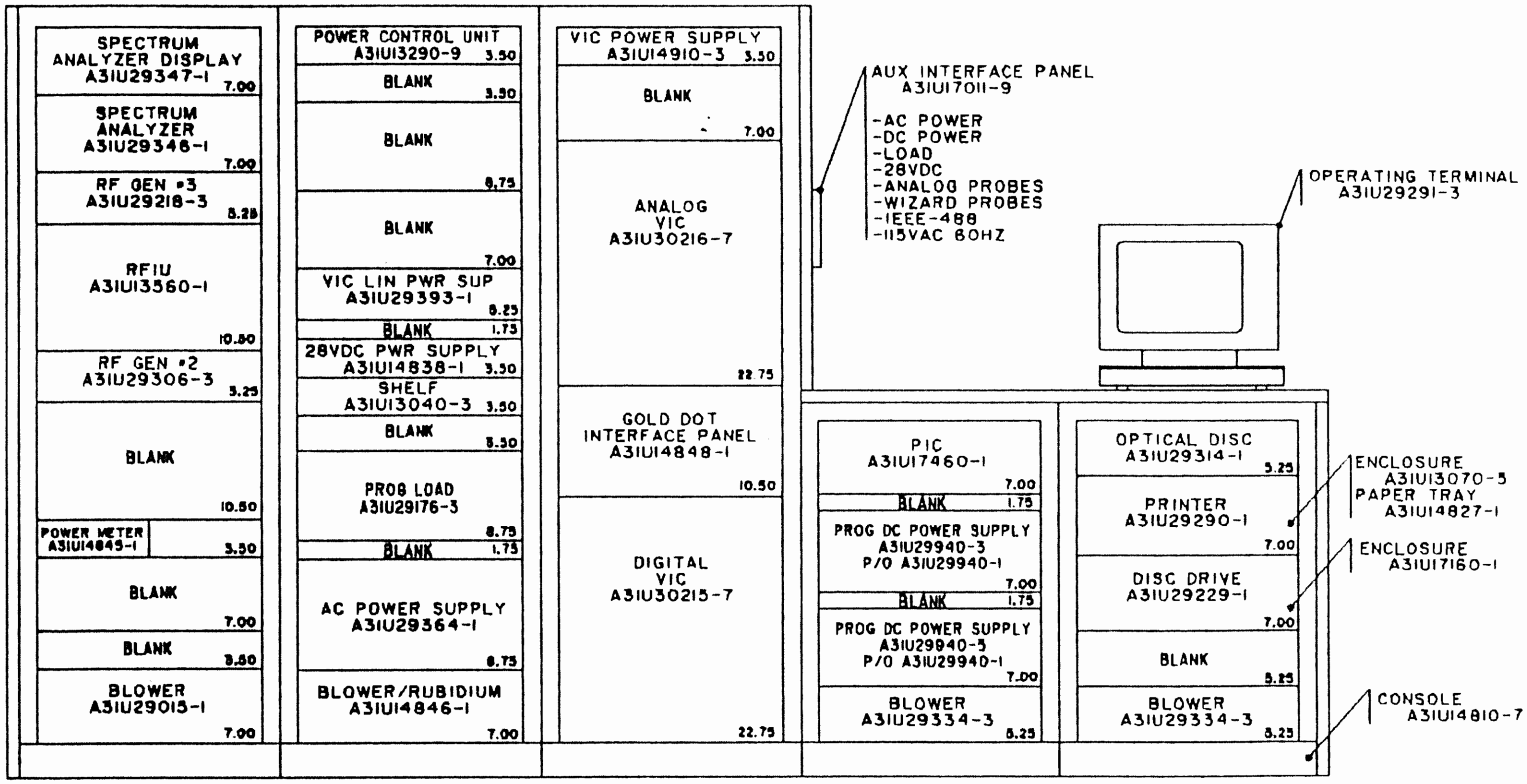
(3) Run Time System

(4) Administrative

(5) ATG Post Processor - Analyzer

FIGURE 1.1

COMMERCIAL EQUIVALENT EQUIPMENT
A31U17000-101



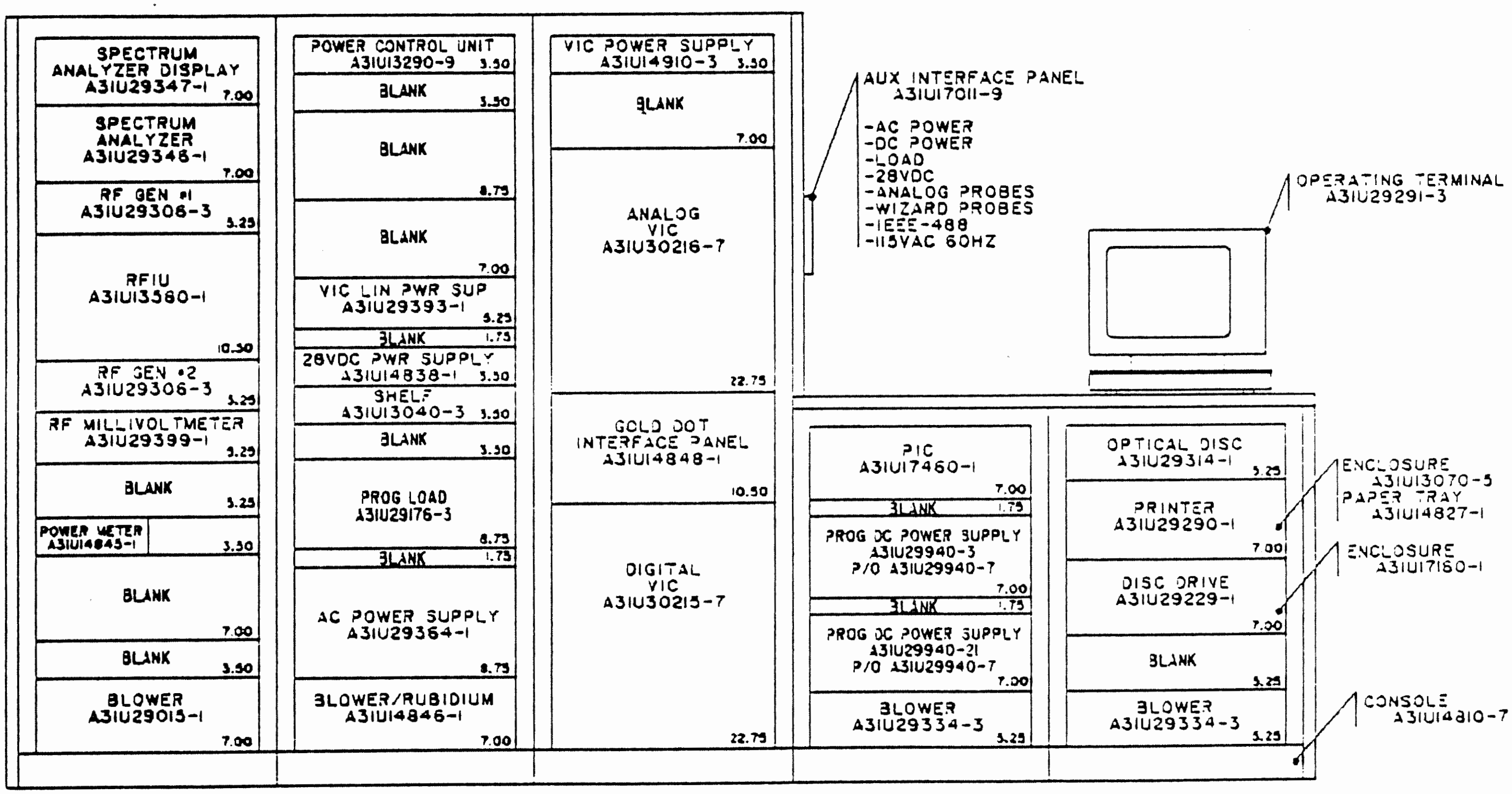
ANALOG VIC RESOURCES	DIGITAL VIC RESOURCES
MIPRCS CONTROLLER	MIPRCS CONTROLLER
TIMING GEN	TIMING GEN
DMM	WIZARD PROBE
AFG/CTR-TIM/DIGITIZER (5)	DWG I/O (16 PIN EA) (10)
DISPLAY ANALYZER/SIMULATOR	BUS TEST UNIT
UNIVERSAL SWITCH (6)	DWG HV (2)
DAC/UTILITY SWITCH	
SYNCH-RES SIM/IND	

APPV'D BY: REV 6 04-13-90

ATE.IFTE.ELEVATION.CEE

FIGURE . 1.2

COMMERCIAL EQUIVALENT EQUIPMENT
A31U17000-103



ANALOG VIC RESOURCES

MIPRCS CONTROLLER
TIMING GEN
DMM
AFG/CTR-TIM/DIGITIZER (5)
DISPLAY ANALYZER/SIMULATOR
UNIVERSAL SWITCH (6)
DAC/UTILITY SWITCH
SYNCH-RES SIM/IND

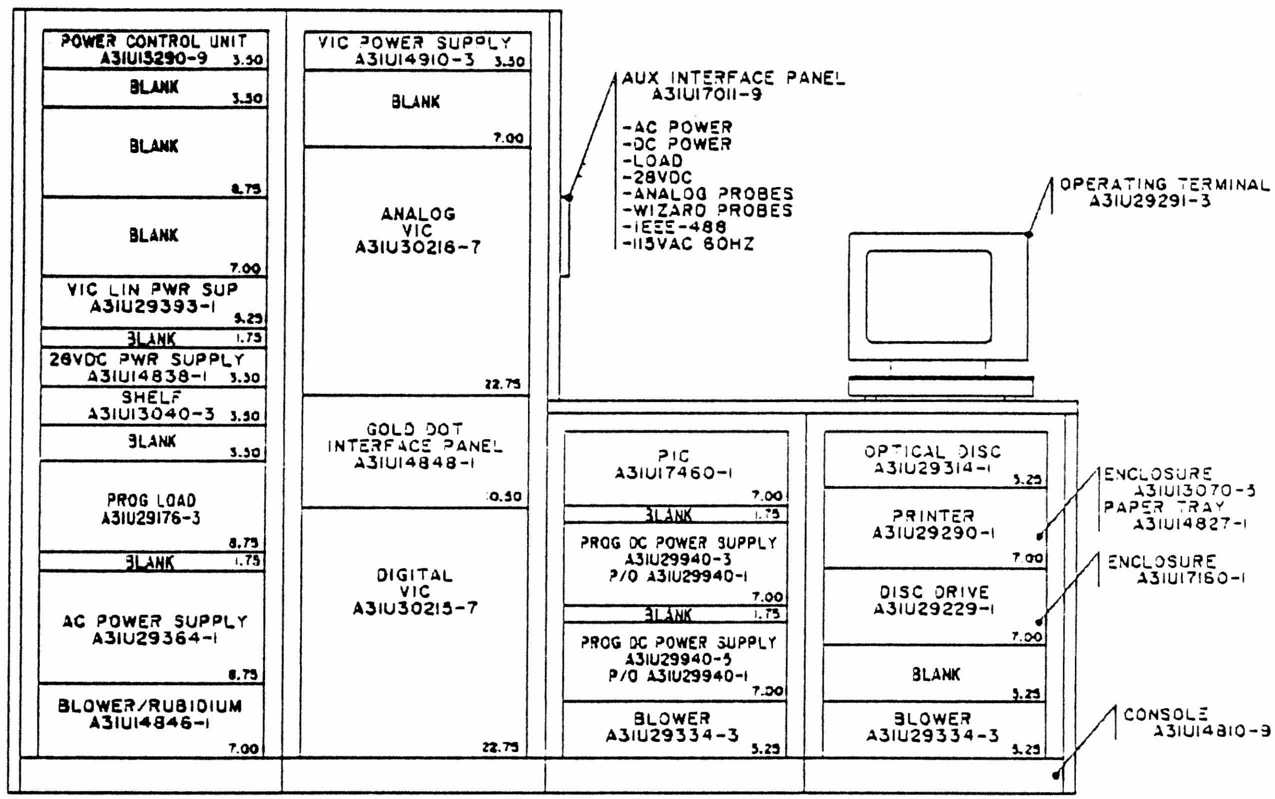
DIGITAL VIC RESOURCES

MIPRCS CONTROLLER
TIMING GEN
WIZARD PROBE
DWG I/O (16 PIN EA) (10)
BUS TEST UNIT
DWG HV (2)

APP'D BY: REV H 02-11-88

ATE.IFTE.ELEVATION.CEE

COMMERCIAL EQUIVALENT EQUIPMENT
A31U17000-105



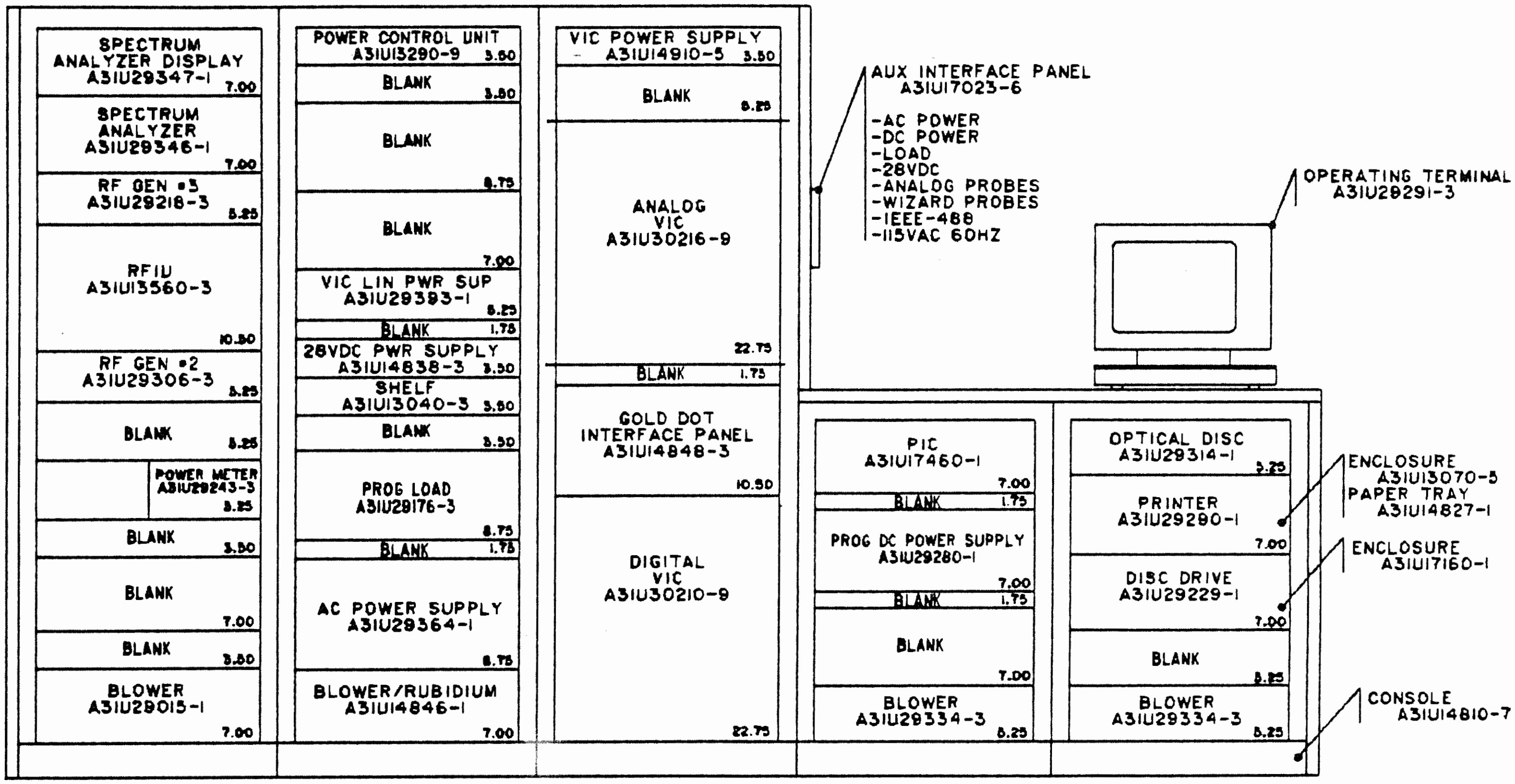
ANALOG VIC RESOURCES	DIGITAL VIC RESOURCES
MIPRCS CONTROLLER	MIPRCS CONTROLLER
TIMING GEN	TIMING GEN
DMM	WIZARD PROBE
AFG/CTR-TIM/DIGITIZER (5)	DWG I/O (16 PIN EA) (10)
DISPLAY ANALYZER/SIMULATOR	BUS TEST UNIT
UNIVERSAL SWITCH (6)	DWG HV (2)
DAC/UTILITY SWITCH	
SYNCH-RES SIM/IND	

APP'D BY: REV E 02-11-89

ATE:FTE.ELEVATION.CE!

FIGURE 1.3

COMMERCIAL EQUIVALENT EQUIPMENT-FULL UP
A31U17000-107



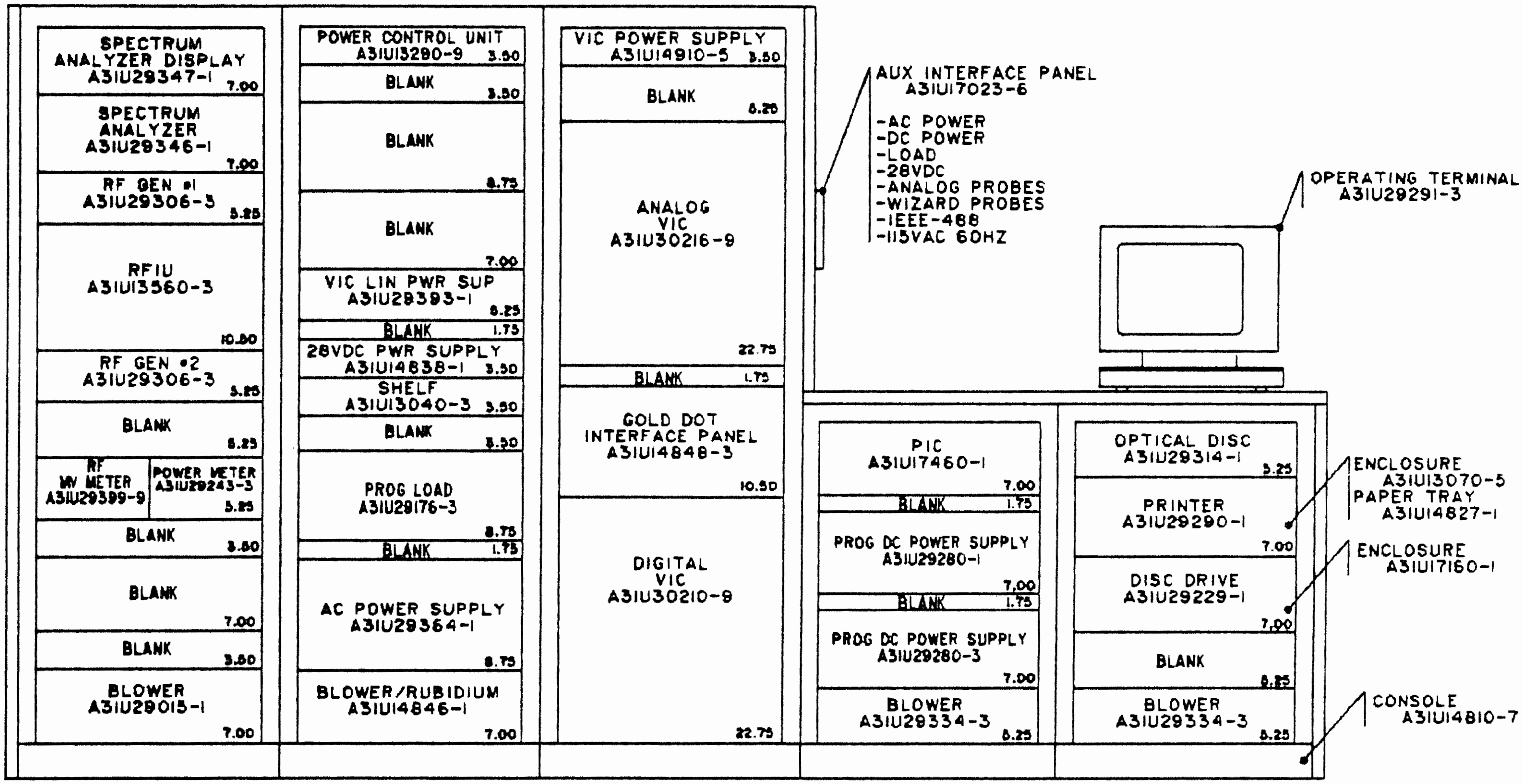
ANALOG VIC RESOURCES

MIPRCS CONTROLLER
TIMING GEN
DMM
AFG/CTR-TIM/DIGITIZER (5)
DISPLAY ANALYZER/SIMULATOR
UNIVERSAL SWITCH (6)
DAC/UTILITY SWITCH
SYNCH-RES SIM/IND

DIGITAL VIC RESOURCES

MIPRCS CONTROLLER
TIMING GEN
WIZARD PROBE
DWG I/O (16 PIN EA) (10)
BUS TEST UNIT
DWG HV (2)

COMMERCIAL EQUIVALENT EQUIPMENT-HAWK
A31U17000-109



ANALOG VIC RESOURCES

MIPRCS CONTROLLER
TIMING GEN
DMM
AFG/CTR-TIM/DIGITIZER (5)
DISPLAY ANALYZER/SIMULATOR
UNIVERSAL SWITCH (6)
DAC/UTILITY SWITCH
SYNCH-RES SIM/IND

DIGITAL VIC RESOURCES

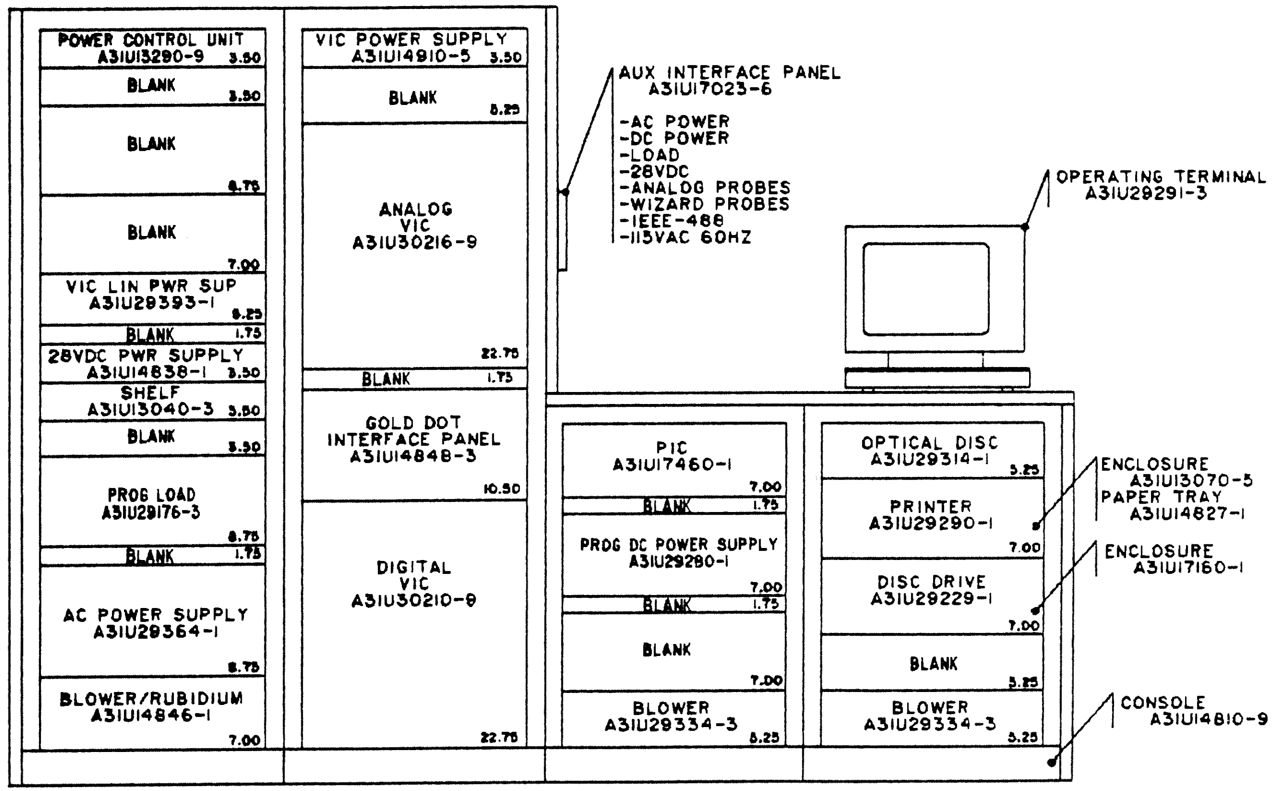
MIPRCS CONTROLLER
TIMING GEN
WIZARD PROBE
DWG I/O (16 PIN EA) (10)
BUS TEST UNIT
DWG HV (2)

APPV'D BY: REV A 04-25-90

ATE.IFTE.ELEVATION.CEE-109

FIGURE 1.5

COMMERCIAL EQUIVALENT EQUIPMENT-HYBRID
A31U17000-111



ANALOG VIC RESOURCES

MIPRCS CONTROLLER
TIMING GEN
DMM
AFG/CTR-TIM/DIGITIZER (5)
DISPLAY ANALYZER/SIMULATOR
UNIVERSAL SWITCH (6)
DAC/UTILITY SWITCH
SYNCH-RES SIM/IND

DIGITAL VIC RESOURCES

MIPRCS CONTROLLER
TIMING GEN
WIZARD PROBE
DWG I/O (16 PIN EA) (10)
BUS TEST UNIT
DWG HV (2)

REV A 4-25-90

ATE.IFTE.ELEVATION.CEE-111

FIGURE 1.6

1.4 PHYSICAL REQUIREMENTS

1.4.1 Power Requirements

External power applied must be three phase, wye configured, five wire (three phases plus neutral and ground), 120 ±10% VAC (line to neutral) at a frequency in the range of 47 Hz to 64 Hz, 50 amperes per phase. The pin assignments for the J1 connector are as follows:

PIN	FUNCTION
A	Phase A - 50 amps, max.
B	Phase B - 50 amps, max.
C	Phase C - 50 amps, max.
D	Neutral
E	Ground
F	Neutral
G	Neutral

The part number of the External Power Interface Connector J1 is MS3450W24-10P. Grumman provides cable P/N A31U17328-3 which connects to the J1 connector, consisting of seven wires, and is approximately 24 feet long, with the ends pigtailed for connections to facility power.

1.4.2 Environmental Requirements

The CEE shall be capable of withstanding the following environmental conditions:

A. Vibration and Shock - 10-33 Hz, 0.1 inches peak excursion

B. Operating Temperature - 10° C to 32° C

C. Non-Operating Temperature - -20° C to 65° C

D. Humidity - 80%, non-condensing

1.4.3 Mechanical Interface

The CEE sits directly on the floor, and requires no special mechanical interface. The footprint of the CEE -101, -103, -107 and -109 is shown in Figure 1.7. The weight is no greater than 3000 pounds. The footprint of the CEE -105 and -111 is shown in Figure 1.8. The weight is no greater than 2500 pounds.

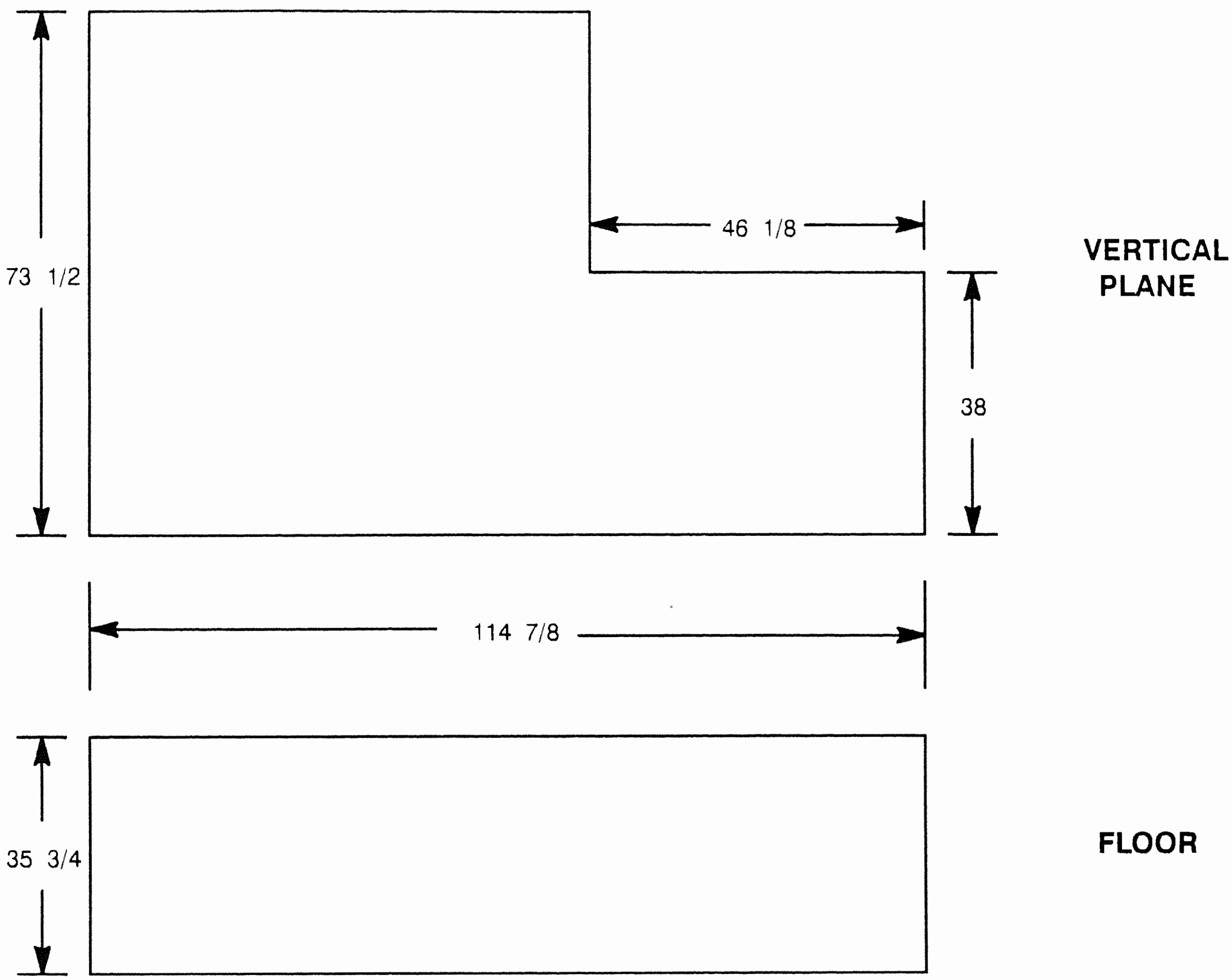


FIGURE 1.7

CEE FOOT PRINT

(-101, -103, -107, -109)

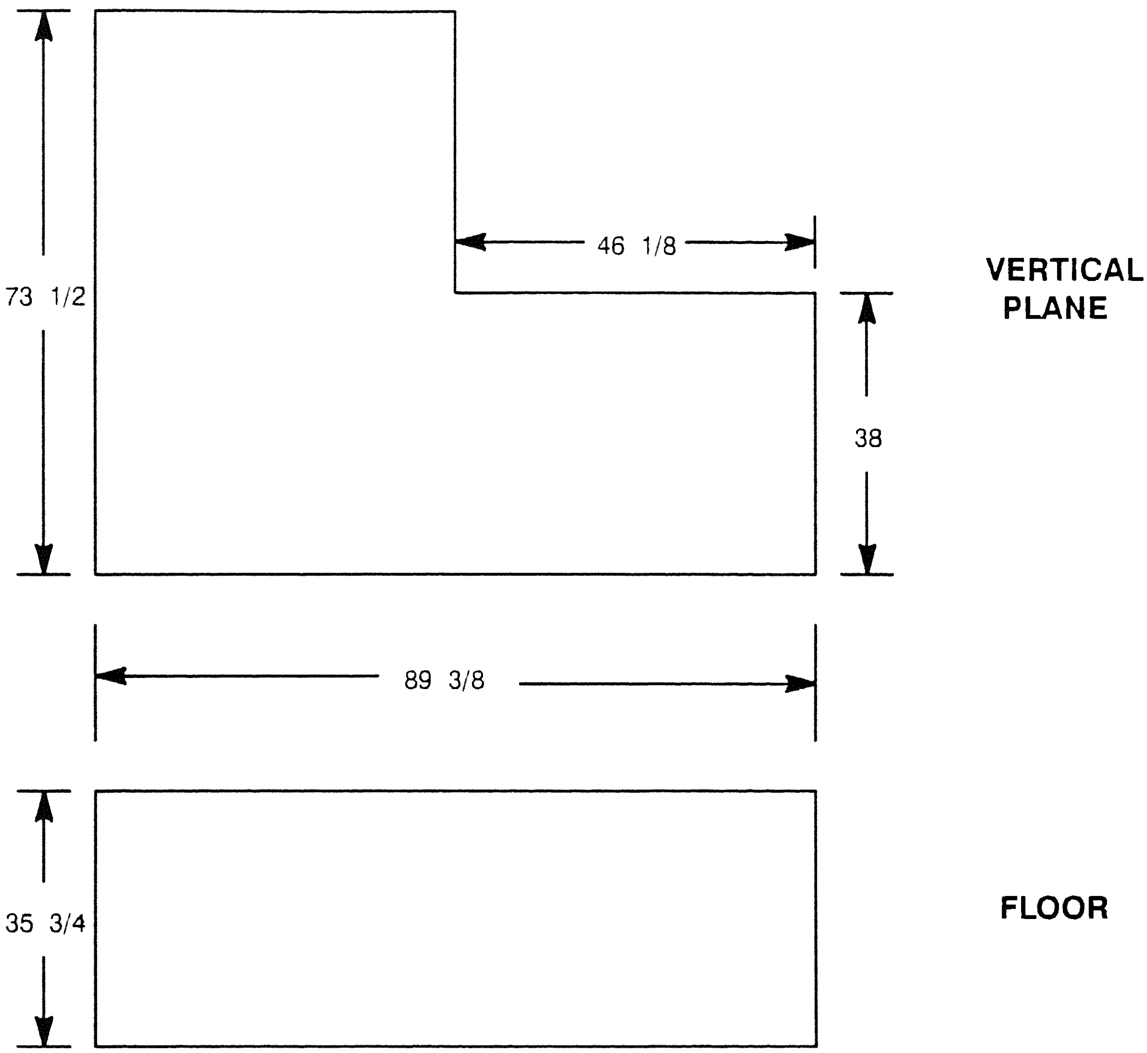


FIGURE 1.8

CEE FOOT PRINT

(-105, -111)

1.5 STATION TOP ASSEMBLY DRAWING

The station top assembly drawing (drawing number A31U17000) contains all part numbers on the CEE station.

1.6 SYSTEM INTERCONNECT

The interconnection block diagrams for the CEE are broken up into two figures. Figure 1.9 shows the bus structure and figure 1.10 shows the signal distribution of the CEE. Drawing number A31U17010 gives a more detailed picture of the System Interconnection and can be obtained from Grumman.

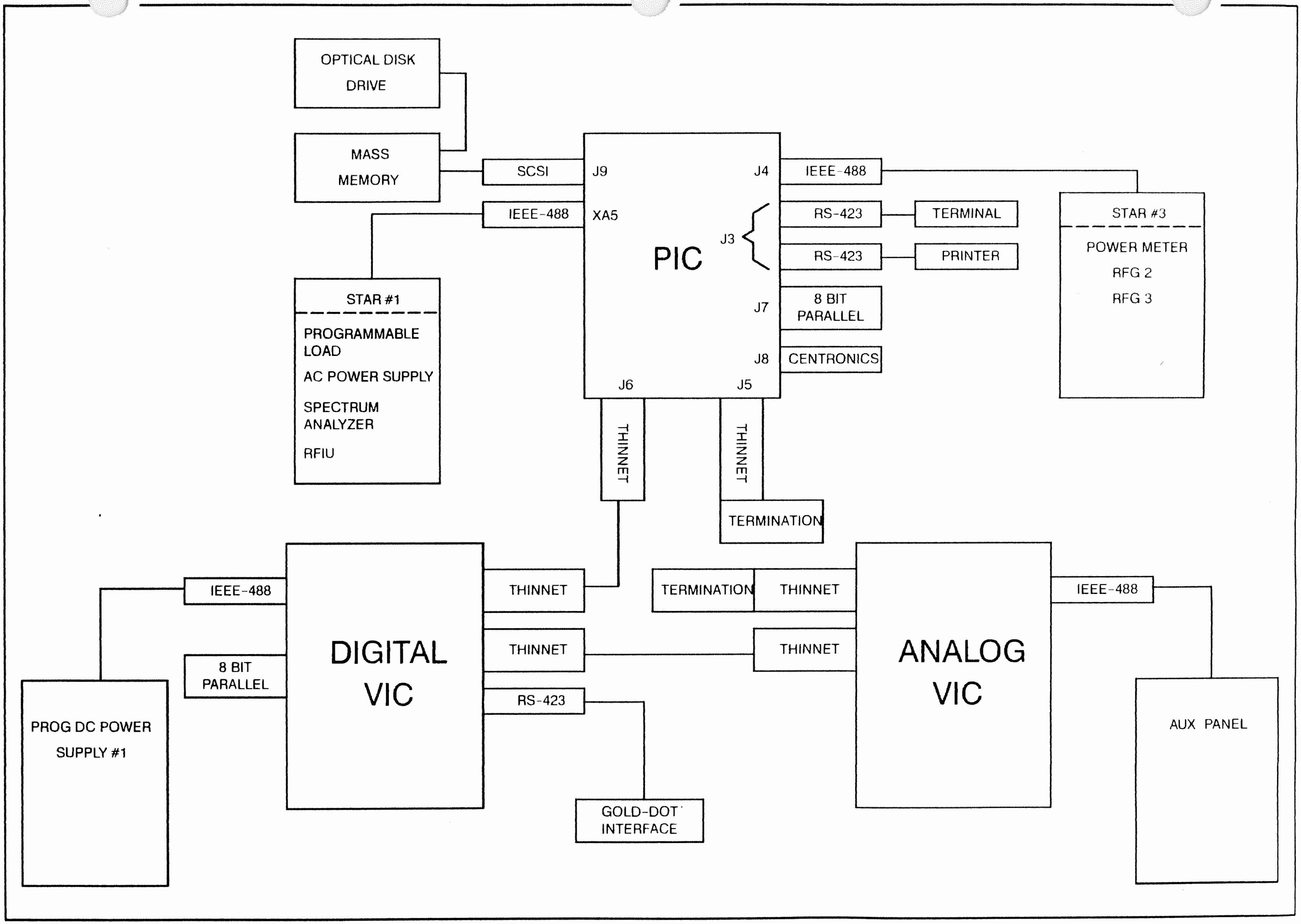


FIGURE 1.9A CEE BUS STRUCTURE (CEE -101, -107)

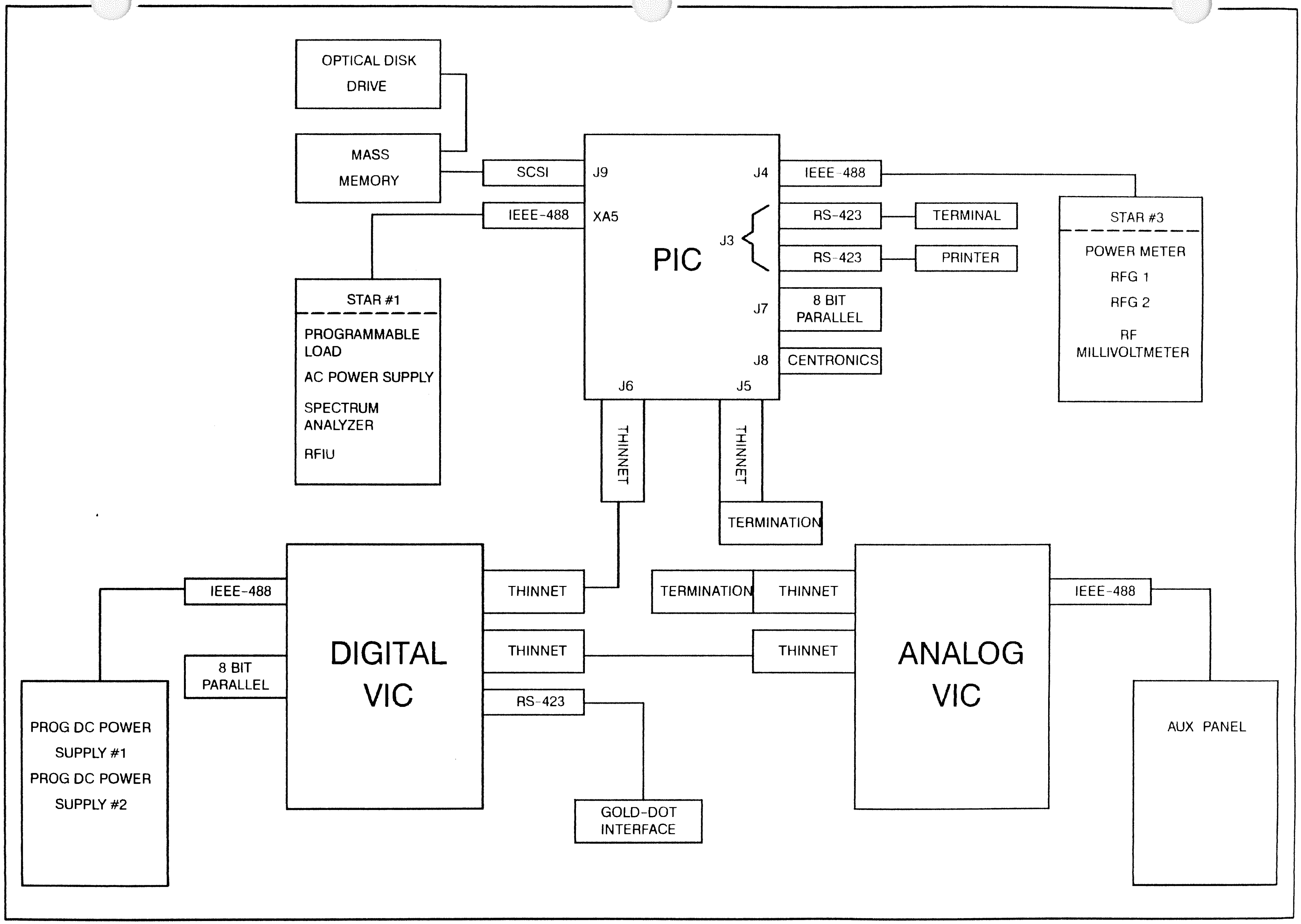


FIGURE 1.9B CEE BUS STRUCTURE (CEE -103, -109)

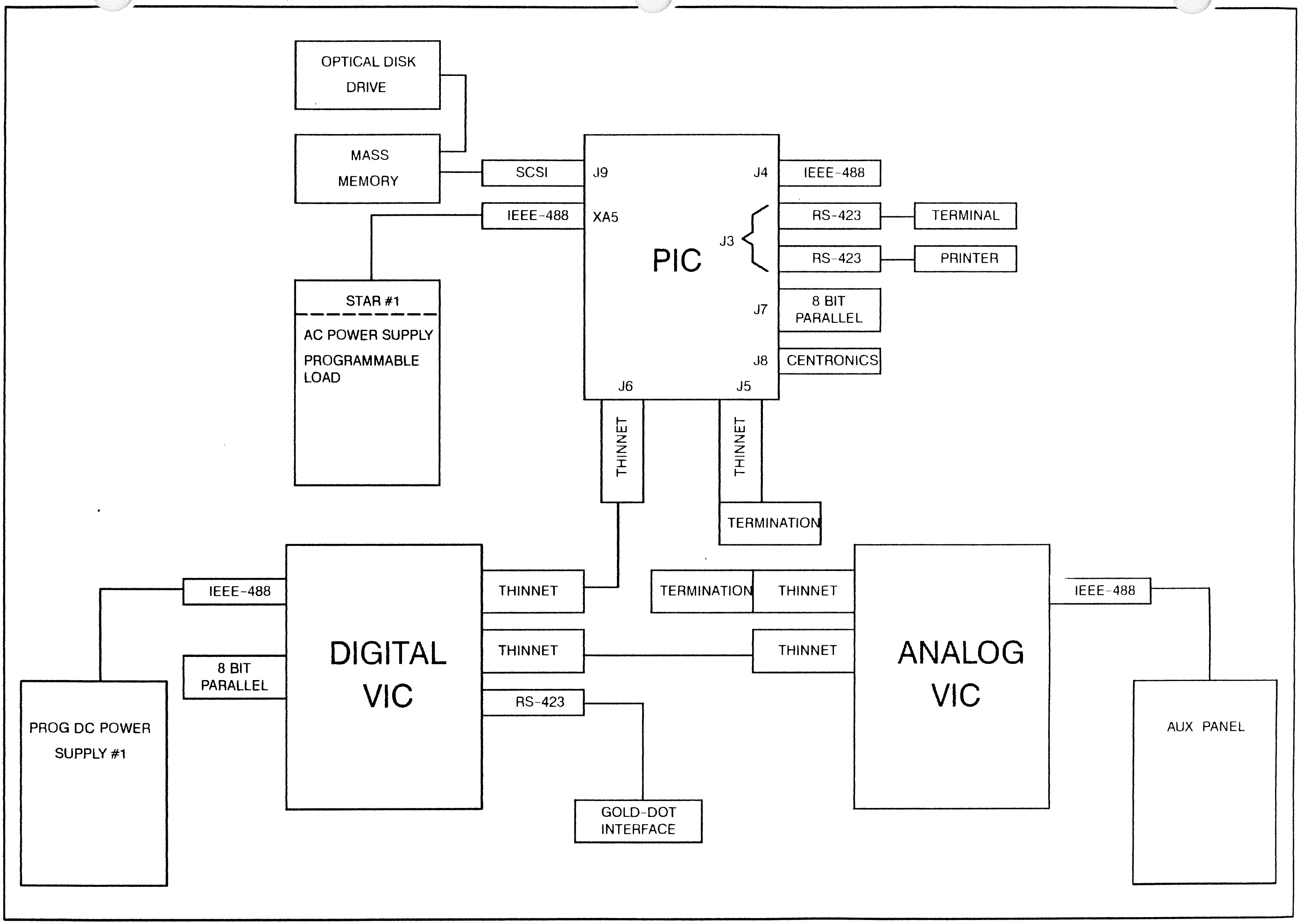


FIGURE 1.9C CEE BUS STRUCTURE (CEE -105, -111)

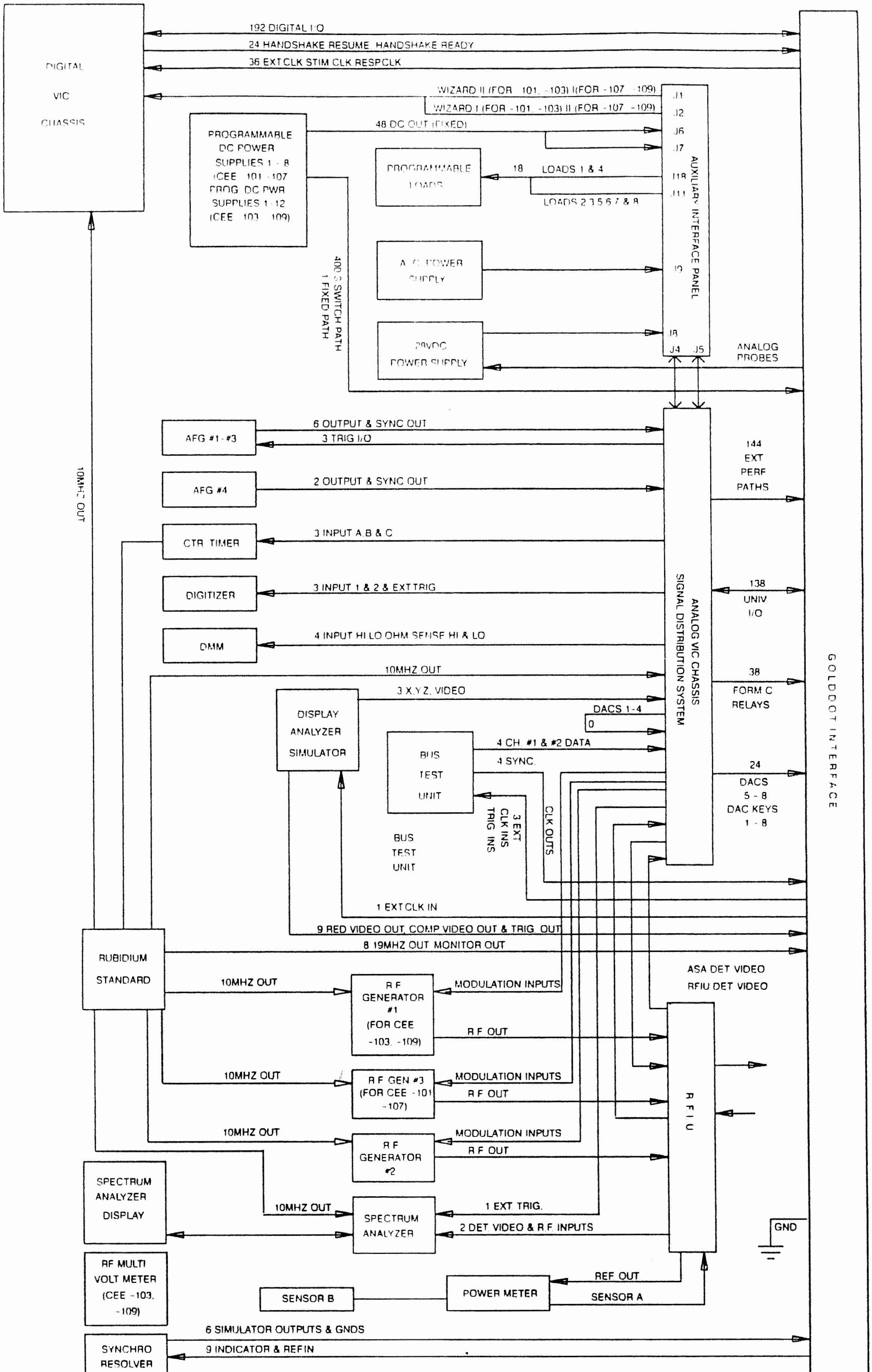


FIGURE 1.10A
CEE SIGNAL DISTRIBUTION
(CEE -101, -103, -107, -109)

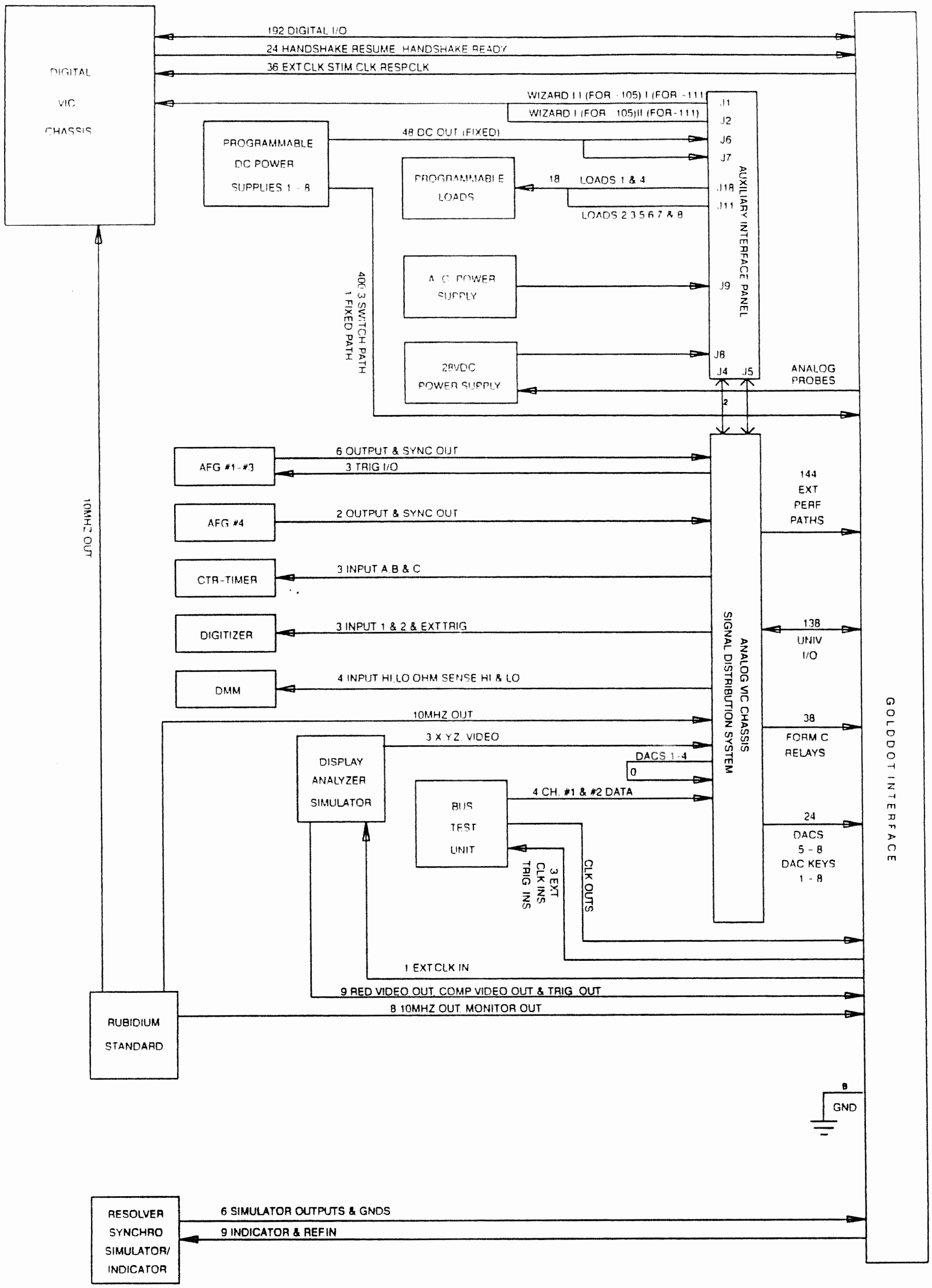


FIGURE 1.10B
CEE SIGNAL DISTRIBUTION
(CEE -105, -111)

2.0 CEE APPLICATIONS

2.1 CEE CONFIGURATIONS

For a savings in cost when less instrumentation or test capability is required, various configurations of the CEE have been created (CEE -101, -103, -105, -107,-109, -111) to meet the requirements of a specific testing application or of a particular maintenance scenario. All configurations maintain TPS transportability to the BSTS. Therefore, for a factory test environment, the same TPSs could be utilized from factory to field.

All CEE configurations must be restricted by the inclusion of that specific equpment which is integral to system operation and to the UUT and operator interfaces. In addition, there are restrictions intended to minimize changes to CEE hardware and software design, for which non-recurring engineering efforts would be required. The following paragraphs outline the common core of equipment/instrumentation used in all CEE configurations. Later sections will describe other resources and will indicate which specific configurations these resources are present in.

2.2 CEE Core Equipment

The equipment comprising the CEE core is integral to the hardware and software design and CEE system architecture.

2.2.1 Power Control Unit

The Power Control Unit is used to route and monitor power.

2.2.2 Peripheral Interface Controller (PIC)

The PIC is the CEE system controller. It performs the following functions:

(a) Controls system operation.

(b) Distributes processing and instrumentation control tasks.

(c) Interfaces to all system peripherals.

(d) Performs test executive functions.

(e) Establishes all system busses.

2.2.3 System Mass Memory

The CEE Mass Memory is an Amcodyne Disc Drive containing 100 MBytes total capacity, including a 20 MByte removable 8-inch cartridge. It interfaces to the PIC via a SCSI (Small Computer System Interface) bus.

2.2.4 UUT Interface

The principal UUT interface is via the Gold Dot Interface Panel. It is a pinless connector system less susceptible to damage than a conventional patch panel, and contains 3200 terminations in a greatly-reduced space. If TPS transportability to the BSTS is not required, an alternative UUT interface could be incorporated into a tailored CEE configuration.

In addition to the Gold Dot Interface Panel, the CEE contain an Auxiliary Interface Panel. The Auxiliary Interface Panel contains conventional connectors to provide additional interface capability for UUT testing. There is an IEEE-488 standard connector which can be used to interface an external instrument to the CEE. In addition, there are connectors for utilizing the Wizard and analog probes, and connectors to provide high-current paths to the DC power supplies, the AC power supply, and the programmable loads.

2.2.5 Virtual Instrument Chassis (VIC)

The Digital and Analog VICs provide the majority of the CEE's non-RF instrumentation, as well as serving as the Signal Distribution System (SDS). Each VIC contains a Resource Controller, which is the identical Common

Microprocessor/Controller card as the System Controller in the PIC, as well as a Timing Generator card. The balance of each VIC contains the appropriate digital, analog and switching resources.

2.2.5.1 Digital VIC

The configuration of the standard Digital VIC is shown in Figure 2.1. Each digital VIC contains a Common Microprocessor/Controller card, a Timing Generator card, and the following test resources:

- One (1) through ten (10) High-Speed Digital I/O card containing 16 pins per card, programmable from -10 to +10 volts, and capable of operation at up to 50 MHz.
- One (1) or two (2) High-Voltage Digital I/O cards containing 16 pins per card, programmable from -30 to +30 volts and capable of operation at up to 10 MHz.
- One (1) Bus Test Unit (BTU) card - 1553B Manchester-compatible.
- One (1) Wizard Probes I & II card containing the electronics for the CEE digital probes.

CHASSIS	CARD TYPE
1	uProc/Controller Card
2	High Speed Digital I/O Card
3	High Speed Digital I/O Card
4	High Speed Digital I/O Card
5	High Speed Digital I/O Card
6	High Speed Digital I/O Card
7	High Speed Digital I/O Card
8	High Speed Digital I/O Card
9	High Speed Digital I/O Card
10	High Speed Digital I/O Card
11	High Speed Digital I/O Card
12	High Voltage Digital I/O Card
13	High Voltage Digital I/O Card
14	Spare Slot
15	Spare Slot
16	Bus Test Unit Card
17	Wizard Probes I & II Card
18	Timing Generator Card

FIGURE 2.1 Virtual Instrument Chassis-Digital

2.2.5.2 Analog VIC

The configuration of a standard Analog VIC is shown in Figure 2.2. As in the Digital VIC, the Analog VIC contains the Common Microprocessor/Controller card and the Timing Generator. In addition, there are seven cards which together comprise the Signal Distribution (or switching) System (SDS) and which are contained in VIC slots 7 through 13 (of 18).

The SDS provides the capabilities of 130 Universal I/O pins, 144 Extended Performance I/O pins, 48 dedicated instrument ports, 32 form C relays, and eight precision DC references. It is inherently a key component of the switching flexibility designed into the compiler and run-time system software.

The Analog VIC also contains the following resources.

CHASSIS	CARD TYPE
1	uProc/Controller Card
2	Spare Slot
3	AFG/C-T/Digitizer Card
4	AFG/C-T/Digitizer Card
5	AFG/C-T/Digitizer Card
6	AFG/C-T/Digitizer Card
7	Univ/Ext. Perf. Pin Switch Card
8	Univ/Ext. Perf. Pin Switch Card
9	Univ/Ext. Perf. Pin Switch Card
10	Univ/Ext. Perf. Pin Switch Card
11	Univ/Ext. Perf. Pin Switch Card
12	Univ/Ext. Perf. Pin Switch Card
13	DACS/Utility Switch Card
14	Synchro-Res/Simulator-Indicator Card
15	AFG/C-T/Digitizer Card
16	DMM Card
17	Display Analyzer/Simulator Card
18	Timing Generator Card

FIGURE 2.2 Virtual Instrument Chassis-Analog

3. OPERATING INSTRUCTIONS

3.1 SYSTEM INITIALIZATION

The CEE automatically initializes itself during power turn-on. (See paragraph 3.2). To reinitialize the station, the user types in the following commands (NOTE: all entries are lower case and are bracketed [ ]):

At the CEE TPS User Interface,

enter [stop] - press return.

At the > prompt,

enter [b] - press return.

The prompt, login: will appear after a short wait. The user will enter:

[ifte] - press return.

After following instructions on screen for date and time update, the prompt for a user-name will appear. Enter [station]

The prompt for a password will appear. Enter [station]

The CEE TPS user interface prompt will appear and the user can run test programs or any of the resident software.

3.2 POWER TURN ON PROCEDURE

To turn on the CEE, the following steps are to be performed (NOTE: all entries are in lower case and are bracketed [ ]):

1. Turn on Circuit Breakers on the Power Control Unit.

2. Press the ON switch on the Power Control Unit.

3. Wait while the station initializes.

4. When the prompt CEE login appears, enter: [ifte] -press return.

3.3 POWER TURN OFF PROCEDURE

To power down the CEE;

At the CEE TPS user interface, type in:

[halt] - press return.

This command will park all the heads on the disk drives. The user then can press the OFF switch on the Power Control Unit and switch the Circuit Breakers to the OFF position.

3.4 PROGRAM EXECUTION

3.4.1 Mounting The Removable Pack

To mount the removable pack, the user must first install the disk in the disk drive and set the START/STOP switch to the START position. Wait for the ready light to illuminate.

3.4.2 Removing the Removable Pack

To remove the removable pack, the user enters the [stop] command from the CEE TPS user interface and waits for the prompt to appear.

When the > prompt is displayed, the user can set the START/STOP switch to the stop position and, after the LOAD indicator illuminates, remove the pack.

3.4.3 Running a Program

After station initialization and login, the station will automatically enter the system user interface.

The operator will then be given a menu of execution options (CEE TPS DEVELOPMENT TOOL MENU). Select the test program execution option. (Ref IFTE Programmers Ref.Manual P/N IFTE85E2101).

This will get the user into the ATLAS Execution System. At the prompt (!) type [run (filename)] and press return. When you are finished executing the program, type: [exit] then press return. This will bring the user back to the user interface. For more information about running programs or mounting and removing disks, see IFTE Programmers Reference Manual P/N IFTE85E2101.

4. OPERATIONAL CHARACTERISTICS

4.1 POWER SUBSYSTEM

4.1.1 Power Control Panel

(1) Controls: Power ON/OFF Switches, Power ON Indicator, Elapsed Time Meter, Voltmeter.

(2) Over Voltage Shut Down: If voltage changes more than 10 volts from nominal 115 VRMS.

4.1.2 AC POWER SUPPLY

The AC Power Supply has programmable output voltage, current-limit, frequency and phase angle capability. The following types of outputs are available to the UUT at J9 of the Auxiliary Interface Panel with the following output voltage and current:

(1)

Voltage Range (L-N)	Voltage Resolution	Maximum Continuous Current	Maximum Allowable Current	Current Limit Resolution
0.0 to 135.0V	0.0342V	6.25A	10.0A	0.1A
0.0 to 270.0V	0.0684V	3.125A	5.0A	0.1A

(2) Output Voltage Accuracy: ±0.5% of full scale voltage range

Output Current Limit Accuracy: ±2% of maximum allowable current

(3) Output Regulation (no load to full load): 0.5% full scale

The frequency and phase angle are programmable with the following ranges:

(4) Output Frequency:

Frequency Range	Frequency Resolution
45.0 to 999.9 Hz	0.1 Hz
1000 to 5000 Hz	1.0 Hz

(5) Output Frequency Accuracy: 0.5% of programmed value.

(6) Phase Angle Relationship:

A. Individual Phases: Phase B and Phase C lag Phase A, and are individually programmable from 0° to 360° with a resolution of 1 degree.

B. Accuracy: ±(1° + 1° per KHz or fraction thereof).

4.1.3 PROGRAMMABLE DC POWER SUPPLIES

There are 8 floating, bipolar DC power supplies (an additional 4 in the CEE -103 and -109). All of the power supplies are brought to the gold dot interface through power relays, and to J6 and J7 of the Auxiliary Interface Panel (the additional 4 of of the CEE -103 and -109 are brought to J9). All supplies have remote sensing for maintaining a constant voltage at the interface. The sense leads are available at the gold dot interface and the auxiliary interface panels. If the sense leads are not connected, the power supplies will operate using internal, local sensing only.

(1) Voltage Range and Maximum Current:

A. 2 @ 0-7V, 20.5A

B. 2 @ 0-16V, 9.1A

C. 1 @ 0-36V, 4.1A

D. 2 @ 0-55V, 2.8A

E. 1 @ 0-100V, 1.5A

F. 4 @ 0-200V, 0.75V (CEE -103 and -109 only)

(2) Resolution: 10 mv or (1/4096) x max. voltage; whichever is greater

(3) Accuracy: ±0.5% programmed value or ± 10 mv; whichever is greater

NOTE: Accuracy specification is valid only when using remote sensing.

(4) Configuration: All power supplies are floating and bipolar.

(5) Ripple and Noise: 12 millivolts p/p max.

4.1.4 28 VDC POWER SUPPLY

The 28 VDC Power Supply has a fixed voltage output of 28 volts DC ±5% with a maximum current rating of 22.5 amperes.

When gold dot pins H51 and G51 are not connected (open), the 28 VDC power supply is turned off. When gold dot pins H51 and G51 are shorted via a relay or switch closure in the Test Program Set (TPS) ICD, the 28 VDC power supply is turned on. It will remain on until the connection between gold dot pins H51 and G51 is opened, at which time the 28 VDC power supply will be turned off. The 28VDC Power is available to the UUT at the Auxiliary Interface Panel via the J8 connector. Overvoltage and overcurrent protection is provided with this supply.

4.1.5 PROGRAMMABLE DC LOAD

The programmable DC loads provide eight individually programmable active load channels. Each load is programmed over the IEEE-488 bus. Each channel is available through a dedicated pair of pins at connectors J10 and J11 on the Auxiliary Interface Panel. The following load characteristics are available at the Auxiliary Interface Panel as shown in Table I.

TABLE I

Programmable Load Characteristics

Characteristics	Load 1	Load 2	Load 3	Load 4	Load 5	Load 6	Load 7	Load 8
Maximum voltage	50V	50V	50V	50V	130V	130V	130V	250V
Minimum compliance voltage	3V	3V	3V	3V	7V	7V	7V	10V
Maximum current	30A	15A	15A	30A	15A	15A	15A	5A
Maximum power 1/	750W	300W	300W	750W	750W	750W	750W	750W

1/ Maximum power dissipation for simultaneous use of load channels must not exceed 3000 watts. Where power dissipation is less than 1000 watts, duty may be continuous. Where power dissipation is greater than 1000 watts, duty cycle is limited to 3 minutes ON followed by 2 minutes OFF.

(1) Load current programming resolution is the load channel's maximum current divided by 1023.

(2) Any combination of loads may be operated in parallel to achieve a higher value load capability (current or power) provided that no individual load specifications are exceeded.

(3) The maximum load current accuracy is 5% of programmed value or 1.0% of full rated current, whichever is greater.

(4) Any or all loads may be modulated by a single source from a pin on J11 on the Auxiliary Interface Panel. The modulating signal's peak positive and peak negative excursions must be in the range of 0 to +10 volts and will program the selected channel(s) for 0 to a maximum rated current, respectively.

(5) The impedance of the modulating signal input depends upon the number of load channels (N) programmed as follows:

$$Z_{in} = 10/N \text{ Kohms}$$

where N = 1 to 8

(6) The loads contain built-in protection for overvoltage, overcurrent and overpower.

4.1.6 VIC Power Supply

The VIC Power Supply provides ±15VDC and +24VDC power for internal use by the VIC instruments and the VIC signal distribution system. This supply is not intended to provide power to units under test.

4.1.7 VIC Linear Power Supply

The VIC Linear Power Supply provides ±15VDC linear power for internal use by the Analog VIC instruments. These supplies are not intended to provide power to units under test.

4.1.8 List Of Power Subsystem Elements

Instrument	Qty.	MFG	Part Number
Prog. DC Power Supply	1	Elgar	5801237-01, 5702007-01
Prog. Load	1	Trans. Devices	SPS3102-1
AC Power Supply	1	NH Research	P2209
Power Control Unit	1	Grumman	A31U13290-9
VIC Power Supply	1	Grumman	A31U14910-3, -5
28V Power Supply	1	Grumman	A31U14838-1

4.2 CONTROL SUBSYSTEM

4.2.1 Peripheral Interface Controller

The Peripheral Interface Controller (PIC) contains a 32 Bit Motorola 68020 microprocessor with a Motorola 68881 as a coprocessor on a Sun Micro-systems board. The system clock operates at 16.67 MHz. The memory for the PIC is made up of 4M Bytes of on board dynamic memory, but can access 2 gigabytes of VME address space. The operating system for the PIC is UNIX. The PIC communicates with the peripherals through the following Buses:

(1) Small Computer System Interface (SCSI)

(2) IEEE-488

(3) RS-423 Serial Data Bus

(4) IEEE-802.3 bus (Thinnet)

(5) Centronics Interface

(6) High Speed 8 Bit Differential Parallel Data Bus

(7) VME Bus

Communication between the PIC and the Analog and Digital VIC's is achieved by a daisy-chained Thinnet Bus. The mass memory is an Amcodyne disk drive connected to the PIC via the SCSI Bus. There are four IEEE-488 buses, two connected to the PIC, one to the analog VIC and one to the Digital VIC. The Terminal and the Printer are connected to the PIC by two RS-423 buses.

4.3 USER INTERFACE

4.3.1 Terminal

The Terminal consists of a colorgraphic's CRT, a graphics generator, a keyboard, and an IR Touch Screen with the following characteristics:

(1) Screen Size: 13 inch diagonal

(2) Type: 60 Hz non-interlaced raster scan

(3) Modes: Alphanumeric and Colorgraphics

(4) Alphanumeric Display Capacity: 24 lines x 80 columns

(5) Graphics Display Capacity: 640 x 480 pixel.

(6) Color: 16 colors displayable simultaneously

(7) Cursor Type: Blinking underline for Alphanumeric. Crosshair for graphics

(8) Graphics Primitives: Point, vector, rectangle, polygon, circle, arc and pie segment drawing, 30 fill patterns, 5 line types

(9) Keyboard.

(10) Touch Screen (IR): 48 x 32 matrix, scan rate of 20 frames per second, resolution 0.125 inches.

4.3.2 Printer

(1) Number of characters/line: 80

(2) Type of Printer: Ink Jet

(3) Speed: 150 characters/second

(4) Resolution: 96 x 96 dots/inch

(5) Paper: 8.5 x 11 inches (trimmed), fan fold

4.3.3 Disk Drive

(1) Computer Interface: Small Computer System Interface (SCSI)

(2) Uses three dual surface fixed disks and one dual surface removable disk cartridge

(3) Disk Cartridge Size: 8 inches (diameter)

(4) Disk Data Surfaces: 8 (6 fixed, 2 removable)

(5) Disk Cartridge Formatted Storage Capacity: 20 Mbytes

(6) Fixed Disk Formatted Storage Capacity: 20 Mbytes/disk

(7) Total Disk Drive Formatted Storage Capacity: 80 Mbytes

(8) Total Disk Drive Unformatted Storage Capacity: 100 Mbytes

4.3.4 Optical Disk Drive

(1) Computer Interface: Small Computer System Interface (SCSI)

(2) Uses removable disk cartridges as storage media

(3) Disk cartridge size: 5.25 inches (diameter)

(4) Disk cartridge data surfaces: 2

(5) Disk Cartridge User Storage Capacity: 200 Megabytes per surface

(6) Read/Write Technology; Write-once-read-many (WORM).

4.4 ANALOG/VIDEO SUBSYSTEM

4.4.1 Digital Multimeter

The Digital Multimeter consists of 5½ digits with the following specifications:

(1) DC Voltage Measurement:

RANGE	RESOLUTION	ACCURACY	INPUT IMPEDANCE
300V	1 mv	0.024% input + 10 digits	10 Megohms
100V	1 mv	0.024% input + 10 digits	10 Megohms
10V	100 uv	0.012% input + 10 digits	10 Gigohms
1V	10 uv	0.012% input + 10 digits	10 Gigohms
0.1V	1 uv	0.012% input + 10 digits	10 Gigohms

NOTE: The input to the 300V range is limited to 200V.

(2) AC Voltage Measurement (AC Coupled Input):

RANGE	RESOLUTION	INPUT IMPEDANCE
300V	1 mv	1 Megohm, 100 pF
100V	1 mv	1 Megohm, 100 pF
10V	100 uv	1 Megohm, 100 pF
1V	10 uv	1 Megohm, 100 pF
0.1V	1 uv	1 Megohm, 100 pF

ACCURACY

10 Hz to 30 Hz	0.6% input + 120 digits
30 Hz to 100 Hz	0.12% input + 50 digits
100 Hz to 20 KHz	0.12% input + 50 digits
20 KHz to 100 KHz	0.36% input + 120 digits
100 KHz to 300 KHz	3.6% input + 360 digits
300 KHz to 1 MHz	12% input + 1200 digits

NOTES: (1) Performance is specified for signals greater than 1% of range.
(2) For DC - coupled voltage measurements, add 0.5% of DC input plus 600 digits.
(3) The input to the 300V range is limited to 200V peak.

(3) Ohms Measurement:

RANGE	RESOLUTION	ACCURACY
10 Mohm	100 ohm	0.12% input + 10 digits
1 Mohm	10 ohm	0.06% input + 10 digits
100 Kohm	1 ohm	0.024% input + 10 digits
10 Kohm	100 mohm	0.02% input + 10 digits
1 Kohm	10 mohm	0.02% input + 10 digits
100 ohm	1 mohm	0.02% input + 10 digits

Specifications are for four-wire ohms measurement. For 2-wire, degrade by 2 ohms plus external lead resistance.

(4) Autoranging - all functions have autoranging

4.4.2 High Frequency Probe

The High Frequency Probe is used in conjunction with the Digital Multimeter (DMM). The probe is connected to either the J4 or J5 connector on the auxiliary interface panel.

The High Frequency Probe has the following characteristics:

(1) Function: Converts DC voltmeter to high-frequency AC voltmeter

(2) Input Voltage Range: 0.25 to 30V RMS

(3) AC to DC Transfer Accuracy (when loaded with 10 megohms ±10%):

A. 100 KHz - 100 MHz: ±0.5 dB

B. 100 MHz - 500 MHz: ±1.2 dB

(4) Input Impedance: 4 Mohms shunted by 3 pF maximum.

4.4.3 Arbitrary Function Generator (AFG)

(1) Number of Channels: 1 per card, 4 cards total.

(2) Standard Waveshapes programmable by parameters: Sine, Triangle, Square, Pulsed DC, DC

(3) In the Arbitrary Function mode, user defined custom waveforms can be created as a series of segments with individually specified amplititudes.

(4) Trigger Function: External pulse initiates the generation of a single shot waveform. Subsequent triggers repeat the generation of the waveform.

A. Input Impedance: 1 megohm

B. Max Input Voltage: ±5 volts

(6) Sync Output: A TTL Output in sync with the programmed output, and capable of driving a 50 ohm load

(7) Output Amplitude: 0 to 10 Vpp into 50 ohm load (200 mA maximum drive current)

(8) Source Impedance: 50 ohms

(9) Pulse Mode Parameters

A. Frequency Range: 0.02 Hz to 25 MHz

B. Frequency Resolution: 20 nanosec

C. Frequency Accuracy: ±0.001% of programmed value

D. Pulse Width: 20 nanoseconds to 39.995 seconds

E. Delay: -180 degrees to +180 degrees

F. Delay Resolution: 0.1 degree

G. Delay Accuracy: ±0.5 degree

H. Rise/Fall Time: less than 50 nanoseconds

I. Amplitude: 50 millivolts to 20 volts peak-to-peak into high impedance (10V peak-to-peak into 50 ohms)

J. Amplitude Resolution: 0.5% of Range

K. Amplitude Accuracy: +/- (4% of Programmed Value + 15 mV)

L. Offset: -10 volts to +10 volts into high impedance (the absolute value of output voltage plus offset shall be 10 volts)

M. Offset Resolution: 5 mV

N. Offset Accuracy: +/- (5% of Programmed Value + 20 mV)

(10) Fixed Waveform Mode Parameters

A. Waveforms: Square, Sine, Triangle

B. Frequency: 0.2 Hz to 2 MHz for sine and triangle

0.005 Hz to 25 MHz for square

C. Frequency Resolution: 20 nanosec

D. Frequency Accuracy: ±0.001% of programmed value

E. Amplitude: 50 millivolts to 20 volts peak-to-peak into high impedance (10 volts peak-to-peak into 50 ohms)

F. Offset: -10 volts to +10 volts into high impedance (the absolute value of output voltage plus offset shall be less than 10 volts)

G. Amplitude Resolution: 0.5% of range

H. Amplitude Accuracy: +/- (5% programmed value + 15 mV) for Sine Wave, +/- (4% programmed value +15 mV) for Square Wave

+/- (6% programmed value +15 mV) for Triangle Wave

I. Offset Resolution: 5 mV

J. Offset Accuracy: +/- (5% of programmed value + 20 mV)

(11) Arbitrary Waveform Mode Parameters

A. Segment Time Duration: 20 nanosec to 42 sec.

B. Segment Time Resolution: 20 nanosec

C. Number of Equal Time Segments: 2 to 4096

D. Segment Time Accuracy: ± (0.005% of programmed value + 5 nanosec)

E. Segment Amplitude: 50 mV to 20V peak-to-peak into high impedance (10V peak-to-peak into 50 ohms)

F. Segment Amplitude Resolution: 0.5% of Range

G. Segment Amplitude Accuracy: +/- (6% of programmed value +15 mV)

H. Offset: -10V to +10V into high impedance (the absolute value of output voltage plus offset shall be 10 volts).

(12) Output Impedance (All modes): 50 ohms

4.4.4 Counter-Timer

(1) Input Signal Frequency (Into 50 ohm Input Impedance):

A. DC Coupling - DC to 100 MHz

B. AC Coupling - 20 Hz to 100 MHz

NOTE: for 1 Mohm input impedance, upper frequency is 50 MHz

(2) Display (equivalent): 8.5 digits

(3) Frequency Range: DC to 100 MHz

(4) Time Interval and Period Range: 100 ns to 10,000 seconds

(5) Input Voltage Range: 100 mV to 200V (7V with 50 ohm input impedance)

(6) Input Impedance: 50 ohms (2 watts) or 1 Mohm (1/8 watt)

(7) Input Coupling: DC or AC

(8) Trigger Slope: positive or negative

(9) Standard Functions:

A. Frequency

B. Period/Period Average

C. PRF

D. Time Interval/TI Average

E. Totalize (Count Events)

F. Pulse Width

G. Rise Time

H. Fall Time

I. Duty Cycle

J. Phase Angle

(10) Number of Input Channels: 2(A,B)

(11) External Gate Input:

A. Impedance: Greater than 1 Kohm or 50 ohm

B. Input Voltage: +7, -0.5 volts DC

(12) Accuracy:

A. Frequency measurement accuracy:

±1 count ± time base error

B. Time measurement accuracy:

±10 ns ±1 count ± time base error

C. Time base error:

Less than 12 parts in million per year

D. Phase angle accuracy:

± Freq Measurement accuracy ± Time Interval measurement accuracy

4.4.5 <u>Digitizer</u>

(1) Number of Channels - two

(2) Input Voltage Range:

A. ±100 mv to ±7 volts with 50 ohm input impedance in the following ranges:

1. Greater than 2 MHz sampling rate: 1, 2, 2.5, 4, 5, 8 and 10 volt ranges

2. Less than or equal to 2 MHz sampling rate: 2.5, 5, 6.25, 10, 12.5, 20 and 25 volt ranges

B. ±100 mv to ±100 volts with 1 Mohm input impedance in the following ranges:

1. Greater than 2 MHz sampling rate: 1, 2, 5, 10, 20, 50 and 100 volt ranges

2. Less than or equal to 2 MHz sampling rate: 2.5, 5, 12.5, 25, 50, 125 and 250 volt ranges

(3) Input Impedance: 50 ohm (2 watt) or 1 Mohm (1/8 watt)

(4) Amplitude Resolution:

A. 12 bits for sampling frequency equal to or less than 2 MHz

B. 8 bits for sampling frequency greater than 2 MHz to 100 MHz

(5) Amplitude Measurement Accuracy:

A. ±6% of full scale of input voltage range*, DC to 1 MHz input signal frequency.

B. ±15% of full scale of input voltage range*, 1 MHz to 25 MHz input signal frequency.

C. ±25% of full scale of input voltage range*, 25 MHz to 50 MHz input signal frequency.

* NOTE: Input voltage ranges are defined above.

(6) Sampling Interval: 10 nanoseconds to 42.9 seconds in 10 nanosecond intervals.

(7) Sample Storage Depth: 1001 samples maximum

(8) Input Channel B.W.: 50 MHz at 50 ohms

(9) Trigger Mode:

A. Internal or external

B. Trigger Delay: 0 to 42 seconds in 10 nsec increments

(10) External Trigger Input:

A. Input Impedance: 50 ohms and greater than 3 Kohms

B. Max input voltage: +7, -0.5 volts DC

(11) Automatic Measurement: Positive Peak, Negative Peak, Peak to Peak, True RMS voltage

4.4.6 Display Analyzer-Simulator

A. Functions: The display anayzer-simulator (DAS) is a multi-format video display generator. Composite with any possible sync format, rectilinear and polar raster, multi-image interactive stroke, and mixed video (stroke over composite, or stroke over raster) are all supported by the DAS. The DAS also supports video image acquisition (for all video formats) and sync processor/analyzer functions.

B. System Time Base: The DAS uses a phase locked loop type frequency synthesizer as its time base.

1. Frequency: 1 Hz to 40 MHz
2. Resolution: ±0.05%
3. Accuracy: ±0.005%
4. Time base is directly accessible at the Gold-Dot interface as a digital singal (20 MHz max)
5. An external clock source may be used as the time base (20 MHz max).

C. Composite video/raster generator (CVRG):

1. Composite video:

a. Pixel time = $\dfrac{1}{\text{time base frequency}}$

(Maximum time base frequency = 40 MHz)

b. Video memories:

(1) Horizontal parameter memory: 4K x 12

(2) Vertical attribute memory: 4K x 6

(3) Pixel depth: 4 bits

c. Horizontal timing: Programmable from 2 to 8192 pixel times with granularity equal to two pixel times

(1) The horizontal line may be arbitrarily divided into active display time and blanking time

(2) The blanking time may be arbitrarily divided into front porch, back porch, and sync times

d. Vertical timing: Programmable from 2 to 4096 horizontal half-lines with granularity equal to one horizontal half-line

(1) Vertical timing may be arbitrarily divided into active display time and blanking time

(2) Vertical sync time may be any time not greater than the vertical blanking time

(3) Vertical sync pulse may be located anywhere within the blanking time. Equalizing and broad pulses may be added as required and are subject to the same granularity as horizontal parameters

e. Video output:

(1) Signal amplitude: 0 to 4 volts peak-to-peak

(2) White positive or white negative

(3) Offset: -4 volts to +4 volts

(4) Output range: -4V less than or equal to (Signal Offset) less than or equal to +4V

(5) Bandwidth: 20 MHz

(6) Voltage accuracy: 20mV or 2% whichever is greater

f. Video pattrn algorithms: The composite video shall create patterns by the operation of a set of two-dimensional vectors [(horz-size, vert-size), (horz-repetition, vert-repetition) and (horz-position, vert-position)], and single valued parameters (width and z-modulation) upon one of the following pattern primitives:

(1) RGB/greyscale (one dimensional repetition only)

(2) Border (repetitions limited to 1 or 0)

(3) Bar

(4) Dot

(5) Checkerboard

Two patterns are simultaneously available in a master-slave relationship. The slave output must follow the sync format and timing as the master output.

2. Raster video portion of CVRG:

a. Three independent output channels:

(1) X - Horizontal deflection

(2) Y - Vertical deflection

(3) Z - Intensity modulation

b. Video memories:

(1) X - 4K x 10

(2) Y - 4K x 10

(3) Z -4K x 9 video data/blanking

(4) 4K x 6 line attribute

c. Time base frequency (maximum): 20 MHz (10 MHz polar)

d. The raster display may be generated in either rectilinear or polar coordinate reference frame.

e. Raster Outputs (Z-intensity):

(1) Signal amplitude: 0 to 3 volts peak-to-peak

(2) White positive or white negative

(3) Offset: -4 volts to +4 volts

(4) Output range: -4V less than or equal to (Signal + Offset) less than or equal to +4V

(5) Bandwidth: 20 MHz

(6) Voltage accuracy: 20 mV or 2% whichever is greater

f. Raster Outputs (X-horizontal deflection, Y-vertical deflection):

(1) Signal amplitude: 0 to 8 volts peak-to-peak

(2) Offset: -4 volts to +4 volts

(3) Output range: -4V less than or equal to (Signal + Offset) less than or equal to +4V

(4) Bandwidth: 20 MHz

(5) Voltage accuracy: 20 mV or 2% whichever is greater

g. Video pattern algorithms are the same as for monochrome composite video.

D. Stroke Video

1. Three output channels:

a. X - Horizontal deflection

b. Y - Vertical deflection

c. Z - Intensity modulation

2. Video memories:

a. X: 32K x 12

b. Y: 32K x 12

c. Z: 32Kx 6

d. Control: 256 x 32

3. Time base frequency (maximum): 5 MHz

4. An external clock source may be used as a separate time base for the stroke video section without affecting the system time base.

5. Stroke Outputs:

   a. Signal amplitude: 0 to 8 volts peak-to-peak

   b. Offset: -4 volts to +4 volts

   c. Output range: -4V less than or equal to (Signal + Offset) less than or equal to +4V

   d. Bandwidth: 20 MHz

   e. Voltage accuracy: 20 mV or 2% whichever is greater

6. Stroke Pattern Algorithms:

   The stroke section can generate any pattern that can be expressed as an arbitrary series of points connected by either blanked or unblanked lines. The stroke section can store and output a continuous series of patterns. Each pattern in a series may be either internally controlled, where the individual pattern repeats for a user defined number of repetitions, or externally controlled where the individual pattern repeats until an external trigger is received. This intermixing of internally controlled and externally controlled patterns allows the simulation of interactive display control.

E. Image acquisition:

1. Input video buffers:

a. Three Channels: 0, 1, 2

Channel 0: CVIA input or RSIA X-MOD input

Channel 1: RSIA Y-MOD input

Channel 2: Sync processor input or RSIA Z-MOD input

b. Impedance: 75 ohms (fixed)

c. Input attenuation: 1:1 or 1:0.268

d. Gain: 0 to 3.75 in 16 steps of 0.25 per step

e. Gain polarity: positive or negative

f. Offset: -4 volts to +4 volts

g. Accuracy: ±3%

h. Bandwidth: 20 MHz

i. Characteristics c, d, e and f are used to level translate each input signal into the DAS internal normalized range of -1 volt to +1 volt.

2. Sync Processor:

a. Processes and captures the sync, blanking and active video pattern for any user specified line within a frame. Detected vertical sync, field state and re-constructed horizontal sync are directly accessible at the Gold-Dot interface as digital signals.

b. Digitizing rate: 10 MHz

c. Input Line Rate: 7.5 KHz to 45 KHz

d. The sync tip and pedestal (blanking) amplitudes of a composite video input are sampled and measured with an accuracy of ±3%.

e. Separate (non-composite) horizontal and vertical syncs may be applied to the sync processor via the digital I/O.

3. Composite video image acquisition (CVIA)

   a. Full frame acquisition: Interlaced and non-interlaced

   b. Available four line window memory: 2K x 16

   c. Video depth: 4 bits

   d. Pixels/line: 2048 max.

   e. Digitizing rate: 40 MHz (max.)

   f. Digitizing accuracy: ± 1/4 LSB

4. Raster/stroke image acquisition (RSIA)

   a. Captures following formats:

      (1) Rectilinear raster

      (2) Polar raster

      (3) Stroke (X-Y-Z)

b. Normalized image written into 256 x 256 x 4 array

c. 'X' and 'Y' address depth: 8 bits

d. 'Z' modulation depth: 4 bits

e. Digitizing rate: 20 MHz (max.)

f. Digitizing accuracy:

(1) 'X' and 'Y'" ±1 LSB

(2) 'Z': ± 1/8 LSB

g. The timing and duration of an RSIA capture may be controlled by an external digital gate signal.

F. Digital I/O characteristics - All digital communication between the DAS and the Gold Dot interface is in differential format.

4.4.7 <u>Synchro/Resolver Indicator</u>

(1) Signal Input:

A. Synchro operation:

1. 11.8V (L-L) at 47 to 440 Hz

2. 90V (L-L) at 47 to 440 Hz

B. Resolver operation:

1. 11.8V (L-L) at 100 to 1000 Hz

2. 26V (L-L) at 100 to 440 Hz

(2) Reference Input:

A. Voltage: 10 to 130V RMS

B. Frequency: 47 Hz to 1000 Hz

C. Impedance: 100 Kohm min.

(3) Angle Range: 359.99 °

(4) Resolution: 0.01 °

(5) Accuracy: ±0.1 °

(6) Dynamic Rate:

A. 450°/sec maximum (tracking) at 400 Hz

B. 110°/sec maximum (tracking) at 60 Hz

4.4.8 Synchro/Resolver Simulator

(1) Angle Range: 0 ° to 359.98 °

(2) Resolution: 0.02 °

(3) Accuracy: ±0.36 ° Full Load

±0.12 ° No Load

(4) Reference Input:

A. Voltage: 26V or 115V (either reference voltage input may be used for any specified signal output below).

B. Frequency: 47-1000 Hz

C. Impedance: 13 Kohms, minimum

(5) Signal Output:

A. Voltage:

1. Resolver mode V (L-L): 11.8V, 26V

2. Synchro mode V (L-L): 11.8V, 90V

B. Frequency:

1. 360-1000 Hz for 11.8V Synchro or Resolver mode, 26V Resolver mode, and 90V Synchro mode.

2. For Synchro operation from 47 Hz to less than 360 Hz, an external 90V Synchro transformer is required. Reference input must be 115 VRMS for 6.8V resolver output to external transformer.

C. Output Impedance:

1. 100 ohms minimum at 11.8V L-L

2. 500 ohms minimum at 26V L-L

3. 4000 ohms minimum at 90V L-L

D. Response Time: 25 millisecond max.

E. Dynamic Rate: 140°/second max.

4.5 RF SUBSYSTEM (CEE -101, -103, -107, -109)

4.5.1 RF Interface Unit (RFIU)

The RFIU provides the RF interface between the entire system and the UUT, encompassing signal switching, amplification, attenuation, and amplitude demodulation. There are eight RF outputs (for CEE -101, -103), nine RF outputs (for CEE -107, -109) and four RF inputs. The RF outputs provide two simultaneous RF signals. All RF connectors are type N precision stainless steel. In addition, there are two rear panel mounted BNC connectors, which connect to one RF output and one RF input. These signals are used as instrument inputs in the Signal Distribution System. The RFIU facilitates the following RF measurements:

(1) Power: Using the power meter and spectrum analyzer.

(2) Frequency: Using the spectrum analyzer.

(3) Pulse/AM Detection: Using the RFIU detectors or the spectrum analyzer detected video output.

The performance of the above instrumentation are normalized to the RFIU interface. The detailed RFIU specifications are as follows:

(4) Four outputs from RFG 1. (CEE -103); Five outputs from RFG1 (CEE -107)

(5) Four outputs from RFG 2.

(6) Four outputs from RFG3 (CEE -101); Five outputs from RFG3 (CEE -107)

(7) Four inputs to the following instrumentation:

A. Power Meter

B. Spectrum Analyzer

C. RF Detectors

(8) Input RF attenuation is provided for all four inputs as follows:

A. Range: 0 to 100 dB

B. Resolution: 10 dB

C. Frequency: DC to 22 GHz

D. Input Power: 1 watt (0 to 20 dB)

10 watts (30 to 100 dB)

(9) Input RF Pulse/AM Detection is provided. Video amplification is available for low level detected signals. Sensitivity at the interface is as follows:

A. 10 MHz to 0.5 GHz: -10 dBm

B. Greater than 0.5 GHz to 22 GHz: -25 dBm

(10) Output RF amplification is provided for both RFG1, RFG2 and RFG3 as follows:

A. RFG1:

1. 0.3 to 1.3 GHz

2. 100 KHz to 300 MHz

B. RFG2:

1. 0.3 to 1.3 GHz

2. 100 KHz to 300 MHz

C. RFG3:

1. 0.3 to 2 GHz

2. 2 to 8 GHz

3. 100 KHz to 300 MHz

4.5.2 RF Generator 1 (RFG1) (CEE -103, -109)

RFG1 is available at any one of four outputs (for CEE -103), five outputs (for CEE -109) in the RFIU. The output signal may also be wrapped around to any of the response instrumentation, through the RFIU, for self-test. An external modulating pulse, AM, FM, or phase modulation signal may be routed to RFG1 from other system resources. RFG1 provides the following capabilities at the interface:

1. Frequency:

   A. Range: 10 KHz to 1.3 GHz

   B. Resolution: 1 Hz

   C. Harmonics:

      10 KHz to 650 MHz:

      Less than or equal to -30 dBc (w/o amplifiers)

Greater than 650 MHz;

Less than or equal to -25 dBc (w/o amplifiers)

D. Spurious: Less than or equal to -50 dBc (w/o amplifiers)

non-harmonic)

E. Accuracy: ± 15 Hz (based on Rubidium Frequency)

Reference time base accuracy of $\pm 2 \times 10^{-9}$.

2. Power:

A. Range:

+8 to -120 dBm (10 KHz to 100 KHz, w/o amp.)

+16 to -120 dBm (100 KHz to 132.1875 MHz, w/o amp.)

+17 to -120 dBm (132.1875 MHz to 528.75 MHz, w/o amp.)

+14 to -120 dBm (528.75 MHz to 1.0575 GHz, w/o amp.)

+13 to -120 dBm (1.0575 GHz to 1.3 GHz, w/o amp.)

+38 to -50 dBm (150 MHz, w/amp.)

+32 to -50 dBm (100 KHz to 150 KHz, w/amp.)

+35 to -50 dBm (150 KHz to 300 MHz, w/amp.)

+20 to -50 dBm (300 MHz to 1.3 GHz, w/amp.)

NOTE (CEE -109 only) Power Range specifications (w/amp.) do not apply to output at RFIU J27.

B. Resolution: 0.1 dB

C. Accuracy: ±1.5 dB (using supplied RF utilities), except:

±2.2 dB from +8 to -65 dBm (10 KHz to 100 KHz, w/o amp.)

±3.2 dB from -65 to -120 dBm (10 KHz to 100 KHz, w/o amp.)

±2.2 dB from +16 to -65 dBm (100 KHz to 8 MHz, w/o amp.)

±3.2 dB from -65 to -120 dBm (100 KHz to 8 MHz, w/o amp.)

±2.2 dB from -65 to -90 dBm (8 MHz to 1.3 GHz, w/o amp.)

±2.0 dB from -90 to -120 dBm (8 MHz to 1.3 GHz, w/o amp.)

For CEE -109 only, the following additional accuracy specification applies to output at RFIU J27 only:

+9.0 dB / -10.0 dB (10 KHz to 20 KHz)

+4.0 dB / -5.0 dB (greater than 20 KHz to 100 KHz)

+1.0 dB / -2.0 dB (greater than 100 KHz to 1 GHz)

+1.0 dB / -3.0 dB (greater than 1 GHz to 1.3 GHz)

3. Pulse Modulation:

   A. ON/OFF ratio: Greater than or equal to 40 dB (10 KHz to

      1.0575 GHz)

      Greater than or equal to 55 dB

      (greater than 1.0575 GHz)

   B. Rise/fall times: Less than or equal to 400 nanosec

   C. Min. pulse width: 2 microsec

   D. Max repetition rate: 100 KHz

4. Amplitude Modulation:

   A. Rate: 20 Hz to 100 KHz (external AC coupling or internal)

      DC to 100 KHz (external DC coupling)

   B. Modulation depth:

      0 to 99.9% (output level less than +8 dBm w/o amp.)

5. Frequency Modulation:

Programmed Frequency	Max. Rate * (fMOD)		Maximum Deviation
	INT	EXT	INT or EXT AC Coupled (smaller of the following)
10 KHz to 1 MHz	0.1 x Prog. Freq.	0.1 x Prog. Freq.	0.5 x Prog. Freq. or fMOD x 1080
1 MHz to 2 MHz	100 KHz		
2 MHz to 3 MHz	100 KHz	200 KHz	
3 MHz to 132.1875 MHz	100 KHz	200 KHz	1.5 MHz or fMOD x 1080
>132.1875 MHz to 264.375 MHz	100 KHz	200 KHz	375 KHz or fMOD x 270
>264.375 MHz to 528.75 MHz	100 KHz	200 KHz	750 KHz or fMOD x 540
>528.75 MHz to 1057.5 MHz	100 KHz	200 KHz	1.5 MHz or fMOD x 1080
>1057.5 MHz	100 KHz	200 KHz	3.0 MHz or fMOD x 2160

* NOTE: Min. rate is 20 Hz.

6. Phase Modulation:

A. Rate: 20 Hz to 15 KHz (external AC coupled or internal)

B. Deviation: 0 to 300 degrees

4.5.3 RF Generator 2 (RFG2)

RFG2 is available at any one of four (4) outputs in the RFIU. The output signal may also be wrapped around to any of the response instrumentation, through the RFIU, for self-test. An external modulating pulse, AM, FM, or phase modulation signal may be routed to RFG2 from other system resources. RFG2 provides the following capabilities at the interface:

(1) Frequency:

A. Range: 10 KHz to 1.3 GHz

B. Resolution: 1 Hz

C. Harmonics:

10 kHz to 650 MHz:

Less than or equal to -30 dBc (w/o amplifiers)

Greater than 650 MHz:

Less than or equal to -25 dBc (w/o amplifiers)

D. Spurious: Less than or equal to -50 dBc (w/o amplifiers) (non-harmonic)

E. Accuracy: ±15 Hz (based on Rubidium Frequency Reference time base accuracy of ±2 x 10^{-9}).

(2) Power:

A. Range:

+8 to -120 dBm (10 KHz to 100 KHz, w/o amp.)

+16 to -120 dBm (100 KHz to 132.1875 MHz, w/o amp.)

+17 to -120 dBm (132.1875 MHz to 528.75 MHz, w/o amp.)

+14 to -120 dBm (528.75 MHz to 1.0575 GHz, w/o amp.)

+13 to -120 dBm (1.0575GHz to 1.3 GHz, w/o amp.)

+38 to -50 dBm (150 MHz, w/amp.)

+32 to -50 dBm (100 KHz to 150 KHz, w/amp.)

+35 to -50 dBm (150 KHz to 300 MHz, w/amp.)

+20 to -50 dBm (300 MHz to 1.3 GHz, w/amp.)

B. Resolution: 0.1 dB

C. Accuracy: ±1.5 dB (using supplied RF utilities), except:

±2.2 dB from +8 to - 65 dBm (10 KHz to 100 KHz, w/o amp.)

±3.2 dB from -65 to- 120 dBm (10 KHz to 100 KHz, w/o amp.)

±2.2 dB from +16 to -65 dBm (100 KHz to 8 MHz, w/o amp.)

±3.2 dB from -65 to -20 dBm (100 KHz to 8 MHz, w/o amp.)

±2.2 dB from -65 to -90 dBm (8 MHz to 1.3 GHz, w/o amp.)

±2.0 dB from -90 to -120 dBm (8 MHz to 1.3 GHz, w/o amp.)

(3) Pulse Modulation:

A. ON/OFF Ratio: Greater than or equal to 40 dB (10 KHz to 1.0575 GHz)

Greater than or equal to 55 dB (greater than 1.0575 GHz)

B. Rise/Fall Times: Less than or equal to 400 nanoseconds

C. Minimum pulse width: 2 microseconds

D. Maximum repetition rate: 100 KHz

(4) Amplitude Modulation:

A. Rate: 20 Hz to 100 KHz (External AC Coupling or internal)

DC to 100 KHz (External DC Coupling)

B. Modulation Depth: 0 to 99.9% (output level less than +8 dBm w/o amp.)

(5) Frequency Modulation:

<table>
<tr><th rowspan="2">Programmed Frequency</th><th colspan="2">Max. Rate * (fMOD)</th><th>Maximum Deviation</th></tr>
<tr><th>INT</th><th>EXT</th><th>INT or EXT AC Coupled (smaller of the following)</th></tr>
<tr><td>10 KHz to 1 MHz</td><td>0.1 x Prog. Freq.</td><td rowspan="2">0.1 x Prog. Freq.</td><td rowspan="3">0.5 x Prog. Freq. or fMOD x 1080</td></tr>
<tr><td>1 MHz to 2 MHz</td><td>100 KHz</td></tr>
<tr><td>2 MHz to 3 MHz</td><td>100 KHz</td><td>200 KHz</td></tr>
<tr><td>3 MHz to 132.1875 MHz</td><td>100 KHz</td><td>200 KHz</td><td>1.5 MHz or fMOD x 1080</td></tr>
<tr><td>>132.1875 MHz to 264.375 MHz</td><td>100 KHz</td><td>200 KHz</td><td>375 KHz or fMOD x 270</td></tr>
<tr><td>>264.375 MHz to 528.75 MHz</td><td>100 KHz</td><td>200 KHz</td><td>750 KHz or fMOD x 540</td></tr>
<tr><td>>528.75 MHz to 1057.5 MHz</td><td>100 KHz</td><td>200 KHz</td><td>1.5 MHz or fMOD x 1080</td></tr>
<tr><td>>1057.5 MHz</td><td>100 KHz</td><td>200 KHz</td><td>3.0 MHz or fMOD x 2160</td></tr>
</table>

* NOTE: Min. rate is 20 Hz.

(6) Phase Modulation:

A. Rate: 20 Hz to 15 KHz (external AC Coupled or internal)

B. Deviation: 0 to 300 degrees.

4.5.4 RF Generator 3 (RFG3) (CEE -101, -107) - RFG3 is available at any one of four outputs (for CEE -101), five outputs (for CEE -107) in the RFIU. The output signal may also be wrapped around to any of the response instrumentation, through the RFIU, for self-test. An external modulating pulse or AM signal may be routed to RFG3 from other system resources. RFG3 provides the following capabilities:

(1) Frequency:

A. Range: 50 MHz to 22 GHz

B. Resolution: 1 KHz

C. Harmonics: -55 dBc (w/o amplifiers)

D. Spurious: -55 dBc (w/o amplifiers)

E. Accuracy: ±55 Hz (based on rubidium frequency reference time base accuracy of $\pm 2 \times 10^{-9}$.

(2) Power:

A. Range:

-3 to -100 dBm (50 MHz to 10 GHz, w/o amp.)

-7 to -100 dBm (10 GHz to 22 GHz, w/o amp.)

+35 to -50 dBm (50 MHz to 300 MHz, w/amp.)

+20 to -50 dBm (300 MHz to 2 GHz, w/amp.)

+25 to -50 dBm (2 GHz to 8 GHz, w/amp.)

NOTE (CEE -107 only): Power Range specifications (w/amp.) do not apply to output at RFIU J27.

B. Resolution: 0.1 dB

C. Accuracy: ±1.5 dB (using supplied RF utilities), except:

±2.2 dB from -65 to -90 dBm (50 MHz to 6.2 GHz, w/o amp.)

±2.5 dB from -90 to -100 dBm (50 MHz to 6.2 GHz, w/o amp.)

±2.2 dB from -65 to -80 dBm (6.2 GHz to 10 GHz, w/o amp.)

±2.5 dB from -80 to -100 dBm (6.2 GHz to 10 GHz, w/o amp.)

±3.5 dB from -80 to -100 dBm (10 GHz to 12.7 GHz, w/o amp.)

±2.2 dB from -65 to -75 dBm (12.7 GHz to 19.9 GHz, w/o amp.)

±3.5 dB from -75 to -100 dBm (12.7 GHz to 19.9 GHz, w/o amp.)

±2.2 dB from -65 to -70 dBm (19.9 GHz to 22 GHz, w/o amp.)

±3.5 dB from -70 to -100 dBm (19.9 GHz to 22 GHz, w/o amp.)

For CEE -107 only, the following additional

accuracy specification applies to output at RFIU J27 only:

+1.0 dB / -2.0 dB (50 MHz to 1 GHz)

+1.0 dB / -3.0 dB (greater than 1 GHz to 4 GHz)

+1.0 dB / -4.0 dB (greater than 4 GHz to 12 GHz)

+1.0 dB / -5.0 dB (greater than 12 GHz to 18 GHz)

+2.0 dB / -7.0 dB (greater than 18 GHz to 22 GHz)

(3) Pulse Modulation:

A. ON/OFF Ratio: Greater than or equal to 60 dB to 18 GHz

Greater than or equal to 30 dB to 22 GHz

B. Rise/Fall Times: Less than or equal to 25 nanosec

(4) Amplitude Modulation:

A. SCAN Mode (DC Coupled):

1. Dynamic Range:

RF Freq. Modulating Rate	50 MHz to less than 200 MHz	200 MHz to 18 GHz	Greater than 18 GHz to 22 GHz
DC to 5 KHz	30 dB	40 dB	35 dB
5 KHz to 20 KHz	21 dB	28 dB	25 dB

B. AM Mode (AC Coupled):

1. Modulation Depth: 0 to 90%

2. Frequency Range: 10 Hz to 20 KHz

4.5.5 Spectrum Analyzer

The spectrum analyzer provides frequency domain analysis. UUT signals are routed to the spectrum analyzer from any one of the four inputs in the RFIU. System RF resource signals may be wrapped around within the RFIU for measurement and self-test. The spectrum analyzer provides the following capabilities at the interface:

(1) <u>Frequency Range</u> - 100 Hz to 22 GHz in two bands.

A. Band 1: 100 Hz to 2.7 GHz

B. Band 2: 2.7 GHz to 22 GHz

(2) <u>Frequency Span</u> -

A. Band 1: 0 Hz or 100 Hz to 2.6999999 GHz.

B. Band 2: 0 Hz or 100 Hz to 19.3 GHz.

(3) Resolution BW: 10 Hz to 3 MHz (1, 3, 10 seq.)

(4) Video BW: 3 Hz to 3 MHz (1, 3, 10 seq.)

(5) Input Power Sensitivity:

A. -70 dBm: 100 Hz to 100 KHz.

B. -80 dBm: greater than 100 KHz to 300 KHz.

C. -90 dBm: greater than 300 KHz to 1.0 MHz.

D. -100 dBm: greater than 1.0 MHz to 6.2 GHz.

E. -90 dBm: greater than 6.2 GHz to 12.7 GHz.

F. -85 dBm: greater than 12.7 GHz to 19.9 GHz.

G. -80 dBm: greater than 19.9 GHz to 22.0 GHz.

(6) Input Power Accuracy using supplied RF utilities:

A. 1.05 dB for inputs up to 8 MHz

B. 1.5 dB for inputs greater than 8 MHz

(7) Input Power Relative Accuracy:

A. ±0.5 dB (0 to 50 dB)

B. ±1.0 dB (50 to 80 dB)

(8) Input Power Resolution: 0.1 dB

(9) Frequency accuracy - ±55 Hz (based on a rubidium frequency reference time base accuracy of $\pm 2 \times 10^{-9}$, and using 100 Hz span).

4.5.6 RF Power Meter

The Power Meter provides the following capabilities at the interface:

(1) Channel A (Internal RFIU power sensor)

a. Frequency: 8 MHz to 22 GHz

b. Power Range: -55 dBm to +40 dBm (using RFIU input attenuator)

c. Accuracy: ±1.5 dB (using supplied RF utilities)

d. Relative Accuracy: ±0.2 dB (0 to 40 dB)

(2) Channel B (External power sensor) -

a. Frequency - 8 MHz to 22 GHz

b. Power range - -20 to -70 dBm

c. Accuracy -

	FREQUENCY RANGE			
POWER LEVEL	8 MHz-10 MHz	10 MHz-10GHz	10 GHz-18GHz	18 GHz-22 GHz
-20 to -60 dBm	±0.19 dB	±0.16 dB	±0.21 dB	±0.26 dB
-60 to -70 dBm	±0.40 dB	±0.39 dB	±0.42 dB	±0.44 dB

NOTE: Above accuracy excludes effect of source VSWR.

4.5.7 Rubidium Frequency Reference (all CEEs)

The Rubidium Frequency Reference is an Efratom FRT-GR-LA and provides eight frequency outputs, as specified below. Four of these outputs are utilized as an external frequency reference input to RFG1, RFG2, RFG3 and the spectrum analyzer.

(1) Frequency: 10 MHz ±0.02 Hz (assumes 1 year calibration interval)

(2) Stability:

A. less than 1×10^{-11} parts/day

B. less than 4×10^{-11} parts/month

(3) Output Voltage:

A. Outputs 1 and 2: 0.5 to 0.7V RMS into 50 ohms

B. Outputs 3 and 4: 1V RMS into 1 Kohm

C. Outputs 5 through 8: 1V RMS into 50 ohms

4.5.8 RF Millivoltmeter (CEE -103, -109 only)

The RF millivoltmeter has the following characteristics:

(1) Input Frequency Range: 10 KHz to 1.2 GHz with supplied probe

(2) Voltage Measurement Range: 200 uv to 3V

A. 8 display ranges in 1-3-10 sequence

B. Four digit display in mv

C. Usable indications extended down to 50 uv

(3) Voltage Measurement Accuracy: The maximum uncertainty is the sum of the basic uncertainty, frequency effect and temperature effect:

A. Basic uncertainty:

Voltage Input Level	Error
3 mv - 3000 mv	1% reading ± 1 count
1 mv - 3 mv	2% reading ± 2 counts
0.2 mv - 1 mv	3% reading ± 3 counts

B. Frequency effect (for properly terminated 50 ohm measurements):

Frequency	Error
1 MHz (calibration freq.)	0
10 KHz - 100 MHz	1% reading
100 MHz - 1 GHz	3% reading
1 GHz - 1.2 GHz	7% reading

C.

Temperature	Error
21°C to 25°C	0
18°C to 30°C	1% reading
10°C to 40°C	6% reading

(4) Maximum AC input: 10V

(5) Maximum DC input: 400V

4.5.9 List of RF Instruments

Instrument	QTY.	MFG	Part Number
Spectrum Analyzer Display	1	HP	70206A
Spectrum Analyzer	1	HP	70001A

C. Programming Resolution: 12 bits

D. Voltage Accuracy: 0.5% of programmed value ±2.44 mV

(9) Bandwidth:

A. Universal Pins: 40 MHz (3 dB)

B. Extended Performance Pins: 100 MHz (3 dB)

(10) Load Sets: There are six load sets, each consisting of one pull-up (to +5V) and one pull-down (to system ground) load. Each load is individually programmable to the following values and accuracy:

A. 50 + 15/-5 ohms

B. 75 + 17.5/-7.5 ohms

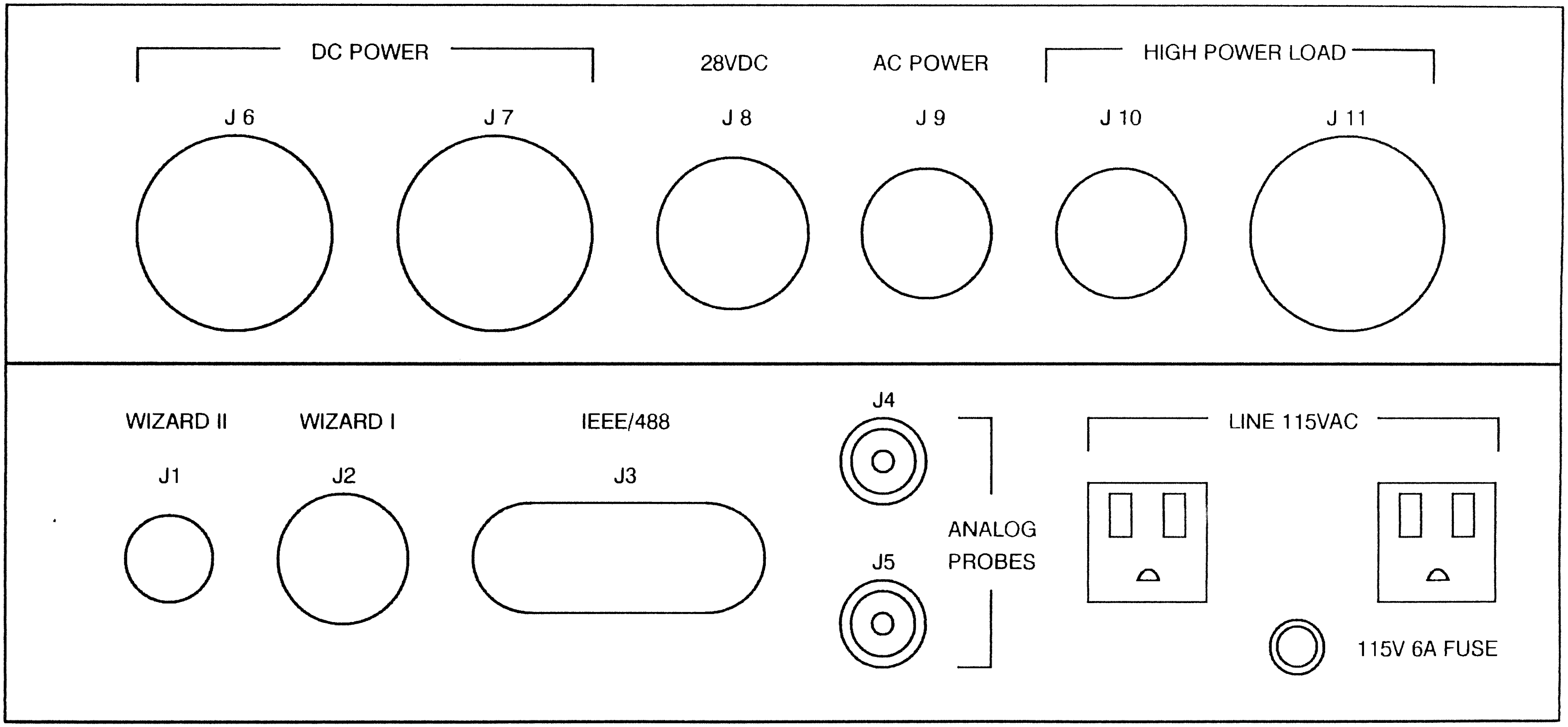
C. 100 + 20/-10 ohms

D. 500 + 60/-50 ohms

E. 1000 + 110/-100 ohms

5.3 AUXILIARY INTERFACE PANEL

The Auxiliary Interface Panel, shown in figure 5.2, provides eleven connectors for additional interfacing capability for UUT testing as follows:



IFTE CEE AUXILIARY INTERFACE PANEL

(CEE –101, –103, –105)

FIGURE 5.2A

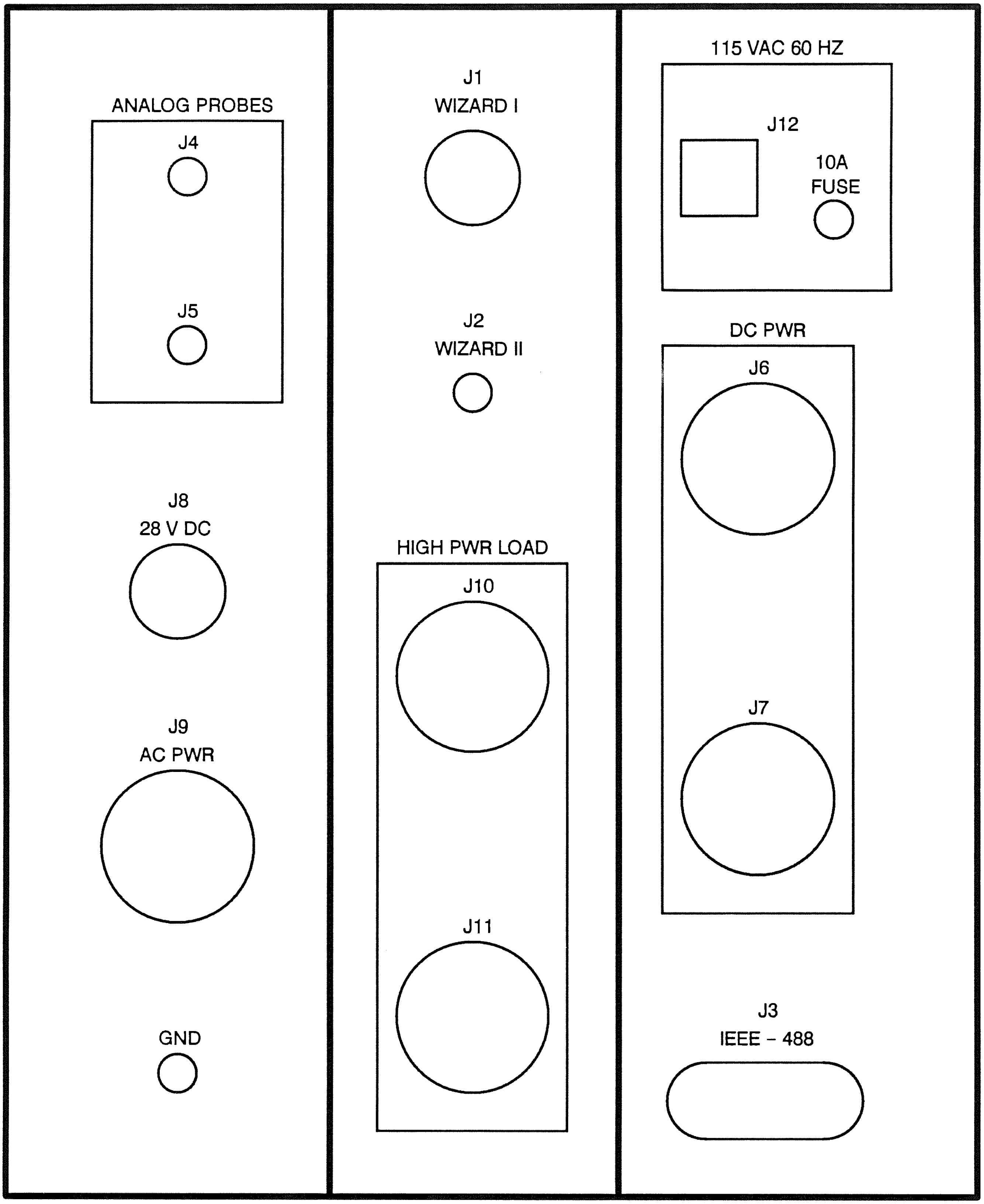


FIGURE 5.2B

CEE AUXILIARY INTERFACE PANEL

(CEE –107, –109, –111)

(1) J1 and J2 provide the interface for the two Wizard probes used for the digital UUT testing.

(2) J3 is an IEEE-488 standard bus connector which enables an operator to interface an external instrument to the station.

(3) J4 and J5 provide BNC connectors for connecting external analog probes to universal I/O pins. J4 signal lead and return is connected to U142 and U143 respectively. J5 signal lead and return is connected to U144 and U144 respectively.

(4) J6 and J7 (Figures 5.3 and 5.4) provide the high current (20.5 amps maximum) interface for the eight programmable DC Power supply outputs.

(5) J8 (Figure 5.5) provides the interface for the 28 VDC, 22.5 amps fixed power supply output.

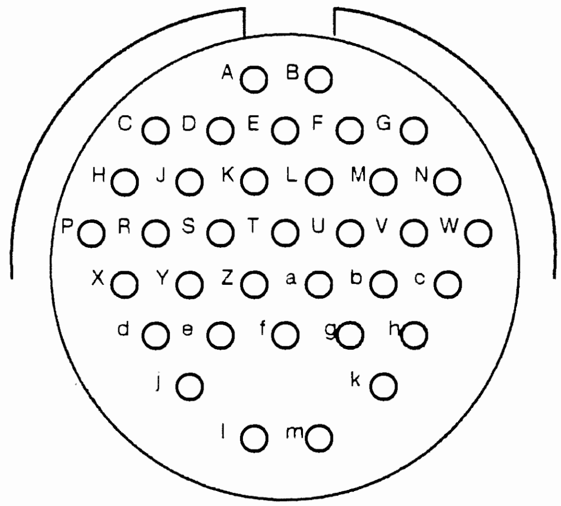
(6) J9 (Figure 5.6) provides the interface for the AC power supply output, and for the four 200 VDC programmable DC power supply outputs (CEE -103, -109).

(7) J10 and J11 (Figures 5.7 and 5.8) provide the interface for the eight programmable high power loads.

FIGURE 5.3A

AUXILIARY INTERFACE PANEL
DC POWER CONNECTOR #1 PIN ASSIGNMENTS
(CEE-101, -103, -105)

J 6

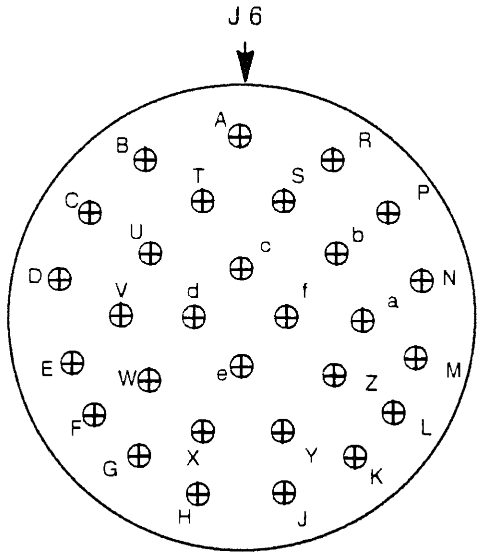


MS3100A28-15S

PIN	FUNCTION			PIN	FUNCTION		
A	P.S. # 1	+	SENSE	V	P.S. # 3	+	V
B	P.S. # 1	+	V	W	P.S. # 3	+	V
C	P.S. # 1	+	V	X	P.S. # 3	-	V
D	P.S. # 1	+	V	Y	P.S. # 3	-	V
E	P.S. # 1	-	V	Z	P.S. # 3	-	V
F	P.S. # 1	-	V	a	P.S. # 3	-	SENSE
G	P.S. # 1	-	V	b	P.S. # 4	+	SENSE
H	P.S. # 1	-	SENSE	c	P.S. # 4	+	V
J	P.S. # 2	+	SENSE	d	P.S. # 4	+	V
K	P.S. # 2	+	V	e	P.S. # 4	+	V
L	P.S. # 2	+	V	f	P.S. # 4	-	V
M	P.S. # 2	+	V	g	P.S. # 4	-	V
N	P.S. # 2	-	V	h	P.S. # 4	-	V
P	P.S. # 2	-	V	j	P.S. # 4	-	SENSE
R	P.S. # 2	-	V	k	SPARE		
S	P.S. # 2	-	SENSE	l	SPARE		
T	P.S. # 3	+	SENSE	m	SPARE		
U	P.S. # 3	+	V				

FIGURE 5.3B

AUXILIARY INTERFACE PANEL
DC POWER CONNECTOR #1 PIN ASSIGNMENTS
(CEE–107, –109, –111)

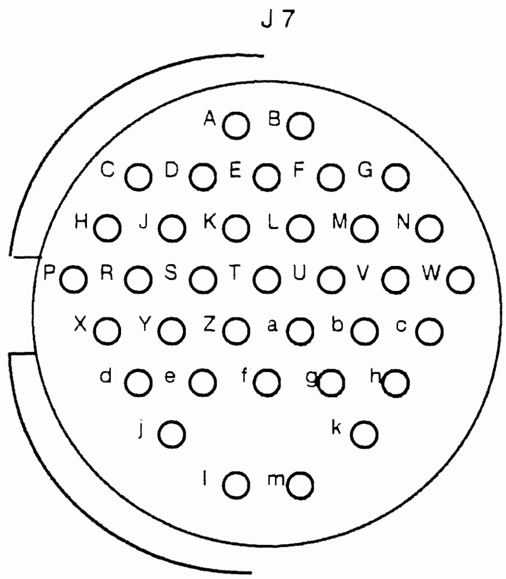


D38999/40 WJ29SN

PIN	FUNCTION			PIN	FUNCTION		
A	P.S. # 1	+	SENSE	V	P.S. # 3	+	V
B	P.S. # 1	+	V	W	P.S. # 3	–	V
C	P.S. # 1	+	V	X	P.S. # 3	–	V
D	P.S. # 1	+	V	Y	P.S. # 3	–	SENSE
E	P.S. # 1	–	V	Z	P.S. # 4	+	SENSE
F	P.S. # 1	–	V	a	P.S. # 4	+	V
G	P.S. # 1	–	V	b	P.S. # 4	+	V
H	P.S. # 1	–	SENSE	c	P.S. # 4	–	V
J	P.S. # 2	+	SENSE	d	P.S. # 4	–	V
K	P.S. # 2	+	V	e	P.S. # 4	–	SENSE
L	P.S. # 2	+	V	f	SPARE		
M	P.S. # 2	+	V				
N	P.S. # 2	–	V				
P	P.S. # 2	–	V				
R	P.S. # 2	–	V				
S	P.S. # 2	–	SENSE				
T	P.S. # 3	+	SENSE				
U	P.S. # 3	+	V				

FIGURE 5.4A

AUXILIARY INTERFACE PANEL
DC POWER CONNECTOR #2 PIN ASSIGNMENTS
(CEE-101, -103, -105)

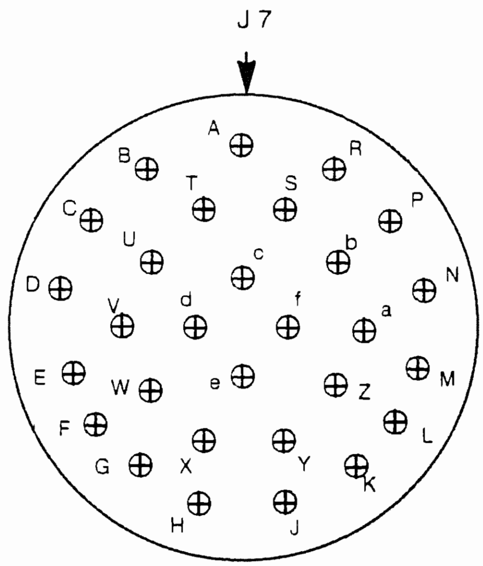


MS3100A28-15SW

PIN	FUNCTION			PIN	FUNCTION		
A	P.S. # 5	+	SENSE	V	P.S. # 7	+	V
B	P.S. # 5	+	V	W	P.S. # 7	+	V
C	P.S. # 5	+	V	X	P.S. # 7	-	V
D	P.S. # 5	+	V	Y	P.S. # 7	-	V
E	P.S. # 5	-	V	Z	P.S. # 7	-	V
F	P.S. # 5	-	V	a	P.S. # 7	-	SENSE
G	P.S. # 5	-	V	b	P.S. # 8	+	SENSE
H	P.S. # 5	-	SENSE	c	P.S. # 8	+	V
J	P.S. # 6	+	SENSE	d	P.S. # 8	+	V
K	P.S. # 6	+	V	e	P.S. # 8	+	V
L	P.S. # 6	+	V	f	P.S. # 8	-	V
M	P.S. # 6	+	V	g	P.S. # 8	-	V
N	P.S. # 6	-	V	h	P.S. # 8	-	V
P	P.S. # 6	-	V	j	P.S. # 8	-	SENSE
R	P.S. # 6	-	V	k	SPARE		
S	P.S. # 6	-	SENSE	l	SPARE		
T	P.S. # 7	+	SENSE	m	SPARE		
U	P.S. # 7	+	V				

FIGURE 5.4B

AUXILIARY INTERFACE PANEL
DC POWER CONNECTOR #2 PIN ASSIGNMENTS
(CEE-107, -109, -111)

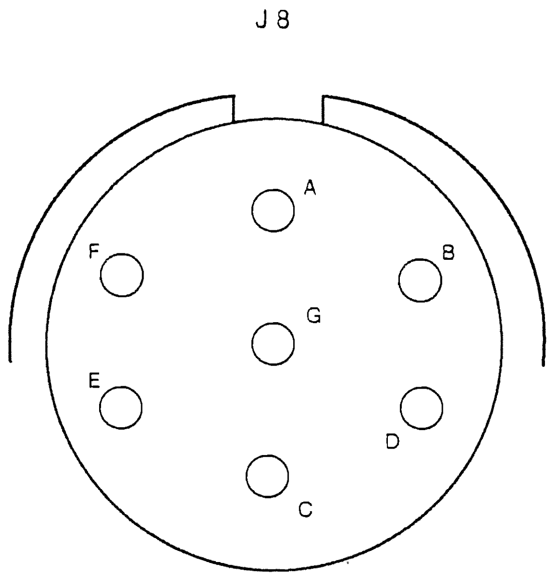


D38999/40 WJ29SA

PIN	FUNCTION			PIN	FUNCTION
A	P.S. # 5	+	SENSE	V	SPARE
B	P.S. # 5	+	V	W	SPARE
C	P.S. # 5	-	V	X	SPARE
D	P.S. # 5	-	SENSE	Y	SPARE
E	P.S. # 6	+	SENSE	Z	SPARE
F	P.S. # 6	+	V	a	SPARE
G	P.S. # 6	-	V	b	SPARE
H	P.S. # 6	-	SENSE	c	SPARE
J	P.S. # 7	+	SENSE	d	SPARE
K	P.S. # 7	+	V	e	SPARE
L	P.S. # 7	-	V	f	SPARE
M	P.S. # 7	-	SENSE		
N	P.S. # 8	+	SENSE		
P	P.S. # 8	+	V		
R	P.S. # 8	-	V		
S	P.S. # 8	-	SENSE		
T	SPARE				
U	SPARE				

FIGURE 5.5A

AUXILIARY INTERFACE PANEL
28V DC CONNECTOR PIN ASSIGNMENTS
(CEE-101, -103, -105)

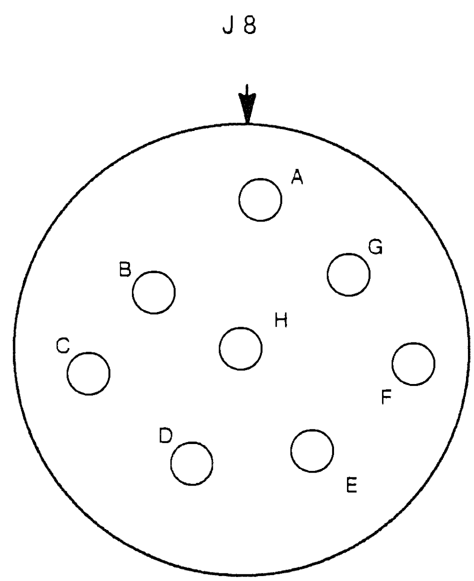


MS3100A24-27S

PIN	FUNCTION
A	+28V DC
B	+28V DC
C	-28V DC
D	-28V DC
E	SPARE
F	SPARE
G	SPARE

FIGURE 5.5B

AUXILIARY INTERFACE PANEL
28V DC CONNECTOR PIN ASSIGNMENTS
(CEE-107, -109, -111)



D38999/40WE8SN

PIN	FUNCTION
A	+ 28V DC
B	+ 28V DC
C	-28V DC
D	-28V DC
E	SPARE
F	SPARE
G	SPARE
H	SPARE

6.1.7 ATSE Data Base and Data Base Manager

The ATSE Data Base Management System (DBMS) is a software interface between the physical ATSE data storage area and the user, where the term "user" refers to either the end-user sitting at a terminal or an ATSE tool utilizing embedded DBMS software. It allows these functions to be performed on the data base:

* Insertion
* Deletion
* Modification
* Retrieval
* Update

6.1.8 ATSE/CEE User Environment Link

The CEE link provides an interactive means of transferring files from the ATSE software development station to the CEE ATE station. The CEE link is capable of copying files as well as entire directory subtrees between systems. Test Program data is transfered from the ATSE workstation to the CEE via the IEEE802.3 Ethernet Protocol.

6.1.9 Tool Interface

The ATSE Tool Interface specification is the basis for integrating new tools into the system. The Tool Interface describes:

a. accessibility to system services

b. interface to the ATSE DBMS

7.0 Testing and Troubleshooting

7.1 Maintenance

7.1.1 General

This section describes the recommended maintenance necessary to support the CEE Test Station. The detailed maintenance for all equipment is covered within their respective maintenance manuals.

Preventative maintenance is performed at scheduled intervals. Its purpose is to prevent equipment deterioration and extend the useful operating life of the test station.

Part replacement procedures are performed when required and their purpose is to restore normal operation to an assembly after a fault has been detected and isolated to a replaceable component.

7.1.2 Preventative Maintenance

SYSTEM AIR FILTERS

Throughly clean the system air intake filters located at the lower front of each rack on a monthly basis. Proceed as follows:

a. Remove blower grill.

b. Remove air filter element.

c. Wash both items thoroughly in warm soapy water and rinse well.

d. Re-install when dry.

7.1.3 Dust

If required, remove dust and other light debris from the test station using a vacuum cleaner. Loosen encrusted dust with a soft bristled brush and remove with vacuum cleaner.

7.1.4 Cables

With system disconnected from facility power sources, check system interconnection cables, connectors and hoods for cracks, burns, dirt or wear. Make necessary repairs where defects are found.

Care should be taken not to extend the Spectrum Analyzer, RF Signal Generators or RFIU without first removing both ends of the semi-rigid coaxial transmission line(s) that attach at the front of the instrument. Flexible coaxial cables are provided for operation of any instrument in its extended position.

7.1.5 Blowers

With the system in operation, check all blowers for proper operation. Ensure that the intake and exhaust areas are unobstructed and that no object interferes with the rotation of the blowers.

7.1.6 Frequency Of System Self-Test

It is recommended that the system Self-Test should be run on a weekly basis in the fault detection mode and daily in the confidence mode.

7.1.7 Frequency Of System Alignment

It is recommended that the system Self-Alignment test be performed on a monthly basis or on an individual basis whenever an assembly has been replaced or a repair action taken.

7.2 LOADING SYSTEM SOFTWARE AND SELF TEST AND ALIGNMENT PROGRAM EXECUTION

7.2.1 General

This section describes the procedures to load the System Software and to execute the Self Test and Self Alignment programs for the CEE station

7.2.2 Loading the System Software

Select System Software disc in accordance with IFTE Software Configuration Index, drawing A31U17380. Proceed as follows:

(a) Install the System Software Disc Cartridge into the Disc Drive Assembly and close the door.

(b) On the Disc Drive Assembly, place the START/STOP switch to the START position. The LOAD light extinguishes.

(c) Depress BREAK key on the terminal. After approximately 90 seconds, the READY light illuminates on the Disc Drive Assembly.

(d) Boot up the operating system by entering the monitor command: bsd (0,3,2)

NOTE: All entries are followed by depressing the RETURN key.

(e) When the prompt, cee (n) login:, is displayed on the terminal, log in by entering: root

NOTE: The (n) in cee (n), indicates a number, or space for a number.

(f) The terminal displays:

Password:

(g) Enter:

grumman

(h) When the prompt, "cee(n)#" a number, on the terminal, enter:

installcee

NOTE: The (n) in "cee(n)#", indicates a number, or space for a number.

The following message is displayed on terminal:

```
***************************************************
*                                                 *
*          CEE OPERATING SYSTEM SOFTWARE          *
*             INSTALLATION PROCEDURE              *
*                                                 *
***************************************************
```

Install Cee System Software   Abort Procedure

(i) Select "Install Cee System Software" by touching appropriate bar on touchscreen. The following message is displayed on terminal:

ENTER STATION SERIAL NUMBER

(j) Enter the station serial number on the terminal. The following message is displayed on terminal:

ENTER ETHERNET ADDRESS FOR THE DIGITAL VIC (DWG)

(k) Enter the enthernet address for the digital VIC in the following format:

x:x:xx:x:xx:xx

(where x:x:xx:x:xx:xx is the unique ethernet address for the digital VIC cpu board as labelled on the front of the board).

The following message is displayed on the terminal:

ENTER ETHERNET ADDRESS FOR THE ANALOG VIC (SDS)

(l) Enter the ethernet address for the analog VIC in the following format:

x:x:xx:x:xx:xx

(where x:x:xx:x:xx:xx is the unique ethernet address for the Analog VIC cpu board as labelled on the front of the board).

The following message is displayed on the terminal:

```
OK TO WRITE OVER FIXED PLATTERS (y OR n)?
```

(m) Type in: y

The following message is displayed on terminal:

```
**************************************************
*                                                *
*  INSTALLING CEE SYSTEM SOFTWARE TO FIXED DISK  *
*                                                *
**************************************************
```

When the installation (duration-approximately 12 minutes) is completed, the following messages are displayed on the terminal: (Do not perform these operations until directed to do so in succeeding steps.)

```
*************************************************************
*                                                           *
*    WAIT FOR PROM MONITOR PROMPT (   ), THEN REPLACE THE   *
*    OP SYSTEM DISK WITH A USER DISK AND REBOOT THE PIC.    *
*    ALSO RECYCLE THE POWER ON THE DIGITAL AND THE ANALOG   *
*    VICS TO REBOOT THE DWG AND SDS.                        *
*                                                           *
*************************************************************

syncing file systems...done

Halted
```

(n) On the Disc Drive Assembly, place the START/STOP switch to the STOP position. Wait (approximately 30 seconds) for LOAD indicator to illuminate.

(o) Remove the System Software Disc cartridge from the Disc Drive. For each VIC drawer, cycle power off, then on.

7.2.3 Self Test Operation

This paragraph contains instructions needed to run the self-test program for individual components of the CEE. Self-Test is run on the instrument the maintainer has just replaced. The self-test program is stored on the Self Test and Alignment Disk P/N TPDA31U12660S2-(*). NOTE: (*) refers to latest version as specified on IFTE Software Configuration Index, drawing A31U17380. To run individual self-test for the CEE install Self-Test and Alignment Disk and, perform these steps:

a. After system power-up and operator log in, the first menu displayed at the terminal is the CEE TPS DEVELOPMENT TOOL MENU. To select self-test, enter st (RETURN).

b. After Self-Test is selected, the IFTE SELF-TEST MAIN MENU is displayed.If the preset run mode or printer option conditions are set correctly, touch the INDIVIDUAL TEST SELECTION MENU bar, and proceed to the SELF-TEST INDIVIDUAL MODE SYSTEM MENU, at step d. If the maintainer needs to change the preset print or run modes, touch the CHANGE PRESET RUN/PRT OPTIONS bar.

c. If the CHANGE PRESET RUN/PRT OPTIONS menu selection is made at the IFTE SELF-TEST MAIN MENU, the PRESET OPTIONS SELECTION MENU is displayed.

To change the self-test run mode option, touch the RUN MODE = ________ bar the required number of times until the desired test mode appears. To change the printer option, touch the PRINT OPTION = ____________ bar the required number of times until the desired printer option appears. When the run mode and printer option are set, touch PREV and the new run mode and printer option become the preset conditions. To return to the CEE TPS DEVELOPMENT TOOL MENU without changing the preset conditions, touch EXIT.

d. Touching the INDIVIDUAL TEST SELECTION MENU bar at the IFTE SELF-TEST MAIN MENU will result in the station readiness test being executed. When it is successfully completed, the CRT will display the SELF-TEST INDIVIDUAL MODE SYSTEM MENU. This menu allows selection of an individual subsystem test.

If the USER INTERFACE/AUX. SUBSYSTEM bar is touched, the USER INTERFACE/AUXILIARY SUBSYSTEM MENU is displayed, from which the User Interface Self-Test or the Analog Probes and J4/J5 Tests can be selected.

If the SIGNAL DISTRIBUTION SYSTEM [SDS] bar is touched, the Signal Distribution System individual Self-Test status screen (step e) is displayed.

If the POWER [AC, DC, LOAD] SUBSYSTEM Bar is touched, the POWER SUBSYSTEM INDIVIDUAL TEST MENU (step f) is displayed.

If the ANALOG [AFGS, DMM ...] SUBSYSTEM bar is touched, the ANALOG SUBSYSTEM INDIVIDUAL TEST MENU (step g) is displayed.

If the DIGITAL [DWG, BTU ...] SYBSYSTEM bar is touched, the DIGITAL SUBSYSTEM INDIVIDUAL TEST MENU (step h) is displayed.

If (for CEE -101, -103, -107,-109) the RADIO FREQUENCY [RF] SUBSYSTEM bar is touched, the RF SUBSYSTEM INDIVIDUAL TEST MENU (for CEE -101, -107), or the RF SUBSYSTEM INDIVIDUAL TEST MENU #1 (for CEE -103, -109) (step i) is displayed.

e. Touching the SIGNAL DISTRIBUTION SYSTEM [SDS] bar at the SELF-TEST INDIVIDUAL MODE SYSTEM MENU displays the Signal Distribution System Self-Test status screen momentarily, followed by the SIGNAL DISTRIBUTION SYSTEM SELF-TEST SELECTION MENU.

This menu is utilized to run the individual portions of the Signal Distribution System Self-Tests.

f. Touching the POWER [AC, DC, LOAD] SUBSYSTEM bar at the SELF-TEST INDIVIDUAL MODE SYSTEM MENU displays the POWER SUBSYSTEM INDIVIDUAL TEST MENU, which is utilized to select self-test for the DC Power Supplies, the AC Power Supply or the High Power Load.

g. Touching the ANALOG [AFGS, DMM ...] SUBSYSTEM bar at the SELF-TEST INDIVIDUAL MODE SYSTEM MENU displays the following menu, which is utilized to select self-test for the AFGs, the Counter-Timer, the Digitizer, the Synchro/Resolver Simulator-Indicator, the DMM and the DAS.

h. Touching the DIGITAL [DWG, BTU ...] SUBSYSTEM bar at the SELF-TEST INDIVIDUAL MODE SYSTEM MENU displays the following menu, which is utilized to select the self-test for the Digital Word Generator, the Bus Test Unit or the Wizard Probing System.

i. If the RADIO FREQUENCY [RF] SUBSYSTEM bar is touched at the SELF-TEST INDIVIDUAL MODE SYSTEM MENU, the RF SUBSYSTEM INDIVIDUAL TEST MENU is displayed, for CEE -101 and -107. This menu is utilized to select the self-test for the RF Generator #3, RF Generator #2, Spectrum Analyzer, the RFIU, the Power Meter and the Rubidium Standard.

For CEE -103 and -109, the RF SUBSYSTEM INDIVIDUAL TEST MENU #1 is displayed, and is utilized to select self-test for the RF Generator #1, RF Generator #2, Spectrum Analyzer, RFIU, Power Meter and Rubidium Standard.

If the NEXT bar is touched, the RF SUBSYSTEM INDIVIDUAL TEST MENU #2, is displayed. This menu is utilized to select self-test for the RF Millivoltmeter.

7.2.4 Self Alignment Operation

This paragraph contains instructions needed to run the self-alignment program for individual components of the CEE. Self-Alignment is run on the instrument requiring alignment that the maintainer has just replaced. The Self-Alignment program is stored on the Self Test and Alignment Disk, P/N TPDA31U12660S2-(*). NOTE: (*) refers to latest version as specified on IFTE Software Configuration Index, drawing A31U17380.

Self-Alignment provides the operator with these capabilities:

- o Automatically verify the calibration of all the components of the CEE that require alignment.
- o Correct out-of-tolerance conditions.
- o Verify CEE performance to specification.
- o Provide system and component stability logs.

The CEE uses transfer and resistance standards to align the measurement instruments. Then those instruments are used to align other components in the system.

To run individual Self-Alignment for the CEE install the Self-Test and Alignment Disk and, perform these steps:

a. After system power-up and operator log in, the first menu displayed at the terminal is the CEE TPS DEVELOPMENT TOOL MENU. To select Self-Alignment, enter align (RETURN).

b. After Self-Alignment is selected, the IFTE SELF-ALIGNMENT MAIN MENU is displayed. The following is general information about each of the menu bars on the IFTE SELF-ALIGNMENT MAIN MENU.

TEST STATUS STATION FRONT VIEW - Touching this bar displays a graphics representation of the station front view, which provides, using color codes, the alignment status of instruments aligned during self-alignment execution.

RUN WITH PRESET PRINT OPTION - Touching this bar runs alignment. End to End (all tests one after another), with the preset print option. Preset options are values that are stored and remain the same, unless changed by the operator.

INDIVIDUAL TEST SELECTION MENU - Touching this bar executes the Readiness Test and at its conclusion brings the operator to another touch screen menu, which will allow the choice of running any alignment program individually. The individual program execution will run using the preset print mode option.

RUN ALIGNMENT ICD SELF-TEST - Touching this bar will run the alignment ICD Self-Test, testing all internal standards and then will return the operator to the Self-Alignment Main Menu.

CHANGE PRESET PRINT OPTION - Touching this bar brings the operator to another touch screen menu, which will allow the operator to change and save the preset print option.

c. If the preset run mode and printer option are set correctly, touch the INDIVIDUAL TEST SELECTION MENU bar to initiate the individual alignment mode. The SELF-ALIGNMENT INDIVIDUAL MODE MENU is displayed. The following is general information about each of the menu bars on this menu.

SDS [DAC 1-8] SLF-ALIGN - Touching this bar runs the Self-Alignment for the Signal Distribution System (D/A Converters or DACs 1 thru 8 housed in the Analog VIC Chassis).

POWER [AC, DC, LOAD] SUBSYSTEM - Touching this bar brings the operator to another menu which allows the selection if either running the DC Power, AC Power or High Power Load Alignments, individually.

ANALOG [AFGs, DMM ...] SUBSYSTEM - Touching this bar brings the operator to another menu which allows the selection of either running the AFG (1 thru 4), Counter-Timer, Digitizer (DIGTZ), Syn/Res Ind/Sim, DMM or Display Analyzer/Simulator (DAS) Alignments, individually.

DIGITAL (BTU) SUBSYSTEM - Touching this bar brings the operator to another menu which allows the selection of running the Bus Test Unit (BTU) Self-Alignment, individually.

RADIO FREQUENCY [RF] SUBSYSTEM - Touching this bar brings the operator to another menu which allows the selection of running the RFG #1 (CEE -103, -105), RFG #2, RFG #3 (CEE -101, -107), RFIU, Spectrum

Analyzer Alignment, RF Millivoltmeter (CEE -103, -109) or Power Meter Sensor Calibration Factor installation individually.

NOTE: Any alignment, that is run in the Individual Test Mode will run with preset print option. If the operator wishes to change the preset values,he must return to the main menu.

7.3 Self-Test ICD and Self-Alignment ICD Description

7.3.1 General

This section contains descriptions of the Self-Test ICD and Self-Alignment ICD.

7.3.2 Self-Test ICD

The self-test interface connection device (ICD) is in accordance with drawing A31U12660, and is connected to the station gold dot interface, when required, during the performance of station self-test.

The structure of the ICD consists of two aluminum side lates P/N's A31U17889-1, A31U17890-1, hinged to the gold dot interface housings.

Internal to the ICD, wiring connects the gold dot interface to a wire wrap motherboard, P/N A31U29801-1, which distributes all required signals and power to the top mounted connector panel, where all components (consisting of sixteen resistors) are mounted. The wire wrap motherboard is hinged to the top panel.

Wiring from the gold dot modules to the wire wrap motherboard is located in the tongue of the ICD. The gold dot interface contains 3200 connections, each of which consists of a gold dot plated with approximately 100 micro inches of 24 karat gold. The plating acts as an oxidation barrier and allows the gold dot to meet military environmental requirements for contacts.

Wiring wrapping is used extensively within the ICD, and provides low cost manufacturing and simplified maintenance, while providing design flexibility and reliability.

The top mounted panel contains connectors J1 through J15, and test points TP1 through TP48. Cables A31U12679-2, A31U12680-2, A31U12681-2, and A31U12682-2 comprise the cable set A31U12687-2, and are connected between J1, J3, J5, J7 on the top mounted panel, and J8, J9, J10, and J11, respectively, on the auxiliary interface panel (CEE -107, -109, -111), during self-test. For the CEE -101, -103, -105, cables and connections are the same except that the cable and cable set dash numbers are -1 instead of -2. In addition, J6 and TP41 are utilized during probe self-test. All other connections are available for integration purposes. The test points are utilized to monitor the programmable DC power supply outputs, the switch card relays, the DWG functions, the programmable loads, and the synchro Indicator/Simulator voltages.

Accessibility to internal wiring is obtained via the hinged clam shell construction of the interface connector panel, which is able to be retained open at a 45 degree angle via pit pins, and two removable panel covers.

7.3.3 Self-Alignment ICD

The self-alignment interface connection device (ICD) is in accordance with drawing A31U12661, and contains the transfer standards used for self-alignment.

The structure of the ICD consists of two aluminum side plate P/N's A31U17889-1 and A31U17890-1, hinged to the gold dot interface housings.

Internal to the ICD, wiring connects the gold dot interface to a wire wrap motherboard, P/N A31U29801-1, which distributes all required signals and power to the precise standard assembly and to the top mounted connector panel.

The wire wrap motherboard is hinged to the top panel.

Wiring from the gold dot modules to the wire wrap motherboard is located in the tongue of the ICD. The gold dot interface contains 3200 connections, each of which consists of a gold dot plated with approximately 100 micro inches of 24 karat gold. The plating acts as environmental requirements for contacts.

Wiring wrapping is used extensively within the ICD, an provides low cost manufacturing and simplified maintenance, while providing design flexibility and reliability.

The precision standard assembly, which contains the DC standards consisting of regulator P/N ZVR-518-18.000 and voltage divider P/N 314242, the AC standard P/N OTS-02-1023, and the thermal converter P/N 1395A-1, is mechanically fastened in place where the component board is normally plugged in for a test program set ICD, and is in accordance with drawing A31U12676.

The resistance standards are mounted on the top mounted, hinged panel P/N A31U12674-7. In addition, the top mounted panel contains connectors J1, J2, J3, J4, J5, J7, and J8, and test points TP1 through TP30. Cables A31U12679-2, A31U12680-2, A31U12681-2, and A31U12682-2 comprise the cable set A1U12687-2, and are connected between J1, J2, J3, J4 on the top mounted panel, and J8, J9, J10, and J11, respectively, on the auxiliary interface panel (CEE -107, -109, -111), during self-alignment. For CEE -101, -103, -105 cables and connections are the same except that the cable and cable set dash numbers are -1 instead of -2. Test points TP1 through TP26 are available for calibration of the ICD at the designed calibration facility. Test points TP27 through TP30 are available for self-test and self-alignment of the Contact Test Set (CTS).

Accessibility to internal wiring and components are obtained via the hinged clam shell construction of the interface connector panel, which are able to be retained open at a 45 degree angle via pit pins, and two removable panel covers.

Transfer standards used for self-alignment have the following characteristics whithin the operating temperature range of 10°C to 32°C:

a. DC standards -

1. 18.0V ± 0.0056%/yr.

2. 9.0V ± 0.0076%/yr.

3. 0.90V ± 0.0076%/yr.

4. 0.090V ± 0.0076%/yr.

b. <u>AC standards</u> -

1. 1 VRMS ± 0.06%/yr; 20 KHz ± 1%

2. 10 VRMS ± 0.06%/yr; 20 KHz ± 1%

c. <u>Resistance standards</u> -

1. 0.1 Kohm ± 0.0055%/yr.

2. 1 Kohm ± 0.0055%/yr.

3. 10 Kohm ± 00.0055%/yr.

4. 100 Kohm ± 0.0055%/yr.

5. 1000 Kohm ± 0.0055%/yr.

d. <u>Programmable Load Current Sense Resistance Standards</u> -

1. 0.01 ohms ± 0.55%/yr.

2. 0.02 ohms ± 0.55%/yr.

3. 0.06 ohms ± 0.55%/yr.

e. <u>Thermal converter</u> -

1. Input impedance: 50 ± 0.15 ohms.

7.4 Instrument Switch Settings

7.4.1 General

This section contains jumper installation and address switch setting (DIP switches) procedures for the following CEE components.

1. Programmable DC Power Supply
2. Spectrum Analyzer
3. RF Generator (upper)
4. RF Generator (lower)
5. RF Millivoltmeter
6. Programmable Load
7. Power Meter
8. AC Power Supply
9. RFIU
10. PIC
11. Printer
12. Optical Disk Drive

13. Digital VIC

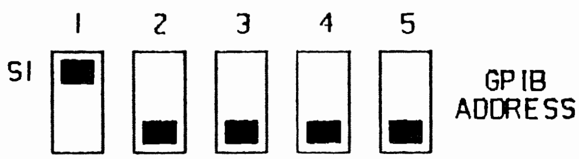
14. Analog VIC

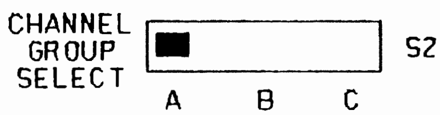
15. Amcodyne Disk Drive

16. Display Terminal

(-101, -103, -105 ASSY)

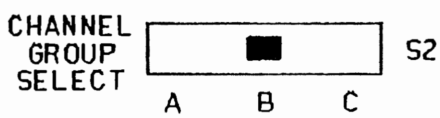
1A. AT REAR PANEL OF THE UPPER PROG DC PS (A31U29940), VERIFY THIS GPIB ADDRESS SWITCH AND THIS CHANNEL GROUP SELECT SWITCH SETTING:



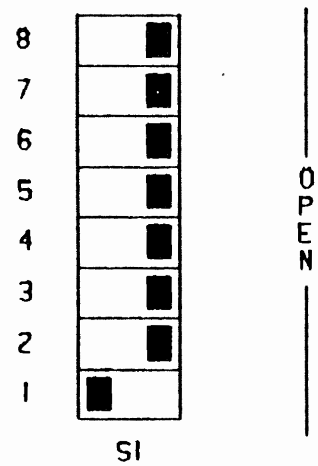


(-101, -103, -105 ASSY)

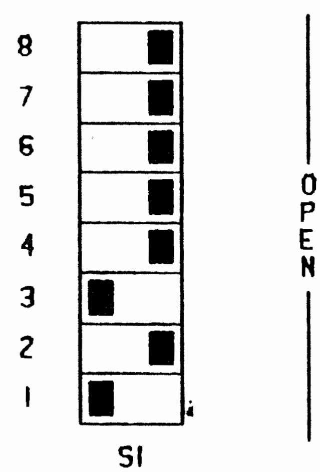
1B. AT REAR PANEL OF THE LOWER PROG DC PS (A31U29940), VERIFY CHANNEL GROUP SELECT SWITCH SETTING AS FOLLOWS:



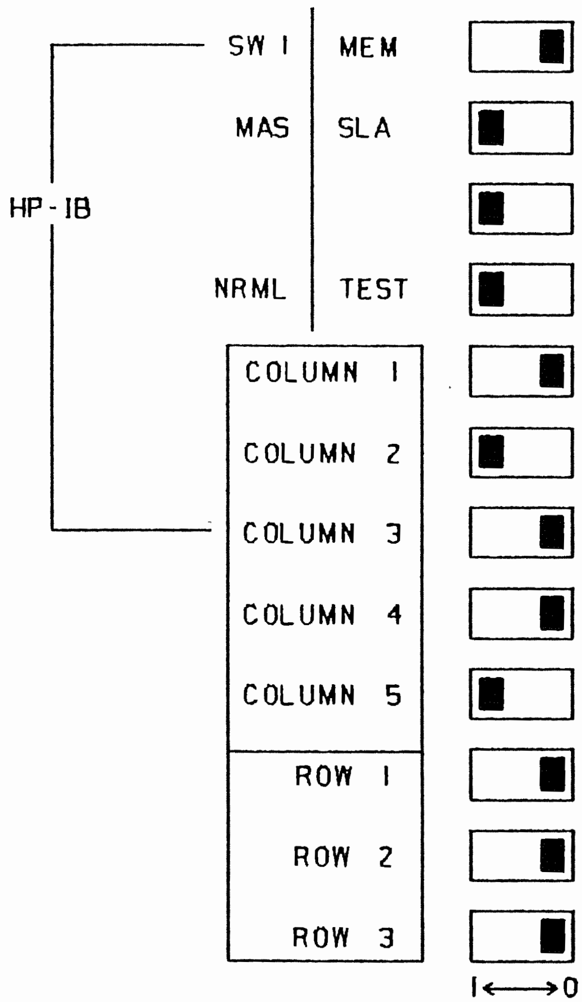
AT THE PROGRAMMABLE POWER SUPPLY, A31U29280-1, (-107, -109 & -111 ASSY),
REMOVE VXP CONTROLLER MODULE, A31U29280-115,
AND ON THE CONTROLLER MODULE,
VERIFY THE ADDRESS SWITCH SETTING:



AT THE PROGRAMMABLE POWER SUPPLY, A31U29280-3, (-109 ASSY)
REMOVE VXP CONTROLLER MODULE, A31U29280-115,
AND ON THE TOP OF THE CONTROLLER MODULE,
VERIFY THE ADDRESS SWITCH SETTING:

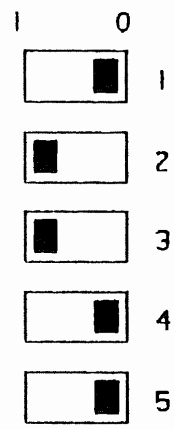


2. AT THE SPECTRUM ANALYZER, A31U29346, (-101, -103, -107, -109 ASSY) ON THE TOP OF THE LOCAL OSCILLATOR MODULE HP 70900A, VERIFY THIS ADDRESS SWITCH SETTING:



3. AT RF GENERATOR (UPPER).
   VERIFY THE FOLLOWING ADDRESS SWITCH SETTINGS:

AT THE REAR PANEL OF A31U29218 (-101 & -107 ASSY)



AT THE FRONT PANEL OF A31U29306 (-103 & -109 ASSY)
(WITH POWER ON).

DISPLAY CURRENT ADDR BY DEPRESSING
"SHIFT" AND "LOCAL" KEYS (ENT ADDR).

IF THE ADDRESS DISPLAYED IS NOT 6,
THEN ENTER 6 USING THE NUMERIC KEY PAD.

DEPRESS THE "Hz uV" KEY (OR ANY TERMINATOR).

4. AT RF GENERATOR (LOWER).
   VERIFY THE FOLLOWING ADDRESS SWITCH SETTINGS:

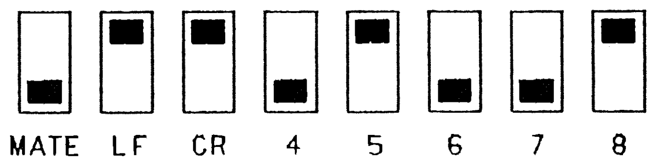
   AT THE FRONT PANEL OF A3IU29306 (-101,-103,-107,-109 ASSY)
   (WITH POWER ON).

   DISPLAY CURRENT ADDR BY DEPRESSING "SHIFT" AND "LOCAL" KEYS (ENT ADDR).

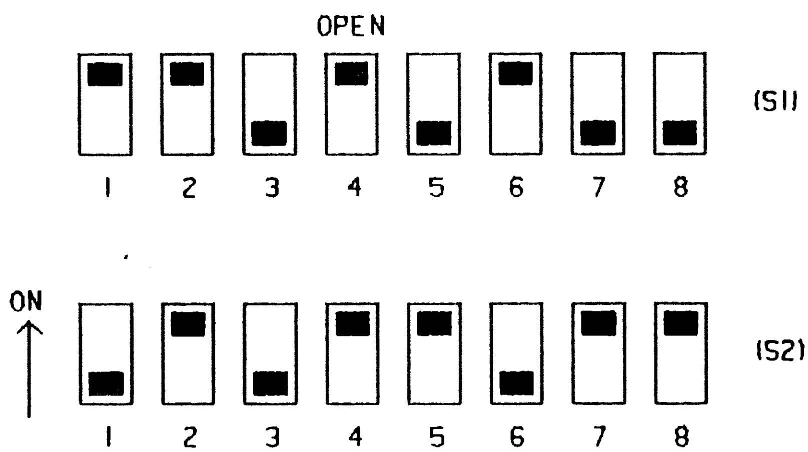
   IF THE ADDRESS DISPLAYED IS NOT 10, THEN ENTER 10 USING THE NUMERIC KEY PAD.

   DEPRESS THE "Hz uV" KEY (OR ANY TERMINATOR).

5. AT REAR PANEL OF RF MILLIVOLTMETER, A31U29399, (-103 & -109 ASSY)
VERIFY THIS GPIB ADDRESS SWITCH SETTING:

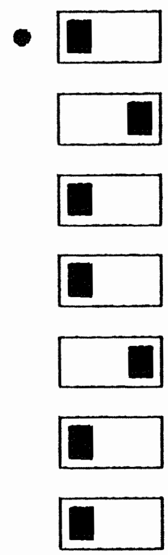


6. AT THE PROG. LOAD (A31U29176),
OPEN HINGED TOP COVER TO GAIN ACCESS TO
MICROPROCESSOR CARD MOUNTED ON INNER SIDE OF TOP COVER.
VERIFY THIS ADDRESS SWITCH SETTING:

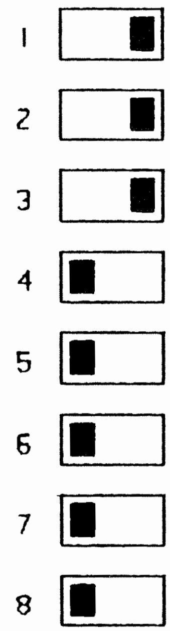


7. AT POWER MTR., A31U14845, (-101, -103, -107, -109 ASSY)

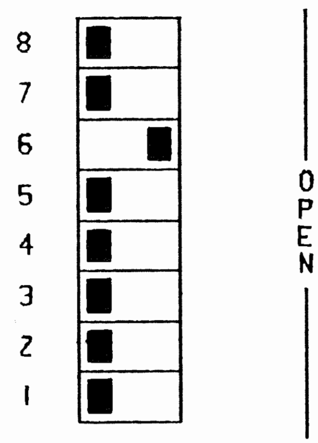
LOOSEN ONE CAPTIVE SCREW AT TOP REAR OF PWR MTR.
SLIDE COVER OFF TOWARD REAR OF PWR MTR.
AT SWITCH NEAR REAR PANEL,
VERIFY THIS ADDRESS SETTING:



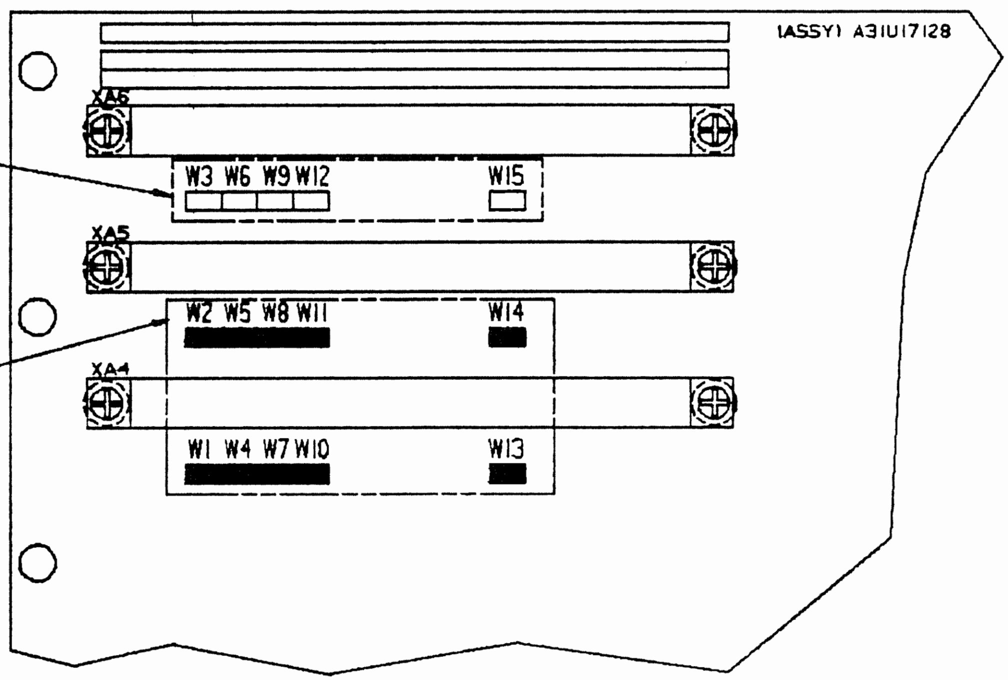
8. AT REAR PANEL OF AC PS, A31U29364,
VERIFY THIS ADDRESS SWITCH SETTING:



9. AT THE RFIU, A31U13560, (-101, -103, -107, -109 ASSY)
OPEN TOP COVER TO GAIN ACCESS TO
MICROPROCESSOR CARD (U20, A31U13696).
VERIFY THIS ADDRESS SWITCH SETTING:

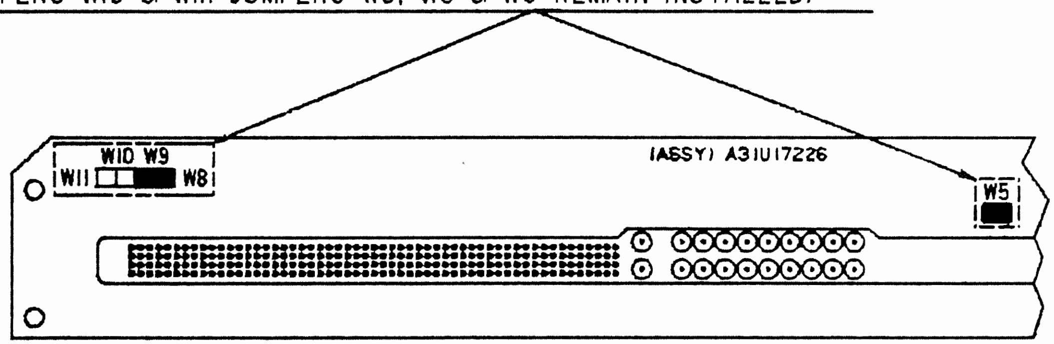


10. ON PIC MOTHERBOARD, (A31U17128), REMOVE JUMPERS W3,W6,W9,W12 & W15.

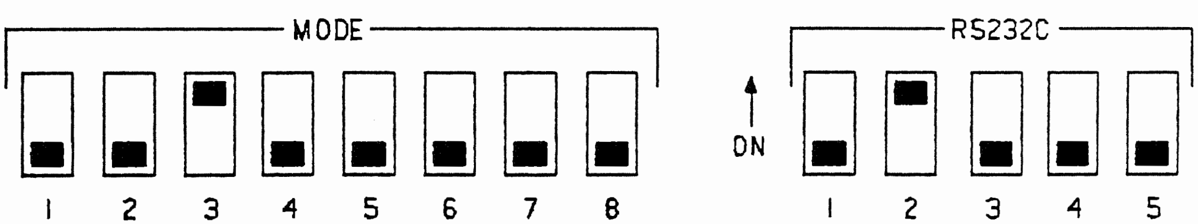


JUMPERS REMAINED INSTALLED
W1,W2,W4,W5,W7,W8,
W10,W11,W13,W14

11. ON PIC MOTHERBOARD (A31U17226).
REMOVE JUMPERS W10 & W11. JUMPERS W5, W8 & W9 REMAIN INSTALLED.



12. AT PRINTER (A31U29290 P/O A31U13070 ASSY), ON REAR.
VERIFY THE FOLLOWING ADDRESS AND MODE SETTINGS.

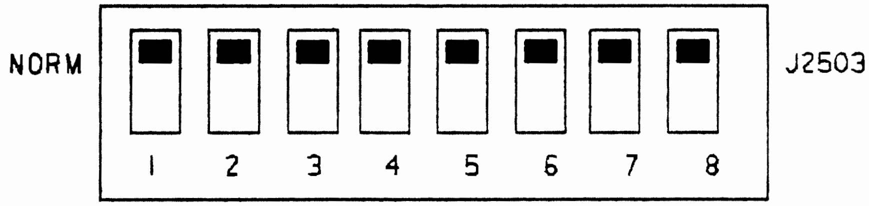


13. AT THE OPTICAL DISK DRIVE (A31U29314), VERIFY THAT THE W4 PARITY ENABLE JUMPER IS INSTALLED.

UNDER THE TOP COVER

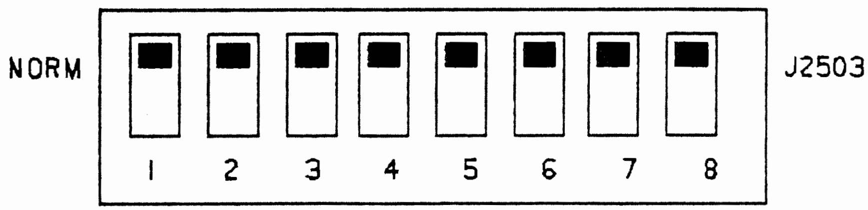
---

14. AT THE DIGITAL AND ANALOG VIC, VERIFY THAT MICROPROSSOR CARDS (P/N A31U29294) LOCATED IN SLOT XA1 HAVE THE FOLLOWING SWITCH SETTINGS.

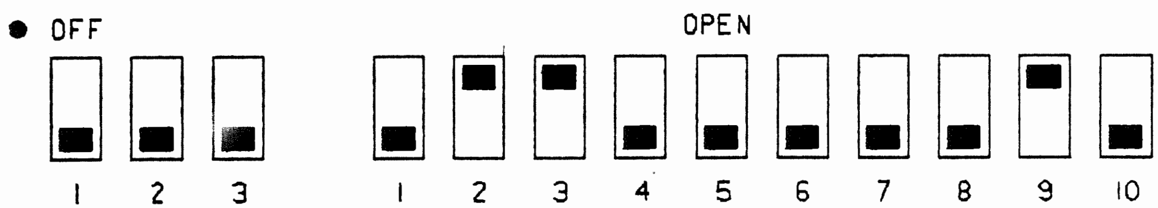


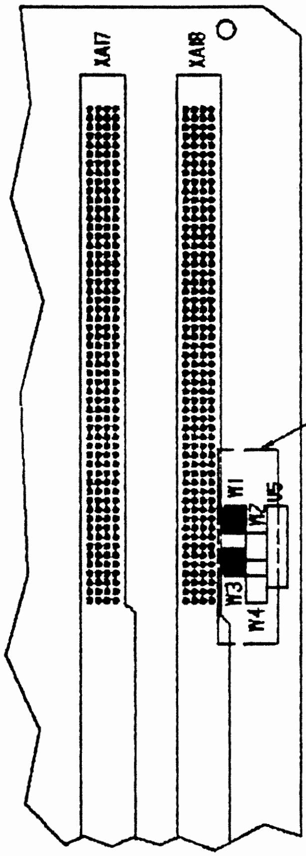
---

15. AT PERIPHERAL INTERFACE CONTROLLER, A31U17460, VERIFY THAT THE MICROPROCESSOR CARD (P/N A31U29294) LOCATE IN SLOT XA1 HAS THE FOLLOWING SWITCH SETTINGS:



16. AT DISC DRIVE (A31U29229) REMOVE LOWER FRONT PANEL (BELOW DISC DRIVE DOOR). VERIFY THIS ADDRESS SWITCH SETTING:





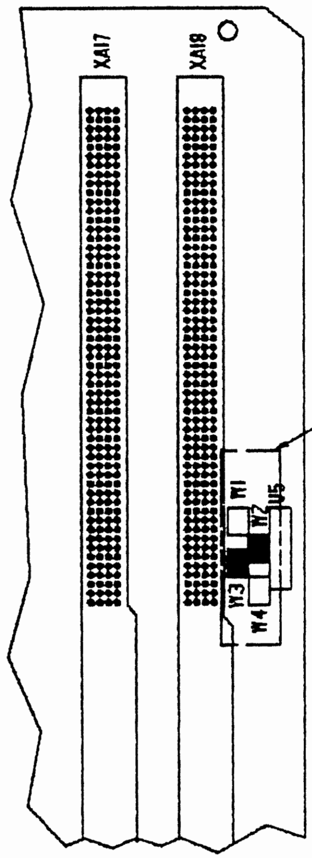
(-101, -103, -105 ASSY ONLY)

17. ON MOTHERBOARD (A31U13640) OF DIGITAL VIC.
REMOVE JUMPERS W2 & W4.

JUMPERS W1 & W3 REMAIN INSTALLED.

(-107, -109, -111 ASSY ONLY)

ON MOTHERBOARD (A31U13640) OF DIGITAL VIC.
VERIFY JUMPERS W1 & W3 ARE INSTALLED



(-101, -103, -105 ASSY ONLY)

18. ON MOTHERBOARD (A31U13640) OF ANALOG VIC,
REMOVE JUMPERS W1 & W4.
JUMPERS W2 & W3 REMAIN INSTALLED.

(-107, -109, -111 ASSY ONLY)

ON MOTHERBOARD (A31U13640) OF ANALOG VIC,
VERIFY JUMPERS W2 & W3 REMAIN INSTALLED.

19. AT THE DISPLAY TERMINAL (A31U29291),
ENTER THE FOLLOWING SEQUENCE OF COMMANDS
ON THE KEYBOARD TO SETUP THE CORRECT PARAMETERS:

DEPRESS THE "SETUP" KEY.

AT THE ASTERISK PROMPT TYPE:

- * FACTORY
  DEPRESS THE "RETURN" KEY.
  DEPRESS THE "SETUP" KEY WHEN THE CURSOR REAPPEARS.

AT THE ASTERISK PROMPT ENTER THE FOLLOWING:
(AFTER EACH ENTRY DEPRESS THE "RETURN" KEY).

- * ORIGINMODE ABSOLUTE
  DEPRESS THE "RETURN" KEY (2) MORE TIMES.
- * BAUDRATE 9600, 9600
- * FLAGGING IN/OUT
- * PARITY EVEN
- * CODE ANSI

  [FOR 4208 TERMINALS W/CAROL TOUCH SMART-Y'S ONLY:
  * TERMINAL 4107]

- * NVSAVE
  DEPRESS THE "SETUP" KEY TO EXIT SETUP MODE.