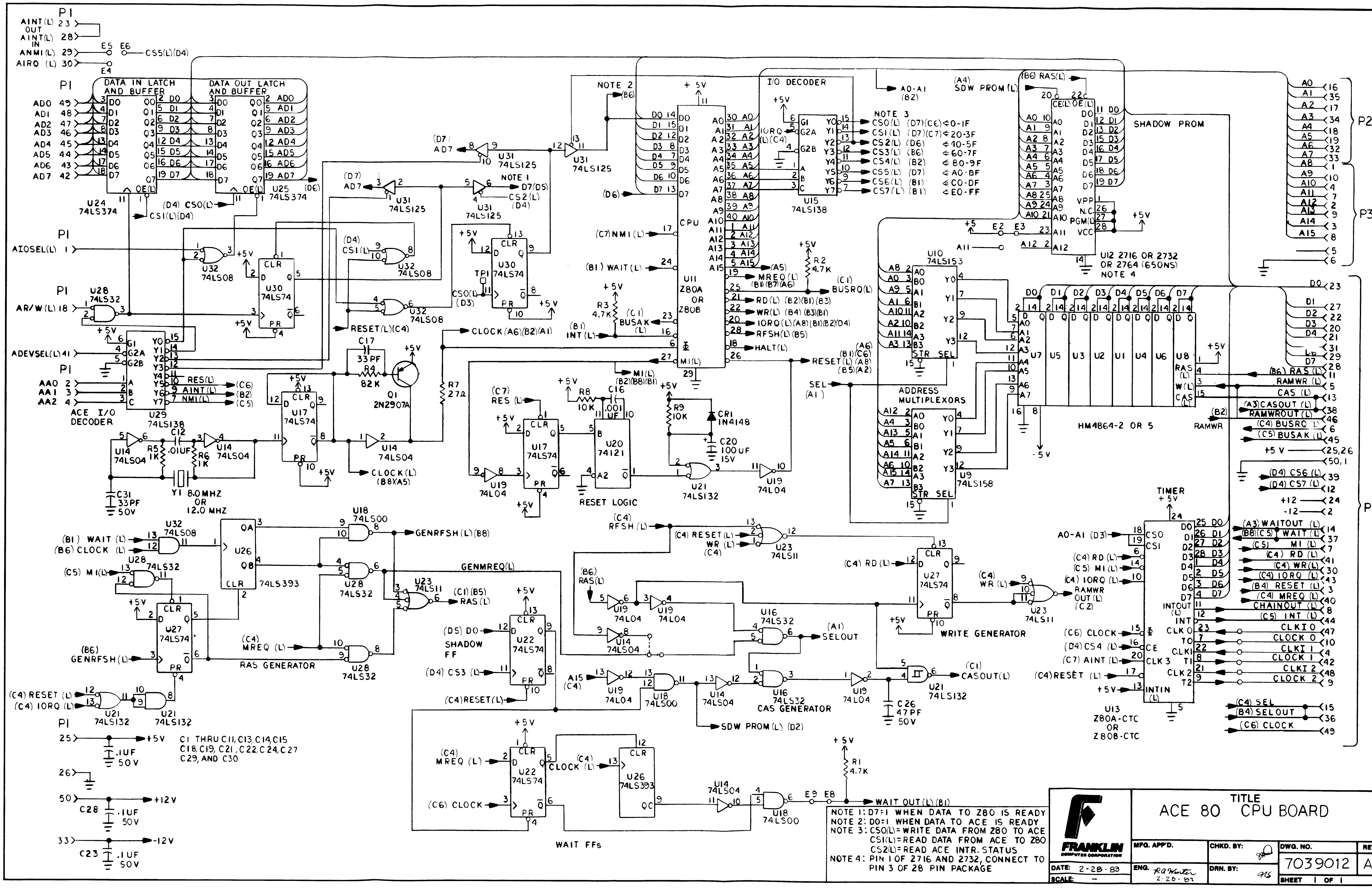

DATA IN LATCH AND BUFFER
U24 74LS374
DATA OUT LATCH AND BUFFER
U25 74LS374
ACE I/O DECODER
U29 74LS138
I/O DECODER
U15 74LS138
U11 Z80A OR Z80B CPU
SHADOW PROM
U12 2716 OR 2732 OR 2764 (650NS)
NOTE 4
ADDRESS MULTIPLEXORS
U10 74LS153
U9 74LS158
HM4864-2 OR 5
U7 U5 U3 U2 U1 U4 U6 U8
RESET LOGIC
U20 74121
Y1 8.0MHZ OR 12.0 MHZ
RAS GENERATOR
CAS GENERATOR
WRITE GENERATOR
SHADOW FF
WAIT FFs
TIMER
U13 Z80A-CTC OR Z80B-CTC
U26 74LS393
Q1 2N2907A
CR1 1N4148
C1 THRU C11, C13, C14, C15 C18, C19, C21, C22, C24, C27 C29, AND C30
NOTE 3
CS0(L) (D7)(C6) ← 0-1F
CS1(L) (D7)(C7) ← 20-3F
CS2(L) (D6) ← 40-5F
CS3(L) (B6) ← 60-7F
CS4(L) (B2) ← 80-9F
CS5(L) (D7) ← A0-BF
CS6(L) (B1) ← C0-DF
CS7(L) (B1) ← E0-FF
NOTE 1: D7=1 WHEN DATA TO Z80 IS READY
NOTE 2: D0=1 WHEN DATA TO ACE IS READY
NOTE 3: CS0(L)=WRITE DATA FROM Z80 TO ACE
CS1(L)=READ DATA FROM ACE TO Z80
CS2(L)=READ ACE INTR. STATUS
NOTE 4: PIN 1 OF 2716 AND 2732, CONNECT TO PIN 3 OF 28 PIN PACKAGE
FRANKLIN COMPUTER CORPORATION
TITLE
ACE 80 CPU BOARD
MFG. APP'D.
CHKD. BY:
DWG. NO. 7039012
REV. A
DATE: 2-28-83
SCALE: —
ENG. RA Winter 2-28-83
DRN. BY:
SHEET 1 OF 1

RAS(L)
MARϕ-11
DXB1,2,4
DYB8,16,32
DYB1-256
DXB1-32
MAR/WDϕ-15
T/C

ZE14 LS283
DXB8
DYB64
DXB16
DYB128
DXB32
1ZD14-1 +5RB6
ZC11 ϕ4

ZE13 LS153
MARϕ
MAR5
DXB1
Σ3
MAR1
MAR6
DXB2
Σ4
YA 7 R/CA2
YB 9 R/CA5

ZE12 LS153
MAR2
MAR4
DXB4
Σ2
MAR3
MAR9
Σ1
DYB32
YA 7 R/CA1
YB 9 R/CA4

ZE11 LS153
MAR7
MAR10
DYB8
MAR8
MAR11
DYB16
YA 7 R/CAϕ
YB 9 R/CA3

1MHZ
R/CAS

R6D1 +5 1K 1K
RSE2

R/CAϕ
R/CA1
R/CA2
R/CA3
R/CA4
R/CA5
R/CA6
DO/DI 3
ZC14-11

4116 DRAM 16Kx1 256/256 ACCESS TYP. 32 PLACES
RAS
Aϕ A1 A2 A3 A4 A5 A6
R/W
DI DO

RAM ARRAY

(MEMORY DATA REG. ϕ THRU 7) MDRϕ-7

ZB5 LS174
ZB8 LS174
RAS(L)
+5RB1 1ZD1-4
+5RB5 3ZB9-2
MDRϕ MDR1 MDR2 MDR3 MDR4 MDR5 MDR6 MDR7
1Q 4Q 5Q 2Q 3Q
CLR 4D 5D 2D 3D
MDQϕ MDQ1 MDQ2 MDQ3 MDQ4 MDQ5 MDQ6 MDQ7

KYBRD
KDATA(L)
MDATA(L)

ZB7 LS257
MDR7 MDR6 MDR5 MDR4
KFLG KYB6 KYB5 KYB4
KYB3 KYB2 KYB1 KYBϕ
YB DB7 DB6 DB5 DB4
YA DB3 DB2 DB1 DBϕ
YC
EO S
3ZH14-6

ZB6 LS257
MDR3 MDR2 MDR1 MDRϕ
EA3-6

+12 CC2-6 CD3-6 CE4-8 CF9-12
+5 CC7-8 CD7-9 CE9-11 CF6-8
-5 CC9-11 CD10-12 CE13-15 CF13
VDD VSS VCC VBB

CASϕ-3(L)
CAS4-7(L)
CAS8-B(L)
CASC-F(L)
CAS
ZC3 ZC4 ZC5 ZC6 ZC7 ZC8 ZC9 ZC10
ZD3 ZD4 ZD5 ZD6 ZD7 ZD8 ZD9 ZD10
ZE3 ZE4 ZE5 ZE6 ZE7 ZE8 ZE9 ZE10
ZF3 ZF4 ZF5 ZF6 ZF7 ZF8 ZF9 ZF10
$\phi\phi\phi\phi$-3FFF
4$\phi\phi\phi$-7FFF
8$\phi\phi\phi$-BFFF
DXXX
D$\phi\phi\phi$-FFFF

ZC12 LS257
DYB1
DYB2
DYB4
DCAϕ
DCA3
DCA6
DRA6
ZC1 LS153
(MCA6) MRA6
YA 7 R/CA6

ZC11 ϕ4
H24/4ϕ 3ZC13-6
3ZG14-6 PAGE 2/1
3ZB11-6 HRES
ZH1 LSϕ8

MAR12
MAR13
MAR12-13
ZF'7 LSϕ8
ZRA6(L)
ZF'9 LS86
ZF'6 LS2ϕ
NOT-EF
ALT-D ZF'6-2
EF'6-2
S-DEF
RG1 +5RG1
ZF'9-1

CASC-F(L)
ZF'8 LS32
S-DEF(L)
ZF'5 LSϕ8

CAS(L)
ZE2 LS139
1E 1Yϕ 1Y1 1Y2 1Y3
2E 2Y3 2Y2 2Y1 2Yϕ
CASϕ-3(L)
CAS4-7(L)
CAS8-B(L)
CASC-F(L)
ZD2 LS2ϕ

ZK1 LS257
MAR14
MAR15
1MHZ

1MHZ(L)
MDR/W
DO/DI ZC3-3
ZC14 LS32

ZA3 LS$\phi\phi$
MDATA(L) ZB6-15
MAR12-13

ZF'5 LSϕ8
1PJ7-32 INH(L)
Y2 X2 ZF'4-9
R-DEF

WENB
DEF
ZF'8 LS32
ZF'6 LS2ϕ
ZF'4 LS$\phi\phi$

1ZH2-15 PSϕ(L)
RH1 100Ω
CG2 22μf

ZF'2
ZF'3 LS175
1D CLK
2D
3D
4D
CLR
ALT-D ZF'6-2
RENB(L)
ZF'7 LSϕ8
X3 Y3

MAR3
MAR1
MARϕ
ZF'9-1ϕ +5RG1
ZF'9 LS86
ZF'7 LSϕ8
ODD READ

CF'1 4.7μfd 35v
RF'1 12K +5

S-DEF(L)
ZF'5 LSϕ8
ZF'2
ZF'4 LS$\phi\phi$
ZF'5-3 R-DEF
MAR > BFFF

ZH1 LSϕ8
MAR15 MAR14 MAR13 MAR12 MAR11
ZG12 LS138
E3 C B A E2 E1
Y7 Y6 Y5 Y4 Y3 Y2 Y1 ϕ
2KF8(L) 2KFϕ(L) 2KE8(L) 2KEϕ(L) 2KD8(L) 2KDϕ(L)
1MHZ(L)
2KC8(L) 1PJ7-2ϕ
2KCϕ(L) 1ZH12-4

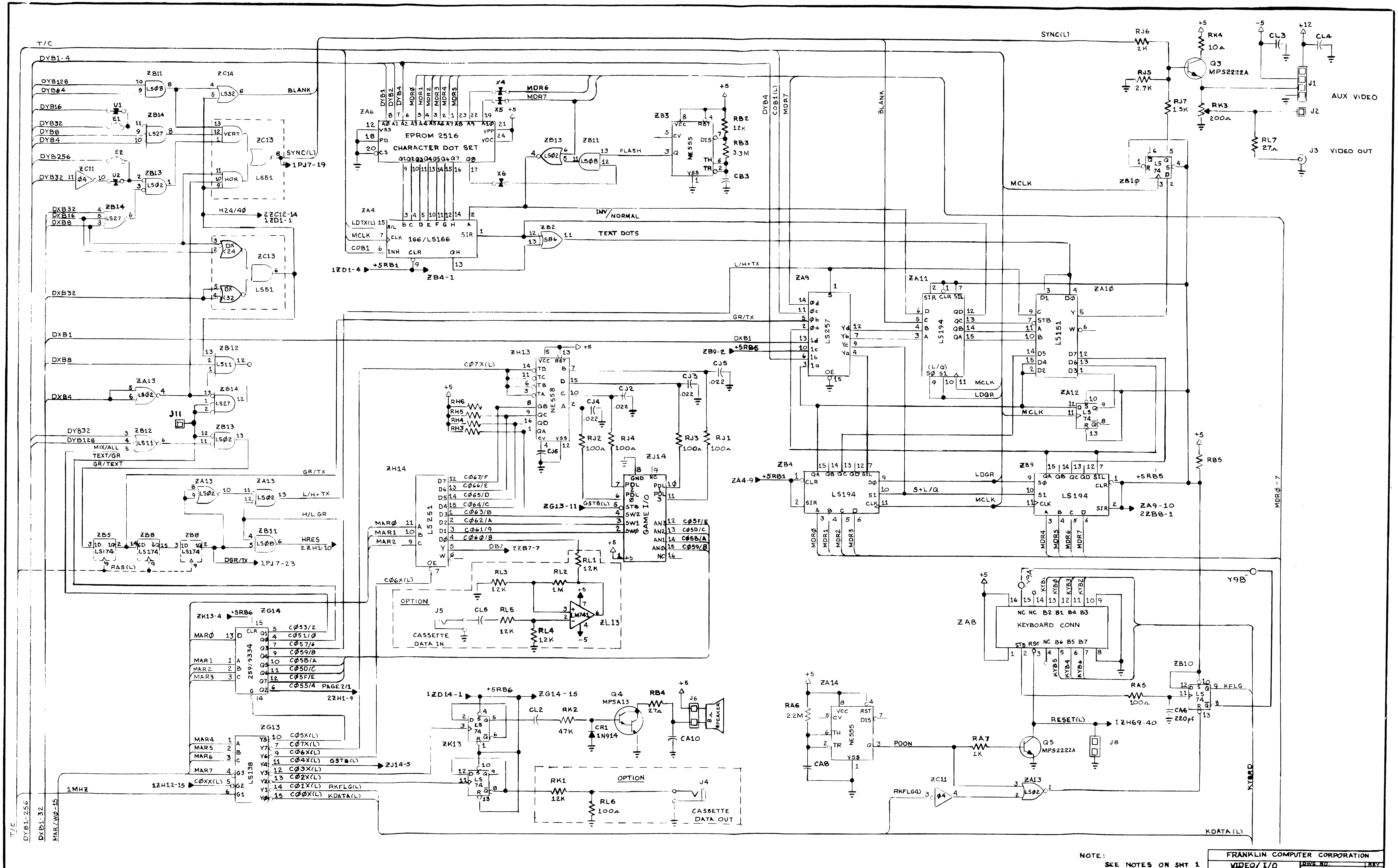
MARϕ MAR1 MAR2 MAR3 MAR4 MAR5 MAR6 MAR7 MAR8 MAR9 MAR10
Aϕ A1 A2 A3 A4 A5 A6 A7 A8 A9 A10

ZG2 ZG3 ZG5 ZG7 ZG8 ZG10
CS PD
Dϕ D1 D2 D3 D4 D5 D6 D7
DBϕ DB1 DB2 DB3 DB4 DB5 DB6 DB7
VCC VPP VSS
CG1, 3 +5
2516 EPROM'S

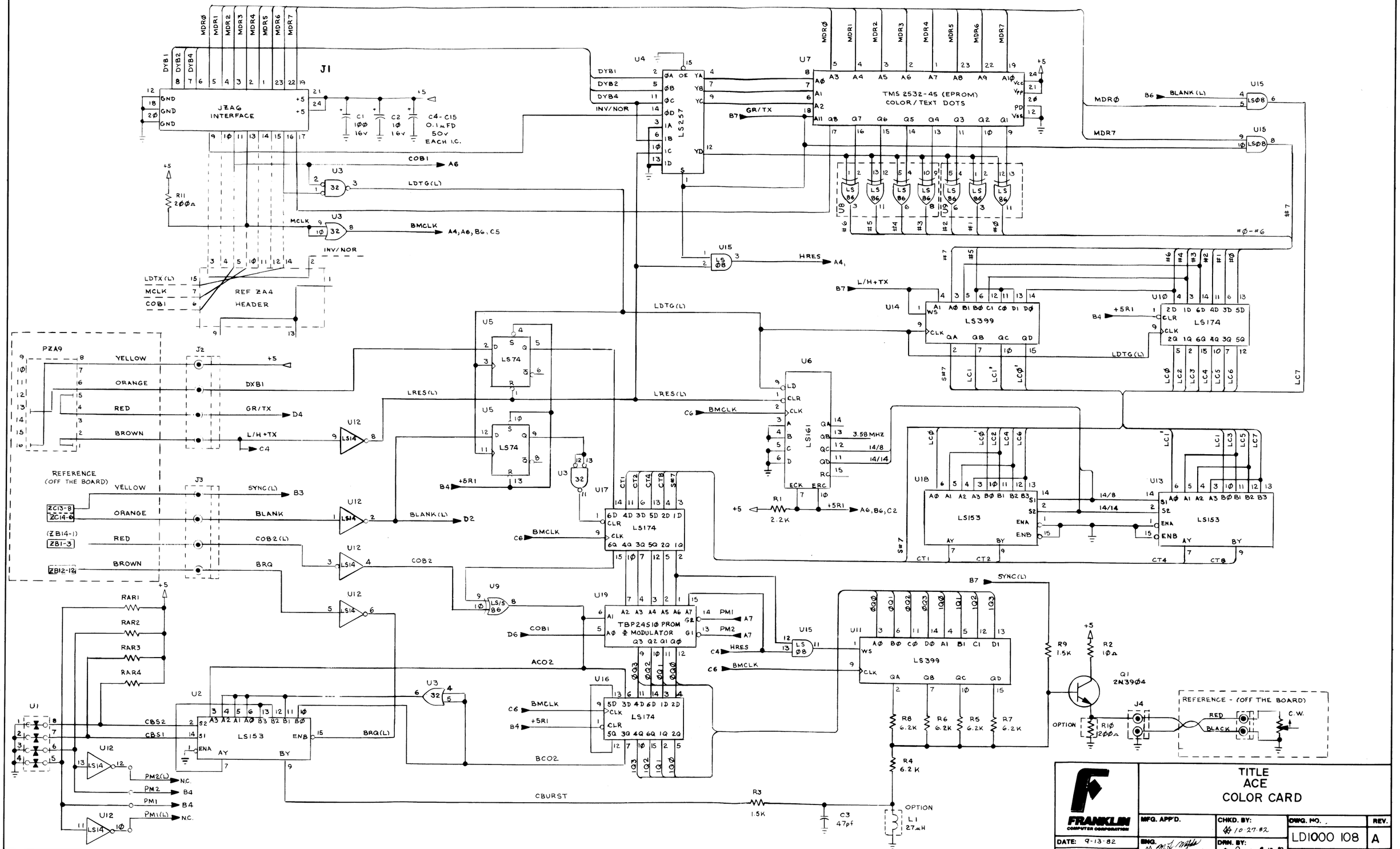
MARϕ-15
1MHZ(L)
DBϕ-7

NOTE:
SEE NOTES ON SHT. 1

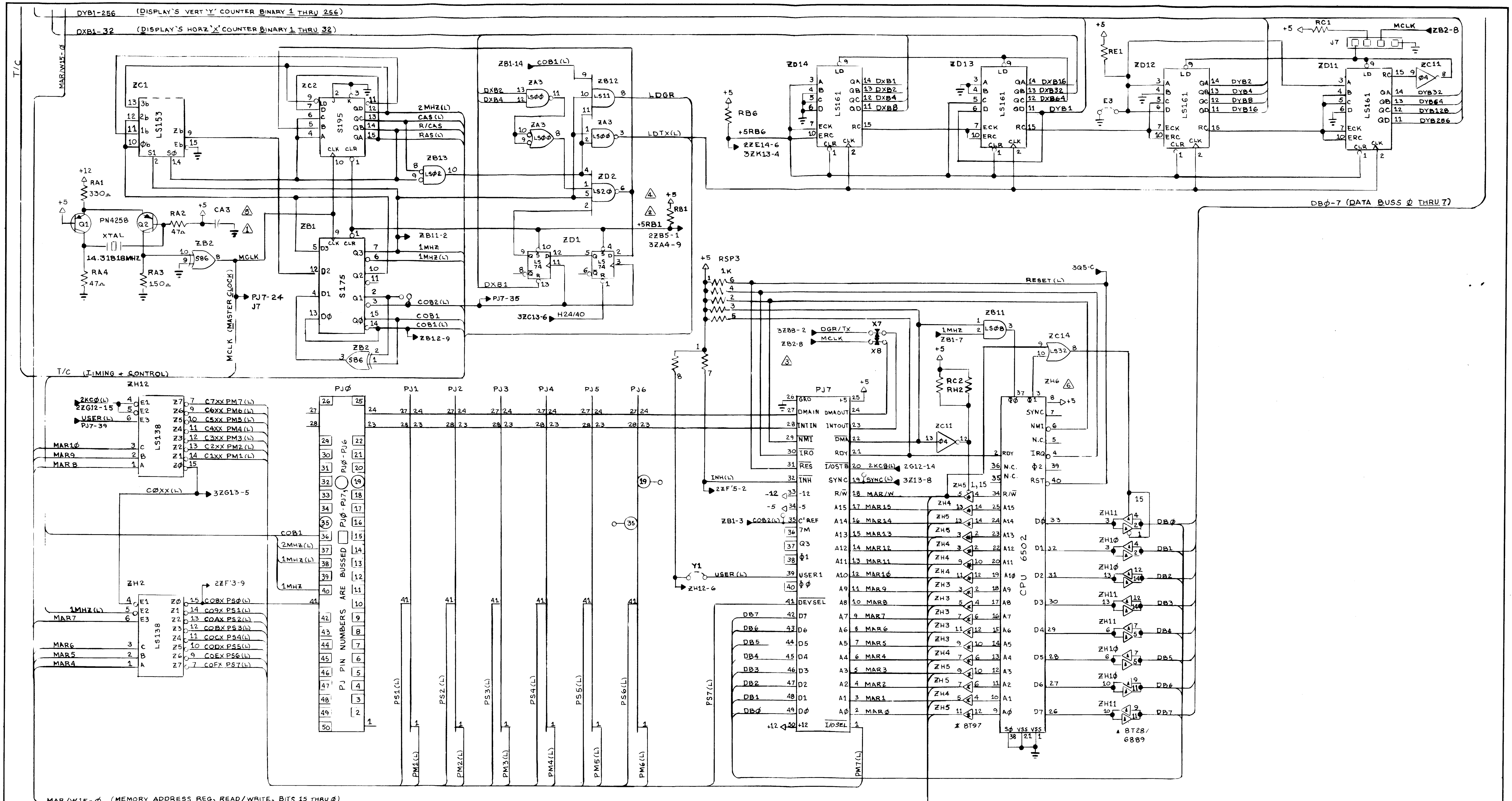
FRANKLIN COMPUTER CORPORATION		
MEMORY ARRAY	DWG NO: LD1200-101-	REV A
DATE 4/82 SHEET 2 OF 3		



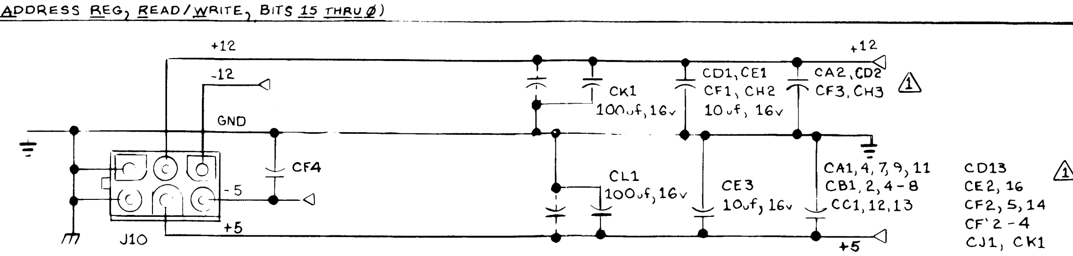
SYNC(L)
AUX VIDEO
VIDEO OUT
MPS2222A
EPROM 2516
CHARACTER DOT SET
BLANK
FLASH
NE555
INV/NORMAL
TEXT DOTS
166/LS166
L/H+TX
GR/TX
LS257
LS194
LS151
MCLK
LDGR
NE558
GAME I/O
LS251
OPTION
CASSETTE DATA IN
LM741
259/9334
LS138
MPSA13
SPEAKER
CASSETTE DATA OUT
KEYBOARD CONN
RESET(L)
POON
KDATA(L)
KYBRD
NOTE: SEE NOTES ON SHT 1
FRANKLIN COMPUTER CORPORATION
VIDEO/I/O
DATE 4/82 SHEET 3 OF 3
LD1200-101-
A



FRANKLIN COMPUTER CORPORATION	TITLE ACE COLOR CARD		
DATE: 9-13-82	MFG. APP'D.	CHKD. BY: 10.27.82	DWG. NO. LD1000 108
SCALE:	ENG. 10.27.82	DRN. BY: M. Brun 9-13-82	REV. A
			SHEET 1 OF 1



DYB1-256 (DISPLAY'S VERT 'Y' COUNTER BINARY 1 THRU 256)
DXB1-32 (DISPLAY'S HORZ 'X' COUNTER BINARY 1 THRU 32)
T/C
MAR/W15-Ø
ZC1 LS153
ZC2 S195
ZB1 S175
ZB2 S86
ZB13 LSØ2
ZA3 LSØØ
ZB12 LS11
ZD2 LS2Ø
ZD1 LS74
ZD14 LS161
ZD13 LS161
ZD12 LS161
ZD11 LS161
ZC11 Ø4
2MHZ(L)
CAS(L)
R/CAS
RAS(L)
LDGR
LDTX(L)
COB1(L)
DXB2
DXB4
DXB1
+12 RA1 330Ω
PN4258
Q1
Q2
RA2 47Ω
CA3
XTAL 14.31818MHZ
RA4 47Ω
RA3 150Ω
MCLK
MCLK (MASTER CLOCK)
PJ7-24 J7
ZB11-2
1MHZ
1MHZ(L)
COB2(L)
PJ7-35
COB1
COB1(L)
ZB12-9
3ZC13-6 H24/40
+5RB1
2ZB5-1
3ZA4-9
RB6
+5RB6
2ZE14-6
3ZK13-4
DXB1 DXB2 DXB4 DXB8
DXB16 DXB32 DXB64 DYB1
DYB2 DYB4 DYB8 DYB16
DYB32 DYB64 DYB128 DYB256
E3
RE1
RC1
MCLK
ZB2-8
DBØ-7 (DATA BUSS Ø THRU 7)
3Q5-C
RESET(L)
+5 RSP3 1K
T/C (TIMING + CONTROL)
ZH12 LS138
2KCØ(L)
2ZG12-15
USER(L)
PJ7-39
C7XX PM7(L)
C6XX PM6(L)
C5XX PM5(L)
C4XX PM4(L)
C3XX PM3(L)
C2XX PM2(L)
C1XX PM1(L)
MAR1Ø
MAR9
MAR8
CØXX(L)
3ZG13-5
COB1
2MHZ(L)
1MHZ(L)
1MHZ
ZH2 LS138
2ZF'3-9
1MHZ(L)
MAR7
MAR6
MAR5
MAR4
COBX PSØ(L)
CO9X PS1(L)
COAX PS2(L)
COBX PS3(L)
COCX PS4(L)
CODX PS5(L)
COEX PS6(L)
COFX PS7(L)
PJØ PJ1 PJ2 PJ3 PJ4 PJ5 PJ6
PJØ-PJ6 PJØ-PJ7 ARE BUSSED
PJ PIN NUMBERS
PS1(L) PS2(L) PS3(L) PS4(L) PS5(L) PS6(L) PS7(L)
PM1(L) PM2(L) PM3(L) PM4(L) PM5(L) PM6(L) PM7(L)
MAR/W15-Ø (MEMORY ADDRESS REG, READ/WRITE, BITS 15 THRU Ø)
X7
X8
3ZB8-2 DGR/TX
ZB2-8 MCLK
PJ7
GND
DMAIN
DMAOUT
INTIN
INTOUT
NMI
IRQ
RES
INH
INH(L)
2ZF'5-2
I/OSTB
2KCB(L)
2G12-14
SYNC
SYNC(L)
3Z13-8
R/W
MAR/W
C'REF
7M
Q3
Φ1
Y1
USER(L)
ZH12-6
USER1
ΦØ
DEVSEL
I/OSEL
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBØ
ZB11 LSØ8
ZB1-7
ZC14 LS32
ZC11 Ø4
RC2 RH2
ZH6
ZH5 ZH4 ZH3
MAR15 MAR14 MAR13 MAR12 MAR11 MAR1Ø MAR9 MAR8 MAR7 MAR6 MAR5 MAR4 MAR3 MAR2 MAR1 MARØ
8T97
CPU 6502
RDY
ΦØ Φ1 Φ2
NMI
IRQ
RST
N.C.
SØ VSS VSS
ZH11
ZH1Ø
8T28/6889

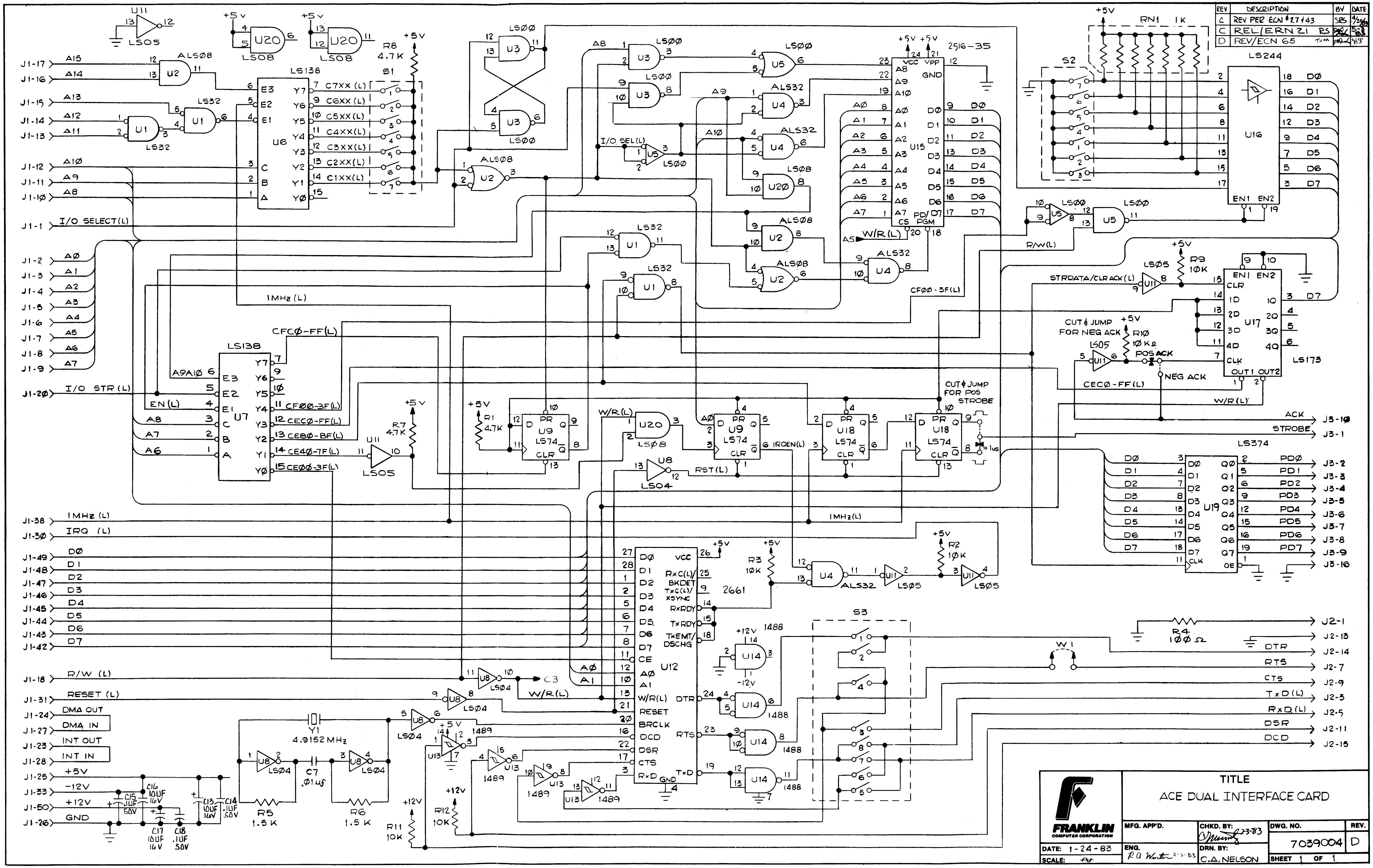


POWER DISTRIBUTION

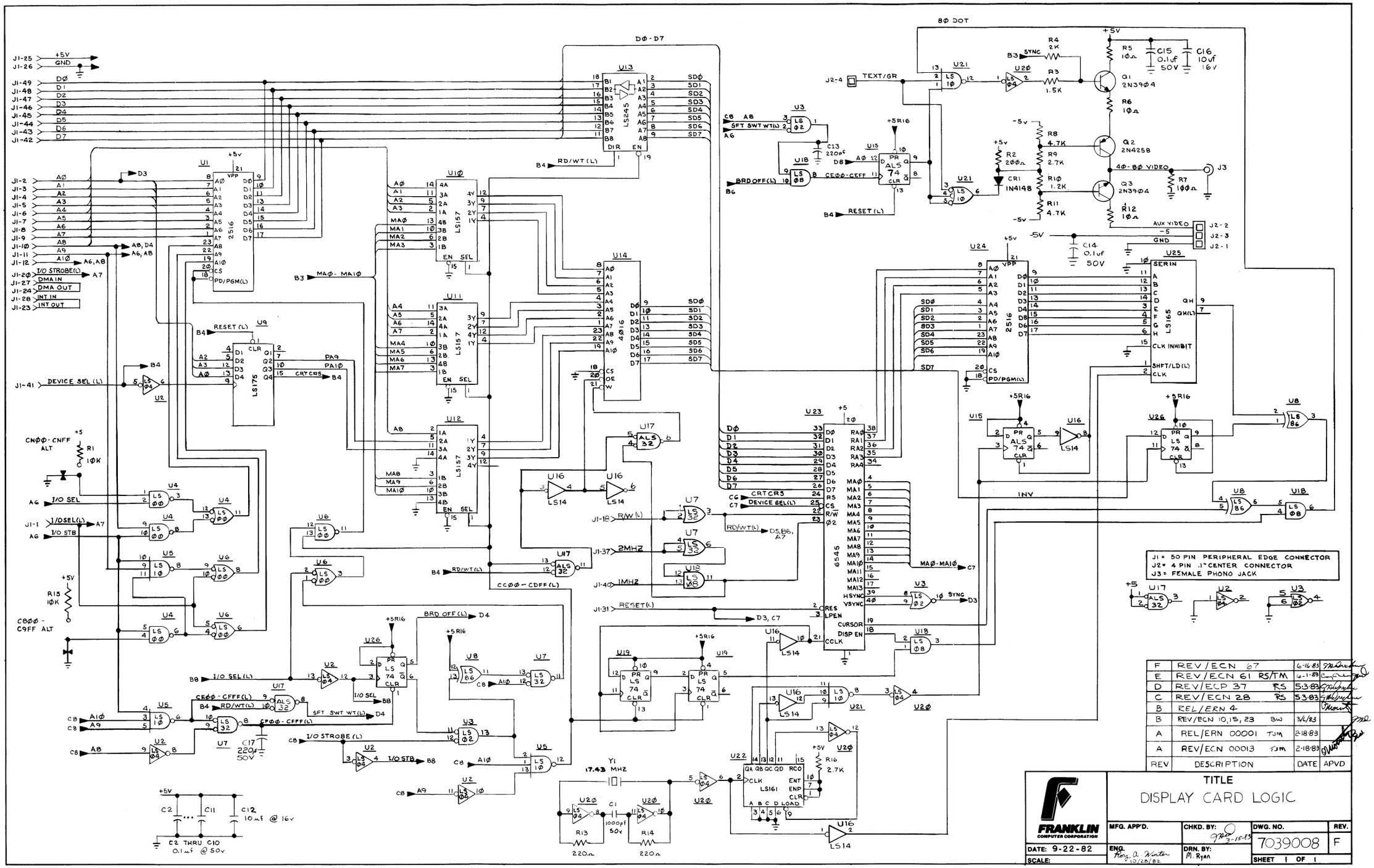
NOTES:

1. ALL CAPS ARE Ø.1 uFD, 50v UNLESS MARKED OTHERWISE.
2. ALL RESISTORS ARE 2.2K, 5%, 1/4w UNLESS MARKED OTHERWISE.
3. ZB2-8 IS PIN 8 OF AN IC AT P.C. BOARD LOCATION B2 SHOWN ON THIS SHEET.
   3ZB8-2 IS PIN 2 OF AN IC AT P.C. BOARD LOCATION B8 SHOWN ON SHEET 3.
4. RB1 IS RESISTOR #1 IN P.C. BOARD ROW 'B'.
5. CA3 IS CAPACITOR #3 IN P.C. BOARD ROW 'A'.
6. ZH6 IS AN IC AT P.C. BOARD LOCATION ROW 'H', COLUMN '6' (HIGHEST IS 14).

FRANKLIN COMPUTER CORPORATION	TITLE ACE 1200 LOGIC			
	MFG. APP'D.	CHKD. BY: [signature]	DWG. NO. LD1200-101-	REV. A
DATE: 4-82	ENG. 7·14·82 [signature] M.L.	DRN. BY: M. Ryan		
SCALE:			SHEET 1 OF 3	



REV | DESCRIPTION | BY | DATE
C | REV PER ECN #27143 | SBS
C | REL/ERN 21 | RS
D | REV/ECN 65
TITLE
ACE DUAL INTERFACE CARD
FRANKLIN COMPUTER CORPORATION
MFG. APP'D.
CHKD. BY:
DWG. NO. 7039004
REV. D
DATE: 1-24-83
ENG.
DRN. BY: C.A. NELSON
SCALE:
SHEET 1 OF 1



REV	DESCRIPTION	DATE	APVD
F	REV/ECN 67	6-16-83	
E	REV/ECN 61 RS/TM	6-1-83	
D	REV/ECP 37 RS	5-3-83	
C	REV/ECN 28 RS	3-3-83	
B	REL/ERN 4		
B	REV/ECN 10,15,23 BW	3/1/83	
A	REL/ERN 00001 TJM	2-18-83	
A	REV/ECN 00013 TJM	2-18-83	

FRANKLIN COMPUTER CORPORATION

TITLE: DISPLAY CARD LOGIC

MFG. APP'D.	CHKD. BY:	DWG. NO.	REV.
DATE: 9-22-82	ENG. Hong A. Winter 10/20/82	DRN. BY: M. Ryan	7039008 F
SCALE:		SHEET 1 OF 1	