bc620AT
Time and Frequency Processor
8500-0011

User's Guide
Rev B.

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This equipment is certified to comply with the limits for a Class A computing device pursuant to Part 15, Subpart B of FCC Rules.

This equipment generates and uses radio frequency (RF) energy. If not installed and used properly, that is, in strict accordance with the manufacturer's instructions, it may cause interference to radio or television reception.

If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment on and off, the user is encouraged to correct the interference by one or more of the following measures:

- Reorient the radio/television receiving antenna.
- Move the antenna leads away from any wire runs to the personal computer with the Datum module.
- If using an indoor antenna, have a quality outdoor antenna installed.
- Relocate the personal computer with respect to the radio/television receiver.
- Connect the AC transformer to a different outlet so the personal computer and the radio/television are on different branch circuits.

If necessary, the user should consult the dealer or an experienced radio/television technician for suggestions or reference the following booklet, prepared by the Federal Communications Commission, helpful: How to Identify and Resolve Radio-TV Interference Problems. This booklet is available from the U.S: Government Printing Office, Washington D.C. 20402. Stock No. 004--000-00345-4.

Properly shielded and grounded cables and connectors must be used for connection to peripherals in order to meet FCC emission limits. Datum Inc. is not responsible for any radio or television interference caused by using other than recommended cables or by unauthorized modifications to this equipment. It is the responsibility of the user to correct such interference.

Declaration of Conformity

Application of Council Directive(s) 89/339/EEC

Standard(s) to which Conformity is Declared EN 50081-1, EN 50082-1

Manufacturer's Address 6781 Via Del Oro, San Jose, CA, USA 95119-1360

Importer's Name _____

Importer's Address _____

Type of Equipment Electronics

Model No. bc620AT

Serial No. _____ Year of Manufacture 1997

I, the undersigned, hereby declare that the equipment specified above conforms to the Directive(s) and Standard(s).

Place Datum, Inc. _____
(Signature)

Date October 7, 1997 Ronald L. Holm
(Full Name)

Engineering Manager
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CHAPTER ONE
INTRODUCTION

1.0 GENERAL

This bc620AT Time and Frequency Processor (TFP) User's Guide provides the following information:

- Introduction and key feature description.
- Installation and setup.
- Detailed operation and programming interfaces.
- Programming examples.
- Input and output signals.
- Drawing set.

1.1 KEY FEATURES

The bc620AT has been designed with the following key features:

- Time on demand (days through microseconds) with zero latency. This feature is implemented with hardware registers which latch the current time upon host request.
- Event logging (days through 0.1 microseconds). This feature is implemented with a second set of hardware registers. Time is captured on a positive or negative input edge or secondary bus time request.
- Four operational modes are supported. Modes are distinguished by the reference source.

Mode	Source Of Synchronization
0	Time code - IRIG A, IRIG B, XR3, 2137, NASA36 (modulated or DC).
1	Free running - on board 10 MHz oscillator (VCXO) used as reference.
2	1pps - synchronizes to external one pulse per second.
3	RTC - uses on board battery backed real time clock IC.
4	GPS - uses Acutime GPS receiver as reference (bc627AT only).

- Provides an output clock synchronized to the selected reference; programmable 1, 5, or 10 MHz TTL.

- All modes of operation are supplemented by flywheel operation (i.e. if synchronization source is lost the TFP will continue to function at the last known reference rate).

- Generates synchronized IRIG B time code. Modulated and DC level shift formats are produced simultaneously.

- Programmable frequency output (periodics) is provided. Pulse rates from 2.3 MHz to 2.5 MHz are supported.

- A time coincidence strobe output is provided. Programmable from days through milliseconds. This strobe also has an "each second" mode programmable to milliseconds.

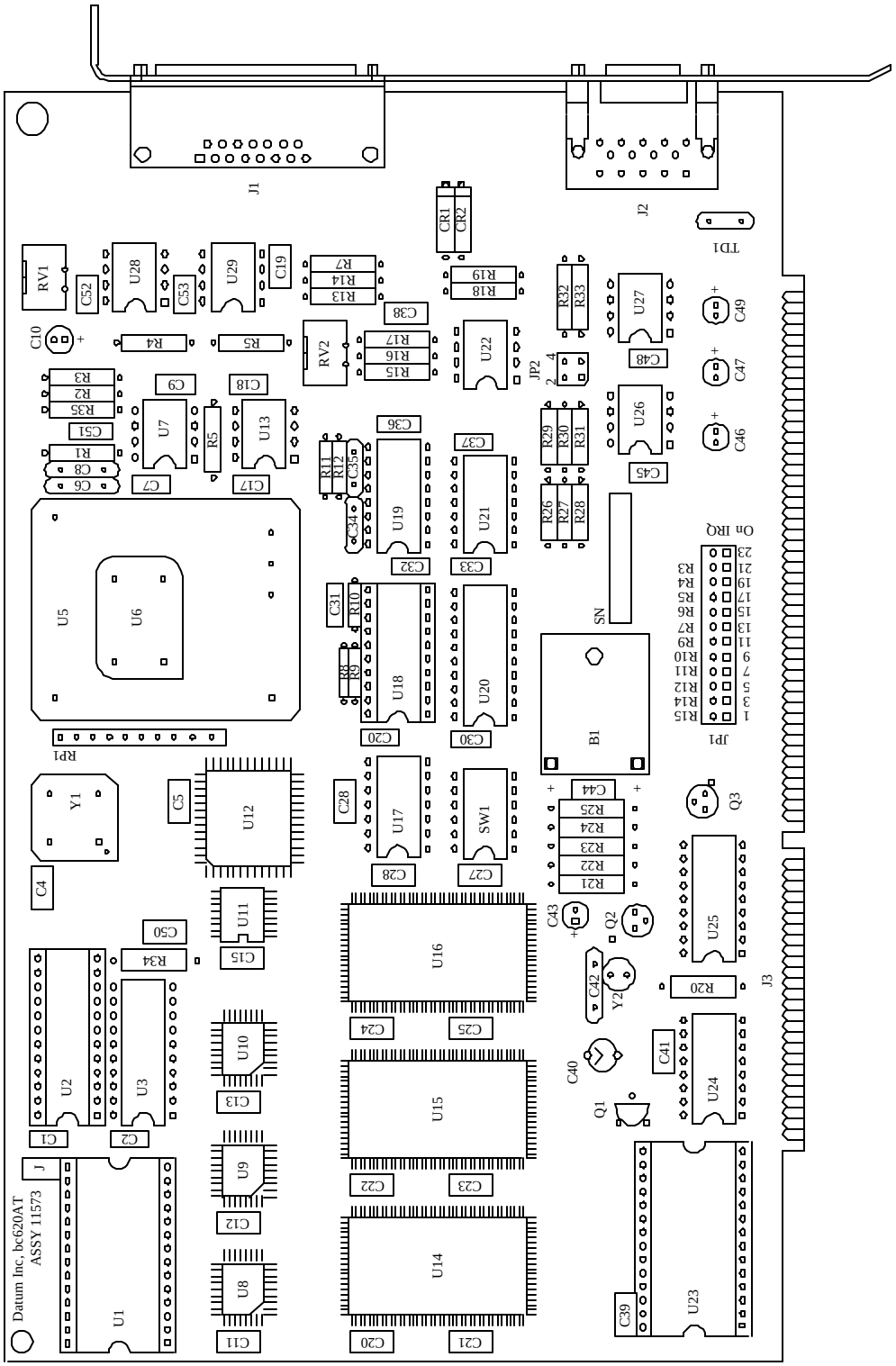
- Five maskable interrupt sources are supported. IRQ levels 3-7, 9-12, 14, and 15 can be selected via jumper JP1.

Interrupt #	Source of Interrupt
0	External event input has occurred.
1	A periodic output has occurred.
2	The time coincidence strobe has occurred.
3	A one second epoch (1pps output) has occurred.
4	An output FIFO data packet is available.

1.2 PHYSICAL AND FUNCTIONAL OVERVIEW

The bc620AT is a half length PC AT I/O expansion bus board. Operation is controlled via two 16 byte pages of 8 bit registers written and read by the host via the PCbus. The bc620AT occupies 16 bytes in the AT I/O address space. The I/O signals are accessible via two 15 pin "D" connectors mounted on the rear panel. The bc620AT is shown in Figure 1-1.

Figure 1-1
bc620AT Time and Frequency Processor



1.3 PERFORMANCE SPECIFICATIONS

1.3.1 TIME CODE READER

Format	IRIG A, and IRIG B. XR3, 2137; NASA36.
Carrier Range	+/- 50ppm.
Flywheel Accuracy	Drift < 2 millisecond per hour (applies to all operational modes).
Modulation Ratio	3:1 to 6:1.
Input Amplitude	0.5 to 5 volts peak-to-peak.
Input Impedance	10KΩ AC coupled.

1.3.2 TIME CODE GENERATOR

Format	IRIG B.
Modulation Ratio	3:1.
Output Amplitude	0 to 0 volts peak-to-peak.
Dc Level Shift	TTL/CMOS compatible.

1.3.3 BUS CHARACTERISTICS

Address Space	16 bytes in PC I/O Address Space (0x100 - 0x3FF).
Data Transfer	D08 (eight bit).
Interrupts	IRQ 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15 (jumper selectable).
Power	+5 @ 450 milliamperes -12 @ 20 milliamps. +12 @ 55 milliamps (250 milliamps - bc627AT).

1.3.4 DIGITAL INPUTS

Event Capture	TTL / CMOS positive or negative edge triggered.
	20 nanoseconds minimum width 250 nanoseconds min. period.
External 1pps	TTL / CMOS positive edge on time.
	20 nanoseconds minimum width.

1.3.5 DIGITAL OUTPUTS

1pps	TTL / CMOS positive edge on time (200 msec pulse width).
Periodics	TTL / CMOS positive edge on time (variable pulse width).
Strobe	TTL / CMOS positive edge on time (1 msec pulse width).
1, 5, 10 MHz Clock	TTL / CMOS positive edge on time.

1.3.6 EXTERNAL 10 MHz INPUT

Digital Input (or)	TTL / CMOS 45% to 55% duty cycle.
10MHz Input	1.5 to 4 volts peak-to-peak.

1.3.7 ENVIRONMENTAL SPECIFICATIONS

Temperature	Operating.	0^{o} to 70^{o} centigrade.
	Non-Operating.	-50^{o} to 125^{o} centigrade.
Relative Humidity	Operating.	5% to 95% non-condensing.
Altitude	Operating.	-400 to 18,000 meters MSL.

1.3.8 DIGITAL SYNCHRONIZATION SIGNALS

Format	DSS.
Signal	RS-422.
Communication	9600 bps, 8 bit, 1 stop bit, no parity.

CHAPTER TWO
INSTALLATION AND SETUP

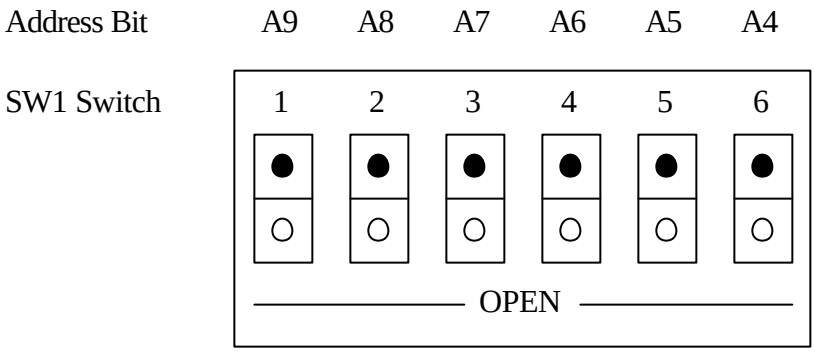
2.0 GENERAL

The bc620AT occupies 16 bytes in the AT I/O address space and the registers are eight bits wide. This section details the steps required to setup the module for operation.

2.1 BASE ADDRESS SELECTION

Before installing the module in the computer, the address select DIP switch (SW1) must be set. The bc620AT occupies 16 bytes in the PC I/O address space and can be freely located on any 16 byte boundary. The six DIP switch positions of SW1 correspond to address bits A9 - A4 as shown in Figure 2-1 and determine the modules base address. The base address is defined as the address selected by the SW1 DIP switch when A3 - A0 are 0.

Figure 2-1
DIP Switch SW1



To select a base address, set each of the 6 DIP switches to the ON (same as CLOSED), or OFF (same as OPEN) position. Setting a DIP switch to the ON position selects a logical zero for that address bit, and the OFF position selects a logical one.

In an AT computer, the base address can be set in the range of 100H - 3F0H. Setting a base address that is out of these ranges will probably prevent your computer from booting.

Example: To set the bc620AT base address to 0x300, set switches one and two to the OFF position and set switches three, four, five, and six to the ON position. Refer to Table 2-1 for a list of all the available base addresses in the PC bus and the corresponding switch settings.

Table 2-1
Section One
PC Bus Base Address Selection (SW1)

Base Addr	S1 A9	S2 A8	S3 S7	S4 A6	S5 A5	S6 A4	A3	A2	A1	A0
100H	ON	OFF	ON	ON	ON	ON	0	0	0	0
110H	ON	OFF	ON	ON	ON	OFF	0	0	0	0
120H	ON	OFF	ON	ON	OFF	ON	0	0	0	0
130H	ON	OFF	ON	ON	OFF	OFF	0	0	0	0
140H	ON	OFF	ON	OFF	ON	ON	0	0	0	0
150H	ON	OFF	ON	OFF	ON	OFF	0	0	0	0
160H	ON	OFF	ON	OFF	OFF	ON	0	0	0	0
170H	ON	OFF	ON	OFF	OFF	OFF	0	0	0	0
180H	ON	OFF	OFF	ON	ON	ON	0	0	0	0
190H	ON	OFF	OFF	ON	ON	OFF	0	0	0	0
1A0H	ON	OFF	OFF	ON	OFF	ON	0	0	0	0
1B0H	ON	OFF	OFF	ON	OFF	OFF	0	0	0	0
1C0H	ON	OFF	OFF	OFF	ON	ON	0	0	0	0
1D0H	ON	OFF	OFF	OFF	ON	OFF	0	0	0	0
1E0H	ON	OFF	OFF	OFF	OFF	ON	0	0	0	0
1F0H	ON	OFF	OFF	OFF	OFF	OFF	0	0	0	0

Table 2-1
Section Two
PC Bus Base Address Selection (SW1)

Base Addr	S1 A9	S2 A8	S3 S7	S4 A6	S5 A5	S6 A4	A3	A2	A1	A0
200H	OFF	ON	ON	ON	ON	ON	0	0	0	0
210H	OFF	ON	ON	ON	ON	OFF	0	0	0	0
220H	OFF	ON	ON	ON	OFF	ON	0	0	0	0
230H	OFF	ON	ON	ON	OFF	OFF	0	0	0	0
240H	OFF	ON	ON	OFF	ON	ON	0	0	0	0
250H	OFF	ON	ON	OFF	ON	OFF	0	0	0	0
260H	OFF	ON	ON	OFF	OFF	ON	0	0	0	0
270H	OFF	ON	ON	OFF	OFF	OFF	0	0	0	0
280H	OFF	ON	OFF	ON	ON	ON	0	0	0	0
290H	OFF	ON	OFF	ON	ON	OFF	0	0	0	0
2A0H	OFF	ON	OFF	ON	OFF	ON	0	0	0	0
2B0H	OFF	ON	OFF	ON	OFF	OFF	0	0	0	0
2C0H	OFF	ON	OFF	OFF	ON	ON	0	0	0	0
2D0H	OFF	ON	OFF	OFF	ON	OFF	0	0	0	0
2E0H	OFF	ON	OFF	OFF	OFF	ON	0	0	0	0
2F0H	OFF	ON	OFF	OFF	OFF	OFF	0	0	0	0

Table 2-1
Section Three
PC Bus Base Address Selection (SW1)

Base Addr	S1 A9	S2 A8	S3 S7	S4 A6	S5 A5	S6 A4	A3	A2	A1	A0
300H	OFF	OFF	ON	ON	ON	ON	0	0	0	0
310H	OFF	OFF	ON	ON	ON	OFF	0	0	0	0
320H	OFF	OFF	ON	ON	OFF	ON	0	0	0	0
330H	OFF	OFF	ON	ON	OFF	OFF	0	0	0	0
340H	OFF	OFF	ON	OFF	ON	ON	0	0	0	0
350H	OFF	OFF	ON	OFF	ON	OFF	0	0	0	0
360H	OFF	OFF	ON	OFF	OFF	ON	0	0	0	0
370H	OFF	OFF	ON	OFF	OFF	OFF	0	0	0	0
380H	OFF	OFF	OFF	ON	ON	ON	0	0	0	0
390H	OFF	OFF	OFF	ON	ON	OFF	0	0	0	0
3A0H	OFF	OFF	OFF	ON	OFF	ON	0	0	0	0
3B0H	OFF	OFF	OFF	ON	OFF	OFF	0	0	0	0
3C0H	OFF	OFF	OFF	OFF	ON	ON	0	0	0	0
3D0H	OFF	OFF	OFF	OFF	ON	OFF	0	0	0	0
3E0H	OFF	OFF	OFF	OFF	OFF	ON	0	0	0	0
3F0H	OFF	OFF	OFF	OFF	OFF	OFF	0	0	0	0

2.2 INSTALLATION PROCEDURE

To install the bc620AT module in your computer chassis:

- Remove the computer chassis cover.
- Select a vacant expansion slot and remove the blank rear panel bracket. Save the screw.
- Slide the bc620AT Module straight down to engage the motherboard connectors.
- Fasten the top of the bracket to the chassis using the screw that was saved from Step 2.
- Replace the chassis cover.

2.3 DEMONSTRATION PROGRAMS

The following demonstration program is provided with the bc620AT. A detailed explanation of the programs operation is included in the text file bc620.hlp. This file can be viewed by executing the README.EXE batch file.

bc620.c / bc620.exe

This program is written in Turbo C, and is intended to illustrate how to exercise the bc620 from a PC or compatible. Both the source code and an executable file have been provided. The modules base address is controlled by the value of the constant "base." Section 3.2.5 of the User's Guide describes the packet protocol used by this program. All the usual disclaimers concerning programming style and liability for use apply to this software.

2.4 MSDOS DEVICE DRIVER

bc620/627AT DOS Clock Device Driver v2.0
==========

A device driver is supplied with the bc620/627AT. This driver is intended to replace the PC real time clock in all aspects; time and date stamping of files, high level language calls, time and date requests from the DOS prompt, and any other applications which use the DOS clock (INT21 funcs 2A, 2B, 2C or 2D).

The driver is installed by adding a line to the config.sys file containing a device load statement. The following statement shows the syntax for the bc620 driver.

device=<path>bc620.sys {- / \}{AMOY}<switch data>

Note: If the path is not included, the system will search for the device driver in the root directory of the boot disk.

Also, there are three allowed switch delimiters: dash(-), slash(/) and the backslash(\).

The switch ids are defined as follows:

Axxx
Address
Three digits of hex base address

Allowed values: 100-3F0
Default: 300

Mx
Mode
One digit to select mode. If the board is not already in the requested mode the driver initialization routine will set the board to the requested mode.

Allowed values:
0 (IRIG Decoder Mode)
1 (Free Running Mode)
2 (External 1 PPS Mode)
3 (Battery Backed RTC Mode)
4 (GPS Mode [bc627AT only])
Default: doesn't change mode

Osxx
Offset
One digit of sign (optional) immediately followed by one or two digits of offset in hours from GMT.

Allowed values:
Sign "+" or "-"
hours 0-12
Default: 0

Yxx
Year
One or two digits of year information.

Allowed values: 91-10
Default: 94

Note: Year values less than ninety-one will be assumed to mean twenty-first century.

None of the switches are "required" and the switches may be added in any order. The user is free to set only those switches which are necessary for the particular implementation. Any switches not set will result in the default behavior noted above.

Some possible device load statements are shown and explained in the following section.

device=c:\bc620at\bc620.sys /A300 /M4 /Y94 /O-08

Description:

/A300	Sets the location where the driver will find the board to 300H.
/M4	Puts the board in GPS mode (if it is not already there).
/Y94	Sets the driver initial year to 1994.
/O-08	Sets the time returned by the driver to reflect 8 hrs behind GMT.

device=bc620.sys -A240 -Y01 -05

Description:

A240	Sets the location where the driver will find the board to 240H.
Y01	Sets the driver initial year value to 2001.
-05	Sets the time returned by the driver to reflect 5 hrs ahead of GMT.

device=bc620.sys \A310 \Y4 \O+03 \M2

Description:

\A310	Sets the location where the driver will find the board to 310H.
\Y4	Sets the driver initial year value to 2004.
\O+03	Sets the time returned by the driver to reflect 3 hrs ahead of GMT.
\M2	Puts the board in External 1 PPS mode (if it is not already there).

CHAPTER THREE
SOFTWARE INTERFACE

3.0 GENERAL

The bc620AT Time and Frequency Processor (TFP) occupies 16 bytes in the PC bus I/O address space. Refer to Chapter Two for details on base address selection. All TFP registers are eight bits wide. This chapter describes the TFP registers and their use.

3.0.1 GLOSSARY OF KEY TERMS

Epoch
A reference time or event. In timing applications "epoch" often refers to a one pulse per second event (1pps).

Flywheel
In the time keeping vernacular, to "flywheel" means to maintain time or frequency or both after the input reference is removed or lost.

Periodic
A programmable frequency which is obtained by dividing the TFP reference frequency. Periodics are sometimes referred to as "heartbeats." Periodics may optionally be synchronous with the 1pps epoch if the period is expressible as a ratio of integers.

Major Time
Units of time larger than or equal to seconds. A day hr:min:sec format is usually implied.

Minor Time
Subsecond time to whatever resolution is supported.

Packet
A group of bytes conforming to a defined structure. Packets are usually used in bit serial or byte serial data transmission to allow framing of the transmitted data.

3.1 REGISTERS

This section describes the registers used on the TFP for controlling its operation and transferring time data. Section 3.2 details the use of these registers. There are two 16-byte pages of registers on the TFP. The page select register determines the active page and is always accessible. The memory map for the TFP is listed in Table 3-1 and Table 3-2 (PAGE 1 registers). The first column of these tables shows the offset from the base address of each register. The second column (R/W) lists the access type of each register. These registers may be read only (R), write only (W), or read/write (R/W). In some cases, a read/write register is structured to support dissimilar data in the read and write directions. The contents of each register following a power-on or software reset is shown (RESET VALUE). A reset value of "---" indicates that the register contents are undefined. A label for each register is listed, as well as a brief description of the register's function.

3.1.1 PAGE SELECT REGISTER (PAGE 0/1)

The page select register is used to activate one of two 16-byte banks of registers. Bit 0 of PAGE selects PAGE 0 or PAGE 1, bits 1-7 are ignored during writes and undefined during reads. PAGE is always accessible.

3.1.2 TIMEREQ AND TIME0 - TIME7 REGISTERS (PAGE 0)

Reading the TIMEREQ register causes the current time (days - microseconds) and status to be loaded into a bank of registers, freezing the time at the instant the TIMEREQ register is accessed. Special circuitry prohibits the time from being latched while the time is changing. This circuitry is designed so that the TIME0 - TIME7 registers can be read immediately after a read of the TIMEREQ register without having to wait some predetermined amount of time (latency) for the time registers to become valid. This is referred to as zero latency time access.

A bank of 8 byte-wide registers (TIME0 - TIME7) holds the captured time and status. The time data is in a packed BCD format as shown in Table 3-3. The time is maintained in these registers until the TIMEREQ register is read again.

The status bits 4 - 6 of the TIME0 and EVENT0 register indicate the tracking status of the TFP with respect to the selected time source.

Bit 4: 0 = Reference time source present (i.e. time code, external 1pps, etc.).
1 = Flywheeling (i.e. time source lost)

Bit 5: 0 = Synchronized to within +/- X microseconds of time source
1 = Not synchronized to within +/- X microseconds of time source
(X = 5 for Mode 0 X = 2 for all other Modes)

Bit 6: 0 = Frequency stability <= 5 parts in 10EX relative to time source
1 = Frequency stability > 5 parts in 10EX relative to time source
(X=7 for Mode 0 X=8 for all other Modes)

Bit 7: Currently unused

A second independent one-hundred nanosecond bus time request is supported with the UNLOCK and EVENT0 - EVENT8 registers. See sections 3.1.4 and 3.1.5.

Note: Register bits which are designated as “unused” are ignored during writes and undefined during reads. For software compatibility with future versions of the TFP, which may use some of the “unused” bits, write zero's to these bits and ignore them during reads.

Table 3-1
bc620AT Page 0 Register Map

Offset Hex	R/W	Reset Value	Label	Description
0	R	---	TIMEREQ	Time Request.
1	R	0	TIME 0	Time Byte 0 (Status, DH).
2	R	0	TIME 1	Time Byte 1 (DT, DU).
3	R	0	TIME 2	Time Byte 2 (HT, HU).
4	R	0	TIME 3	Time Byte 3 (MT, MU).
5	R	0	TIME 4	Time Byte 4 (ST, SU).
6	R	0	TIME 5	Time Byte 5 (MSH, MST).
7	R	0	TIME 6	Time Byte 6 (MSU, USH).
8	R	0	TIME 7	Time Byte 7 (UST, USU).
9	--	---	---	Not Used.
A	--	---	---	Not Used.
B	--	---	---	Not Used.
C	--	---	---	Not Used.
D	--	---	---	Not Used.
E	--	---	---	Not Used.
F	R/W	0	PAGE	Page Select.

Table 3-2
bc620AT Page 1 Register

Offset Hex	R/W	Reset Value	Label	Description
0	R	0	CR0	Control Register 0.
1	R	0	EVENT 0	Event Time 0 (Status, DH).
2	R	0	EVENT 1	Event Time 1 (DT, DU).
3	R	0	EVENT 2	Event Time 2 (HT, HU).
3	W	0	STROBE 2	Strobe Time 2 (HT, HU).
4	R	0	EVENT 3	Event Time 3 (MT, MU).
4	W	0	STROBE 3	Strobe Time 3 (MT, MU).
5	R	0	EVENT 4	Event Time 4 (ST, SU).
5	W	0	STROBE 4	Strobe Time 4 (ST, SU).
6	R	0	EVENT 5	Event Time 5 (MSH, MST).
6	W	0	STROBE 5	Strobe Time 5 (MSH, MST).
7	R	0	EVENT 6	Event Time 6 (MSU, USH).
7	W	0	STROBE 6	Strobe Time 6 (MSU, XX).
8	R	0	EVENT 7	Event Time 7 (UST, USU).
9	R	0	EVENT 8	Event Time 8 (NSH, XX).
A	R/W	---	UNLOCK	Lockout Release / Capture Time.
B	R/W	0	ACK	Data Acknowledge.
C	R/W	0	MASK	Interrupt Mask.
D	R/W	0	INTSTAT	Interrupt Status.
E	R/W	---	FIFO	FIFO Input / Output.
F	R/W	0	PAGE	Page Select.

Table 3-3
Time Data Format (Time, Event,

TIME REGS	Time Data (Packed BCD Format)	
	7 6 5 4	3 2 1 0
TIME0 EVENT0	Status Bits.	Days Hundreds.
TIME1 EVENT1	Days Tens.	Days Units.
TIME2 EVENT2 STROBE2	Hours Tens.	Hours Units.
TIME3 EVENT3 STROBE3	Minutes Tens.	Minutes Units.
TIME4 EVENT4 STROBE4	Seconds Tens.	Seconds Units.
TIME5 EVENT5 STROBE5	Milliseconds Hundreds.	Milliseconds Tens.
TIME6 EVENT6 STROBE6	Milliseconds Units.	Microseconds Hundreds (not used for STROBE6).
TIME7 EVENT7	Microseconds Tens.	Microseconds Units.
EVENT8	Nanoseconds Hundreds.	Undefined.

Table 3-4
CR0 Control Register

Bit	Name	Function
0	LOCKEN	Capture Lockout Enable. 0 = Disable. 1 = Enable.
1	HBEN	Periodic Time Capture Enable. 0 = Disable. 1 = Enable.
2	EVSENSE	Event Input Active Edge Select. 0 = Rising edge. 1 = Falling edge.
3	EVENTEN	Event Input Time Capture Enable. 0 = Disable. 1 = Enable.
4	STREN	Time Coincidence Strobe Output Enable. 0 = Disable. 1 = Enable.
5	STRMODE	Time Coincidence Strobe Mode Select. 0 = Major/Minor. 1 = Minor Only.
6	FREQSEL0	Output Clock Frequency Select. 00 = 10 MHz. 01 = 5 MHz. 1X = 1 MHz. X = don't care.
7	FREQSEL1	

3.1.3 CR0 CONTROL REGISTER 0 (PAGE 1)

CR0 controls various functions on the TFP; event time capture, periodic time capture, time capture lockout, event input sense, strobe output, strobe mode, clock frequency output. Table 3-4 summarizes the function of each bit in CR0. Each bit is described below.

LOCKEN
Enables/disables the time capture lockout feature.

HBEN
Enables/disables time capture by the periodic heartbeat pulse generated by the TFP.

EVSENSE
Selects the active edge for the external event input signal.

EVENTEN
Enables/disables time capture by the external event input signal.

STREN
Enables/disables the time coincidence strobe output. When disabled, the strobe output is always low.

STRMODE
Selects the mode of operation for the time coincidence strobe. "Major/Minor" mode generates an output pulse when both the major time (hours - seconds) and the minor time (milliseconds) match the programmed strobe time (STROBE2 - STROBE6). "Minor Only" mode generates an output pulse when the minor time matches the programmed strobe time (i.e. once per second).

FREQSEL0,1
Selects one of three clock output frequencies. The output frequency is either 1, 5, or 10 MHz.

3.1.4 EVENT0 - EVENT8 TIME CAPTURE REGISTERS (PAGE 1)

The EVENT0 - EVENT8 registers hold time which has been captured in response to the active edge of the external event input the programmable periodic output, or a bus time request accomplished by writing to the UNLOCK register. Time is captured only when the capture sources (i.e. external event or periodic) are enabled with Bits 1 and 3 of CR0. This set of time capture registers is completely separate from the TIME0 - TIME7 registers on page 0. Time is captured to a resolution of 100 nanoseconds. The time capture lockout feature prevents the EVENT0 - EVENT8 registers from being overwritten with a new time before they can be read (See Section 3.2.3.3). Table 3-3 shows the time data format for these registers.

3.1.5 UNLOCK REGISTER (PAGE 1)

To release the time capture lockout mechanism, the UNLOCK register is read. The data read from UNLOCK is undefined.

A write to the UNLOCK register latches time in the EVENT0 - EVENT8 registers. The data written to the UNLOCK register is insignificant. This feature allows two independent times to be captured via the PCbus by the host CPU

3.1.6 ACK REGISTER (PAGE 1)

The ACK data acknowledge register provides a means for acknowledging a data transfer to/from the TFP via the FIFO interface, provides a mechanism for clearing the output FIFO and provides a 1pps flag bit. Table 3-5 summarizes the function of each bit in the ACK register.

FIFO RX (Bit 0)
The 620AT acknowledges receipt of a valid input FIFO data packet by setting this bit. The user is responsible for clearing the bit before instructing the TFP to take action on the FIFO data. (Refer to bit 7).

1pps (Bit 1)
This bit is set by the TFP once each second with the rising edge of the on-time 1pps output pulse. The user is responsible for clearing the bit.

FIFO RDY (Bit 2)
The 620AT sets this bit when an output FIFO data packet is ready to be read by the host.

EF/CLR FIFO (Bit 4)
A read of this bit returns the output FIFO empty flag status. When reading data from the FIFO this bit is monitored to insure all the FIFO data is read. The bit is clear (zero) when the FIFO is empty.

Writing a one to this register bit clears the output FIFO of all data and sets the empty flag to zero.

FIFO PACKET RDY (Bit 7)
Writing a one to this bit causes the TFP to take action on the input FIFO packet data.

Note: Acknowledge register bits 0, 1, 2 are cleared by writing a one to that bit location. For example, writing the value 0x01 to ACK will clear bit 0 and leave bit 1 unaltered. Writing the value 0x03 to ACK will clear both bit 0 and bit 1.

Table 3-5
ACK Acknowledge Register

bit#	CONTROL	FUNCTION (SET = "1" = high voltage CLEAR = "0" = low voltage).
0	TFP **HOST**	SETS bit to acknowledge the receipt of a valid input packet from host. **CLEARS bit by writing to this register with bit 0 SET.**
1	Reserved.	
2	TFP **HOST**	SETS bit when output FIFO contains a data packet. **CLEARS bit by writing to this register with bit 2 SET.** **This bit can generate an interrupt. (See Section 3.1.7.)**
3	Reserved.	
4	TFP **HOST**	SETS bit if output FIFO contains data. CLEARS bit if output FIFO empty. **CLEARS output FIFO by writing to this register with bit 4 SET.**
5	Reserved.	
6	Reserved.	
7	**HOST**	**Must write to this register with bit 7 SET to cause TFP to take action on the data packet previously written to the input FIFO.**

3.1.7 MASK INTERRUPT MASK REGISTER (PAGE 1)

The TFP supports five sources of interrupts as listed in Table 3-6. The MASK register is used to enable the interrupt source to generate a PCbus interrupt. When the interrupt source is enabled a PCbus interrupt will be generated any time the corresponding interrupt status bit (INTSTAT) transitions from a 0 to 1. A 1 enables the interrupt source, and a 0 disables it. Bit 0 corresponds to interrupt source 0, bit 1 to interrupt source 1, etc. Only bits 0 - 4 are used, bits 5 - 7 are ignored during writes and undefined during reads. The interrupt level select jumper (JP1) must be installed before an interrupt can be generated by the TFP to the desired IRQ. See Table 6-2 for the proper JP1 setting.

Note: After programming the MASK register, it is normal programming practice to clear the respective INTSTAT bit to arm the interrupt. Interrupts will not occur unless the INTSTAT bit transitions from a 0 to a 1 while the respective MASK bit is set.

3.1.8 INTSTAT INTERRUPT STATUS REGISTER (PAGE 1)

Each of the five interrupt sources will set the corresponding INTSTAT register bit to 1 when activated. The INTSTAT bits will be set even if the corresponding MASK bit is cleared. The INTSTAT register allows polling of the interrupt sources and notifies the user about which interrupt source(s) generated the PC interrupt. INTSTAT bits 0 - 4 are cleared by writing to the INTSTAT register with the corresponding bit(s) set. Only bits 0 - 4 are used, bits 5 - 7 are ignored during writes and undefined during reads. This register is mapped identically to the MASK register.

Table 3-6
bc620AT Interrupt MASK/INTSTAT Register Bit Map

Bit #	Int #	Source Of Interrupt
0	0	External event input has occurred.
1	1	Periodic pulse output has occurred.
2	2	Time coincidence strobe has occurred.
3	3	The one pulse per second (1pps) output has occurred.
4	4	A data packet is available in the output FIFO.

3.1.9 FIFO REGISTER (PAGE 1)

The TFP uses two FIFO (First-In First-Out) buffers; one to hold data packets written to the TFP for setting time, setting the programmable periodic rate, etc. (Input FIFO); and one to hold data packets from the TFP (Output FIFO). Each FIFO holds up to 512 bytes of data.

3.1.10 STROBE2 - STROBE6 TIME COINCIDENT STROBE REGISTERS (PAGE 1)

STROBE2 - STROBE6 registers hold the time coincidence strobe time from hours through milliseconds. Table 3-3 shows the time data format for these registers.

3.2 FUNCTIONAL DESCRIPTION

This section provides a description of how to use these registers to achieve the desired function.

3.2.1 CHANGING THE ACTIVE PAGE

To access the page 0 registers write 0x00 to PAGE. To access the page one registers write 0x01 to PAGE. The respective PAGE registers will be active until the PAGE register is changed.

3.2.2 READING TIME ON DEMAND

A read of the TIMEREQ register will latch the current time (days through microseconds), and this time will remain in the TIME0 - TIME7 registers until a subsequent read of TIMEREQ. The TIME0 - TIME7 registers can be read immediately after reading TIMEREQ.

A second bus time request is supported with the EVENT time capture registers. A write to the UNLOCK register latches time (days through 0.1 microseconds) in the EVENT0 - EVENT8 registers. The EVENT0 - EVENT8 registers can be read immediately after writing the UNLOCK register.

3.2.3 EVENT TIME CAPTURE

The EVENT0 - EVENT8 registers are used to hold time which has been captured in response to the active edge of the external event input, the programmable periodic output, or a write to the UNLOCK register. As with the TIME0 - TIME7 registers, the EVENT0 - EVENT8 registers can be read immediately after the event has occurred.

3.2.3.1 EXTERNAL EVENT INPUT

The external event input provides a means of capturing time based on an event that occurs externally to the TFP. Use the EVENTEN bit (CR0 bit 3) to enable the external event time capture. Use the EVSENSE bit (CR0 bit 2) to select the active edge. When the active edge of the external event input occurs, INTSTAT bit 0 will be set, and if MASK bit 0 is set a PC AT bus interrupt will be generated.

3.2.3.2 PROGRAMMABLE PERIODIC OUTPUT

The programmable periodic output will capture time in the EVENT0 - EVENT8 registers if the HBEN bit (CR0 bit 0) is set to 1. When the rising edge of the periodic output occurs, INTSTAT bit 1 will be set, and if MASK bit 1 is set a PC AT bus interrupt will be generated. The periodic output rate is programmable over the range from 2.5 MHz to 2.3 MHz.

3.2.3.3 TIME CAPTURE LOCKOUT

Time capture lockout is used with the event capture registers to prevent them from being overwritten before they can be read. The lockout (if enabled) will allow a capture signal (external event or periodic) to capture time once, then subsequent capture signals will be blocked until the lockout is released. The lockout is released by reading the UNLOCK register. The time capture lockout feature is enabled with LOCKEN (CR0 bit 0).

A write instruction to the UNLOCK register will latch time in the EVENT0 - EVENT8 registers.

3.2.4 TIME COINCIDENCE STROBE OUTPUT

The TFP provides a time coincidence strobe output which generates a one millisecond wide pulse (rising edge on time) at the time set in the STROBE2 - STROBE6 registers. Use STREN (CR0 bit 4) to enable/disable the strobe output pulse. When changing the STROBE2 - STROBE6 registers, the strobe output should be disabled to prevent false strobe outputs. The strobe can be operated in one of two modes: “major/minor” mode or “minor only” mode. In major/minor mode, the strobe output pulse occurs when the time matches both the programmed major time (hours - seconds) and the programmed minor time (milliseconds). In minor only mode, the strobe output pulse occurs once per second when the time matches the programmed minor time. The rising edge of the strobe will set INTSTAT bit 2, and if MASK bit 2 is set a PC, AT bus interrupt will be generated.

3.2.5 FIFO INTERFACE - PROGRAMMING THE BC620AT

Reads cycles take data from the output FIFO. Writes cycles place data into the input FIFO. Both the input FIFO and the output FIFO may be accessed at offset 0x0E of register PAGE 1. Each FIFO has a depth of 512 bytes.

Data must be written to and read from the FIFO in the following data packet format:

byte 1	0x01 header byte (ASCII SOH).
byte 2	"A" through "Z" idbyte.
byte 3	Data always ASCII (i.e. 0 = 0x30).
byte 4	Data.
.	.
.	. The number of data bytes varies.
byte N	Data.
byte N+1	0x17 tail byte (ASCII ETB).

See Chapter Four for a description of the available FIFO data packets and programming protocol.

3.3 PC AT INTERRUPTS

The TFP supports the five interrupt sources listed in Table 3-6. Interrupts are maskable with the MASK register. When multiple interrupt sources are enabled in the MASK register, the interrupt service routine can read the INTSTAT register to determine which interrupt source(s) caused the interrupt. Interrupt source activity can be polled by disabling interrupts (MASK register = 0) and then reading the INTSTAT register to determine when an interrupt signal is activated. The interrupt jumper JP1 on the TFP allows interrupt level selection. The TFP supports interrupt levels IRQ3-7, IRQ9-12, and IRQ14-15.

CHAPTER FOUR
FIFO DATA PACKETS

4.0 GENERAL

Communication with the bc620AT Time and Frequency Processor (TFP) is performed using byte serial data packet protocol. The packet bytes are read from and written to the TFP using eight bit data transfers at offset 0x0E of PAGE1. Following is a description of the available TFP FIFO data packets and the programming protocol.

4.1 WRITING DATA PACKETS

The following steps should be followed when loading data packets to the TFP. Failure to perform one or more of these steps correctly is a common reason for customer support calls.

- Write the packet to the input FIFO.
- Clear bit zero of the ACK register by writing 0x01 to the ACK register.
- Inform the TFP that an input packet is available by writing 0x80 to the ACK register.
- The TFP will set bit zero of the ACK register when the packet is processed.

When the host sets bit 7 of the ACK register and an interrupt is generated to the TFP CPU, the TFP service routine performs minimalist packet integrity checking. The TFP checks that the first packet byte is 0x01 (ASCII SOH). If the SOH is found, the TFP loads FIFO data into an input buffer until a byte value of 0x17 (ASCII ETB) is found. The packet is then processed in accordance with the idbyte value. When processing is complete the TFP sets bit 1 of the ACK register, clears the input FIFO, and resumes its previous task. If an SOH is not the first packet byte or if more than 40 bytes are read before encountering an ETB or if the idbyte value is invalid, then TFP clears the FIFO, sets bits 1 of the ACK register, and resumes its previous task.

A demonstration program written in the "C" language is provided with the disk accompanying the TFP. This program demonstrates the use of the primary data packets described below.

4.1.1 PACKET "A" - SELECT OPERATIONAL MODE

This packet contains a single data byte defining the operational mode of the TFP. Five operational modes are supported, modes 0, 1, 2, 3, and 4 corresponding to ASCII data bytes "0," "1," ... "4."

MODE 0
TIME CODE DECODING MODE

The TFP uses an input time code as the timing reference. The following codes are supported (see packet "H"): IRIG A, and B; 2137, XR3; and NASA36. Both modulated carrier and DC level shift formats are supported (DC level shift is not supported for 2137 or XR3 codes). The TFP locks its crystal oscillator to the input code rate. The oscillator has a control range of +/- 30 PPM for the standard VCXO version, and ± 2 PPM for the optional oven (OCXO) version. If the input code is outside these limits the TFP will exhibit periodic slips (i.e., if the TFP reference deviates from the input source by more than ± 1 millisecond a forced jamsync is performed). If the input code is lost or removed the TFP will continue to "flywheel" at the last known code rate. Typical accuracy is less than five parts in 10E7 (two milliseconds of drift per hour).

MODE 1
FREE RUNNING MODE

This mode is virtually the same as mode 2. Without a 1pps input the TFP runs at the last known oscillator frequency. Major time can be set with the "B" packet. The TFP time base can be adjusted with packet "D."

MODE 2
EXTERNAL 1PPS MODE

The TFP synchronizes to the external 1pps input signal. Major time can be loaded with the "B" packet. The acquisition range is the same as described in mode 0.

MODE 2 is used when a primary time standard such as a GPS receiver is available. In this case the 1pps output of the standard is input to the TFP.

MODE 3
REAL TIME CLOCK MODE

The TFP synchronizes to a 1pps signal from the on-board real time clock (RTC) IC, and the major time is also derived from the clock IC. The RTC is battery backed. This mode is not recommended when using the oven oscillator because the accuracy of the RTC is not high enough to ensure that the oven will be able to track it with slippage. See Mode 0 description.

MODE 4
GPS MODE (bc627AT GPS Satellite Receiver)

This optional mode is discussed in the bc627AT GPS Satellite Receiver Addendum User's Guide.

The bc620.c file has an example function, mode(), which sets the TFP operational mode as described above.

4.1.2 PACKET "B" - SET MAJOR TIME

TFP Modes 1 and 2 require the major time to be input using this data packet. Modes 0, 3 and 4 acquire major time from their respective time sources. Set time in Mode 3 with Packet "L." Packet "B" can be used to load time in any mode when the TFP is flywheeling. The data field of this packet consists of nine ASCII time digits in the order of seconds through days as follows:

byte	1	SOH.
byte	2	"B."
byte	3	Seconds Units.
byte	4	Seconds Tens.
byte	5	Minutes Units.
byte	6	Minutes Tens.
byte	7	Hours Units.
byte	8	Hours Tens.
byte	9	Days Units (JAN 1 = DAY 001).
byte	10	Days Tens.
byte	11	Days Hundreds.
byte	12	ETB.

The following paragraphs are about timing. This information should be well understood to avoid problems loading the major time.

The TFP firmware partitions each one second epoch into 30 periods plus a fractional period. Each period is 65536 counts of a 2 MHz clock. If the 2 MHz clock was perfect and the one second epoch was perfect then the number of counts in the one second epoch would be exactly two million. There would be thirty periods plus a remainder of 33920 counts.

For now it is important to know that the bc620AT increments, and then transfers major time, from a software buffer to a set of hardware latches on the 29th period of the internal counter. The time loaded into the latches will be the major time used for the next one second epoch (i.e. the next 1pps pulse rising edge transfers the time loaded at the 29th period to a second set of latches that are used for the major time reference). This double buffering approach ensures that the major and minor times are completely coherent, and that no ambiguities occur during the 1pps transition. What does all this mean? When loading the major time observe the following rules:

- If time is loaded before 29/30 into the second then the loaded time should reference the current epoch. (Recall the bc620 increments major time before downloading to the hardware latches.)

- If time is loaded after 29/30 into the second then the loaded time should reference the following epoch.

- Avoid loading major time near 29/30 into the second for obvious reasons.

- The loaded time will not be output by the bc620 at the next 1pps on-time mark. So don't expect your download to be used before the appropriate 1pps occurs.

The bc620.c file has an example function, load_clock(), which sets the time as described above.

4.1.3 PACKET "C" - COMMAND INPUT

This packet allows the user to exercise some direct control of the bc620 firmware. Five commands are supported at this time. These are:

"1" WARMSTART - Perform a reset without variable initialization. (Defaults not loaded.)

"2" RESET - Same as power on reset.

"3" JAMSYNCH - Forces minor time to jam to zero on the next 1pps pulse.

"4" !JAMSYNCH - Disable any pending jamsynch.

"5" Sync RTC - Synchronizes the battery back RTC IC time to current TFP time.

Commands three and four are provided for advanced users who may need to exercise control over the normal flow of the bc620 firmware. Issuing a jam sync can be useful when using an external fixed oscillator that can not be disciplined. Command four has no known useful purpose. It was initially implemented during the TFP checkout phase and has not been removed.

The bc620.c file has an example function, command(), which downloads a command as described above.

4.1.4 PACKET "D" - LOAD THE D/A CONVERTER

The TFP disciplines a reference oscillator using a DC control voltage which is the buffered output of a 16 bit D/A converter. This voltage is routed to an on board 10 MHz VCXO and to pin#1 on rear panel connector J1 to discipline an external oscillator. The control equations are compatible with virtually any oscillator which has a positive voltage versus frequency control characteristic (increasing voltage = increasing frequency).

The TFP divides the reference frequency input (whether input from an external 10 MHz source or the on-board 10 MHz VCXO) to produce a 1pps pulse. This pulse is compared to the reference 1pps epoch which is derived from the selected time reference (i.e., time code, external 1pps etc.). The D/A voltage is adjusted to steer the 1pps derived from the voltage controlled oscillator into phase coherence with the reference 1pps.

Some users may wish to control the D/A converter directly. Packet "D" is provided for this purpose. The format is as follows:

byte	1	SOH.
byte	2	"D."
byte	3	ASCII "0" - "F" (bits 12 through 15)..
byte	4	ASCII "0" - "F" (bits 8 through 11).
byte	5	ASCII "0" - "F" (bits 4 through 7).
byte	6	ASCII "0" - "F" (bits 0 through 3).
byte	7	ETB.

The bc620 firmware routines which normally load the D/A (i.e. disciplining) must be disabled using the path packet "P" to prevent the bc620 from overwriting the data input with this packet ("D").

The bc620.c file has an example function, preset_DA( ), which presets the D/A as described above.

4.1.5 PACKET "F" - HEARTBEAT (PERIODICS) CONTROL

The programmable frequency output is a very powerful bc620AT feature. Feedback from the users of other board level products motivated the inclusion of a very comprehensive periodic programming capability. Rates from 2.5 MHz to 2.3 MHz are easily achieved.

The heartbeat engine of the bc620AT consists of two sections of an INTEL 82C54 programmable interval timer connected in a serial configuration and driven by the TFP 10 MHz reference. Glue logic in one of the logic cell arrays supports both synchronous (with the 1pps epoch) and asynchronous operation. It is helpful (although not essential) to read the INTEL data sheet on the 82C54. Packet "F" allows the user complete access to the serial counters using standard INTEL loading protocols.

Two counter modes are supported; 1pps synchronous and asynchronous. It is the responsibility of the user to select the appropriate mode. No error checking is performed by the bc620AT firmware. The synchronous mode should only be selected if the number of output counts per second is an integer. If the number of counts per second is not an integer then the asynchronous mode should be used. The number of counts per second is always of the following form:

N = (10,000,000) / (n1 * n2)

where: N = counts per second
n1 = Counter #1 divide
n2 = Counter #2 divide

The range of values for Counter #1 and #2 is mode dependent as follows.

Asynchronous Mode: 2 to 65535
Synchronous Mode: 3 to 65535

*** * * WARNING * * ***

Periodic heartbeat pulse/interrupt generation can *not* be guaranteed in synchronous mode when counter divide values of two are used.

The two modes of operation are accessed using standard INTEL mode identifiers. For synchronous operation the mode byte must be an ASCII "5." For asynchronous operation the mode byte must be an ASCII "2." The packet format is as follows:

byte	1	SOH.
byte	2	"F."
byte	3	ASCII "2" (asynch) or ASCII "5" (synch).
byte	4	ASCII "0" - "F" (n1 bits 12 through 15).
byte	5	ASCII "0" - "F" (n1 bits 8 through 11).
byte	6	ASCII "0" - "F" (n1 bits 4 through 7).
byte	7	ASCII "0" - "F" (n1 bits 0 through 3).
byte	8	ASCII "0" - "F" (n2 bits 12 through 15).
byte	9	ASCII "0" - "F" (n2 bits 8 through 11).
byte	10	ASCII "0" - "F" (n2 bits 4 through 7).
byte	11	ASCII "0" - "F" (n2 bits 0 through 3).
byte	12	ETB.

*** * * IMPORTANT * * ***

When Mode 5 is used, the value of n1 and n2 produced by the 82C54 hardware is n1+1 and n2+1. This is a result of the way INTEL designed the 82C54, and is unrelated to our design.

Example: It is desired to implement 10000 counts per second synchronous with the 1pps.

mode	= "5"	(synchronous)
n1+1	= 10	
n2+1	= 100	(10,000,000) / (10 * 100) = 10000

Other values of (n1+1) and (n2+1) could have been used.
For example, (n1+1) = 25 and (n2+1) = 40.

byte	1	SOH.
byte	2	"F."
byte	3	"5" (mode).
byte	4	"0."
byte	5	"0."
byte	6	"0."
byte	7	"9" (n1 = 9).
byte	8	"0."
byte	9	"0."
byte	10	"6."
byte	11	"3" (n2 = 99 = 0x63).
byte	12	ETB.

The bc620.c file has an example function, load_82C54( ), illustrating the use of this packet.

4.1.6 PACKET "G" - PROPAGATION DELAY OFFSET CONTROL

It is frequently desirable to be able to program an offset into the basic timekeeping functions, relative to the reference input. For example, if the reference input is IRIG B test range time, there may be a significant cable propagation delay between the IRIG B source and the bc620. This delay may be removed by simply advancing the bc620AT from the reference by the known delay. The offset is programmable in steps of one-hundred nanoseconds (7 digits plus the sign byte spans a one second range).

The packet format is as follows:

byte	1	SOH.
byte	2	“G.”
byte	3	ASCII “±” (advance/retard).
byte	4	ASCII “0” - ”9” (most significant digit).
.	.	
.	.	
byte	10	ASCII “0” - ”9” (least significant digit).
byte	11	ETB.

*** * * WARNING * * ***

If offsets larger than +/- 990 microseconds are used, then the TFP jamsynch feature must be turned off using packet “P.” The reason for this requirement is that under normal operation if a difference between the reference time and the TFP time is detected to be greater than +/- 1 millisecond the TFP time base is “jammed” to the reference time so that a lengthy steering process is avoided.

4.1.7 PACKET “H” - SET TIME CODE FORMAT FOR MODE 0

Packet “H” allows the host to select the format and modulation type. The packet format is as follows. The time code format and modulation values are maintained in battery backed RAM.

byte	1	SOH.
byte	2	“H.”
byte	3	Format.
byte	4	Modulation.
byte	5	ETB.

Format Choices

“A”	IRIG A.
“B”	IRIG B.
“C”	2137 (XR3 with 100 Hz symbol rate).
“N”	NASA36.
“X”	XR3 (25 Hz symbol rate).

Modulation Choices

"M" Amplitude modulated sinewave.
"D" Pulse code modulation (DC level shift).
DC level shift not is supported for 2137 and XR3 codes.

4.1.8 PACKET "I" - CLOCK SOURCE SELECT

Packet "I" is used to select the clock source for the TFP. The TFP uses a frequency of 10MHz for all timing functions. The 10MHz be may derived from the TFP VCXO or it may be supplied from an external oscillator via J1 pin#1. The packet format is as follows:

byte 1 SOH.
byte 2 "I."
byte 3 "E" or "I" External or Internal.
byte 4 ETB.

On power on the TFP always defaults to the internal oscillator selection.

4.1.9 PACKET "J" - SEND DATA TO THE GPS RECEIVER (bc627AT only)

The format and content variations are discussed in a separate User's Guide.

4.1.10 PACKET "K" - SELECT GENERATOR CODE

The time code generated by the TFP is selected by packet "K." Only two options are available as described below. The generator code type is maintained in battery backed RAM.

byte 1 SOH.
byte 2 "K."
byte 3 Code.
byte 4 ETB.

Code Options

"B" Generate IRIG B amplitude modulated and DC level shift.
"H" Generate IRIG H DC level shift only.

4.1.11 PACKET “L”' - SET REAL TIME CLOCK

This packet loads the battery backed real time clock IC which is used as the source of major time and 1pps epoch when mode 3 is selected. The format follows:

byte	1	SOH.
byte	2	“L.”
byte	3	Years Tens.
byte	4	Years Units.
byte	5	Months Tens.
byte	6	Months Units (January = month 1).
byte	7	Day of Month Tens.
byte	8	Day of Month Units.
byte	9	Hours Tens.
byte	10	Hours Units.
byte	11	Minutes Tens.
byte	12	Minutes Units.
byte	13	Seconds Tens.
byte	14	Seconds Units.
byte	15	ETB.

As usual all data is in the ASCII format. The TFP need not be in Mode 3 when packet “L”' is downloaded.

4.1.12 PACKET “M” - LOCAL TIME OFFSET SELECT (bc627AT GPS Mode 4 Only)

This packet allows time to be maintained with an hour offset. This situation usually arises when the source of time is in a UTC (Universal Time Coordinated) format and the local time is required from the TFP. The offset only applies to the hours digits. The format is as follows:

byte	1	SOH.
byte	2	“M.”
byte	3	Sign “+” or “-”.
byte	4	Hours Tens.
byte	5	Hours Units.
byte	6	ETB.

A positive sign is from the prime meridian heading East, and a negative sign is used from the prime meridian heading West. For example, Eastern Standard Time would be -05 relative to UTC.

4.1.13 PACKET "O" - REQUEST DATA FROM THE bc620AT

This packet is used to request data from the TFP which is not available via the register interfaces. It was added primarily to allow the user to verify the integrity of the programmed setup data. This packet has been created with a very extensible format, and additional data will be made available as customer needs and suggestions are addressed.

The TFP signals a packet ready condition by setting bit2 in the ACK register. It is the responsibility of the host to clear this bit by writing to the ACK register with bit2 set.

Note: The user is advised against repetitively issuing Packet "O" to the TFP. Processing overhead is introduced to the TFP on-board CPU which could momentarily disrupt time keeping.

The packet format follows:

REQUEST FORMAT

byte	1	SOH.
byte	2	"O" (Upper case letter).
byte	3	"0" or "1" or "2."
byte	4	ETB.

RESPONSE FORMAT "0" REQUEST RTC TIME (see Packet "L"')

byte	1	SOH.
byte	2	"o" (Lower case letter).
byte	3	"0" (ASCII zero).
byte	4	Years Tens.
byte	5	Years Units.
byte	6	Months Tens.
byte	7	Months Units.
byte	8	Day of Month Tens.
byte	9	Day of Month Units.
byte	10	Hours Tens.
byte	11	Hours Units.
byte	12	Minutes Tens.
byte	13	Minutes Units.
byte	14	Seconds Tens.
byte	15	Seconds Units.
byte	16	ETB.

RESPONSE FORMAT "1" REQUEST CURRENT D TO A VALUE
(See Packet "D")

byte 1 SOH.
byte 2 "o" (Lower case letter).
byte 3 "1."
byte 4 "0" - "F" bits 12-15.
byte 5 "0" - "F" bits 08-11.
byte 6 "0" - "F" bits 04-07.
byte 7 "0" - "F" bits 00-03.
byte 8 ETB.

RESPONSE FORMAT "2" REQUEST LEAP SECONDS
(currently GPS specific)

byte 1 SOH.
byte 2 "o" (Lower case letter).
byte 3 "2."
byte 4 Leap Second Tens.
byte 5 Leap Second Units.
byte 6 ETB

RESPONSE FORMAT "3" REQUEST PROGRAMMABLE DATA

byte	1	SOH.
byte	2	"o" (Lower case letter).
byte	3	"3."
byte	4	Mode (See Packet "A").
byte	5	Time Format (See Packet "H").
byte	6	Time Code Type.
byte	7	Generator Format (See Packet "K").
byte	8	Path Byte (High nibble) (See Packet "P").
byte	9	Path Byte (Low nibble).
byte	10	Local Time Offset (Sign) (See Packet "M").
byte	11	Local Time Offset (Hours Tens).
byte	12	Local Time Offset (Hours Units).
byte	13	Propagation Delay Offset (Sign) (See Packet "G").
byte	14	Propagation Delay Offset (Millisecond Hundreds).
byte	15	Propagation Delay Offset (Millisecond Tens).
byte	16	Propagation Delay Offset (Millisecond Units).
byte	17	Propagation Delay Offset (Microsecond Hundreds).
byte	18	Propagation Delay Offset (Microsecond Tens).
byte	19	Propagation Delay Offset (Microsecond Units).
byte	20	Propagation Delay Offset (Nanosecond Hundreds).
byte	21	Heartbeat Mode (See Packet "F").
byte	22	Heartbeat Cnt1 (Bits 12-15).
byte	23	Heartbeat Cnt1 (Bits 08-11).
byte	24	Heartbeat Cnt1 (Bits 04-07).
byte	25	Heartbeat Cnt1 (Bits 00-03).
byte	26	Heartbeat Cnt2 (Bits 12-15).
byte	27	Heartbeat Cnt2 (Bits 08-11).
byte	28	Heartbeat Cnt2 (Bits 04-07).
byte	29	Heartbeat Cnt2 (Bits 00-03).
byte	30	ETB.

RESPONSE FORMAT "4" REQUEST bc620AT MODEL & VERSION

byte	1	SOH.
byte	2	"o" (Lower case letter).
byte	3	"4"
byte	4	Model 1 ("b").
byte	5	Model 2 ("c").
byte	6	Model 3 ("6").
byte	7	Model 4 ("2").
byte	8	Model 5 ("0",'7').
byte	9	Model 6 ("A").
byte	10	Model 7 ("T").
byte	11	Model 8 ("-").
byte	12	Version 1 ("9").
byte	13	Version 2 ("5").
byte	14	Version 3 ("0").
byte	15	Version 4 ("0" to "9").
byte	16	Version 5 ("0" to "9").
byte	17	Version 6 ("0" to "9").
byte	18	Version 7 ("0" to "9").
byte	19	ETB.

RESPONSE FORMAT "5" REQUEST YEAR (currently bc627AT GPS specific)

byte	1	SOH
byte	2	"o" (lower case letter).
byte	3	"5."
byte	4	Year Thousands.
byte	5	Year Hundreds.
byte	6	Year Tens.
byte	7	Year Units.
byte	8	ETB.

4.1.14 PACKET "P" - PATH SELECTION

The term "path selection" might more appropriately be called switch selection or option control. The purpose of this packet is to create branch points in the bc620 firmware. The path packet contains two data bytes, each byte controls four switches, and each switch is assigned to a particular bit in the lower 4 bits of each byte. The upper four bits of each byte are set to 3. The default settings set all switches to 0 *except that* the diagnostics bit which is set to 1. The format is as follows:

byte	1	SOH.
byte	2	"P."
byte	3	Data A (see below).
byte	4	Data B (see below).
byte	5	ETB.

Data A:

Bit 0: 0 = disable FIFO echo 1 = enable FIFO echo.
Bit 1: 0 = UTC Time 1 = GPS Time <1>.
Bit 2: 0 = Dynamics Code to Static 1 = Dynamics Code to Non-static <2>.
Bit 3: 0 = Packed BCD Time Format 1 = long second format <3>.

<1> UTC time = GPS time - GPS leap seconds. GPS time does not use GPS leap seconds.

<2> Auto set of GPS dynamics code to Static by bc627AT after initialization to GPS. Allows accurate time keeping without a full position fix for stationary users.

<3> Major time over PCbus is binary seconds since Jan 6, 1980. Minor time remains in BCD format.

Note: Bits 1, 2 and 3 of data A apply to Mode 4 GPS only (bc627AT).

Data B:

Bit 0: 0 = diagnostics on. 1 = diagnostics off <4>.
Bit 1: 0 = leap year off. 1 = leap year on.
Bit 2: 0 = enable jamsynchs. 1 = disable jamsynchs.
Bit 3: 0 = enable disciplining. 1 = disable disciplining.

<4> Diagnostics feature deleted beginning with bc620AT Rev E hardware .

An example is provided in bc620.c. The example requires two hexadecimal digits to be entered to cover the range of possible values 0 to 255.

4.1.15 PACKET “Q”' - SET DISCIPLINING GAIN

This packet allows the gain and sense of the disciplining process to be set via the host bus. Originally this feature was used for Datum Inc developmental purposes, but it could be useful when attempting to discipline an external oscillator using the TFP. The format is as follows:

byte	1	SOH.
byte	2	“Q.”'
byte	3	“0” - “F” least significant nibble.
byte	4	“0” - “F” most significant nibble.
byte	5	sense “1” = positive (default) “0” = negative.
byte	6	ETB.

4.1.16 PACKET “R” - GENERATOR TIME OFFSET SELECT

This packet allows the time code generator output to be offset from the TFP time. This is useful, for example, when UTC time is maintained in the TFP but local time must be generated to other devices such as time displays. The offset only applies to the hours digits. The format is as follows:

byte	1	SOH.
byte	2	“R.”
byte	3	Sign “+” or “-”.
byte	4	Hours Tens.
byte	5	Hours Units.
byte	6	ETB.

CHAPTER FIVE
PROGRAMMING EXAMPLES

5.0 GENERAL

The example code fragments in this chapter are written in the "C" programming language. A system dependent base address (BASE) indicates a 16 byte page of memory used in the PC AT I/O address space as selected by the SW1 switch settings (SSS).

```
#define BASE        0xSSS
```

The following definitions pertain to FIFO data transfer:

```
#define SOH         0x01
#define ETB         0x17
```

The following general definitions also apply :

```
#define ACK         (BASE+0x0B)
#define CRO         (BASE+0x00)
#define EVENT0      (BASE+0x01)
#define INTSTAT     (BASE+0x0D)
#define FIFO        (BASE+0x0E)
#define PAGE        (BASE+0x0F)
#define TIME0       (BASE+0x01)
```

The following global variables are also declared and used throughout this chapter.

```
char     i, dummy, time[9];
```

5.1 READING TIME ON DEMAND

The following example reads the time from the TFP registers TIME0 thru TIME7 and loads this data into the array time[ ]. Note that the time is latched by reading the TIMEREQ register, and that the register is assigned to a global variable. In most cases assignment to a global avoids the possibility that the dummy read operation will be removed by an optimizing compiler (beware).

```
outportb(PAGE,0x00);                          /* Access PAGE0  */
dummy = inportb(BASE+0x00);                   /* latch time */
for(i=0;i<8;i++) time[i]=inportb(TIME0+i);    /* read the time registers */
```

5.2 EXTERNAL EVENT TIME CAPTURE

This example sets up the TFP event capture to occur on a rising edge. The time capture lockout mechanism is also used.

/* Initialize TFP Event Hardware */

```
outportb(PAGE, 0x01);      /* Switch to PAGE1 */
outportb(CR0, 0x09);       /* enable event and lockout */
outportb(INTSTAT, 0x01);   /* clear event INTSTAT bit  */
```

/* Wait for Event and Process Data */

```
while(!(inportb(INTSTAT) & 0x01));     /* wait for event to occur    */
for(i=0; i<9; i++)                     /* read event time            */
   time[i] = inportb(EVENT0+i);
dummy = inportb(BASE+0x0A);            /* release capture lockout    */
outportb(INTSTAT, 0x01);               /* clear event INTSTAT bit    */
```

5.3 PROGRAM PERIODIC FREQUENCY OF 1000 Hz

This example uses a generalized send_packet( ) function to program a 1000 Hz output periodic synchronized to the TFP 1pps epoch.

```
void send_packet(char *charptr)
{
   outportb(FIFO, SOH );
   while(*charptr) outportb(FIFO, *charptr++ );    /* load body of packet
*/
   outportb(FIFO, ETB);
   outportb(ACK, 0x81);                /* command TFP & clear ACK */
   while(!(inportb(ACK) & 0x01));      /* wait for TFP acknowledge */
}
```

/* Code Fragment which sets Periodic */

```
send_packet("F500630063");       /* 0x0063 = 99 = (100-1) */
```

5.4 SET MODE 1 AND THE MAJOR TIME

This example selects the free running mode and sets the TFP major time using the “B” packet.

```
send_packet("A1");                     /* select mode 1 */
outportb(INTSTAT, 0x08);               /* clear INTSTAT 1 PPS bit */
while(!(inportb(INTSTAT) & 0x08));     /* wait for 1 PPS */
send_packet("B123112233");             /* set the days thru seconds */
```

5.5 SELECT MODE 0 (IRIG B) AND ADVANCE TFP 2.5 MILLISECONDS

The following code fragment selects the mode, time code, and offset. The last "P" packet is used to disable jamsynchs since the required offset is larger than 990 microseconds. See the "G" packet description for additional details on the jamsynch function.

```
send_packet("A0");              /* select mode 0 */
send_packet("HB");              /* select IRIG B time code */
send_packet("G+0025000");       /* advance 2.5 milliseconds */
send_packet("P04");             /* disable jamsynchs */
```

CHAPTER SIX

INPUT AND OUTPUT SIGNALS

6.0 GENERAL

This chapter describes the input/output connectors located on the bc620AT rear panel. The jumper options are also described.

6.1 CONNECTOR I/O

The bc620AT has two rear panel connectors, J1 and J2. J1 is a 15 pin DS type connector which carries most of the I/O signals. J2 is a high density DP type connector used for RS-422 serial I/O, and signal lines which accommodate an optional GPS signal suite for the bc627AT.

Table 6-1
J1 Pinouts

Signals On J1 15 Pin "DS"		Signals On J2 15 Pin "DP"	
Pin	**Signal**	**Pin**	**Signal**
1	External 10 MHz input.	1	RS-422 Rx(+).
2	Ground.	2	RS-422 Rx(-).
3	Strobe Output.	3	RS-422 Tx(+).
4	1pps Output.	4	RS-422 Tx(-).
5	Time Code Output (AM).	5	Ground.
6	External Event Input.	6	Not Used.
7	Time Code Input (AM).	7	GPS 1pps.
8	Ground (Recommended Time Code Return).	8	GPS 1pps RS-422 Rx(+).
9	Oscillator Control Output.	9	GPS 1pps RS-422 Rx(-).
10	Time Code Input (DCLS).	10	Ground.
11	Time Code Output (DCLS).	11	GPS RS-422 Tx(-).
12	Ground.	12	GPS RS-422 Tx(+).
13	1,5,10 MHz Output.	13	GPS +12 VDC.
14	External 1pps Input.	14	Ground.
15	Periodics Output.	15	GPS +12 VDC.

6.2 JUMPER SELECTIONS

Refer to Figure 1-1 to locate the Jumpers described below.

Table 6-2
JP1 Jumper Positions for PC AT Interrupt

JP1 Position	PC at Interrupt
1 to 2	IRQ15
3 to 4	IRQ14
5 to 6	IRQ12
7 to 8	IRQ11
9 to 10	IRQ10
11 to 12	IRQ9
13 to 14	IRQ7
15 to 16	IRQ6
17 to 18	IRQ5
19 to 20	IRQ4
21 to 22	IRQ3
* 22 to 23	No IRQ

Table 6-3
JP2 Jumper Positions for RS-422 RX 100 OHM Termination

JP2 Position	RS-422 Rx 100 W Termination
* 1 to 2	Terminated.
3 to 4	No Termination.

*Indicates factory default position.

CHAPTER SEVEN
ADJUSTMENTS

7.0 GENERAL

There are only two adjustments on the bc620AT module, RV1 and RV2. (See figure 1-1 for the location of these potentiometers.)

7.1 TIME CODE PHASE LOCK LOOP ADJUSTMENT

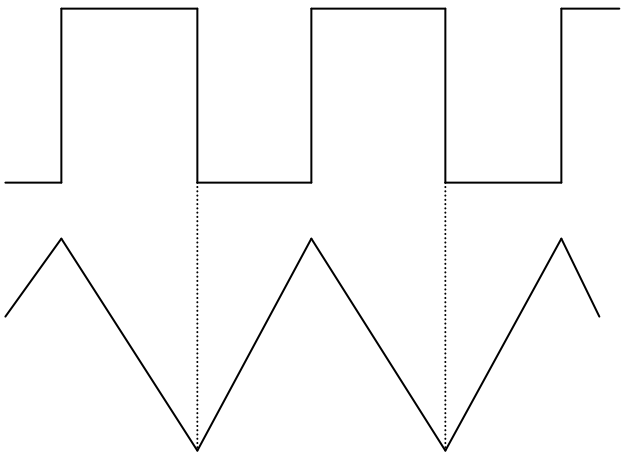
RV2 adjusts the center frequency of the VCO which locks to the carrier of a modulated input time code. This adjustment is made at the factory and rarely needs adjustment by the customer. This adjustment can be verified and adjusted correctly using a dual trace oscilloscope and a time code input.

- Set the bc620AT to Mode 0 (Packet "A") and select the appropriate time code format and modulation type (Packet "H").

- Connect channel #1 of the oscilloscope to pin #16 of U19 (XR2212). Connect channel #2 of the oscilloscope to the modulated input time code. Trigger the oscilloscope on the channel #1 input.

- Adjust RV2 so that the positive transition of the TTL signal input to channel #1 is centered on the positive crest of the input sine wave. The negative TTL transition should be centered on the most negative part of the input sine wave. See Figure 7-1 below.

Figure 7-1
Phase Lock Loop Adjustment



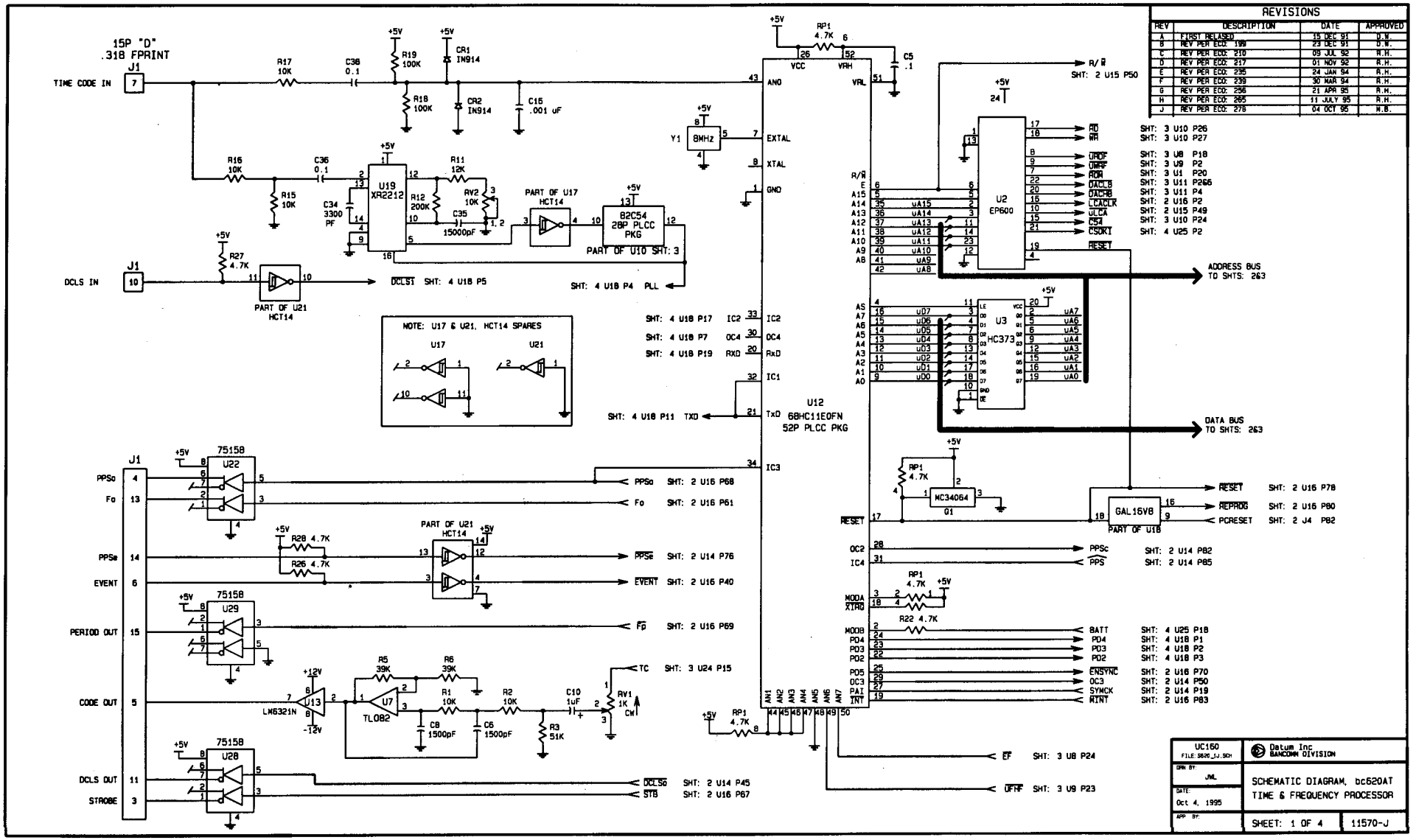
7.2 TIME CODE OUTPUT AMPLITUDE ADJUSTMENT

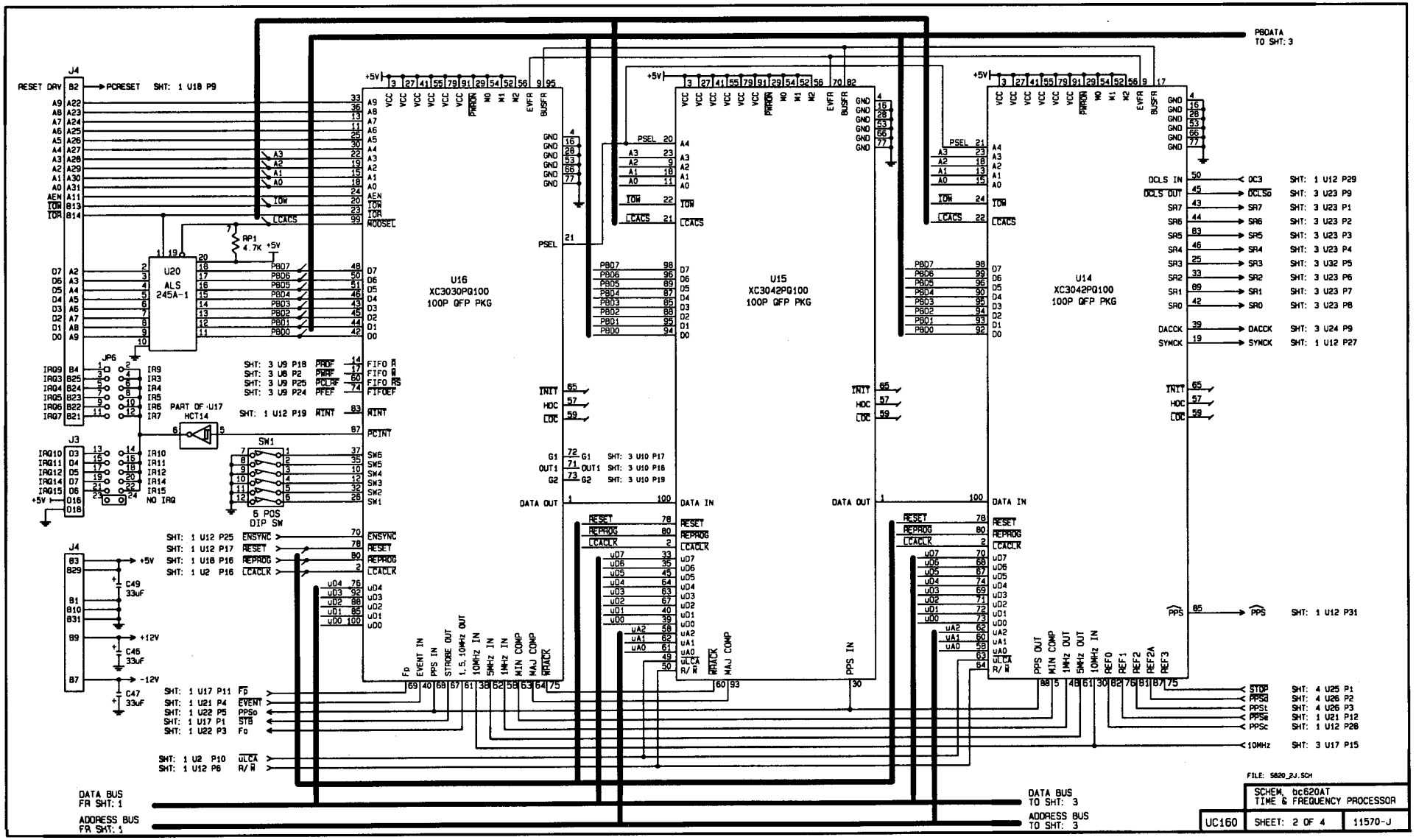
RV1 adjusts the amplitude of the modulated IRIG B output time code. A value of one volt RMS is common as is three volts peak-to-peak on the high cycles. Adjust this value to suit the equipment being driven. The range is zero to twenty-four volts peak-to-peak.

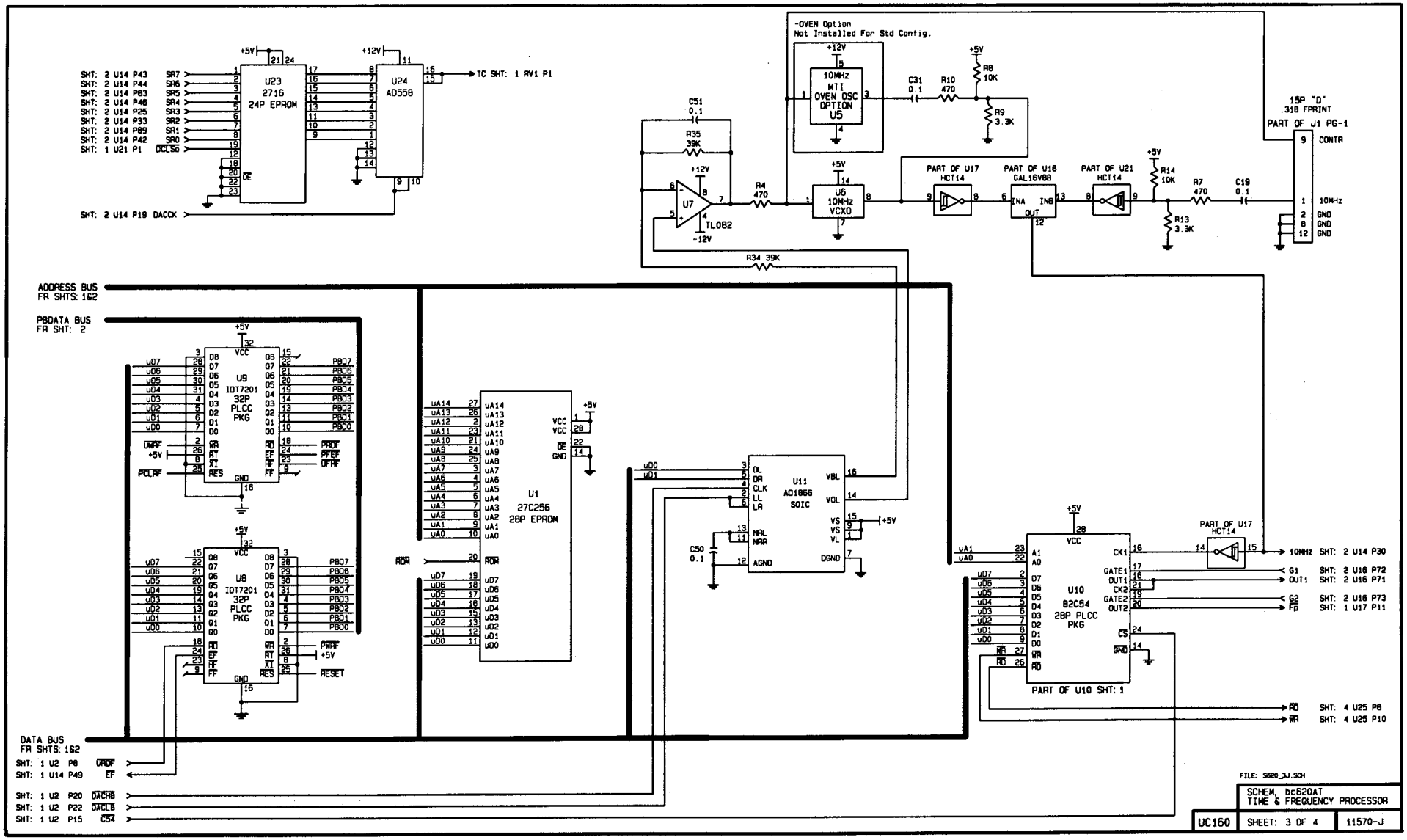
CHAPTER EIGHT
DRAWING SET

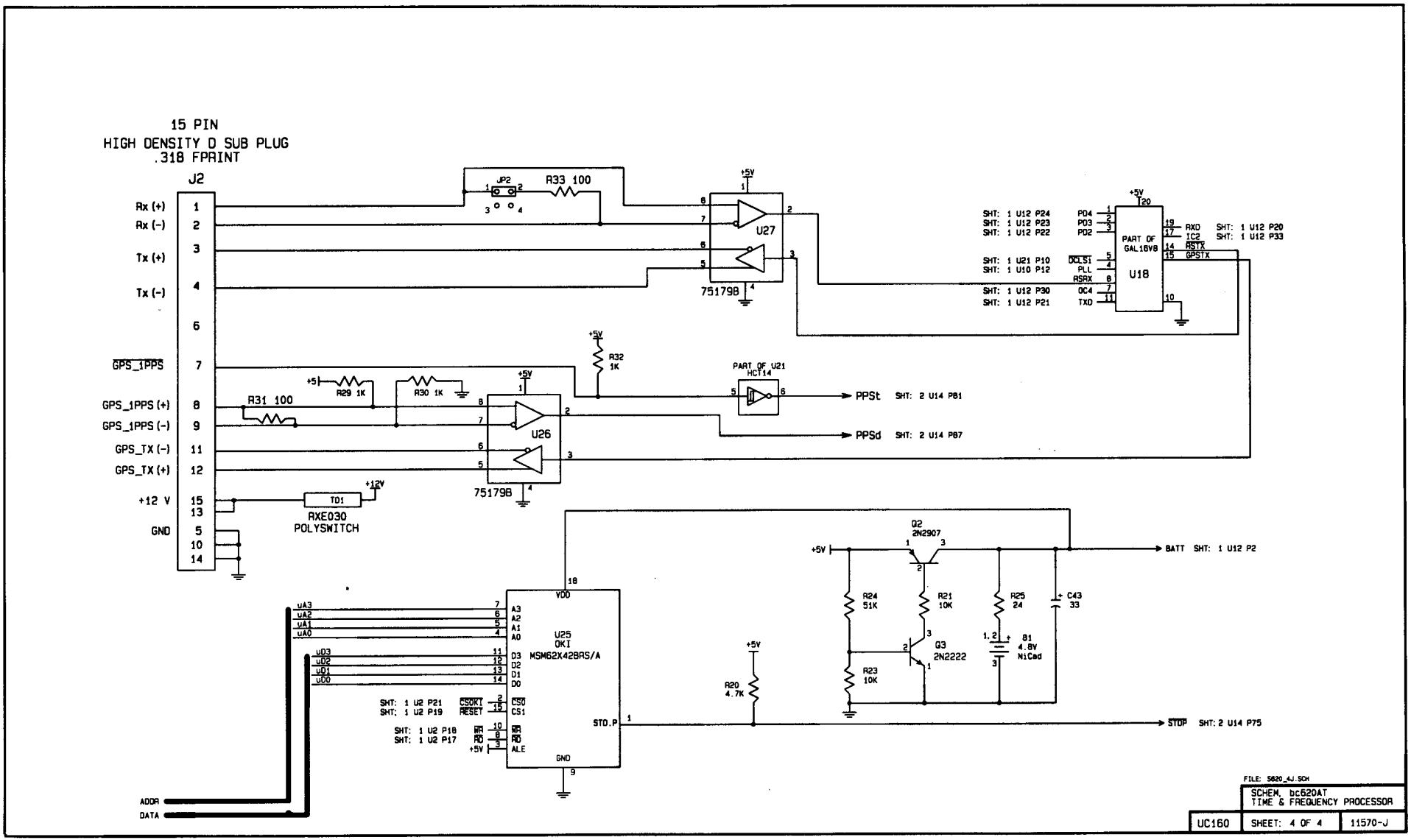
8.0 GENERAL

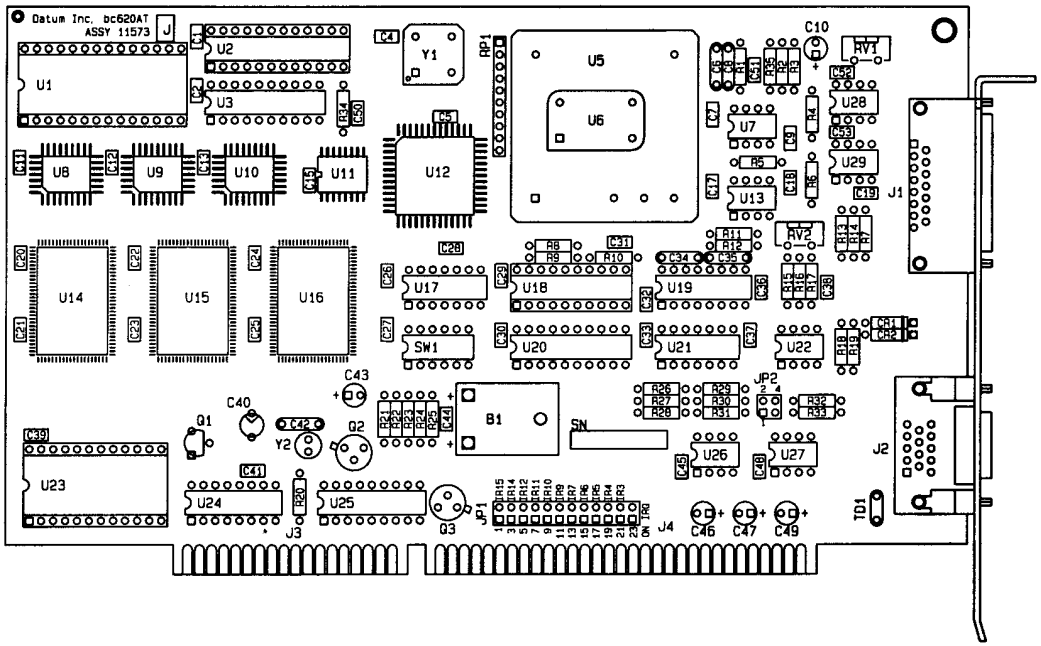
This chapter contains the schematic diagram, assembly drawing, and parts list for the bc620AT.


15P "D"
.318 FPRINT
J1
TIME CODE IN
DCLS IN
U12
68HC11E0FN
52P PLCC PKG
U2
EP600
U3
HC373
U19
XR2212
82C54
28P PLCC
PKG
PART OF U10 SHT: 3
U22
U29
U28
75158
U13
LM6321N
U7
TL082
Y1
8MHz
Q1
MC34064
GAL16V8
PART OF U18
NOTE: U17 & U21, HCT14 SPARES
U17
U21
ADDRESS BUS
TO SHTS: 2&3
DATA BUS
TO SHTS: 2&3
PPSo
Fo
PPSe
EVENT
PERIOD OUT
CODE OUT
DCLS OUT
STROBE
REVISIONS
REV
DESCRIPTION
DATE
APPROVED
A FIRST RELEASED 15 DEC 91 D.W.
B REV PER ECO: 199 23 DEC 91 D.W.
C REV PER ECO: 210 09 JUL 92 R.H.
D REV PER ECO: 217 01 NOV 92 R.H.
E REV PER ECO: 235 24 JAN 94 R.H.
F REV PER ECO: 239 30 MAR 94 R.H.
G REV PER ECO: 256 21 APR 95 R.H.
H REV PER ECO: 265 11 JULY 95 R.H.
J REV PER ECO: 278 04 OCT 95 N.B.
UC160
FILE: S620_JJ.SCH
Datum Inc
BANCOMM DIVISION
DRN BY: JML
DATE: Oct 4, 1995
APP BY:
SCHEMATIC DIAGRAM, bc620AT
TIME & FREQUENCY PROCESSOR
SHEET: 1 OF 4
11570-J


PBDATA
TO SHT: 3
RESET DRV
PCRESET
SHT: 1 U18 P9
U20
ALS
245A-1
RP1
4.7K
+5V
U16
XC3030PQ100
100P QFP PKG
U15
XC3042PQ100
100P QFP PKG
U14
XC3042PQ100
100P QFP PKG
PART OF U17
HCT14
SW1
6 POS
DIP SW
C49
33uF
C45
33uF
C47
33uF
+5V
+12V
-12V
DCLS IN
DCLS OUT
PPS
STOP
10MHz
DATA BUS
FR SHT: 1
ADDRESS BUS
FR SHT: 1
DATA BUS
TO SHT: 3
ADDRESS BUS
TO SHT: 3
FILE: S620_2J.SCH
SCHEM, bc620AT
TIME & FREQUENCY PROCESSOR
UC160
SHEET: 2 OF 4
11570-J


SHT: 2 U14 P43 SA7
SHT: 2 U14 P44 SA6
SHT: 2 U14 P83 SA5
SHT: 2 U14 P46 SA4
SHT: 2 U14 P25 SA3
SHT: 2 U14 P33 SA2
SHT: 2 U14 P89 SA1
SHT: 2 U14 P42 SA0
SHT: 1 U21 P1 DCLSG
U23
2716
24P EPROM
U24
AD558
TC SHT: 1 RV1 P1
SHT: 2 U14 P19 DACCK
-OVEN Option
Not Installed For Std Config.
10MHz
MTI
OVEN OSC
OPTION
U5
C31
0.1
R10
470
R8
10K
R9
3.3K
C51
0.1
R35
39K
U7
TL082
R4
470
U6
10MHz
VCXO
PART OF U17
HCT14
PART OF U18
GAL16V8B
PART OF U21
HCT14
R14
10K
R13
3.3K
R7
470
C19
0.1
15P "D"
.318 FPRINT
PART OF J1 PG-1
CONTR
10MHz
GND
GND
GND
R34 39K
ADDRESS BUS
FR SHTS: 1&2
PBDATA BUS
FR SHT: 2
U9
IDT7201
32P
PLCC
PKG
U8
IDT7201
32P
PLCC
PKG
PBD7
PBD6
PBD5
PBD4
PBD3
PBD2
PBD1
PBD0
PRDF
PFEF
OFRF
PWRF
RESET
U1
27C256
28P EPROM
U11
AD1868
SOIC
U10
82C54
28P PLCC
PKG
PART OF U10 SHT: 1
10MHz SHT: 2 U14 P30
G1 SHT: 2 U16 P72
OUT1 SHT: 2 U16 P71
G2 SHT: 2 U16 P73
Fo SHT: 1 U17 P11
RD SHT: 4 U25 P6
WR SHT: 4 U25 P10
DATA BUS
FR SHTS: 1&2
SHT: 1 U2 P8 ORDF
SHT: 1 U14 P49 EF
SHT: 1 U2 P20 DACHB
SHT: 1 U2 P22 DACLB
SHT: 1 U2 P15 C54
FILE: S620_3J.SCH
SCHEM, bc620AT
TIME & FREQUENCY PROCESSOR
UC160
SHEET: 3 OF 4
11570-J


15 PIN
HIGH DENSITY D SUB PLUG
.318 FPRINT
J2
Rx (+)
Rx (-)
Tx (+)
Tx (-)
GPS_1PPS
GPS_1PPS (+)
GPS_1PPS (-)
GPS_TX (-)
GPS_TX (+)
+12 V
GND
JP2
R33 100
U27
75179B
R32 1K
R31 100
R29 1K
R30 1K
U26
PART OF U21 HCT14
PPSt
PPSd
TD1
RXE030
POLYSWITCH
U18
PART OF GAL16V8
RXD
IC2
RSTX
GPSTX
U25
OKI
MSM62X428RS/A
STO.P
R20 4.7K
Q2 2N2907
Q3 2N2222
R24 51K
R21 10K
R23 10K
R25 24
C43 33
B1 4.8V NiCad
BATT
STOP
ADDR
DATA
SCHEM, bc620AT
TIME & FREQUENCY PROCESSOR
UC160
SHEET: 4 OF 4
11570-J



REVISIONS			
LTR	DESCRIPTION	DATE	APPVD
A	FIRST RELEASED	15 NOV 91	D.W.
B	REV PER ECO# 199	23 DEC 91	D.W.
C	REV PER ECO# 210	09 JUL 92	R.H.
D	REV PER ECO# 217	01 NOV 92	R.H.
E	REV PER ECO# 235	24 JAN 94	R.H.
F	REV PER ECO# 239	30 MAR 94	R.H.
G	REV PER ECO# 256	21 APR 95	R.H.
H	REV PER ECO# 265	11 JUL 95	R.H.
J	REV PER ECO# 278	04 OCT 95	M.B.

UC160 BCM0106H.ZIP FILE: A620_1J.SCH	Datum Inc BANCOMM DIVISION	
DRWN BY: JWL	ASSEMBLY, bc620AT	
DATE: 4 OCT 95	TIME & FREQUENCY PROCESSOR	
APP. BY:	SHEET: 1 OF 2	11573-J

Assembly, Parts Listing
bc620AT T&F Processor

Ref: Drawing No. 11573 J

Ref: UC 160

Oct 4, 1995

OPT	BC P/N	MANF P/N	MANUFACTURE	VALUE	DESCRIPTION	QTY#	REF DESIG.
	1419026	11575B	DATUM INC, BC	bc620AT	IBM PC BRKT	1.00	BKT1
	1503336	336RMR025M	IC	33 MF, 35V	ALUMINUM ELECTROLYTIC CAP.	4.00	C43,46,47,49
	1504105	196D105X9035HA1	SPRAGUE	1.0 MF, 35V	TANTALUM CAP, RADIAL LEADS	1.00	C10
	1506102	SR211C102KAA	AVX	1000 PF, 50V	MONO CERAMIC CAPACITOR .2 R/L	1.00	C16
	1506152	SR211C152KAA	AVX	1500 PF, 100V	MONO CERAMIC CAPACITOR .2 R/L	2.00	C6,8
	1506153	SR211C153KAA	AVX	15000 PF, 100V	MONO CERAMIC CAPACITOR .2 R/L	1.00	C35
	1506332	SR211C332KAA	AVX	3300 PF, 100V	MONO CERAMIC CAPACITOR .2 R/L	1.00	C34
	1514104	12065E104MAT050	AVX	0.1 MF, 50V	CERAMIC CHIP CAP	12.00	C36-39,41,44,45,48,50,51-53
	1514104	12065E104MAT050	AVX	0.1 MF, 50V	CERAMIC CHIP CAP	27.00	C1,2,4,5,7,9,11-13,15,17-33
	1701160	11572J	DATUM INC, BC	bc620AT	PRINTED CIRCUIT BOARD	1.00	PCB1
	2117061	TSW-130-07-G-D	SAMTEC	2X30 POS	STRAIGHT TERMINAL STRIP	1.00	JP1=2x12, JP2=2x2
	2124215	869521-1	AMP	15 POS	'D' SKT, .318 RTANG PCMNT B/L	1.00	J1
	2149024	824-AG31D	AUGAT	24 POS	SLIM DIP SOCKET	1.00	U2
	2150020	10620-01-445	ANDON/SPECTRA	20 POS	DIP SOCKET	1.00	U18
	2150024	10624-01-445	ANDON/SPECTRA	24 POS	DIP SOCKET	1.00	U23
	2150028	10628-01-445	ANDON/SPECTRA	28 POS	DIP SOCKET	1.00	U1
	2192015	749767-1	AMP	15 POS	.350 RTANG PCMNT B/L MALE	1.00	J2
	2306008	OECS-8O-2-A401A	ECS	8 MHz	HALF SIZE TTL/CMOS CLOCK OSC	1.00	Y1
	2802001	3341-1L	3M		JACK SCREW KIT	2.00	BKT1 J1,2
	3902001	PMB4.8-15-H3	PLAINVIEW INC.	4.8V	NICAD PCMNT BATTERY	1.00	B1
	4305030	RXE030	RAYCHEM		POLYSWITCH	1.00	TD1
	4701101	RC07GF101J	ALLEN BRADLEY	100 OHM, 1/4W	FIXED RESISTOR	2.00	R31,33
	4701102	RC07GF102J	ALLEN BRADLEY	1 K OHM, 1/4W	FIXED RESISTOR	3.00	R29,30,32
	4701103	RC07GF103J	ALLEN BRADLEY	10 K OHM, 1/4W	FIXED RESISTOR	9.00	R1,2,8,14,15-17,21,23
	4701104	RC07GF104J	ALLEN BRADLEY	100 K OHM, 1/4W	FIXED RESISTOR	2.00	R18,19
	4701123	RC07GF123J	ALLEN BRADLEY	12 K OHM, 1/4W	FIXED RESISTOR	1.00	R11
	4701204	RC07GF204J	ALLEN BRADLEY	200 K OHM, 1/4W	FIXED RESISTOR	1.00	R12
	4701240	RC07GF240J	ALLEN BRADLEY	24 OHM, 1/4W	FIXED RESISTOR	1.00	R25
	4701332	RC07GF332J	ALLEN BRADLEY	3.3 K OHM, 1/4W	FIXED RESISTOR	2.00	R9,13
	4701393	RC07GF393J	ALLEN BRADLEY	39 K OHM, 1/4W	FIXED RESISTOR	4.00	R5,6,34,35
	4701471	RC07GF471J	ALLEN BRADLEY	470 OHM, 1/4W	FIXED RESISTOR	3.00	R4,7,10
	4701472	RC07GF472J	ALLEN BRADLEY	4.7 K OHM, 1/4W	FIXED RESISTOR	5.00	R20,22,26-28
	4701513	RC07GF513J	ALLEN BRADLEY	51 K OHM, 1/4W	FIXED RESISTOR	2.00	R3,25
	4705472	710A472	ALLEN BRADLEY	4.7 K OHM, 1/8W	C-SIP RESISTORS, 10 PIN 'X'	1.00	RP1
	4709102	POT3104H-1-102K	MURATA	1 K OHM, 1/4W	SINGLE TURN POT PC MT VERTICAL	1.00	RV1
	4709103	POT3104H-1-103K	MURATA	10 K OHM, 1/4W	SINGLE TURN POT PC MT.VERTICAL	1.00	RV2
	4801002	2N2222			NPN SWITCHING/AMPLIFIER (TO18)	1.00	Q3
	4802002	2N2907A			PNP SWITCHING/AMPLIFIER (TO18)	1.00	Q2
	4803001	IN914			SILICON DIODE	2.00	CR1,2
	5108005	76SB06	GRAYHILL		6PST DIP SWITCH	1.00	SW1
	9002710	74HCT14	RCA	14P DIP PKG	HEX SCHMITT INVERTER	2.00	U17,21
	9008657	74HC373	VARIOUS	20P DIP PKG	OCTAL D TRANSPARENT LATCH, T/S	1.00	U3
	9102003	MC68HC11E0FN	MOTOROLA	52P PLCC PKG	MICROCOMPUTER	1.00	U12
	9103035	MSM62X42BRS/A	OKI	18P DIP PKG	REAL TIME CLOCK/CALENDER	1.00	U25
	9103040	82C54-2	INTEL	28P PLCC PKG	PROGRAMMABLE COUNTER TIMER	1.00	U10
	9201030	MC34064P-5	MOTOROLA	3P CASE29-04 P	UNDERVOLTAGE SENSING DEVICE	1.00	Q1
	9203005	AD558JN	ANALOG	16P DIP PKG	8 BIT DACPORT	1.00	U24
	9203040	AD1866R	ANALOG DEVICE	16P SOIC PKG	D/A CONVERTER	1.00	U11
	9207070	SN75158P	TI	08P DIP PKG	DUAL 50 OHM TTL LINE DRIVER	3.00	U22,28,29
	9207079	SN75179B	TI	08P DIP PKG	DIFF DRIVER/RECIVER PAIR	2.00	U26,27
	9207920	SN74ALS245A-1N	TI	20P DIP PKG	OCTAL BUS TRANSCEIVER	1.00	U20
	9306007	LM6321N	NATIONAL	08P DIP PKG	HIGH SPEED BUFFER	1.00	U13
	9306035	TL082	TI	08P DIP PKG	DUAL BIPOLAR JFET OP AMP	1.00	U7
	9307030	XR2212CP	EXAR	16P DIP PKG	PHASE LOCKED LOOP (COMMERICAL	1.00	U19
	9404010	IDT7201SA120J	IDT	32P PLCC PKG	FIFO 9 X 512	1.00	U8,9
	9405001	EP600PC-3	ALTERA	24P DIP PKG .3W	EPLD	1.00	REF U2 (SKT)
	9405059	XC3030-70PQ100C	XILINX	100P QFP PKG	PLD QUAD FLAT PKG	1.00	U16
	9405061	XC3042-70PQ100C	XILINX	100 QFP PKG	PLD QUAD FLAT PKG	2.00	U14,15
	9405063	GAL16V8B-25LP	LATTICE	20P DIP PKG	GAL-25NS	1.00	REF U18 (SKT)
	9406005	2716	VARIOUS	24P DIP PKG .6W	2 K X 8 UV ERASABLE PROM	1.00	REF U23 (SKT)
	9406040	27C256	VARIOUS	28P DIP PKG .6W	32K BYTE, CMOS EPROM	1.00	REF U1 (SKT)
ANT					bc627GPS ANTENNA OPTION		
ANT	2193015	HDT15-SD	A.T./SPRECTA	15 POS	HD D-SUB,SOLDER CUP FEMALE	1.00	EXT. ANT. CABLE
ANT	9700007	18636/19360-50	TRIMBLE NAV.	ANTENNA	TRIMBLE ACUTIME W/TSI & RS422	1.00	REMOTE ANTENNA
BNC					BNC CABLE OPTION		
BNC	2106001	31-317	AMPHENOL	50 OHM	BNC JACK, STRIGHT	4.00	EXT. CABLE PARTS
BNC	2123015	DA15P	CANNON	15 POS	'D' PLUG	1.00	EXT. CABLE PARTS
OVN					OVEN OSC OPTION		
OVN	2307001	240-0530AT	MTI	10MHz	OVEN OSC.	1.00	U5
00					STANDARD OSC. ASSEMBLY		
00	2305002	C0-401V-AX	VECTRON	10 MHz	VCXO	1.00	U6

APPENDIX A

IRIG TIME CODE FORMAT

A.0 GENERAL

The widespread use of coded timing signals to assist in the correlation of intercept and test data began in the early 1950's. These signals can be decoded in real time to indicate the current Time of Day (TOD) or recorded along with intercept/test data on magnetic tape recorders for post processing and time correlation.

Hundreds of time code formats were developed - one for each agency involved. During the early 1960's the InterRange Instrumentation Group (IRIG) promoted a series of "standard" time code formats now loosely referred to as "IRIG Time Codes." The bc620AT decodes the most widely used format, IRIG B, as well as IRIG A. Figure A-1 illustrates a frame of IRIG time code.

Figure A-1
IRIG Time Code Frame

IRIG B Time Code Frame

Symbols:

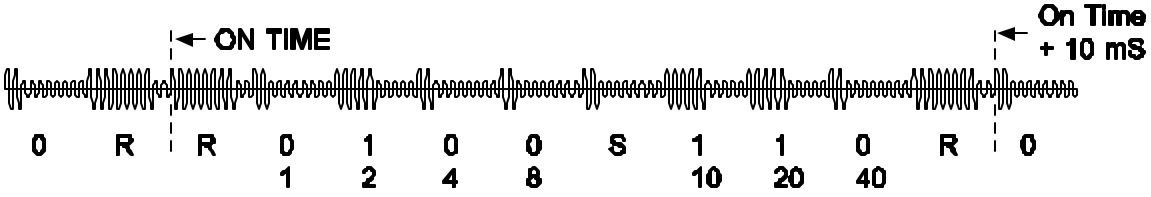
Reference Mark: 8 HC, 2 LC

Logical '1': 5 HC, 2 LC

Logical '0' or Space: 2 HC, 8 LC

10 Cycles or 10 milliseconds for IRIG B or IEEE1344

On Time and First Sub Frame:



A double reference mark denotes the start of the frame, 'On Time'. Encoded BCD data is the time at On Time. The encoded data is this first subframe is 32 Seconds.

Frame:

IRIG B:

OT
R R SS R MM R HH R DD R D _ R C C R C C R C C R B B R B B R
Seconds
Minutes
Hours
Days
Control Characters
Control Characters
Control Characters
17 BIT BINARY
TOD