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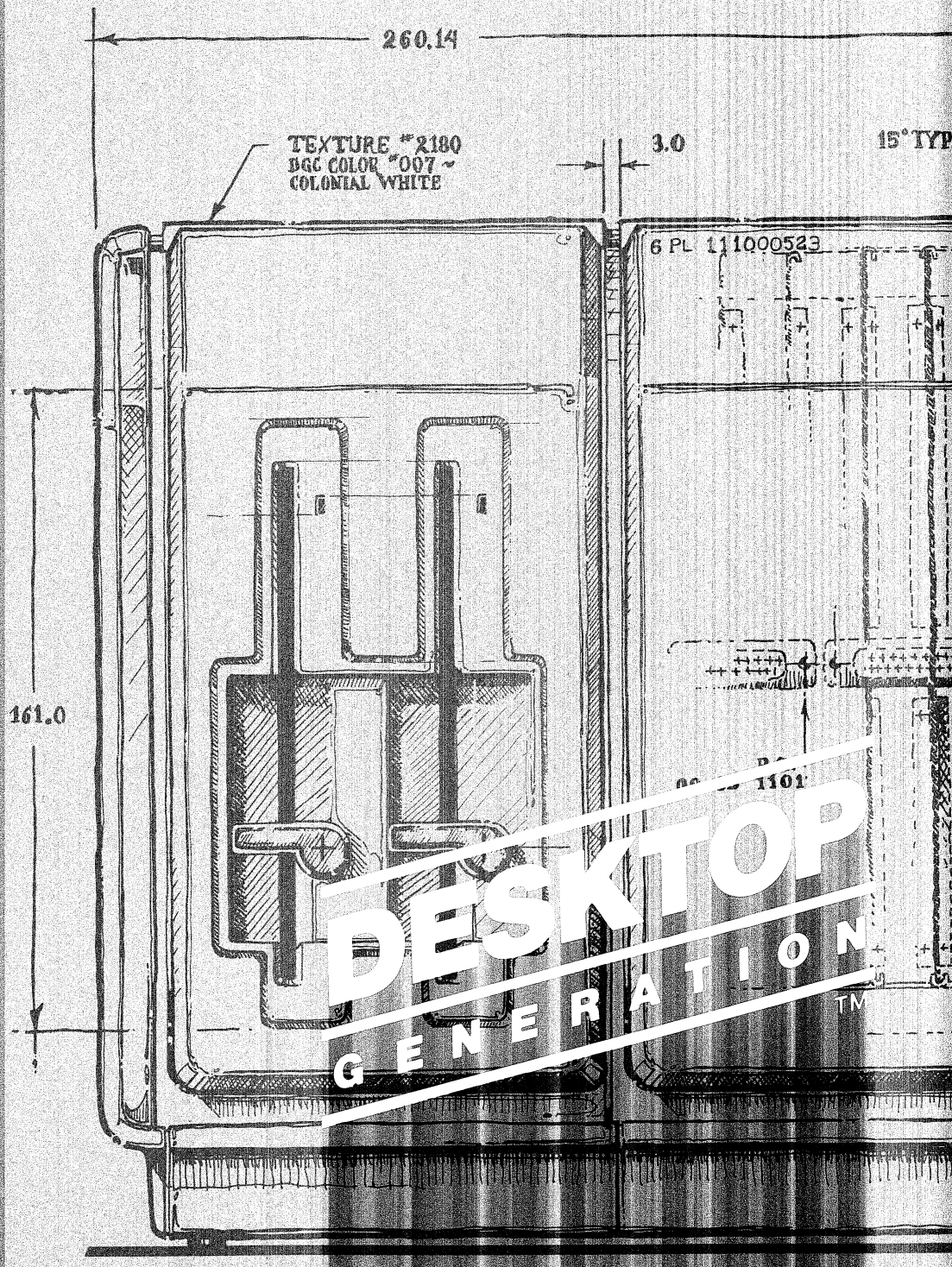
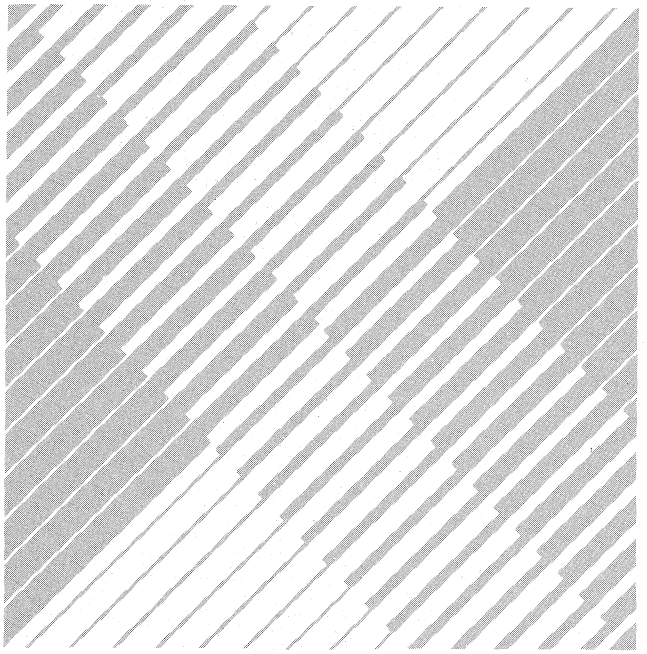


DESKTOP GENERATION™

Model 6271 Disk Subsystem

DataGeneral

DESKTOP GENERATION™
Disk Subsystems



DESKTOP GENERATION™

Technical Reference

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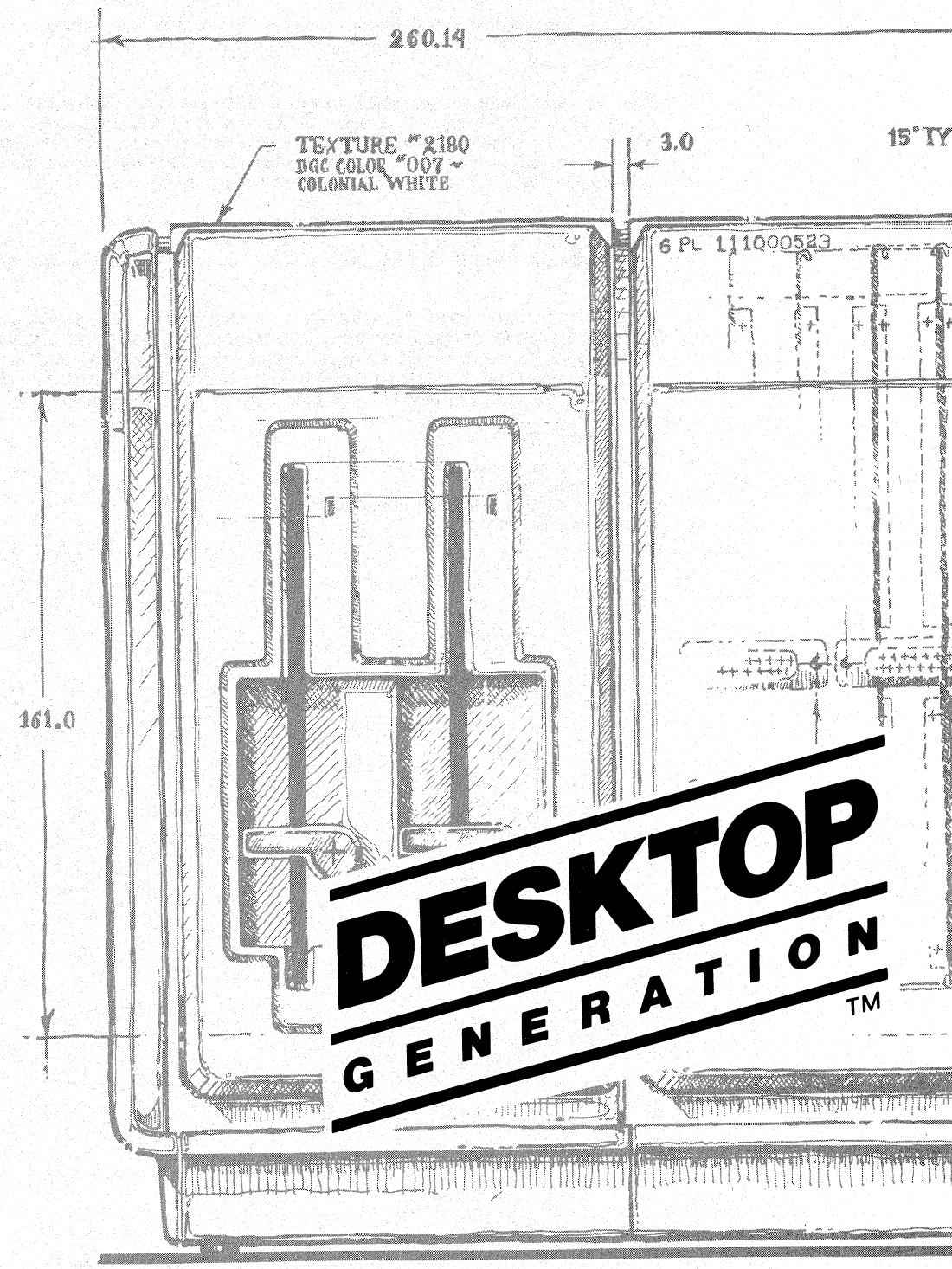
Ordering No. 014-000768

Rev. 02, April 1985

Data General

Technical Reference



Model 6271
Disk Subsystem

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Ordering No. 014-000768

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Rev. 00, October 1983

Preface

The DESKTOP GENERATION™ computers and their peripherals come with a complete set of manuals organized in three libraries according to the user's needs.

This manual is part of the *Technical Reference Library*. This library contains the information needed to write assembly language applications, including interface driver routines and operating systems. It also contains an assembly-level functional description of the system, and information on system expansion and custom interface design.

The *Operator's Library* provides information on using the equipment, cleaning and other routine maintenance, and conducting simple trouble-shooting procedures.

The *Installation Library* provides information on system configurations, specifications, system assembly, cable connections, and site planning.

Organization

This manual describes the disk subsystems that supply on-line storage for DESKTOP GENERATION computers. It includes four chapters, two appendices, and an index. It is organized so that portions of it can be read selectively.

- Chapter 1 gives an overview of the disk subsystem and lists its technical specifications.
- Chapter 2 defines the I/O instruction set for the subsystem and provides guidelines for writing I/O subroutines in assembly language to drive it. It also describes disk formatting procedures.
- Chapter 3 includes information about power requirements and interconnections with the host desktop generation system.
- Chapter 4 presents the theory of operation of the subsystem's controller.
- Appendix A describes the diagnostic instructions used to test the subsystem.
- Appendix B contains an exploded view of the subsystem's components and interconnection drawings.

The index alphabetically lists key concepts and terms. A comment form at the end of the book invites you to help us improve Data General publications by sending us your comments and suggestions.

Related Manuals

A comprehensive documentation set supports all the hardware and software products available for DESKTOP GENERATION computers. Many of the documents have been grouped into libraries, including the three libraries previously described. The First Step, a brochure packaged with your DESKTOP GENERATION equipment, describes all of the libraries and suggests reading paths for you to follow, based on the components you have selected for your system. The brochure also describes

- Product Briefs, two- to six-page summaries; each focusing on the features, capabilities, and specifications of a single hardware or software product;
- Self-Study Package offered by Data General's Customer Education organization;
- User Guides for DESKTOP GENERATION peripherals.

Your source for DESKTOP GENERATION and other Data General publications is the TIPS (Technical Information Publications Service) catalog. To request a copy of the catalog (DGC ordering no. 012-1749), order forms, or general publications information, write or call

Data General Corporation
Attn: TIPS Administrator/TIPS F019
4400 Computer Drive
Westboro, MA 01580
(617) 366-2900

Communications Interfaces
Technical Reference

Discusses the functional and physical organization of the asynchronous/ synchronous communications interfaces available for Desktop Generation computers. Defines their I/O instruction sets, offers guidelines for writing assembly language I/O subroutines, and contains theory of operation for each communications card. DGC ordering no. 014-000769.

Sensor I/O
Technical Reference

Defines instruction sets, offers guidelines for writing assembly language I/O subroutines, describes theory of operation at an overview level, and explains how to connect field wiring for the 4222 digital I/O interface, 4223 analog-to-digital interface, 4224 digital-to-analog interface, and 4335 analog subsystem. DGC ordering no. 014-000775.

IEEE-488 Bus Interface
Technical Reference

Provides the information needed to interface, program in assembly language, and troubleshoot this card in a Desktop Generation system. Reviews the contents of the IEEE-488 bus standard, summarizing its commands, messages, and states, and includes a theory of operation. DGC ordering no. 014-000773.

The following books are how-to manuals written for anyone who needs to know how to install, operate, and test a Desktop Generation system.

Installing Model 10 and 10/SP Systems

The first book that a Model 10 or 10/SP owner should read, explains how to unpack and install either system and its optional peripherals. Simple instructions and ample illustrations make the book accessible to any reader. DGC ordering no. 014-000901.

Operating Model 10 and 10/SP Systems

A logical follow-on to Model 10 and 10/SP installation, this guide takes you from powering up the system and its optional peripherals through performing such routine operations as loading paper in a printer and inserting or removing diskettes. Brings you to the point of loading the system software. Amply illustrated and written for users at any level of experience. DGC ordering no. 014-000900.

Testing Model 10 and 10/SP Systems

Follows the installation and operating manuals with instructions for verifying the operation of Model 10 or 10/SP systems and their optional peripherals. Steps you through the power-up test and Customer Diagnostics and explains how to troubleshoot customer-replaceable components. Simple instructions and diagrams make the book accessible to any user. Includes phone numbers for Data General assistance. DGC No. 014-000902.

Installing Model 20 and 30 Systems

The first book a Model 20 or 30 owner should read, explains how to unpack and install either system and its optional peripherals. Accessibly written and illustrated, for users at any level of experience. DGC ordering no. 014-000904.

Operating Model 20 and 30 Systems

Follows Model 20 and 30 installation, leading you from powering up the system and its optional peripherals through performing such routine operations as loading paper in a printer and inserting or removing diskettes. Brings you to the point of loading the system software. The simple instructions and generous illustrations are suitable for any reader. DGC ordering no. 014-000903.

Testing Model 20 and 30 Systems

A follow-on to the installation and operating manuals, explains how to verify the operation of Model 20 or 30 systems and their optional peripherals. Simple instructions and diagrams lead you through the power-up test, Customer Diagnostics, and trouble-shooting of customer-replaceable components. Includes phone numbers for Data General assistance. DGC No. 014-000905.

This last book is a product overview, addressed to all Desktop Generation users.

The Desktop Generation

Introduces the Desktop Generation, summarizing each model of the family, and describes its many hardware and software products, features, and capabilities. Includes a brief history of Data General, a sampling of applications, and an overview of the customer service and support programs available to you as a Desktop Generation user. DGC ordering no. 014-000751.

Conventions

The following conventions are used throughout this manual.

MNEMONIC	Uppercase sans serif letters indicate a signal name or instruction mnemonic. When a signal is active low, it is barred—for example, $\overline{\text{FDCHE}}$
argument	Italicized lowercase letters mean that a particular instruction takes an argument. In your program, you must replace this symbol with the exact code for the argument you need.
[optional]	Brackets signify an optional argument. If you decide to use this argument, do not include the brackets in your code; they only set off the choice.

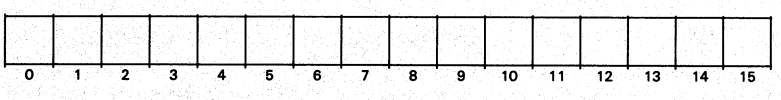
In dialogues between system and user, we use this typeface to show your input:

USER INPUT

and this typeface to show the system's response:

SYSTEM RESPONSE.

In addition, we use the following diagram to show the arrangement of the 16 bits in an instruction. The diagram is always divided into 16 boxes, numbered 0 through 15.



Other Publications

The DESKTOP GENERATION

Introduces the DESKTOP GENERATION, summarizing each model of the family, and describes its many hardware and software products, features, and capabilities. Includes a brief history of Data General, a sampling of applications, and an overview of the customer service and support programs available to the DESKTOP GENERATION user. This manual is not included in the standard documentation package. DGC ordering no. 014-000751.

Conventions

The following conventions are used throughout this manual.

MNEMONIC	Uppercase sans serif letters indicate a signal name or instruction mnemonic. When a signal is active low, it is barred — for example, $\overline{\text{FDCHE}}$.
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[optional]	Brackets signify an optional argument. If you decide to use this argument, do not include the brackets in your code; they only set off the choice.

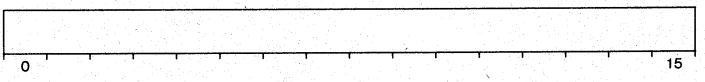
In dialogs between system and user, we use this typeface to show your input:

USER INPUT

and this typeface to show the system's response:

SYSTEM RESPONSE

In addition, we use the following diagram to show the arrangement of the 16 bits in a microECLIPSE instruction. The diagram is always divided into boxes, numbered 0 through 15.



Contents

1

Subsystem Overview

The disk subsystems provide disk storage for Data General DESKTOP GENERATION™ computer systems. The basic, primary subsystem can be expanded by adding a second disk subsystem. This secondary disk subsystem (designated by either an "A" or "B" suffix on the model number) consists of a disk drive module and an associated power supply module (see Figure 1-3). The primary subsystem contains a controller printed circuit card that provides the interface and control logic for operating both the primary and, when present, secondary units.

This chapter introduces the functional parts of the disk subsystems and lists their physical and technical specifications.

Disk Drive Unit

The disk drives are based on Winchester technology and contain three or more (depending on model), nonremovable recording disks. There is one head per surface and each head spans the full number of tracks on a surface. Each of the 17 sectors in a track can store 512 data bytes.

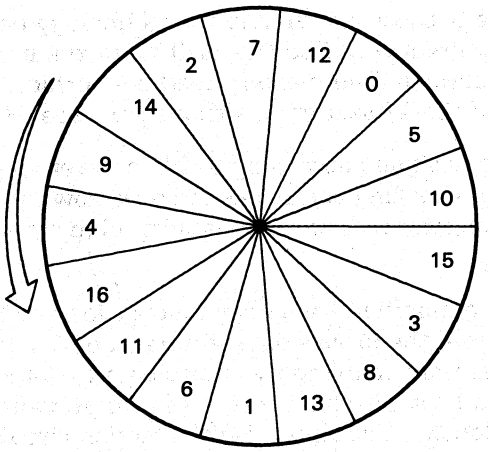
The heads are designed according to Winchester-type technology, allowing them to land on the recording surface as the disk slows to a stop. the heads and media together offer maximum reliability, high storage density, and fast data transfers.

In addition, the modified frequency modulations (MFM) method of encoding is used to maximize the drive's data storage capacity. Sectors are formatted with a special address field enabling the subsystem to detect access errors. A Bad Sector flag can be set in this address field to prevent data transfers on sectors known to be faulty. In addition, fault detection circuits in the drive mechanism itself help to maintain the integrity of the recorded data.

Disk Format

Each disk has two surfaces, top and bottom, which are formatted by Data General to provide the specified number of user tracks and one diagnostic track per surface. Each track is divided into 17 sectors which are soft-sectored, meaning that there are no physical reference points to identify sector boundaries. Transfers between main memory and the disk drive are fully sector-buffered to prevent the drive from exceeding the throughput capacity of the data channel facility. To minimize waiting time between transfers, the sectors are functionally numbered independently of the physical sequence. In this scheme, called logical mapping, the sectors are interleaved by a factor of seven, as shwon in Figure 1-1. This logical mapping function is performed by the controller and is transparent to the host program.

With interleaving by seven, the drive transfers every seventh physical sector during a multiple sector transfer. for example, during a read operation, when the disk finishes-reading-sector 0 on a track, there is enough time before sector 1 comes under the head to transfer the data from sector 0 to the host and to prepare to read sector 1. Subsequently, the controller reads and writes contiguous data on every seventh physical sector.



ID-00609

Figure 1-1 Sector numbering interleaved by seven

In this manner, up to sixteen sectors can be transferred in one command. A multiple-sector transfer beginning with one head can continue on the next head. Thus, any sixteen contiguous sectors can be transferred out of the total number of sectors available at a particular cylinder. The controller also performs extensive error checks, including Cyclic Redundancy Checks (CRC), on the recorded data.

Disk Controller

The controller logic provides the facilities to handle two drive units and is incorporated on a separate printed circuit card. The five major sections of the controller card, as well as their functions, are listed below:

I/O controller (IOC). Provides control for data transfers and interface functions with the host's microI/O bus.

Microprocessor (interface controller CPU). Interprets commands, handles error and status, and directs subsystem activites.

Disk controller chip. Handles seek and read/write operations on the disk drive.

DCH/RAM controller chip. Handles data transfer operations between the disk controller logic and the sector buffer RAM. Also supervises data channel operations between the sector buffer RAM and the host memory.

Disk interface circuits. Provide head positioning signals, select the active head, provide a write signal to the drive, monitor drive status and error signals, develop a read clock, and decode data from the drive's read signal.

Physical Description

Each disk drive resides in its own modular enclosed chassis, as shown in Figure 1-2. In this modular configuration, the disk module physically joins with other system modules by a simple latching scheme, and is electrically connected by

DIN connectors that join its backpanel with those of adjoining modules (Appendix B provides detailed interconnect information).

The first primary drive in a system receives its power from the system's number 2 power supply via a cable connected to the module's backpanel. The controller card is mounted in the same module with the drive unit and is connected to the CPU's I/O bus via its B connector which plugs into the module's backpanel. A flat ribbon cable, which connects to the A connector on the controller card, provides signal connection to the drive. This cable also joins to a D-type connector on the rear panel of the disk module for connection to a second drive.

When a second disk drive is used, it resides in a separate, stand-alone two-module unit, as shown in Figure 1-3. In this configuration, one module contains only a disk drive and its associated cabling, while the second module contains a power supply unit that provides it with dc power. System interfacing and control functions are performed by the first drive's controller card, joined by a cable to the D-type connectors on the rear panels of the disk modules.

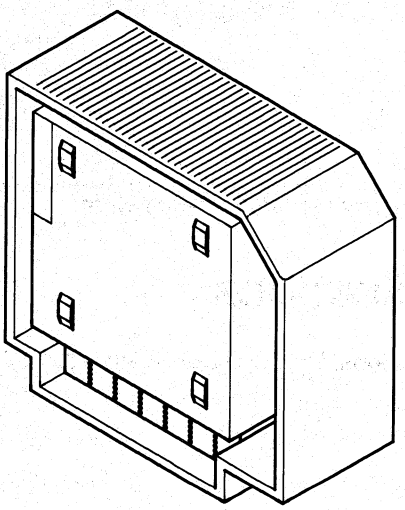


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Figure 1-2 Disk drive subsystem (primary drive)

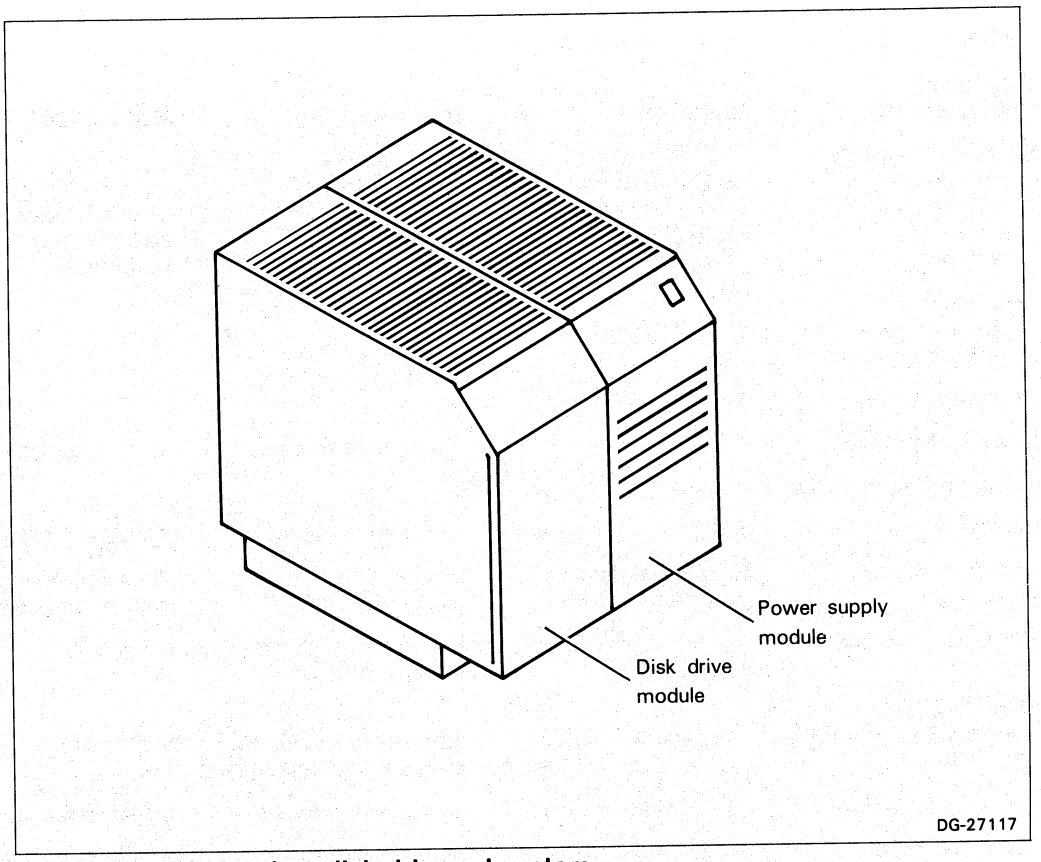


Figure 1-3 Secondary disk drive subsystem

Technical Specifications

Technical specifications for the disk subsystems are listed in Table 1-1.

Table 1-1 Technical specifications

Physical Description	
Module dimensions:	4.8 in. wide (12.2 cm), 10.7 in. high (27.2 cm), 12.8 in. deep (32.5 cm)
External panels:	Earth-tone brown, plastic, snap-on attachment
Internal chassis:	Metal chassis houses backpanel, drive unit, and controller card
Backpanel:	Printed circuit card providing both internal and external connections
Internal connections:	Power cable for drive unit. receptacle for controller card B connector, ribbon cable from controller card A connector to drive unit
External connections:	Power and signal connections via 96-pin DIN connectors for both input/output and for transfer to next module
Controller configuration:	7 in. by 9 in. printed circuit card

Table 1-1 Technical specifications (cont.)

Functional Characteristics	Model 6271[2]	Model 6301[2]	Model 6336[3]
Formatted capacity			
per drive:	15.928 Mbytes[1]	38.628 Mbytes[1]	71.233 Mbytes[1]
per surface:	2.655 Mbytes[1]	5.518 Mbytes[1]	8.904 Mbytes[1]
per cylinder:	52,224 bytes	60,928 bytes	69,632 bytes
per track:	8704 bytes	8704 bytes	8704 bytes
Disk format			
sectors/track:	17	17	17
bytes/sector:	512	512	512
Number of disks:	3	4	5
Number of surfaces:	6	7 data plus 1 servo	8 data plus 1 servo
Number of heads/surface:	1	1	1
Number of cylinders:	305 data, 1 diagnostic,	634 data, 1 diagnostic	1023 data, 1 diagnostic
Encoding method:	Modified frequency modulation (MFM)	Modified frequency modulation (MFM)	Modified frequency modulation (MFM)
Write current reduction:	Automatic for tracks 256 through 305	Automatic for tracks 320 through 645	Automatic
Write data peak shift precompensation:	12 ns early or late on cylinders 256 through 305	12 ns early or late on cylinders 320 through 645	Not required
Power-on to ready:	30 seconds maximum	15 seconds maximum	25 seconds maximum
Rotational speed:	3600 RPM, nominal	3600 RPM, nominal	3600 RPM, nominal
Rotational latency:	8.333 ms, nominal average	8.333 ms nominal average	8.333 ms nominal average
Read/write data rate:	5 MHz, typical	5 MHz, typical	5 MHz, typical
Seek time (includes settling):	19 ms track to track; 68 ms average; 122 ms full stroke	8 ms track to track 55 ms average 130 ms full stroke	6 ms track to track 32 ms average 63 ms full stroke

[1] *Does not include diagnostic cylinder.*

[2] *Same specifications apply for drives with an "A" suffix.*

[3] *Same specifications apply for drives with a "B" suffix.*

Table 1-1 Technical specifications (cont.)

Functional Characteristic (cont.)	Model 6271[1]	Model 6301[1]	Model 6336[2]
Head switch time:	20 μs maximum	8 μs maximum	20μs maximum
Write to read recovery time:	20 μs maximum	8 μs maximum	8μs maximum
Host interface (controller):	Data General microI/O bus, using both programmed I/O and data channel transfers.		
Data transfer rate (controller)			
Disk to/from buffer:	625 Kbytes per second	625 Kbytes per second	
Buffer to data channel	approximately 146 Kbytes per second (host-dependent)		
Data channel to buffer	approximately 171 Kbytes per second (host-dependent)		

Electrical Requirements

Model 6271: Primary drive

Voltage:	+5 VDC	-5 VDC	+12 VDC
Regulation:	±5%	±5%	±5%
Maximum running current:	4.5 amps	.05 amps	1.6 amps
Peak starting current:	5 amps	.05 amps	4.1 amps
Power dissipation (max.) (disk/controller):	44.5 watts		

Model 6301: Primary drive

Voltage:	+5 VDC	-5 VDC	+12 VDC
Regulation:	±5%	±5%	±5%
Maximum running current:	3.5 amps	.05 amps	3.3 amps
Peak starting current:	4 amps	.05 amps	4.6 amps
Power dissipation (max.) (disk/controller):	45.5 watts		

Model 6336: Primary drive

Voltage:	+5 VDC	+12 VDC
Regulation:	±5%	±5%
Maximum running current:	1.9 amps	3.3 amps
Peak starting current:	2.0 amps	4.5 amps
Power dissipation (max.) (disk/controller):	45.5 watts	

[1] *Same specifications apply for drives with an "A" suffix.*

[2] *Same specifications apply for drives with an "B" suffix.*

Electrical Requirements, Models 6271-A, 6301-A, and 6336-B, secondary drives

Voltage:	100 VAC supply; range 90 to 115 VAC 120 VAC supply; range 102 to 132 VAC 220/240 VAC supply; range 187 to 264 VAC
Maximum in-rush current:	30 amps (RMS) @ 120 VAC
Maximum running current:	1.5 amps (RMS) @ 120 VAC
Power dissipation (disk and power (modules)	70 watts maximum

2

Programming

From a programming point of view, the disk controller contains seven major registers and two status flags for use in data transfers and operations related to them. Your programs can incorporate instructions to direct the controller to set up and initiate a data transfer, and two others to read status information.

This chapter provides the information required to create an interface program for the disk subsystems. It begins with a tabular summary of programming information, followed by a description of the registers and flags in the disk controller that your program can manipulate. Then five instructions are defined for your use in programming a host interface for disk subsystems. A discussion of programming considerations and guidelines supplements this information, and discussions of I/O timing and error conditions conclude the chapter.

Programming Summary

In this section, Table 2-1 summarizes the characteristics of the disk subsystems; Figure 2-1 presents the accumulator formats of the instructions used to program them; and Table 2-2 defines the Start, Pulse, and Clear command flags and the IORST function.

Table 2-1 Programming Summary: subsystem specifications

	Model 6271[2]	Model 6301[2]	Model 6336[3]
Mnemonic[1]	DEP	DEP	DEP
Device code[1]	26 octal	26 octal	26 octal
Mask bit	7	7	7
Maximum capacity	15.92 Mbytes*	38.62 Mbytes*	71.23 Mbytes
Data encoding method	Modified frequency modulation (MFM)	Modified frequency modulation (MFM)	Modified frequency modulation (MFM)
Number of surfaces	6	7	8
Heads/surface	1	1	1
Tracks/head	305 user (0-460 octal); 1 diagnostic	634 user (0-1171 octal); 1 diagnostic	1023 user (0-1776 octal); 1 diagnostic
Sectors/track	17 (0-20 octal)	17 (0-20 octal)	17 (0-20 octal)
Bytes/sector	512 (1000 octal)	512 (1000 octal)	512 (1000 octal)
Data transfer rate			
disk to/from buffer:	625,000 bytes/second	625,000 bytes/second	625,000 bytes/second
buffer to data channel:	approximately 146 Kbytes/second	(CPU-dependent)	
data channel to buffer:	approximately 171 Kbytes/second	(CPU-dependent)	
Data channel latency	N/A (full-sector buffered)	N/A (full-sector buffered)	N/A (full-sector buffered)
Track access time			
minimum:	19 ms	8 ms track-to-track	6 ms track-to-track
average:	68 ms (1/3 stroke)	55 ms average	32 ms average
maximum:	122 ms	130 ms full stroke	63 ms full stroke
Recalibrate time	5.7 seconds, maximum	7 seconds, maximum	20 seconds, maximum
Rotational speed	3600 RPM, nominal	3600 RPM, nominal	3600 RPM nominal
Rotational latency	8.3 ms, average	8.3 ms, average	8.3 ms, average

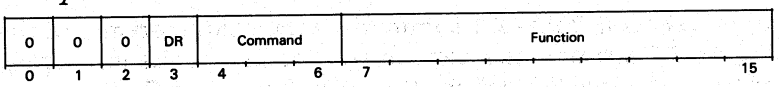
* *Includes diagnostic tracks*

[1] *Applies for both primary and secondary drives.*

[2] *Same specifications apply for drives with an "A" suffix.*

[3] *Same specifications apply for drives with a "B" suffix.*

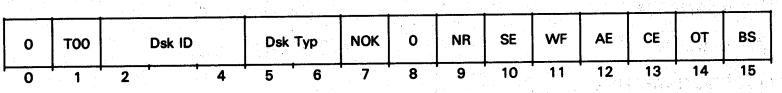
Specify Command (DOA)



Bit Values	Commands
000	Read Disk
010	Write Disk
011	Format Track
100	Diagnostic Operation
101	Get Sector Count
110	Seek Cylinder
111	Recalibrate

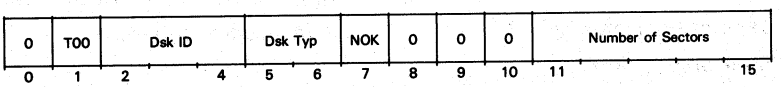
Read Status (DIA)

Context: A "Get Sector Count" command was not issued previously.

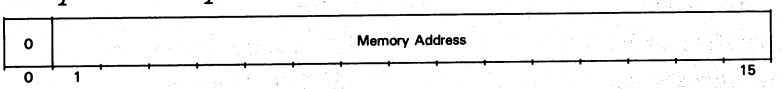


Read Status (DIA)

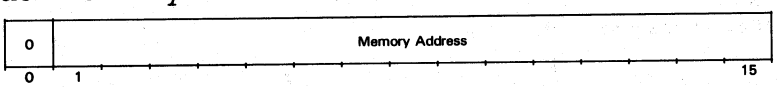
Context: A "Get Sector Count" command was issued previously.



Specify Memory Address (DOB)



Read Memory Address (DIB)



Specify Word Count (DOC)

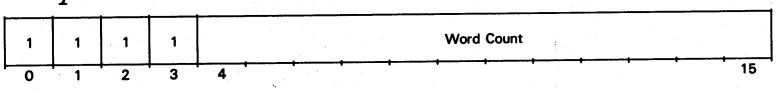


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Figure 2-1 Programming summary: accumulator formats

Table 2-2 Programming Summary: START, CLEAR, PULSE, and IORST functions

f = S	Sets the Busy flag to 1 and sets the Done flag to 0. Initiates the command specified by the contents of the command register.
f = P	Sets the Done flag to 0[1]
f = C	Sets the Busy and Done flags to 0 and initializes the controller. Current position of the heads is lost.
IORST	Performs all functions of the Clear flag and clears the memory address register. Also sets the IPL flag to 1 and sets the Interrupt Disable flag to 0.

[1]*The Pulse command should be issued to clear program interrupts since the Clear command and I/O Reset (IORST) instruction cause the interface to lose position information for the drives. Thereafter, a Seek command must be issued before a Read or a Write operation can be performed. The controller automatically recalibrates the drive before it processes the first Seek command after a Clear or IORST operation.*

Program-Accessible Elements

Figure 2-2 depicts the various registers and flags in the controller that are accessible to the programmer. In general, the registers are used to temporarily store commands issued from the host, read subsystem status, program the controller card for data channel operation, and also as temporary registers for data transfers to and from the host. The Busy and Done flags provide status for operations initiated by program commands. This section briefly describes the individual registers and flags.

Memory Address Register

The memory address register is self-incrementing and contains the address of the next memory location to be accessed for a data channel transfer. The register is written to by a Specify Memory Address instruction (DOB) from the host and is read by a Read Memory Address instruction (DIB).

Word Count Register

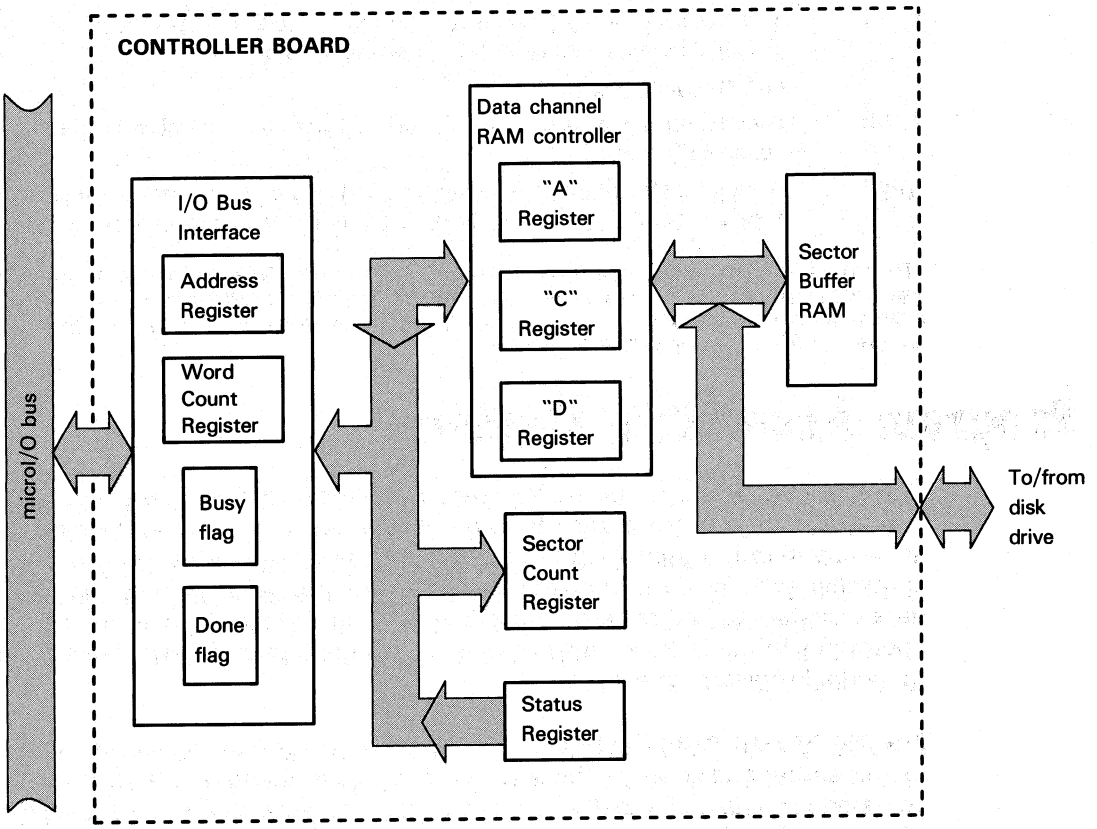
The word count register is self-incrementing and contains the two's complement of the number of words to be transferred to or from memory via the data channel facility. The word count register is written to by a Specify Word Count instruction (DOC) from the host.

Busy Flag

The Busy flag is set to 1 when a Start command is received and reset to 0 by the controller upon completion of the functions specified by the contents of the command (A) register.

Done Flag

The Done flag is set to 1 when an operation is completed or an error occurs. The controller initiates a program interrupt request whenever the Done flag is set to 1 and interrupts are enabled.



NOTE *Though not directly accessible by the program, the sector buffer RAM is shown to depict the data transfer scheme.*

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Figure 2-2 Program-accessible registers and flags

A Register

The A register functions as the command register for Specify Command instructions (DOAs) from the host. It also functions as a temporary data storage register for data channel transfers from memory to the Sector Buffer RAM (a write to disk operation). The register is loaded as a single 16-bit word and is read out as two 8-bit bytes.

C and D Registers

The C and D registers are 8-bit registers that provide temporary data storage for data channel transfers from the sector buffer RAM to memory (a Read Disk operation). These registers can also be read using a DIC input instruction. Each register is loaded independently with an 8-bit byte, but both are read out together as a single 16-bit word to the host.

Sector Count Register

The sector count register is an 8-bit register that is written to with a Specify Word Count (DOC) instruction, which also loads the word count register. When the word count is loaded into the word count register, the most significant byte (which also equals sector count) is loaded into the sector count register.

Status Register

The status register stores the subsystem status and is read by a Read Status (DIA) instruction from the host.

Sector Buffer RAM

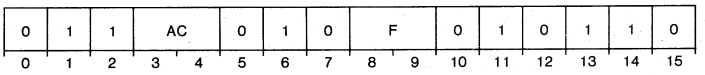
The Sector Buffer RAM, though not directly accessible to the programmer, is accessed indirectly as a consequence of Read Disk and Write Disk instructions.

Programming Instructions

This section defines and gives the format of the five instructions used to program a host interface for the disk subsystems. Three of these instructions supply the controller with the information necessary to select a cylinder and initiate data transfers between main memory and the disk subsystem via the data channel facility. The remaining two instructions allow the program to retrieve detailed status information.

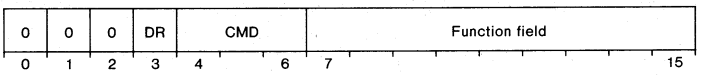
Specify Command

DOA*[f]* *ac*, DEP



Loads bits 0-15 of the specified accumulator (AC) into the command register and sets the IPL flag to 0. After the data transfer, the controller's Busy and Done flags are set according to the function specified by *f*. The contents of specified accumulator remain unchanged.

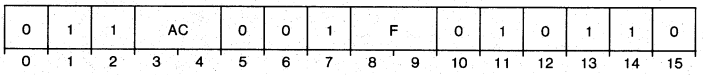
The format of the accumulator follows:



Bit(s)	Name	Function
0		Must be 0
1		For 15 Mbyte drive, must be 0; for 38.6 Mbyte and 71.2 Mbyte drives, this is track bit 9
2		Must be 0
3	Drive Select	Specifies which drive is active, where: 0 = drive 0 1 = drive 1
4-6	Command	Specifies the command to be performed as follows: 000 = Read 001 = Reserved 010 = Write 011 = Format track (see section entitled Disk Reformatting 100 = Diagnostic operation (defined by bits 9-15) 101 = Get sector count for last data transfer 110 = Seek track (cylinder) 111 = Recalibrate
7-15	Function field	Operation defined by the contents of the function field as explained below.
	Track 0-8	If Seek track command, specifies the target track (cylinder) address on bits 7-15.
	Sector	If Read, Write, or Format track command, bit 7 must be 0; bits 8-10 specify head select code; bits 11-15 Specify the starting sector address to read or write data. All 0's for Format command.
	Diganostic Command	If Diagnostic command, bits 7-10 depends on diagnostic command; bits 11-15 specify the diagnostic operation to be performed.

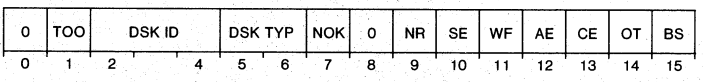
Read Status

DIA*[f]* *ac*, DEP



Context: Get Sector Count command was not issued previously.

When the previous command issued to the controller was any command other than a Get Secto Count, this command loads the contents of the currently-selected drive status register into bits 0-15 of the specified accumulator. After the data transfer, the controller's Busy and Done flags are set according to the function specified by *f*. The format of the specified accumulator following the transfer is shown below.



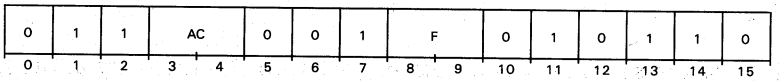
Bit(s)	Name	Function
0		Always set to 0.
1	Track 00	If 1, indicates the last disk drive selected has its heads positioned over track (cylinder) zero.
2-4	Disk ID	Identifies the disk subsystem; always set to a value of 3 (011).
5-6	Disk Type	Identifies the disk type and capacity, as follows: 00 = reserved 01 = 15 Mbytes, 10 = 38.6 Mbytes 11 = 71.2 Mbytes
7	Not OK	If 1, indicates that the controller failed its self-test after a power-up operation. This bit resets when the controller passes its self-test diagnostic.
8		Always 0 (reserved for future use).
9	Not ready	If 1, indicates that the drive is not ready to accept commands. This may be because the drive is not up to speed, a fault is present in the drive, or the dc voltages in the drive are out of tolerance.
10	Seek Error	If 1, indicates that the Track 00 signal failed to assert during a Recalibrate operation or a Seek operation that performed an automatic recalibrate operation. This error is also set if a Seek command is issued with a cylinder address greater than the maximum. To recover head position, reissue the Recalibrate command and, if successful, continue with the normal command sequence.
11	Write/Fault	If 1, indicates that a condition exists at the drive that causes improper writing on the disk. Three conditions can cause this fault: (1) write current in a head without write gate active, or no write current in the head with write gate active and drive selected; (2) multiple heads are selected; (3) dc voltages in the drive are grossly out of tolerance (Not Ready will also be set).

Bit(s)	Name	Function
12	Address Error	If 1, indicates that (a) the controller was unable to find the sector desired or the data field was not found following the address field; (b) a Read/Write command was issued with a head or sector address greater than the maximum; (c) an attempt was made to transfer a sector past the end of the current cylinder; or (d) the Bad Sector flag (bit 15) is set.
13	Checkword Error	If 1, indicates that the checkword read from the Error current sector did not match the checkword calculated by the controller during a read operation.
14	Operation Time-Out	If 1, indicates that the specified operation failed to complete within a reasonable time (approximately 11 seconds).
15	Bad Sector	If 1, indicates that the last sector accessed is unreliable for data storage and was flagged bad by the formatter program. Also causes address error to be set.

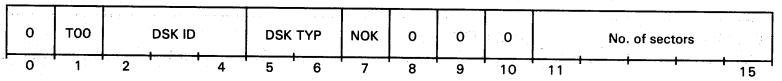
Read Status

DIA*[f]* *ac*,DEP

Context: Get Sector Count command was issued previously.



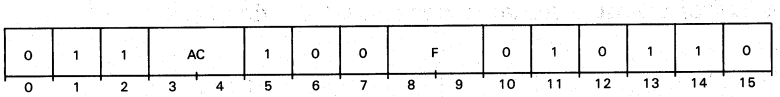
When the previous command issued to the controller was a Get Sector Count, this command loads the first eight, high-order bits of the currently-selected drive status registers and the sector count (for number of sectors transferred) into bits 0-15 of the specified accumulator. After the data transfer, the controller's Busy and Done flags are set according to the function specified by *f*. The format of the specified accumulator following the transfer is shown below.



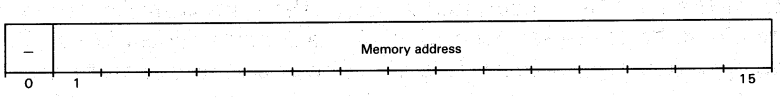
Bit(s)	Name	Function
0	—	Always set to 0.
1	Track 00	If 1, indicates the last disk drive selected has its heads positioned over track (cylinder) zero.
2-4	Disk ID	Identifies the disk subsystem; always set to a value of 3 (011).
5-6	Disk Type	Identifies the disk type and capacity, as follows: 00 = reserved 01 = 15 Mbytes, 6 heads, 305 tracks (cylinders) 10 = reserved 11 = reserved
7	Not OK	If 1, indicates that the controller failed its self-test after a power-up operation. This bit resets when the controller passes its self-test diagnostic.
8-10	—	All 0s (reserved for future use).
11-15	No. Sectors	Indicates the number of sectors transferred during the last read/write operation that preceded the Get Sector Count command.

Specify Memory Address

DOB*[f]* *ac*,DEP



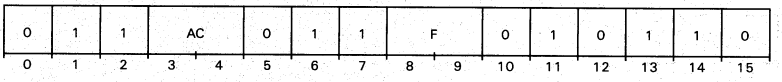
Loads bits 1-15 of the specified accumulator (AC) into the memory address register. After the data transfer, the controller's Busy and Done flags are set according to the function specified by *f*. The contents of the specified accumulator remain unchanged. The format of the accumulator follows:



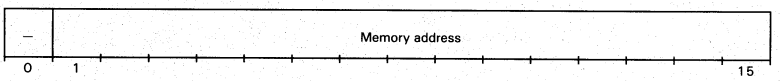
Bit(s)	Name	Function
0	–	Reserved for future use.
1-15	Memory Address	Location in memory to be accessed for the first data channel transfer.

Read Memory Address

DIB*[f]* *ac*,DEP



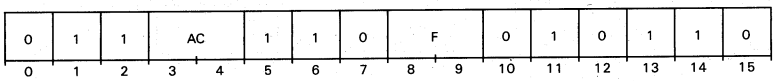
Places the contents of the memory address register in bits 1-15 of the specified accumulator (AC). After the data transfer, the controller's Busy and Done flags are set according to the function specified by *f*. The format of the accumulator follows:



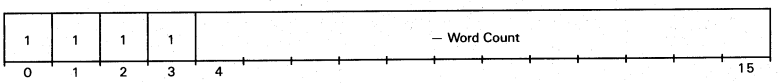
Bit(s)	Name	Function
0	–	Reserved for future use.
1-15	Memory Address	Location in memory to be accessed for the next data channel transfer.

Specify Word Count

DOC*[f]* *ac*,DEP



Loads bits 0-15 of the specified accumulator (AC) into the word count register; loads bits 0-7 into the sector count register. After the data transfer, the controller's Busy and Done flags are set according to the function specified by *f*. The contents of the specified accumulator remain unchanged. The format of the accumulator follows.



Bit(s)	Name	Function
0-3	—	Must be set to 1s.
4-15	Word Count	Two's complement of the total number of words to be transferred (-256 x no. of sectors).

Programming Guidelines

Factors involved in programming the disk subsystem are the subject of this section, which covers the following areas and provides guidelines for handling each one:

- Power-up conditions
- Initial program load (IPL) facility
- Selecting and recalibrating the drive
- Position the drive's read/write heads over the desired cylinder
- Performing a data transfer, including specifying the number of words to be transferred, specifying the location in memory to be used as the source or destination of the transfer, selecting a starting head and sector, and issuing a read or write command
- I/O timing constraints
- Powering down
- Reformatting a disk, as required
- Error conditions

The programming sequences assume that no errors occur during head positioning and data transfer operations. Any error conditions should therefore be corrected (refer to "Error Conditions" later in this chapter).

Power-Up Conditions

When the drive is first powered up, the disk starts rotating and the controller logic is automatically initialized. At this point, the controller is idle, waiting for a command.

NOTE *The drives are not recalibrated when the subsytem is powered up. Instead, the track address register of each drive is initialized to an illegal address number, which prompts the subsystem to recalibrate the drive automatically when the first Seek command is issued.*

Initial Program Load

The disk subsystem has an initial program load (IPL) feature that can transfer a low-level bootstrap program from the disk to the CPU. The transfer originates from drive number 0. If the drive is not ready, the IPL operation waits until it is ready. The bootstrap program must first be recorded on the first sector of the disk: sector 0 on head and track 0. The IPL sequence transfers this sector to the first 256 locations of the computer's memory bank.

An IPL operation usually occurs when the subsytem is first powered up. (There are several ways to initiate an IPL. Refer to information on the specific system for details). The computer first executes a small loader program that initializes the disk subsystem. The loader program issues an I/O Reset (IORST) instruction followed by a Start flag command. Then the program branches to memory location 377 octal and waits. (This memory location contains a Jump instruction to itself.)

The I/O Reset initializes the controller logic, sets the IPL flag to 1, and clears the memory address register. The Start command sets the Busy flag to 1, sets the Done flag to 0, and starts the operation. The controller directs a recalibrate operation on the drive and then transfers the sector. When the transfer is completed, the Busy flag is set to 0, the Done flag is set to 1, and a program interrupt request is initiated, if interrupts are enabled.

The last word in the sector contains a Jump instruction to a location in the bootstrap program. This forces the computer to execute the program after all 256 words are transferred. First the program terminates the Read operation. Next it transfers information from other sectors on the disk to load the operating system and bring the system on line. The IPL flag is cleared the first time the computer issues a Specify Command with a Seek instruction (DOA).

Selecting and Recalibrating a Drive

The following steps ensure that the subsystem is ready to perform an operation and select and recalibrate the drive.

1. Before initiating any operation, ensure that the Busy flag is set to 0.
2. Issue a Specify Command (DOA) instruction with a Start command, specifying the selected drive and a Recalibrate instruction.
3. When Done sets to 1, follow up with a Read Status instruction (DIA) and check to make sure that no errors occurred.

Positioning the Heads

Positioning operations move the read/write heads to the desired cylinder for a data transfer or a format operation. Following a Recalibrate command, the selected drive has its heads positioned at track (cylinder) 0 (the drives detect a mechanical reference point to recalibrate on track 0). When a Seek command is issued, the positioner moves the heads the required number of steps to select the desired cylinder. It is important to note that the positioner must be recalibrated before the first Seek operation can occur. Note too, that the positioner is automatically recalibrated during the first Seek operation that follows an I/O Reset (IORST) instruction or a Clear command.

Use the following programming sequence to position the heads in a selected cylinder. Refer to Figure 2-3.

1. Issue a Specify Command (DOA) instruction with a Start command and Seek track instruction to move the heads to the desired cylinder. The Start command sets the Busy flag to 1, sets the Done flag to 0, and starts the positioning operation. When the operation is completed, the controller sets the Busy flag to 0, sets the Done flag to 1, and initiates a program interrupt request, if interrupts are enabled.
2. After the Seek operation is completed, issue a Read Status instruction (DIA) with a Pulse command. Check that the Not Ready, Seek Error, and Operation Timeout flags are set to 0. If a recoverable error occurred, try the operation again.

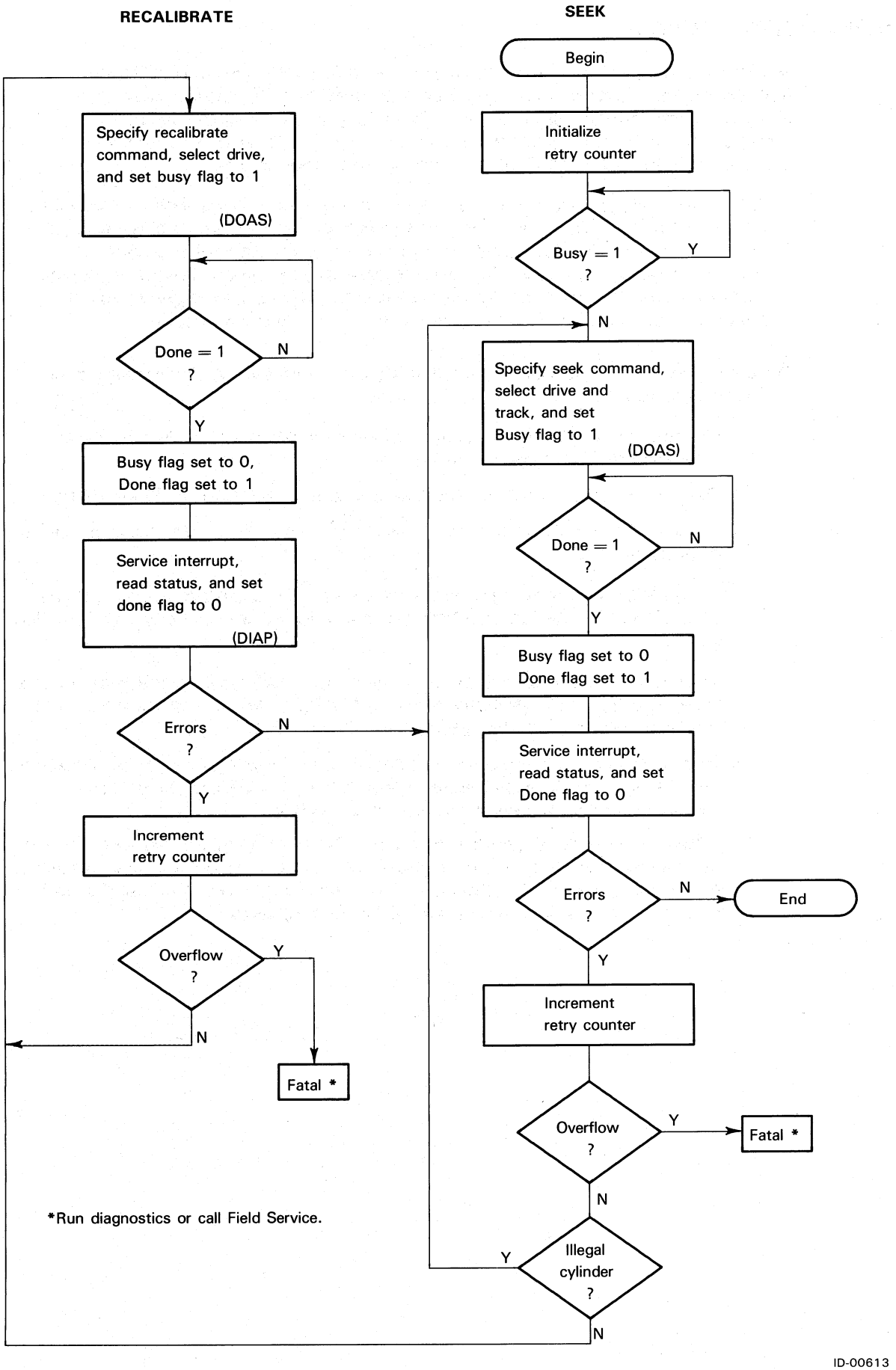


Figure 2-3 Head positioning

Transferring Data

Read and write operations can transfer one or more 256-word data blocks (depending on the word count specified) between the CPU and the disk drive. Data is transferred via the data channel, starting at the memory location specified by the Specify Memory Address instruction (DOB). Note that the disk subsystem is fully sector-buffered to prevent data-late conditions.

Fully-buffered transfers occur in two phases. In one phase, data moves between the buffer and the disk. In the other phase, data moves between the buffer and the CPU. Two-phase buffering means that the subsystem cannot transfer contiguous physical sectors on the drive. A hardware mapping function provides that every seventh physical sector on the disk is assigned a contiguous logical address to allow transfer of more than one sector per disk revolution.

Read Operation

Observe the following precautions before proceeding with a read operation.

1. Be sure that the heads are positioned over the desired cylinder. (Refer to "Positioning the Heads" in this section.)
2. Be sure that data is recorded on the disk before attempting a Read operation.
3. Do not initiate a multiple sector transfer that exceeds 16 sectors or crosses a cylinder boundary.

Continue with the following programming sequence to read data from the disk. Refer to Figure 2-4. Before initiating any operation, make sure that the Busy flag is set to 0.

4. Issue a Specify Command and Read instruction (DOA) with no flag command, using the appropriate accumulator bits to select a drive, sector count, and head and sector address, and to specify a Read command.
5. Issue a Specify Memory Address instruction (DOB) with no flag command and use the appropriate accumulator bits to specify the address of the first memory location to receive the read data block(s).
6. Issue a Specify Word Count instruction (DOC) with a Start command. Use the appropriate accumulator bits to specify the number of sectors to be transferred (two's complement). The Start command sets the controller's Busy flag to 1, sets the Done flag to 0, and initiates the Read operation.

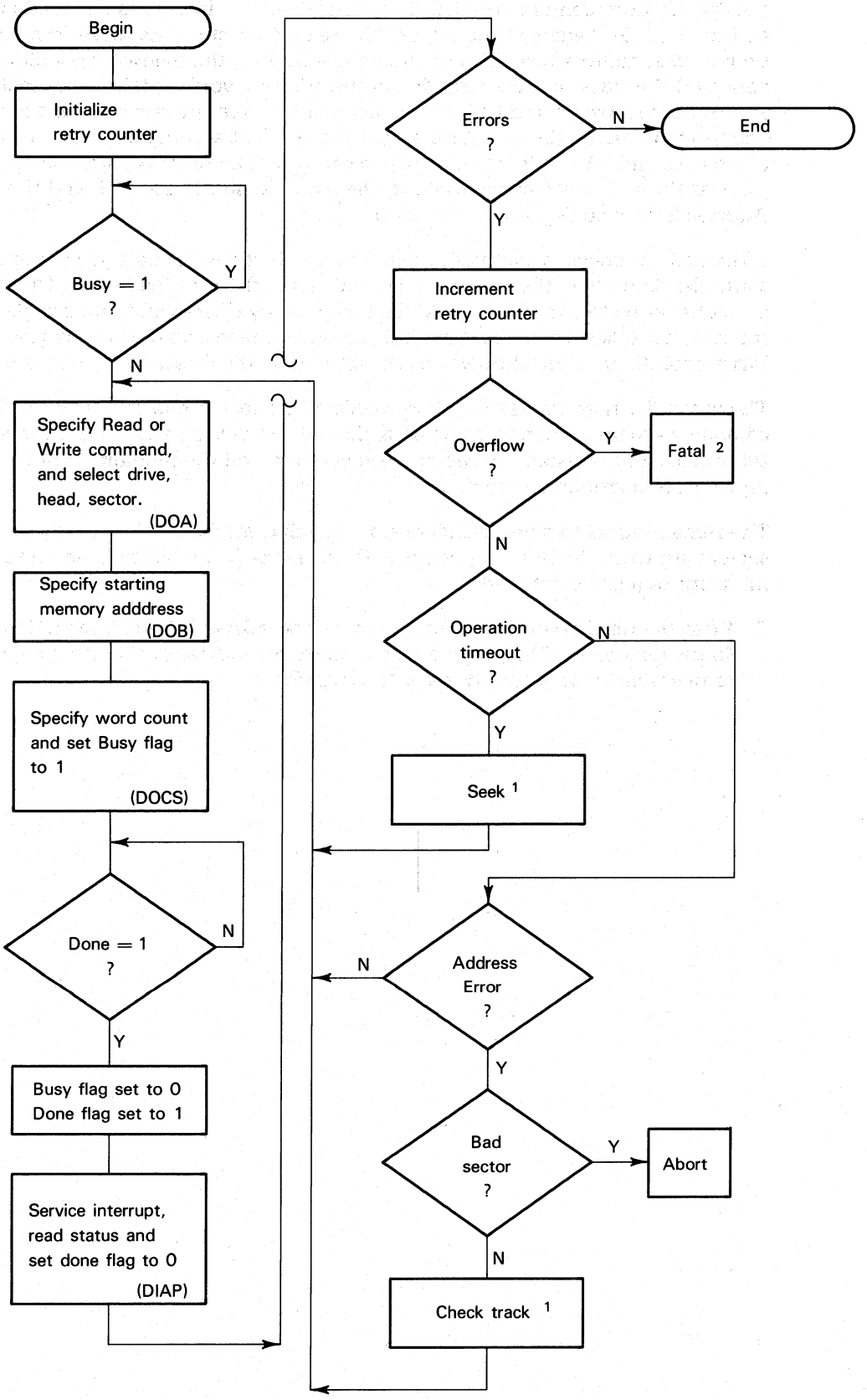
In performing a read operation, the controller searches for the sector selected by the Specify Command instruction. The controller then initializes the read logic, and the transfer begins at the start of the selected sector. The drive first reads the prerecorded address field. The controller checks that the following conditions apply: (1) the track address recorded in the address word matches the track address in the Seek command; (2) the head and sector address recorded in the address field match the head and sector address that accompanied the Read command; and (3) The Bad Sector flag is set to 0. If an error occurs, the operation stops at the end of the address check, the data transfer is aborted, and the Address Error and Done flags are set to 1.

If the address check is successful, the drive reads the serial data stream and the controller assembles 16-bit data words and stores them in the buffer. The controller also calculates a 16-bit Cylic Redundancy Checkword and compares it to the one that follows the data field (calculated and recorded during the previous Write operation). If the checkwords do not match, the Check Error flag is set to 1.

The controller now transfers all 256 words of the sector, one at a time, to the computer's memory bank via the data channel. Each time a word is transferred, the word count register, the sector word counter, and the memory address register are incremented by one.

The remaining sectors are transferred in a similar manner. When all the sectors are read, the Busy flag is set to 0, the Done flag is set to 1, and a program interrupt request is initiated.

7. After the Read operation is completed on the selected drive, issue a Read Status instruction (DIA) with a Pulse command and check the error flags. If a recoverable error occurred, retry the transfer.



[1] *See head positioning figure*
[2] *Run diagnostics or call Field Service.*

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Figure 2-4 Read or write data

Write Operation

Observe the following precautions before proceeding with a write operation.

1. Be sure that the heads are positioned over the desired cylinder. (Refer to "Positioning the Heads" in this section.)
2. Be sure that the disk is properly formatted.

Continue with the following programming sequence to write data on the disk. Refer to Figure 2-4. Before initiating any operation, make sure that the Busy flag is set to 0.

3. Issue a Specify Command instruction (DOA) with no flag command, using the appropriate accumulator bits to select a drive, a Write command, and head and sector address.
4. Issue a Specify Memory Address instruction (DOB) with no flag command, using the appropriate accumulator bits to specify the address of the first memory location that contains the write data blocks.
5. Issue a Specify Word Count instruction (DOC) with a Start command. Use the accumulator bits to specify the number of sectors to be transferred (two's complement). The Start command sets the Busy flag to 1, sets the Done flag to 0, and initiates the Write operation.

The controller first transfers all 256 words of the first sector to be written, one word at a time, from the computer's memory bank to the sector buffer via the data channel facility. Each time a word is transferred, the memory address register, and word count register are each incremented by one. When the transfer is complete, the controller prepares to record the data on the disk.

The controller now locates the starting sector and checks the address field as it does for a Read operation. If the address check is successful, the controller fetches and disassembles the 16-bit data words from the buffer and the drive records the serial data stream. The controller calculates a CRC word as the transfer proceeds. When all 256 words are written, the final checkword is appended to the data block.

The remaining sectors are transferred in a similar manner. When all sectors are written, the Busy flag is set to 0, the Done flag is set to 1, and a program interrupt request is initiated.

6. After the Write operation is completed on the selected drive, issue a Read Status instruction (DIA) with a Pulse command and check the Error flags. If a recoverable error occurred, retry the transfer.

I/O Timing

Several factors determine the time necessary to access and transfer data blocks to or from the disk drive. These factors are broadly grouped as (a) recalibrate or seek time and (b) read or write time, and are the subject of this discussion.

Recalibrate Or Seek Time

The read/write heads must be positioned in the proper cylinder before a data transfer can begin. The following factors determine the time necessary to seek a specified cylinder or recalibrate the positioner to select track 0.

1. The time the computer takes to issue the Seek command and then process the

interrupt when the operation is completed (referred to as the computer's overhead time).

2. The time the controller takes to initiate the Seek operation and the program interrupt request (referred to as the controller's overhead time): 1 ms.
3. The time the positioner takes to move the heads to the specified cylinder: 19 ms for a minimum seek, 68 ms for an average seek and 122 ms for a maximum seek.

The time necessary to execute a Recalibrate operation depends on the position of the heads when the Recalibrate command is issued. Thus, a Recalibrate operation could take from 19 ms to 5.7 seconds, to which 1 ms must be added for overhead time.

Read Or Write Time

The time necessary to read or write information on the disk depends on its rotational position when the transfer is initiated, as well as the number of sectors to be transferred. The following factors determine read/write time.

1. The time the computer takes to issue the Read or Write command along with a starting memory address, disk address and word count, and then process the interrupt when the operation is completed (referred to as the computer's overhead time).
2. The time the controller takes to initiate the read or write operation and the data channel operation, and the program interrupt request (referred to as the controller's overhead time): less than 1.2 ms.
3. The time the disk takes to rotate to the selected sector, once the controller initiates the Read operation or completes the data channel transfer for a write operation: variable, averaging 8.33 ms.
4. The time necessary to read the header and then transfer the data block and CRC word: 936 μs.
5. The time necessary to transfer the data across the data channel: less than 4 ms for a read operation or less than 3.5 ms for a write operation, provided no higher priority devices interfere.

Thus, the minimum total time to transfer a single sector is less than 6.2 ms (excluding the computer's overhead time) for a read operation or 5.7 ms for a write operation.

The factors that determine the minimum total time for a Format operation are the same as those for a Write operation.

NOTE *Since data channel transfers occur between sectors on a multiple sector transfer, the subsystem can transfer at best only every seventh physical sector.*

Powering Down

It is suggested that prior to powering down a system with 15 Mbyte drives, the heads be positioned to cylinder 329, a designated safe shipping/landing zone, to reduce wear on the media's active surface area. This precaution is not required with the 38.6 Mbyte and 71.2 Mbyte drives as the heads are automatically positioned to the landing zone upon power down.

Release the disk subsystem from the host's operating system before powering down the host system. Since the controller board and the disk drive both receive their power from the host system, they are automatically powered down with removal of power on the host system.

Reformatting a Disk

CAUTION *To preclude any loss of data, never reformat without first backing up the entire disk. Also, reformat* ***only*** *those track(s) with a problem, taking care to include the bad sectors flagged by the factory (see bad sector log on the drive unit). This is important since the instrumentation used during factory formatting can detect marginally bad sectors. With each reformatting operation, the bad sector log on the drive unit should be updated to list the newly flagged bad sectors.*

The format delineates an address field and a 256-word data field in each sector of every data track on the recording disk. The address field of a sector is a coded header that precedes the data block. The format records the field at a specific location within the sector to give the read and write control circuits enough time to initialize and settle before the field is read.

The disk drive uses a *soft sector* technique to locate sectors in which the controller reads address fields until it finds the one with the desired track, head, and sector address. Two CRC bytes test the validity of the address information. Since the soft sector method requires formatting an entire track at once, individual sectors cannot be reformatted.

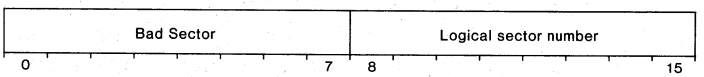
Each disk is completely formatted before it leaves the factory. Reformatting should not be performed unless a problem develops and then should be performed only on the affected track. If a particular sector becomes bad, the recorded data must be recovered (either from the disk itself or from previously recorded backup media) and the whole track should then be reformatted.

The formatted program, part of the disk reliability program (DGC No. 095-003239), is available on diskette and its operation is described in a companion document (DGC No. 096-003239). Bear in mind that whenever any sector or track is reformatted, the previously recorded information is lost.

The disks are soft sectored, meaning that there is no physical reference point for each sector. A particular sector is found by reading all sector headers until the one desired is found. Special MFM-illegal address marks are written to differentiate header fields from data and to mark the beginning of the data field. These headers with their address marks are written during the initial formatting and are never written again in normal operation. (Data field address marks are written every time a data field is written.) Formatting must be done a track at a time. An Index pulse from the drive tells the controller when to begin and end the format operation.

For a format operation, the controller generates most of the data written; the host CPU provides the sequence of sectors and determines whether or not the sector is bad. The memory buffer should therefore contain 17 words (one for each sector) with the least significant byte of each word being the sector number (0-20 octal) and the most significant byte the Bad Sector flag. The DOC should be set to -256 for all format operations.

The format of the sector address header is shown below, where a good sector equals 0 and a bad sector equals 80 hexadecimal.



Since the controller performs internal mapping, the format buffer should be set up with the sector numbers from 0 to 20 octal in numerical sequence. Note that if a sector is to be set bad after a track has been formatted, all sectors in that track must first be read to determine if any other sectors are bad. If additional sectors are bad, they must again be set bad because a track format operation rewrites all previous information on the track. (Refer to the opening cautionary note.)

In reformatting to flag a bad sector, seek to the appropriate track and issue a format command, specifying the head with the DOA register. The format operation is outlined below.

1. Position the heads to the appropriate cylinder.
2. Set up the format buffer in memory as described above.
3. Specify the appropriate head with the DOA register.
4. Initiate the format operation by issuing a DOAS, specifying a format command.
5. Repeat steps one through four for other heads and/or tracks as required, heeding the cautionary note that opened this subsection.

NOTE *The logical sector number read from the controller must be translated to the physical sector number for the format data.*

Error Conditions

This section defines the disk subsysem's error conditions. Error conditions are monitored by reading the status register. The error flags are valid until cleared by a Clear, or IORST command.

Not OK If 1, indicates that the controller failed its self-test after a power-up operation. This bit resets when the controller passes its self-test diagnostic.

Not Ready If 1, indicates that the drive is not ready to accept commands. This may be because the drive is not up to speed, not selected (or wrong drive selected), or there is a fault present in the drive.

Seek Error If 1, indicates that the Track 00 signal failed to assert during either a recalibrate or a seek operation and the controller cannot determine the current head location. This error is also set if a Seek command is issued with a track address greater than the maximum. To recover head position, reissue the recalibration command and, if successful, continue with the normal operational sequence.

Write Fault If 1, indicates that a condition exists at the drive that causes improper writing on the disk. Three conditions can cause this fault: (1) write current in a head without write gate active or no write current in the head with write gate active and drive selected; (2) multiple heads are selected; or (3) dc voltages in the drive are grossly out of tolerance.

When this error occurs, data on the disk may have been damaged and, in general, the operation should not be retried.

Address Error If 1, indicates that (1) the controller was unable to find the sector desired or data was not found following the address; (2) a Read or Write command was issued with a head or sector address greater than the maximum; (3) an attempt was made to transfer a sector past the end of the current cylinder; or (4) the Bad Sector flag (bit 15) is set.

Checkword Error If 1, indicates that the checkword read from the current sector did not match the checkword calculated by the controller during a read operation.

Operation Time-Out If 1, indicates that the specified operation failed to complete within a reasonable time (approximately 11 seconds).

Bad Sector If 1, indicates that the last sector accessed is unreliable for data storage and was flagged bad by the formatter program. Also causes address error to be set.

3

Electrical Interfacing

This chapter describes interconnections among components of the disk subsystem, which receives power and communicates with its host CPU via a 96-pin DIN connector on its backpanel. A second DIN connector on the opposite side of the backpanel transfers power and communication to the next module in the system.

The disk controller card receives power and communication via its b edge-connector, which plugs into the backpanel. The disk controller card communicates with the disk drive unit through a cable that connects to the card's A edge-connector. This cable also leads to a connector on the module's rear bulkhead panel (used when a second drive is configured). On the disk drive unit, the signal cable joins with two connectors on the drive's read/write card. Power to the drive unit is distributed from the backpanel via a cable that connects to the read/write card as well.

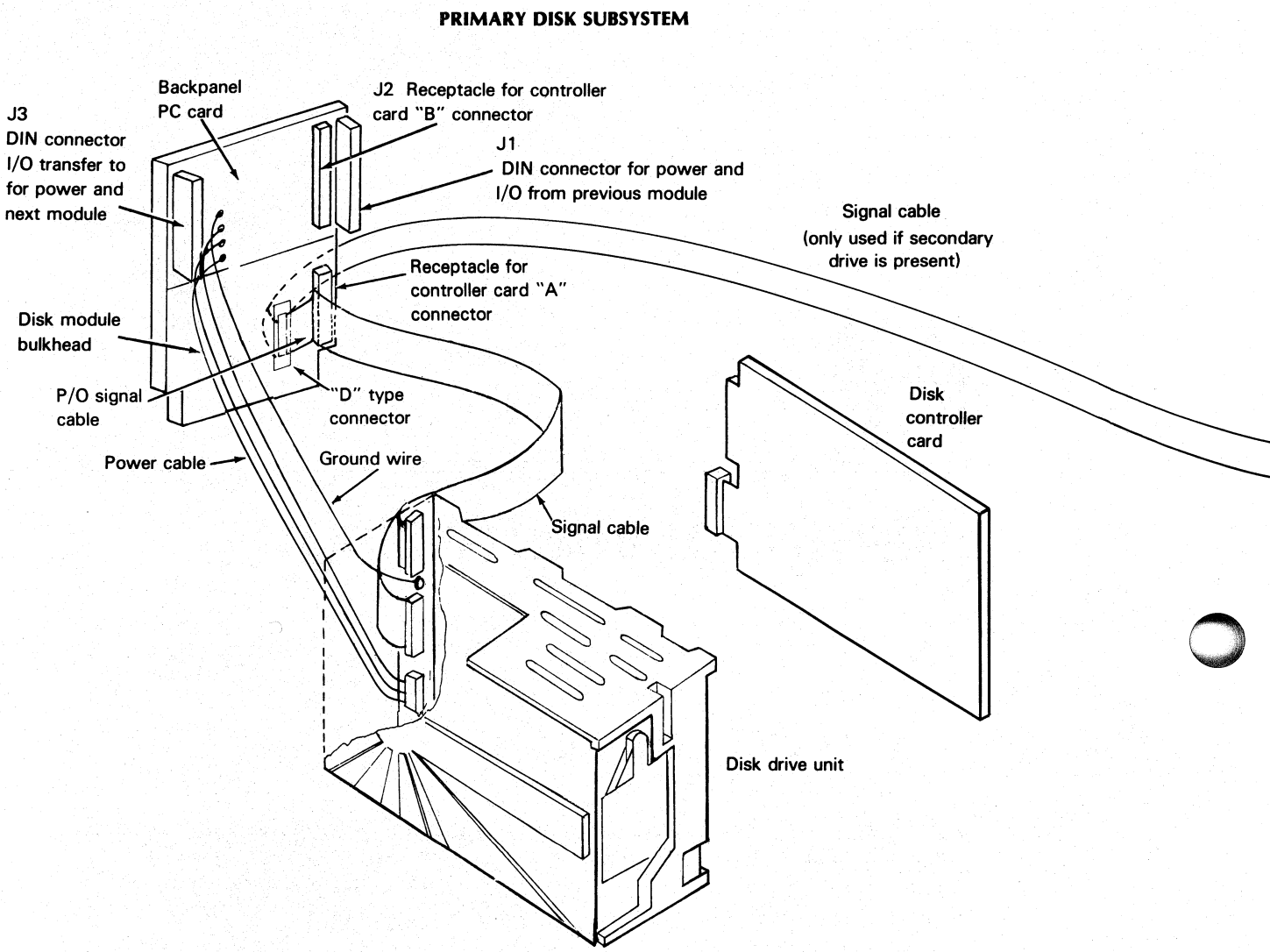
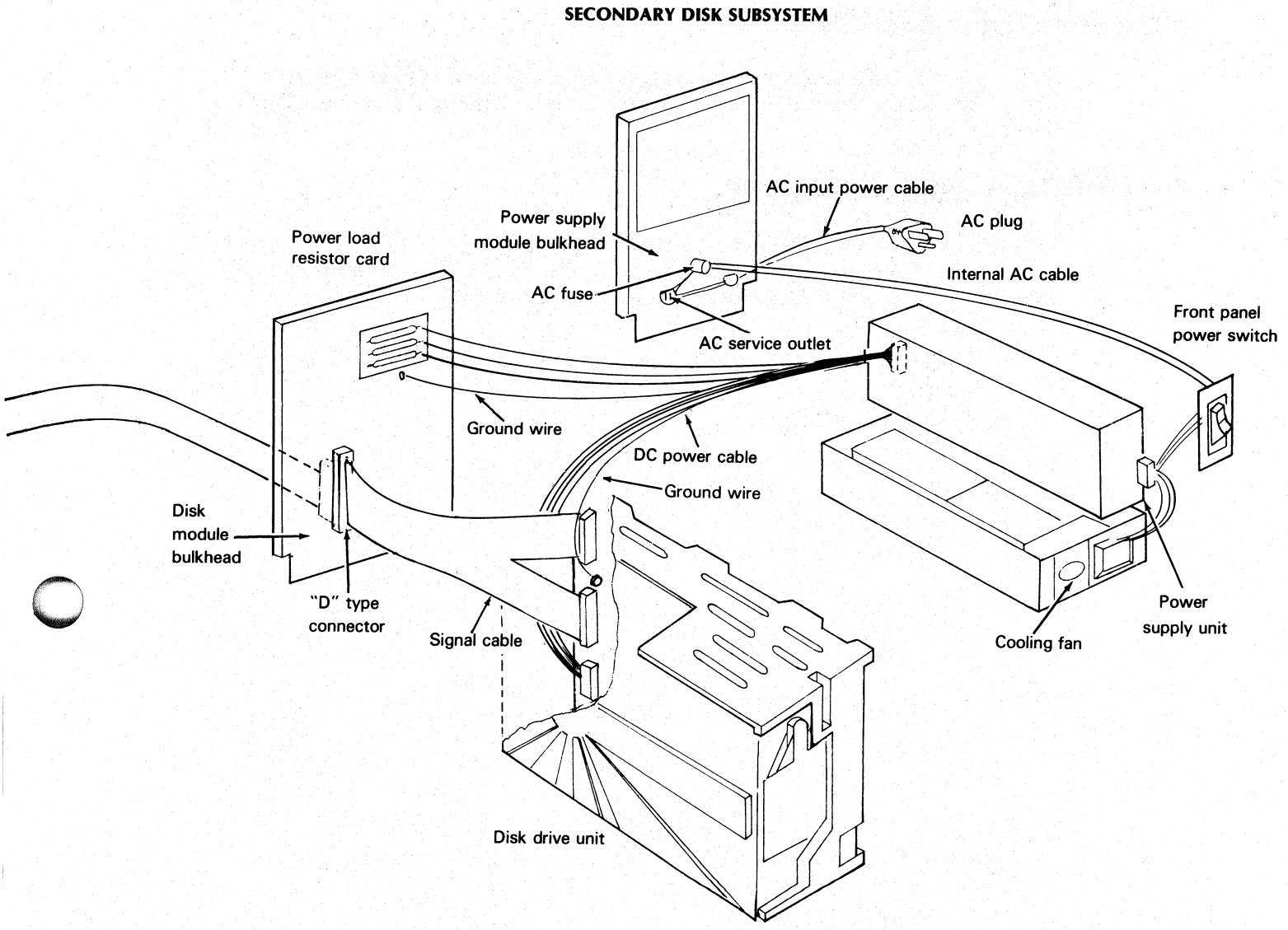


Figure 3-1 Disk subsystem interconnections



DG-26484

Figure 3-1 Disk subsystem interconnections

Power Requirements

Power requirements for the disk subsystem models are listed in Chapter 1.

Unit Interconnections

Figure 3-1 shows the interconnections between the various components of the disk subsystems. For more detailed information about interconnections, refer to Appendix B.

Installation and Tailoring

For information on installing and configuring the disk subsystems into a Desktop Generation system, refer to the appropriate installation manual for your Desktop Generation computer. (The Preface lists the manuals related to this one.)

Theory Of Operation

4

This chapter describes the functional operation of the disk controller card, which controls operation of the drive unit and provides the interface and communications link with the host system. The controller logic is based on four major integrated circuit (IC) elements: an input/output bus controller (IOC), an internally-programmed, 8-bit microprocessor (interface controller CPU), a DCH/RAM controller, and a programmable, byte-oriented, disk controller (HDC). Associated circuitry provides required support functions such as counters and registers.

Major Elements

The functional integration of these four major elements into subsystem operations is described in the pages ahead. The discussion is based on the functional block diagram in Figure 4-1. For detailed circuit information, see the appropriate schematic drawings.

I/O Bus Interface

The I/O bus interface connects the controller logic on the card with the host computer's microI/O bus. It consists of an I/O transceiver chip, a clock driver chip, an I/O controller chip (IOC), plus data channel and interrupt priority circuits.

The I/O transceiver chip is the first element of the interface logic as seen from the I/O bus. It is essentially a bidirectional data latch that buffers the data transfer between the IOC and the I/O bus.

The IOC portion of the interface provides control for data transfer and interface functions with the host system's I/O bus. These functions include the normal interrupt, busy/done, and data channel communications that characterize the Data General microI/O bus. It also performs the parallel-to-serial and serial-to-parallel conversion of the data transferring to and from the I/O bus. The IOC decodes all instructions received from the I/O bus and determines whether an instruction is directed to the IOC or to other functional areas of the card. The IOC internally responds to the following instructions.

Interrupt Acknowledge (INTA)

I/O Skip (SKP)

Load Memory Address Register (DOB)

Load Word Count Register (DOC)

Mask Out (MSKO)

I/O Reset (IORST)

No I/O Transfer (NIO)

Further instruction decoding is performed by the Function Decoder. The Function Decoder decodes a 4-bit code received from the IOC into one of eleven individual control signals. These control signals provide support functions for the various programmed I/O and data channel operations.

The DCHR (data channel request) and interrupt priority circuits implement the Data General I/O priority scheme for both data channel and interrupt requests. This scheme provides priority according to the physical (slot) location in the logic chassis in respect to the CPU. The I/O controller physically closest to the CPU has the highest priority. The interrupt priority can be altered by a Mask-Out (MASKO) instruction used by the host CPU to selectively inhibit interrupt requests. This instruction identifies the device(s) to be masked by the accompanying bit pattern.

The integration of the I/O bus interface into overall controller card functions is further described in the description of data channel operation.

Interface Controller CPU

The interface controller CPU is an 8-bit microprocessor (8049) with its own self-contained program memory (2K x 8 ROM) and a 128 x 8 RAM. It is clocked by an external 5 MHz clock.

Functionally, the interface controller responds to commands from the host system and initiates the appropriate responses. It supervises overall controller operations and provides direct selection of drive and head functions.

The interface controller CPU is initialized by an I/O Reset instruction (IORST) from the host CPU. This instruction interrupts the controller, which then executes its initialization subroutine. The IORST also sets the IPL (initial program load) flag to 1, causing the controller to execute an IPL subroutine following the initialization. This subroutine reads a low-level bootstrap program from track 0 of head 0 on disk 0 (if more than one disk is in system) and transfers it out to the host via the data channel facility.

Read, Write, Seek, and similar commands to the interface controller CPU are DOA instructions, which are loaded into the A Register in the DCH/RAM controller chip. When these commands are accompanied by a Start command, they also set the Busy flag to 1 in the IOC.

When waiting for a command from the host, the interface controller CPU polls the IOC for an active Busy condition. When a Busy condition is detected, the interface controller CPU issues two sequential commands to transfer the contents of the A Register into the controller. Each command transfers one byte of the 16-bit command word; the most significant byte transfers first.

The interface controller CPU communicates status back to the host by writing status information into the status register. The host reads this information with a Read Status instruction (DIA), which reads the contents of the status registers and Read Status Gates into the IOC for transfer to the host.

The controller responds to the host command with appropriate instructions to either the drive unit or the disk controller chip.

DCH/RAM Controller

The DCH/RAM controller chip handles data transfers between the disk controller chip and the sector buffer RAM and between the sector buffer RAM and host memory (via the I/O bus interface). The latter transfers utilize data channel protocol to manage the data transfer activities.

The DCH/RAM controller consists of three registers (A, C, and D) and associated control circuitry. The A register is a 16-bit register used during a write to disk operation to buffer data being transferred from the IOC into the sector buffer. After being loaded, the register is read out in two sequential 8-bit bytes into the sector buffer. The A register is also used to buffer the transfer of host initiated commands from the IOC to the interface controller CPU.

The C and D registers are 8-bit registers used during a read from disk operation to buffer data being transferred from the sector buffer to the IOC. The registers are loaded sequentially. First the high order byte is loaded into the D register; then the low-order byte into the C register. The data is then read out to the IOC as one 16-bit word. Alternatively, these registers can be loaded by commands from the interface controller CPU and read out to the IOC upon command (DIC) from the host. Refer to the diagnostic command description in Appendix A.

The C register is also used during disk read operations to buffer the data transfers between the disk controller chip and the sector buffer RAM. A Buffer Data Request (BDRQ) signal from the disk controller chip loads the data into the C register, from which it is written into the sector buffer RAM.

During disk write operations, the data is transferred directly from the RAM to the disk controller, with memory control provided by the DCH/RAM controller chip. Each transfer is initiated by a BDRQ signal from the disk controller.

An important function of the DCH/RAM controller is to provide appropriate memory control signals for accessing the sector buffer RAM. Addressing is provided by an address counter, which is incremented with each byte transferred. At the beginning of each sector transfer operation, whether writing into the RAM or reading from it, the address counter is reset to zero by the disk controller.

Data channel requests $\overline{\text{DCHSYNC}}$ to the IOC are automatically initiated upon completion of a write or read operation at the sector buffer.

Upon completion of the data channel operation for a sector (signalled by the sector word counter), the DCH/RAM controller tells the interface controller CPU that it is done (asserts a $\overline{\text{DCHDONE}}$ signal). As a result, the interface controller CPU reloads the word count into the sector word counter and signals the disk controller chip to continue with the next sector.

Disk Controller Chip

The disk controller chip (WD1010) provides the control and data interface functions that are directly associated with the disk drive unit. It monitors status from the drive unit and issues head positioning and read/write control signals. Both Disk Read and Disk Write data are processed by the controller chip. Other functions include:

- CRC logic, which generates and checks the cyclic redundancy check characters appended to the ID and data fields. The polynomial is X16 + X12 + X5 + 1.
- Encode and decode of MFM data to be written to or read from the drive. Provides early/late precompensation on Write Data signal to drives for inner tracks on the disks, beginning with track 256.
- Drive interface logic, which controls and monitors communication to and from the drive. Includes head positioning signals: Step and Direction.
- Serial/parallel data conversion and buffering between parallel M0-7 bus and serial read/write data interface with drive.
- Control logic, which generates an Interrupt Request (INTRQ) signal that advises the interface controller that a command is completed. It also generates a Buffer Data Request (BDRQ) signal, which requests the DCH/RAM controller to transfer data between the sector buffer and the disk controller chip.

Prior to any operation by the disk controller, it must first be programmed by the Interface Controller CPU with the appropriate parameter information. It is then issued the command for the specific operation to be performed. The Interface Controller CPU can check drive and controller operations by reading status from the disk controller.

After completing the operations implicit in a command, the disk controller chip indicates that it has completed its operations by asserting the INTRQ signal to the Interface Controller CPU.

Subsystem Operations

The following paragraphs describe the normal sequence of operations for typical disk functions: data channel operations, seek track, read disk, and write disk functions.

Data Channel Operations

Data channel (DCH) operations must first be set up by the host CPU before a Read Disk or a Write Disk command is issued. To start a data channel operation, the host issues

1. Specify Word Count instruction (DOC), which loads the total number of words to be transferred into the IOC's word count register and also loads the sector count portion of the word count (most significant byte) into the sector count register.
2. Specify Memory Address instruction (DOB), which loads the memory address for the first data channel transfer into the IOC's memory address register.
3. Specify Command instruction (DOA), for either a read disk or a write disk operation. The instruction specifies the drive, the track (cylinder) number, and the sector number.

The interface controller CPU responds to the host's commands in the following manner:

1. Reads the sector count from the sector count register and uses this count to determine the number of times it initiates a read sector or write sector operation.
2. Loads the word count for a full sector transfer (256 words) into the sector word counter.
3. Conditions the disk controller chip and issues the appropriate read or write command for each sector transfer.
4. Defines the data channel direction bit (IOC0) that the IOC appends to the memory address word.
5. Issues a Start DCH command to the DCH/RAM controller chip.
6. Upon completion of a sector transfer, a DCHDONE signal from the DCH/RAM controller tells the interface controller CPU that the transfer is completed. If more sectors are still to be transferred (sector count not equal to 0), the interface controller CPU initiates a new sector transfer. After the last sector has been transferred, the CPU signals the IOC, which sets the Done flag to 1 and and resets the Busy flag to 0.

During data channel transfers, the I/O bus interface provides the data link between the DCH/RAM controller chip and the host system's I/O bus. After a data channel operation has been initiated by the interface controller CPU, the DCH/RAM controller requests each individual word transfer by asserting the $\overline{\text{DCHSYNC}}$ signal to the IOC. In turn, the IOC initiates a DCH request to the host system.

Assuming that the disk subsystem currently has priority on DCH requests, the host responds with a Data Channel Address Request, which in the IOC initiates a $\overline{\text{DCHA}}$ signal to the DCH/RAM controller chip and also tells the IOC to transmit the 15-bit memory address plus direction bit (0) to the host.

If it is a data channel *out* operation for the host, the host transmits the data word to the IOC and the IOC generates a $\overline{\text{DCHO}}$ signal to the DCH/RAM controller chip. The $\overline{\text{DCHO}}$ loads the data word into the A register. From the A register, the data word is transferred to the sector buffer RAM.

A data channel *in* operation is similar in protocol to the data channel *out* described above. The primary difference is that the direction bit (IOC0) to the IOC is 0 and the C and D registers in the DCH/RAM controller chip are used to buffer the transfer and assemble the two bytes into a 16-bit word; also, a $\overline{\text{DCHI}}$ controls the transfer instead of the $\overline{\text{DCHO}}$.

Upon completion of a sector transfer (flagged by the sector word counter), the DCH/RAM controller asserts a DCHDONE signal to tell the interface controller CPU that the sector transfer operation is complete.

Seek Track Operations

Seek track (cylinder) operations are initiated by an explicit command from the host or an implied command inherent in a Recalibrate instruction. In performing a Seek operation, the interface controller CPU first defines the cylinder number to the disk controller chip and then issues a Seek command to initiate the action. The disk controller chip performs head positioning (seek) operations as follows:

- All head movement is specified to the drive as step pulses. Another signal line defines the direction in which the heads are to move. The drive returns a Seek Complete status signal when it has completed a head positioning operation. Each step pulse moves the heads one cylinder position, either toward the center (away from track 0) or away from the center (toward track 0).
- A normal seek steps the heads from their current position to the cylinder specified.
- A recalibrate steps the heads to track (cylinder) 0.

Read Disk Operation

In response to a Read command from the host, the interface controller CPU first issues the appropriate head positioning instructions to the disk controller chip, as described under "Seek Track Operations". Then it programs the disk controller chip with the sector count, starting sector number, sector size, drive number, and head number. The actual read operation is initiated with a Start command to the controller.

As the modified frequency modulation (MFM) encoded data is received from the drive, it is synchronized by phase-lock loop logic in the read data circuits to convert it into a serial bit stream with logic levels useable by the disk controller chip.

When the disk controller chip has a byte assembled, it issues a Buffer Data Request (BDRQ) to the DCH/RAM controller. This device responds by first loading the byte into its C register and then writing it into the sector buffer RAM. As the data transfers through the disk controller, a check word (CRC) is

generated. At the end of the sector transfer, this check word is compared with the CRC word that is read from disk. If the check words do not match, the Check Error flag is set to 1.

After a full sector of data has been read and loaded into the sector buffer, the disk controller asserts its interrupt request line to the interface controller CPU. This device, in turn, provides direction information to the IOC. The data channel operation is started by the interface controller CPU, which issues a Start DCH command to the DCH/RAM controller chip.

Write Disk Operation

A write disk operation is essentially a read operation in reverse. Data from the host must be transferred into the sector buffer and then read out to the disk controller. Upon receiving a write command from the host, the interface controller CPU writes the sector word count into the sector word counter and defines proper transfer direction by setting the direction bit (IOC0) to 1. Again, the data channel operation is initiated by a command from the interface controller CPU.

When the host has completed the transfer of a full sector of data to the sector buffer, the interface controller CPU issues a Write command to the disk controller chip. (Prior to issuing the command, the interface controller CPU prepares the disk controller for drive operation, just as it does before a Read command.)

Upon receiving a Write command, the disk controller chip asserts the BDRQ line to the DCH/RAM controller to initate the reading of a byte of data from the sector buffer into the disk controller chip. This byte of data is transformed to serial format and converted to modified frequency modulation form by the write data circuits, which also insert precompensation for writing to the inner tracks. The write data signal is then sent to the drive unit.

Subsequent data bytes are similarly transferred and written to disk. The controller calculates a CRC word as the transfer proceeds. When all 256 words for a sector are written, the final check word is appended to the data block. Upon completion of the sector, the disk controller again asserts its INTRQ line to the interface controller CPU.

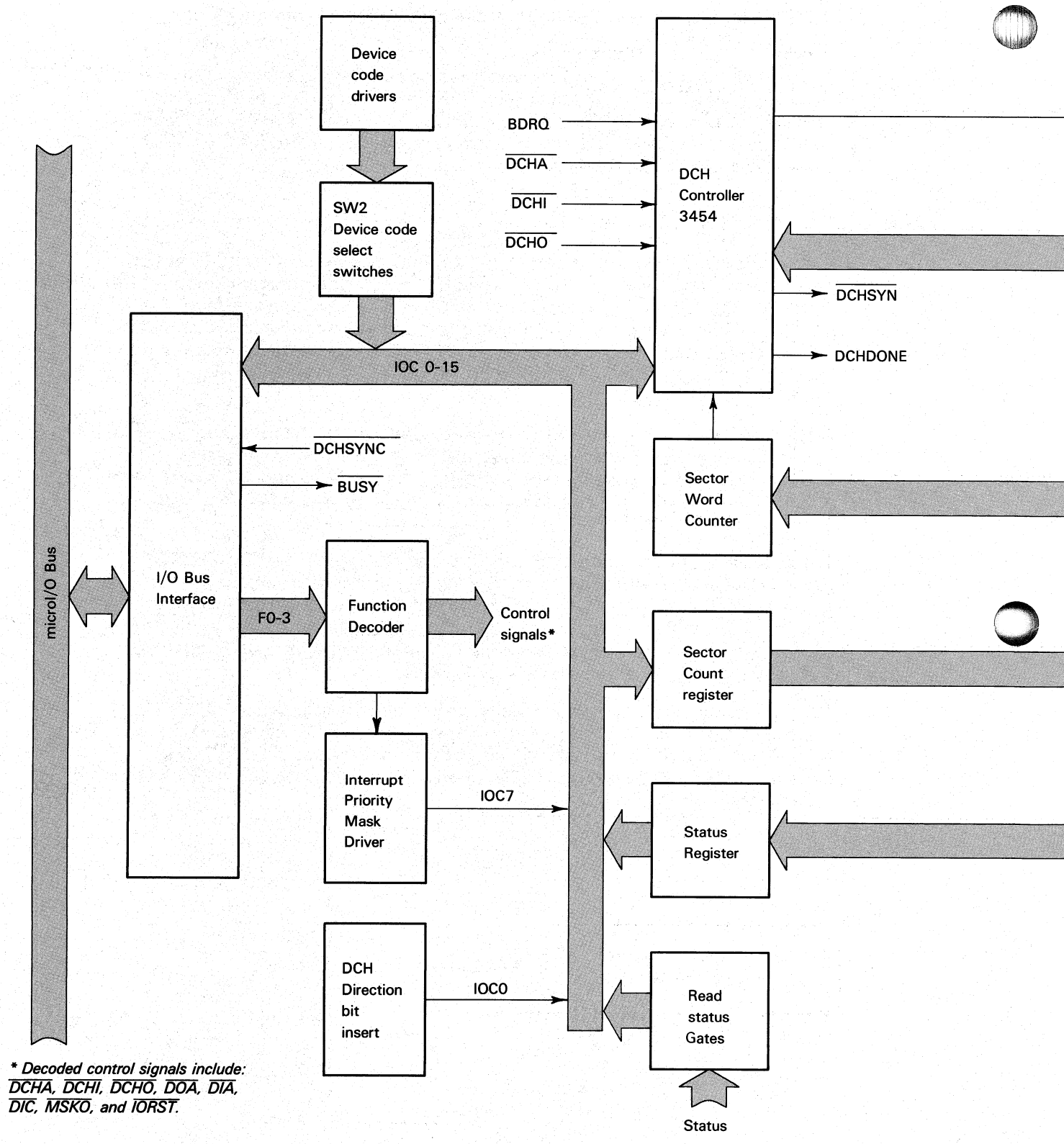
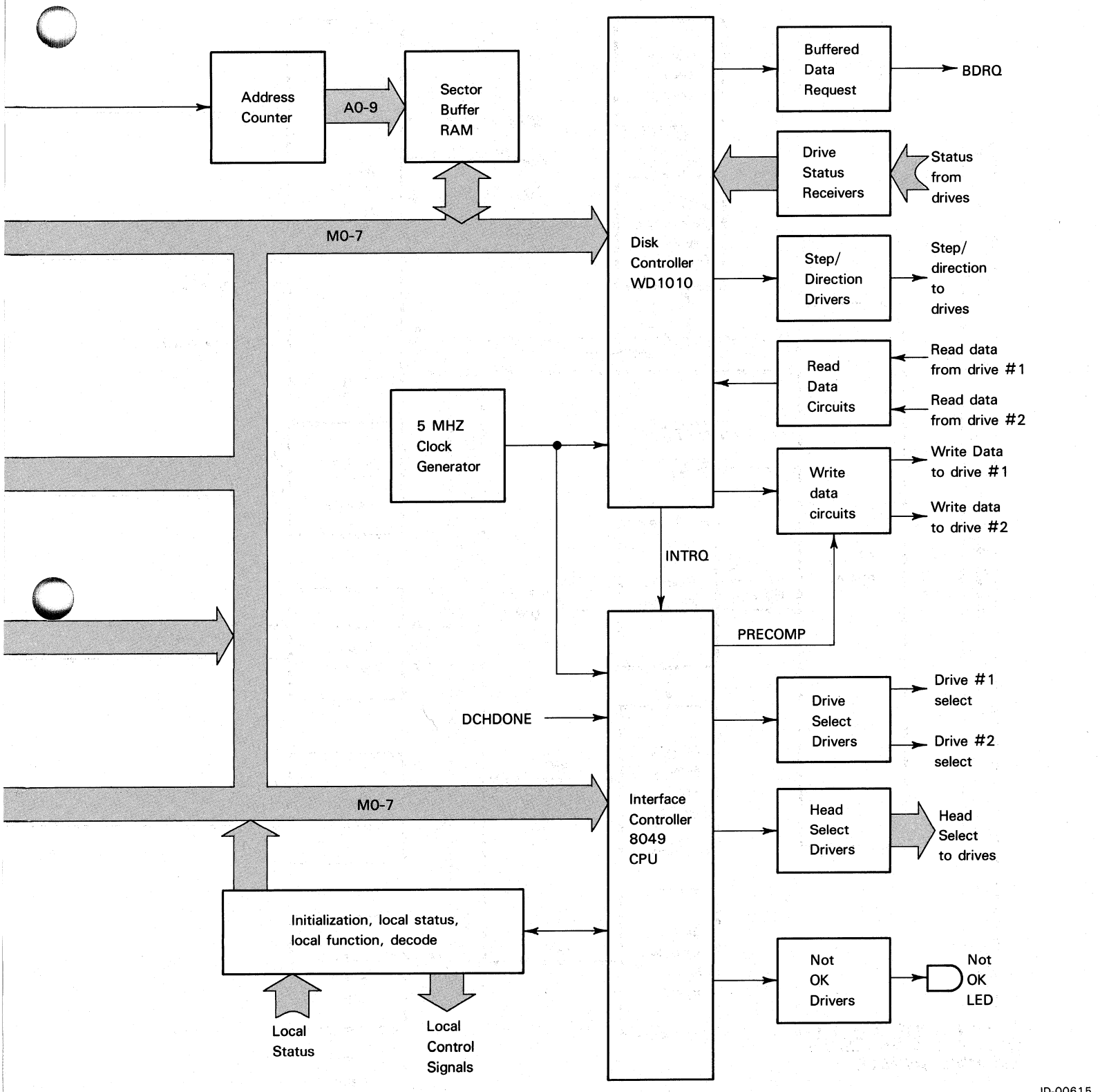


Figure 4-1 Disk controller board functional block diagram


Address Counter
A0-9
Sector Buffer RAM
M0-7
Disk Controller WD1010
Buffered Data Request
BDRQ
Drive Status Receivers
Status from drives
Step/ Direction Drivers
Step/ direction to drives
Read Data Circuits
Read data from drive #1
Read data from drive #2
Write data circuits
Write Data to drive #1
Write data to drive #2
5 MHZ Clock Generator
INTRQ
PRECOMP
DCHDONE
Drive Select Drivers
Drive #1 select
Drive #2 select
Interface Controller 8049 CPU
Head Select Drivers
Head Select to drives
M0-7
Initialization, local status, local function, decode
Not OK Drivers
Not OK LED
Local Status
Local Control Signals

ID-00615

Diagnostic Commands and Flags

A

If the disk subsystem needs troubleshooting, use the following information as an aid in understanding the diagnostic programs. This appendix explains the special operations that can be carried out under program control. However, this section does not explain how the commands are used or how the hardware works.

Diagnostic operations are selected by the function field of the command register when a diagnostic command is specified. They override other commands and may redefine the accumulator formats of the programming instructions.

The diagnostic commands are encoded in bits 11-15 of the Specify Command instruction (DOA). These commands are listed in Table A-1. Their functions are defined in Table A-2.

Table A-1 Diagnostic commands

Bits 11-15	Diagnostic Command
00000	NOP
00001	NOP
00010	NOP
00011	Read Drive Type Bits
00100	Write DIA Bits 8-15
00101	Seek To Diagnostic Track
00110	Seek To Landing Zone
00111	Start Data Channel Operation
01000	Test Index Timing
01001	NOP
01010	NOP
01011	Read Control Program Revision Number
01100	Read Current Track Address
01101	NOP
01110	Inititate Continuous Cycle
01111	NOP
10000	Write WD1010 Sector Count Register
10001	Write WD1010 Sector Number Register
10010	Write WD1010 Track Low Register
10011	Write WD1010 Track High Register
10100	Write WD1010 SDH Register
10101	Read WD1010 Status Register
10110	Read WD1010 Error Flag Register
10111	Read WD1010 Sector Count Register
11000	Read WD1010 Sector Number Register
11001	Read WD1010 Track Low Register
11010	Read WD1010 Track High Register
11011	Read WD1010 SDH Register
11100	Read DOA Bits 8-15
11101	Read DOA Bits 0-7
11110	Read Self-Test Results
11111	Run Self-Test

Table A-2 Diagnostic command functions

Command	Function
NOP	No operation is performed. The done flag is set to 1.
Write DIA Bits 8-15	Bits 0-3 and 7-10 of the DOA are returned in bits 8-15 of the DIA, bits 0-7 of the DIC, and bits 8-15 of the DIC.
Read DOA Bits 0-7	Bits 0-7 of the DOA are returned in bits 8-15 of the DIA.
Read DOA Bits 8-15	Bits 8-15 of the DOA are returned in bits 8-15 of the DIA.
Read Drive Type Bits	Bits 12-15 of the DIA return identify the drive type as follows. **12 13 14 15 Drive Type** 1 1 1 1 5-Mb, type A (not used) 1 1 1 0 15-Mb, type A (normally used) 1 0 1 1 5-Mb, type B (not used) 1 0 1 0 15-Mb, type B (not used) 0 1 1 1 5-Mb, type C (not used) 0 1 1 0 15-Mb, type C (not used)
Read Control Program Revision Number	The revision number of the firmware in the 8049 microprocessor is returned in bits 8-15 of the DIA.
Read Current Track Address	The current track address for the selected drive is returned in bits 0-15 of the DIC.
Seek To Diagnostic Track	The selected drive is recalibrated and then a seek to the diagnostic track (Track 305) is performed.
Seek To Landing Zone	The selected drive is recalibrated and then a seek to the landing zone is performed.
Start Data Channel	Prior to this command, the DOB register should be loaded with a memory buffer address and the DOC with -256. If bit 8 of the DOA is a 1 when the command is issued, words are transferred from the host memory to the controller buffer. If bit 8 of the DOA is 0, words are transferred from the buffer to the host.
Test Index Timing	The timing of the index on the selected drive is checked to approximately ± 5 percent of nominal. If this timing is out of specification, a Seek error (DIA bit 10) is set. If the selected drive does not exist or is not ready, the Not Ready error flag is set.
Initiate Continuous Cycle	Once this command is issued for the selected disk, the controller will continuously seek to track 0, read sector 0, head 0 without data channeling; seek to track 128, read sector 0, head 0 without data channeling, and so on until it encounters a Read error or receives an IORST or Clear. If an error occurs, the Done flag will be set and the error status will be presented in the DIA.

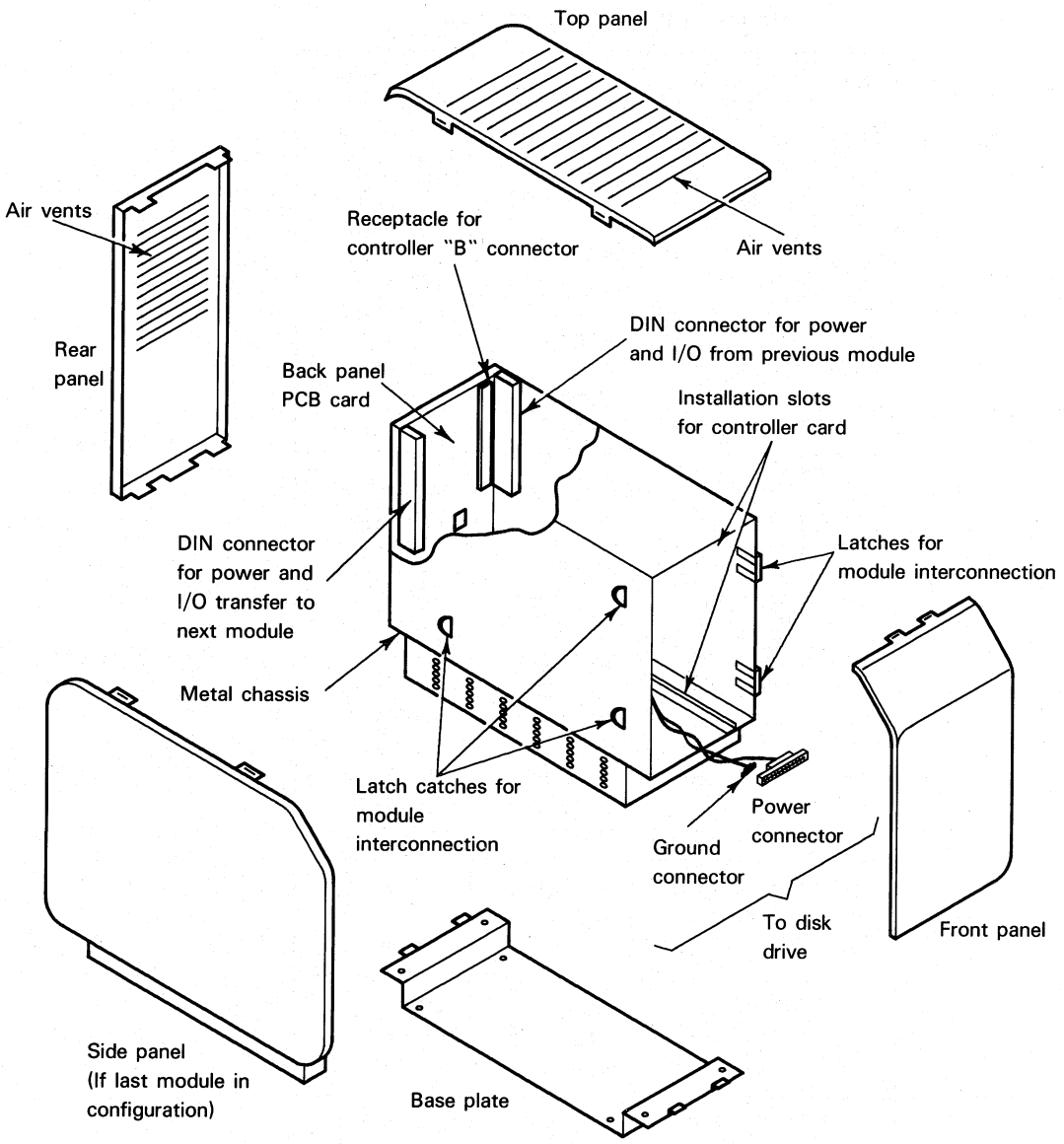
Table A-2 Diagnostic command functions (cont.)

Command	Function
Write WD1010 Count Register	Sector Bits 0-3 and 7-10 of the DOA are written to this register.
Write WD1010 Sector Number Register	Bits 0-3 and 7-10 of the DOA are written to this register.
Write WD1010 Track Low Register	Bits 0-3 and 7-10 of the DOA are written to this register.
Write WD1010 Track High Register	Bits 0-3 and 7-10 of the DOA are written to this register.
Write WD1010 SDH Register	Bits 0-3 and 7-10 of the DOA are written to this register (sector size, drive select number, head select number).
Read WD1010 Status Register	Bits 7-0 of this register are returned in bits 8-15 of the DIA.
Read WD1010 Error Register	Bits 7-0 of this register are returned in bits 8-15 of the DIA.
Read WD1010 Sector Count Register	Bits 7-0 of this register are returned in bits 8-15 of the DIA.
Read WD1010 Sector Number Register	Bits 7-0 of this register are returned in bits 8-15 of the DIA.
Read WD1010 Track Low Register	Bits 7-0 of this register are returned in bits 8-15 of the DIA.
Read WD1010 Track High Register	Bits 7-0 of this register are returned in bits 8-15 of the DIA.
Read WD1010 SDH Bits Register	Bits 7-0 of this register are returned in bits 8-15 of the DIA.
Read Self-Test Results	DIA bits 8-15 contain one of the following: 0, 1, 2, or 3. These are interpreted as follows: 0 = no error 1 = failure in RAM test 2 = failure in ROM test 3 = failure in WD1010 disk controller test
Run Self-Test	A subset of the self-test run at power-up is initiated. A Not Ok status shows the results of this test.

Assembly and Internal Cabling

B

An exploded view of the modular enclosure for the disk subsystem is shown in Figure B-1. Figures B-2 and B-3 provide detailed interconnection information for the subsystem.



ID-00616

Figure B-1 Construction detail for modular enclosure

96 SOCKET DIN CONNECTOR-J3

Pin	Column A	Column B	Column C
32	+5 PS #1	+5 PS #1	+5 PS #1
31	+5 PS #1	+5 PS #1	+5 PS #1
30	+5 PS #1	+5 PS #1	+5 PS #1
29	+5 PS #1	+5 PS #1	+5 PS #1
28	+5 PS #1	+5 PS #1	+5 PS #1
27	+5 PS #1	+5 PS #1	+5 PS #1
26	GROUND	GROUND	GROUND
25	GROUND	GROUND	GROUND
24	GROUND	GROUND	GROUND
23	GROUND	GROUND	GROUND
22	GROUND	GROUND	GROUND
21	GROUND	GROUND	GROUND
20	GROUND	$\overline{\text{BMCLOCK}}$	$\overline{\text{BMCLOCK}}$
19	$\overline{\text{DCHPOUT1}}$	BI/ODATA1	BI/ODATA1
18	$\overline{\text{EXTDCHR}}$	INTPOUT1	$\overline{\text{CLEAR}}$
17	$\overline{\text{EXTINT}}$	$\overline{\text{BI/ODATA2}}$	$\overline{\text{BI/ODATA2}}$
16	GROUND	$\overline{\text{BI/OCLOCK}}$	BI/OCLOCK
15	GROUND	GROUND	GROUND
14	GROUND	GROUND	GROUND
13	GROUND	GROUND	GROUND
12	−12 PS #1	+12 PS #1	+12 PS #1
11	−5 PS #1	−5 PS #2	+12 PS #2
10	−12 PS #2	+12 PS #2	+12 PS #2
9	GROUND	GROUND	GROUND
8	GROUND	GROUND	GROUND
7	GROUND	GROUND	GROUND
6	+5 PS #2	+5 PS #2	+5 PS #2
5	+5 PS #2	+5 PS #2	+5 PS #2
4	+5 PS #2	+5 PS #2	+5 PS #2
3	+5 PS #2	+5 PS #2	+5 PS #2
2	+5 PS #2	+5 PS #2	+5 PS #2
1	+5 PS #2	+5 PS #2	+5 PS #2

J4

Ground Connector Lug

Power cable attachment

E1 0 - 12 PS #2

E2 0 - GROUND

E3 0 - GROUND

E4 0 - +5 PS #2

E5 0 - NO CONNECTION

E6 0 - GROUND

Figure B-2 Backpanel connections

Slot 1 - J2

Even Pins		Odd Pins	
60	+5 PS #2	59	+5 PS #2
58	−5 PS #2	57	+5 PS #2
56	+12 PS #2	55	+12 PS #2
54	GROUND	53	GROUND
52		51	
50		49	
48		47	
46		45	
44		43	
42		41	
40		39	−12 PS #2
38		37	
36	GROUND	35	
34		33	
32		31	
30		29	
28		27	
26		25	
24		23	
22	DCHPIN	21	DCHPOUT1
20	INTPIN	19	INTPOUT1
18		17	
16	BI/OCLOCK	15	$\overline{\text{BI/OCLOCK}}$
14	GROUND	13	BI/ODATA2
12	$\overline{\text{BI/ODATA2}}$	11	GROUND
10		9	$\overline{\text{EXTDCHR}}$
8	$\overline{\text{EXTINT}}$	7	
6	$\overline{\text{CLEAR}}$	5	$\overline{\text{BI/ODATA1}}$
4	BI/ODATA1	3	GROUND
2	$\overline{\text{BMCLOCK}}$	1	BMCLOCK

96 PIN DIN CONNECTOR-J1

Pin	Column A	Column B	Column C
32	+5 PS #1	+5 PS #1	+5 PS #1
31	+5 PS #1	+5 PS #1	+5 PS #1
30	+5 PS #1	+5 PS #1	+5 PS #1
29	+5 PS #1	+5 PS #1	+5 PS #1
28	+5 PS #1	+5 PS #1	+5 PS #1
27	+5 PS #1	+5 PS #1	+5 PS #1
26	GROUND	GROUND	GROUND
25	GROUND	GROUND	GROUND
24	GROUND	GROUND	GROUND
23	GROUND	GROUND	GROUND
22	GROUND	GROUND	GROUND
21	GROUND	GROUND	GROUND
20	$\overline{\text{BMCLOCK}}$	BMCLOCK	GROUND
19	BI/ODATA1	$\overline{\text{BI/ODATA1}}$	DCHPIN
18	$\overline{\text{CLEAR}}$	INTPIN	$\overline{\text{EXTDCHR}}$
17	$\overline{\text{BI/ODATA2}}$	BI/ODATA2	$\overline{\text{EXTINT}}$
16	BI/OCLOCK	$\overline{\text{BI/OCLOCK}}$	GROUND
15	GROUND	GROUND	GROUND
14	GROUND	GROUND	GROUND
13	GROUND	GROUND	GROUND
12	+12 PS #1	+12 PS #1	+12 PS #1
11	+12 PS #2	−5 PS #2	−5 PS #1
10	+12 PS #2	+12 PS #2	−12 PS #2
9	GROUND	GROUND	GROUND
8	GROUND	GROUND	GROUND
7	GROUND	GROUND	GROUND
6	+5 PS #2	+5 PS #2	+5 PS #2
5	+5 PS #2	+5 PS #2	+5 PS #2
4	+5 PS #2	+5 PS #2	+5 PS #2
3	+5 PS #2	+5 PS #2	+5 PS #2
2	+5 PS #2	+5 PS #2	+5 PS #2
1	+5 PS #2	+5 PS #2	+5 PS #2

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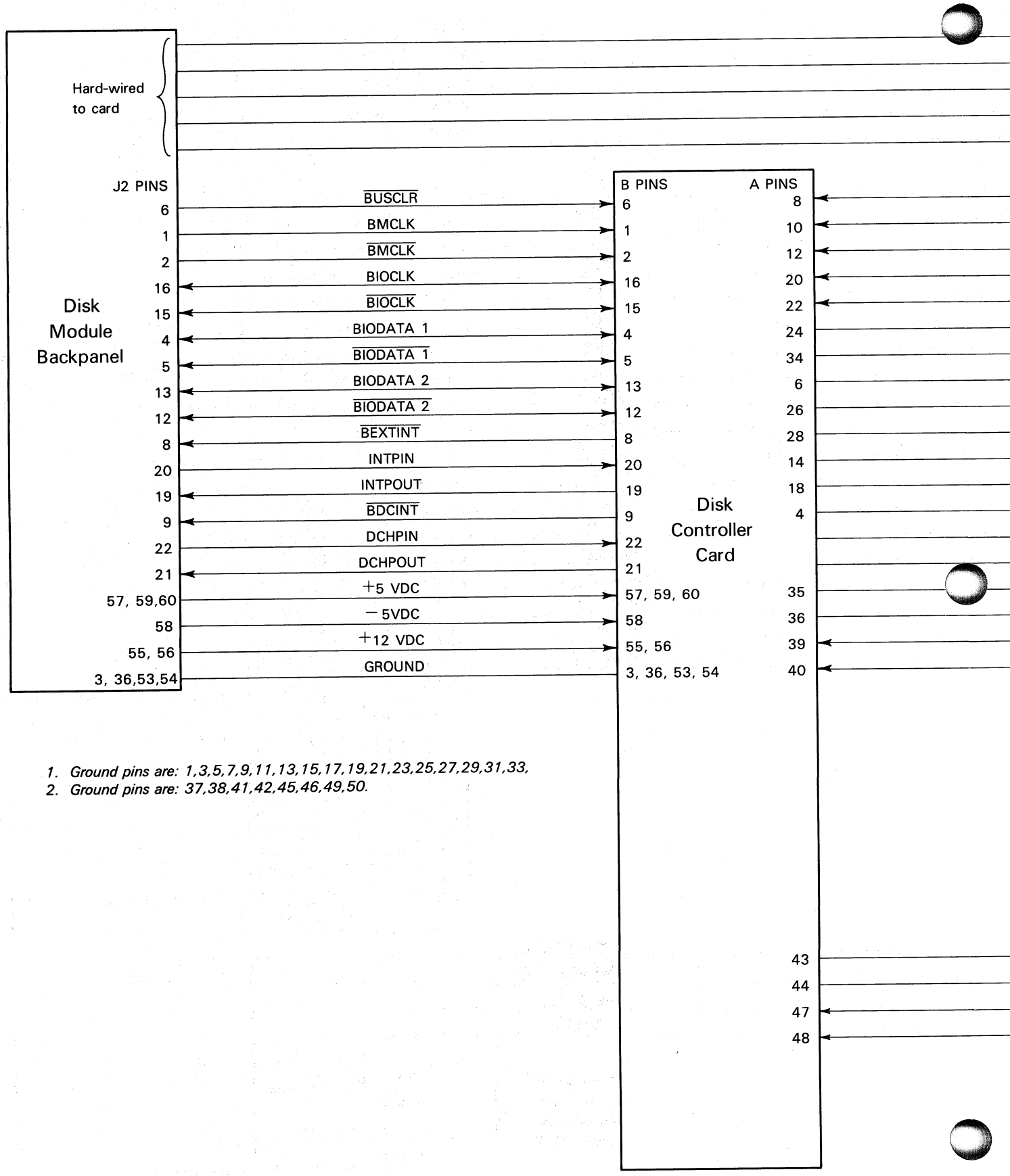
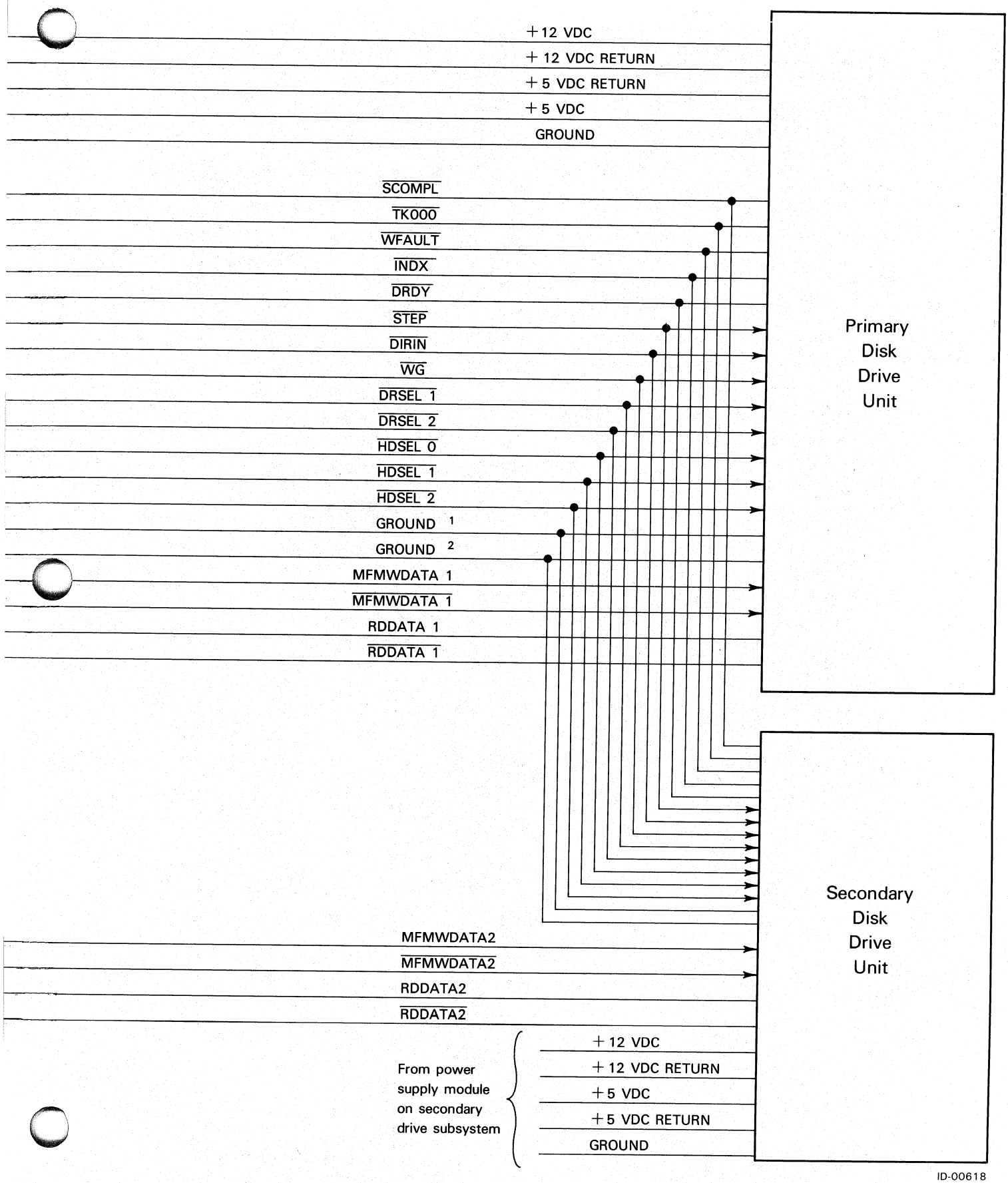


1. *Ground pins are: 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,*
2. *Ground pins are: 37,38,41,42,45,46,49,50.*

Figure B-3 Detailed subsystem interconnections


+12 VDC
+ 12 VDC RETURN
+ 5 VDC RETURN
+ 5 VDC
GROUND
SCOMPL
TK000
WFAULT
INDX
DRDY
STEP
DIRIN
WG
DRSEL 1
DRSEL 2
HDSEL 0
HDSEL 1
HDSEL 2
GROUND 1
GROUND 2
MFMWDATA 1
MFMWDATA 1
RDDATA 1
RDDATA 1
Primary Disk Drive Unit
Secondary Disk Drive Unit
MFMWDATA2
MFMWDATA2
RDDATA2
RDDATA2
From power supply module on secondary drive subsystem
+ 12 VDC
+ 12 VDC RETURN
+ 5 VDC
+ 5 VDC RETURN
GROUND

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