Reference Manual

CONTROL DATA 8528

DIGITAL COMMUNICATIONS TERMINAL

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CALL
RECEIVE
ERROR
TEST
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RESET

CHAPTER I
DESCRIPTION

The CONTROL DATA* 8528 Digital Communication Terminal is an inter-computer communication device which provides long distance serial data transfer at high speeds under program control.

Twelve bits of data are transferred between computer and terminal over standard parallel logic cables; the terminal equipments transmit and receive 24 serial bits for each 12-bit computer word. The first 12 serial bits are data; 100% redundancy is used for error detection at the receiving terminal equipment. The data and redundancy are transmitted as one 24-bit word. The serial data can be transferred on a single duplex channel by coaxial cable, microwave, or leased landline telephone.

Either party line or private line techniques can be used on as many as seven independent serial communication channels. (Logic for one channel is furnished as standard equipment; the other six are optional.) Communication networks can be expanded almost indefinitely by using combinations of the two techniques.

One audio communication facility between terminal locations is provided as standard equipment for the first channel. A test simulator for computer free maintenance is incorporated in the equipment.

PHYSICAL DESCRIPTION

CABINET

The logic chassis containing the printed circuit logic cards, power supply, blower unit, and video logic are housed in a cabinet. The cabinet is 61 inches high, 25 1/2 inches deep, 24 1/2 inches wide and weighs approximately 400 pounds. The logic chassis are slide mounted in the cabinet. There are three blowers in the cabinet; one at the base for pressurizing and two under the chassis for cooling.

Equipment operating requirements are a maximum of 400 watts of 110 volt, 60 cycle power, and a normal room temperature not exceeding 80°F.

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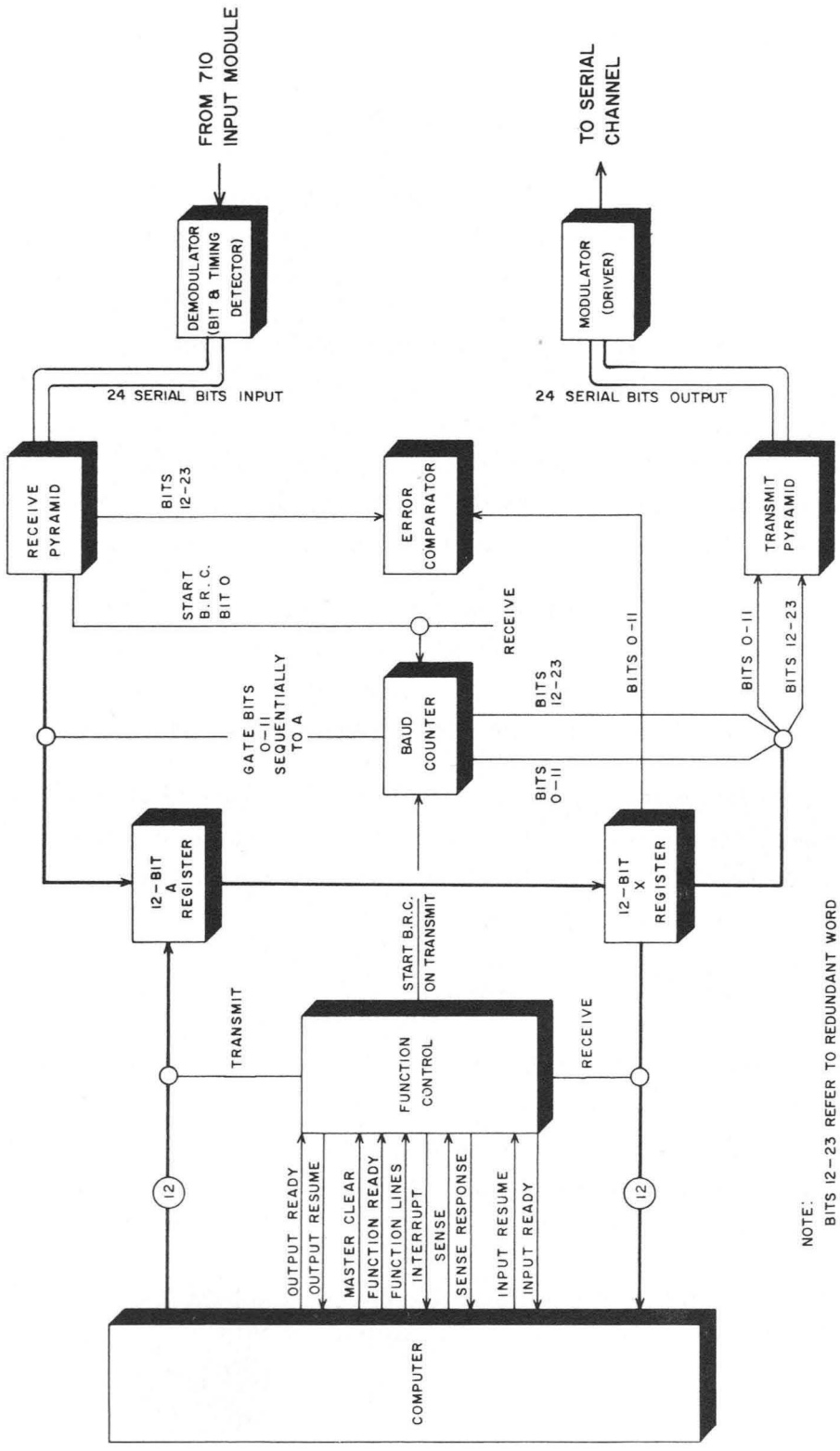


Figure 1-1. Digital Communication Terminal

CONTROL HEAD

The main operation switches and the audio handset are in a desk-top control head which can be placed near the operator.

PRINCIPLES OF OPERATION

Parallel data and control signals are conveyed between the computer and terminal equipment over standard parallel logic cables. Four cables connect the terminal to the high speed transfer channel of the 1604/1604-A computer, two cables to channel 7 (input) and two cables to channel 8 (output). Two cables are required when a 160/160-A or 924/924-A computer is being used, one for normal or buffer input and one for normal or buffer output. Only one computer can be connected to a terminal at any time via parallel logic cables. The block diagram (figure 1-1) shows the terminal and control signals when the terminal equipment is connected to the 1604/1604-A computer. The terminal can operate with the 924/924-A in 160 mode without modification.

CONTROL SIGNALS

Data flow between computer and terminal is maintained by a sequence of control signals (tables 1-1 and 1-2).

TABLE 1-1. 1604/1604-A←→TERMINAL

Signal	Origin	Description
Function Ready	Computer	A 12-bit external function code is available for translation. Translation is contingent on proper equipment select digits in the code.
Output Ready	Computer	A 12-bit word is available to the terminal for transmission.
Output Resume	Terminal	Response to Output Ready which indicates terminal has accepted computer word and is ready for another.
Input Ready	Terminal	Terminal has a word available for computer.
Input Resume	Computer	Computer has accepted a word and is ready for another.
Sense Ready	Computer	Samples sense circuit of terminal for presence of condition specified by external function code.
Sense Response	Terminal	Response to Sense Ready which indicates presence of condition specified by external function code.

TABLE 1-1. 1604/1604-A←→TERMINAL (Cont'd)

Signal	Origin	Description
Interrupt	Terminal	Causes computer to interrupt main program, determine cause of interrupt and take action on it.
Master Clear	Computer	Establishes initial operating conditions within terminal.

TABLE 1-2. 160/160-A←→TERMINAL

Signal	Origin	Description
Function Ready	Computer	Accompanies external function code and causes equipment to examine the external function code (turned off by Output Resume).
Information Ready	Computer	A 12-bit word is available to the terminal for transmission. Turned off by Output Resume.
Output Resume	Terminal	Response to Information Ready or Function Ready indicating terminal has accepted computer word and is ready for another. Turned off by dropping of Information Ready or Function Ready.
Input Ready	Terminal	Terminal has a word available for computer.
Input Request	Computer	Computer is ready for an input word.
Interrupt	Terminal	Causes computer to interrupt main program, determine cause of interrupt and take action on it.
Master Clear	Computer	Establishes initial operating conditions within terminal.
Input Active	Computer	160 only.
Disconnect	Terminal	Discontinues input operation.

FUNCTION CODES

Local terminal equipment operations are initiated by coded external function instructions. The upper 6 bits select the terminal equipment; the lower bits specify the serial communication channel and operation requested. An accompanying Function Ready signal allows recognition of the 12 bits as an external function code. The external function codes vary with the type of computer using the terminal equipment.

The sense code or status response indicates to the computer conditions within the terminal equipment. Either the presence or absence of the condition can be sensed.

TABLE 1-3. SELECT AND SENSE CODES

Select Codes		Function
1604/1604-A	160/160-A	
7407 70n1	34n1*	Select Interrupt and Select Channel n
7407 70n2	34n2	Select Receive and Select Channel n
7407 70n3	34n3	Select Receive and Interrupt and Select Channel n
7407 70n4	34n4	Select Transmit and Select Channel n
7407 70n6	34n6	Clear Interrupt Selection and Select Channel n
	34n0	Select Status and Select Channel n

1604/1604-A		160/160-A	
Sense Code	Indication	Status Reply	Indication
7477 70n0	Exit on Data Terminal Interrupt	0001	Error
		0002	Fake Ready Set
7477 70n1	Exit on No Data Terminal Interrupt	4000	Interrupt
7477 70n2	Exit on Fake Block		
7477 70n3	Exit on No Fake Block		
7477 70n4	Exit on Detected Errors		
7477 70n5	Exit on No Detected Errors		

Select Codes

Select Transmit and Select Channel n: Upon receipt and translation of this code, the terminal prepares to transmit data on the independent serial communication channel n. If n = 0 the terminal will transmit on all connected channels simultaneously.

After the terminal has established the initial transmission conditions, the computer places a 12-bit (parallel) word and a ready signal on the output lines. The word is passed into a Buffer register, A, and transferred to a second register, X. A baud counter scans the X register at a predetermined rate, gating bits 0 through 11 sequentially to the transmission line. The X register is immediately scanned a second time, gating bits 12 through 23 to the transmission line. These bits form the redundant word for error detection at the receiving terminal equipment. (Data plus redundancy comprise a 24-bit serial word.)

*Only 160-A or 924/924-A in 160 mode will be interrupted.

When the entire 24 bits have been transmitted and an exchange of ready and resume signals has occurred, the next computer word is ready to be serialized.

Words are separated by short controlled null periods; blocks are separated by longer nulls. The length of inter-block null periods varies according to the computer program and is set to a minimum limit by the terminal. Inter-word null periods are selected by the Word Space Control (WSC) switch and remain constant during an operation.

Select Receive and Select Line n: Unless transmit is selected, a terminal will monitor the serial channel. Any data received will be assembled as though the data were being transferred to the computer. A receive selection enables the actual transfer of data to the computer.

During reception, the A register acts as an assembly register. Incoming serial data after an inter-word null causes the counter to start gating bits 0 through 11 into A. When assembly of the first 12 bits is complete, the word is transferred to X; an error detection circuit compares each incoming bit of the redundant word with its corresponding stage of X. The contents of X are sent to the computer. If a block or word received is in error a FF will set, lighting the red Error light on the control head.

The 24th bit signifies the end of a word and the A register is cleared (after error comparison) to receive the following word. The X register is cleared after receipt of bit 10 of the following word. This allows for data comparison without interferring with the incoming word.

Select Receive and Interrupt and Select Channel n: This code is permissible only under certain program conditions. If it is programmed on a 160/160-A or 924/924-A computer, it may be followed by an input instruction. One of the following instances will apply:

a) Input word is the correct interrupt code word (no error).
   An interrupt will occur.
b) Input word is not the correct interrupt code word.
   No interrupt will occur.
c) No input word at all. (A status check should reveal a Fake Ready if timed wait for data is in effect.)
   No interrupt will occur.

If this code is programmed on the 1604/1604-A following a 62 instruction, the interrupt and a ready may occur simultaneously, permitting an entire block to be accepted before recognizing the interrupt.

Select Interrupt and Select Line n: During an interrupt selection the terminal equipment compares the first word* of each block of data received with a predesignated interrupt code. If the two match and no error is detected, an interrupt signal is activated and the main computer program is interrupted. The interrupt code word is set manually by six switches. The word can be anything except $00XX_8$.

A switch provides two options for this select code: Program Cleared Interrupt Selection (PCI) and Function Cleared Interrupt Selection (FCI).

PCI - In this position a sense code or status request will clear the interrupt condition (not the selection) after sampling. The selection can be cleared by a computer master clear or by a clear interrupt selection (34n6) only.

FCI - In this position, a 34nX function code, with X even, will clear the Interrupt Selected FF when executed. If X is odd, the Interrupt Selected FF will be set, or will remain set.

8528 CHARACTERISTICS

STANDARD

Communication established and transfer effected through program control. Error detection hardware incorporated.

Parallel Interface (12 bits)	Compatible with - 160/160-A 924/924-A (160 mode) 1604/1604-A

A test simulator is provided for computer free serial channel maintenance.

Serial Data Format	Split Phase Discontinuous; word by word basis Asynchronous on serial input Variable block lengths 12-bit serial word plus 12-bit redundancy

* First word is the word preceded by an inter-block null.

Peak Serial Data Rate	2.5×10^6 bits per second (fixed)
Word Rate During Block	Adjustable to maximum determined by formula: $\frac{1}{25 \times \frac{1}{\text{peak rate}}}$
Output	20v p-p, 75 Ω load, balanced
Input Requirements	10 mv p-p, 75 Ω load, balanced
Band Width Required	0.5 mc to 3.5 mc at 2.5×10^6 bits per second
Audio	Multiplexed into data channel

Equalization for up to 1.5 miles of RG-22/BU cable.

Coded Interrupt

Switch Selections

Time/Indefinite Wait for Data
Wait/Not Wait Beginning of Block
Interrupt on Error
Interrupt on Fake Ready
Disconnect on Error
Disconnect on Fake Ready
Interrupt Selection cleared under program control in two ways:

PCI	34n6
FCI	34nX, X even

OPTIONS

Up to six additional serial communication channels

Any fixed bit rate from 3×10^3 to 5×10^6 bits/sec

512_{10} word error counter

Output impedance of 50, 75, 100, or 125 Ω

Equalization as required for cable other than RG-22/BU

Cable exchange boxes other than those required to connect RG-108/U to RG-22/BU

External pads and attenuators

Receive and transmit on single cable

Single ended operation

Audio on/off data channel - must be removed at peak bit rates less than 0.5×10^6 bits/sec

CHAPTER II
OPERATION

This chapter contains information necessary for operating the digital communication terminal after the power, communication channels, and control cables have been connected.

MAIN CABINET CONTROLS AND INDICATORS

Switches on the main cabinet are used primarily for establishing initial operating conditions or for maintenance.

EXTERNAL

Power On (Blue)	S/I*	When pressed, full operating power is applied to the terminal equipment.
Power Off (Red)	S/I	When pressed, turns off all operating power and the Power On light.
+20/-20 (White/Blue)	I	The upper half of this indicator lights when +20 vdc is being applied to the system. The lower half indicates that -20 vdc is applied.

INTERNAL

These controls are located on the lower quarter of the logic chassis (figure 2-1).

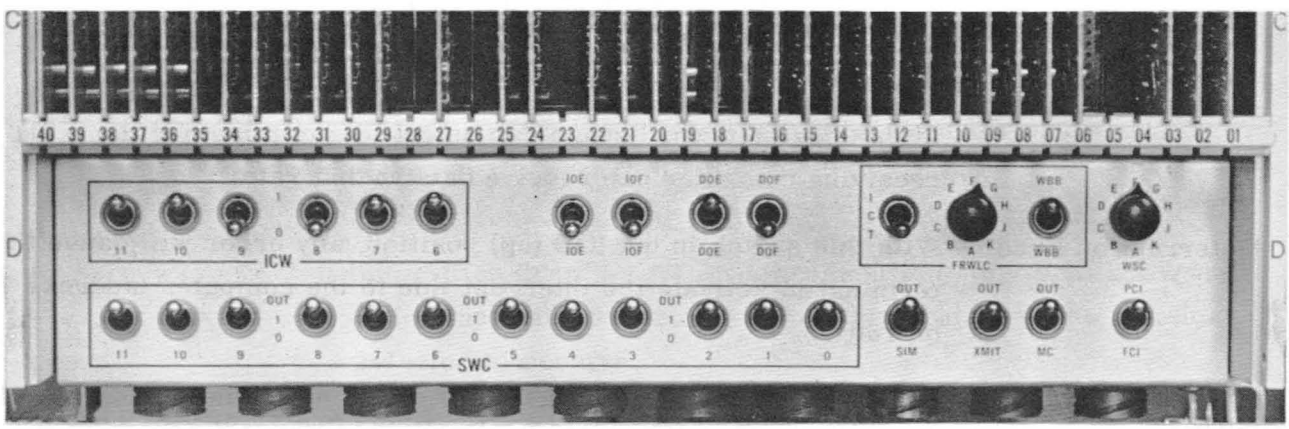


Figure 2-1. Internal Controls

* S = Switch
I = Indicator

Interrupt Code Word (ICW)

The position of these six switches determines the interrupt code word. This word can be anything except $00XX_8$. In most instances each terminal in a network is assigned a different interrupt code, corresponding to the master program. If the computer connected is a 160-A, an address 40 interrupt will occur if bit 0 of the interrupt word is even; an address 30 interrupt will occur if bit 0 is odd.

Simulator

The switches controlling simulator operation consist of the 12 Simulator Word Control (SWC) switches, and three master switches. The master switches are SIM, XMIT, and MC.

To use the simulator, throw the SIM switch down. Select a word by setting the SWC switches to some combination of "1's" and "0's". Placing the XMIT switch in the down position will cause the selected word (the one set by the SWC switches) to be continuously transmitted. To return the 8528 to normal operation, throw all simulator switches to the OUT position and toggle the MC switch. All of these switches must be the OUT position for normal operation.

Word Space Control (WSC)

This ten-position rotary switch controls the spacing between each transmitted word and is variable at each installation. The 160/160-A computers can send one 12-bit word every 19.0 usec. Since it takes the terminal 9.6 usec to send a 24-bit serial word (at 2.5×10^6 bits/sec), the time between words will be approximately 9.4 usec. The 1604/1604-A can send one every 6.8 usec; in this case the word space can be cut to a minimum if the receiving computer can receive data at that rate.

*Interrupt on Error (IOE)

With this switch in the IOE (up) position, any error will cause the terminal to activate the interrupt line to the computer (address 40 on 160-A).

*Interrupt on Fake (IOF)

If the IOF switch is in the IOF (up) position, a Fake Ready signal (see FRWLC) causes the terminal to activate the interrupt line (address 40 on 160-A).

---

* Sense or status responses will not indicate an interrupt.

Disconnect on Error (DOE) - (160/160-A only)

If this switch is in the DOE (up) position, an error in reception will cause an Input Disconnect signal to be sent to the computer. This terminates the input instruction without counting up the buffer field.

Disconnect on Fake (DOF) - (160/160-A only)

With the switch in the DOF (up) position, the terminal will activate the Input Disconnect line when a Fake Ready signal is generated (see FRWLC). This will terminate the input instruction without counting the buffer field further.

Fake Ready Wait Length Control (FRWLC)

These controls consist of a three-position switch, a ten-position rotary switch and the WBB switch.

The ten-position rotary switch varies the length of time the terminal will hang up the computer to await data. If receive is selected immediately before the input instruction and no data is received within the specified time limit, the terminal generates Fake Ready signals for the computer. This allows the input instruction to be completed.

By placing the three-position switch in the INDEFINITE (I) position, the operator can terminate the input instruction by momentarily pressing the Reset button on the control head. The CONTINUOUS (C) position causes Fake Ready signals as soon as receive is selected. In the TIMED WAIT (T) position, Fake Ready signals are sent to the computer after a predetermined delay. The timed wait is determined by the ten-position rotary switch.

With receive selected and the Wait Beginning of Block switch in the WBB (up) position, the terminal cannot transfer any words it may receive until it senses the beginning of a block. This prevents the computer from receiving a block of data out of sequence.

If this switch is in the $\overline{\text{WBB}}$ (down) position, the terminal will transfer incoming data to the computer as soon as the terminal is selected to receive.

Normally this switch will remain in the WBB position because programming usually stipulates that the computer examine the first several words (depending on format) in each block for procedural data and/or tags. In the $\overline{\text{WBB}}$ position it would be possible for the computer to examine any word of a block as though it were the first word.

CONTROL HEAD INDICATORS AND SWITCHES

The more frequently used indicators and switches are on the control head. A single logic cable connects the control head to the main cabinet.

Power (Green)	I*	When lit, indicates that 115 vac is applied to circuits in the terminal.
Test (White)	I	Lights if any of the simulator switches are in a position other than OUT.
Receive (Green)	I	Lights when the computer has selected the terminal to receive. If short blocks of data are being received, the time period will be too short for the light to change state.
Error (Red)	I	Lights if an error occurred during reception of a block of data. A sense or status function code automatically clears the indication. If short blocks are being received and errors are sensed at the end of each block, the light will not be visible.
Reset (Amber)	S/I*	If the terminal has been selected to receive and data does not arrive by the time the FRWLC signal terminates, the Reset indicator lights. This signifies that a false block of data has been sent to the computer to terminate the input instruction (short blocks may not change the state of the light). If the FRWLC switch is in the I position and receive is selected, the operator can terminate the input instruction at any time by momentarily pressing the Reset button. If data is present no Fake Ready will occur. If the FRWLC switch is in the T position, the operator can change to I by holding down the button before receive is selected, and continuing to hold it down. Releasing the button returns the terminal equipment to timed wait status.

* S = Switch
I = Indicator

Call (White)	S/I	Any or all of the stations on a network may be signalled by removing the handset from the cradle and pressing the appropriate Audio Line Selector buttons and then the Call button. Hold the Call button in until the parties answer or until it is determined they are not available.
Audio Line Selector (1 through 7)	S/I	An incoming call will light the Audio Line Selector indicator corresponding to the number of the calling station and an audio tone will emanate from the loudspeaker. To answer a call remove the handset from the cradle, momentarily press the appropriate Audio Line Selector button to engage the line, and push the Push to Talk button on the handset. Replacing the handset removes all selections.

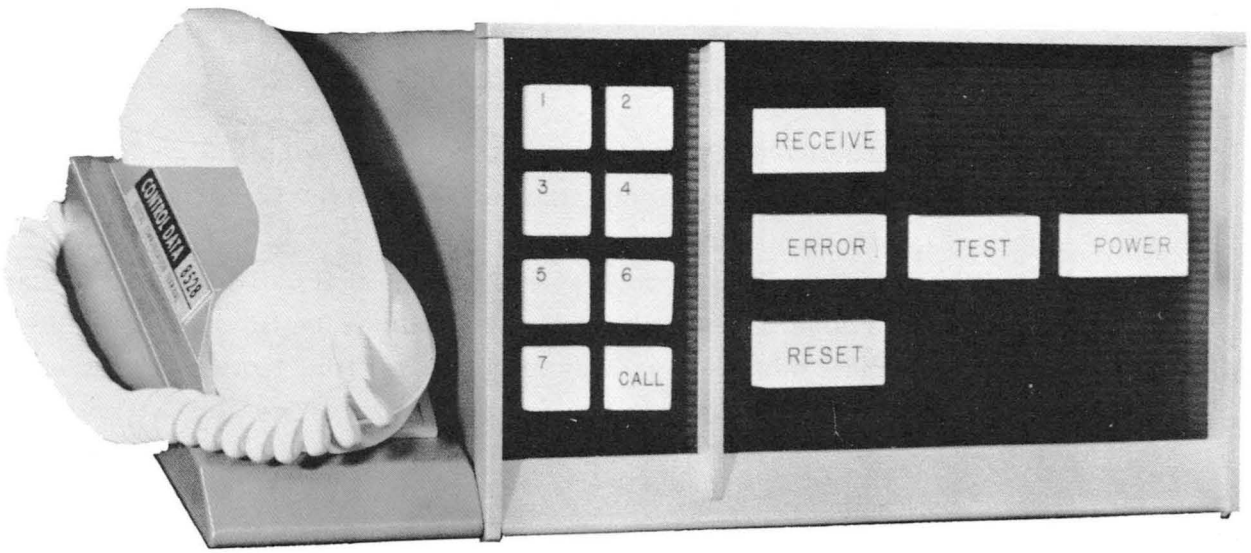


Figure 2-2. Control Head

CHAPTER III

PROGRAMMING

Programming information in this section presupposes some knowledge of programming procedures. The material is intended to serve as a guide for establishing communication between computers linked by terminal equipments.

Each computer on a serial communication network must have a transmit routine and a receive routine previously programmed before data can be transferred. The receive routine must designate the initial and terminal addresses of the block reserved for receipt of data; the only other major consideration is that the transmit and receive routines be able to accommodate each other with minimum loss of time.

The terminal equipment does not differentiate between straight data and procedural information. This distinction must be made in programming. Usually it will be necessary for both routines to contain transmit and receive subroutines in order to establish terms of contact.

EXAMPLE A (TWO COMPUTER PRIVATE SYSTEM)

The flow chart in figure 3-1 illustrates a data transfer without the use of interrupt. The transfer is initiated by the computer which is to transmit.

Assume that computer B is in the receive subroutine (loop Ba), and that computer A is to enter the transmit subroutine. Whichever computer enters the transmit or receive subroutine first must wait for the other to respond. The length of the wait period will depend on the relative events in the two main programs which lead to the entrance of the subroutines.

Computer B	Computer A
B1 Computer B enters receive subroutine. The conditions inserted by the main program are: loop limits, initial and terminal addresses, maximum block limits, line selection.	
B2 Select 8528 to receive. The FRWLC must be in the T position and WBB in effect.	
	A1 Enter transmit subroutine, set initial conditions.
	A2 Select 8528 to transmit and send message indicating block length.
B3 Interrogate 8528. If response does not indicate a fake block or an error, continue to B4. If an error or fake block is indicated, take loop Ba to B2.	
	A3 Select receive with timed wait for data and WBB in effect.
	A4 Interrogate. If an error or a fake block is indicated, cycle back to A2 through loop Aa.
B4 If in B3 neither an error nor a fake block is found, the block length is compared with the predetermined limit. If it is in excess, go to B5. If not, go to B6.	
B5 If limit was exceeded, indicate and exit or stop.	
B6 Wait for block of data.	
B7 Interrogate. A fake block indicates either that B did not select receive quickly enough to satisfy WBB or the reply back to A was in error. In either case, loop Bc will be cycled.	
	A5 If, in A4, no error or fake block was indicated, evaluate reply. If negative, indicate and exit or stop. If affirmative, proceed to A6.
	A6 Transmit block.
	A7 Select receive and await reply.
B8 If no error or fake block was indicated in B7, examine first word (tag) of block. If tag indicates A is still in loop Aa, B cycles loop Bd. If tag is not listed, stop. If an error is detected, call for retransmission and go to B9.	
B9 Transmit call for retransmission if necessary, then return to B6 (loop Bf). If no retransmission is necessary, exit.	
	A8 If fake block terminates transmission, interrogate. If no fake or error, exit. If an error occurs assume a call for retransmission was sent. Unless computer A receives an affirmative final reply without error, computer A cannot be certain that the block was received. Likewise computer B cannot be certain that its reply was received, but the exchange of replies must stop eventually if any additional information is to be transferred. The action of the last reply will be greatly influenced by the initial choice of the mode of communication (interrupt or probe) and which computer initiates the transaction.

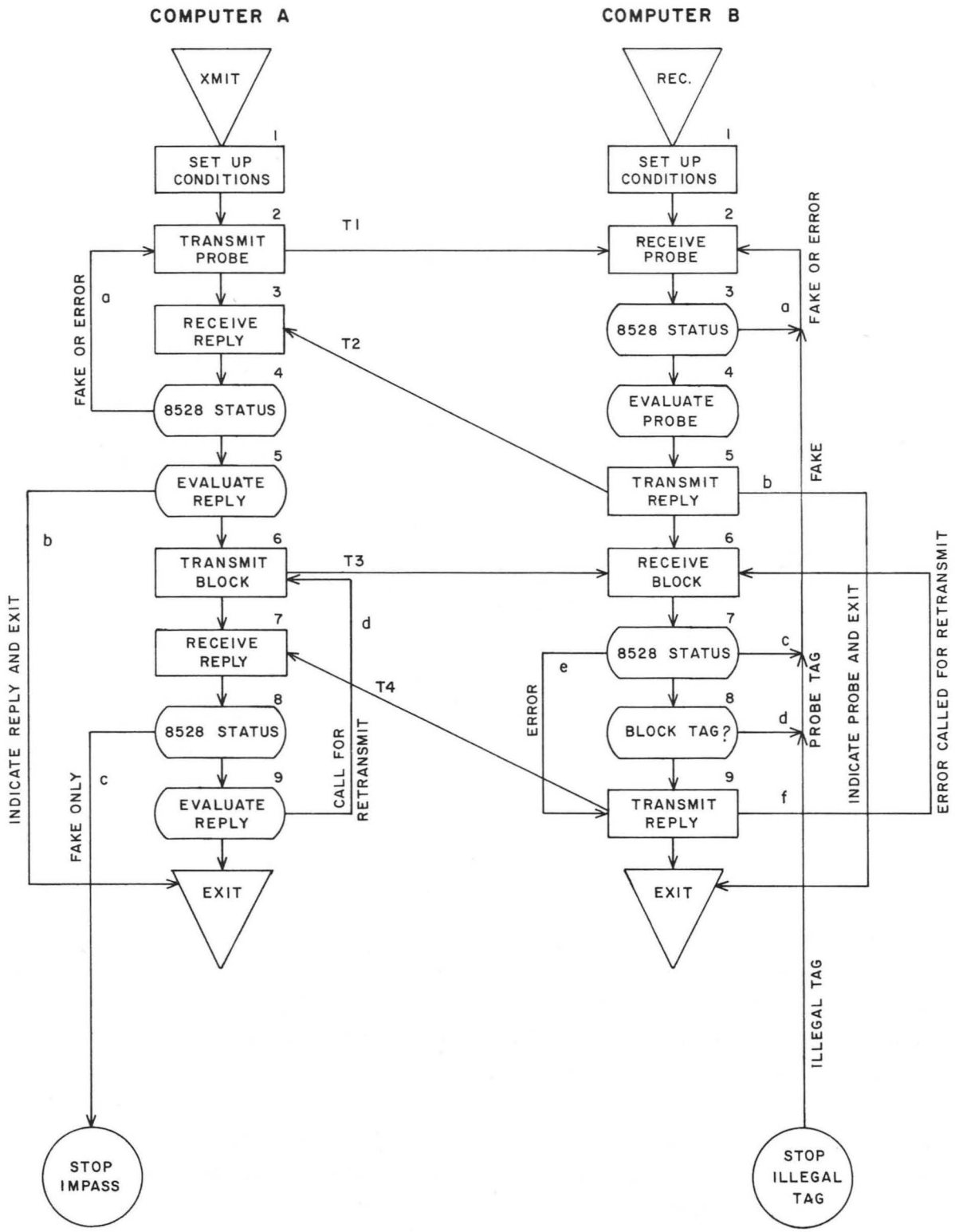


Figure 3-1. Typical General Purpose Receive/Transmit Routine

EXAMPLE B (MULTI-COMPUTER NETWORK)

When more than two computers are to communicate on a party line basis, it is convenient to assign the task of directing the flow of information to a master computer; other computers on the line are referred to as remote computers. The master computer program must include a subroutine for each remote computer. This subroutine includes (1) the unique designation of the remote computer (2) starting and terminating addresses of the data to be transmitted to the remote computer (3) starting and terminating addresses of the block reserved for receipt of data from the remote computer, and (4) the flag which indicates to the main program what the subroutine accomplishes. When the main program enters the list of subroutines, each remote terminal is probed in turn. If the remote terminal can be interrupted, the subroutine interrupts it. The terminal equipment continuously monitors the serial communication channels unless selected to transmit. If the correct interrupt code word is received at the beginning of a block and the word is not in error, an Interrupt FF sets and the interrupt line to the computer is activated. If the remote terminal cannot be interrupted, it must sense the Interrupt FF to determine if it is being probed. For programming simplification, the following rules are arbitrarily adopted:

1) Remote computers can communicate only with the master computer. The master computer must periodically interrogate (probe) the remote computers to determine what action, if any, should be taken on or by a specific remote computer.

2) Remote computers cannot interrupt the master computer. The remote computer must recognize the probe.

The probe from the master computer may be a procedural probe or an interrupt (if the remote computer can be interrupted). The procedural probe (data in a fixed format) is used to define communications procedures to a receiving computer. An interrupt code word sent by the master computer will cause a remote computer to cycle until it receives instructions via a procedural message.

A typical master computer routine for a number of remote computers is shown in figure 3-2. It will accommodate computers which can or cannot be interrupted. The routine for a remote computer is shown in figure 3-3.

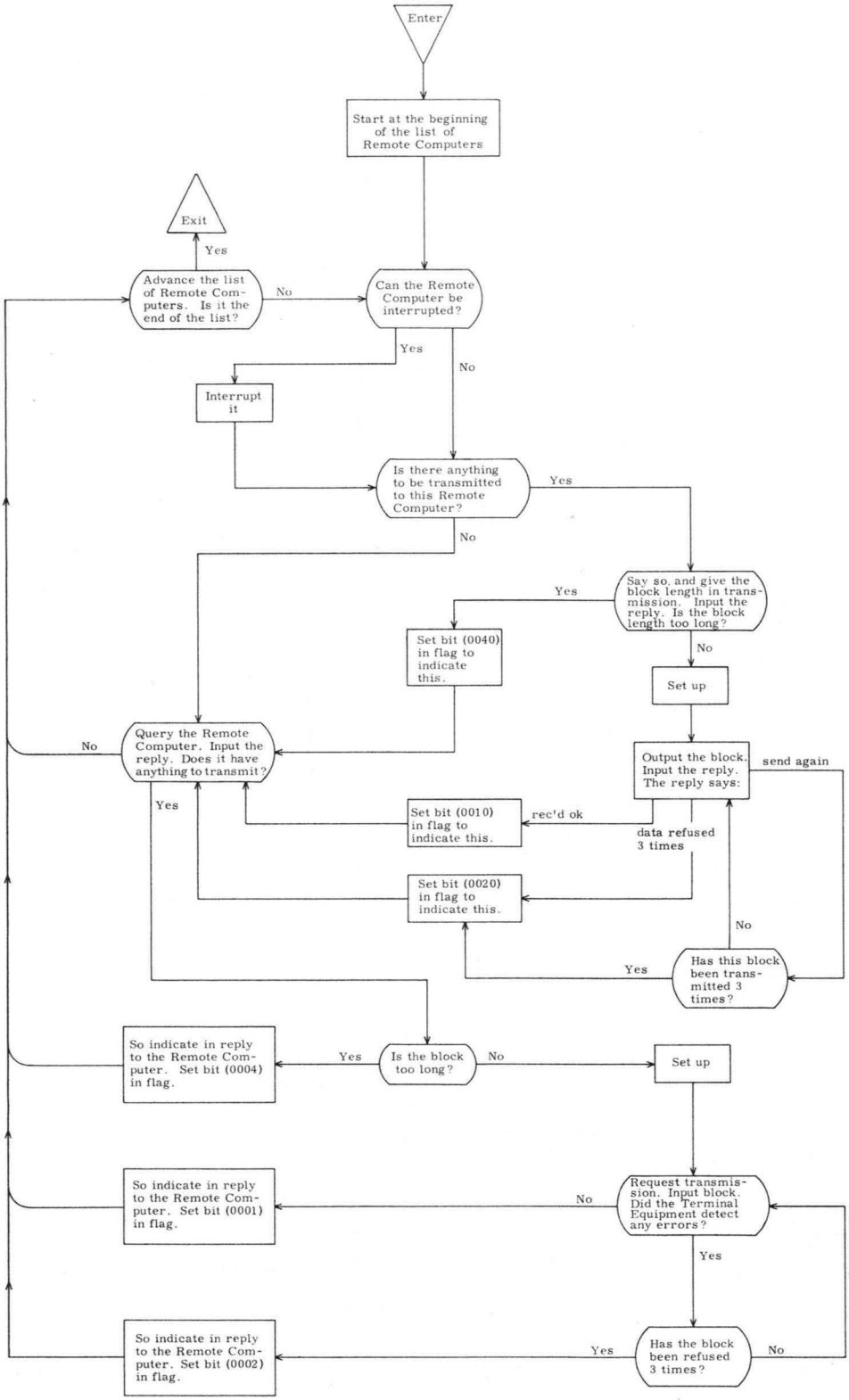


Figure 3-2. Master Computer Routine

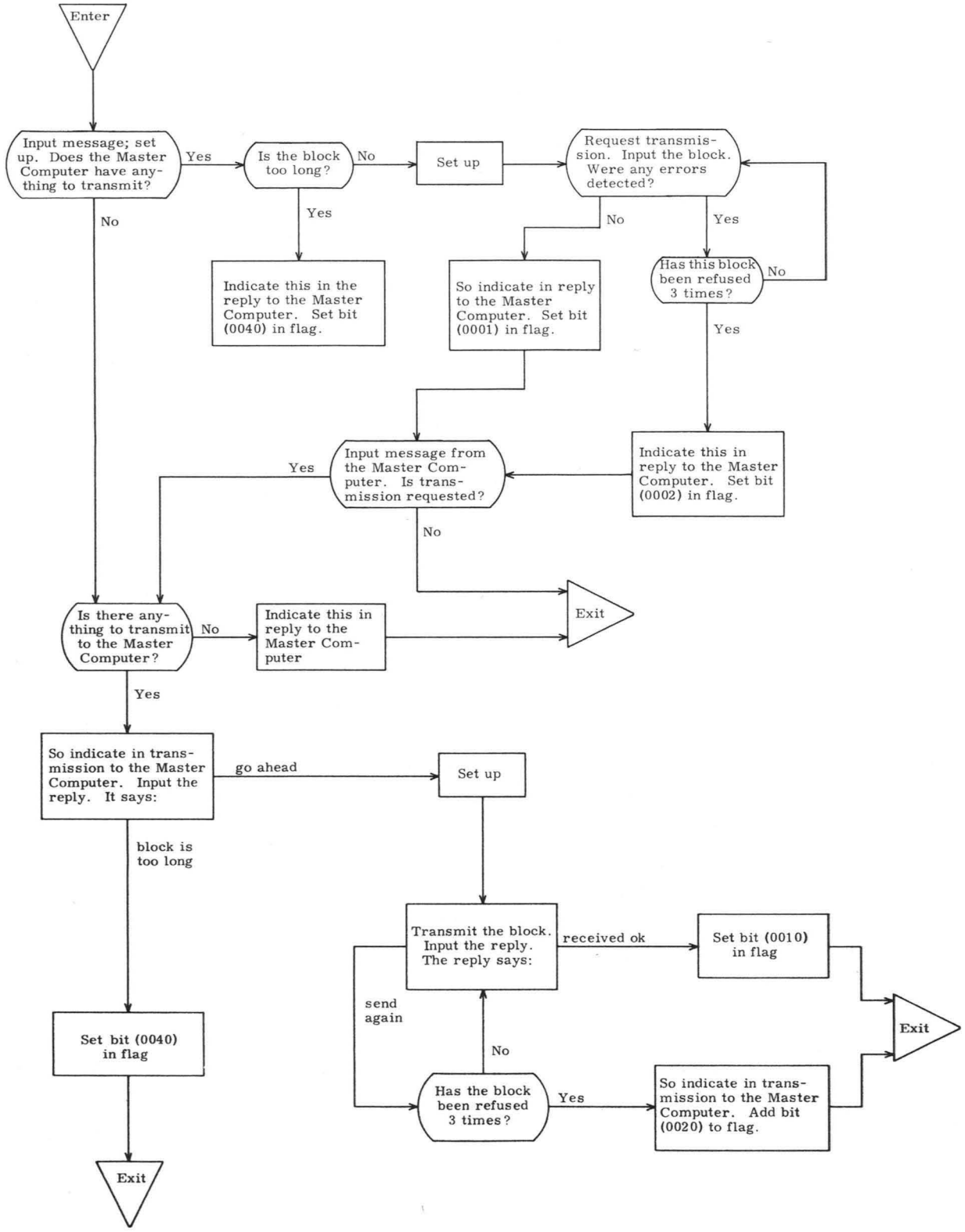


Figure 3-3. Remote Computer Routine

Only a few programming possibilities have been touched on here. In a sense there is as much flexibility in the system as there is flexibility in programming. The use of interrupt will prevent one computer from waiting for data for any great length of time; however, unless fixed block lengths are to be used, the length of each block and conditions of contact must be communicated as in example A.

PROGRAMMING AIDS

EFFECTS OF FAKE READY OR WBB

If receive is selected while data is coming in and WBB is in effect, the fake ready will not occur until the end of the block has been received and the timed wait period has expired. If the interrupted portion of the block is longer than the timed wait, the fake ready will occur at the end of the block. If the timed wait expires after the block has been received, the fake ready will occur at the time of expiration.

When the input is terminated, all remaining locations in the memory block used will be filled with the last word received in the interrupted block.

FAKE READY WHEN NO DATA IS BEING RECEIVED

If receive is selected, no data is being received, and the fake ready delay expires, the fake ready will cause input words consisting of 0000_8 to be sent to the computer until the block is terminated.

LINE SELECTION

All function codes are translated relative to a line selection. However, the status or sense code responses indicate the status irrespective of line selection.

INTERRUPT ON ERROR OR FAKE READY

The interrupt line to the computer is activated as soon as an error or fake ready occurs. When an interrupt occurs because of the error or fake ready, a status or sense response would indicate this condition rather than an interrupt.

STATUS AND SENSE

A status or sense code automatically clears the FFs indicating the conditions when the response has been returned to the computer.

Status (160/160-A Only)

A status selection must be followed by a one word input. The program may provide for a status response by selecting receive without a one word input. The block received will then contain, as its first word, the status prior to the first word received. The first word of data will be the second word in the input block. The input block length must be increased by one to allow for the address occupied by the status response.

RECEIVE AND INTERRUPT SELECTION WITH TIMED WAIT FOR DATA

After this selection a fake ready will occur if the block input is not terminated by a status or sense selection before the time period expires. From the occurrence of the fake ready until data is again being received, the word loaded into memory will be the last word of the previous block.

DISCONNECT (160/160-A ONLY)

A disconnect caused by a fake ready or an error will terminate the input and stop the address count.

RESTRICTIONS

1. An input instruction must be initiated immediately after execution of select receive. Reasons:
   a) The computer data channels do not provide a Channel Active signal. Therefore, the timed wait for data must be conditioned on the receive selection.
   b) To insure that the input request is up by bit 11 time when the 160/160-A computer is being used.
2. A status request or sense code must be executed immediately after the termination of the input instruction. Reasons:
   a) To disengage the timed wait for data by clearing the receive selection.
   b) The terminal, unless actually transmitting, is always on line. Therefore, an error might occur after the information is correctly received.
3. In a multi-line system, if the remote stations are allowed to initiate transfers independently of the master, a status or sense request with a line selection other than "0" must be executed after a master clear. Reason:
   a) A master clear selects all lines; if data arrives on more than one line at the same time, an error will result.

4. On computers where the input/output rate is determined by the number of active channels, the activity of these channels must be eliminated during receive or transmit or the word rate and relative time delays must be slowed so that words during block transfers are uniformly spaced. Reasons:
   a) If the channels are active, the spacing between words on the serial channel will become greater than the WBB delay or interrupt null detector, thus causing an inter-word null to appear as an inter-block null.
   b) The terminal is basically a one word buffer. If the computer is not always ready to accept the following word by bit 11 time (160/160-A) or by bit 24 time (1604/1604-A) it will miss the words resulting in a fake ready.

CHAPTER IV
PRINCIPLES OF OPERATION

This chapter covers the logical operations occurring in the terminal equipment. The terminal equipment logic is constructed from standard CONTROL DATA 3600 building blocks. The special circuits in the terminal equipment are described in appendix B.

TIMING

TRANSMIT

Transmit operations are accomplished by executing an external function code (Select Transmit On Line n) followed by an output instruction. Receipt of the select code and subsequent execution of an output instruction causes the terminal equipment to react as described below. Figure 4-1 shows the main steps in transmit timing.

Those events which occur simultaneously are given in the sequence which has the most apparent logical significance.

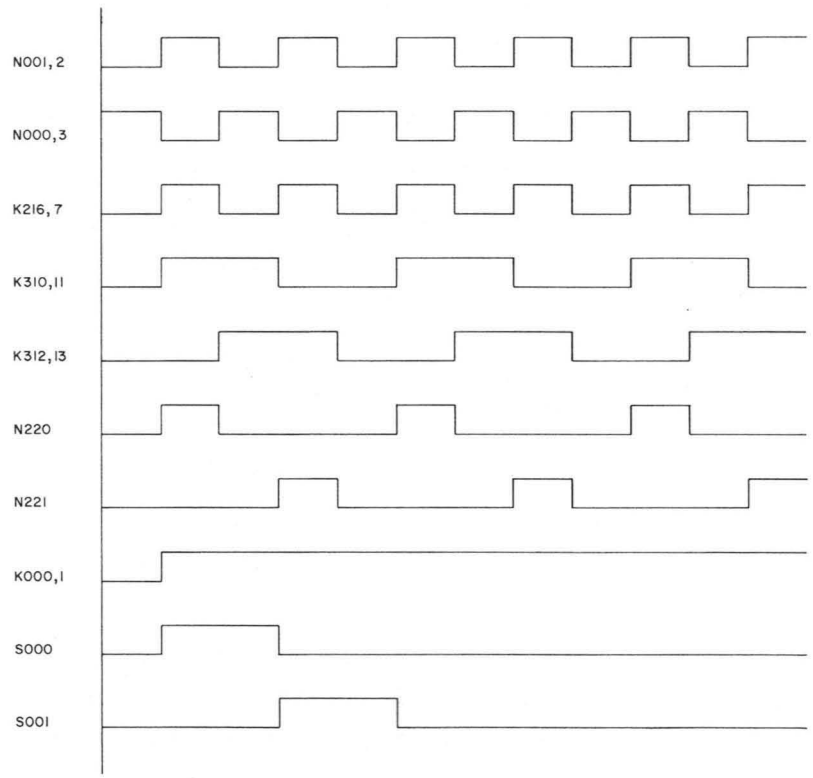


Figure 4-1. Transmit Timing

Step	Event	Remarks
1	Function Lines Up	External function code made available to terminal.
2	Function Ready	Appears after function lines have stabilized; permits terminal to recognize data on function lines. In the case of a 1604/1604-A this signal drops after 8 usec; if 160/160-A computer is connected, the signal remains up until the terminal equipment generates an Output Resume.
2a	Select Transmit FF	Set by translation of the proper EF code in conjunction with a Function Ready signal. Outputs of this FF enable the transmit logic to respond when the computer begins output operation.
3	Output Resume (160/160-A only)	This signal is generated by the terminal equipment after the EF code has been translated; causes Function Ready signal to drop; absence of Function Ready causes Output Resume to drop.
4	Output Ready (1604/1604-A) Information Ready (160/160-A)	Indicates that 12 bits of output data are available on the output lines.
5	M → A	After the data lines have had time to stabilize, the data is transferred to the A register.
6	A → X	Data in the X register is available for transmission; therefore the A → X transfer is effected early.
7	Timing Enable FF	This FF is set on the first odd clock phase after the M → A transfer; clock pulses can then trigger the baud counter.
7a	Baud Counter	The first even output of the frequency divider enables the baud counter to begin its cycle. Successive stages in the baud counter are set alternately by odd and even clock phases.
8	Sync FF	These FFs synchronize the setting of the Drive Enable FF with the gating of the first bit from the X register out of the transmit pyramid into the serial channel.
9	Sync Check FF	
10	Drive Enable	Set when first bit is available for transfer.

Step	Event	Remarks
10a	Data Ready	Set when drive lines are enabled; enables Output Resume to computer.
11	Mixer FF	Each bit from the transmit pyramid is gated into both sides of the Mixer FF by odd and even clock pulses. The output of the Mixer FF will therefore consist of a single cycle for each bit.
12	Output Resume	This signal indicates to the computer that the word has been serialized and that the terminal is ready for another word. The Word Space Control (WSC) is adjusted to fix the space between each word. Z099 is adjusted to control the minimum delay between blocks. Serialization of the next word cannot begin until these delays have expired.

The baud counter transfers the 12 consecutive stages of the X register into the transmit pyramid as each counter stage sets. When all 12 stages of X have been gated into the transmit pyramid, the counter begins clearing on consecutive odd and even clock phases. This action gates the contents of X into the transmit pyramid for the second time to form the redundant part of the 24-bit word.

Transmission of the entire 24 bits occurs in 24 times the bit rate frequency. As bit 24 is sent, the A and X registers are cleared. An Output Resume signal is sent to the computer as soon as serialization is completed.

The entire sequence from step 4 is repeated for each word in the block.

RECEIVE

A receive operation is initiated by executing a Select Receive external function code followed by an input instruction.* Figure 4-2 shows the main steps in receive timing.

* Select Receive must be followed by an input instruction in the next program step if timed wait for data is used.

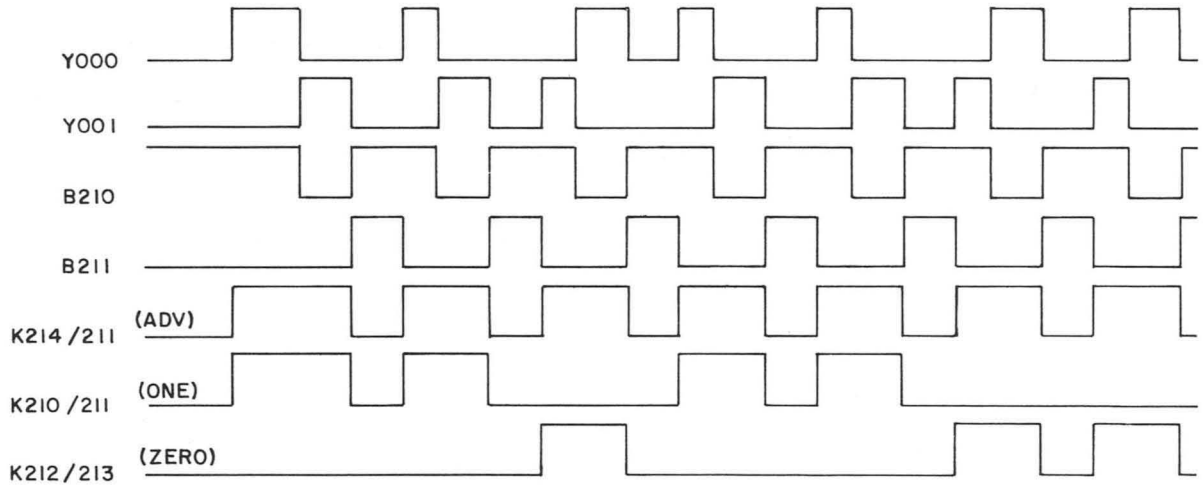


Figure 4-2. Receive Timing

Step	Event	Remarks
1	Function Lines Up	Function code appears on output lines.
2	Function Ready	This signal from the computer appears after function lines have stabilized and permits the 8528 to recognize and translate function code.
3	Receive Selected FF	This FF is set by the proper external function code in conjunction with a Function Ready signal. Outputs enable the receive circuits to react when input data is received.
4	Output Resume (160/160-A only)	An Output Resume signal is generated by the terminal equipment after the external function code is translated. The Output Resume causes the computer to drop the Function Ready signal. Absence of the Function Ready causes the 8528 to drop the Output Resume.

When the 8528 is not selected to transmit, the receive circuits continuously monitor the last selected serial channel. The data is received and assembled as it would be for a normal receive operation, but none of this data can be sent to the computer until receive

is selected. However, when receive is selected, the input data lines are enabled to the computer. This means that, immediately after receive is selected, either an input instruction must be executed or the FRWLC switch must be in the INDEFINITE WAIT position. In the Wait Beginning of Block (WBB) mode Input Ready signals are blocked if data is being received when receive is selected; the Input Ready cannot be sent until an inter-block null is detected by the WBB circuit. This insures that the computer will always begin receiving from the first word of a block. The following events occur:

Step	Event	Remarks
5a	Wait Beginning of Block FF	If no information is presently being received, this FF sets and enables the Input Ready FF.
5b	Signal Present B220 = 0	If information is being received, the output of this inverter will prevent setting the Input Ready FF until one inter-block null is detected. Failure to select receive before the beginning of a block will cause a Fake Ready at the end of the incoming data if WBB is used.
6	Sample Advance FF	As information begins to trigger the threshold amplifiers, this FF sets and clears at the rate of the incoming data.
7	Timing Slave	This FF is set and cleared by the Sample Advance FF. The output of the Timing Slave FF drives the frequency divider during reception.
8	Baud Counter	The counter, indirectly driven by the incoming data, gates the first 12 serial bits into consecutive stages of A.
9	A → X	As bit 12 of the incoming word is gated into A, the contents of A are transferred to the X register.
10	Error Detection	The counter gates the second 12 bits received (the redundant word) into a bank of inverters with the corresponding bit of the data word in the X register. If the two agree, no error is registered.

If an error occurs because of a mismatch between the contents of the X register and the incoming data, the Word and Block Error FF will be set. All data in the block will be transferred to the computer, even though there was an error. If the receiving computer is a 1604/1604-A, a "1" bit is transmitted to the computer and stored as bit 23 in the

same storage location as the word in error. The Word Error FF is cleared at bit 10 time of each word; that is, before the redundancy of the next word is compared to the data in X.

The Block Error FF is set when the Word Error FF is set for the first time during the receipt of any block. The Block Error FF and the Word Error FF light the red Error light on the control head. The light is cleared by a master clear, or sense or status request, if the last word received was correct. Thus, if any errors have occurred during the receipt of a block, that fact can be sensed at the end of a block.

Step	Event	Remarks
11	Input Ready	Signal from 8528 indicating to computer that a word is available on the input lines. If the 160/160-A is being used, the signal is initiated at bit 12 time; if 1604/1604-A is being used, signal is initiated at bit 23 time.
12	X → L	The transfer is enabled when receive is selected and effected when the Input Ready FF is set.
13	Input Resume (1604/1604-A)	Signal to 8528 from computer indicating that the computer has accepted the word. Receipt of the Input Resume causes the 8528 to drop the Input Ready signal; the computer then drops the Input Resume.
14	Clear A Clear Counter	Cleared prior to receipt of next word.

Steps 5-14 are repeated for each word of data received. When the computer buffer field has been filled, the input instruction is terminated at the computer. Fake Ready signals are generated by the 8528 to terminate the input instruction if data is absent for a time designated by the Fake Ready Wait Length Control position.

CIRCUITS

FUNCTION CONTROL CIRCUITS

The function control circuits (figure 4-3) regulate data flow between the computer and the terminal equipment. All control signals and sense, status, and select information pass through these circuits for translation.

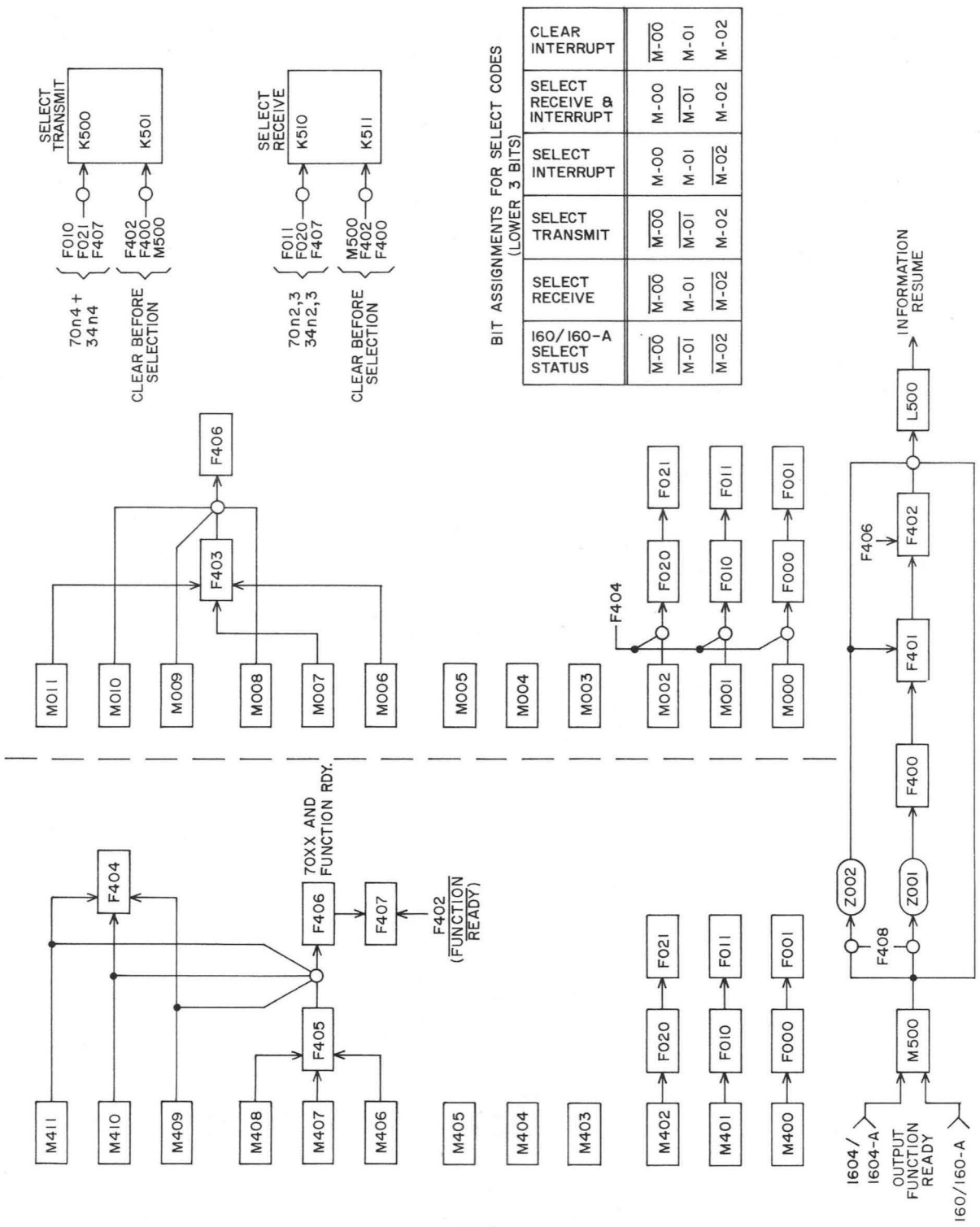


Figure 4-3. Function Control Circuits

External function codes from the 1604/1604-A computer are accompanied by a Function Ready or Sense Ready signal. This signal, in conjunction with the proper select digit, sets the control FFs. Outputs from the control FFs enable the circuits which are to perform the requested function. After 8 usec the computer automatically drops the external function code and the Ready signal.

The 12-bit output cable from the 160/160-A computer carries external function codes during an EF instruction and output data during an output instruction. The Function Ready signal differentiates between the two instructions.

The equipment select digits are the upper 6 bits of the external function code. Only the EF codes with the correct select digits (70_8 for the 1604/1604-A and 34_8 for the 160/160-A) will be translated by the terminal equipment.

1604/1604-A SENSE CODES

The 1604/1604-A computer determines the status of the terminal equipment through the use of external function sense codes. When accompanied by a Sense Ready signal, the sense code is translated, causing the Sense Ready FFs to be set or cleared to partially enable a specific response. The responses are enabled by outputs from the FFs storing the condition sensed (figure 4-4). The Sense Ready FFs are cleared when the Sense Ready signal from the 1604/1604-A drops.

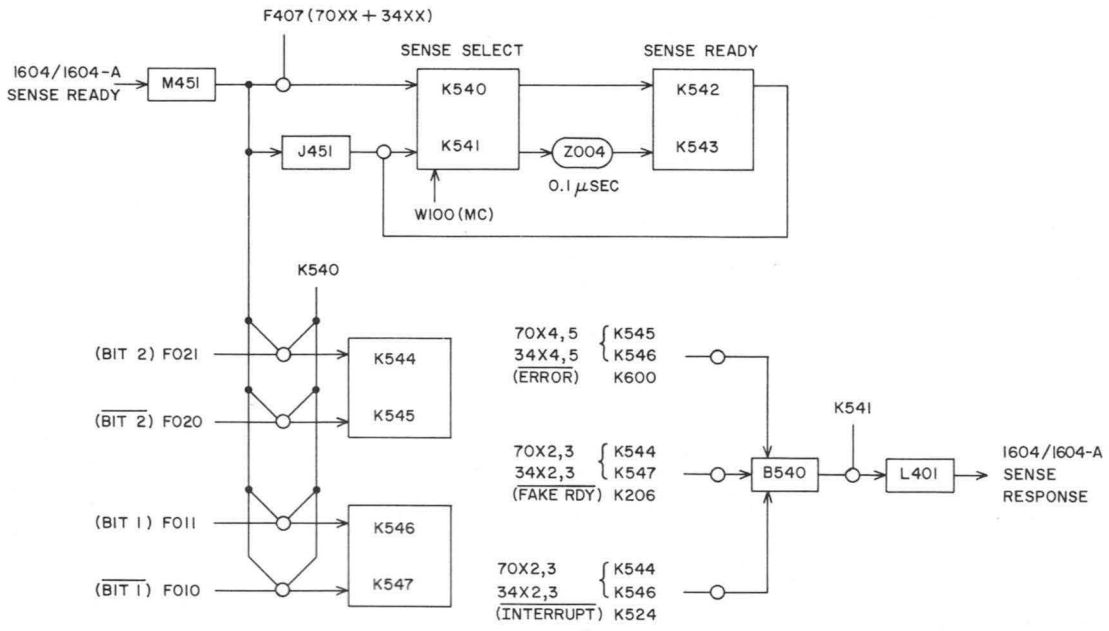


Figure 4-4. 1604/1604-A Sense Codes

Either the presence or absence of a specific condition can be determined. A positive response is interpreted by the computer as the presence of the condition sensed for; no response (a negative response) indicates the condition is not present.

A sense code will clear the Select Receive FF. Receive or transmit must be reselected after each operation.

160/160-A STATUS REQUEST

A status request external function code from the 160/160-A sets the Status Request FF in the terminal. When the subsequent input instruction is executed, the Status Enable FF sets to allow the 12-bit status response to be routed to the computer (figure 4-5).

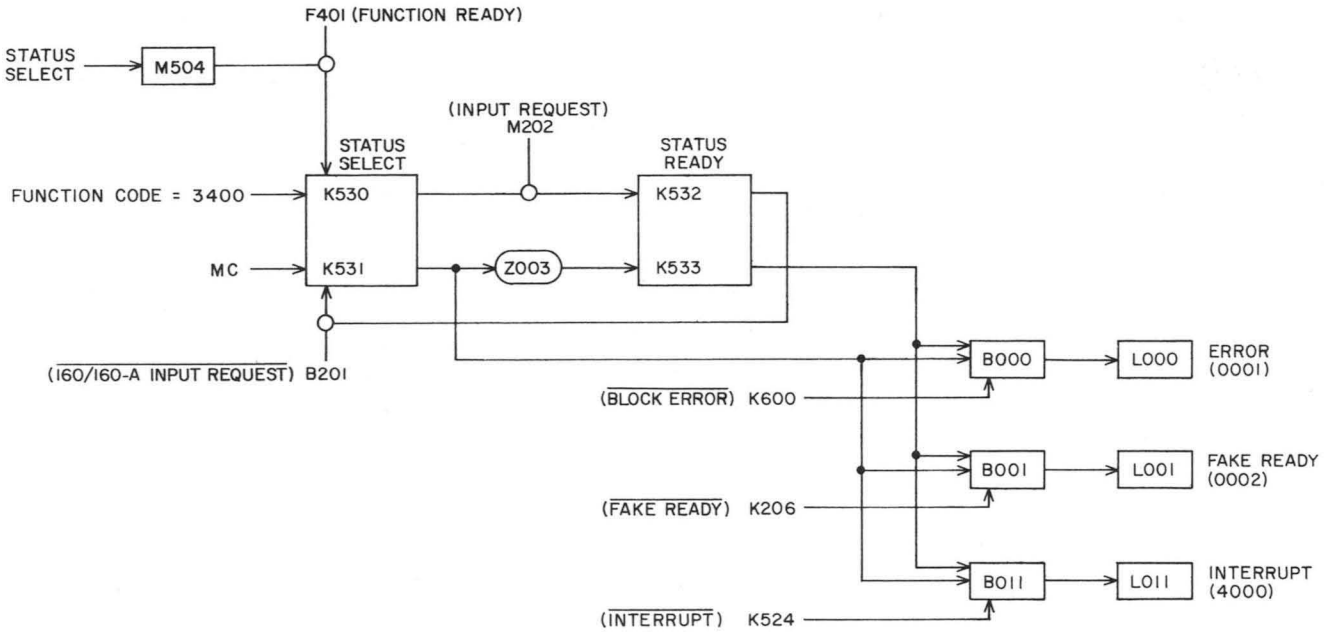


Figure 4-5. 160/160-A Status Response

The response will consist of logical zeros, except in those bit positions which have been enabled by the set state of the Error, Fake Ready or Interrupt FFs. The response must be examined by computer program for any specific condition. Bits 2 through 10 will indicate the contents of the optional 512_{10} counter.

The status request clears the Receive or Transmit FF and the operation must be reselected.

INTERRUPT

An interrupt code word is manually preset by the Selector switches mounted on the printed circuit card chassis (figure 4-6). If interrupt is selected and the inter-block null is detected, the Beginning of Block FF is set. If the upper 6 bits in the first word of the succeeding block agree with the predesignated interrupt word and no error is found after the redundant word is compared, the Interrupt FF will set, activating the interrupt line. If any of these conditions are not met, the Beginning of Block FF is cleared and the first word of the next block will be examined for the interrupt code word. Any other word which is the same as the interrupt code word but is not the first word of a block cannot set the Interrupt FF.

The interrupt condition, but not the selection, is cleared after either a sense code or status request.

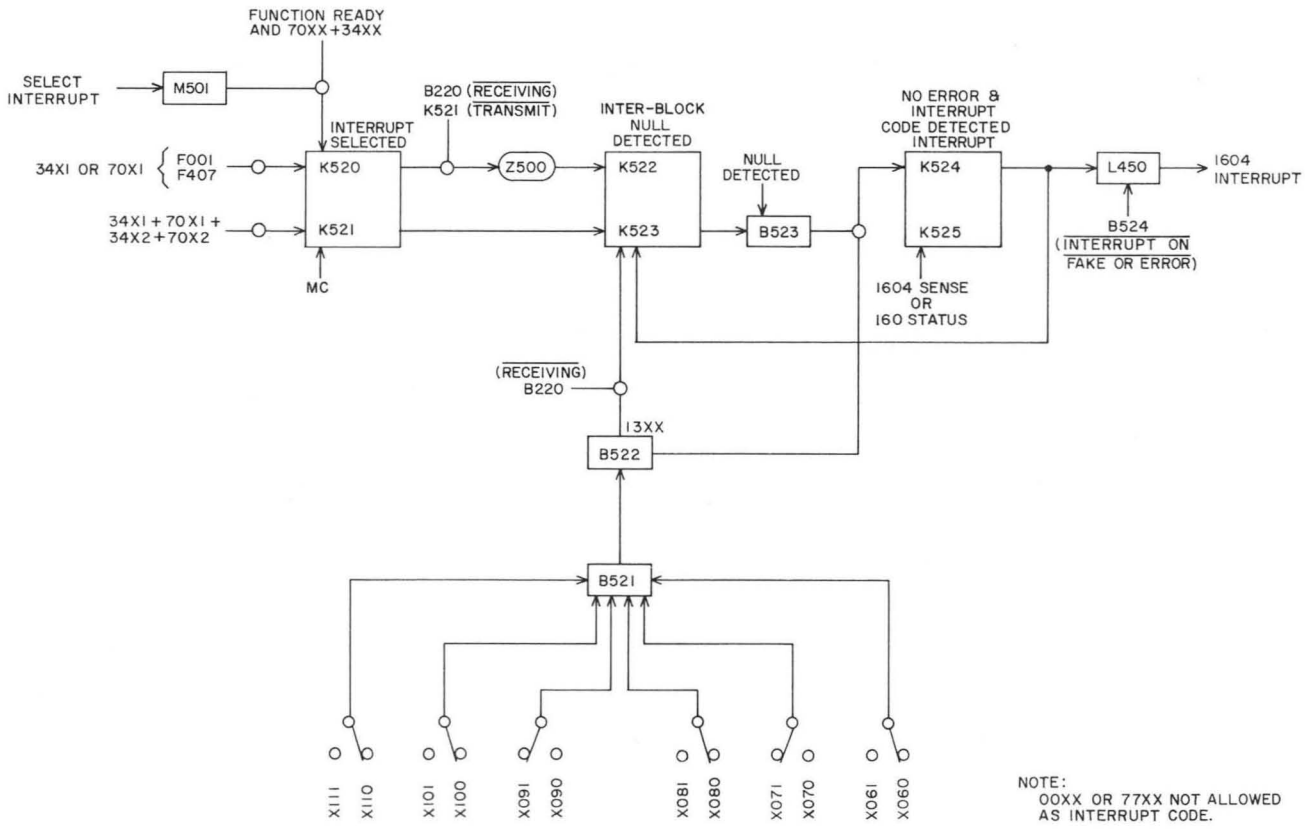


Figure 4-6. Interrupt Logic

OUTPUT RESUME

When the terminal equipment has been selected to transmit, a subsequent Output Ready signal (1604/1604-A) or Information Ready (160/160-A) indicates that a word is available on the output lines. A short delay permits the output word to stabilize before sampling. This enables an A → X transfer if the preceding word has been completely serialized, and triggers the Word Space Control, which at expiration sets the Timing Enable FF. The Sync FF then enables clock pulses to the frequency divider. Outputs from the frequency divider permit the Sample and Enable FFs to set in sequence. When the Drive Enable FF is set, the drive lines to the driver are enabled. An Output Resume is sent to the computer when the word has been serialized. The Output Resume causes the computer to drop the Output Ready, which in turn causes the terminal equipment to drop the Output Resume (figure 4-7).

The word space control delay (S18) determines the space between words and is variable at each installation. When a 160/160-A computer is at the receiving end, this delay must be switched in to prevent overrunning the computer.

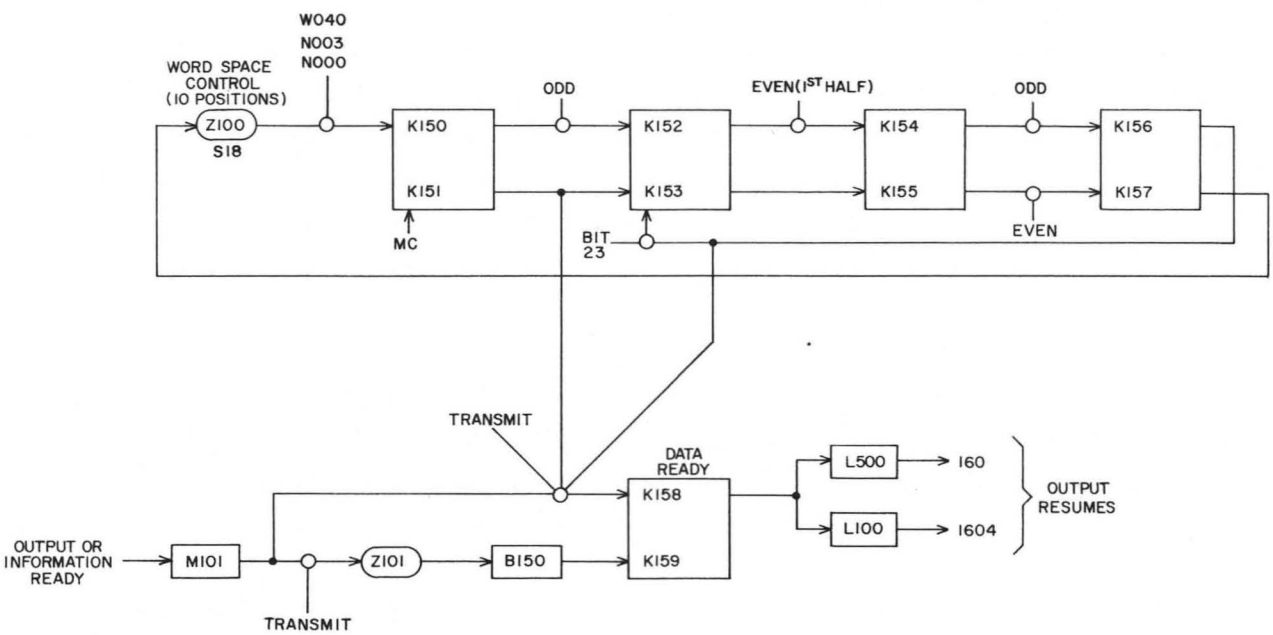


Figure 4-7. Output Resume

INPUT READY/RESUME (1604/1604-A)

When the terminal equipment is selected to receive, an Input Ready signal is sent to the computer as the last bit of the redundant word is received and made available to the computer. The computer recognizes the signal, accepts the word, and responds with an Input Resume signal. The Input Resume signal clears the Input Ready FF, causing the Input Resume to drop (figure 4-8).

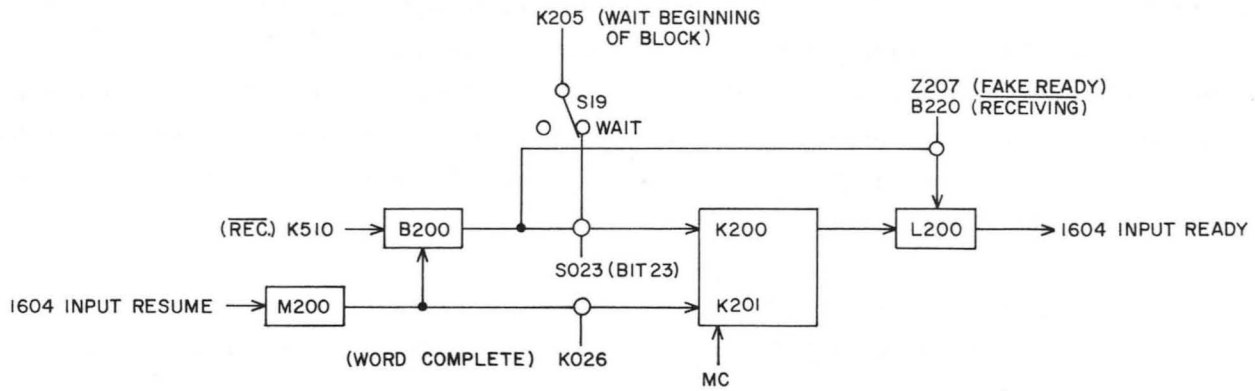


Figure 4-8. 1604/1604-A Input Ready/Resume

Procedural messages, when present, are always at the beginning of a block of data or in blocks preceding a block of data. Therefore, it is imperative that the computer not begin receiving elsewhere in a block. To prevent this, the Receive Selected Before Beginning of Block (RSBBB) FF is set only if there is no incoming data when receive is selected. An Input Ready signal can be sent to the computer only if this FF is set. If receive is selected while the terminal equipment is receiving, RSBBB FF will not be set until an inter-block null is recognized.

INPUT REQUEST/READY (160/160-A)

After transfer of the first word, the Input Request signal from the 160/160-A computer and the Input Resume from the 1604/1604-A serve the same purpose (figure 4-9). As with the 1604/1604-A, the RSBBB FF prevents an Input Ready signal from being sent to the 160/160-A until the beginning of the first block received after receive is selected.

The Input Active signal permits the 160 computer to accept data faster than is possible with normal repetitive Input Request signals. The Input Active signal is not used with the 160-A. If an Input Active signal is present, words can be transferred to the computer at a maximum rate of one every 14 usec.

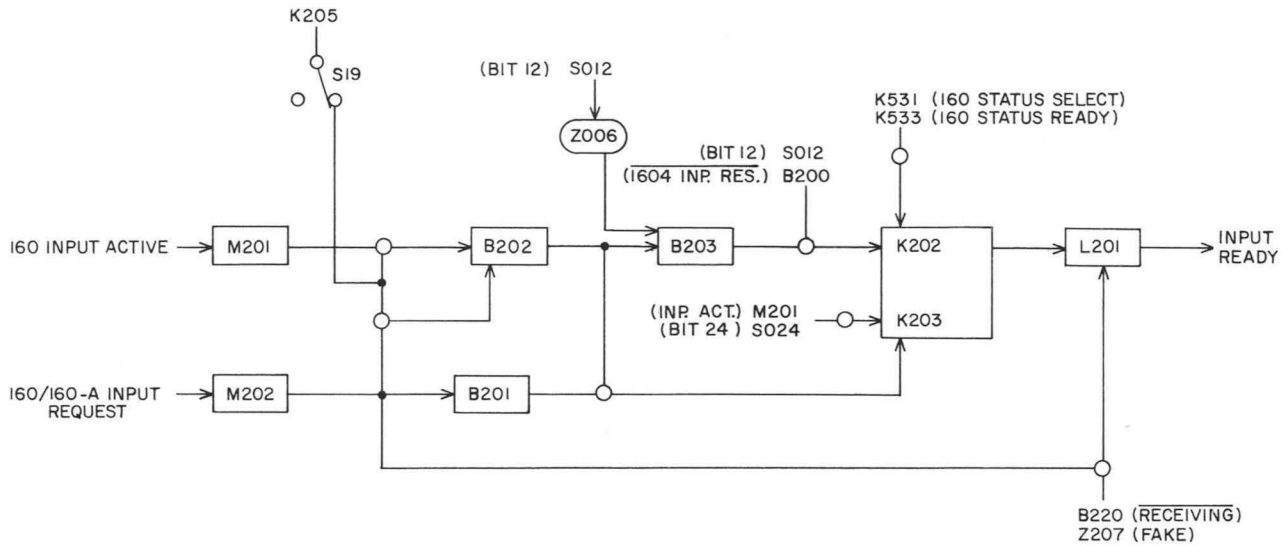


Figure 4-9. Input Request Ready

The 160/160-A Input Ready FF is set when the Input Request or Input Active signal is present and after bit 11 of the data word has been accepted by the A register. If the Input Active signal is up, the Input Ready FF is cleared when the null between words is recognized (figure 4-10).

If a 1604/1604-A is transmitting, the terminal equipment must be slowed down to prevent data from overrunning the 160/160-A.

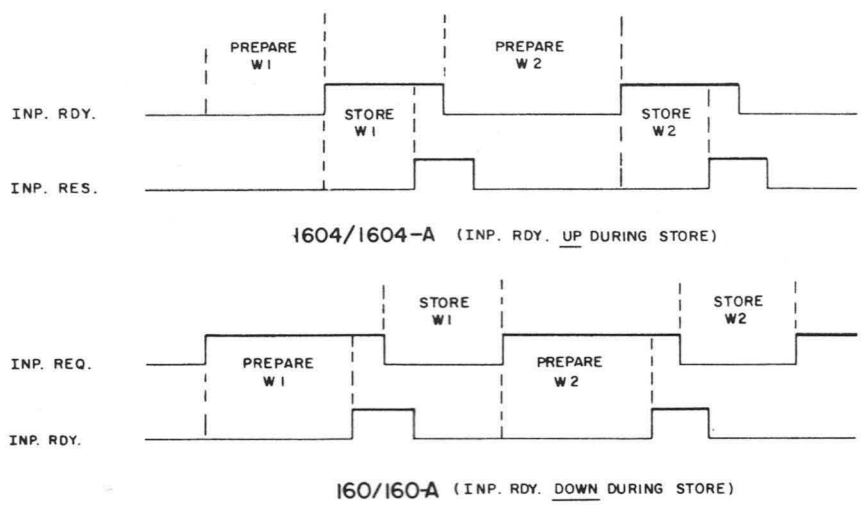


Figure 4-10. Ready/Resume Timing

FAKE READY TIME DELAY

The fake ready logic provides a timed wait for data after receive (input instruction) is selected. If data is not received before the timed wait period ends, the input instruction will be terminated by (1) a Disconnect signal if Disconnect on Fake (DOF) is used, or (2) repeatedly generating Fake Ready signals. The input instruction will also be terminated if the number of words received is less than the number of words requested by the computer.*

The fake ready logic sequence is initiated when receive is selected; the sequence stops when a sense or status request is made. The status request or sense code must be executed as soon as the input is terminated. Otherwise, the Fake Ready FF may set since receive will still be selected when all words have been received.

Delay Z207 determines the time between receipt of the last word in a block of data and the setting of the Fake Ready FF. This delay is adjustable from a minimum of 100 usec. It is set after the block is terminated.

If the [block length] x [receiving word rate] is greater than the delay of V200, the delay time will elapse before the block is terminated. This will cause a fake ready even though words are still being received. The interaction of B220 and Z207 prevents this condition from arising during normal operations if Z207 is set within minimum limits. The minimum limit must allow for program execution of a status request or sense code after input termination, and for the longest possible inter-word null to be received.

The delay time of V200 is determined by doubling the inherent delay in the transmission line and adding the time required for the other computer to evaluate and acknowledge receipt of the block. The setting of the 10-position rotary switch determines the delay time of V200; a fine adjustment can be made by varying the potentiometer on the CM12 card.

* In this instance the fake ready will cause the computer to store the contents of X (which contains the last word received) in all remaining storage addresses assigned to the block.

MAIN TIMING

The timing circuits sequence digital information out of the X register at a constant rate during transmission. During reception they are used to assemble serial data in the A register and time the comparison of the redundant word.

Transmission

Transmit timing is provided by a free running clock of a predetermined frequency. Clock output is shaped and divided by a 1:2 frequence divider. Both phases of the divider (arbitrarily called odd and even phases) are used (figure 4-11).

The baud counter is a chain of 13 FFs. The counter is started by the first even output of the frequency divider after an Output Ready signal enables the Timing Slave FF. Successive stages of the counter are set by alternating odd and even divider outputs and an enable is provided from a stage of the X register into the transmit pyramid. The 12-bit redundancy is gated out of X as each counter stage is cleared.

Reception

The master clock is disabled during reception and timing pulses are provided by the incoming serial information. Each complete cycle received toggles the Timing Slave FF, providing an input to the frequency divider. The counter, triggered by the frequency divider, enables each of the first 12 bits received into successive stages of the A register. The counter clears by stages, enabling comparison of each bit of the redundant word with the corresponding stage of the X register. The incoming redundancy and the X register are gated to the error detector for comparison.

TRANSMIT PYRAMID AND MIXER FF

The transmit pyramid is enabled by outputs from the baud counter and the X register. Each bit is made available to the pyramid for one complete clock cycle. To generate the characteristic serial waveform, the Mixer FF (figure 4-12) is forced to change state twice for each bit transmitted. This is accomplished by gating each bit with odd and even clock phases to opposite sides of the FF.

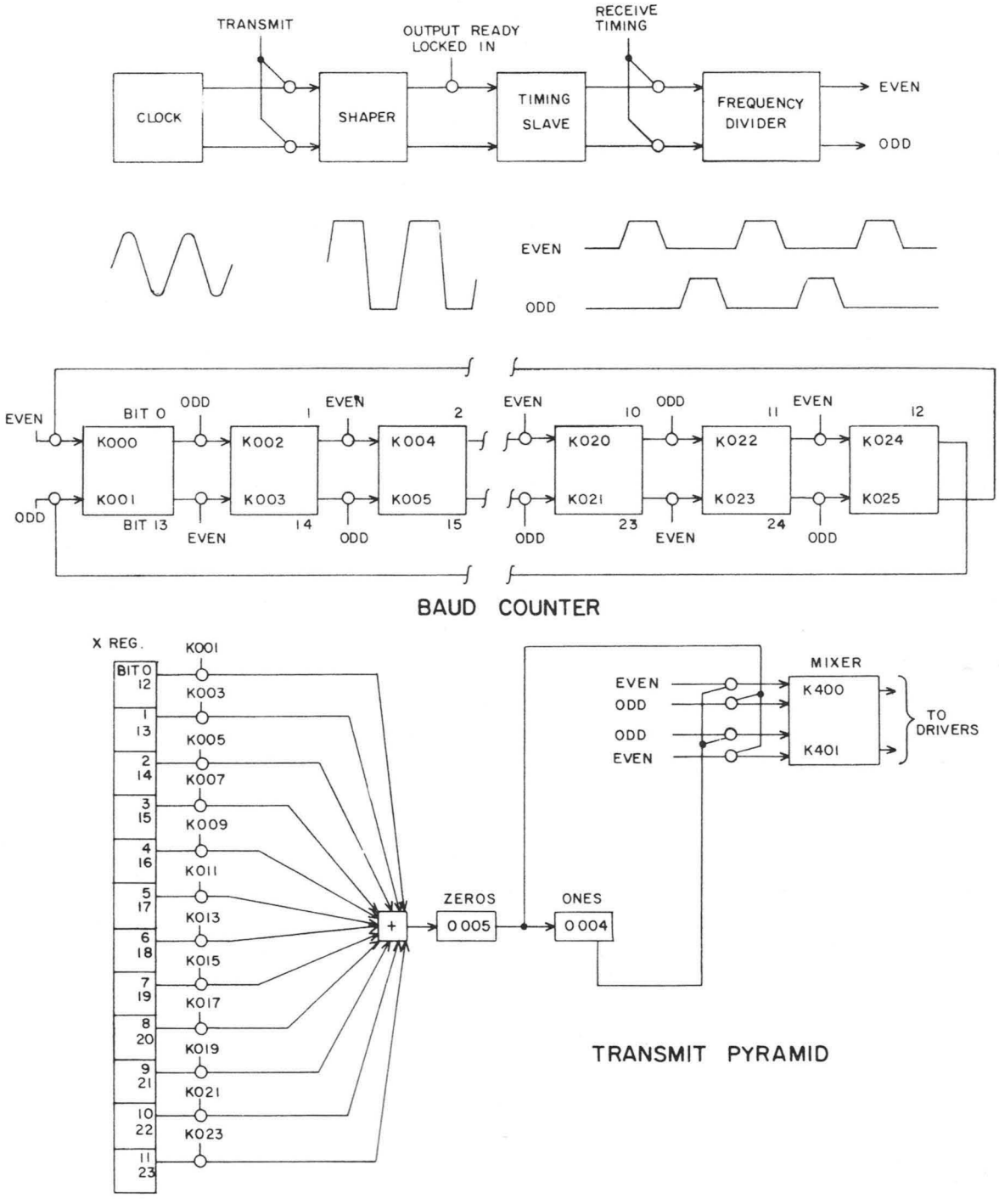


Figure 4-11. Transmission Circuits

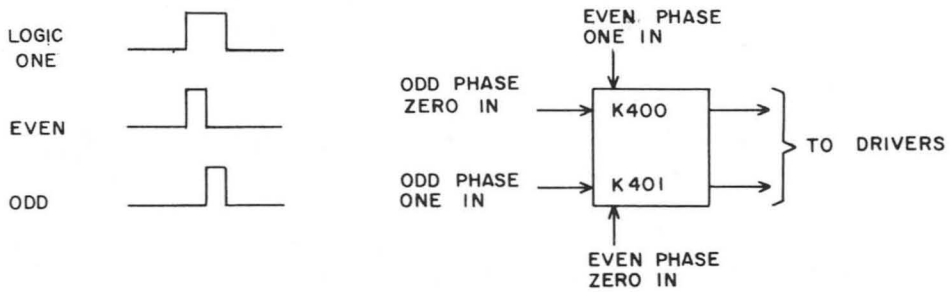
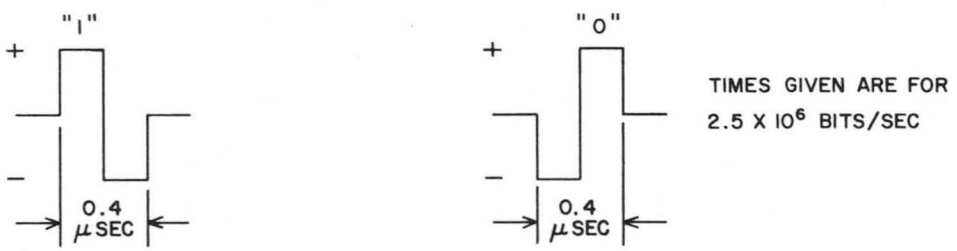


Figure 4-12. Mixer Input

To transmit a "1", the Mixer FF will be set during the first half cell cycle and be cleared during the second half cell cycle. To transmit a "0", the FF will be cleared during the first half cell cycle and set during the second half cell cycle, as shown below.



The entire transmit function is diagrammed in figure 4-13.

BIT AND TIMING DETECTOR

The bit and timing detector (figure 4-14) changes the incoming serial waveform to standard logic voltage levels and provides timing for word assembly and error detection.

Operation of the circuit is dependent on the first half cell cycle of every cycle. If the first half cell cycle is positive, a logical "1" is detected; if it is negative, a logical "0" is detected. In either case, the Sample-Advance FF sets (to Sample). The output of this FF triggers the Timing Slave FF and partially enables the baud counter. When the bit cycle changes direction, the Sample-Advance FF clears, advancing the baud counter. The counter enables the output of the detecting FF (set during the first half cell cycle) to the correct stage of A.

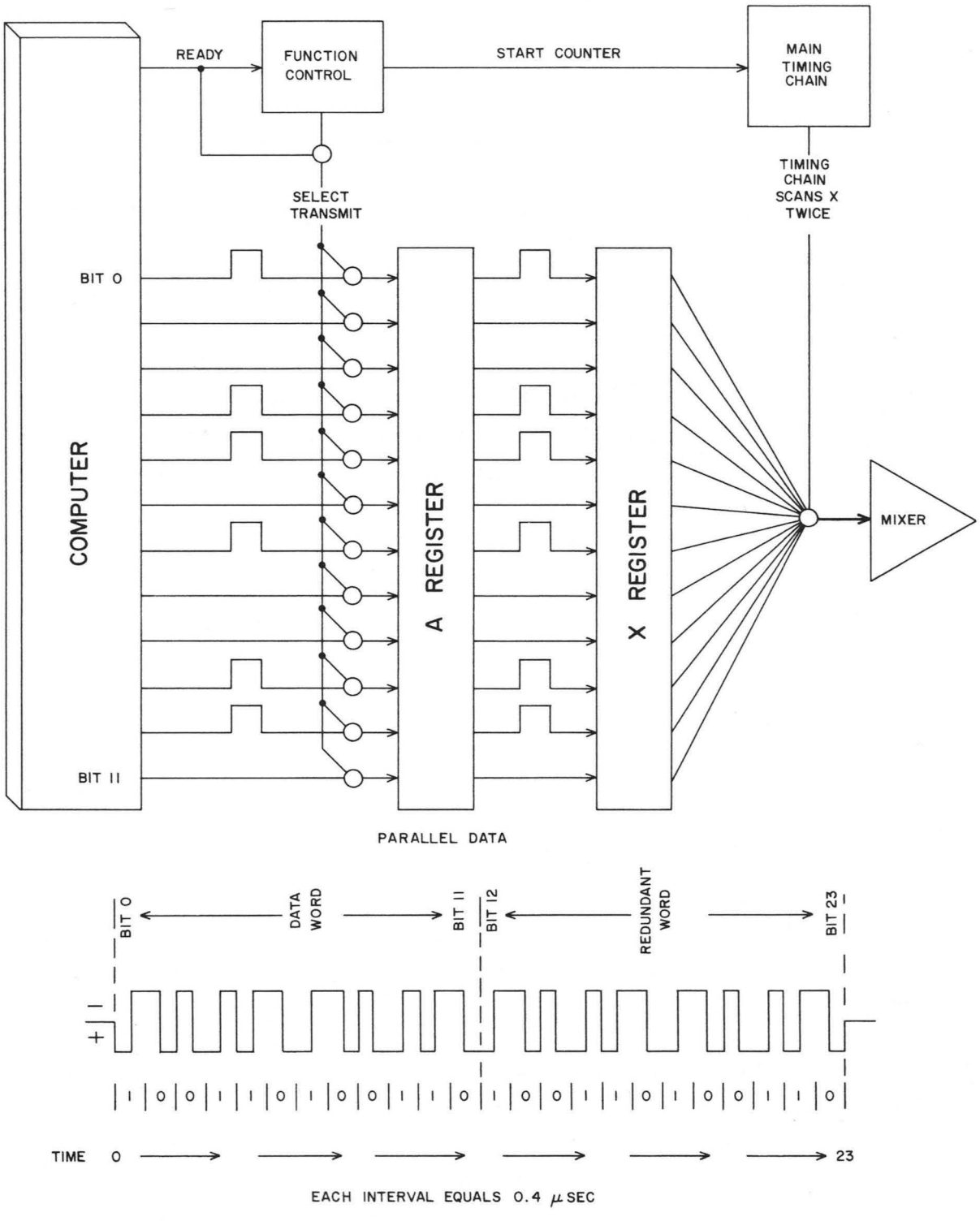


Figure 4-13. Transmit Pyramid and Output

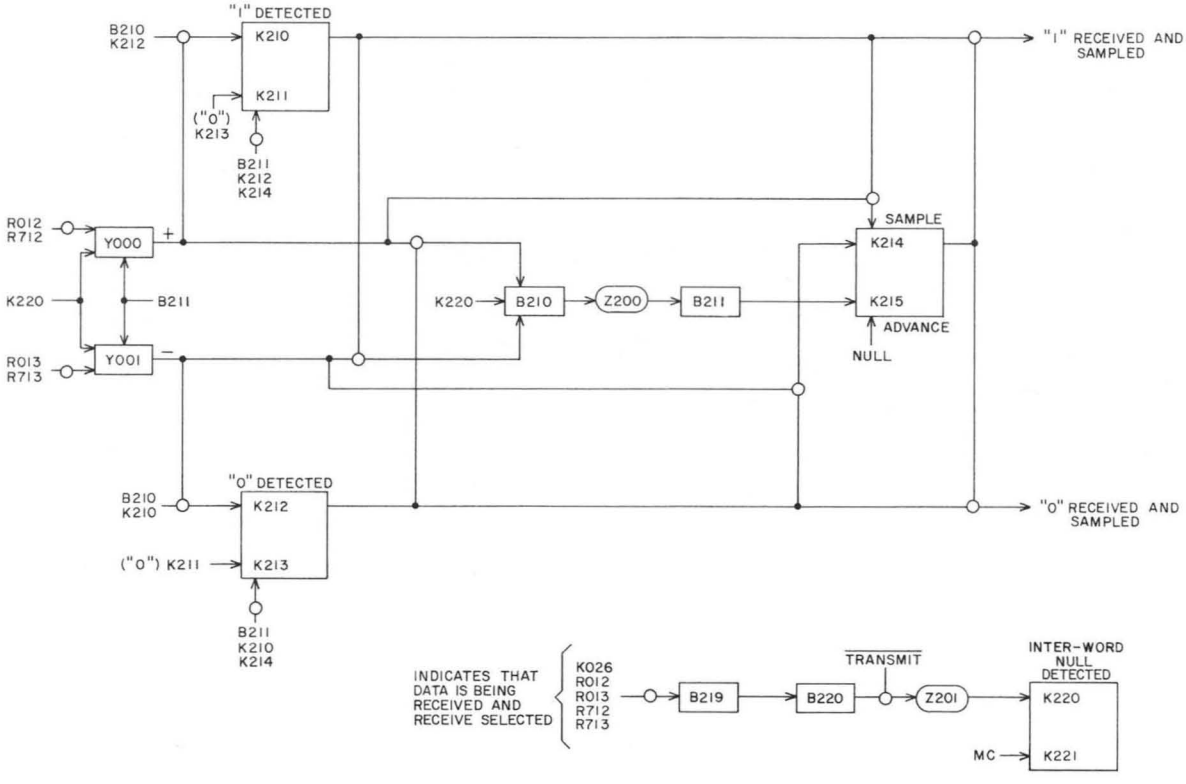


Figure 4-14. Bit and Timing Detector

At the end of each cycle, the output of B211 clears the detecting FF. Inverter B211 has a "1" output at the end of every cycle and acts as a driven clock with speed determined by the incoming data.

An absence of data at the threshold amplifiers for a period longer than delay Z207 signals the end of a block of data or a break in communication. The latter is detected as an incomplete transmission by the computer. The delay must be set to be longer than the null between words.

ERROR DETECTOR

Error detection is done dynamically at the receiving terminal equipment. The baud counter gates each incoming bit of the redundant word and the corresponding bit of the original word into a pyramid. If the two do not compare, the AND gate at the input to E040 or E041 will be broken, setting the Block Error FF and Word Error FF.

If the receiving terminal is connected to a 1604/1604-A computer, a word error will appear as a "1" in bit 23 position of the same storage location as the erroneous word.

When the 160/160-A is connected to the terminal, the error FFs must be interrogated by the computer. The 1604/1604-A can determine if an error exists in a block by sensing the Block Error FF.

AUDIO COMMUNICATION

A voice communication facility is provided with each data line. Any audio activity on the audio channels may be monitored by either the audio handset or a loudspeaker, both on the control head. With the handset removed from the cradle the loudspeaker is muted. The loudspeaker volume is controlled by adjusting the disk extending from under the right hand edge of the control head. The handset has a Push to Talk button on it.

If the peak data rate is greater than 0.5×10^6 bits/sec the audio may be carried over the data channel without interference.* A frequency selective switch circuit in the data amplifier (card type CM08) detects the presense of an audio tone on the audio channel to which the amplifier is connected. The audio signals are fed through a transformer and amplified further before going to a 4 inch speaker.

Operation of the audio facility is as follows:

Calling

1. Remove the handset from the cradle and select those lines on which the call is to be placed by pressing their respective Line Selector buttons.
2. Press the Call switch until all parties answer or until it is determined they are not available.
3. If, during use, another line indicator should light indicating a call on that line, the call may be answered by pressing the button for that line.
4. Replacing the handset on the cradle releases all line selections and places the loudspeaker back into operation on all incoming lines.

Answering Call

1. If an audio tone is heard over the loudspeaker, locate the line involved by noting which indicator is lit.
2. Remove the handset from the cradle and momentarily press the appropriate Line Selector button to engage the line.

* A peak data rate of less than 0.5×10^6 bits/sec requires a separate channel for audio communication.

CHAPTER V
INSTALLATION AND MAINTENANCE

INSTALLATION

The 8528 may be installed in any area that meets the requirements for a computer system. The cabinet should be easily accessible to the operator and to maintenance personnel and equipment.

Operating voltages (±20 vdc) are supplied by a constant voltage power supply at the base of the cabinet. The power supply operates from 110 vac 60 cycle power line; the d-c output will remain constant with input variations of from 95 to 135 volts. Power requirement is 450 watts.

The interior temperature of the cabinet is monitored by a thermostat on top of the chassis assembly. If the temperature exceeds $90^{o}F$ the thermostat opens, dropping all power. The thermostat will close automatically when the temperature drops below $90^{o}F$; power can then be reapplied by pressing the Power On switch.

The air filters (figure 5-1) should be cleaned or replaced when the equipment is down for maintenance.

Blowers, fuses and the thermostat are shown in figure 5-1.

The information cables between the computer and the 8528 enter the cabinet through an opening in the back. Maximum length of these cables is 50 feet; they are connected as shown in figure 5-2. Cable and pin designations are given in appendix A.

MAINTENANCE

Before attempting any maintenance, personnel should be thoroughly familiar with the logic and theory of operation. The equipment diagrams, publication 411, are the ultimate source of logic information. Special circuits used in the 8528 are described in appendix B.

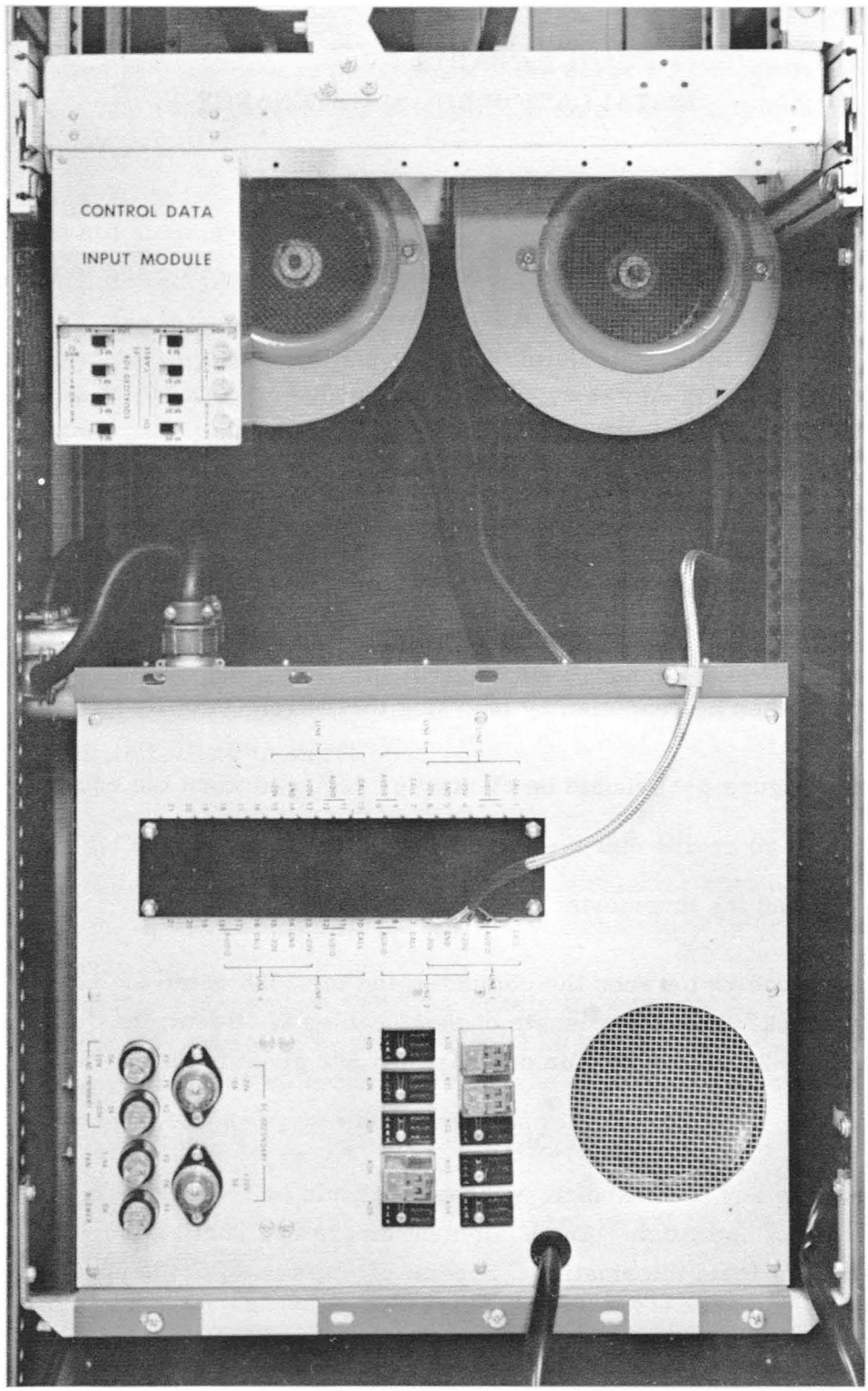


Figure 5-1. Cabinet Interior

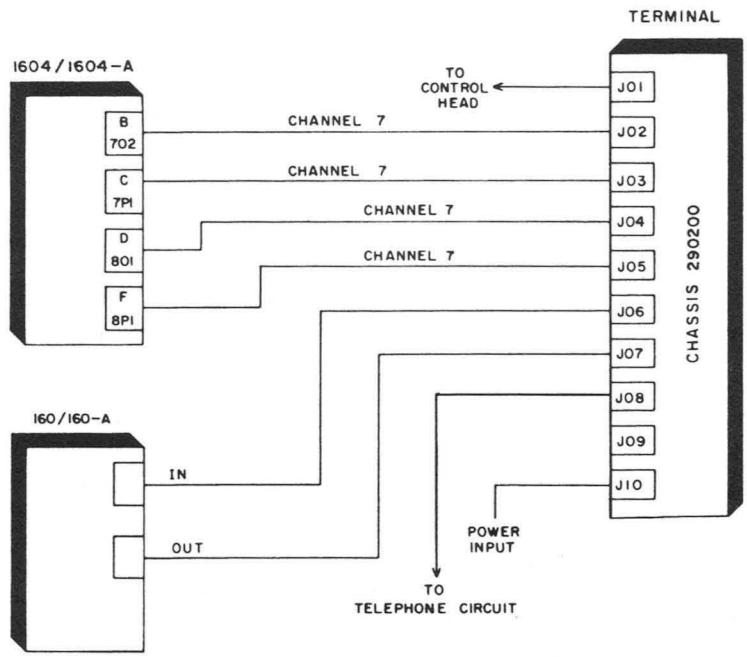


Figure 5-2. Cabling Diagram

SIMULATOR

The test simulator provides a transmission pattern for the serial communication channel which leaves the computer free. Using the simulator, the error detector, and a high speed oscilloscope, the receive or transmit logic can be checked as though the unit were in actual operation. (Refer to chapter II for simulator operation.) A "bursting" effect, which would occur during transmission of short blocks, can be simulated by manipulating the Transmit switch.

All communication channel parameters and margins can be set using the simulator.

DELAYS

Many of the delays in the terminal equipment can be adjusted over a limited range by varying the resistance in the RC time network or by minor variations in the capacitor value.

Rather than attempting to specify the time exactly, the delays should be adjusted according to their function within the circuit, relative to the requirements of the channel, program, and computer.

Delay	Function
V200	Fake ready wait length control. This delay can be adjusted to one of ten positions by the FRWLC switch on the chassis control panel. The delay should be long enough to allow the receipt of the first word of a block. Usually the delay can be set to two times the inherent transmission path delay plus the time necessary for the other computer programs to evaluate the block and reply.
Z001, Z002	These two delays work together to form a sample pulse out of F401. Z001 should be at least 2 usec to allow the logic cables to settle; Z002 should be 0.5 usec longer than Z001. Z002 prevents an Output Resume from being returned to the computer prematurely. When the 8528 is connected to a 160/160-A these delays prevent a status check from occurring until the last word is completely checked.
Z003, Z004	These are 0.1 usec fixed delays. They delay clearing the Status Ready or Sense Ready FF until all the interrogated FFs have been cleared.
Z005	A fixed 0.1 usec delay which prevents the Status Select FF from being cleared immediately after an Input Active or Input Request has been dropped.
Z006	A fixed 0.1 usec delay which, at low bit rates, prevents K203 from setting more than once during S012.
Z027	A fixed 0.1 usec delay which clears K027 automatically.
Z100	Word space control delay which is wired to a 10-position rotary switch for selecting different delay times. Once the switch is set the delay can be varied ±15% using the potentiometer on the delay card.

Delay		Function
Z100 (Cont'd)	Switch Setting	Delay
	A, B, C, D	Capacitors are required for other delay times
	E	5 usec
	F	10 usec
	G	25 usec
	H	50 usec
	J	100 usec
	K	600 usec

Z200 Once B210 goes to "0", this delay holds a "0" in B211 until the center of the first half cell cycle of a bit period. In effect, this provides a forced clear on K214, K210, K212 and holds a "1" in Y000 and Y001 until the center of the first half cell cycle. For bit rates between 500 kc and 5 mc, pulse delay lines are used in location A53; below 500 kc, a CM12 is used in location A54.

When a CM12 is used, the delay should be set to approximately 3/4 of the cell period. For example, at 10 kc the total delay from the time B210 drops to "0" to the time B211 returns to "0" should be approximately 3/4 of $\frac{1}{10 \times 10^3}$ (75 usec). In the case of a pulse delay line the same rule applies, but since a delay line delays both the leading and lagging edge of a pulse, the delay should be set to 3/8 of the cell period. This gives an over-all delay of 3/4 cell period.

Z201 This is the inter-word null delay and should be adjusted to a value equal to 3/4 the minimum null between words in a system, subject to special requirements. It is adjustable ±15% and can be made equal to 5, 10, 25, 50, 100 or 600 usec or combinations of those values by inserting jumper wires on the connector.

Z205 A variable delay which is used to condition the Wait Beginning of Block FF such that it will set only if a null greater than the maximum null between words is detected. It is adjustable in the same manner as Z201.

Delay	Function
Z207	This delay should be at least 10% greater than the maximum null between words and no less than 100 usec, whichever is greater. It is adjustable in the same manner as Z201.
Z500	This delay should be adjusted to be equal to Z207 unless there are special requirements. It is adjustable in the same way as Z201.
Z600	This delay helps to detect the absence of timing when receiving data. It should be set to a value slightly less than 1/2 cell period. To establish the setting of this delay: 1) Adjust the attenuator to the maximum limit where no errors are detected by comparison. 2) Check (X) against the incoming data. 3) Check E000, E010, E020, E030, E001, E011, E021, and E031 to see that the redundancy also checks. If not, the maximum limit is being exceeded. 4) Adjust Z600 so that B600 = "1". Then increase the attentuator beyond the maximum limit by 0.5 db. B600 should occasionally go to "0" and errors should be made. This allows Z600 to distinguish between the minimum pulse width permissable (as represented by the time that B220 is a "1" during the word) and to make the detection of an error coincide with the occurrence of the error.

SERIAL COMMUNICATION CHANNELS

710 Input Module

The 710 input module contains the equalizers, attentuators, and video amplifiers for the serial communication channels.* At fixed installations, where channel parameters will not vary, the amount of equalization necessary will be determined during installation. This will be recorded on the decal on the module. Spare input modules must be purchased if the channel parameters are subject to change.

* Equivalent attenuation-equalization may be provided without the input module, but this will not allow transmission and reception on a single cable unless special consideration is given to termination. Termination must be such that the data drivers may be placed ahead of the equalizer-attenuator.

The amplitude of the output signal from the line drivers is approximately 20v p-p. Over long reaches of coax, this signal may drop off considerably and invariably high frequencies are attenuated more than low frequencies. To offset the high frequency attenuation, an equalizer at the receiving end equally attenuates the low frequencies. The amount of equalization needed must be determined at each installation. The equalizers are designed for specific lengths and types of coaxial cable.

The bandwidth of the video amplifiers is controlled to keep audio signals out of the threshold amplifiers. The input coupling capacitor is the controlling element; in general, if more than one amplifier is necessary, the input capacitance of the first amplifier is kept small in relation to that of the second amplifier.

If the equalized signal drops below 50 mv p-p, an additional video amplifier is used to increase the signal strength. A signal of at least 0.6v p-p is required to drive the 2.5×10^6 bits/sec threshold amplifiers. At least one video amplifier will usually be necessary to provide power gain.

Attenuators prevent overdriving the video amplifiers. If it is necessary to cascade video amplifiers, the output of one of the first stages may be large enough to overdrive the following stage but not large enough to drive the threshold amplifiers. Diagrams for the attenuators, video amplifiers, and equalizers are in appendix B.

Requirements for connector exchange boxes, video amplifiers, drivers, attenuators, equalizers, pads and Tee pads must be determined after the installation has been fully specified (i.e., type of cable, length, impedance, and environmental limitations). Some recommendations can be made in view of conditions relative to the site and the required reliability.

Coaxial Cable Characteristics

The input module and the 8528 use type 31-223 and 31-224 Amphenol connectors for serial interface connections. For internal short cable runs RG-108/U is used. For reaching the serial channel connections the same cable (RG-108/U) may be used externally for runs of up to 10 feet at 2.5×10^6 bits/sec.

The frequency response of RG-108/U is not predictable and therefore this cable cannot be equalized. However, at a frequency of 2.5×10^6 bits/sec, short runs (up to 1000 feet) of this cable can be used safely.

With an input of 20v p-p, 66 db of loss in the cable and equalizer is the maximum allowable in order to yield the required 10 mv p-p of input voltage. A signal to noise ratio of at least 3 to 1 or 10 db is necessary for reliable operation.

Table 5-1 gives the maximum allowable lengths of cable where there is less than 3.5 mv p-p of noise at the receiving end and a peak bit rate of 2.5×10^6 bits/sec.

TABLE 5-1. MAXIMUM CABLE LENGTHS

Cable Type	*Usable Length at 2.5×10^6 bits/sec.
RG 8, 9, 10, 11, 12, 13	to 5 miles
RG 17, 18, 35, 84, 85	to 8 miles
16 PSVL	to 3.6 miles
RG-59/U	to 1.8 miles
RG-22/U	to 1.5 miles
RG-108/U	to 1000 feet

At lower peak bit rates the cable length can be longer. In this case equalizer redesign is necessary.

If balanced cable is used equalization will not usually be possible if an inflection occurs in the frequency response curve within the required data frequency spectrum.

* These lengths must be reduced by at least one half if transmission and reception is to be on a single cable.

Best equalization results can be expected when the bit rate frequency is before the knee* of the cable response curve (figure 5-3a).

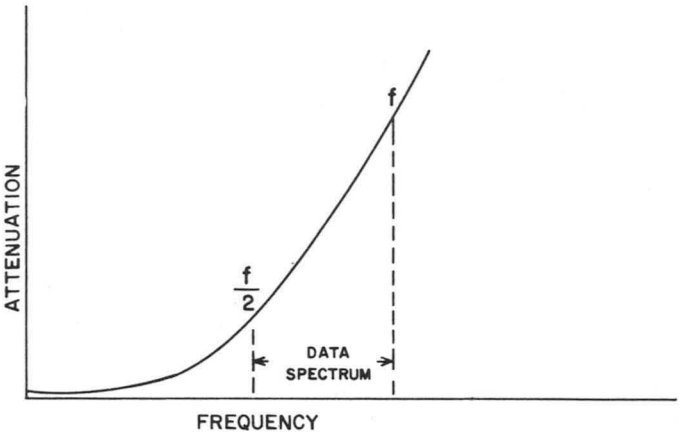


Figure 5-3a. Cable Response Curve (Best)

The poorest results can be expected when the bit rate and half bit rate frequencies straddle the knee of the cable response curve (figure 5-3b).

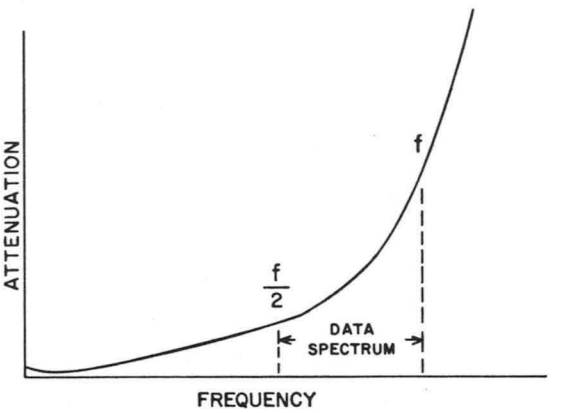


Figure 5-3b. Cable Response Curve (Poor)

* The "knee" refers to the sharp change of slope of the cable response curve when plotted on semi-log graph paper.

Good equalization may be obtained when the half bit rate and bit rate frequencies tend to lie on a similar slope, just after the knee of the cable response curve (figure 5-3c).

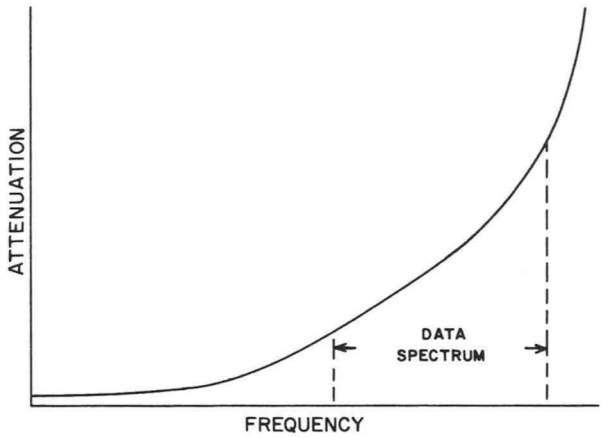


Figure 5-3c. Cable Response Curve (Good)

Noise

In a noisy environment a balanced coaxial cable is preferrable to a single center cable since it affords common mode rejection by differential detection. In most instances, however, single center conductor cable is adequate.

When the coax run is through a high energy electric field, it must be well shielded. If a pair of conductors is cut by a high gradient magnetic field, the proximity of the conductors is more important than when the gradient is small. For example, two parallel RG-11/U cables in the same shield may be adequate for some noise situations but 16 PSVL may be the necessary cable in others.

If the coax is to be subjected to mechanical stress, corrosive atmosphere or other detrimental conditions, suitable precautions should be taken.

Microwave

If microwave is used as the serial communication channel, the requirements for connector exchange boxes, attentuation, amplification, equalization pads, and Tee pads will be considerably different from those for a coaxial cable. Equalizing coaxial cable signals is ordinarily a necessity but is not necessarily a factor in microwave communications because the equipments usually require only a short interconnecting coaxial cable. The microwave equipment should be specified prior to the installation. Requirements and margins will be determined at the installation.

APPENDIX A
CABLING

TABLE A-1. CABLE IDENTIFICATION (1604/1604-A)

Cable Group One	A/7J2	Cable Group Three	A/7M2
	Ch. 1-2		Ch. 5-6
	B/7K1		B/7N1
	Ch. 1-2		Ch. 5-6
	C/7K2		C/7N2
	Ch. 1-2		Ch. 5-6
	D/8J2		D/8M2
	Ch. 1-2		Ch. 5-6
	E/8K1		E/8N1
	Ch. 1-2		Ch. 5-6
	F/8K2		F/8N2
	Ch. 1-2		Ch. 5-6
Cable Group Two	A/7L1	Cable Group Four	A/7O1 **
	Ch. 3-4		Ch. 7
	B/7L2		B/7O2
	Ch. 3-4		Ch. 7
	C/7M1		C/7P1
	Ch. 3-4		Ch. 7
	D/8L1		D/8O1
	Ch. 3-4		Ch. 7
	E/8L2		E/8O2 **
	Ch. 3-4		Ch. 7
	F/8M1		F/8P1
	Ch. 3-4		Ch. 7

Group 1
channel 1 - buffer input
channel 2 - buffer output

Group 2
channel 3 - buffer input
channel 4 - buffer output

Group 3
channel 5 - buffer input
channel 6 - buffer output

Group 4
channel 7 - transfer input and output

* Cable tag identifies connection point in computer. For example, A/7J2 indicates cable A of group one connects to chassis 10700 at location J2.
** The cables are not used with the terminal equipment.

TABLE A-2. PIN ASSIGNMENTS, COMMUNICATION CABLES (1604/1604-A)

Wire Color (Nema)	Pin No.	Input Buffer or Transfer Channel			Output Buffer or Transfer Channel		
		Cable A	Cable B	Cable C	Cable D	Cable E	Cable F
0	A	bit 47	bit 24	bit 01	bit 00	bit 23	bit 46
2	B	46	23	00	01	24	47
4	C	45	22	Input Data Ready[2]	02	25	Output Data Ready[2]
5	D	44	21	Input Data Resume[2]	03	26	Output Data Resume[2]
6	E	43	20	Input Buffer Active[1]	04	27	Interrupt
90	F	42	19	External Master Clear	05	28	Input Function Ready[1]
91	H	41	18	NU	06	29	Input Sense Ready[1]
92	J	40	17	NU	07	30	Output Function Ready
93	K	39	16	NU	08	31	Output Sense Ready
94	L	38	15	NU	09	32	Sense Response
95	M	37	14	NU	10	33	Output Buffer Active[1]
96	N	36	13	NU	11	34	Function Bit 00
97	P	35	12	NU	12	35	01
98	R	34	11	NU	13	36	02
900	S	33	10	NU	14	37	03
910	T	32	09	NU	15	38	04
920	U	31	08	NU	16	39	05
930	V	30	07	NU	17	40	06
940	W	29	06	NU	18	41	07
950	X	28	05	NU	19	42	08
960	Y	27	04	NU	20	43	09
970	Z	26	03	NU	21	44	10
980	a	25	02	NU	22	45	11
990	b	grd	grd	grd	grd	grd	grd

1. Buffer cable only, unused in transfer. Input/Output Buffer Active signals designated Input/Output Transfer Active in Transfer Channel.
2. Input/Output Data Ready/Resume signals designated Input/Output Transfer Ready/Resume in Transfer Channel

TABLE A-3. CABLE IDENTIFICATION (924/924-A)

Cable Group 1

- A/3A2 CH 1-2
- B/3B1 CH 1-2
- C/4M1 CH 1-2
- D/1A2 CH 1-2
- E/1B1 CH 1-2
- F/4K2 CH 1-2
- 160 MODE/1D2 Output Cable
- 160 MODE/3D2 Input Cable

Cable Group 2

- A/3B2 CH 3-4
- B/3C1 CH 3-4
- C/4M2 CH 3-4
- D/1B2 CH 3-4
- E/1C1 CH 3-4
- F/4L1 CH 3-4
- 160 MODE/1E1 Output Cable
- 160 MODE/3E1 Input Cable

Cable Group 3

- A/3C2 CH 5-6
- B/3D1 CH 5-6
- C/4N1 CH 5-6
- D/1C2 CH 5-6
- E/1D1 CH 5-6
- F/4L2 CH 5-6
- 160 MODE/1E2 Output Cable
- 160 MODE/3E2 Input Cable

Group 1:
Channel 1 - buffer input
Channel 2 - buffer output

Group 2:
Channel 3 - buffer input
Channel 4 - buffer output

Group 3:
Channel 5 - buffer input
Channel 6 - buffer output

NOTE: Each label indicates cable by a prefix letter. The expression following the slash gives the computer connector for the cable.

TABLE A-4. CONNECTOR PIN NUMBER ASSIGNMENTS
(924/924-A)

Pin No.	Input Buffer Channel			Output Buffer Channel		
	Cable A	Cable B	Cable C	Cable D	Cable E	Cable F
A	bit 47	bit 24	bit 01	bit 00	bit 23	bit 46
B	46	23	00	01	24	47
C	45	22	Input Ready	02	25	Output Ready
D	44	21	Input Resume	03	26	Output Resume
E	43	20	Input Buffer Active	04	27	Interrupt Function
F	42	19	External Master Clear	05	28	Input Function Ready
H	41	18	Not Used	06	29	Input Sense Ready
J	40	17	↑	07	30	Output Function Ready
K	39	16	|	08	31	Output Sense Ready
L	38	15	|	09	32	Sense Response
M	37	14	|	10	33	Output Buffer Active
N	36	13	|	11	34	Function Bit 00
P	35	12	|	12	35	↑ 01
R	34	11	|	13	36	| 02
S	33	10	|	14	37	| 03
T	32	09	|	15	38	| 04
U	31	08	|	16	39	| 05
V	30	07	|	17	40	| 06
W	29	06	|	18	41	| 07
X	28	05	|	19	42	| 08
Y	27	04	|	20	43	| 09
Z	26	03	|	21	44	| 10
a	25	02	↓	22	45	↓ 11
b	GRD	GRD	GRD	GRD	GRD	GRD

TABLE A-5. PIN ASSIGNMENTS, INPUT/OUTPUT CABLES (160/160-A)

Normal Input and Buffer Input Cable	Pin	Normal Output and Buffer Output Cable
Bit 0 input status and information	A	Bit 0 output function and information
1	B	1
2	C	2
3	D	3
4	E	4
5	F	5
6	H	6
7	J	7
8	K	8
9	L	9
10	M	10
11	N	11
	P	
Input Ready	R	Information Ready
Input Request	S	Output Resume
Input Active	T	Function Ready
	U	Master Clear
Input Disconnect	V	Output Active
	W	
	X	
	Y	Interrupt 30
	Z	Interrupt 40
	a	
Ground	b	Ground

APPENDIX B

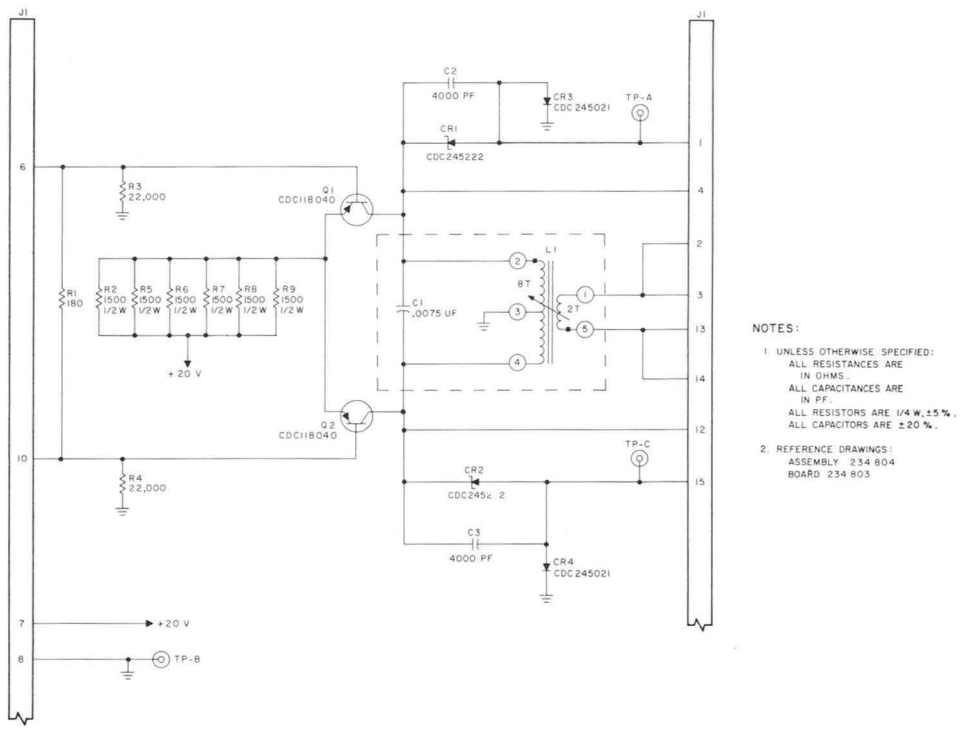
SCHEMATICS

The special printed circuit cards on the following pages are shown and described for operation at 2.5×10^6 bits/sec. Operation at other frequencies may require component changes on some cards; components affected are shown with dotted lines.

CM01 - CLOCK OSCILLATOR AMPLIFIER

This circuit provides the clocking for the 8528 logic during transmission. By varying the value of C1 or both C1 and L1 the oscillator frequency can be varied from 0.5×10^6 to 8×10^6 cps. The oscillator is also adjustable by means of a slug tuned coil.

Two of these circuits are used in parallel to prevent overloading.



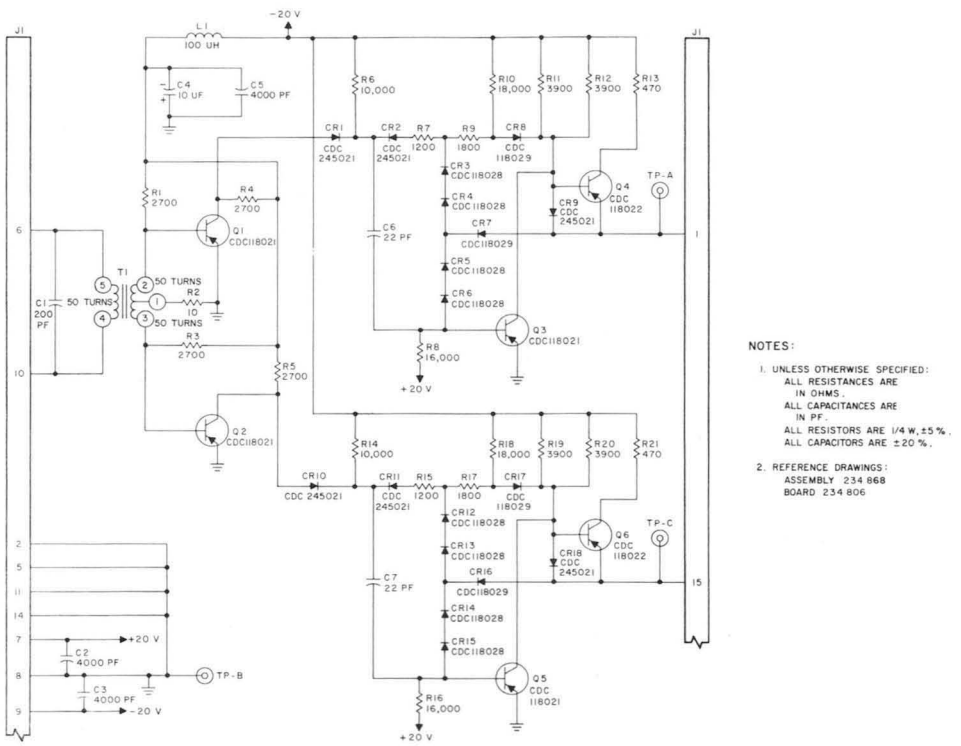
CM02 - BIPOLAR THRESHOLD AMPLIFIER

This circuit is driven by the balanced split phase input signal from the 710 input module. The signal is converted into standard two level logic signals to drive the logic circuits during reception. One circuit is required for each data line.

With no signal applied, Q1 and Q2 are non-conducting and the output of pins 1 and 15 are "0". If a -0.3v signal is applied to the base of either transistor, the output at pin 1 or pin 15 will be a "1".

The circuit is subject to variation dependent on bit rate. For example, if the bit rate is so low as to require a rather large transformer which cannot be mounted on the card, the transformer will be mounted between the coaxial connectors on the chassis 290100 frame. In some instances a coupling network may be used rather than a transformer.

The bias on the base of Q1 and Q2 is established by the d-c resistance of the transformer secondary and should not exceed 10 ohms per half. If the transformer secondary exceeds 10 ohms per half, or if a coupling network is used, a resistor network is used to compensate.

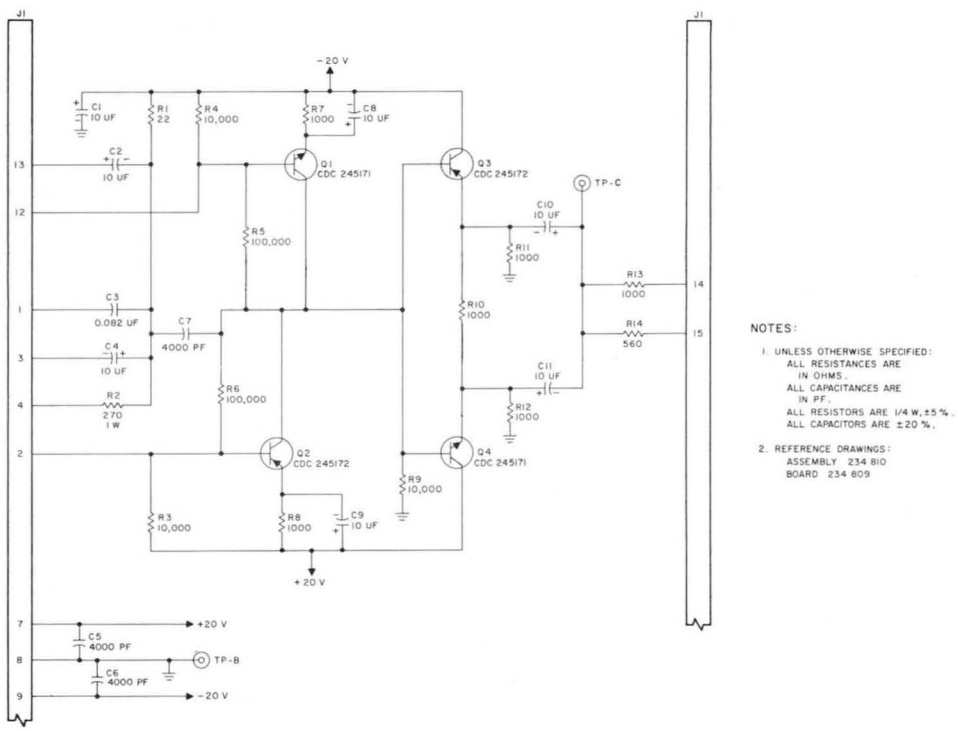


CM03 - AUDIO TRANSMIT AMPLIFIER

The output of CM03 is fed into a low pass filter which in turn drives the audio line drivers (CM06). The output of this circuit is limited to approximately 0.6v peak-to-peak to prevent very large signals from being put on the data line. The output is subsequently filtered by the low pass filter before being applied to the relay selected audio line driver.

The circuit has two inputs. When calling, the output of a tank circuit is fed to the CM03 to place the call signal on the audio channel. It is also fed by the output of the microphone in the handset.

Besides the limited output to the low pass filter, an output 180^{o} out of phase with the circuit is provided for feedback into the Audio Receive Amplifier (CM04) to produce a side tone.

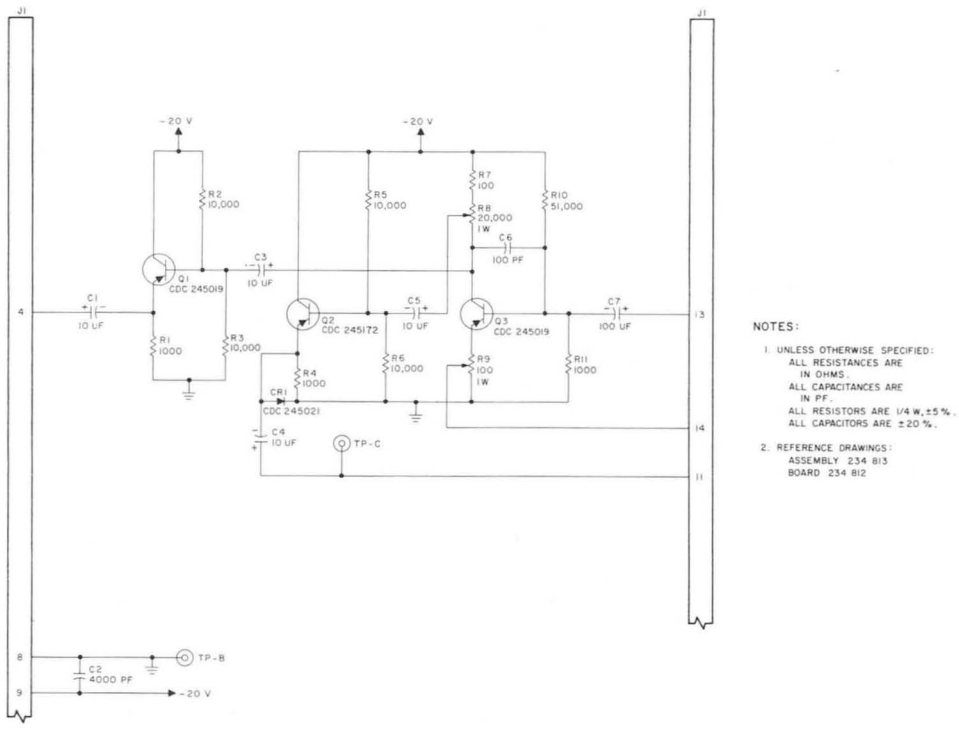


NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 234 810
   BOARD 234 809

CM04A - AUDIO RECEIVE AMPLIFIER

The CM04 amplifies the mixed outputs of the Audio Differential Amplifier for the speaker or earphone of the handset. An input from the transmit amplifier produces the side tone, controlled by R9. The gain is adjustable by means of R8 (20K pot).

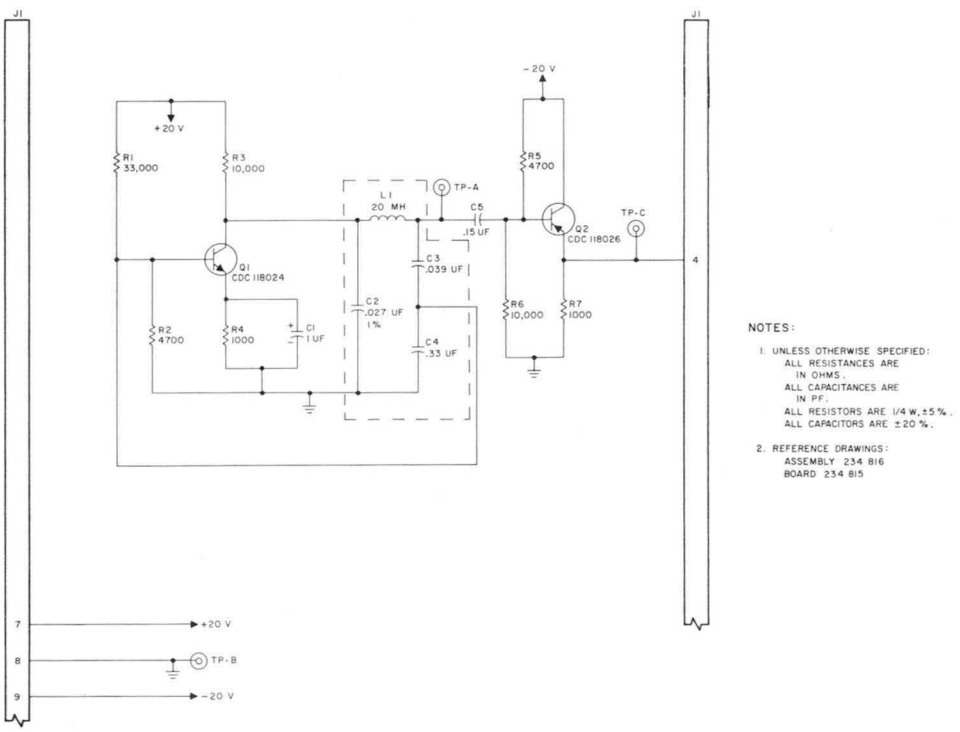


CM05 - LOW FREQUENCY OSCILLATOR

This is a modified Clapp oscillator circuit that serves with the Phase Splitter, CM09, as a clock oscillator at lower bit rates. The circuit shown is designed for 10 kc operation. Both CM05 and CM09 can be substituted for CM01's without wiring changes.

Q1 and associated circuit components act as the modified Clapp oscillator. L1 and C2 are the frequency determining components. L1, C2 and C3, C4 change with frequency requirements.

The oscillator can be provided with an adjustable coil in place of the fixed inductor in the tank circuit. In this case the card must be placed next to an empty location.

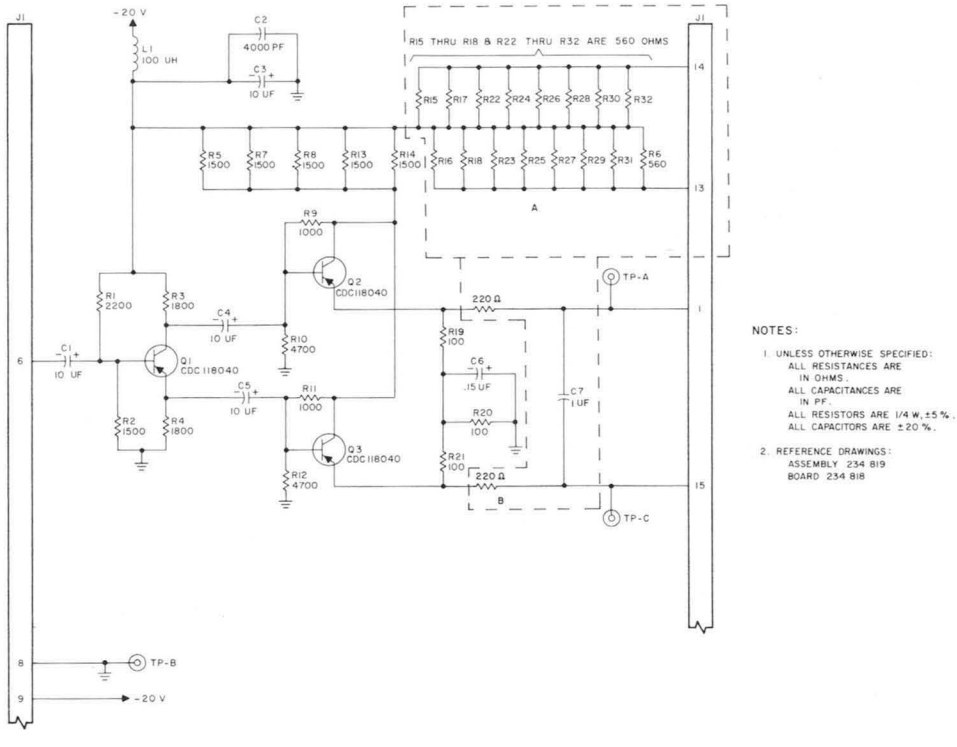


CM06 - POWER GAIN PHASE SPLITTER

This circuit is normally intended to serve as the audio line driver. When selected it converts the single ended signal produced by the CM03 circuit into a differential balanced signal suitable for driving a 75 ohm line. One circuit is required for each audio line and each data line.

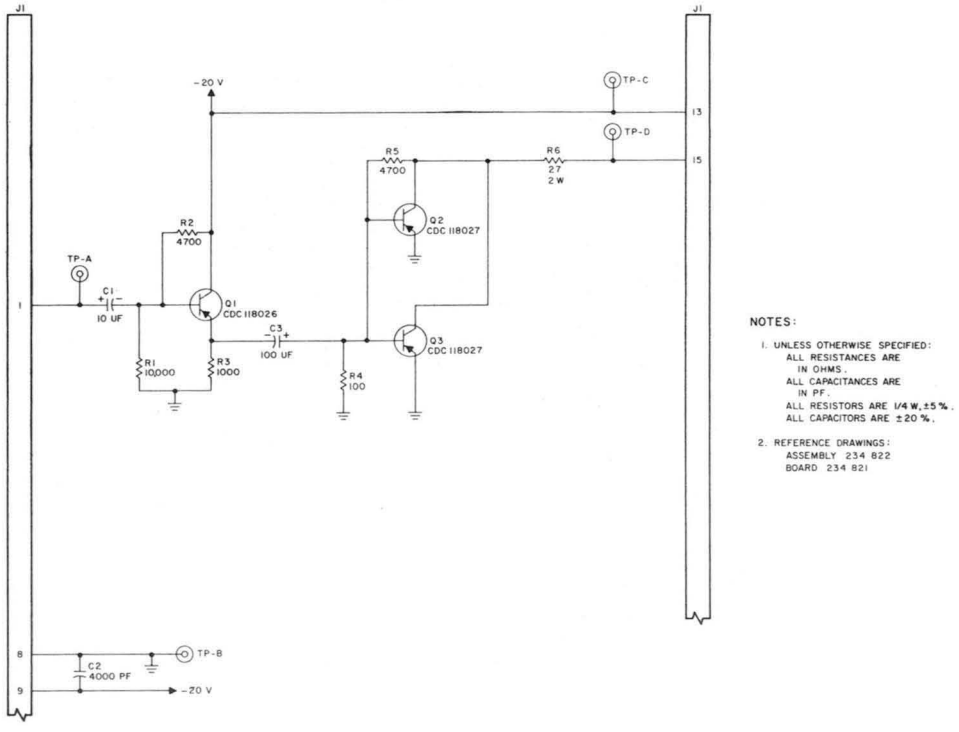
C7, the 1.0 uf capacitor across pins 1 and 15, serves to complete the secondary of the Data Driver Transformer of the CM11 circuit at the bit rate frequency, and provide for high impedance at the low frequency.

The circuit shown is designed for data frequencies of at least 0.5×10^6 bits/second. Lower bit rates require a separate audio channel.



CM07 - SPEAKER DRIVER AMPLIFIER

This circuit drives a 45 ohm intercom type speaker in the control head. An input from the CM04 circuit is present when the handset is on the cradle. The volume control is placed in series with the input.

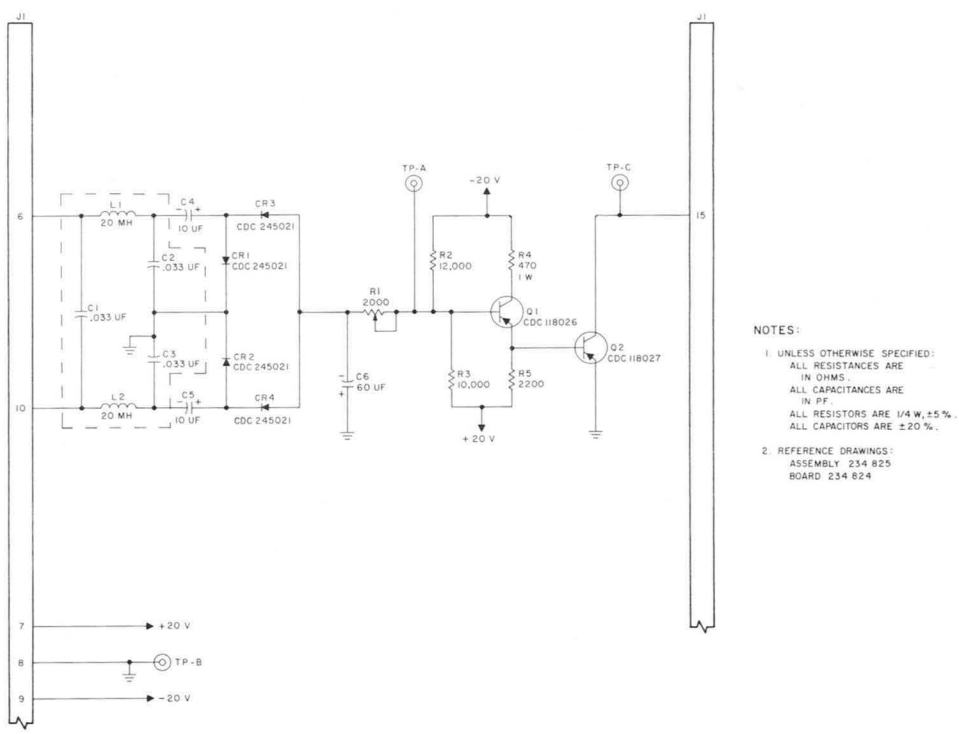


CM08 - FREQUENCY SELECTIVE SWITCH

This circuit lights a parallel pair of GE 327 bulbs when an audio tone of a preset level is present on the audio channel. One is required for each audio line and each data channel. The card is located in the 710 input module for that line.

The circuit consists of two series resonant tank circuits made up of L1 and C2, and L2 and C3. The signal amplitude at the node between L1 and C2 and L2 and C3 with respect to ground will be maximum whenever the resonant frequency is present. This signal is then coupled by a capacitor to a full wave voltage doubler, CR1, CR2, CR3, CR4 and C6. The output of the full wave voltage doubler is coupled to the base of Q1 through R1, which also provides sensitivity control. When the signal is sufficiently negative with respect to ground the emitter of Q1 will cause Q02 to conduct, lighting the 2 bulbs.

Tank circuit components may vary with frequency change dependent upon frequency requirements.

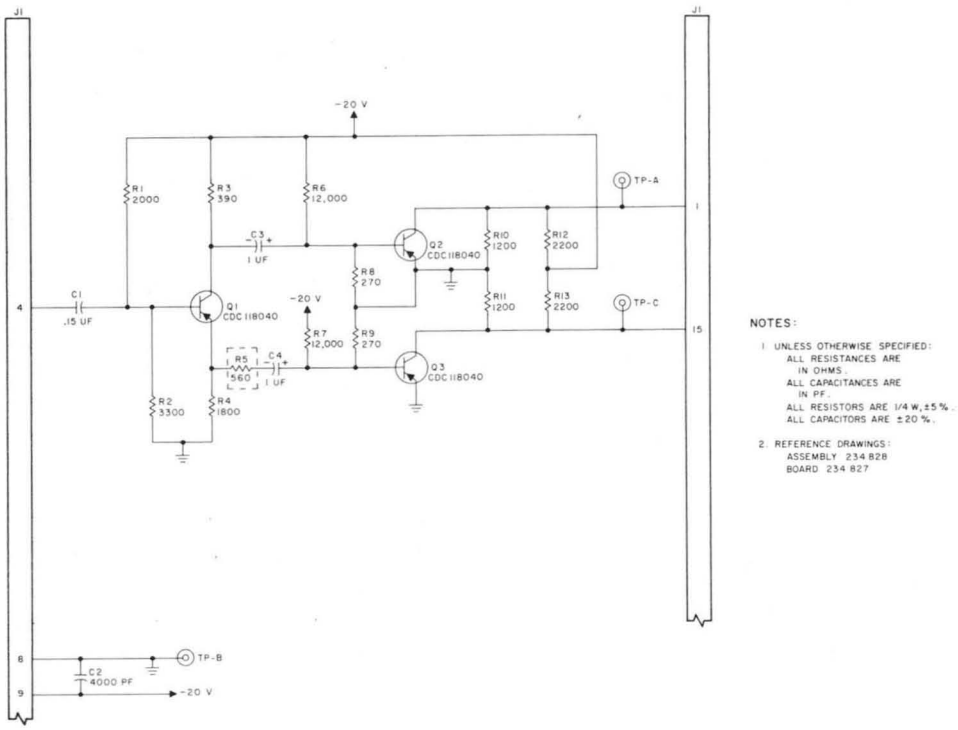


CM09 - VG PHASE SPLITTER

This circuit works in conjunction with the CM05. It can be directly substituted along with the CM05 into the connector locations used by the CM01 to slow down the clock rate of the terminal.

The circuit is a conventional class B phase splitter, and converts the single phase output of the CM05 into a 2 phase output to serve as a clock for the terminal.

One circuit is required by the terminal when the bit rate is to be less than 0.5×10^6 bits/second.

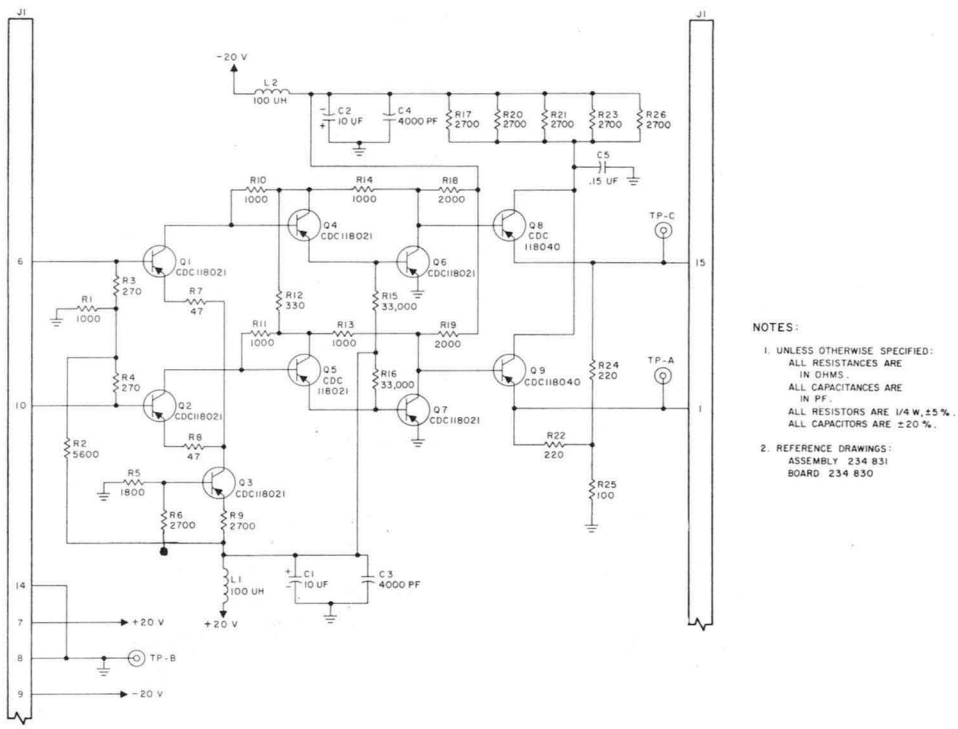


CM10 - LOW OUTPUT IMPEDANCE DIFFERENTIAL AMPLIFIER

This circuit amplifies the split phase data signal and drives the CM02 bipolar threshold amplifier. It is a high gain differential amplifier providing for common mode rejection. One is required for each data line; the card is placed in the input module.

The circuit has an open circuit gain of 100 and a common mode rejection that will produce a 0.2v p-p signal with a common mode signal of 3.0v on the input.

This circuit will be used whenever the received data signal, after equalization, is in excess of 10 mv p-p.



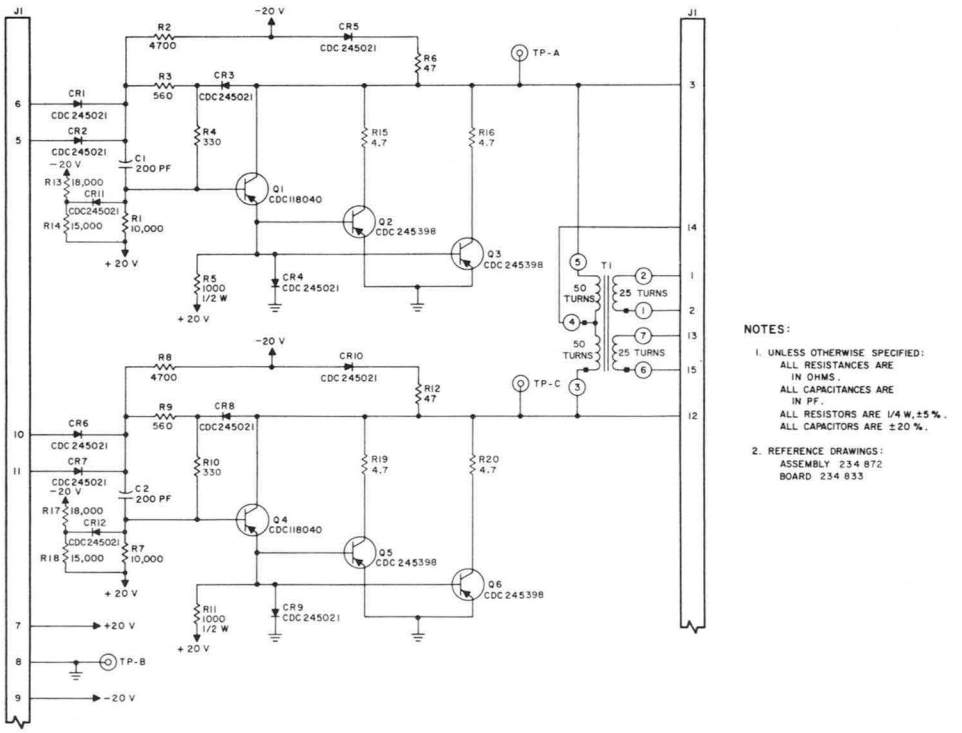
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 234 831
   BOARD 234 830

CM11A - DATA LINE DRIVER

This circuit converts the differential logic level signal output of the transmit pyramid into a split phase differential or single ended signal for presentation to a 75 ohm transmission line at 20v p-p. One is required for each data line.

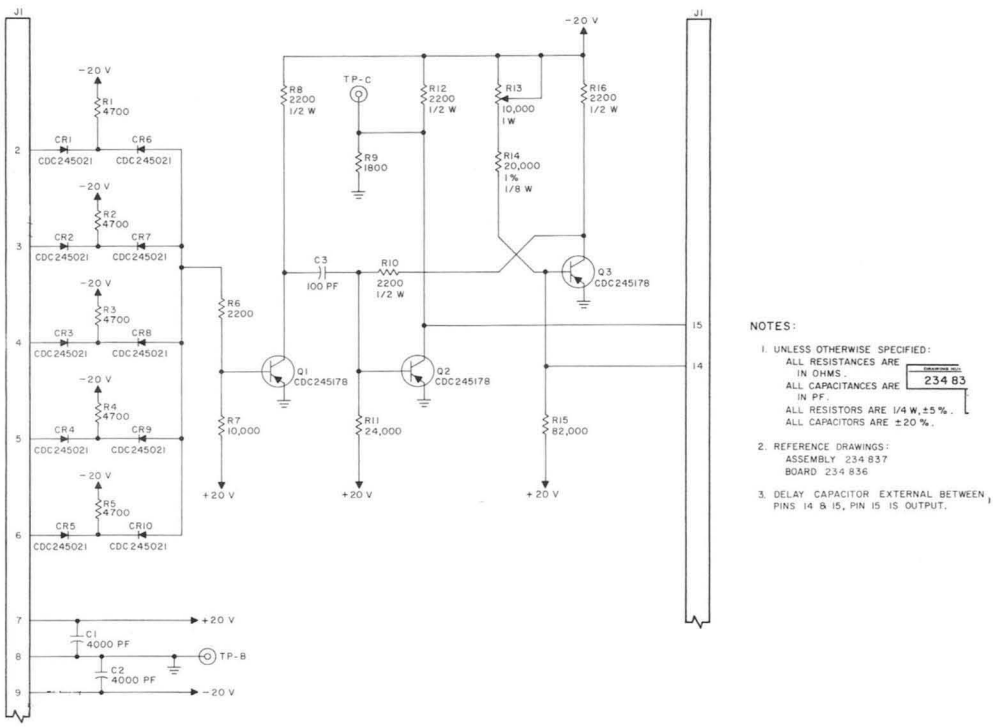
The circuit is subject to variation relative to the placement and type of transformer used with it, dependent upon the data frequency output level and desired impedance.



CM12 - ONE SHOT DELAY

This circuit provides a variable delay and is used in the Fake Ready delay of the terminal. For a "0" input, the output will become a "0" for a specified time, and then return to a "1", independent of the input. To reset the delay at least one input must be a "1" and return to a "0" to produce a delayed "0" out. The delay period is determined by an external capacitor and may be adjusted by R13 on the card.

The circuit may also be used in the bit timing detector logic when the bit rate is too low to permit use of a delay line.



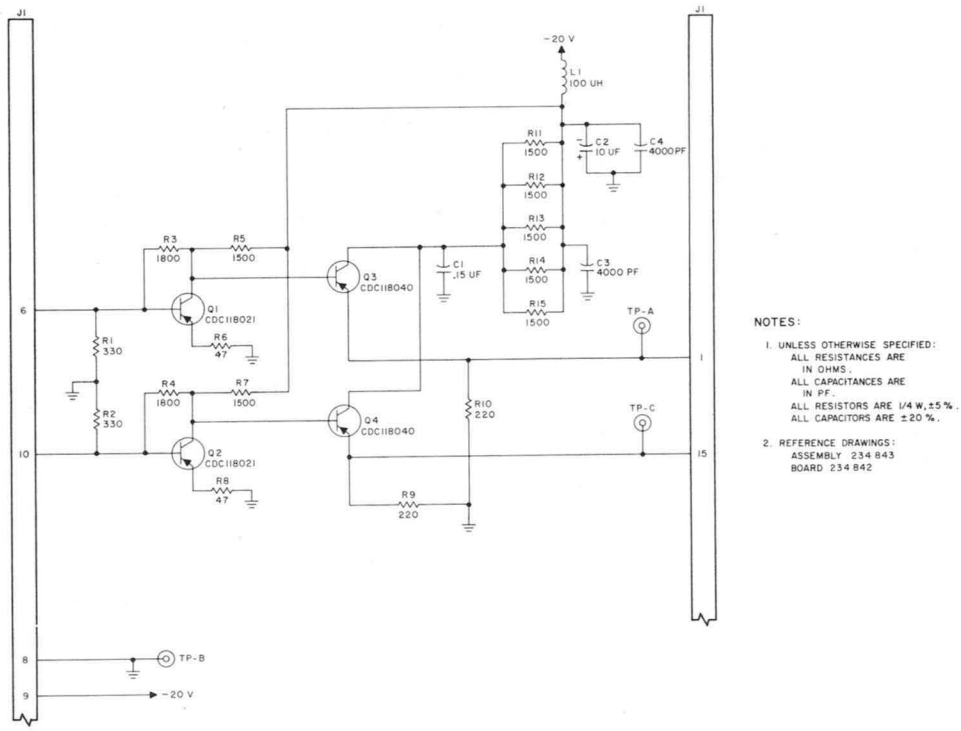
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
   DRAWING NO. 234 83
2. REFERENCE DRAWINGS:
   ASSEMBLY 234 837
   BOARD 234 836
3. DELAY CAPACITOR EXTERNAL BETWEEN PINS 14 & 15, PIN 15 IS OUTPUT.

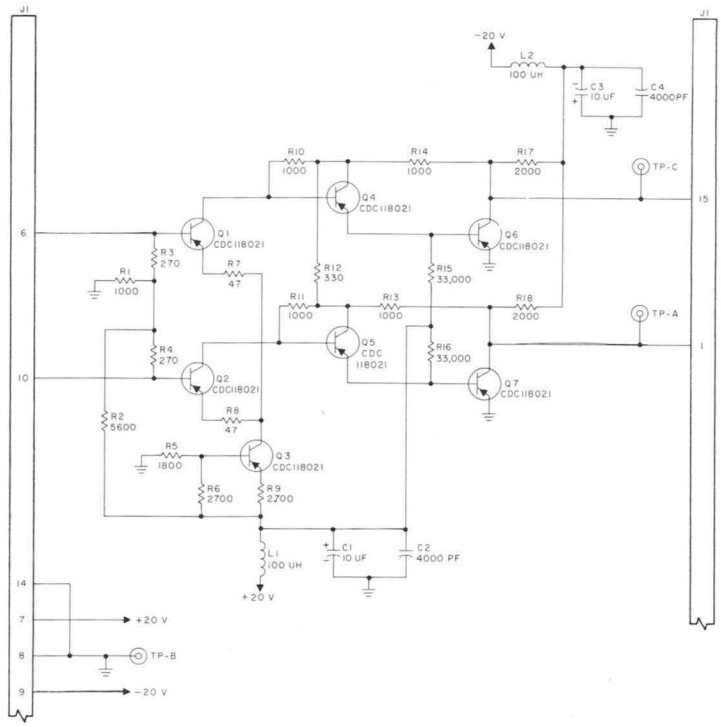
CM14 - SECOND STAGE FOR HIGH GAIN DIFFERENTIAL DATA AMPLIFIER

This circuit serves as a second stage for the CM13/CM16 so that the CM13 or CM16 and CM14 can produce a gain 20 db greater than that of the CM10/CM15.

One is required per line when the CM13 or CM16 is used. It is located in the input module.



CM13 - DIFFERENTIAL AMPLIFIER, HIGH IMPEDANCE OUTPUT



NOTES:

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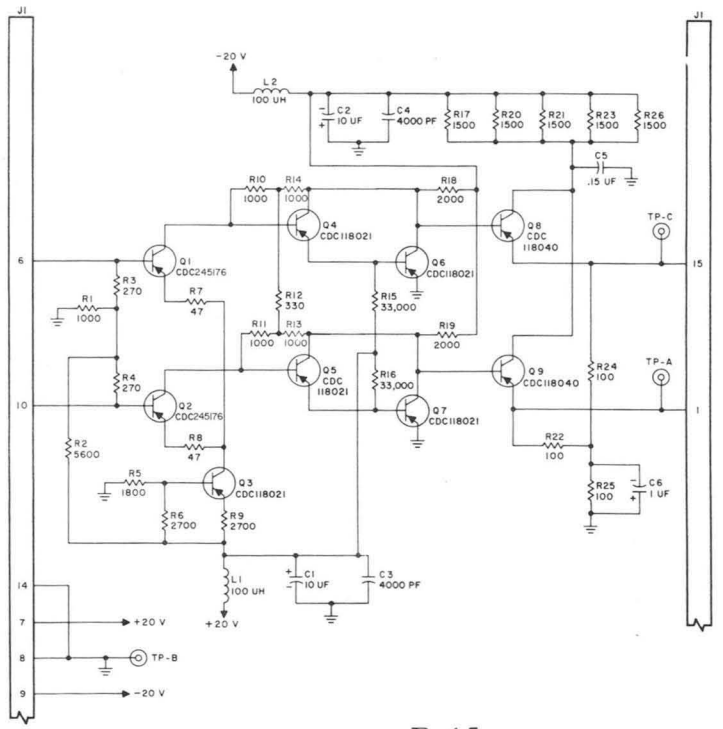
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 234 840
   BOARD 234 839

CM15 - DIFFERENTIAL AMPLIFIER, LOW IMPEDANCE OUTPUT



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
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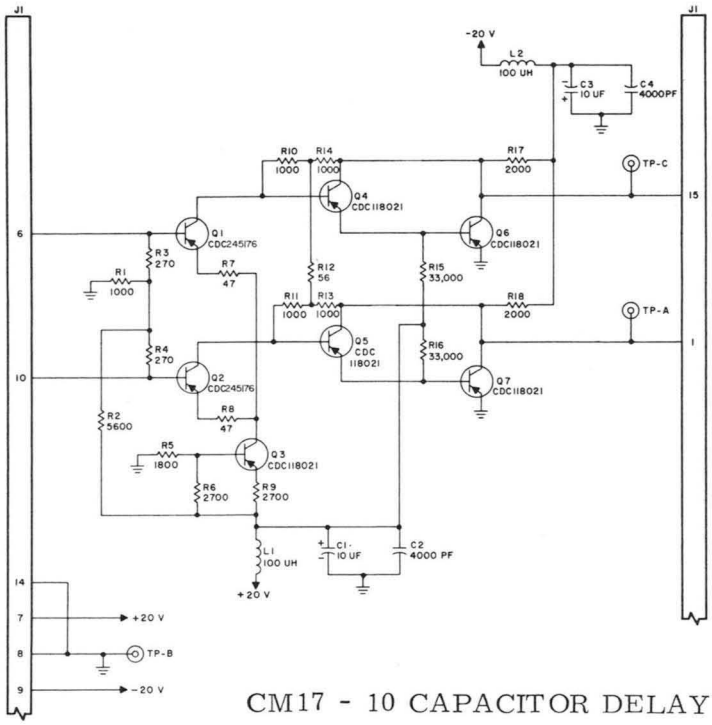
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 234 852
   BOARD 234 851

CM16 - DIFFERENTIAL AMPLIFIER, HIGH IMPEDANCE OUTPUT



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
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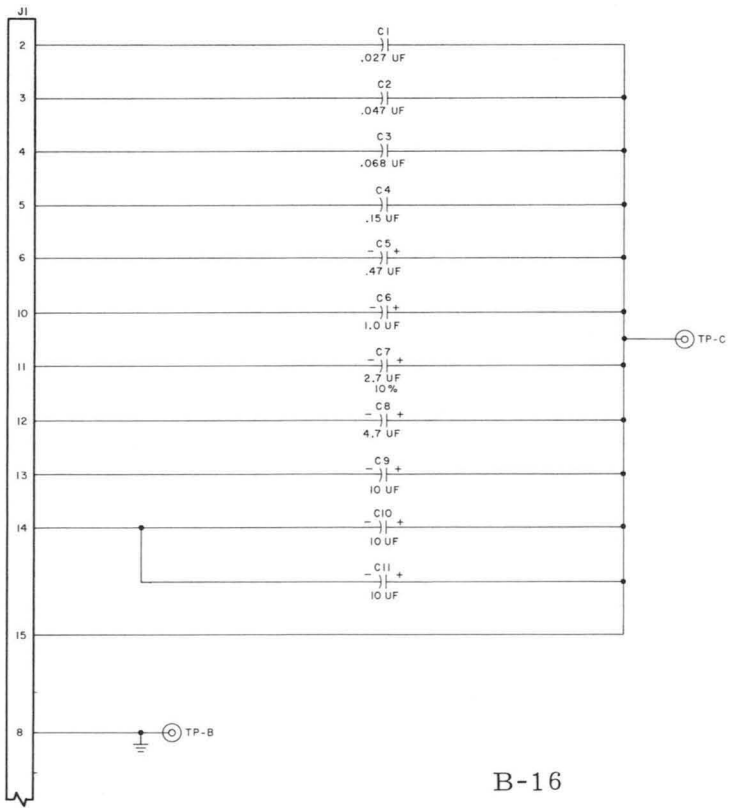
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5 %.
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 234 855
   BOARD 234 854

CM17 - 10 CAPACITOR DELAY



NOTES:

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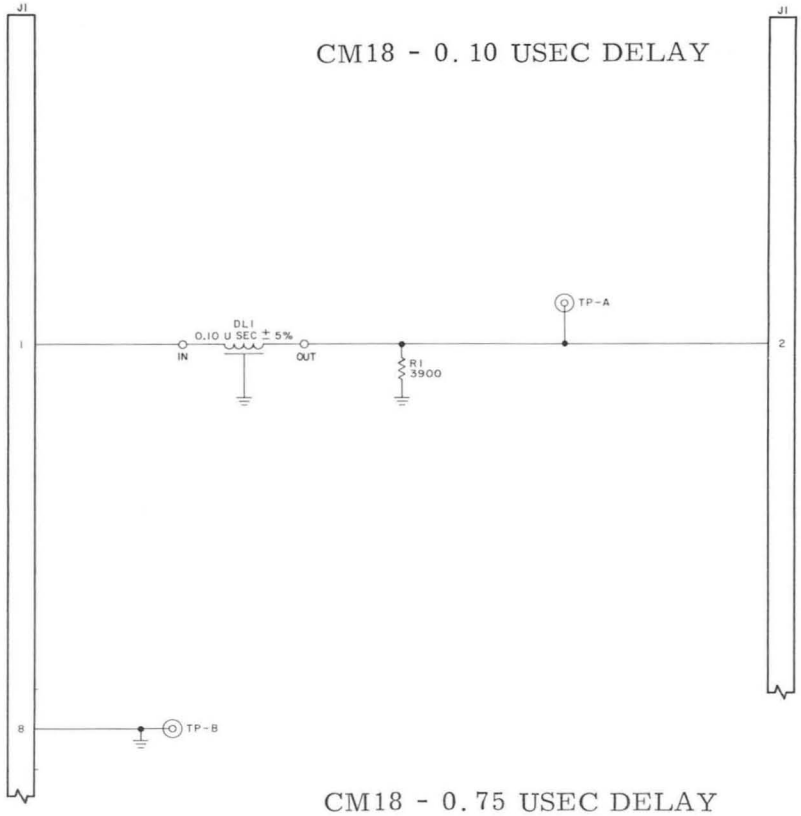
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 234 862
   BOARD 234 861

CM18 - 0.10 USEC DELAY



NOTES:

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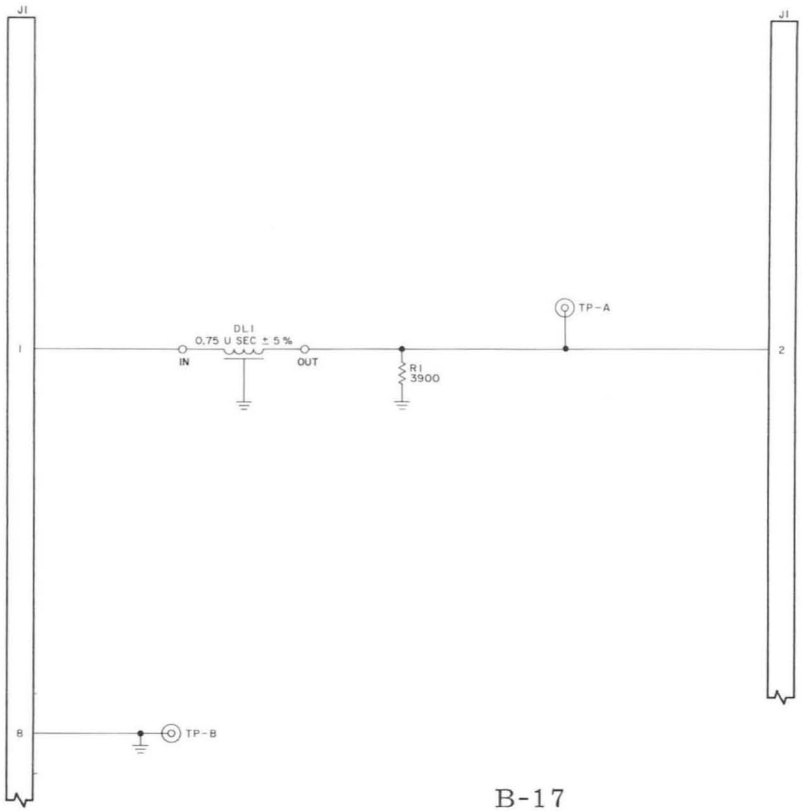
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.

2. REFERENCE DRAWINGS:
   ASSEMBLY 234 875
   BOARD 234 874

CM18 - 0.75 USEC DELAY

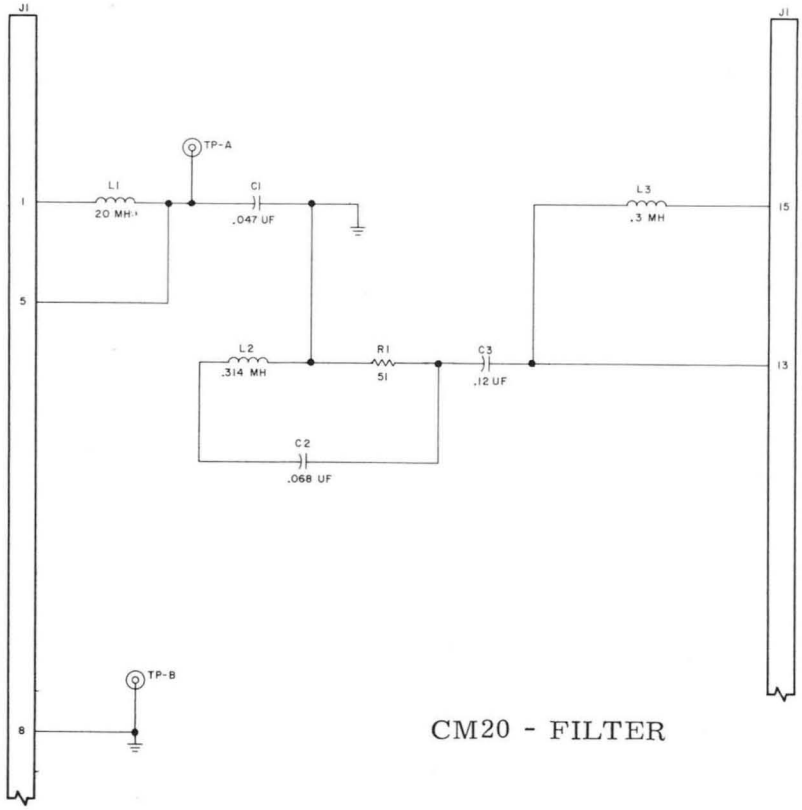


NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.

2. REFERENCE DRAWINGS:
   ASSEMBLY 234 883
   BOARD 234 874

CM19 - TANK CIRCUIT AND FILTER



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
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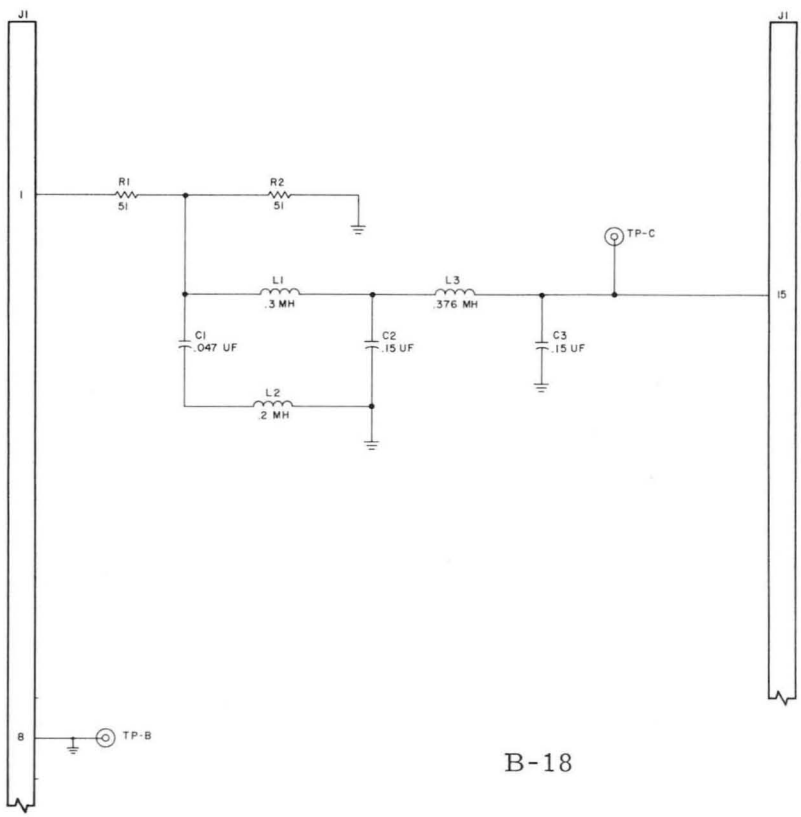
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.

2. REFERENCE DRAWINGS:
   ASSEMBLY 234878
   BOARD 234877

CM20 - FILTER



NOTES:

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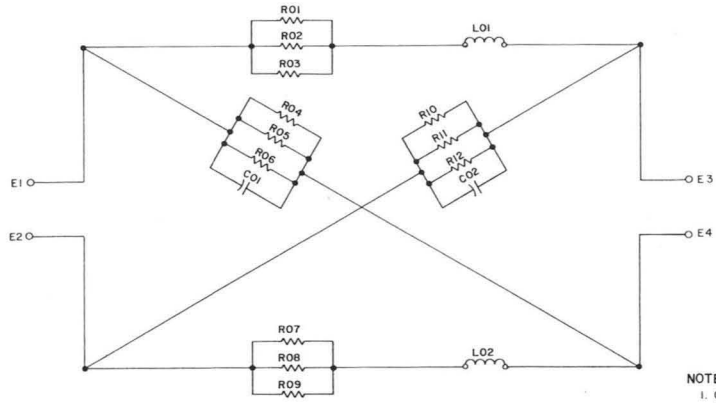
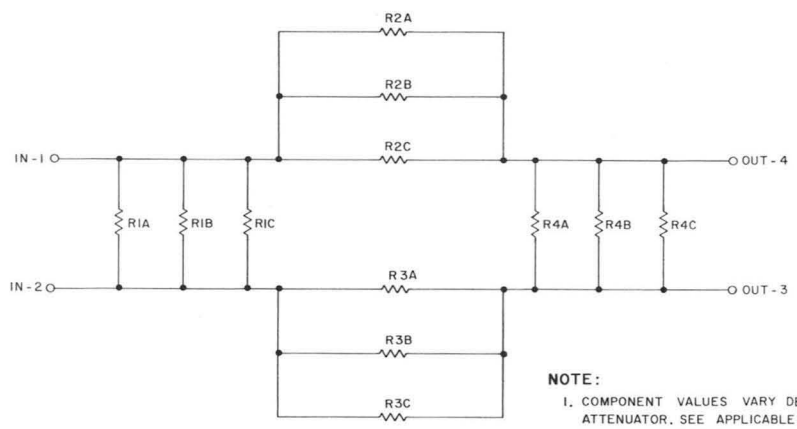
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.

2. REFERENCE DRAWINGS:
   ASSEMBLY 234881
   BOARD 234880



NOTE:
1. COMPONENT VALUES VARY DEPENDING ON CABLE TO BE EQUALIZED.
2. REFERENCE DRAWINGS:
   ASSEMBLY 244092
   BOARD 244091

CABLE EQUALIZER



NOTE:
1. COMPONENT VALUES VARY DEPENDING ON ATTENUATOR. SEE APPLICABLE GROUP NUMBER ON LIST OF MATERIAL 234886.
2. REFERENCE DRAWINGS:
   ASSEMBLY 234886
   BOARD 234885

ATTENUATOR

CONTROL DATA

CORPORATION

501 PARK AVENUE, MINNEAPOLIS 15, MINNESOTA • FEDERAL 9-0411