N82S102, N82S103 Bipolar Field Pro-grammable Gate Array (16 x 9)

GENERAL DESCRIPTION

The 82S102 and 82S103 are Bipolar programmable AND/NAND gate arrays, containing 9 gates sharing 16 common inputs. On-chip input buffers enable the user to individually program for each gate either the True (I_m), Complement ($\overline{I_m}$), or Don't Care (X) logic state of each input. In addition, the polarity of each gate output is individually programmable to implement either AND or NAND logic functions.

Alternatively, if desired OR/NOR logic functions can also be realized by programming for each gate the complement of its input variables, and output (DeMorgan theorem).

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

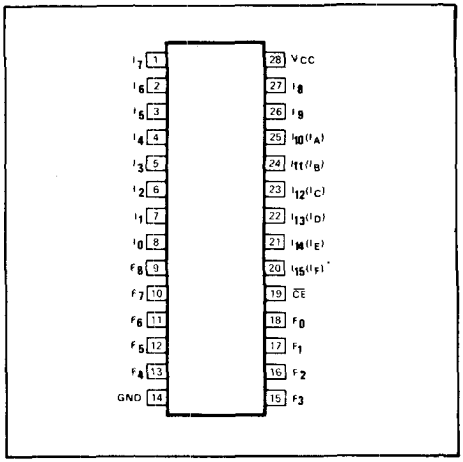
The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, I or N, and for the military range (−55°C to +125°C) specify S82S102/103, I.

FEATURES

- Field programmable (NI-Cr link)
- 16 input variables
- 9 output functions
- Chip enable input
- I/O propagation delay:
  N82S102/103: 30ns max
  S82S102/103: 50ns max
- Power dissipation: 600mW typ
- Input loading:
  N82S102/103: −100μA max
  S82S102/103: −150μA max

CONNECTION DIAGRAM

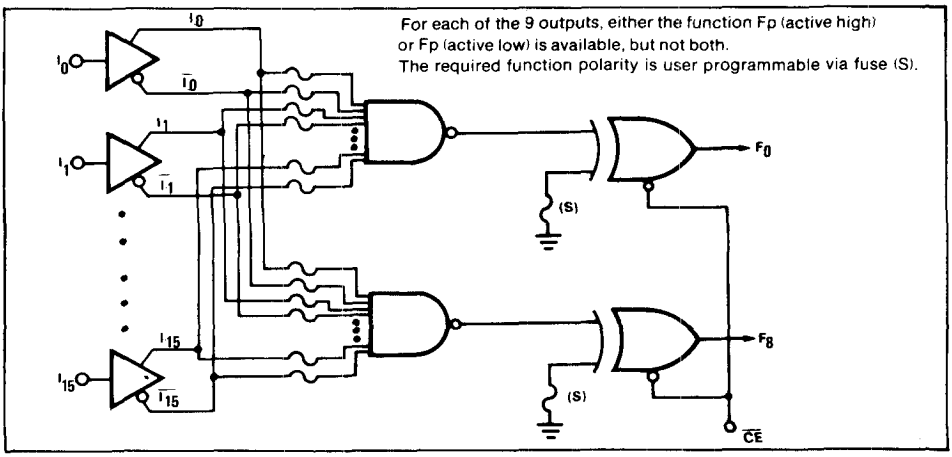


- Output options:
  82S102: Open collector
  82S103: Tri-state
- Output disable function:
  82S102: Hi
  82S103: Hi-Z
- Fully TTL compatible

APPLICATIONS

- Random logic
- Address decoders
- Code detectors
- Peripheral selectors
- Fault monitors
- Machine state decoders

LOGIC DIAGRAM



N82S102, N82S103 (Cont.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	–55 to +125	
T_{STG}	Storage	–65 to +150	

REFERENCE TABLE

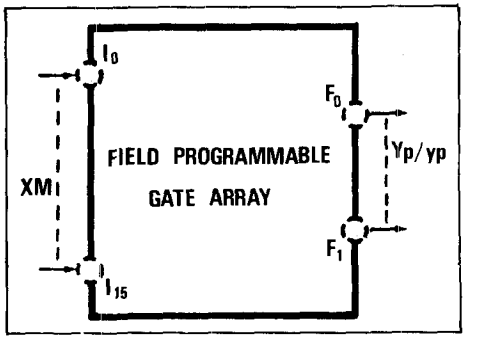
TYPE NO.	STOCK NO.	OUTLINE DRWG. NO.
N82S102N	56359A	5
N82S103N	56360D	5

EQUIVALENT LOGIC PATH

The Field Programmable Gate Array consists of 9 gates with individually programmable inputs and outputs.

The inputs to each gate can be programmed either True (I_m), Complement ($\overline{I_m}$), or Don't Care via corresponding links (j) and (k). The outputs of each gate can be programmed active-high (F_p) or active=low (F_p^*) via corresponding links (S). Thus, each gate provides either of 2 output logic functions in terms of ***external*** input logic variables X_m as defined below (positive logic):

CONNECTION DIAGRAM



At S = Open:
$F_p = \overline{CE} + (X_0 \bullet X_1 \bullet X_2 \bullet \ldots . Xm) = Yp$

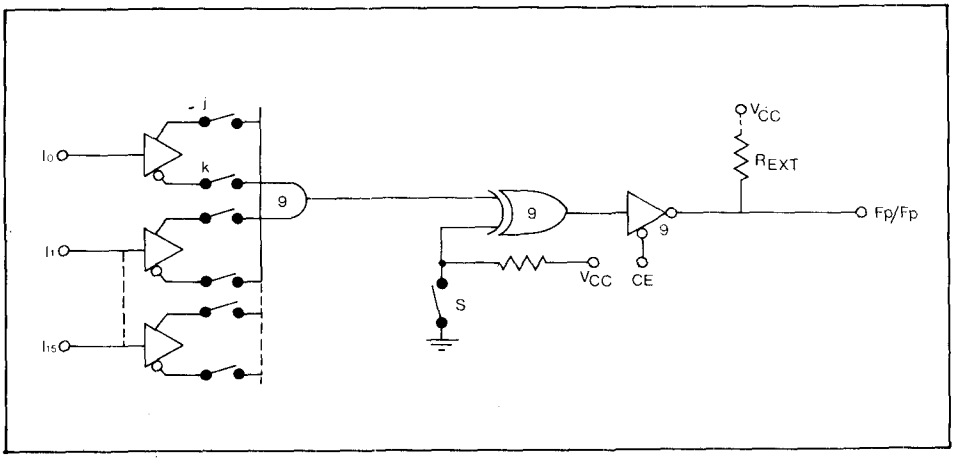
At S = Closed:
$Fp = \overline{CE} + (\overline{X_0} + \overline{X_1} + \overline{X_2} + \ldots . \overline{X_m}) = yp$
$m = 0, 1, 2, \ldots . 15$
$p = 0, 1, 2, \ldots . 8$
and where $X_m = I_m, \overline{I_m}$, Don't Care, as assigned by programming polarity of inputs I_0–I_{15}.

When $\overline{CE}$ = low, all gates are enabled, and $F_p^* = \overline{F_p}$ giving $y_p = \overline{Y_p}$.

PROGRAMMABLE LOGIC FUNCTIONS

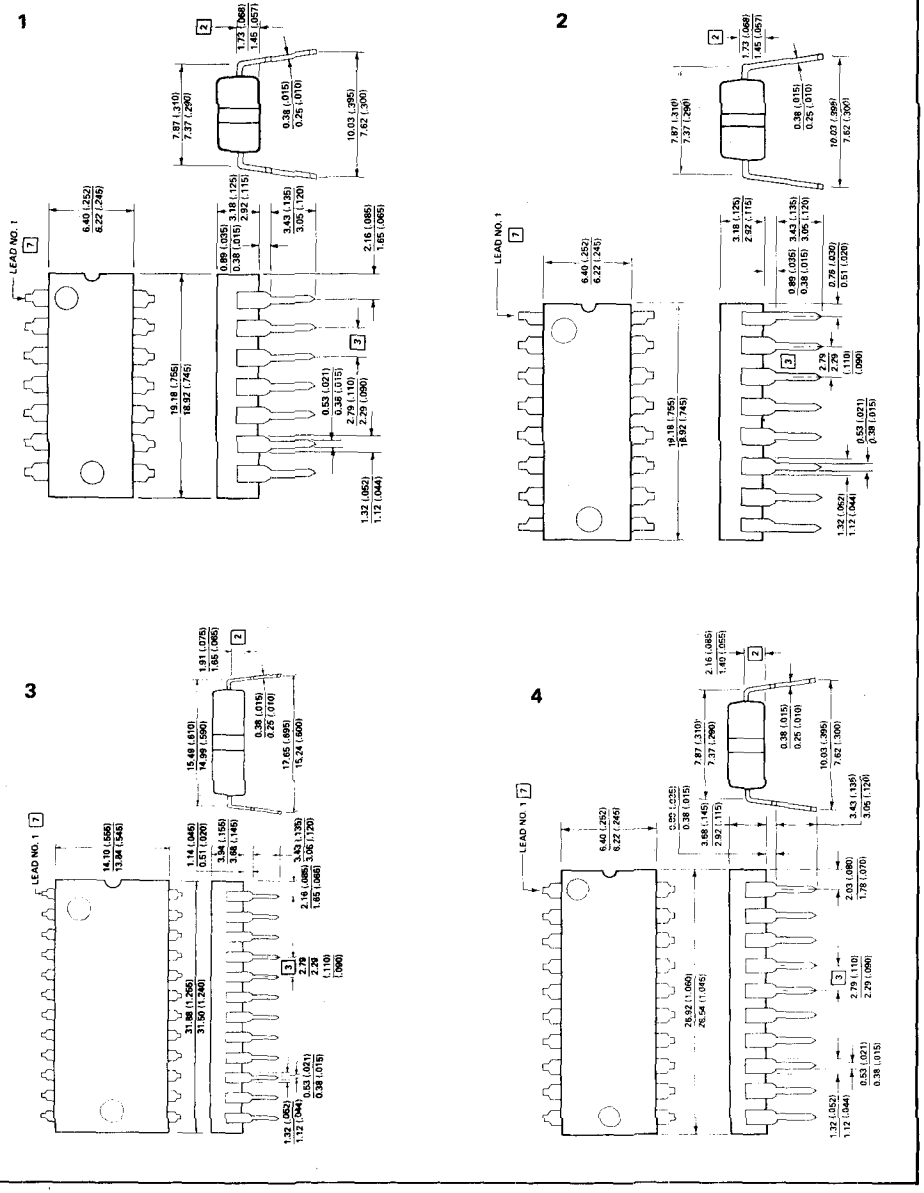
All internal links of virgin FPGAs are intact. Therefore, as shown in the Equivalent Logic Path, all symbolic switches are initially closed. Selective programming (opening) or links (J), (K), and (S) enables the user to assign input and output polarities to each gate for implementing NAND, NOR, AND, OR logic functions without changing the routing of input and output wires. This is shown in the following diagrams for a typical gate in terms of 2 input variables, which can be readily extended up to 16.

LOGIC DIAGRAM



PLEASE QUOTE STOCK NO.
AND MANUFACTURERS PART NO. WHEN ORDERING

ITT GEMINI



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AND MANUFACTURERS PART NO. WHEN ORDERING

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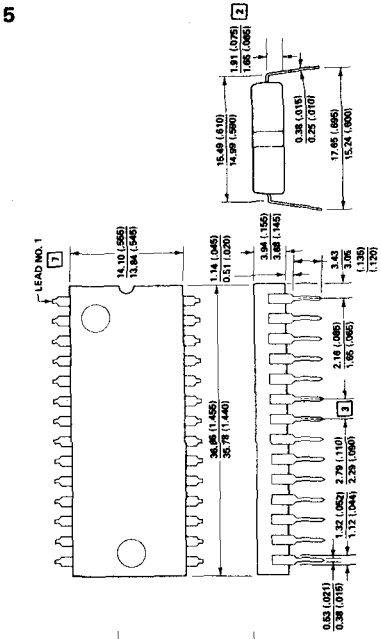
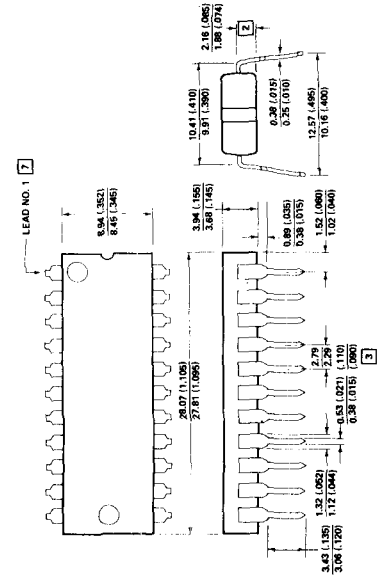
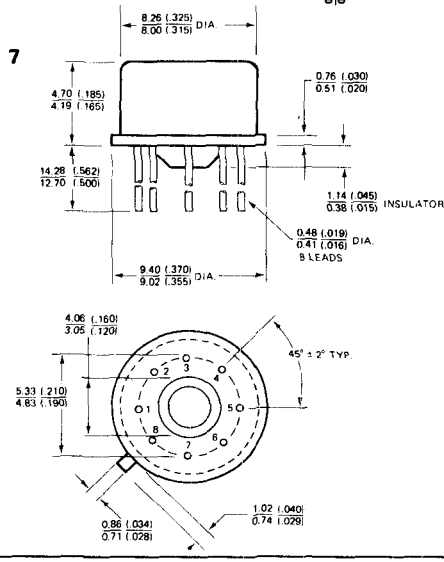
5


LEAD NO. 1
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)
14.10 (.555)
13.84 (.545)
1.14 (.045)
0.51 (.020)
3.94 (.155)
3.68 (.145)
3.43 (.135)
3.05 (.120)
2.16 (.085)
1.65 (.065)
36.85 (1.450)
35.79 (1.440)
2.79 (.110)
2.29 (.090)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)

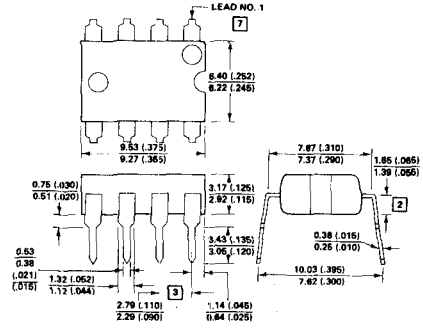
6


LEAD NO. 1
2.16 (.085)
1.88 (.074)
10.41 (.410)
9.91 (.390)
0.38 (.015)
0.25 (.010)
12.57 (.495)
10.16 (.400)
8.94 (.352)
8.45 (.345)
3.94 (.155)
3.68 (.145)
0.89 (.035)
0.38 (.015)
1.52 (.060)
1.02 (.040)
25.07 (1.105)
27.81 (1.095)
2.79
2.29
(.110)
(.090)
0.53 (.021)
0.38 (.015)
1.32 (.052)
1.12 (.044)
3.43 (.135)
3.06 (.120)

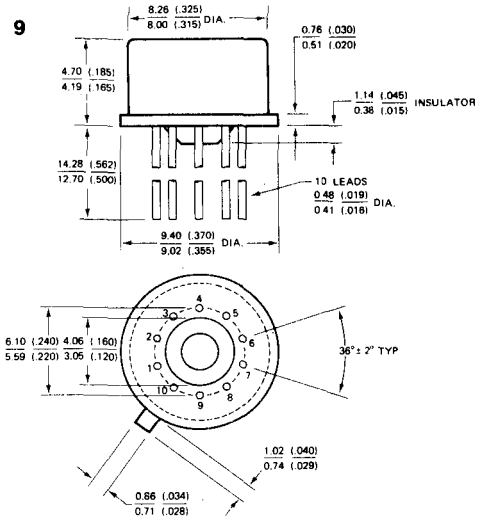
7


8.26 (.325)
8.00 (.315) DIA.
4.70 (.185)
4.19 (.165)
0.76 (.030)
0.51 (.020)
14.28 (.562)
12.70 (.500)
1.14 (.045)
0.38 (.015) INSULATOR
0.48 (.019)
0.41 (.016) DIA.
8 LEADS
9.40 (.370)
9.02 (.355) DIA.
4.06 (.160)
3.05 (.120)
45° ± 2° TYP.
5.33 (.210)
4.83 (.190)
0.86 (.034)
0.71 (.028)
1.02 (.040)
0.74 (.029)

8


LEAD NO. 1
6.40 (.252)
6.22 (.245)
9.53 (.375)
9.27 (.365)
7.87 (.310)
7.37 (.290)
1.85 (.065)
1.39 (.055)
0.75 (.030)
0.51 (.020)
3.17 (.125)
2.92 (.115)
0.38 (.015)
0.25 (.010)
3.43 (.135)
3.06 (.120)
0.53
0.38
(.021)
(.015)
1.32 (.052)
1.12 (.044)
10.03 (.395)
7.62 (.300)
2.79 (.110)
2.29 (.090)
1.14 (.045)
0.64 (.025)

9



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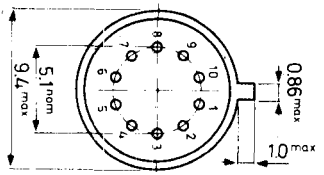
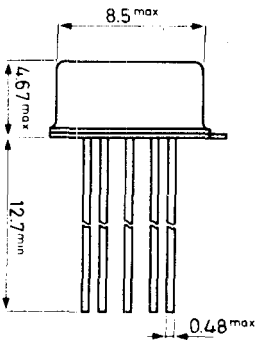
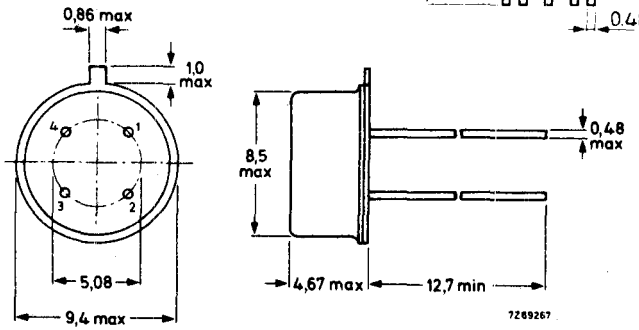
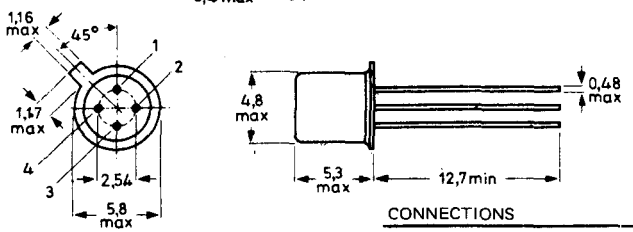




11



12

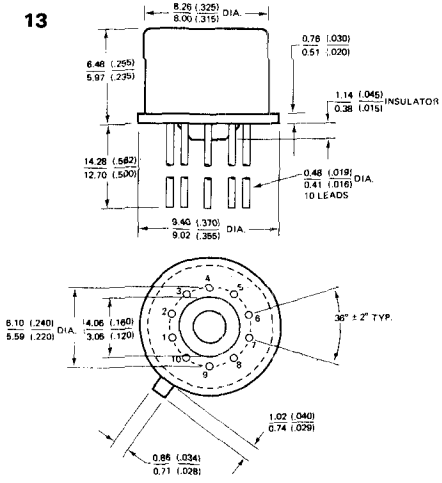


pin 4 connected to case

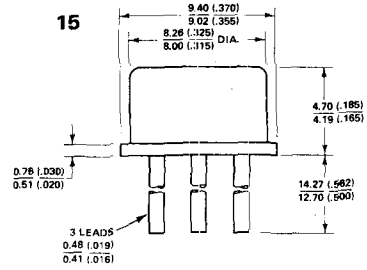
CONNECTIONS

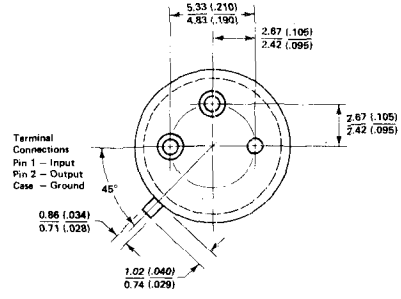
DRWG NO.	1	2	3	4	
12.1	V_O	V_P	V_i	V_N	Substrate connected to envelope
12.2	d	g_2	g_1	S	
12.3	s	d	g	*	

13

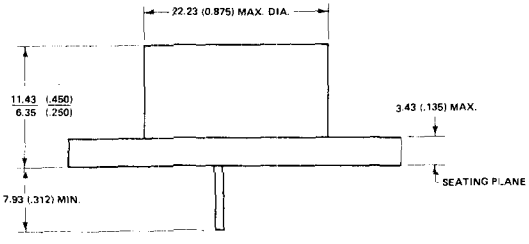

8.26 (.325)
8.00 (.315) DIA.
0.76 (.030)
0.51 (.020)
6.48 (.255)
5.97 (.235)
1.14 (.045)
0.38 (.015) INSULATOR
14.28 (.562)
12.70 (.500)
0.48 (.019)
0.41 (.016) DIA.
10 LEADS
9.40 (.370)
9.02 (.355) DIA.
6.10 (.240)
5.59 (.220) DIA.
4.06 (.160)
3.06 (.120)
36° ± 2° TYP.
1.02 (.040)
0.74 (.029)
0.86 (.034)
0.71 (.028)

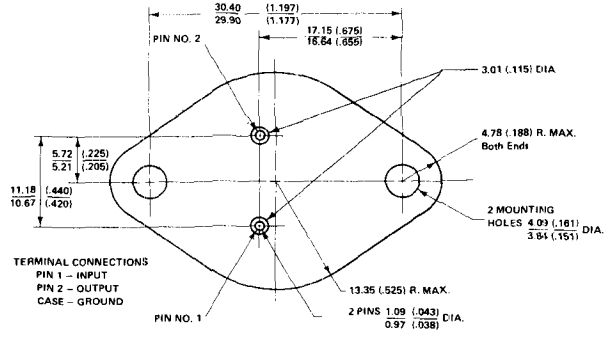
15


9.40 (.370)
9.02 (.355)
8.26 (.325)
8.00 (.315) DIA.
4.70 (.185)
4.19 (.165)
0.76 (.030)
0.51 (.020)
14.27 (.562)
12.70 (.500)
3 LEADS
0.48 (.019)
0.41 (.016)

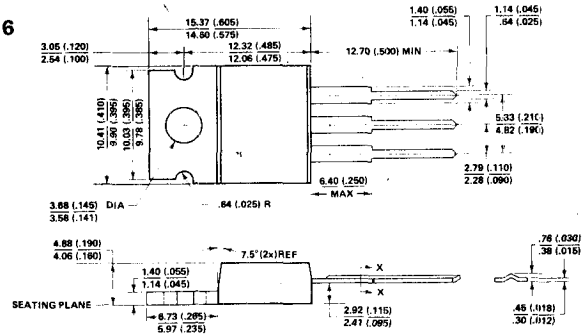

5.33 (.210)
4.83 (.190)
2.67 (.105)
2.42 (.095)
2.67 (.105)
2.42 (.095)
Terminal
Connections
Pin 1 – Input
Pin 2 – Output
Case – Ground
45°
0.86 (.034)
0.71 (.028)
1.02 (.040)
0.74 (.029)

14

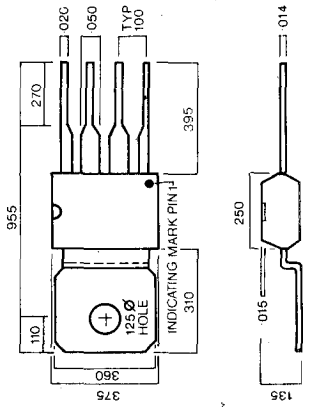

22.23 (0.875) MAX. DIA.
11.43 (.450)
6.35 (.250)
3.43 (.135) MAX.
SEATING PLANE
7.93 (.312) MIN.


30.40 (1.197)
29.90 (1.177)
17.15 (.675)
16.64 (.655)
PIN NO. 2
3.01 (.115) DIA.
4.78 (.188) R. MAX.
Both Ends
5.72 (.225)
5.21 (.205)
11.18 (.440)
10.67 (.420)
2 MOUNTING
HOLES 4.09 (.161)
3.84 (.151) DIA.
TERMINAL CONNECTIONS
PIN 1 – INPUT
PIN 2 – OUTPUT
CASE – GROUND
13.35 (.525) R. MAX.
PIN NO. 1
2 PINS 1.09 (.043)
0.97 (.038) DIA.

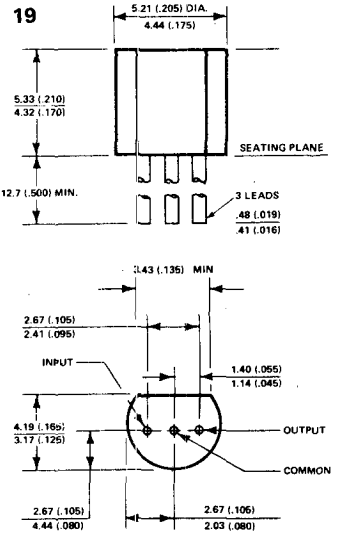
16



17

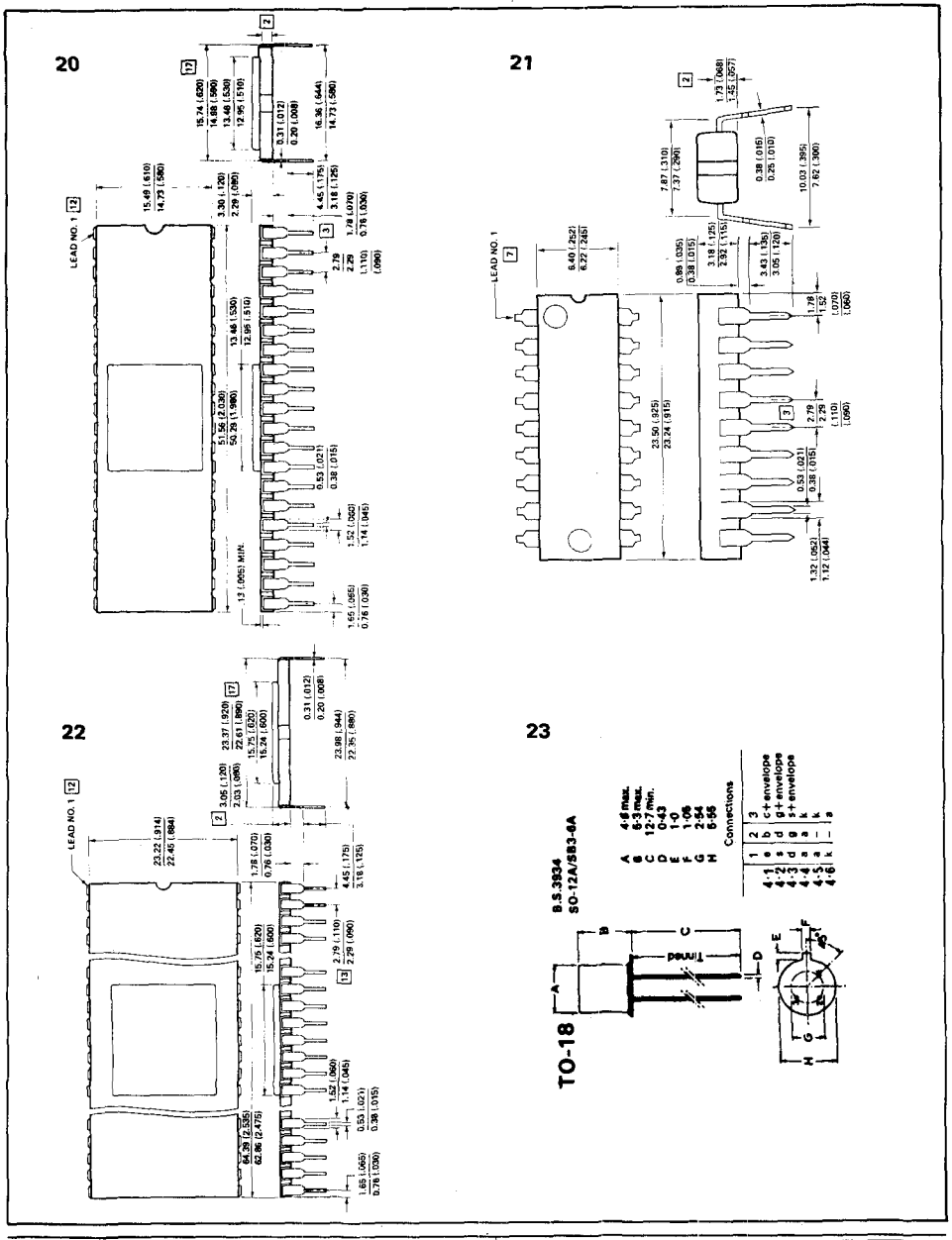


19



PLEASE QUOTE STOCK NO.
AND MANUFACTURERS PART NO. WHEN ORDERING

ITT GEMINI


20
21
22
23
LEAD NO. 1
TO-18
SO-12A/SB3-6A
B.S.3934
Connections