# MICROPROCESSOR
## DATA
## HAND BOOK

COVERS
UP TO
80486

MP MICRO-TECH PUBLICATIONS

# MICROPROCESSOR DATA HAND BOOK

| TTL – CMOS |
| --- |
| LINEAR I.C.'s |
| MEMORY CHIPs |
| ANALOG DEVICES |
| 8/16/32 BIT CPUs |
| VOLTAGE REGULATOR I.C.'s |
| CLOCK/CALCULATOR I.C.'s |

# PREFACE

This microprocessor data hand book is the third revised edition of our earlier book. Since the first edition was published quite a bit of change has occurred in the industry. Many new chips and devices have also been added.

This new edition has been compiled after looking carefully in to various applications including personal computers, sophisticated instruments and communication systems.

It will also serve as a good reference book for computer hardware Hobbyists, Engineers and Educationists. It will help them identify all support chips applicable to specific microprocessor circuitry.

The publishers are thankful to various manufacturers of these devices whose datas have been used in this work.

The publishers are also grateful to Mr. A.K. Jain who have been very helpful in the compilation of this book.

Publishers

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**TTL DATA**

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# 7400, LS00, S00
## Gates

**Quad Two-Input NAND Gate**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7400 | 9ns | 8mA |
| 74LS00 | 9.5ns | 1.6mA |
| 74S00 | 3ns | 15mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7400N, N74LS00N, N74S00N |
| Plastic SO | N74LS00D, N74S00D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A, B | Inputs | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



1

# 74LS01
## Gate

**Quad Two-Input NAND Gate (Open Collector)**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 74LS01 | 16ns | 1.6mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|----------------------------------------------------------------|
| Plastic DIP | N74LS01N |
| Plastic SO | N74LS01D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|------|-------------|------|
| A, B | Inputs | 1LSul |
| Y | Output | 10LSul |

**NOTE:**
Where a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



CD04180S

## LOGIC SYMBOL



LS05210S

## LOGIC SYMBOL (IEEE/IEC)



LS05220S

2

# 7402, LS02, S02
## Gates

**Quad Two-Input NOR Gate**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7402 | 10ns | 11mA |
| 74LS02 | 10ns | 2.2mA |
| 74S02 | 3.5ns | 22mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE V_CC = 5V ±5%; T_A = 0°C to +70°C |
|---|---|
| Plastic DIP | N7402N, N74LS02N, N74S02N |
| Plastic SO | N74LS02D, N74S02D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A, B | Inputs | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD04180S

## LOGIC SYMBOL



LS03200S

## LOGIC SYMBOL (IEEE/IEC)



LS03210S

3

# 7403, S03
## Gates

**Quad Two-Input NAND Gate (Open Collector)**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7403 | 35ns ($t_{PLH}$)<br>8ns ($t_{PHL}$) | 8mA |
| 74S03 | 5ns ($t_{PLH}$)<br>4.5ns ($t_{PHL}$) | 13mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7403N, N74S03N |
| Plastic SO | N74S03D |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S |
|---|---|---|---|
| A, B | Inputs | 1ul | 1Sul |
| Y | Output | 10ul | 10Sul |

NOTE:
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$.

## PIN CONFIGURATION



CD05480S

## LOGIC SYMBOL



LS05230S

## LOGIC SYMBOL (IEEE/IEC)



LS05240S

4
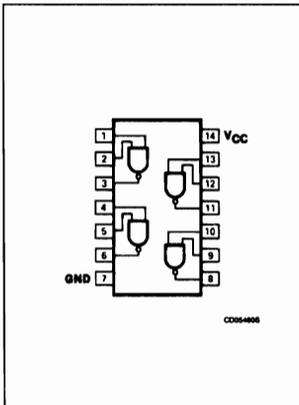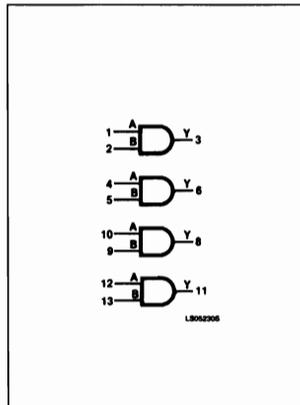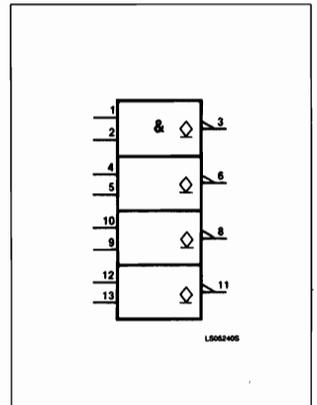
# 7404, LS04, S04
## Inverters

**Hex Inverter**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7404 | 10ns | 12mA |
| 74LS04 | 9.5ns | 2.4mA |
| 74S04 | 3ns | 22mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7404N, N74LS04N, N74S04N |
| Plastic SO | N74LS04D, N74S04D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUT | OUTPUT |
|---|---|
| A | Y |
| L | H |
| H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A | Input | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



5

# 7405, LS05, S05
## Inverters

**Hex Inverter (Open Collector)**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7405 | 40ns ($t_{PLH}$)<br>8ns ($t_{PHL}$) | 12mA |
| 74LS05 | 17ns ($t_{PLH}$)<br>15ns ($t_{PHL}$) | 2.4mA |
| 74S05 | 5ns ($t_{PLH}$)<br>4.5ns ($t_{PHL}$) | 20mA |

## FUNCTION TABLE

| INPUT | OUTPUT |
|---|---|
| A | Y |
| L | H |
| H | L |

H = HIGH voltage level
L = LOW voltage level

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7405N, N74LS05N, N74S05N |
| Plastic SO | N74LS05D, N74S05D |
| Ceramic DIP | |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A | Input | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

NOTE:
Where a 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$, a 74S unit load (Sul) is $50\mu A$ $I_{IH}$ and $-2.0mA$ $I_{IL}$, and 74LS unit load (LSul) is $20\mu A$ $I_{IH}$ and $-0.4mA$ $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

# 7406, 07
# Inverter/Buffer/Drivers

**'06 Hex Inverter Buffer/Driver (Open Collector)**
**'07 Hex Buffer/Driver (Open Collector)**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7406 | 10ns ($t_{PLH}$)<br>15ns ($t_{PHL}$) | 31mA |
| 7407 | 6ns ($t_{PLH}$)<br>20ns ($t_{PHL}$) | 25mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7406N, N7407N |
| Plastic SO | N7406D, N7407D |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| '06 | | '07 | |
|---|---|---|---|
| INPUT | OUTPUT | INPUT | OUTPUT |
| A | Y | A | Y |
| H | L | H | H |
| L | H | L | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| A | Input | 1ul |
| Y | Output | 10ul |

NOTE:
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



7
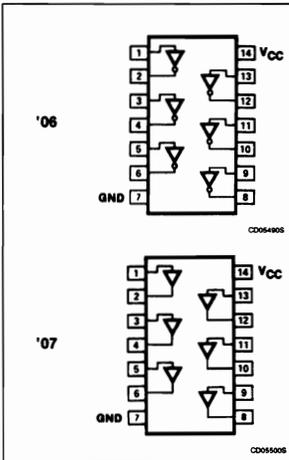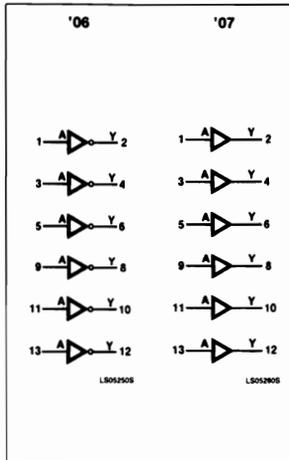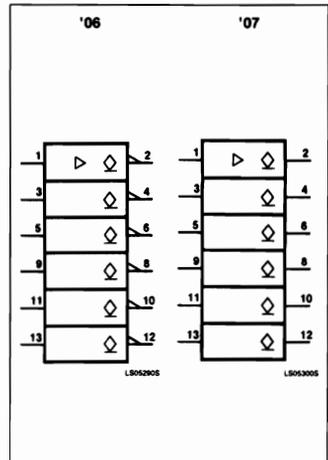
# 7408, LS08, S08
## Gates

**Quad Two-Input AND Gate**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7408 | 15ns | 16mA |
| 74LS08 | 9ns | 3.4mA |
| 74S08 | 5ns | 25mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7408N, N74LS08N, N74S08N |
| Plastic SO | N74LS08N, N74S08N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A, B | Inputs | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, a 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and $-2.0$mA $I_{IL}$, and 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



8

# 74LS09
## Gates

**Quad Two-Input AND Gate (Open Collector)**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS09 | 23ns | 4.3 |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS09N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| A, B | Inputs | 1LSul |
| Y | Output | 10LSul |

**NOTE:**
Where 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD05510S

## LOGIC SYMBOL



LS05310S

## LOGIC SYMBOL (IEEE/IEC)



LS05320S

9
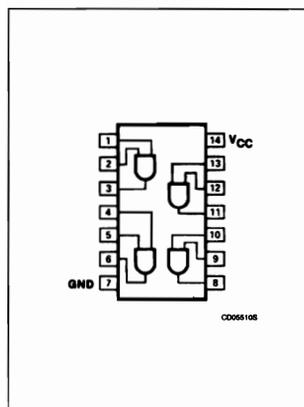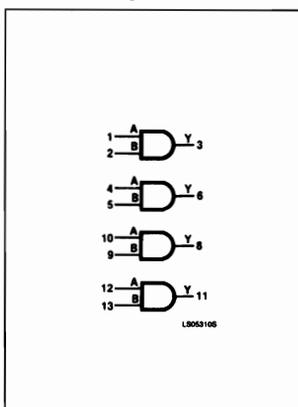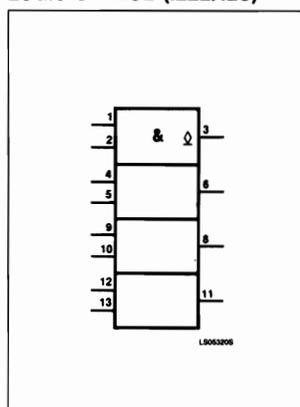
# 7410, 7411, LS10, LS11, S10, S11
## Gates

**Triple Three-Input NAND ('10), AND ('11) Gates**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7410 | 9ns | 6mA |
| 74LS10 | 10ns | 1.2mA |
| 74S10 | 3ns | 12mA |
| 7411 | 10ns | 11mA |
| 74LS11 | 9ns | 2.6mA |
| 74S11 | 5ns | 19mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP '10 | N7410N, N74LS10N, N74S10N |
| '11 | N7411N, N74LS11N, N74S11N |
| Plastic SO '10 | N74LS10D, N74S10D |
| Plastic SO '11 | N74LS11D, N74S11D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| A | B | C | Y('10) | Y('11) |
| L | L | L | H | L |
| L | L | H | H | L |
| L | H | L | H | L |
| L | H | H | H | L |
| H | L | L | H | L |
| H | L | H | H | L |
| H | H | L | H | L |
| H | H | H | L | H |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A – C | Inputs | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and –1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and –2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION

'10, '11



## LOGIC SYMBOL

'10          '11



## LOGIC SYMBOL (IEEE/IEC)

'10          '11



10´
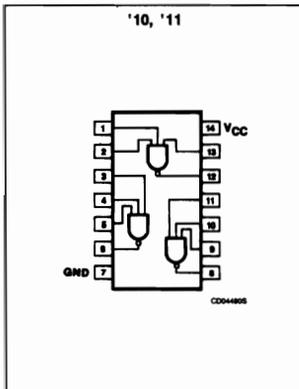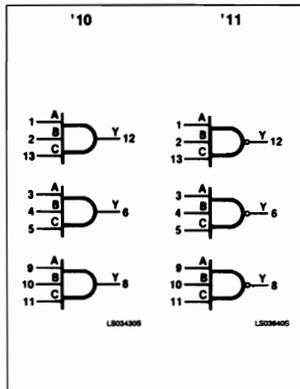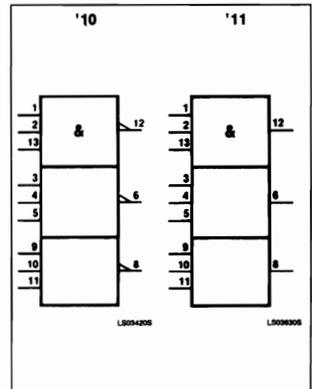
# 54/7412

## TRIPLE 3-INPUT NAND GATE

### (With Open-Collector Output)

```
        ___
   1 |        | 14  Vcc
   2 |        | 13
   3 |        | 12
   4 |        | 11
   5 |        | 10
   6 |        |  9
GND 7 |       |  8
```

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>Vcc = +5.0 V ±5%,<br>T_A = 0°C to +70°C | MILITARY GRADE<br>Vcc = +5.0 V ±10%,<br>T_A = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 7412PC | | 9A |
| Ceramic DIP (D) | A | 7412DC | 5412DM | 6A |
| Flatpak (F) | A | 7412FC | 5412FM | 3I |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PINS | 54/74 (U.L.)<br>HIGH/LOW |
|---|---|
| Inputs | 1.0/1.0 |
| Outputs | OC**/10 |

**DC AND AC CHARACTERISTICS:** See Section 3*

| SYMBOL | PARAMETER | 54/74 Min | 54/74 Max | UNITS | CONDITIONS | |
|---|---|---|---|---|---|---|
| $I_{CCH}$ | Power Supply Current | | 6.0 | mA | $V_{IN}$ = Gnd | $V_{CC}$ = Max |
| $I_{CCL}$ | | | 16.5 | | $V_{IN}$ = Open | |
| $t_{PLH}$ | Propagation Delay | | 45 | ns | Figs. 3-2, 3-4 | |
| $t_{PHL}$ | | | 15 | | | |

*DC limits apply over operating temperature range; AC limits apply at $T_A$ = +25°C and $V_{CC}$ = +5.0 V.

**OC — Open Collector

11

# 7413, LS13
## Gates

**Dual 4-Input NAND Schmitt Trigger**
*Product Specification*

**Logic Products**

## DESCRIPTION
The '13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than $V_{t+ MAX}$, the gate will respond in the transitions of the other input as shown in Waveform 1.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7413 | 17ns | 17mA |
| 74LS13 | 17ns | 3.5mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7413N, N74LS13N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| All | Inputs | 1ul | 1LSul |
| Y | Output | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD04370S

## LOGIC SYMBOL



LS03440S

## LOGIC SYMBOL (IEEE/IEC)



L903450S
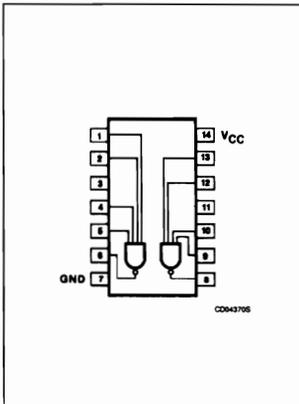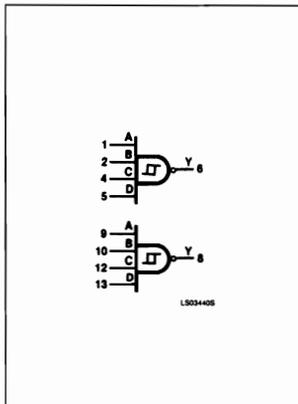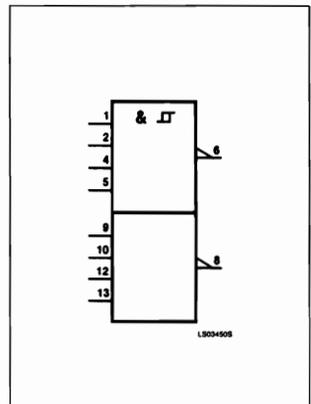
# 7414, LS14
## Schmitt Triggers

**Hex Inverter Schmitt Trigger**
*Product Specification*

## DESCRIPTION

The '14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7414 | 15ns | 31mA |
| 74LS14 | 15ns | 10mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7414N, N74LS14N |
| Plastic SO | N74LS14D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| A | Inputs | 1ul | 1LSul |
| Y | Output | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, and 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



13
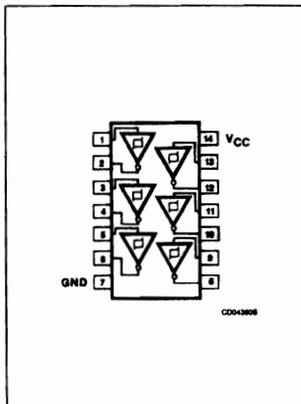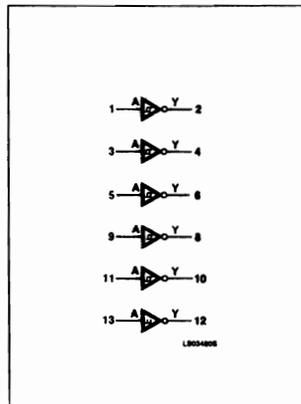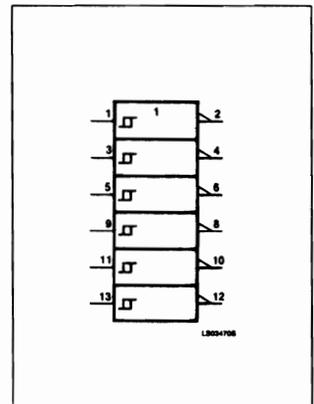
# 54S/74S15
# 54LS/74LS15

## TRIPLE 3-INPUT AND GATE
### (With Open-Collector Outputs)
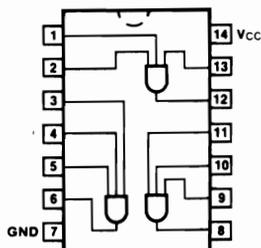
**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE Vcc = +5.0 V ±5%, TA = 0°C to +70°C | MILITARY GRADE Vcc = +5.0 V ±10%, TA = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 74S15PC, 74LS15PC | | 9A |
| Ceramic DIP (D) | A | 74S15DC, 74LS15DC | 54S15DM, 54LS15DM | 6A |
| Flatpak (F) | A | 74S15FC, 74LS15FC | 54S15FM, 54LS15FM | 3I |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PINS | 54/74S (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---|---|---|
| Inputs | 1.25/1.25 | 0.5/0.25 |
| Outputs | OC**/12.5 | OC**/5.0 (2.5) |

**DC AND AC CHARACTERISTICS:** See Section 3*

| SYMBOL | PARAMETER | 54/74S Min | 54/74S Max | 54/74LS Min | 54/74LS Max | UNITS | CONDITIONS | |
|---|---|---|---|---|---|---|---|---|
| Iccн | Power Supply | | 19.5 | | 3.6 | mA | Vin = Open | Vcc = Max |
| Iccl | Current | | 42 | | 6.6 | | Vin = Gnd | |
| tPLH | Propagation Delay | | 8.5 | | 20 | ns | Figs. 3-2, 3-5 | |
| tPHL | | | 9.0 | | 15 | | | |

*DC limits apply over operating temperature range; AC limits apply at TA = +25°C and Vcc = +5.0 V.
**OC — Open Collector

# 7416, 17
## Inverter/Buffer/Drivers

'16 Hex Inverter Buffer/Driver (Open Collector)
'17 Hex Buffer/Driver (Open Collector)
*Product Specification*

Logic Products

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7416 | 10ns ($t_{PLH}$) 15ns ($t_{PHL}$) | 31mA |
| 7417 | 6ns ($t_{PLH}$) 20ns ($t_{PHL}$) | 25mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7416N, N7417N |
| Plastic SO | N7417D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### FUNCTION TABLE

| '16 | | '17 | |
|---|---|---|---|
| INPUT | OUTPUT | INPUT | OUTPUT |
| A | Y | A | Y |
| L | H | L | L |
| H | L | H | H |

H = HIGH voltage level
L = LOW voltage level

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| A | Input | 1ul |
| Y | Output | 10ul |

**NOTE:**
A 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$.

### PIN CONFIGURATION



### LOGIC SYMBOL



### LOGIC SYMBOL (IEEE/IEC)



.15
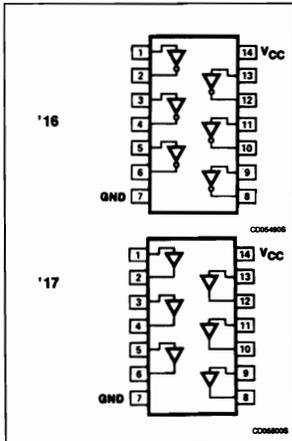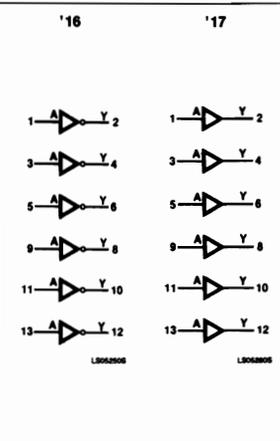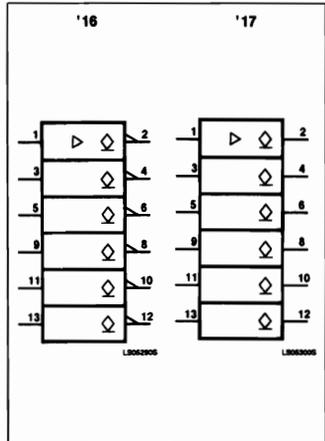
# 7420, 7421, LS20, LS21, S20
## Gates

**Logic Products**

**Dual Four-Input NAND ('20) AND ('21) Gate**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7420 | 10ns | 8mA |
| 74LS20 | 10ns | 0.8mA |
| 74S20 | 3ns | 8mA |
| 7421 | 12ns | 8mA |
| 74LS21 | 9ns | 1.7mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP '20 | N7420N, N74LS20N, N74S20N |
| '21 | N7421N, N74LS21N |
| Plastic SO | N74LS20D, N74S20D, N74LS21D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| A | B | C | D | Y('20) | Y('21) |
| L | X | X | X | H | L |
| X | L | X | X | H | L |
| X | X | L | X | H | L |
| X | X | X | L | H | L |
| H | H | H | H | L | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A – D | Inputs | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and –1.6mA $I_{IL}$, a 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and –2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION

**'20, '21**

CD0439OS

## LOGIC SYMBOL

**'20, '21**

LS03500S

## LOGIC SYMBOL (IEEE/IEC)

**'20, '21**

LS03490S

16
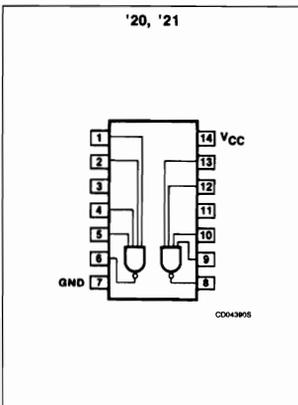
# 7425
## Gate

### Dual Four-Input NOR Gate With Strobe
*Product Specification*

Logic Products

## FUNCTION TABLE

| INPUTS | | | | | OUTPUT |
|---|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **G** | **Y** |
| X | X | X | X | L | H |
| H | X | X | X | H | L |
| X | H | X | X | H | L |
| X | X | H | X | H | L |
| X | X | X | H | H | L |
| L | L | L | L | H | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## LOGIC DIAGRAM



OUTPUT Y

LD0274OS
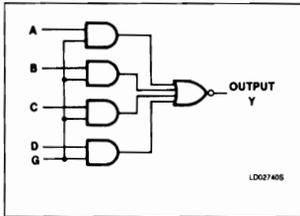
| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7425 | 9ns | 9mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7425N |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| A – D | Inputs | 1ul |
| G | Input | 4ul |
| Y | Output | 10ul |

NOTE:
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and $-1.6$mA $I_{IL}$.

## PIN CONFIGURATION



CD05520S

## LOGIC SYMBOL



LS05330S

## LOGIC SYMBOL (IEEE/IEC)



LS05340S

17
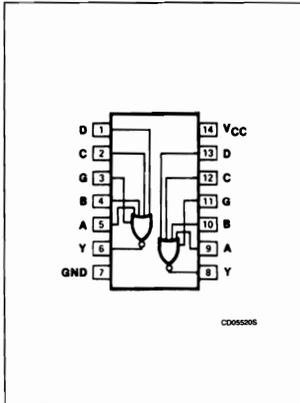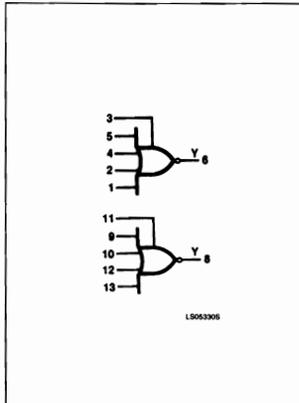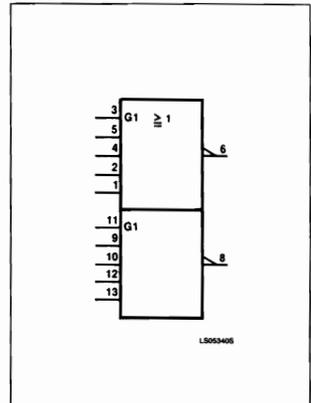
# 7426, LS26
## Gates

### Quad Two-Input NAND Gate (Open Collector)
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7426 | 14ns | 8mA |
| 74LS26 | 16ns | 1.6mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7426N, N74LS26N |
| Plastic SO | N74LS26D |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| A,B | Inputs | 1ul | 1LSul |
| Y | Output | 10ul | 10LSul |

NOTE:
Where a 74 unit load (ul) is understood to be $40\mu$ $I_{IH}$ and $-1.6mA$ $I_{IL}$ and a 74LS unit load (LSul) is $20\mu A$ $I_{IH}$ and $-0.4mA$ $I_{IL}$.

### PIN CONFIGURATION



CD04230S

### LOGIC SYMBOL



LS03300S

### LOGIC SYMBOL (IEEE/IEC)



LS03290S

# 7427, LS27
## Gates

### Triple Three-Input NOR Gate
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7427 | 9ns | 13mA |
| 74LS27 | 10ns | 2.7mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7427N, N74LS27N |
| Plastic SO | N74LS27D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| L | L | L | H |
| X | X | H | L |
| X | H | X | L |
| H | X | X | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| A – C | Inputs | 1ul | 1LSul |
| Y | Output | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, a 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD04170S

## LOGIC SYMBOL



LS05350S

## LOGIC SYMBOL (IEEE/IEC)



LS05360S

19
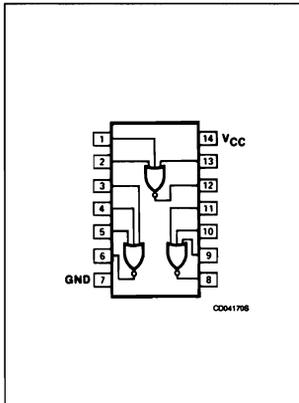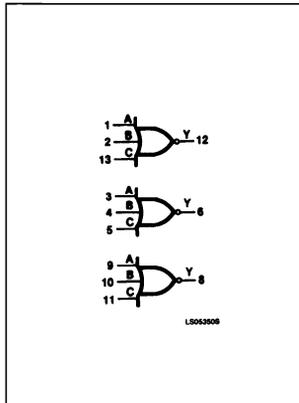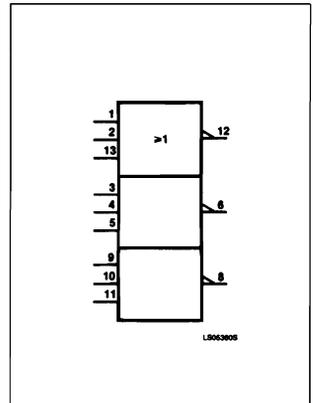
# 7428
## Buffer

**Quad Two-Input NOR Buffer**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7428 | 7ns | 23mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7428N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| A, B | Inputs | 1ul |
| Y | Output | 30ul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$.

## PIN CONFIGURATION



CD04180S

## LOGIC SYMBOL



LS03200S

## LOGIC SYMBOL (IEEE/IEC)



LS05380S

20

# 7430, LS30
## Gates

**Eight-Input NAND Gate**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7430 | 11ns | 2mA |
| 74LS30 | 11ns | 0.5mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7430N, N74LS30N |
| Plastic SO | N74LS30D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|
| A | B | C | D | E | F | G | H | Y |
| L | X | X | X | X | X | X | X | H |
| X | L | X | X | X | X | X | X | H |
| X | X | L | X | X | X | X | X | H |
| X | X | X | L | X | X | X | X | H |
| X | X | X | X | L | X | X | X | H |
| X | X | X | X | X | L | X | X | H |
| X | X | X | X | X | X | L | X | H |
| X | X | X | X | X | X | X | L | H |
| H | H | H | H | H | H | H | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| A – H | Inputs | 1ul | 1LSul |
| Y | Output | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD05550S

## LOGIC SYMBOL



LS05390S

## LOGIC SYMBOL (IEEE/IEC)



LS05400S

21
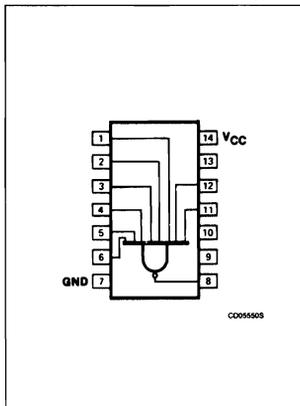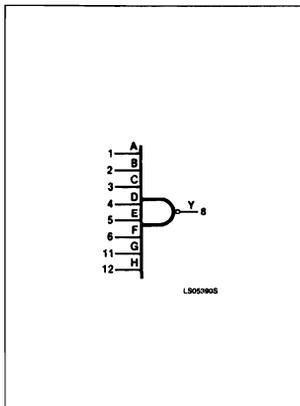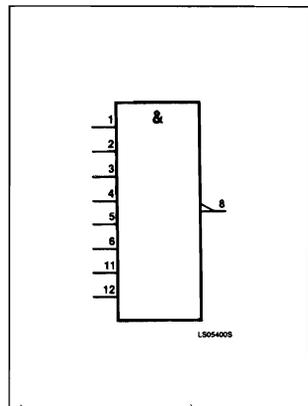
# 7432, LS32, S32
# Gates

**Quad Two-Input OR Gate**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7432 | 12ns | 19mA |
| 74LS32 | 14ns | 4.0mA |
| 74S32 | 4ns | 28mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7432N, N74LS32N, N74S32N |
| Plastic SO – 14 | N74LS32D, N74S32D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | H |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A, B | Inputs | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and −1.6mA $I_{IL}$, and a 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and −2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and −0.4mA $I_{IL}$

## PIN CONFIGURATION



CD044005

## LOGIC SYMBOL



LS03520S

## LOGIC SYMBOL (IEEE/IEC)



LS03510S

22
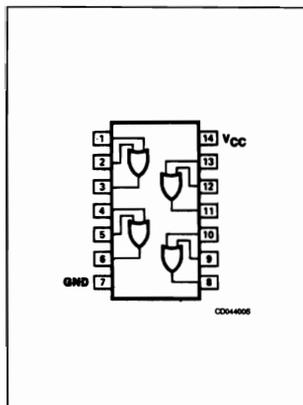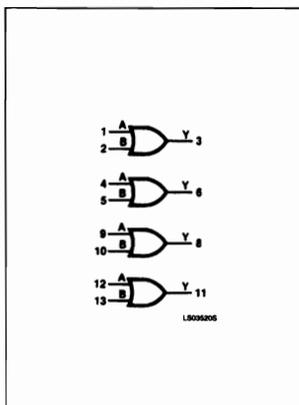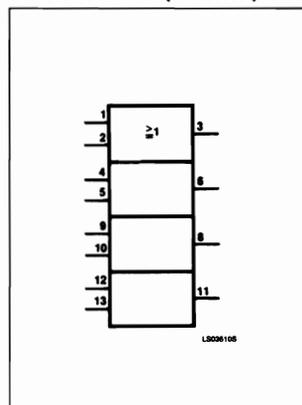
# 7433, LS33
## Buffers

**Quad Two-Input NOR Buffer (Open Collector)**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7433 | 11ns | 23mA |
| 74LS33 | 19ns | 4mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7433N, N74LS33N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| A, B | Inputs | 1ul | 1LSul |
| Y | Output | 30ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$, a 74LS unit load (LSul) is $20\mu A$ $I_{IH}$ and $-0.4mA$ $I_{IL}$.

## PIN CONFIGURATION



CD05560S

## LOGIC SYMBOL



LS05210S

## LOGIC SYMBOL (IEEE/IEC)



LS05420S

# 7437, LS37, S37
## Buffers

**Quad Two-Input NAND Buffer**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 7437 | 11ns | 22mA |
| 74LS37 | 12ns | 3.5mA |
| 74S37 | 4ns | 33mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|--------------------------------------------------------------|
| Plastic DIP | N7437N, N74LS37N, N74S37N |
| Plastic SO | N74S37D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|--|--------|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|------|-------------|----|-----|------|
| A, B | Inputs | 1ul | 2Sul | 1LSul |
| Y | Output | 30ul | 30Sul | 30LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and $-1.6$mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and $-2.0$mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



CD04410S

## LOGIC SYMBOL



LS03540S

## LOGIC SYMBOL (IEEE/IEC)



LS03530S

# 7438, LS38, S38
## Buffers

**Quad Two-Input NAND Buffers (Open Collectors)**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7438 | 13ns | 28mA |
| 74LS38 | 19ns | 3.5mA |
| 74S38 | 6.5ns | 33mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N7438N, N74LS38N, N74S38N |
| Plastic SO | N74S38D, N74LS38D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A, B | Inputs | 1ul | 2Sul | 1LSul |
| Y | Output | 30ul | 30Sul | 30LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50μA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD04420S

## LOGIC SYMBOL



LS03560S

## LOGIC SYMBOL (IEEE/IEC)



LS03550S

25

# 7439
## Buffer

**Quad Two-Input NAND Buffer (Open Collector)**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 7439 | 11ns | 4.5mA ($I_{CCH}$)<br>30mA ($I_{CCL}$) |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE<br>$V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|------------------------------------------------------------------|
| Plastic DIP | N7439N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|-------------|----|
| A, B | Inputs | 1ul |
| Y | Output | 30ul |

**NOTE:**
A 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$.

## PIN CONFIGURATION



CD07600S

## LOGIC SYMBOL



LS05210S

## LOGIC SYMBOL (IEEE/IEC)



LS05440S
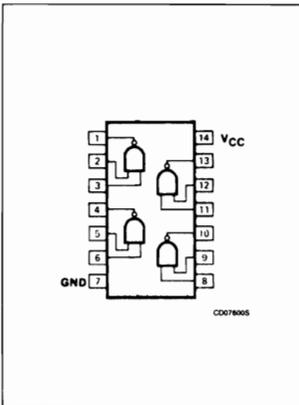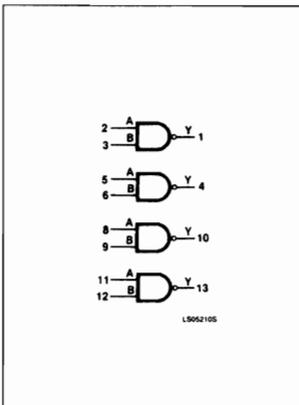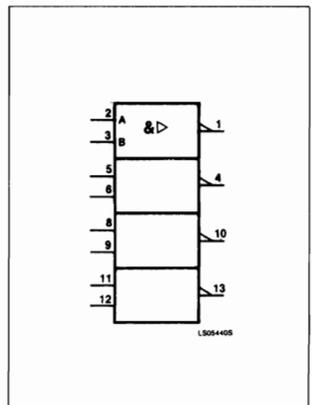
# 7440, LS40, S40
## Buffers

**Dual Four-Input NAND Buffer**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7440 | 11ns | 11mA |
| 74LS40 | 12ns | 1.8mA |
| 74S40 | 6ns | 18mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7440N, N74LS40N, N74S40N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |
| H | H | H | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A – D | Inputs | 1ul | 2Sul | 1LSul |
| Y | Output | 30ul | 30Sul | 30LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50μA $I_{IH}$ and −2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



27
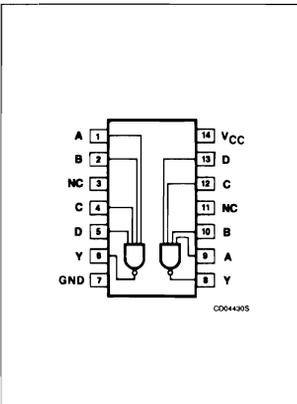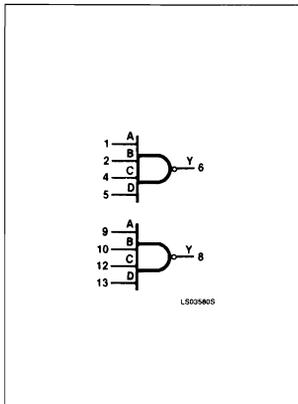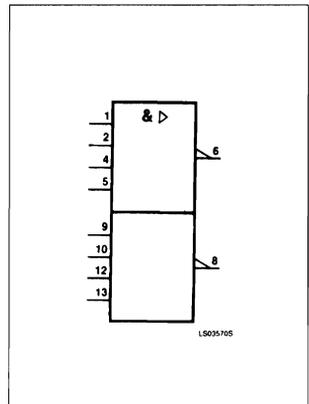
# 7442, LS42
## Decoders

**BCD-To-Decimal Decoder (1-of-10)**
*Product Specification*

## FEATURES
- Mutually exclusive outputs
- 1-of-8 demultiplexing ability
- Outputs disabled for input codes above nine

## DESCRIPTION
The '42 decoder accepts four active HIGH BCD inputs and provides 10 mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the '42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input, $A_3$, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The $A_3$ input can also be used as the Data input in an 8-output demultiplexer application.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7442 | 15ns | 28mA |
| 74LS42 | 18ns | 7mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7442N, N74LS42N |
| Plastic SO | N74LS54D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| $A_0 - A_3$ | Inputs | 1ul | 1LSul |
| $\overline{0} - \overline{9}$ | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$ and a 74LS unit load (LSul) is $20\mu A$ $I_{IH}$ and $-0.4mA$ $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



28
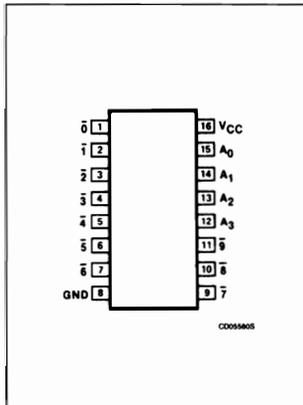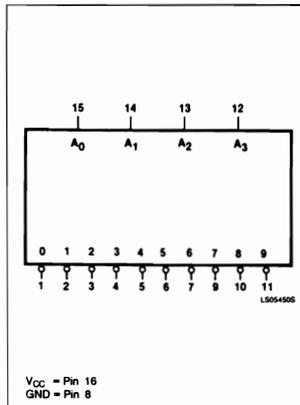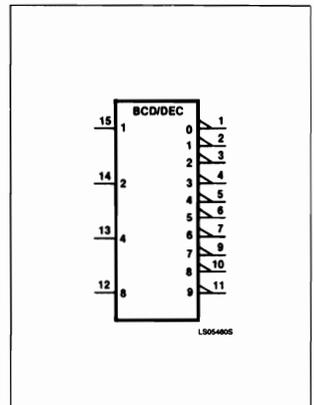
# 7445
# Decoder/Driver

**BCD-To-Decimal Decoder/Driver (Open Collector)**
*Product Specification*

## FEATURES
- 80mA output sink capability
- 30V output breakdown voltage
- Ideally suited as lamp or solenoid driver
- See '42 for standard TTL output version
- See '145 for "LS" version

## DESCRIPTION

The '45 decoder accepts BCD inputs on the $A_0$ to $A_3$ address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are off. This device can therefore be used as a 1-of-8 decoder with $A_3$ used as an active LOW enable.

The '45 can sink 20mA while maintaining the standardized guaranteed output LOW voltage ($V_{OL}$) of 0.4V, but it can sink up to 80mA with a guaranteed $V_{OL}$ of less than 0.9V.

The '45 features an output breakdown voltage of 30V and is ideally suited as a lamp or solenoid driver.

| TYPE | MAX $I_{OL}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|------|------|
| 7445 | 80mA | 43mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|------|------|
| Plastic DIP | N7445N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|------|------|
| $A_0 - A_3$ | Inputs | 1ul |
| $\bar{0} - \bar{9}$ | Outputs | 12.5ul |

**NOTE:**
A 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$.

## PIN CONFIGURATION



```
 0̄ [1      16] Vcc
 1̄ [2      15] A0
 2̄ [3      14] A1
 3̄ [4      13] A2
 4̄ [5      12] A3
 5̄ [6      11] 9̄
 6̄ [7      10] 8̄
GND [8      9 ] 7̄
```
CD05580S

## LOGIC SYMBOL



LS05470S

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



LS05480S

29
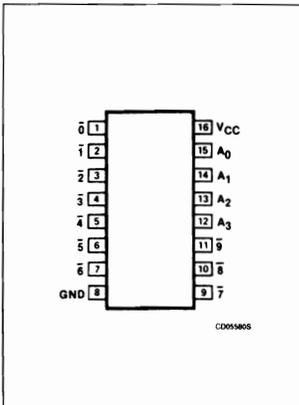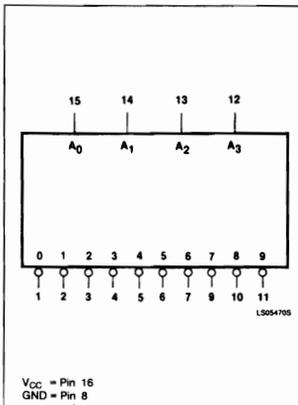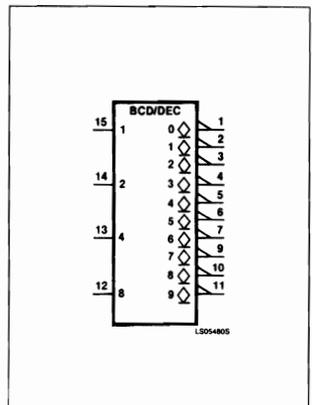
# 54/7446A • 54/7447A
# 54LS/74LS47
## BCD TO 7-SEGMENT DECODER/DRIVER

**DESCRIPTION** — The '46A, '47A and 'LS47 accept four lines of BCD (8421) input data, generate their complements internally and decode the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 40 mA (24 mA for the 'LS47) in the ON (LOW) state and withstand 15 V (30 V for the '46A) in the OFF (HIGH) state with a maximum leakage current of 250 μA. Auxiliary inputs provide blanking, lamp test and cascadable zero-suppression fuctions. Also see the 'LS247 data sheet.

- **OPEN-COLLECTOR OUTPUTS**
- **DRIVE INDICATOR SEGMENTS DIRECTLY**
- **CASCADABLE ZERO-SUPPRESSION CAPABILITY**
- **LAMP TEST INPUT**

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE $V_{CC}$ = +5.0 V ±5%, $T_A$ = 0°C to +70°C | MILITARY GRADE $V_{CC}$ = +5.0 V ±10%, $T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 7446APC, 7447APC 74LS47PC | | 9B |
| Ceramic DIP )D) | A | 7446ADC, 7447ADC 74LS47DC | 5446ADM, 5447ADM 54LS47DM | 7B |
| Flatpak (F) | A | 7446AFC, 7447AFC 74LS47FC | 5446AFM, 5447AFM · 54LS47FM | 4L |
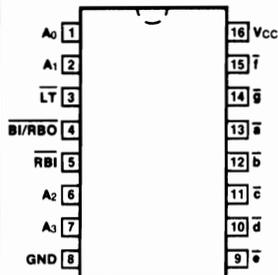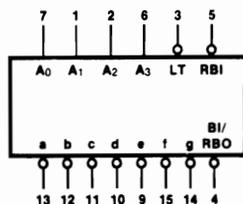
**LOGIC SYMBOL**



**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74 (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---|---|---|---|
| $A_0 - A_3$ | BCD Inputs | 1.0/1.0 | 0.5/0.25 |
| $\overline{RBI}$ | Ripple Blanking Input (Active LOW) | 1.0/1.0 | 0.5/0.25 |
| $\overline{LT}$ | Lamp Test Input (Active LOW) | 1.0/1.0 | 0.5/0.25 |
| $\overline{BI/RBO}$ | Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW) | -/2.5 5.0/5.0 | -/0.75 1.25/2.0 (1.0) |
| $\overline{a} - \overline{g}$ | Segment Outputs (Active LOW) | OC*/25 | OC*/15 (7.5) |

*OC— Open Collector

**FUNCTIONAL DESCRIPTION** — The '46A, '47A and 'LS47 decode the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multidigit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, ie: by driving $\overline{RBI}$ of an intermediate decoder from an OR gate whose inputs are $\overline{BI/RBO}$ of the next highest and lowest order decoders. $BI/RBO$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI/RBO}$ can be forced LOW by enternal means, using wired-collector logic. A LOW signal thus applied to $\overline{BI/RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI/RBO}$ is not forced LOW.

## LOGIC DIAGRAM
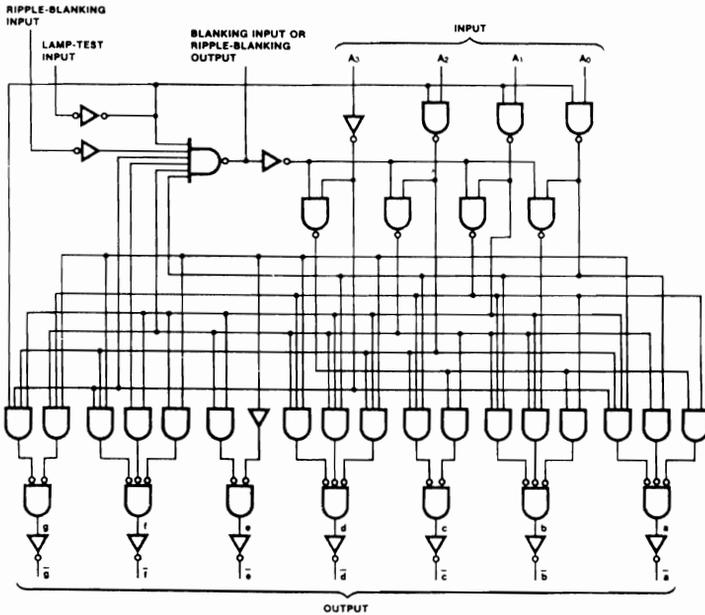


## NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS
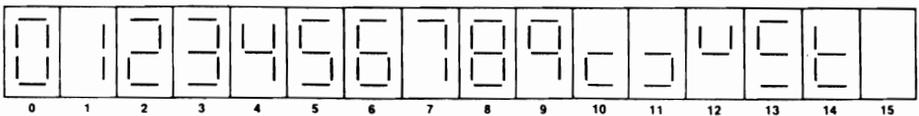
TRUTH TABLE

| DECIMAL OR FUNCTION | INPUTS | | | | | | | OUTPUTS | | | | | | | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{LT}$ | $\overline{RBI}$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | $\overline{BI}/\overline{RBO}$ | $\overline{a}$ | $\overline{b}$ | $\overline{c}$ | $\overline{d}$ | $\overline{e}$ | $\overline{f}$ | $\overline{g}$ | |
| 0 | H | H | L | L | L | L | H | L | L | L | L | L | L | H | 1 |
| 1 | H | X | L | L | L | H | H | H | L | L | H | H | H | H | 1 |
| 2 | H | X | L | L | H | L | H | L | L | H | L | L | H | L | |
| 3 | H | X | L | L | H | H | H | L | L | L | L | H | H | L | |
| 4 | H | X | L | H | L | L | H | H | L | L | H | H | L | L | |
| 5 | H | X | L | H | L | H | H | L | H | L | L | H | L | L | |
| 6 | H | X | L | H | H | L | H | H | H | L | L | L | L | L | |
| 7 | H | X | L | H | H | H | H | L | L | L | H | H | H | H | |
| 8 | H | X | H | L | L | L | H | L | L | L | L | L | L | L | |
| 9 | H | X | H | L | L | H | H | L | L | L | H | H | L | L | |
| 10 | H | X | H | L | H | L | H | H | H | H | L | L | H | L | |
| 11 | H | X | H | L | H | H | H | H | H | L | L | H | H | L | |
| 12 | H | X | H | H | L | L | H | H | L | H | H | H | L | L | |
| 13 | H | X | H | H | L | H | H | L | H | H | L | H | L | L | |
| 14 | H | X | H | H | H | L | H | H | H | H | L | L | L | L | |
| 15 | H | X | H | H | H | H | H | H | H | H | H | H | H | H | |
| $\overline{BI}$ | X | X | X | X | X | X | L | H | H | H | H | H | H | H | 2 |
| $\overline{RBI}$ | H | L | L | L | L | L | L | H | H | H | H | H | H | H | 3 |
| $\overline{LT}$ | L | X | X | X | X | X | H | L | L | L | L | L | L | L | 4 |

NOTES:
(1) $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{RBI}$) and inputs $A_0$, $A_1$, $A_2$ and $A_3$ are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

# 7451, LS51, S51
## Gates

'51, 'S51 Dual 2-Wide 2-Input AND-OR-Invert Gate
'LS51 Dual 2-Wide 3-Input, 2-Wide 2-Input AND-OR-Invert Gate

**Logic Products**

*Product Specification*

## FUNCTION TABLE
### '51, 'S51, ½ 'LS51

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| H | H | X | X | L |
| X | X | H | H | L |
| All other combinations | | | | H |

### 'LS51

| INPUTS | | | | | | OUTPUT |
|---|---|---|---|---|---|---|
| A | B | C | D | E | F | Y |
| H | H | H | X | X | X | L |
| X | X | X | H | H | H | L |
| All other combinations | | | | | | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7451 | 11ns | 5.7mA |
| 74LS51 | 12ns | 1.1mA |
| 74S51 | 3.5ns | 11mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7451N, N74LS51N, N74S51N |
| Plastic SO | N74LS51D, N74S51D |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| All | Inputs | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

NOTE:
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



33

# 54/7453
# 54H/74H53

## EXPANDABLE 4-WIDE, 2-INPUT AOI GATE ('53)
## EXPANDABLE 2-2-2-3-INPUT AOI GATE ('H53)

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE $V_{CC}$ = +5.0 V ±5%, $T_A$ = 0°C to +70°C | MILITARY GRADE $V_{CC}$ = +5.0 V ±10%, $T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 7453PC | | 9A |
| | B | 74H53PC | | |
| Ceramic DIP (D) | A | 7453DC | 5453DM | 6A |
| | B | 74H53DC | 54H53DM | |
| Flatpak (F) | C | 7453FC | 5453FM | 3I |
| | D | 74H53FC | 54H53FM | |

PINOUT B
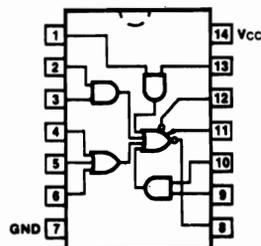


**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PINS | 54/74 (U.L.) HIGH/LOW | 54/74H (U.L.) HIGH/LOW |
|---|---|---|
| Inputs | 1.0/1.0 | 1.25/1.25 |
| Outputs | 20/10 | 12.5/12.5 |

PINOUT C
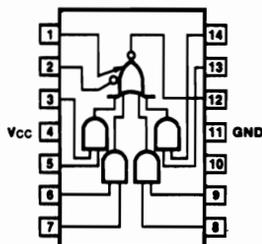


PINOUT D
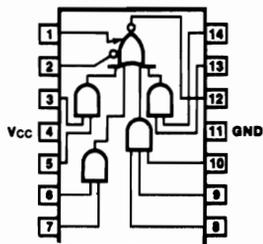
# 74LS54
# Gate

### Four-Wide Two- & Three-Input AND-OR-Invert Gate
### *Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS54 | 12ns | 0.9mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS54N |
| Plastic SO | N74LS54D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| A – K | Inputs | 1LSul |
| Y | Output | 10LSul |

**NOTE:**
Where a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## FUNCTION TABLE

| INPUTS | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | E | F | G | H | J | K | Y |
| H | H | X | X | X | X | X | X | X | X | L |
| X | X | H | H | X | X | X | X | X | X | L |
| X | X | X | X | X | H | H | X | X | X | L |
| X | X | X | X | X | X | X | H | H | H | L |
| All other combinations | | | | | | | | | | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## PIN CONFIGURATION
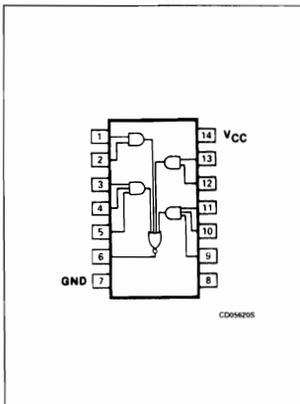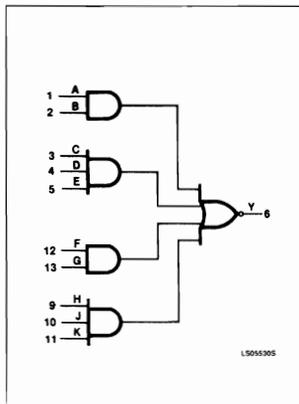


## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)
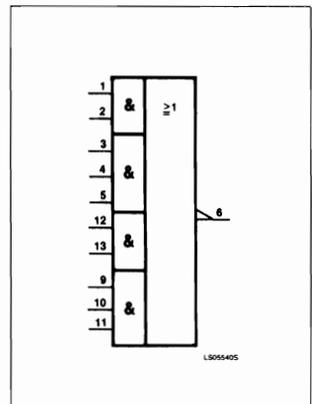
# 74S64
## Gate

**Four-Two-Three-Two-Input AND-OR-Invert Gate**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74S64 | 3.5ns | 8mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74S64N |
| Plastic SO | N74S64D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S |
|---|---|---|
| A – L | Inputs | 1Sul |
| Y | Output | 10Sul |

**NOTE:**
A 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$.

## FUNCTION TABLE

| INPUTS | | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | E | F | G | H | J | K | L | Y |
| H | H | X | X | X | X | X | X | X | X | X | L |
| X | X | H | H | H | H | X | X | X | X | X | L |
| X | X | X | X | X | X | H | H | H | X | X | L |
| X | X | X | X | X | X | X | X | X | H | H | L |
| All other combinations | | | | | | | | | | | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## PIN CONFIGURATION



CD05630S

## LOGIC SYMBOL



LS03030S

## LOGIC SYMBOL (IEEE/IEC)



LS03020S

36
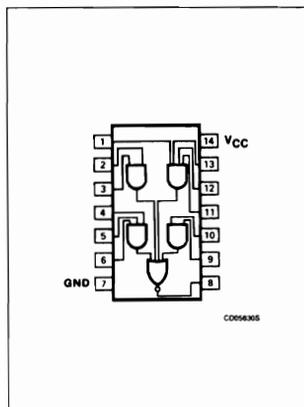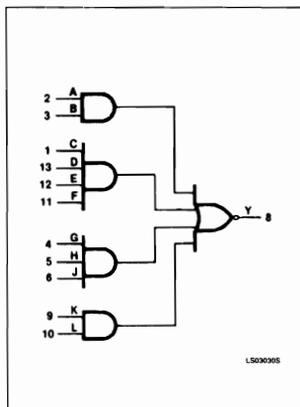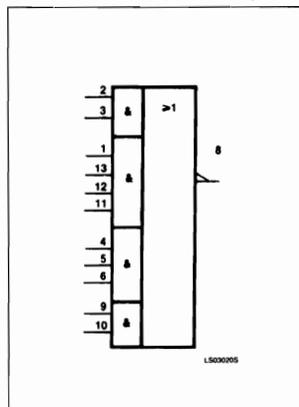
# 7473, LS73
## Flip-Flops

### Dual J-K Flip-Flop
*Product Specification*

**Logic Products**

## DESCRIPTION
The '73 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 7473 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW transition. For the 7473, the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS73 is a negative edge-triggered flip-flop. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset ($\bar{R}_D$) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the $\bar{Q}$ output HIGH.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7473 | 20MHz | 10mA |
| 74LS73 | 45MHz | 4mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7473N, N74LS73N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| $\overline{CP}$ | Clock input | 2ul | 4LSul |
| $\bar{R}_D$ | Reset input | 2ul | 3LSul |
| J, K | Data inputs | 1ul | 1LSul |
| Q,$\bar{Q}$ | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEE/IEC)



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## LOGIC DIAGRAM



LD02770S

## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\bar{R}_D$ | $\overline{CP}^{(2)}$ | J | K | Q | $\bar{Q}$ |
| Asynchronous reset (Clear) | L | X | X | X | L | H |
| Toggle | H | ⎍ | h | h | $\bar{q}$ | q |
| Load "0" (Reset) | H | ⎍ | l | h | L | H |
| Load "1" (Set) | H | ⎍ | h | l | H | L |
| Hold "no change" | H | ⎍ | l | l | q | $\bar{q}$ |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.[1]
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.[1]
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
X = Don't care
⎍ = Positive Clock pulse.

**NOTES:**
1. The J and K inputs of the 7473 must be stable while the Clock is HIGH for conventional operation.
2. The 74LS73 is edge triggered. Data must be stable one set-up time prior to the negative edge of the Clock for predictable operation.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

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# 7474, LS74A, S74
# Flip-Flops

**Dual D-Type Flip-Flop**
*Product Specification*

**Logic Products**

## DESCRIPTION

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and $\bar{Q}$ outputs.

Set ($\bar{S}_D$) and Reset ($\bar{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|-------------------|--------------------------------|
| 7474 | 25MHz | 17mA |
| 74LS74A | 33MHz | 4mA |
| 74S74 | 100MHz | 30mA |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|----------|---------------------------------------------------------|
| Plastic DIP | N7474N, N74LS74AN, N74S74N |
| Plastic SO | N741S74A, N74S74D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|------|-------------|----|----|------|
| D | Input | 1ul | 1Sul | 1LSul |
| $\bar{R}_D$ | Input | 2ul | 3Sul | 2LSul |
| $\bar{S}_D$ | Input | 1ul | 2Sul | 2LSul |
| CP | Input | 2ul | 2Sul | 1LSul |
| Q,$\bar{Q}$ | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and –1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and –2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION
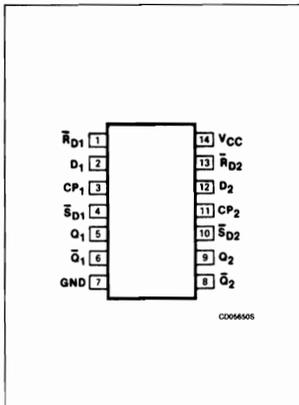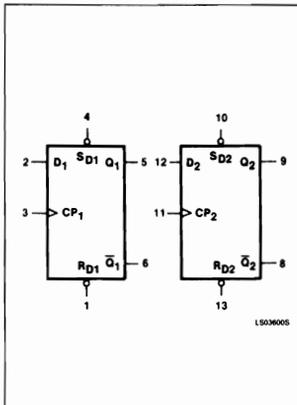


## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)
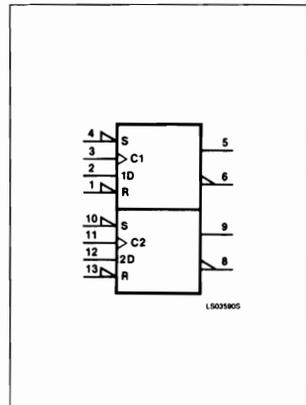
# 7474, LS74A, S74

## LOGIC DIAGRAM



LD02780S
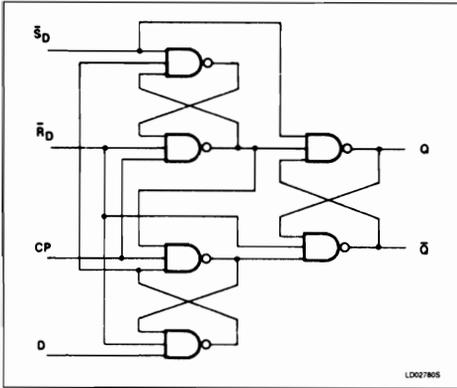
## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\overline{S}_D$ | $\overline{R}_D$ | CP | D | Q | $\overline{Q}$ |
| Asynchronous Set | L | H | X | X | H | L |
| Asynchronous Reset (Clear) | H | L | X | X | L | H |
| Undetermined[1] | L | L | X | X | H | H |
| Load "1" (Set) | H | H | ↑ | h | H | L |
| Load "0" (Reset) | H | H | ↑ | l | L | H |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
NOTE:
(1) Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | 74S | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −400 | | | −1000 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | 0 | | 70 | °C |

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# 7475, LS75
## Latches

### Quad Bistable Latch
### *Product Specification*

**Logic Products**

## FEATURES
- **4-bit bistable latch**
- **Refer to 74LS375 for $V_{CC}$ and GND on corner pins**

## DESCRIPTION
The '75 has four bistable latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is HIGH. The data on the D inputs one set-up time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7475 | 18ns ($t_{PLH}$) <br> 9ns ($t_{PHL}$) | 32mA |
| 74LS75 | 15ns ($t_{PLH}$) <br> 9ns ($t_{PHL}$) | 6.3mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N7475N, N74LS75N |
| Plastic SO | N74LS25D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| D | Input | 2ul | 1LSUI |
| E | Input | 4ul | 4LSUI |
| All | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and – 1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20μA $I_{IH}$ and – 0.4mA.

## PIN CONFIGURATION



CD056605

## LOGIC SYMBOL



LS05630S

$V_{CC}$ = Pin 5
GND = Pin 12

## LOGIC SYMBOL (IEEE/IEC)



LS05640S

41
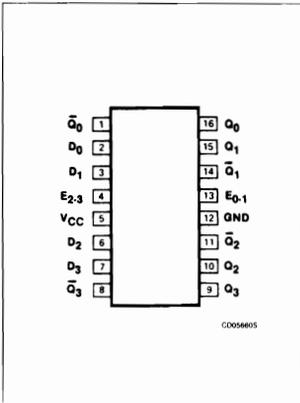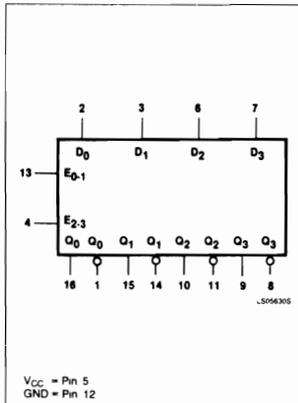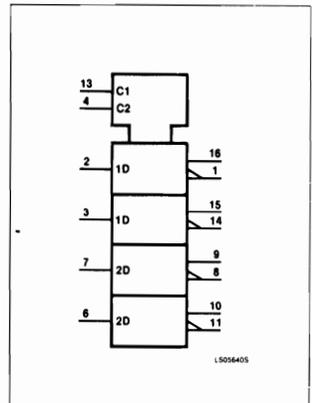
# 7476, LS76
## Flip-Flops

### Dual J-K Flip-Flop
*Product Specification*

**Logic Products**

## DESCRIPTION
The '76 is a dual J-K flip-flop with individual J, K, Clock, Set and Reset inputs. The 7476 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one set-up time prior to the HIGH-to-LOW Clock transition.

The Set ($\bar{S}_D$) and Reset ($\bar{R}_D$) are asynchronous active LOW inputs. When LOW, they override the Clock and Data inputs, forcing the outputs to the steady state levels as shown in the Function Table.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7476 | 20MHz | 10mA |
| 74LS76 | 45MHz | 4mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N7476N, N74LS76N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| $\overline{CP}$ | Clock input | 2ul | 2LSul |
| $\bar{R}_D$, $\bar{S}_D$ | Reset and Set inputs | 2ul | 2LSul |
| J, K | Data inputs | 1ul | 1LSul |
| Q, $\bar{Q}$ | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and –1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEE/IEC)

## LOGIC DIAGRAM



LD02800S

## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| | $\overline{S}_D$ | $\overline{R}_D$ | $\overline{CP}^{(2)}$ | J | K | Q | $\overline{Q}$ |
| Asynchronous set | L | H | X | X | X | H | L |
| Asynchronous reset (Clear) | H | L | X | X | X | L | H |
| Undetermined[1] | L | L | X | X | X | H | H |
| Toggle | H | H | ⊓ | h | h | $\overline{q}$ | q |
| Load "0" (Reset) | H | H | ⊓ | l | h | L | H |
| Load "1" (Set) | H | H | ⊓ | h | l | H | L |
| Hold "no change" | H | H | ⊓ | l | l | q | $\overline{q}$ |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.[3]
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.[3]
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
X = Don't care.
⊓ = Positive Clock pulse.

**NOTES:**
1. Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.
2. The 74LS76 is edge triggered. Data must be stable one set-up time prior to the negative edge of the Clock for predictable operation.
3. The J and K inputs of the 7476 must be stable while the Clock is HIGH for conventional operation.

# 7483, LS83A
## Adders

**4-Bit Full Adder**
*Product Specification*

**Logic Products**

## FEATURES
- High speed 4-bit binary addition
- Cascadeable in 4-bit increments
- LS83A has fast internal carry lookahead
- See '283 for corner power pin version

## DESCRIPTION
The '83 adds two 4-bit binary words ($A_n$ plus $B_n$) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry ($C_{OUT}$) according to the equation:

$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3)$
$+ 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4$
$+ 16C_{OUT}$

Where $( + ) = $ plus.

Due to the symmetry of the binary add function, the '83 can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). See Function Table. With active-HIGH inputs, $C_{IN}$ cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus $C_{IN}$, $A_1$, $B_1$, can arbitrarily be assigned to pins 10, 11, 13, etc.

| TYPE | TYPICAL ADD TIMES (TWO 8 – BIT WORDS) | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7483 | 23ns | 66mA |
| 74LS83A | 25ns | 19mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7483N, N74LS83AN |
| Plastic SO | N74LS83AD |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| $A_1$, $B_1$, $A_3$, $B_3$, $C_{IN}$ | Inputs | 2ul | |
| $A_2$, $B_2$, $A_4$, $B_4$ | Inputs | 1ul | |
| A, B | Inputs | | 2LSul |
| $C_{IN}$ | Input | | 1LSul |
| Sum | Outputs | 10ul | 10LSul |
| Carry | Output | 5ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and – 1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20μA $I_{IH}$ and – 0.4mA $I_{IL}$.

## PIN CONFIGURATION



A4 [1]  [16] B4
Σ3 [2]  [15] Σ4
A3 [3]  [14] COUT
B3 [4]  [13] CIN
VCC [5]  [12] GND
Σ2 [6]  [11] B1
B2 [7]  [10] A1
A2 [8]  [9] Σ1

CD05680S

## LOGIC SYMBOL



10 11 8 7 3 4 1 16
A1 B1 A2 B2 A3 B3 A4 B4
13 CIN        COUT 14
Σ1 Σ2 Σ3 Σ4
9 6 2 15

LS05680S

VCC = Pin 5
GND = Pin 12

## LOGIC SYMBOL (IEEE/IEC)



LS05700S

44
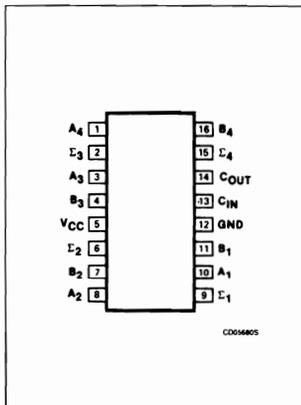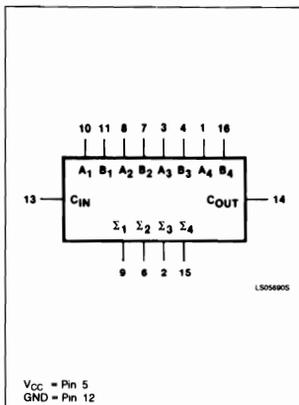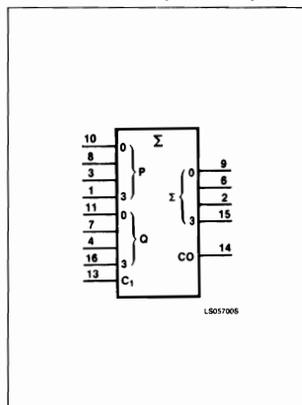
# 7485, LS85, S85
# Comparators

**4-Bit Magnitude Comparator**
*Product Specification*

**Logic Products**

## FEATURES
- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating
- Use 74S85 for very high speed comparisons

## DESCRIPTION
The '85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted $(A_0 - A_3)$ and $(B_0 - B_3)$, where $A_3$ and $B_3$ are the most significant bits.

The operation of the '85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7485 | 23ns | 55mA |
| 74LS85 | 23ns | 10mA |
| 74S85 | 12ns | 73mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7485N, N74LS85N, N74S85N |
| Plastic SO | N74LS85D, N74S85D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| $A_0 - A_3$, $B_0 - B_3$, $I_{A = B}$ | Inputs | 3ul | 3Sul | 3LSul |
| $I_{A < B}$, $I_{A > B}$ | Inputs | 1ul | 1Sul | 1LSul |
| $A = B$, $A < B$, $A > B$ | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50μA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION
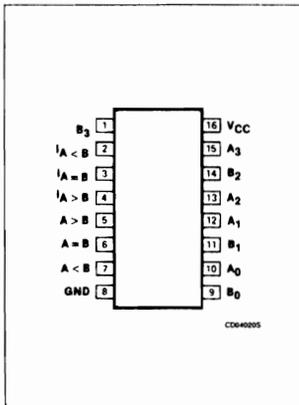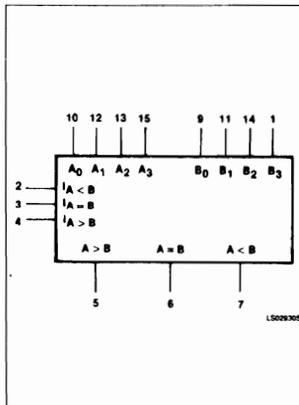


## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)
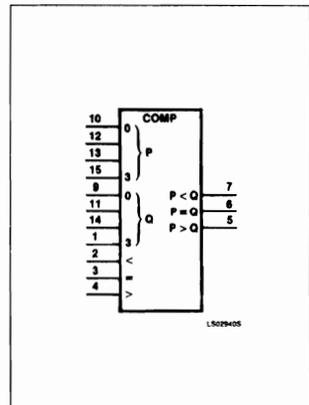
## LOGIC DIAGRAM
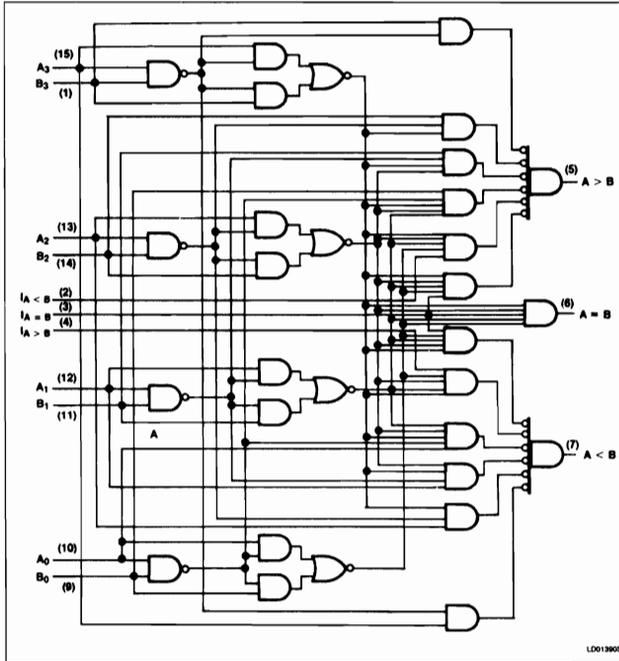


In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the $A > B$, $A = B$ and $A < B$ outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = LOW, $I_{A=B}$ = HIGH, and $I_{A<B}$ = LOW.

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ LOW. The '85 can be used as a 5-bit comparator only when the outputs are used to drive the ($A_0 - A_3$) and ($B_0 - B_3$) inputs of another '85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

## FUNCTION TABLE

| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| $A_3$, $B_3$ | $A_2$, $B_2$ | $A_1$, $B_1$ | $A_0$, $B_0$ | $I_{A>B}$ | $I_{A<B}$ | $I_{A=B}$ | $A > B$ | $A < B$ | $A = B$ |
| $A_3 > B_3$ | X | X | X | X | X | X | H | L | L |
| $A_3 < B_3$ | X | X | X | X | X | X | L | H | L |
| $A_3 = B_3$ | $A_2 > B_2$ | X | X | X | X | X | H | L | L |
| $A_3 = B_3$ | $A_2 < B_2$ | X | X | X | X | X | L | H | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 > B_1$ | X | X | X | X | H | L | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 < B_1$ | X | X | X | X | L | H | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 > B_0$ | X | X | X | H | L | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 < B_0$ | X | X | X | L | H | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | H | L | L | H | L | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | L | H | L | L | H | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | L | L | H | L | L | H |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | X | X | H | L | L | H |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | H | H | L | L | L | L |
| $A_3 = B_3$ | $A_2 = B_2$ | $A_1 = B_1$ | $A_0 = B_0$ | L | L | L | H | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

# 7486, LS86, S86
## Gates

**Quad Two-Input Exclusive-OR Gate**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7486 | 14ns | 30mA |
| 74LS86 | 10ns | 6.1mA |
| 74S86 | 7ns | 50mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7486N, N74LS86N, N74S86N |
| Plastic SO | N74LS86D, N74S86D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| A, B | Inputs | 1ul | 1Sul | 1LSul |
| Y | Output | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and –1.6mA $I_{IL}$, a 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and –2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD04450S

## LOGIC SYMBOL



LS03620S

## LOGIC SYMBOL (IEEE/IEC)



LS05720S

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# 7490, LS90
## Counters

**Decade Counter**
*Product Specification*

## DESCRIPTION

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the $\overline{CP}_1$ input must be externally connected to the $Q_0$ output. The $\overline{CP}_0$ input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the $Q_3$ output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the $CP_1$ input and a divide-by-ten square wave is obtained at output $Q_0$. To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and $Q_0$ as the output). The $\overline{CP}_1$ input is used to obtain a divide-by-five operation at the $Q_3$ output.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT |
|---|---|---|
| 7490 | 30MHz | 30mA |
| 74LS90 | 42MHz | 9mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7490N, N74LS90N |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| $\overline{CP}_0$ | Input | 2ul | 6LSul |
| $\overline{CP}_1$ | Input | 4ul | 8LSul |
| MR, MS | Inputs | | 1ul |
| $Q_0 - Q_3$ | Outputs | 10ul | 10LSul |

NOTE:
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 5
GND = Pin 10

## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



MS$_1$ (6)
MS$_2$ (7)

$\overline{CP}_0$ (14)

$\overline{CP}_1$ (1)

MR$_1$ (2)
MR$_2$ (3)

(12) (9) (8) (11)
Q$_0$ Q$_1$ Q$_2$ Q$_3$

LD02640S

V$_{CC}$ = Pin 5
GND = Pin 10

## MODE SELECTION — FUNCTION TABLE

| RESET/SET INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| MR$_1$ | MR$_2$ | MS$_1$ | MS$_2$ | Q$_0$ | Q$_1$ | Q$_2$ | Q$_3$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| L | X | L | X | Count | | | |
| X | L | X | L | Count | | | |
| L | X | X | L | Count | | | |
| H | L | X | X | Count | | | |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## BCD COUNT SEQUENCE — FUNCTION TABLE

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | Q$_0$ | Q$_1$ | Q$_2$ | Q$_3$ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |

NOTE:
Output Q$_0$ connected to input $\overline{CP}_1$.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| V$_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| V$_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| I$_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| V$_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +V$_{CC}$ | −0.5 to +V$_{CC}$ | V |
| T$_A$ | Operating free-air temperature range | 0 to 70 | | °C |

NOTE:
V$_{IN}$ is limited to +5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs on the 74LS90 only.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| V$_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| V$_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| V$_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| I$_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| I$_{OH}$ | HIGH-level output current | | | −800 | | | −400 | μA |
| I$_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| T$_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 7491A
# Register

**8-Bit Shift Register**
*Product Specification*

**Logic Products**

## FEATURES
- **8-bit serial-in-serial-out shift register**
- **Common buffered clock**
- **2-input gate for serial data entry**
- **True and Complement outputs**

## DESCRIPTION
The '91A is an 8-bit serial-in-serial-out shift register. The serial data is entered through a 2-input AND gate ($D_{Sa}$ and $D_{Sb}$). HIGH data is entered when both $D_{Sa}$ and $D_{Sb}$ are HIGH. LOW data is entered when either Serial Data input is LOW. The Data inputs are edge-triggered and must be stable just one set-up time prior to the LOW-to-HIGH transition of the Clock input (CP) for predictable operation. The data is shifted one bit to the right ($Q_0 \rightarrow Q_2 \cdots \rightarrow Q_7$) synchronous with each LOW-to-HIGH clock transition. The '91A has no reset capacity, so initialization requires the shifting in of at least 8 bits of known data.

Once the register is fully loaded, the Q output follows the Serial inputs delayed by eight clock pulses. The Complement ($\overline{Q}$) output from the last stage is also available for simpler decoding applications.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7491A | 18MHz | 3.5mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7491AN |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| All | Inputs | 1ul |
| All | Outputs | 10ul |

**NOTE:**
A 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$.

## PIN CONFIGURATION



CD05710S

## LOGIC SYMBOL



LS05750S

$V_{CC}$ = Pin 5
GND = Pin 10
Pin numbers for DIP package

## LOGIC SYMBOL (IEEE/IEC)



LS05760S

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# 7491A

## LOGIC DIAGRAM



```
DIP          Flat Pack
Vcc = Pin 5   Vcc = Pin 4
GND = Pin 10  GND = Pin 11
```
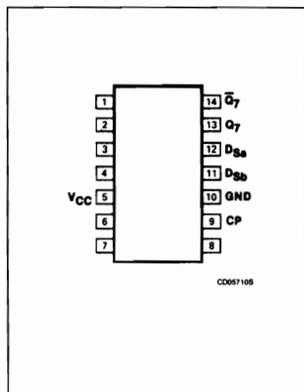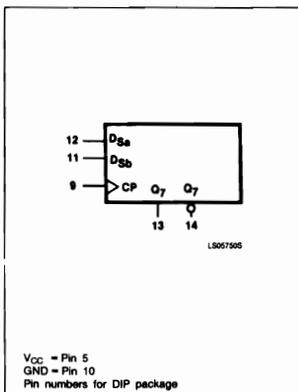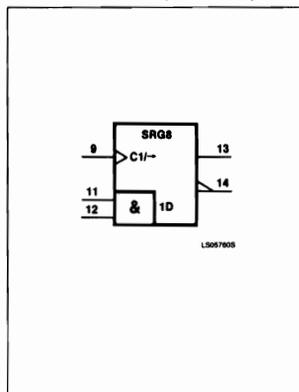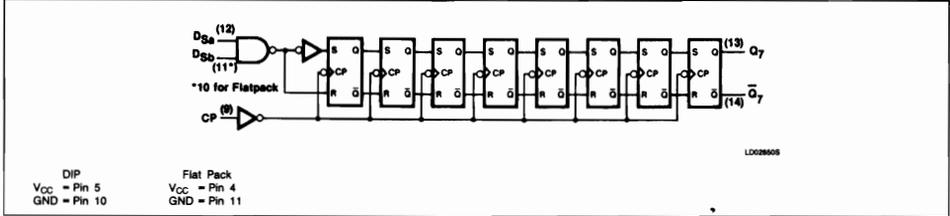
## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | FIRST STAGE | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| | CP | $D_{Sa}$ | $D_{Sb}$ | $Q_0$ | $\bar{Q}_0$ | $Q_7$ | $\bar{Q}_7$ |
| Shift, reset first stage | ↑ | l | X | L | H | $q_6$ | $\bar{q}_6$ |
| | ↑ | X | l | L | H | $q_6$ | $\bar{q}_6$ |
| Shift, set first stage | ↑ | h | h | H | L | $q_6$ | $\bar{q}_6$ |

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$q_n$ = Lower case letters indicate the state of the referenced register output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | | | 2.0 | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | µA |
| $I_{OL}$ | LOW-level output current | | | 16 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

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# 7492, LS92
## Counters

**Divide-By-Twelve Counter**
*Product Specification*

## DESCRIPTION

The '92 is a 4-bit, ripple-type Divide-by-12 Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-six section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT |
|------|------|------|
| 7492 | 28MHz | 28mA |
| 74LS92 | 42MHz | 9mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|------|------|
| Plastic DIP | N7492N, N74LS92N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|------|------|------|------|
| MR | Master reset inputs | 1ul | 1LSul |
| $CP_0$ | Input | 2ul | 6LSul |
| $CP_1$ | Input | 4ul | 8LSul |
| $Q_0 - Q_3$ | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and − 1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 5
GND = Pin 10
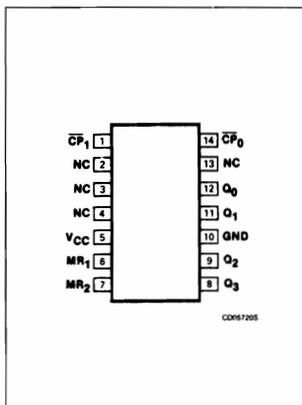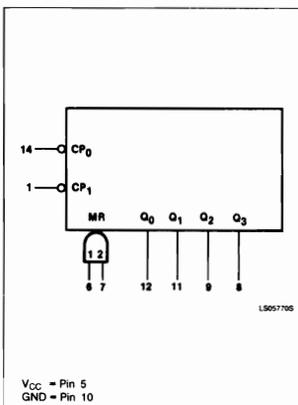
## LOGIC SYMBOL (IEEE/IEC)
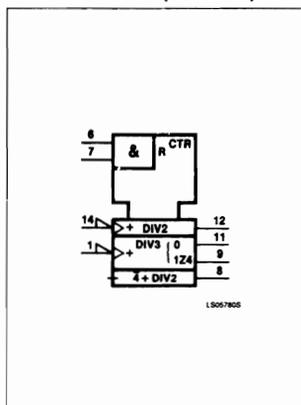
## LOGIC DIAGRAM
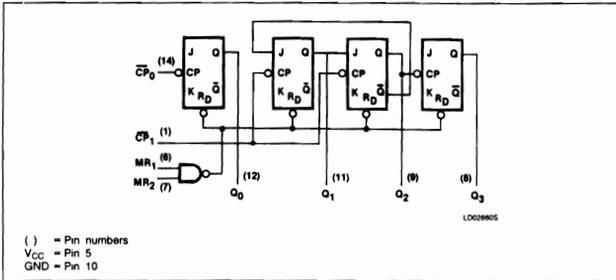


Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a Modulo-12, Divide-by-12 Counter the $\overline{CP}_1$ input must be externally connected to the $Q_0$ output. The $\overline{CP}_0$ input receives the incoming count and $Q_3$ produces a symmetrical divide-by-12 square wave output. In a divide-by-six counter no external connections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the $Q_1$ and $Q_2$ outputs and divide-by-six operation at the $Q_3$ output.

( ) = Pin numbers
$V_{CC}$ = Pin 5
GND = Pin 10

## FUNCTION TABLE

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | L | L | H |
| 7 | H | L | L | H |
| 8 | L | H | L | H |
| 9 | H | H | L | H |
| 10 | L | L | H | H |
| 11 | H | L | H | H |

**NOTE:**
Output $Q_0$ connected to input $\overline{CP}_1$.

## MODE SELECTION

| RESET INPUTS | | OUTPUTS | | | |
|---|---|---|---|---|---|
| $MR_1$ | $MR_2$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| H | H | L | L | L | L |
| L | H | Count | | | |
| H | L | Count | | | |
| L | L | Count | | | |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

**NOTE:**
$V_{IN}$ is limited to 5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs only on the 74LS92.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 7493, LS93
## Counters

**4-Bit Binary Ripple Counter**
*Product Specification*

**Logic Products**

## DESCRIPTION
The '93 is a 4-bit, ripple-type Binary Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output $Q_0$ must be connected externally to input $\overline{CP}_1$.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|------|------|
| 7493 | 40MHz | 28mA |
| 74LS93 | 42MHz | 9mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|------|------|
| Plastic DIP | N7493N, N74LS93N |
| Plastic SO | N74LS93D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|------|------|------|------|
| MR | Master reset inputs | 1ul | 1LSul |
| $\overline{CP}_0$ | Input | 2ul | 6LSul |
| $\overline{CP}_1$ | Input | 2ul | 4LSul |
| $Q_0 - Q_3$ | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and – 1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



54

## LOGIC DIAGRAM



( ) = Pin number
$V_{CC}$ = Pin 5
GND = Pin 10

The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the $Q_0$, $Q_1$, $Q_2$ and $Q_3$ outputs as shown in the Function Table.

As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the $Q_1$, $Q_2$ and $Q_3$ outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

## FUNCTION TABLE

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |
| 10 | L | H | L | H |
| 11 | H | H | L | H |
| 12 | L | L | H | H |
| 13 | H | L | H | H |
| 14 | L | H | H | H |
| 15 | H | H | H | H |

## MODE SELECTION

| RESET INPUTS | | OUTPUTS | | | |
|---|---|---|---|---|---|
| $MR_1$ | $MR_2$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| H | H | L | L | L | L |
| L | H | Count | | | |
| H | L | Count | | | |
| L | L | Count | | | |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

**NOTE:**
Output $Q_0$ connected to input $\overline{CP}_1$.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | | | −400 | µA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 7494
# Shift Register

### 4-Bit Shift Register
*Product Specification*

**Logic Products**

## FEATURES
- 4-bit parallel-to-serial converter
- Two asynchronous ones transfer parallel data ports
- Buffered active HIGH Master Reset
- Buffered positive edge-triggered clock

## DESCRIPTION
The '94 is a 4-bit shift register with serial and parallel (ones transfer) data entry. To facilitate parallel ones transfer from two sources, two Parallel Load inputs ($PL_0$ and $PL_1$) with associated Parallel Data inputs ($D_{0a} - D_{0d}$ and $D_{1a} - D_{1d}$) are provided. To accommodate these extra inputs only the output of the last stage is available. The asynchronous Master Reset (MR) is active HIGH. When MR is HIGH, it overrides the clock and clears the register, forcing $Q_d$ LOW.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT |
|---|---|---|
| 7494 | 25ns | 35mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7494N |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| $PL_0$, $PL_1$ | Parallel load inputs | 4ul |
| $D_S$, $D_n$, CP, MR | All other inputs | 1ul |
| $Q_d$ | Serial Data output | 10ul |

NOTE:
Where a 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



56

## LOGIC DIAGRAM



```
( )  = Pin number
Vcc  = Pin 5
GND  = Pin 12
```
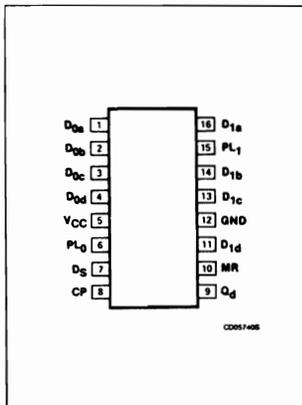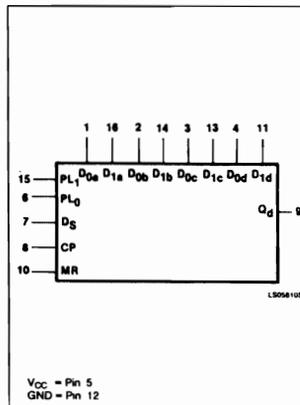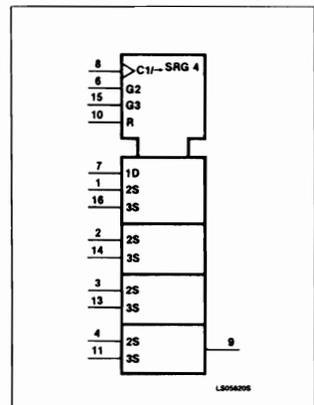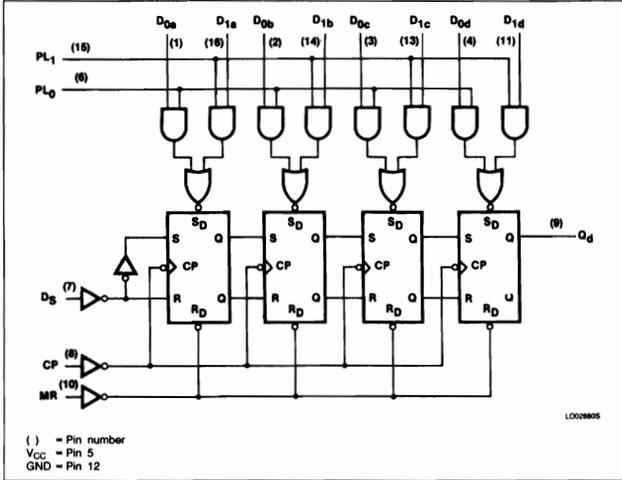
Four flip-flops are connected so that shifting is synchronous; they change state when the clock goes from LOW-to-HIGH. Data is accepted at the serial $D_S$ input prior to this clock transition. Two Parallel Load inputs and Parallel Data inputs allow an asynchronous ones transfer from two sources. The flip-flops can be set independently to the HIGH state when the appropriate Parallel input is activated. Parallel inputs $D_{0a}$ through $D_{0d}$ are activated during the time the $PL_0$ is HIGH and Parallel inputs $D_{1a}$ through $D_{1d}$ are activated when $PL_1$ is HIGH. If both sets of inputs are activated, a HIGH on either input will set the flip-flops to a HIGH. The register should not be clocked while the Parallel Load inputs are activated. The Parallel Load and Parallel Data inputs will override the MR if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $PL_0$ | $PL_1$ | $D_{0n}$ | $D_{1n}$ | MR | CP | $D_S$ | $Q_a$ | $Q_b$ | $Q_c$ | $Q_d$ |
| Parallel load | H | L | L | X | X | X | X | $Q_a$ | $Q_b$ | $Q_c$ | $Q_d$ |
| | H | L | H | X | X | X | X | H | H | H | H |
| | L | H | X | L | X | X | X | $Q_a$ | $Q_b$ | $Q_c$ | $Q_d$ |
| | L | H | X | H | X | X | X | H | H | H | H |
| Reset (clear) | L | L | X | X | H | X | X | L | L | L | L |
| Shift right | L | L | X | X | L | ↑ | l | L | $q_a$ | $q_b$ | $q_c$ |
| | L | L | X | X | L | ↑ | h | H | $q_a$ | $q_b$ | $q_c$ |

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$q_n$ = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

# 7495, LS95B
## Shift Registers

**4-Bit Shift Register**
*Product Specification*

**Logic Products**

## FEATURES
- Separate negative-edge-triggered shift and parallel load clocks
- Common mode control input
- Shift right serial input
- Synchronous shift or load capabilities

## DESCRIPTION
The '95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has serial Data ($D_S$) and four parallel Data ($D_0 - D_3$) inputs and four Parallel outputs ($Q_0 - Q_3$). The serial or parallel mode of operation is controlled by a Mode Select input (S) and two Clock inputs ($\overline{CP}_1$ and $\overline{CP}_2$). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected Clock input.

When the Mode Select input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_2$ loads parallel data from the $D_0 - D_3$ inputs into the register. When S is LOW, $CP_1$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_1$ shifts the data from Serial input $D_S$ to $Q_0$ and transfers the data in $Q_0$ to $Q_1$, $Q_1$ to $Q_2$, and $Q_2$ to $Q_3$

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7495 | 36MHz | 39mA |
| 74LS95B | 36MHz | 13mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7495N, N74LS95BN |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| S | Input | 2ul | 1LSul |
| Other | Inputs | 1ul | 1LSul |
| Q | Output | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

respectively (shift right). Shift left is accomplished by externally connecting $Q_3$ to $D_2$, $Q_2$ to $D_1$, $Q_1$ to $D_0$, and operating the '95 in the parallel mode (S = HIGH).

In normal operations the Mode Select (S) should change states only when both Clock inputs are LOW. However, changing S from HIGH-to-LOW while $\overline{CP}_2$ is LOW, or changing S from LOW-to-HIGH while $\overline{CP}_1$ is LOW will not cause any changes on the register outputs.

## PIN CONFIGURATION
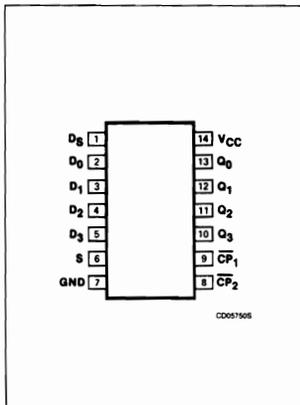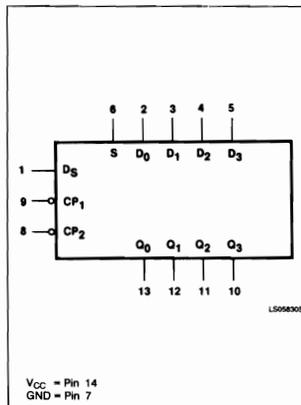


| | |
|---|---|
| $D_S$ 1 | 14 $V_{CC}$ |
| $D_0$ 2 | 13 $Q_0$ |
| $D_1$ 3 | 12 $Q_1$ |
| $D_2$ 4 | 11 $Q_2$ |
| $D_3$ 5 | 10 $Q_3$ |
| S 6 | 9 $\overline{CP}_1$ |
| GND 7 | 8 $\overline{CP}_2$ |

CD05750S

## LOGIC SYMBOL



$V_{CC}$ = Pin 14
GND = Pin 7

LS05830S

## LOGIC SYMBOL (IEEE/IEC)



LS05840S

58

# Shift Registers

## LOGIC DIAGRAM



```
( )  = Pin numbers
Vcc  = Pin 14
GND = Pin 7
```
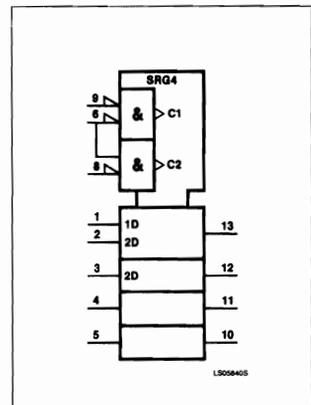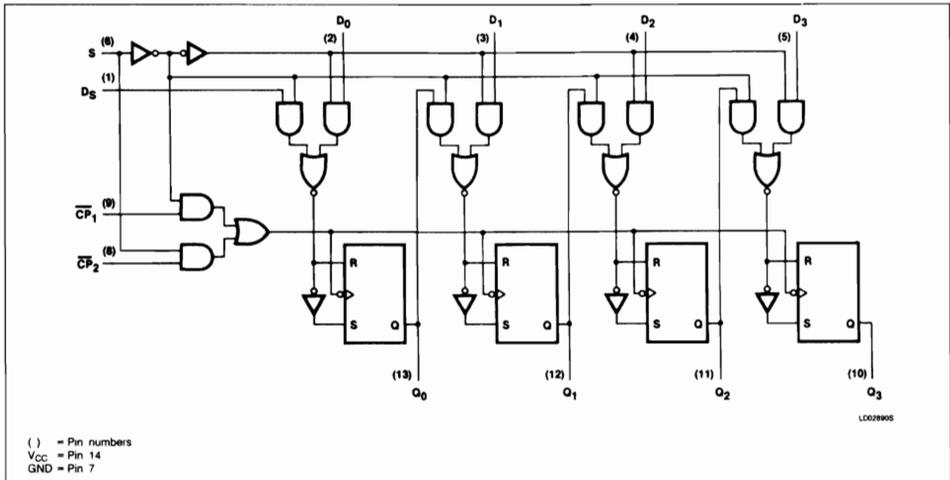
## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|
| | S | CP$_1$ | CP$_2$ | D$_S$ | D$_N$ | Q$_0$ | Q$_1$ | Q$_2$ | Q$_3$ |
| Parallel load | H | X | ↓ | X | l | L | L | L | L |
| | H | X | ↓ | X | h | H | H | H | H |
| Shift right | L | ↓ | X | l | X | L | q$_0$ | q$_1$ | q$_2$ |
| | L | ↓ | X | h | X | H | q$_0$ | q$_1$ | q$_2$ |
| Mode change | ↑ | L | X | X | X | no change | | | |
| | ↑ | H | X | X | X | undetermined | | | |
| | ↓ | X | L | X | X | no change | | | |
| | ↓ | X | H | X | X | undetermined | | | |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition.
q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW clock transition.
X = Don't care.
↓ = HIGH-to-LOW transition of clock or mode select.
↑ = LOW-to-HIGH transition of mode select.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| V$_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| V$_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| I$_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| V$_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +V$_{CC}$ | +0.5 to +V$_{CC}$ | V |
| T$_A$ | Operating free-air temperature range | 0 to 70 | | °C |

# 7496, LS96
## Shift Registers

### 5-Bit Shift Register
*Product Specification*

**Logic Products**

## FEATURES
- 5-bit parallel-to-serial or serial-to-parallel converter
- Asynchronous ones transfer preset entry
- Buffered positive-triggered clock
- Buffered active LOW Clear (Master Reset)

## DESCRIPTION
The '96 is a 5-bit shift register with both serial and parallel (ones transfer) data entry. Since the '96 has the output of each stage available as well as a D-type serial input and ones transfer inputs on each stage, it can be used in 5-bit serial-to-parallel, serial-to-serial and some parallel-to-serial data operations.

The '96 is five master/slave flip-flops connected to perform right shift. The flip-flops change state on the LOW-to-HIGH transition of the clock. The Serial (S) input is edge-triggered and must be stable only one set-up time before the LOW-to-HIGH clock transition.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 7496 | 25ns | 48mA |
| 74LS96 | 25ns | 12mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N7496N, N74LS96N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Mamual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| Preset enable | Inputs | 5ul | 5LSul |
| All other | Inputs | 1ul | 1LSul |
| Q | Outputs | 10ul | 10LSul |

**NOTE:**
A 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



CP [1] ... [16] MR
PRESET A [2] ... [15] $Q_A$
PRESET B [3] ... [14] $Q_B$
PRESET C [4] ... [13] $Q_C$
$V_{CC}$ [5] ... [12] GND
PRESET D [6] ... [11] $Q_D$
PRESET E [7] ... [10] $Q_E$
PE [8] ... [9] S

CD05760S

## LOGIC SYMBOL



$V_{CC}$ = Pin 5
GND = Pin 12

LS05850S

## LOGIC SYMBOL (IEEE/IEC)



LS05860S

60

## LOGIC DIAGRAM



( )  = Pin number
$V_{CC}$ = Pin 5
GND = Pin 12
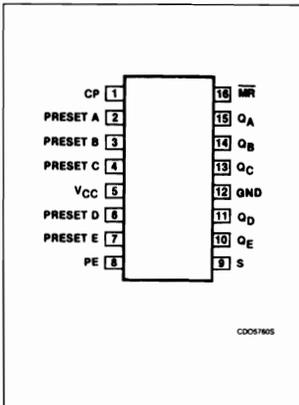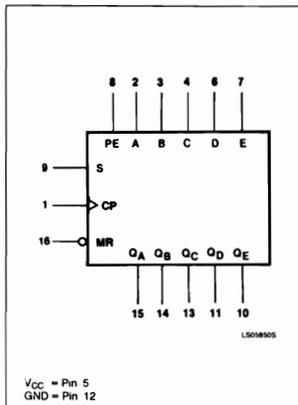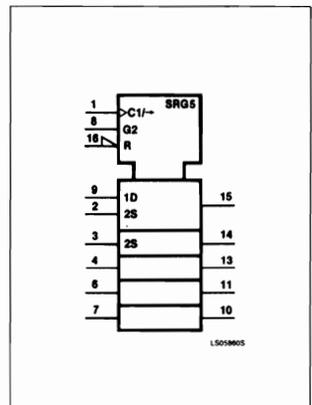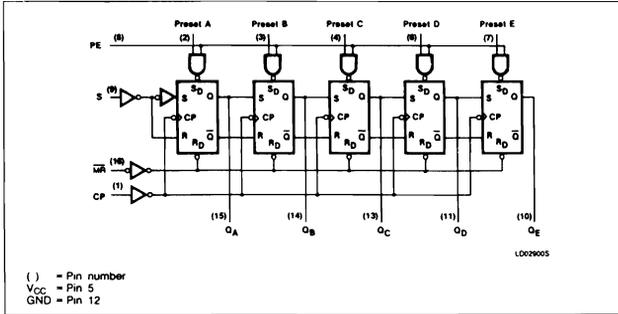
Each flip-flop has asynchronous set inputs, allowing them to be independently set HIGH. The set inputs are controlled by a common active HIGH Preset Enable (PE) input. The PE input is not buffered, and care must be taken not to overload the driving element. When the PE is HIGH, a HIGH on the Preset (A – E) inputs will set the associated flip-flops HIGH. A LOW on the A – E inputs will cause "no change" in the appropriate flip-flops.

The asynchronous active LOW Clear ($\overline{MR}$) is buffered. When LOW, the $\overline{MR}$ overrides the clock and clears the register if the PE is not active. The Preset inputs override the $\overline{MR}$, forcing the flip-flops HIGH if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

## FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Master Reset | Preset Enable | Preset | | | | | Clock | Serial | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ |
| | | A | B | C | D | E | | | | | | | |
| L | L | X | X | X | X | X | X | X | L | L | L | L | L |
| L | X | L | L | L | L | L | X | X | L | L | L | L | L |
| H | H | H | H | H | H | H | X | X | H | H | H | H | H |
| H | H | L | L | L | L | L | L | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ |
| H | H | H | L | H | L | H | L | X | H | $Q_{B0}$ | H | $Q_{D0}$ | H |
| H | L | X | X | X | X | X | L | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ | $Q_{E0}$ |
| H | L | X | X | X | X | X | ↑ | H | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ |
| H | L | X | X | X | X | X | ↑ | L | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ |

H  = HIGH voltage level, (steady state)
L  = LOW voltage level (steady state)
X  = Irrelevant (any input, including transitions)
↑  = Transition from LOW-to-HIGH level
$Q_{A0}$, $Q_{B0}$, etc  = The level of $Q_A$, $Q_B$, etc, respectively before the indicated steady-state input conditions were established.
$Q_{An}$, $Q_{Bn}$, etc  = The level of $Q_A$, $Q_B$, etc, respectively before the most recent ↑ transition of the clock.
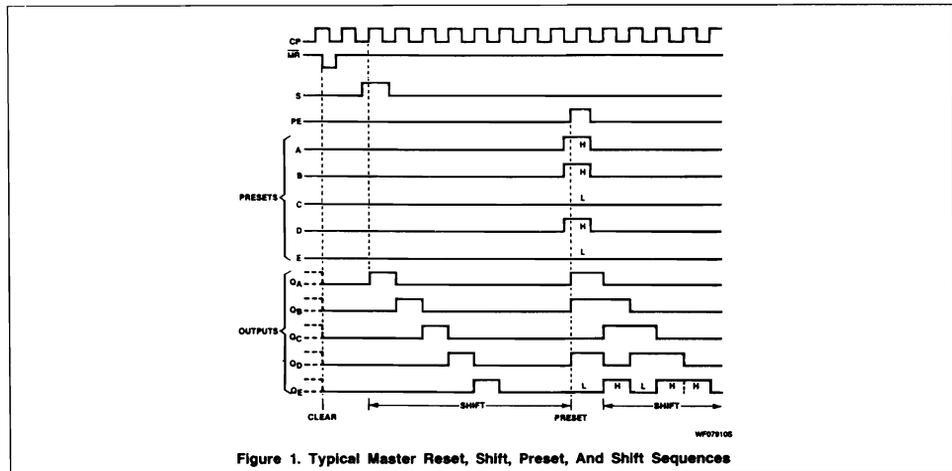


**Figure 1. Typical Master Reset, Shift, Preset, And Shift Sequences**

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# 74107, LS107
## Flip-Flops

### Dual J-K Flip-Flop
*Product Specification*

**Logic Products**

## DESCRIPTION

The '107 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 74107 is a positive pulse-triggered flip-flop. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. For these devices the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS107 is a negative edge-triggered flip-flop. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset ($\overline{R}_D$) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74107 | 20MHz | 20mA |
| 74LS107 | 45MHz | 4mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74107N, N74LS107N |
| Plastic SO | N74LS107D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| $\overline{CP}$ | Clock input | 2ul | 4LSul |
| $\overline{R}_D$ | Reset input | 2ul | 3LSul |
| J, K | Data inputs | 1ul | 1LSul |
| Q, $\overline{Q}$ | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



LD02910S

## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\overline{R}_D$ | $\overline{CP}$[2] | J | K | Q | $\overline{Q}$ |
| Asynchronous Reset (Clear) | L | X | X | X | L | H |
| Toggle | H | ⊓ | h | h | $\overline{q}$ | q |
| Load "0" (Reset) | H | ⊓ | l | h | L | H |
| Load "1" (Set) | H | ⊓ | h | l | H | L |
| Hold "no change" | H | ⊓ | l | l | q | $\overline{q}$ |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.[2]
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.[2]
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
X = Don't care.
⊓ = Positive Clock pulse.

**NOTES:**
1. The J and K inputs of the 74107 must be stable while the Clock is HIGH for conventional operation.
2. The 74LS107 is edge-triggered. Data must be stable one set-up time prior to the negative edge of the Clock for predictable operation.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 74109, LS109A
## Flip-Flops

**Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop**
*Product Specification*

**Logic Products**

## DESCRIPTION
The '109 is dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active LOW inputs and operate independently of the Clock input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table.

The J and $\overline{K}$ inputs must be stable just one set-up time prior to the LOW-to-HIGH transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74109 | 33MHz | 9mA |
| 74LS109A | 33MHz | 4mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74109N, N74LS109AN |
| Plastic SO | N74LS109D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| CP | Clock input | 2ul | 1LSul |
| $\overline{R}_D$ | Reset input | 4ul | 2LSul |
| $\overline{S}_D$ | Set input | 2ul | 2LSul |
| J, $\overline{K}$ | Data inputs | 1ul | 1LSul |
| Q, $\overline{Q}$ | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and –1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



LD02920S

## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| | $\overline{S}_D$ | $\overline{R}_D$ | CP | J | $\overline{K}$ | Q | $\overline{Q}$ |
| Asynchronous set | L | H | X | X | X | H | L |
| Asynchronous reset (clear) | H | L | X | X | X | L | H |
| Undetermined (note) | L | L | X | X | X | H | H |
| Toggle | H | H | ↑ | h | l | $\overline{q}$ | q |
| Load "0" (reset) | H | H | ↑ | l | l | L | H |
| Load "1" (set) | H | H | ↑ | h | h | H | L |
| Hold "no change" | H | H | ↑ | l | h | q | $\overline{q}$ |

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition.
↑ = LOW-to-HIGH Clock transition.

**NOTE:**
Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 74LS112, S112
## Flip-Flops

**Dual J-K Edge-Triggered Flip-Flop**
*Product Specification*

## DESCRIPTION
The '112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS112 | 45MHz | 4mA |
| 74S112 | 125MHz | 15mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74S112N, N74LS112N |
| Plastic SO | N74LS112D, N74S112D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|---|---|---|---|
| $\overline{CP}$ | Clock input | 2Sul | 4LSul |
| $\overline{R}_D$, $\overline{S}_D$ | Reset and set inputs | 3.5Sul | 3LSul |
| J, K | Data inputs | 1Sul | 1LSul |
| Q, $\overline{Q}$ | Outputs | 10Sul | 10LSul |

**NOTE:**
A 74 unit load (ul) is $50\mu A$ $I_{IH}$ and $-2.0mA$ $I_{IL}$, and a 74LS unit load (LSul) is $20\mu A$ $I_{IH}$ and $-0.4mA$ $I_{IL}$.

## PIN CONFIGURATION

## LOGIC SYMBOL

## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



LD01830S
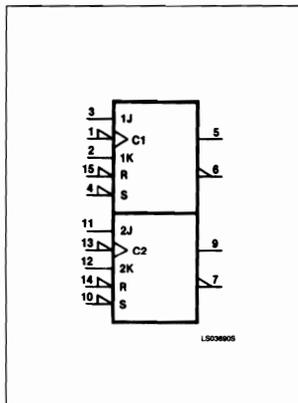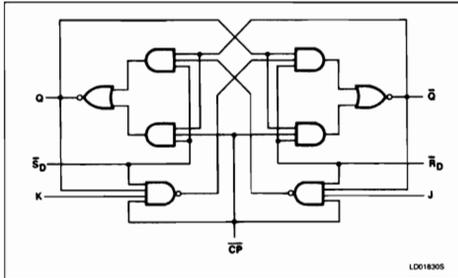
## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| | $\overline{S}_D$ | $\overline{R}_D$ | $\overline{CP}$ | J | K | Q | $\overline{Q}$ |
| Asynchronous set | L | H | X | X | X | H | L |
| Asynchronous reset (clear) | H | L | X | X | X | L | H |
| Undetermined | L | L | X | X | X | H | H |
| Toggle | H | H | ↓ | h | h | $\overline{q}$ | q |
| Load "0" (reset) | H | H | ↓ | l | h | L | H |
| Load "1" (set) | H | H | ↓ | h | l | H | L |
| Hold "no change" | H | H | ↓ | l | l | q | $\overline{q}$ |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
↓ = HIGH-to-LOW Clock transition.
NOTE:
Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74LS | 74S | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to −7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −1000 | μA |
| $I_{OL}$ | LOW-level output current | | | 8 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 74LS113, S113
## Flip-Flops

**Dual J-K Edge-Triggered Flip-Flop**
*Product Specification*

## DESCRIPTION

The '113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set ($\overline{S}_D$) input, when LOW, forces the outputs to the steady state levels as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum set-up and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS113 | 45MHz | 4mA |
| 74S113 | 125MHz | 15mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74S113N, N74LS113N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|---|---|---|---|
| $\overline{CP}$ | Clock input | 2Sul | 4LSul |
| $\overline{S}_D$ | Set inputs | 3.5Sul | 3LSul |
| J, K | Data inputs | 1Sul | 1LSul |
| Q, $\overline{Q}$ | Outputs | 10Sul | 10LSul |

**NOTE:**
A 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION

## LOGIC SYMBOL

## LOGIC SYMBOL (IEEE/IEC)



68
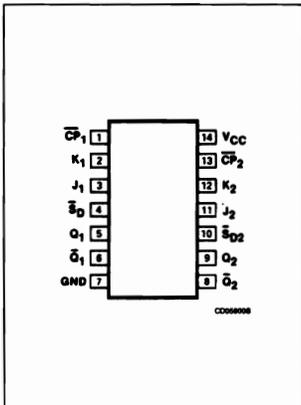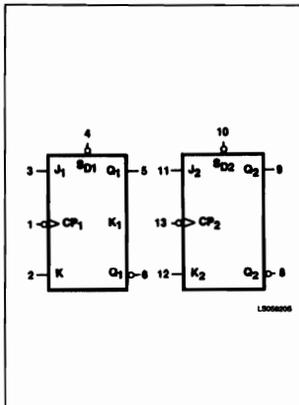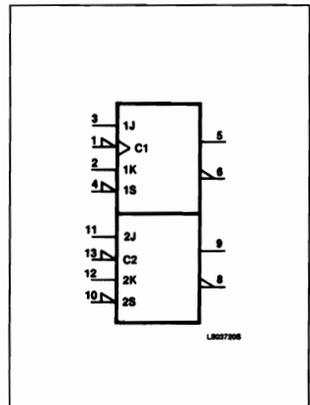
## LOGIC DIAGRAM
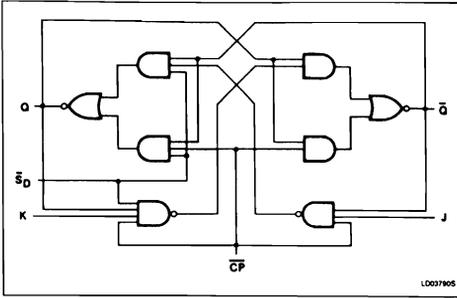


## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| | $\overline{S}_D$ | $\overline{CP}$ | J | K | Q | $\overline{Q}$ |
| Asynchronous set | L | X | X | X | H | L |
| Toggle | H | ↓ | h | h | $\overline{q}$ | q |
| Load "0" (reset) | H | ↓ | l | h | L | H |
| Load "1" (set) | H | ↓ | h | l | H | L |
| Hold "no change" | H | ↓ | l | l | q | $\overline{q}$ |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one set-up time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
↓ = HIGH-to-LOW Clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74LS | 74S | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to −7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −1000 | μA |
| $I_{OL}$ | LOW-level output current | | | 8 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 74116
## Latch

**Dual 4-Bit Transparent Latch**
*Product Specification*

## DESCRIPTION

The '116 has two independent 4-bit transparent latches. Each 4-bit latch is controlled by a two-input active LOW Enable gate ($\overline{E}_0$ and $\overline{E}_1$). When both $\overline{E}_0$ and $\overline{E}_1$ are LOW, the data enters the latch and appears at the output. The outputs follow the Data inputs as long as $\overline{E}_0$ and $\overline{E}_1$ are LOW. The data on the D inputs one set-up time before the LOW-to-HIGH transition of $\overline{E}_0$ or $\overline{E}_1$ will be stored in the latch. The Latched outputs remain stable as long as either $\overline{E}_0$ or $\overline{E}_1$ is HIGH.

Each 4-bit latch has an active LOW asynchronous Master Reset ($\overline{MR}$) input. When LOW, the $\overline{MR}$ input overrides the Data and Enable inputs and sets the four Latch outputs LOW.

| TYPE | TYPICAL PROPAGATION DELAY—DATA TO OUTPUT | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74116 | 11ns | 50mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74116N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| $\overline{E}_0$, $\overline{E}_1$ | Enable inputs | 1ul |
| $D_0 – D_3$ | Data inputs | 1.5ul |
| $\overline{MR}$ | Master reset input | 1ul |
| $Q_0 – Q_3$ | Latch outputs | 10ul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$.

## PIN CONFIGURATION
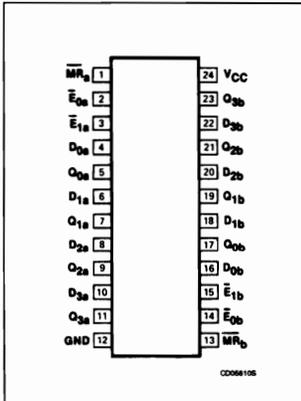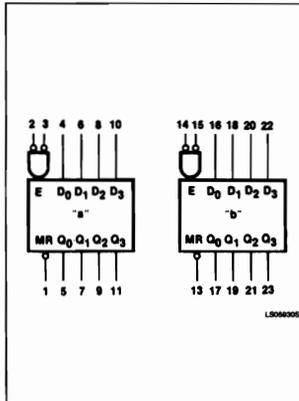


## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)
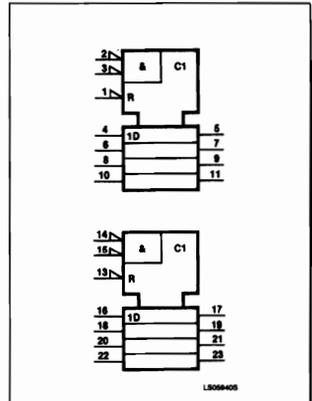
# 74121
# Multivibrator

**Monostable Multivibrator**
*Product Specification*

## FEATURES
- Very good pulse width stability
- Virtually immune to temperature and voltage variations
- Schmitt trigger input for slow input transitions
- Internal timing resistor provided

## DESCRIPTION
These multivibrators feature dual active LOW going edge inputs and a single active HIGH going edge input which can be used as an active HIGH enable input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to $V_{CC}$ noise of typically 1.5 volts is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the inputs and are a function only of the

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74121 | 43ns | 18mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74121 N |
| Plastic SO | N74121 D |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 20 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., $R_{int}$ connected to $V_{CC}$, $C_{ext}$ and $R_{ext}/C_{ext}$ open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of $V_{CC}$ and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and $V_{CC}$ ranges for more than six decades of timing capacitance (10pF to 10$\mu$F) and more than one decade of timing resistance (2k$\Omega$ to 30k$\Omega$ for the 54121 and 2K$\Omega$ to 40k$\Omega$ for the 74121). Throughout these ranges, pulse width is defined by the relationship: (see Figure 1)

$$t_W(out) = C_{ext} R_{ext} \ln 2$$
$$t_W(out) \cong 0.7 C_{ext} R_{ext}$$

## PIN CONFIGURATION



CD05820S

## LOGIC SYMBOL



LS05950S

## LOGIC SYMBOL (IEEE/IEC)



LS05960S

71
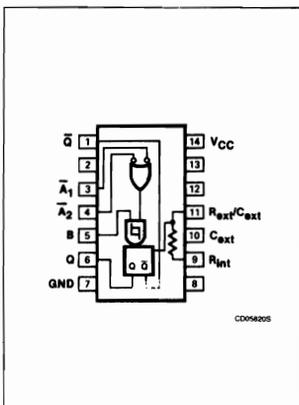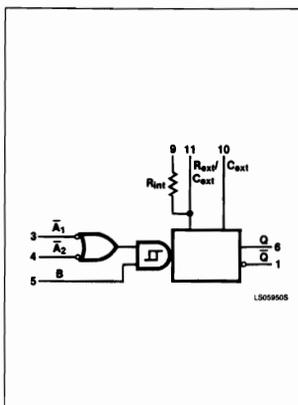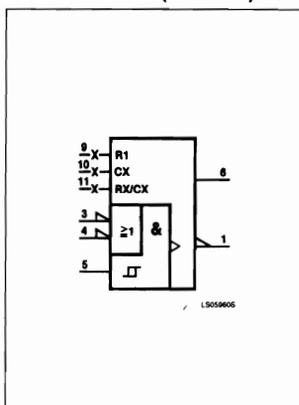
## FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|--------|--------|--------|--------|--------|
| $\overline{A}_1$ | $\overline{A}_2$ | B | Q | $\overline{Q}$ |
| L | X | H | L | H |
| X | L | H | L | H |
| X | X | L | L | H |
| H | H | X | L | H |
| H | ↓ | H | ⎍ | ⎍ |
| ↓ | H | H | ⎍ | ⎍ |
| ↓ | ↓ | H | ⎍ | ⎍ |
| L | X | ↑ | ⎍ | ⎍ |
| X | L | ↑ | ⎍ | ⎍ |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|-------------|-----|
| $\overline{A}_1$, $\overline{A}_2$ | Inputs | 1ul |
| B | Input | 2ul |
| Q, $\overline{Q}$ | Outputs | 10ul |

NOTE:
A 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$.

In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4kΩ may be used.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | UNIT |
|--|-----------|-----|------|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | | 74 | | | UNIT |
|--|-----------|--|-----|-----|-----|------|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | | 4.75 | 5.0 | 5.25 | V |
| $I_{IK}$ | Input clamp current | | | | −12 | mA |
| $I_{OH}$ | HIGH-level output current | | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | | 16 | mA |
| dv/dt | Rate of rise or fall of input pulse | B input | 1 | | | V/s |
| | | $\overline{A}_1$, $\overline{A}_2$ inputs | 1 | | | V/μs |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

# 74123
## Multivibrator

**Dual Retriggerable Monostable Multivibrator**
*Product Specification*

## FEATURES
- **DC triggered from active HIGH or active LOW inputs**
- **Retriggerable for very long pulses — up to 100% duty cycle**
- **Direct reset terminates output pulse**
- **Compensated for $V_{CC}$ and temperature variations**

## DESCRIPTION
The '123 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance ($R_{ext}$) and capacitance ($C_{ext}$) values. Once triggered, the basic pulse width may be extended by retriggering the gated active LOW going edge input ($\overline{A}$) or the active HIGH going edge input (B), or be reduced by use of the overriding active LOW reset.

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 74123 | 24ns | 46mA |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|---------------------------------------------------------------|
| Plastic DIP | N74123N |
| Plastic SO | N74123D |

For pulse widths when $C_{ext} \leqslant 1000pF$, see Figure A.

When $C_{ext} > 1000pF$, the output pulse width is defined as:

$$t_W = 0.28\ R_{ext} \cdot C_{ext} \left(1 + \frac{0.7}{R_{ext}}\right)$$

The external resistance and capacitance are normally connected as shown in Figure B. If an electrolytic capacitor is to be used with an inverse voltage rating of less than 1V then Figure C should be used. (Inverse voltage rating of an electrolytic is normally specified at 5% of the forward voltage rating.) If the inverse voltage rating is 1V or more (this includes a 100% safety margin) then Figure B can be used. Note that if Figure C is used the timing equations change as follows:

$$t_W \cong 0.25\ R_{ext} \cdot C_{ext} \left(1 + \frac{0.7}{R_{ext}}\right)$$

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



73
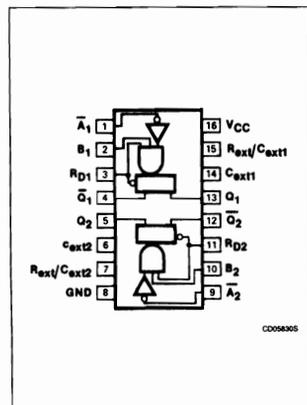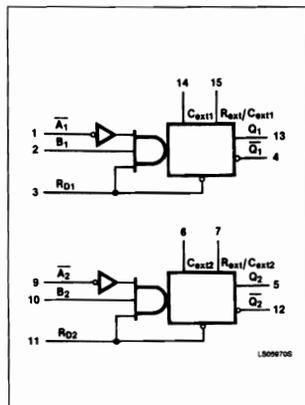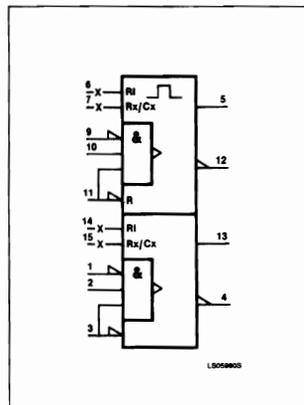
# Multivibrator

# 74123

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $R_D$ | $\overline{A}$ | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↑ | ⊓ | ⊔ |
| H | ↓ | H | ⊓ | ⊔ |
| ↑ | L | H | ⊓ | ⊔ |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⊓ = One HIGH-level pulse
⊔ = One LOW-level pulse

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| $\overline{A}$, B | Inputs | 1ul |
| $R_D$ | Input | 2ul |
| Q, $\overline{Q}$ | Outputs | 10ul |

NOTE:
A 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and −1.6mA $I_{IL}$.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| $I_{IK}$ | Input clamp current | | | −12 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | $\mu$A |
| $I_{OL}$ | LOW-level output current | | | 16 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | V |

## TYPICAL PERFORMANCE CHARACTERISTICS
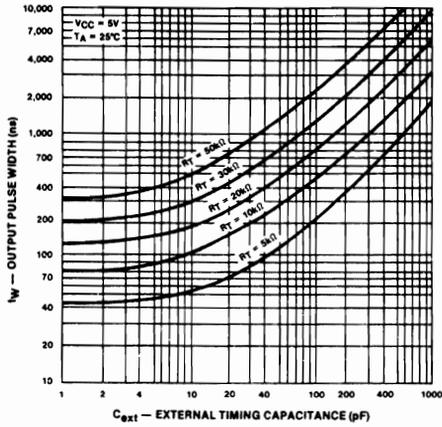


Figure A
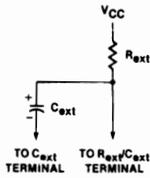


Figure B
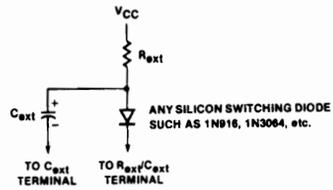


Figure C

# 74125, 74126, LS125A, LS126A
# Buffers

**Quad 3-State Buffer**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74125 | 10ns | 32mA |
| 74LS125A | 8ns | 11mA |
| 74126 | 10ns | 36mA |
| 74LS126A | 9ns | 12mA |

## FUNCTION TABLE '125, 'LS125A

| INPUTS | | OUTPUT |
|---|---|---|
| C | A | Y |
| L | L | L |
| L | H | H |
| H | X | (Z) |

## FUNCTION TABLE '126, 'LS126A

| INPUTS | | OUTPUT |
|---|---|---|
| C | A | Y |
| H | L | L |
| H | H | H |
| L | X | (Z) |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off)

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74125N, N74LS125N N74126N, N74LS126N |
| Plastic SO | N74LS125AD |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| All | Inputs | 1ul | 1LSul |
| All | Outputs | 10ul | 30LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION

'125
'LS125A



## LOGIC SYMBOL

'125
'LS125A



## LOGIC SYMBOL (IEEE/IEC)

'125
'LS125A
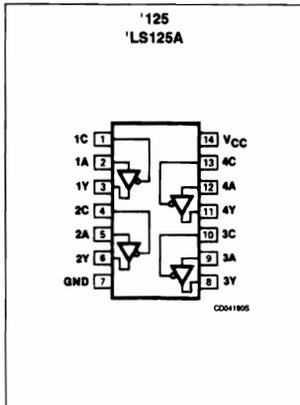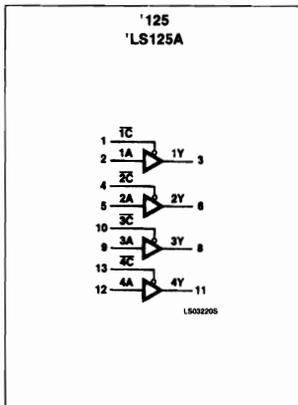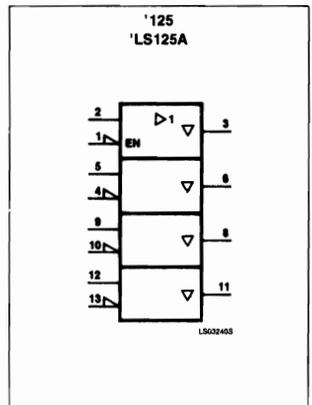
# 74125, 74126, LS125A, LS126A

## PIN CONFIGURATION

'126
'LS126A



CD04206S

## LOGIC SYMBOL

'126
'LS126A



LS03230S

## LOGIC SYMBOL (IEEE/IEC)

'126
'LS126A



LS03650S

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ • | Operating free-air temperature range | | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −5.2 | | | −2.6 | mA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

77

# 74128
## Buffer

**Quad Two-Input NOR Buffer**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|-------------------------------|
| 74128 | 7ns | 23mA |

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|--------|--------|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|------------------------------------------------------------------|
| Plastic DIP | N74128N |

**NOTES:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|-------------|-----|
| A, B | Inputs | 1ul |
| Y | Output | 30ul |

**NOTE:**
Where a 74 unit load is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



78
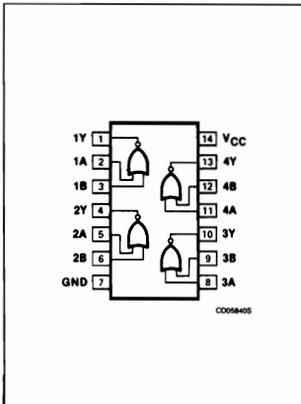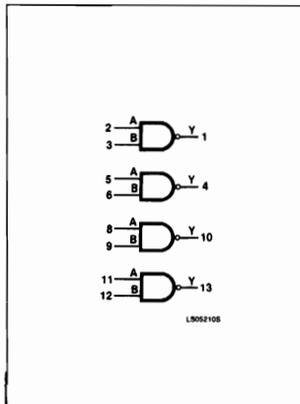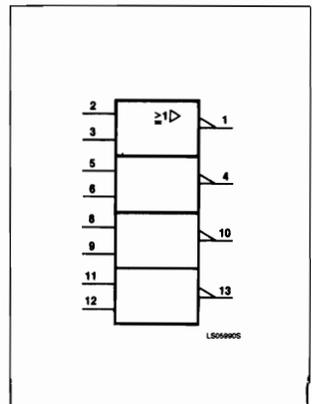
# 74132, LS132
## Schmitt Triggers

**Quad 2-Input NAND Schmitt Trigger**
*Product Specification*

**Logic Products**

The '132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mW) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than $V_{T + MAX}$, the gate will respond to the transitions of the other input as shown in Waveform 1.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74132 | 15ns | 21mA |
| 74LS132 | 15ns | 7mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74132N, N74LS132N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| A, B | Inputs | 1ul | 1LSul |
| Y | Output | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## PIN CONFIGURATION



CD04600S

## LOGIC SYMBOL



LS03780S

## LOGIC SYMBOL (IEEE/IEC



LS037705

79
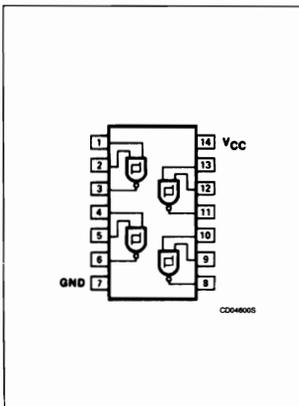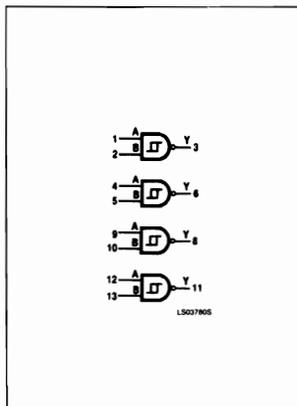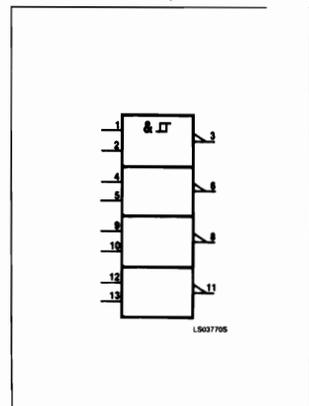
## 74S133
## Gate

**13-Input NAND Gate**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74S133 | 4ns | 4mA |

### FUNCTION TABLE

| INPUTS | OUTPUT |
|---|---|
| A … M | $\overline{Y}$ |
| H … H | L |
| one input = L | H |

H = HIGH voltage level
L = LOW voltage level

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74S133N |
| Plastic SO | N74S133D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S |
|---|---|---|
| All | Inputs | 1Sul |
| $\overline{Y}$ | Output | 10Sul |

**NOTE:**
A 74S unit load (Sul) is understood to be 50µA $I_{IH}$ and −2.0mA $I_{IL}$.

### PIN CONFIGURATION



CD05850S

### LOGIC SYMBOL



LS06000S

### LOGIC SYMBOL (IEEE/IEC)



LS06010S

80
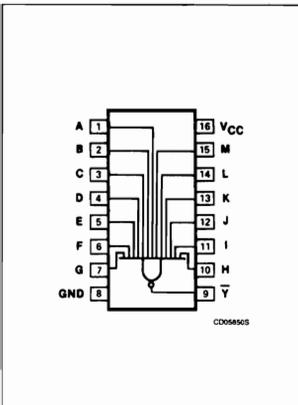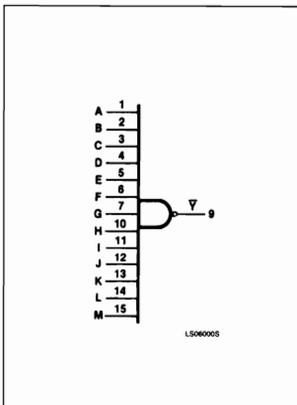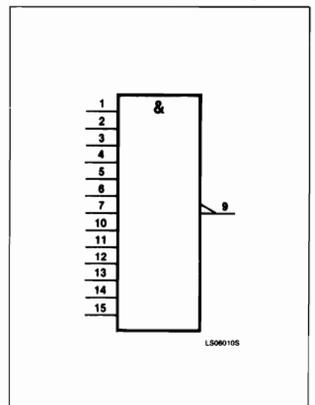
# 74S134
## Gate

**12-Input NAND Gate (3-State)**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT |
|---|---|---|
| 74S134 | 5ns | 10mA |

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| $D_0 \dots D_{11}$ | $\overline{OE}$ | $\overline{Y}$ |
| H ... H | L | L |
| one input = L | L | H |
| X ... X | H | (Z) |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74S134N |
| Plastic SO | N74S134D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S |
|---|---|---|
| All | Inputs | 1Sul |
| $\overline{Y}$ | Output | 10Sul |

**NOTE:**
Where a 74S unit load (Sul) is understood to be 50µA $I_{IH}$ and –2.0mA $I_{IL}$.

## PIN CONFIGURATION
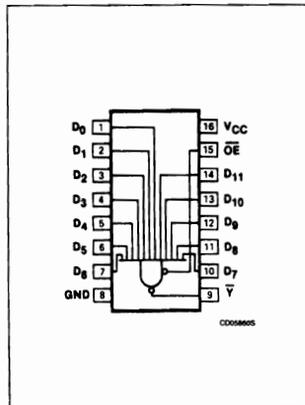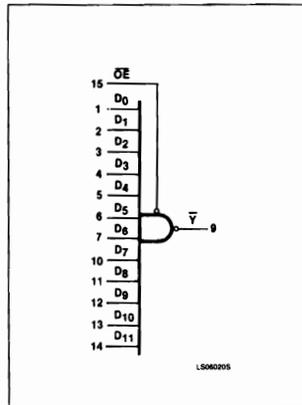


## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)
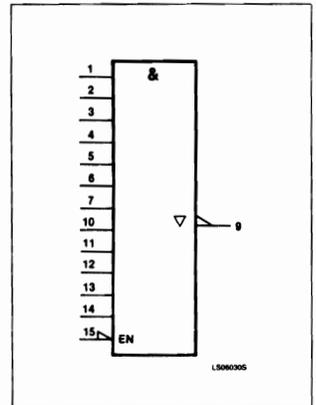
# 74S135
## Gate

**Quad Exclusive OR/NOR Gate**
*Product Specification*

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 74S135 | 9ns | 65mA |

## FUNCTION TABLE

| INPUTS | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| L | L | L | L |
| L | H | L | H |
| H | L | L | H |
| H | H | L | L |
| L | L | H | H |
| L | H | H | L |
| H | L | H | L |
| H | H | H | H |

H = HIGH voltage level
L = LOW voltage level

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|--------------------------------------------------------------|
| Plastic DIP | N74S135N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S |
|------|-------------|-----|
| All | Inputs | 1Sul |
| All | Outputs | 10Sul |

**NOTE:**
A 74S unit load (Sul) is understood to be 50µA $I_{IH}$ and −2.0mA $I_{IL}$.

## PIN CONFIGURATION



CD05870S

## LOGIC SYMBOL



LS06040S

## LOGIC SYMBOL (IEEE/IEC)



LS06050S

82
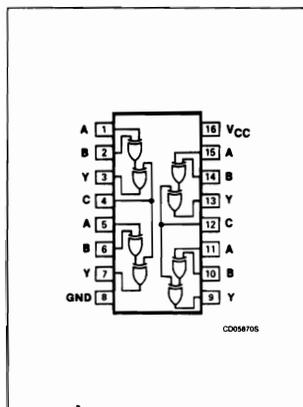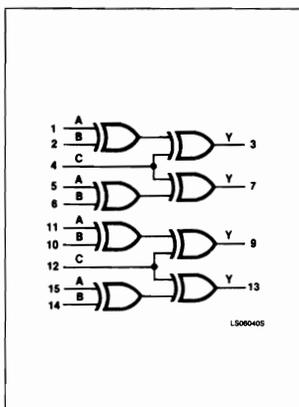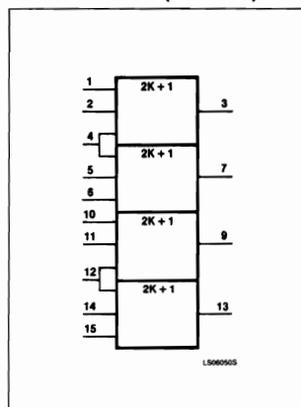
# 74LS136
## Gate

Quad Two-Input Exclusive-OR Gate (Open Collector)
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 74LS136 | 18ns | 6.1mA |

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

H = HIGH voltage level
L = LOW voltage level

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|-------------------------------------------------------------|
| Plastic DIP | N74LS136N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|------|-------------|------|
| A, B | Inputs | 2LSul |
| Y | Output | 10LSul |

**NOTE:**
Where a 74LS unit load (LSul) is 20μA $I_{IH}$ and−0.4mA $I_{IL}$.

## PIN CONFIGURATION



$V_{CC}$ = Pin 14
GND = Pin 7

## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



83
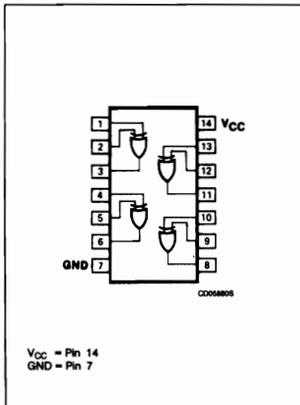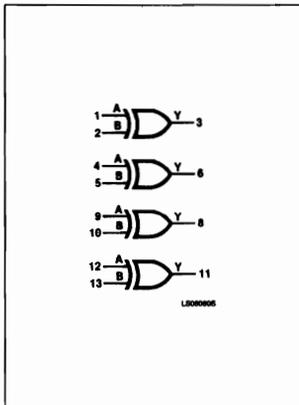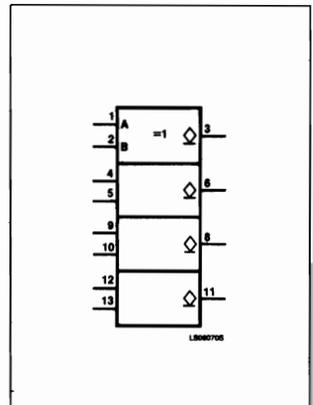
# 54S/74S137
## 1-OF-8 DECODER/DEMULTIPLEXER
### (With Input Latches)

**DESCRIPTION** — The 'S137 is a very high speed 1-of-8 decoder/demultiplexer with latches on the three address inputs. This device essentially combines the function and speed of the 'S138 1-of-8 decoder with a 3-bit storage latch. When the latch is enabled ($\overline{LE}$ = LOW), the 'S137 acts as a 1-of-8 active LOW decoder. When the Latch Enable ($\overline{LE}$) goes from LOW to HIGH, the last data present at the inputs before this transition is stored in the latches. Further address changes are ignored as long as $\overline{LE}$ remains HIGH. The output enable gate ($\overline{E}_1 \cdot E_2$) controls the state of the outputs independent of the Address inputs or latch operation. All outputs are HIGH unless $\overline{E}_1$ is LOW and $E_2$ is HIGH. The 'S137 is ideally suited for implementing non-overlapping decoders in 3-state systems and strobed (stored address) applications in bus oriented systems. The 'S137 is fabricated with the Schottky barrier diode process for high speed.

- SCHOTTKY PROCESS FOR HIGH SPEED
- COMBINES 1-OF-8 DECODER WITH 3-BIT LATCH
- MULTIPLE INPUT ENABLE FOR EASY EXPANSION OR INDEPENDENT CONTROLS
- ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE $V_{CC}$ = +5.0 V ±5%, $T_A$ = 0°C to +70°C | MILITARY GRADE $V_{CC}$ = +5.0 V ±10%, $T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 74S137PC | | 9B |
| Ceramic DIP (D) | A | 74S137DC | 54S137DM | 6B |
| Flatpak (F) | A | 74S137FC | 54S137FM | 4L |

**LOGIC SYMBOL**

$V_{CC}$ = Pin 16
GND = Pin 8

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74S (U.L.) HIGH/LOW |
|---|---|---|
| $A_0 - A_2$ | Address Inputs | 1.25/1.25 |
| $\overline{LE}$ | Latch Enable Input (Active LOW) | 1.25/1.25 |
| $\overline{E}_1$ | Enable Input (Active LOW) | 1.25/1.25 |
| $E_2$ | Enable Input (Active HIGH) | 1.25/1.25 |
| $\overline{O}_0 - \overline{O}_7$ | Outputs (Active LOW) | 25/12.5 |
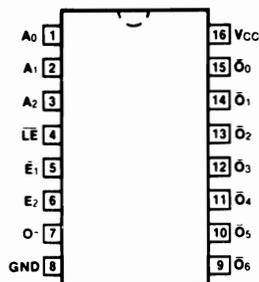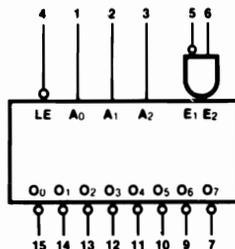
## TRUTH TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{LE}$ | $\overline{E}_1$ | $E_2$ | $A_0$ | $A_1$ | $A_2$ | $\overline{O}_0$ | $\overline{O}_1$ | $\overline{O}_2$ | $\overline{O}_3$ | $\overline{O}_4$ | $\overline{O}_5$ | $\overline{O}_6$ | $\overline{O}_7$ |
| H | L | H | X | X | X | STABLE | | | | | | | |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | H | L | L | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | H | L | H | H | H | L | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | L | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

## LOGIC DIAGRAM
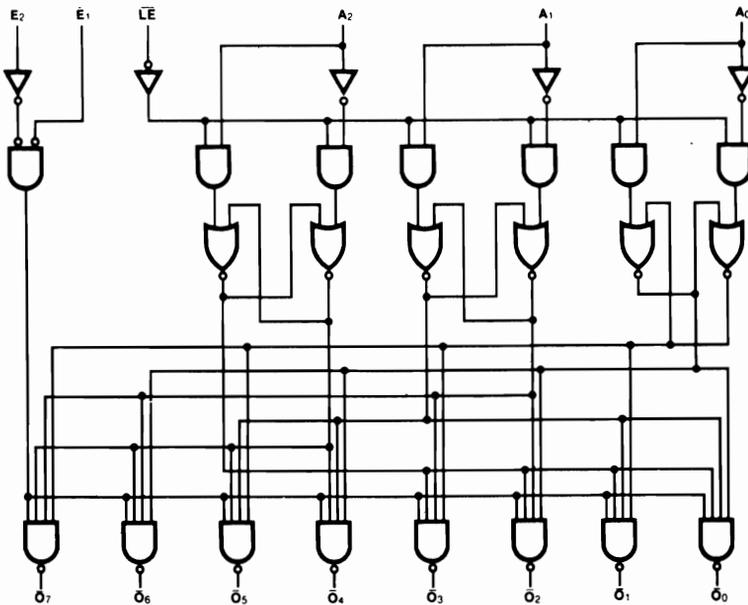
**FUNCTIONAL DESCRIPTION** — The 'S137 is a very high speed 1-of-8 decoder/demultiplexer fabricated with the Schottky barrier diode process. The decoder accepts three binary weighted inputs ($A_0$, $A_1$, $A_2$) and when enabled provides eight mutually exclusive active LOW outputs ($\overline{O}_0 - \overline{O}_7$). The 'S137 also features a 3-bit latch on the Address inputs. The device functions as a 1-of-8 decoder (same as 'S138) when the Latch Enable ($\overline{LE}$) is LOW. When $\overline{LE}$ is HIGH, the address present one setup time prior to the LOW-to-HIGH transition of $\overline{LE}$ will be stored in the address latches and the outputs will not be affected by further address changes. The output enable control is an AND gate comprised of one active LOW input ($\overline{E}_1$) and one active HIGH input ($E_2$). All outputs are HIGH unless the enable inputs ($\overline{E}_1 \bullet E_2$) are in their true (active) state.

A non-overlapping decoder with edge-triggered address inputs can be easily implemented by tying the Latch Enable input $\overline{LE}$ to the active HIGH Enable input ($E_2$). When this input ($\overline{LE} \bullet E_2$) is LOW, all outputs are forced HIGH and a new address enters the latches. When the $\overline{LE} \bullet E_2$ input goes HIGH, the address is stored in the latches and the corresponding output gate is enabled (goes LOW). In this configuration, the address must be stable only one setup time prior to the LOW-to-HIGH transition of the $\overline{LE} \bullet E_2$ input. The addressed output remains active LOW as long as the ($\overline{LE} \bullet E_2$) input remains HIGH, even if the address changes. Data or control information can thus be strobed into the 'S137 from very noisy or bus oriented systems using a LOW pulse width equal to the minimum latch enable pulse width $t_w(L)$.

The multiple enable inputs along with the address latches allows easy expansion to a 1-of-64 decoder with nonoverlapping outputs (see *Figure a*).
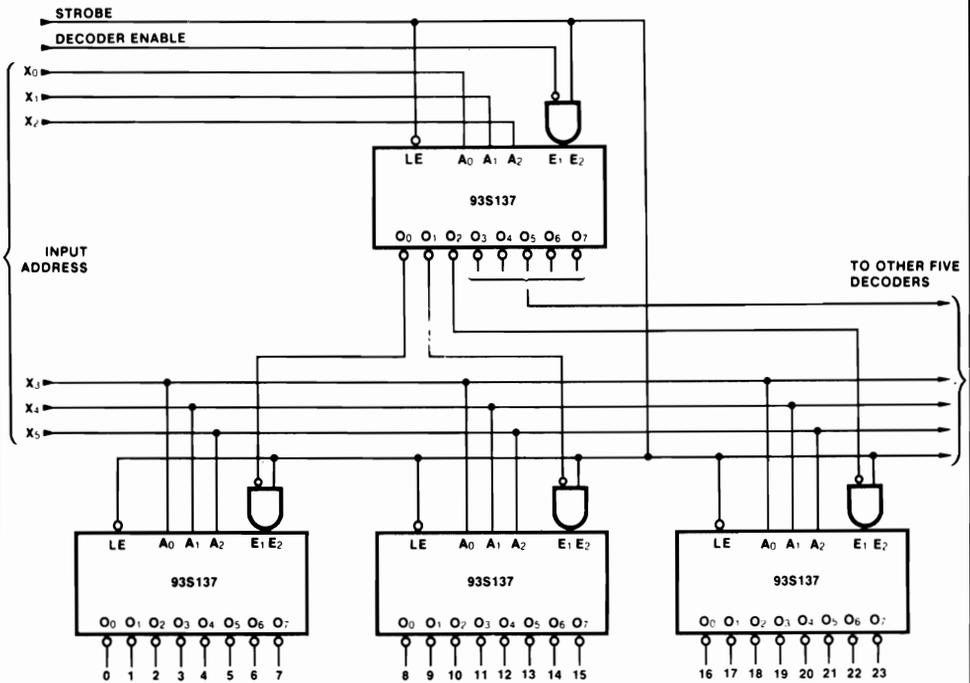


**Fig. a   High Speed 1-of-64 Decoder with Input Data Storage**

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# 74LS138, S138
## Decoders/Demultiplexers

### 1-Of-8 Decoder/Demultiplexer
*Product Specification*

## FEATURES
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

## DESCRIPTION
The '138 decoder accepts three binary weighted inputs ($A_0$, $A_1$, $A_2$) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{0} - \overline{7}$). The device features three Enable Inputs: two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH ($E_3$). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and $E_3$ is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS138 | 20ns | 6.3mA |
| 74S138 | 7ns | 49mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74S138N, N74LS138N |
| Plastic SO | N74LS138D, N74S138D |

**NOTE:**
For information regarding devices processed to Military Specifications see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|---|---|---|---|
| All | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 10LSul |

**NOTE:**
Where a 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and $-2.0$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION
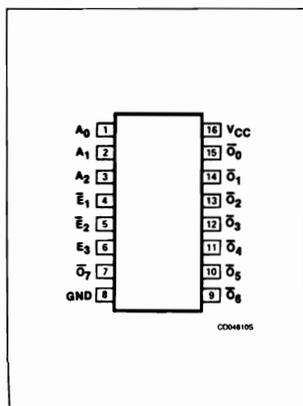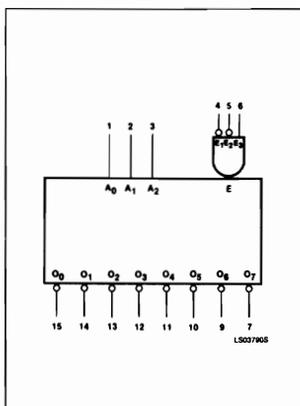


## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)
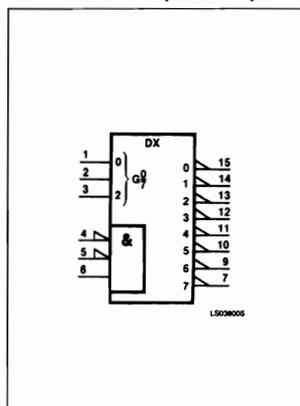
# 74LS138, S138

## LOGIC DIAGRAM



```
A₂    A₁    A₀           Ē₁  Ē₂  E₃
(3)   (2)   (1)          (4) (5) (6)
```

```
(7)   (9)   (10)  (11)  (12)  (13)  (14)  (15)
Ō₇    Ō₆    Ō₅    Ō₄    Ō₃    Ō₂    Ō₁    Ō₀
```

```
LD01880S
```

( ) = Pin number
$V_{CC}$ = Pin 16
GND = Pin 8
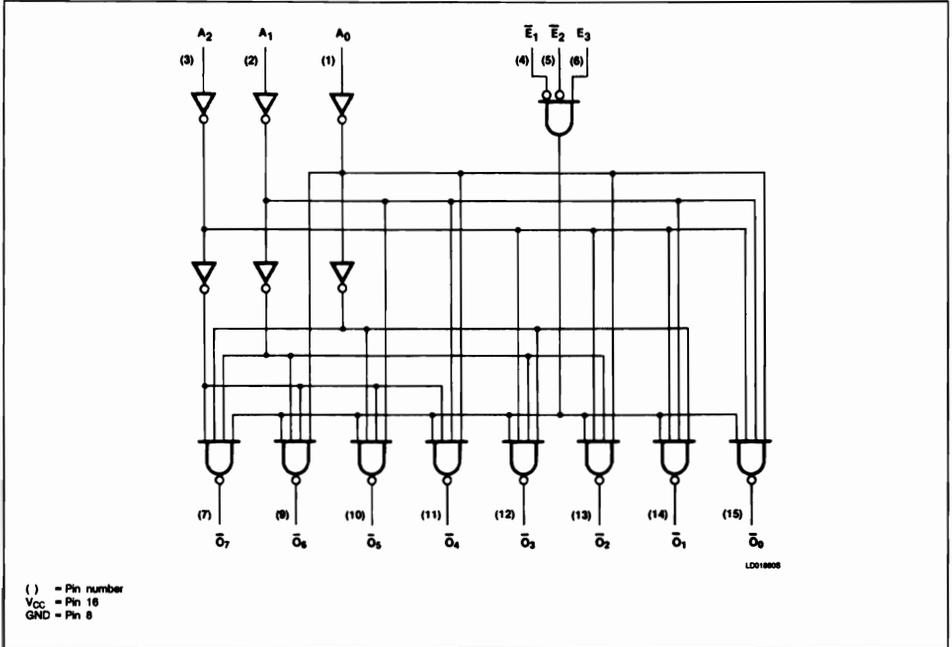
## FUNCTION TABLE

| INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ē₁ | Ē₂ | E₃ | A₀ | A₁ | A₂ | 0̄ | 1̄ | 2̄ | 3̄ | 4̄ | 5̄ | 6̄ | 7̄ |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | H | L | L | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | H | L | H | H | H | L | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | L | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

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# 74LS139, S139
## Decoders/Demultiplexers

**Dual 1-of-4 Decoder/Demultiplexer**
*Product Specification*

**Logic Products**

## FEATURES
- Demultiplexing capability
- Two independent 1-of-4 decoders
- Multifunction capability
- Replaces 9321 and 93L21 for higher performance

## DESCRIPTION
The '139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs ($A_0$, $A_1$) and providing four mutually exclusive active LOW outputs ($\overline{0} - \overline{3}$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH, every output is forced HIGH. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

| TYPE | TYPICAL PROPAGATION DELAY (ENABLE AT 2 LOGIC LEVELS) | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS139 | 19ns | 6.8mA |
| 74S139 | 6ns | 60mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74S139N, N74LS139N |
| Plastic SO | N74LS139D, N74S139D |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|---|---|---|---|
| All | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 10LSul |

NOTE:
A 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8
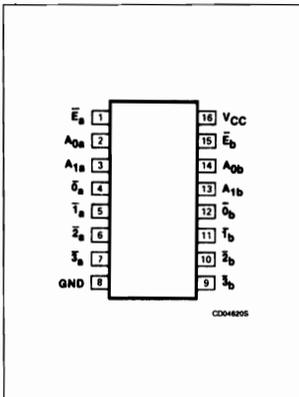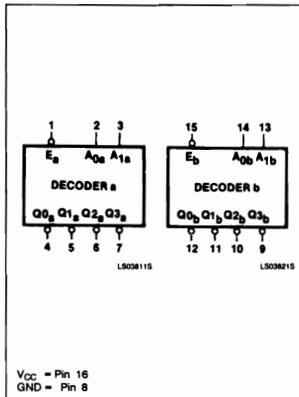
## LOGIC SYMBOL (EEE/IEC)
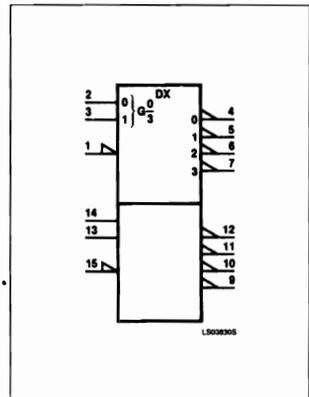
# 74LS139, S139

## LOGIC DIAGRAM



```
( )  = Pin number
VCC  = Pin 16
GND  = Pin 8
```
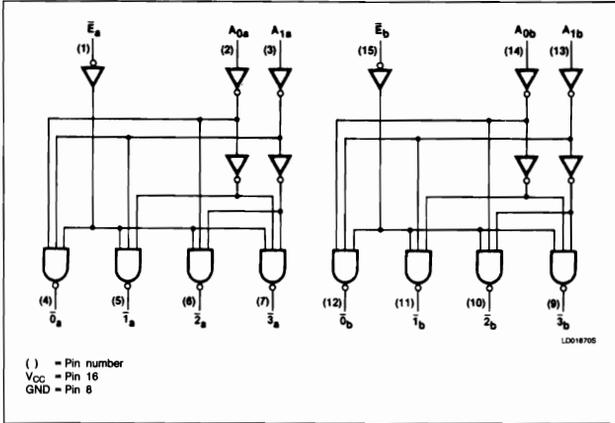
## FUNCTION TABLE

| INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|
| $\bar{E}$ | $A_0$ | $A_1$ | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | H | L | H | L | H | H |
| L | L | H | H | H | L | H |
| L | H | H | H | H | H | L |

H = HIGH voltage level
L = LOW voltage level

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74LS | 74S | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −1000 | μA |
| $I_{OL}$ | LOW-level output current | | | 8 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 74145
## Decoder/Driver

**BCD-To-Decimal Decoder/Driver (Open Collector)**
*Product Specification*

**Logic Products**

## FEATURES
- 80mA output drive capability
- 15V output breakdown voltage
- See '45 for 30V output voltage
- See '42 for standard TTL outputs

## DESCRIPTION
The '145 is a 1-of-10 decoder with Open Collector outputs. This decoder accepts BCD inputs on the $A_0$ to $A_3$ address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with $A_3$ used as an active LOW enable.

The '145 features an output breakdown voltage of 15V. This device is ideal as a lamp or solenoid driver.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|-------------------------------|
| 74145 | 24ns | 43mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|----------------------------------------------------------------|
| Plastic DIP | N74145N |
| Plastic SO | N74145D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|-------------|-----|
| All | Inputs | 1ul |
| All | Outputs | 12.5ul |

**NOTE:**
Where a 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



91

## LOGIC DIAGRAM



( ) = Pin number
$V_{CC}$ = Pin 16
GND = Pin 8
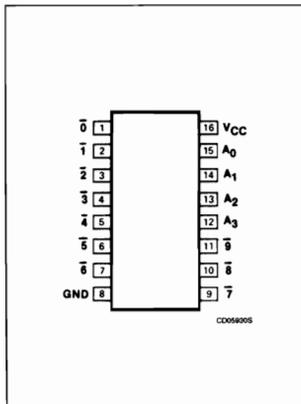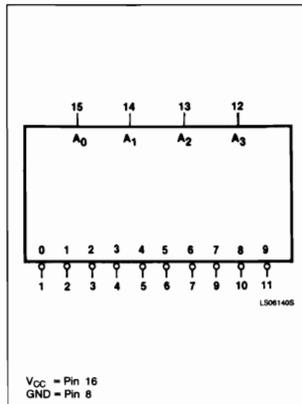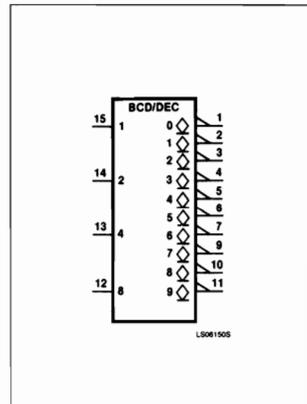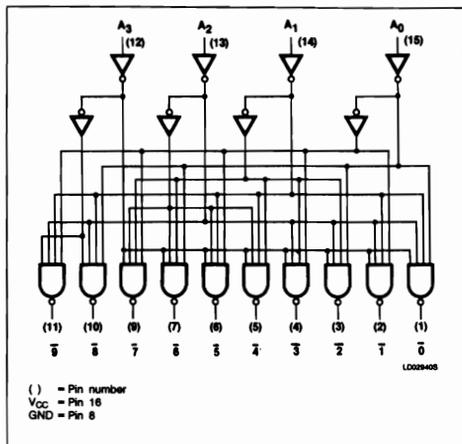
## FUNCTION TABLE

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | $\bar{0}$ | $\bar{1}$ | $\bar{2}$ | $\bar{3}$ | $\bar{4}$ | $\bar{5}$ | $\bar{6}$ | $\bar{7}$ | $\bar{8}$ | $\bar{9}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | L | L | L | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | H | H | L | H | H | H | H | H | H | H |
| L | L | H | H | H | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| L | H | L | H | H | H | H | H | H | L | H | H | H | H |
| L | H | H | L | H | H | H | H | H | H | L | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | L | H | H |
| H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |
| H | L | H | L | H | H | H | H | H | H | H | H | H | H |
| H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | L | L | H | H | H | H | H | H | H | H | H | H |
| H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = HIGH voltage levels
L = LOW voltage levels

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +15 | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | mA |
| $V_{OH}$ | HIGH-level output voltage | | | 15 | V |
| $I_{OL}$ | LOW-level output current | | | 80 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

# 74147
## Encoder

**10-Line-To-4-Line Priority Encoder**
*Product Specification*

**Logic Products**

## FEATURES
- **Encodes 10-line decimal to 4-line BCD**
- **Useful for 10-position switch encoding**
- **Used in code converters and generators**

## DESCRIPTION
The '147 9-input priority encoder accepts data from nine active-LOW inputs ($\bar{I}_1 - \bar{I}_9$) and provides a binary representation on the four active-LOW outputs ($A_0 - A_3$). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\bar{I}_9$ having the highest priority.

The device provides the 10-line-to-4-line priority encoding function by use of the implied decimal "zero." The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|-------------------------------|
| 74147 | 10ns | 46mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|---------------------------------------------------------------|
| Plastic DIP | N74147N |

**NOTE:**
For information regarding devices processed to Military Specifications see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|-------------|-----|
| All | Inputs | 1ul |
| All | Outputs | 10ul |

**NOTE:**
A 74 unit load (ul) is understood to be 40μA $I_{IH}$ and $-1.6$mA $I_{IL}$.

## PIN CONFIGURATION



CD05940S

## LOGIC SYMBOL



LS05160S

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



LS05170S

93

## LOGIC DIAGRAM



( ) = Pin number
$V_{CC}$ = Pin 16
GND = Pin 8

LD02950S
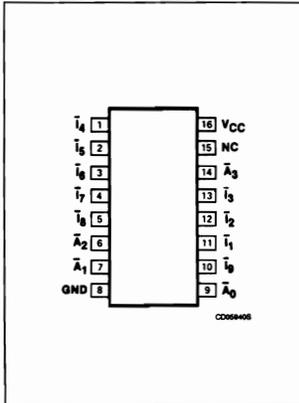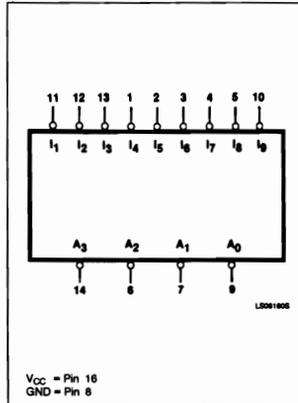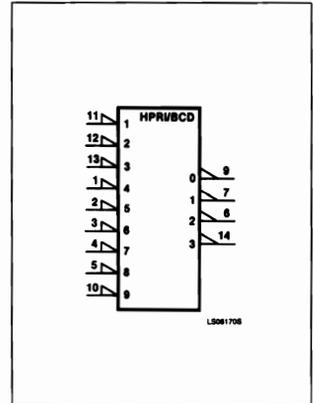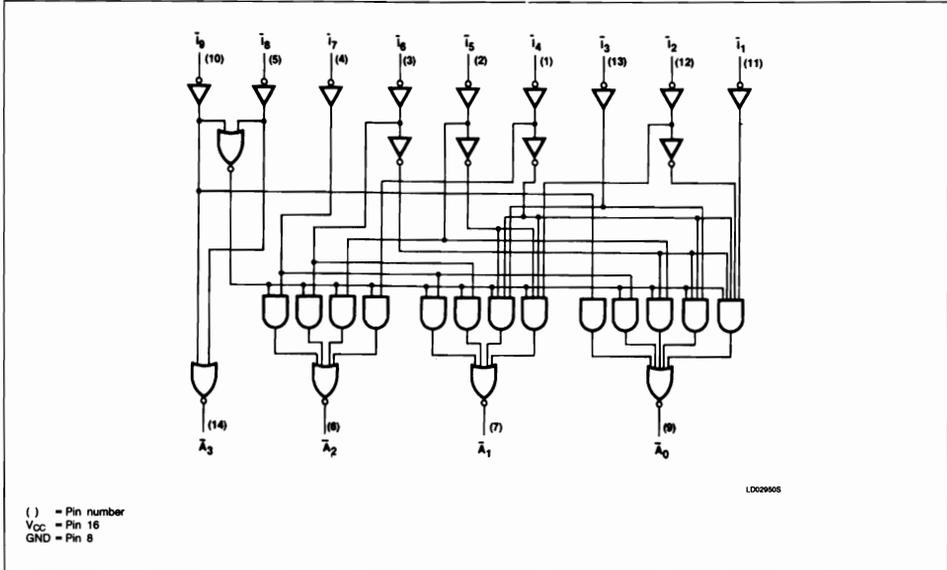
## FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $I_8$ | $I_9$ | $\bar{A}_3$ | $\bar{A}_2$ | $\bar{A}_1$ | $\bar{A}_0$ |
| H | H | H | H | H | H | H | H | H | H | H | H | H |
| X | X | X | X | X | X | X | X | L | L | H | H | L |
| X | X | X | X | X | X | X | L | H | L | H | H | H |
| X | X | X | X | X | X | L | H | H | H | L | L | L |
| X | X | X | X | X | L | H | H | H | H | L | L | H |
| X | X | X | X | L | H | H | H | H | H | L | H | L |
| X | X | X | L | H | H | H | H | H | H | L | H | H |
| X | X | L | H | H | H | H | H | H | H | H | L | L |
| X | L | H | H | H | H | H | H | H | H | H | L | H |
| L | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

# 74148
## Encoder

### 8-Input Priority Encoder
### *Product Specification*

## FEATURES
- Code conversions
- Multi-channel D/A converter
- Decimal-to-BCD converter
- Cascading for priority encoding of "N" bits
- Input Enable capability
- Priority encoding — automatic selection of highest priority input line
- Output Enable — active LOW when all inputs HIGH
- Group Signal output — active when any input is LOW

## DESCRIPTION
The '148 8-input priority encoder accepts data from eight active-LOW inputs and provides a binary representation on the three active-LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\bar{I}_7$ having the highest priority.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74148 | 10ns | 38mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74148N |
| Plastic SO | |

**NOTES:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| $\bar{I}_0$ | Input | 1ul |
| $\bar{I}_1 - \bar{I}_7$ | Inputs | 2ul |
| $\overline{EI}$ | Input | 2ul |
| All | Outputs | 10ul |

**NOTE:**
A 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$.

## PIN CONFIGURATION



CD04630S

## LOGIC SYMBOL



LS03840S

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



LS03850S
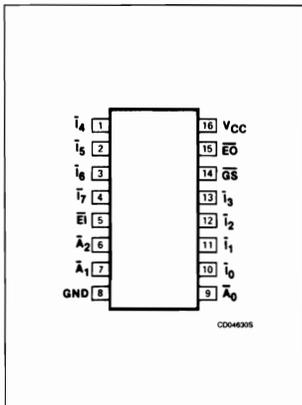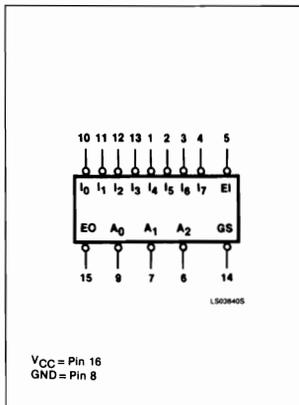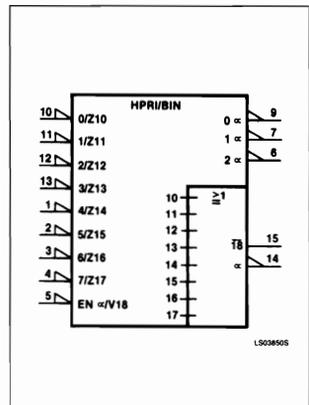
A HIGH on the Enable Input (EI) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

A Group Signal (GS) output and an Enable Output (EO) are provided with the three data outputs. The GS is active-LOW when any input is LOW; this indicates when any input is active. The EO is active-LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both EO and GS are active-HIGH when the Enable input is HIGH.

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8

LD01880S
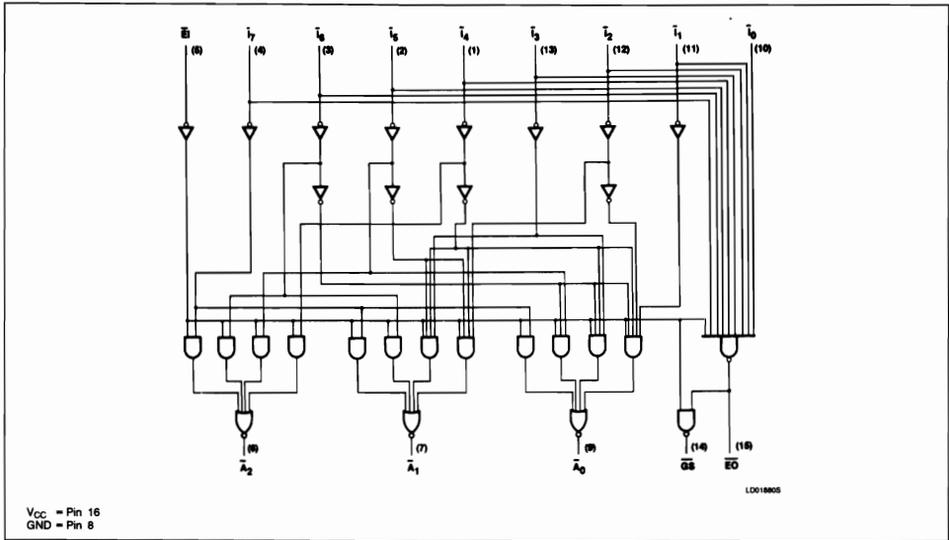
## FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EI | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | GS | $A_0$ | $A_1$ | $A_2$ | EO |
| H | X | X | X | X | X | X | X | X | H | H | H | H | H |
| L | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | X | X | X | X | X | X | X | L | L | L | L | L | H |
| L | X | X | X | X | X | X | L | H | L | H | L | L | H |
| L | X | X | X | X | X | L | H | H | L | L | H | L | H |
| L | X | X | X | X | L | H | H | H | L | H | H | L | H |
| L | X | X | X | L | H | H | H | H | L | L | L | H | H |
| L | X | X | L | H | H | H | H | H | L | H | L | H | H |
| L | X | L | H | H | H | H | H | H | L | L | H | H | H |
| L | L | H | H | H | H | H | H | H | L | H | H | H | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

# 74150
## Multiplexer

16-Input Multiplexer
*Product Specification*

**Logic Products**

## FEATURES
- Select data from 16 sources
- Demultiplexing capability
- Active-LOW enable or strobe
- Inverting data output

## DESCRIPTION
The '150 is a logical implementation of a single-pole, 16-position switch with the switch position controlled by the state of four Select inputs. $S_0$, $S_1$, $S_2$, $S_3$. The Multiplexer output ($\bar{Y}$) inverts the selected data. The Enable input ($\bar{E}$) is active-LOW. When $\bar{E}$ is HIGH the $\bar{Y}$ output is HIGH regardless of all other inputs. In one package the '150 provides the ability to select from 16 sources of data or control information.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 74150 | 17ns | 40mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|----------------------------------------------------------------|
| Plastic DIP | N74150N |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|-------------|-----|
| All | Inputs | 1ul |
| $\bar{Y}$ | Output | 10ul |

NOTE:
A 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$.

## PIN CONFIGURATION



```
·D₇  [1]      [24]  V_CC
D₆  [2]      [23]  D₈
D₅  [3]      [22]  D₉
D₄  [4]      [21]  D₁₀
D₃  [5]      [20]  D₁₁
D₂  [6]      [19]  D₁₂
D₁  [7]      [18]  D₁₃
D₀  [8]      [17]  D₁₄
Ē   [9]      [16]  D₁₅
Ȳ   [10]     [15]  S₀
S₃  [11]     [14]  S₁
GND [12]     [13]  S₂
```

CD05950S

## LOGIC SYMBOL



$V_{CC}$ = Pin 24
GND = Pin 12

LS06180S

## LOGIC SYMBOL (IEEE/IEC)



LS06190S

# 74150

## LOGIC DIAGRAM



( ) = Pin numbers
$V_{CC}$ = Pin 24
GND = Pin 12

LD02960S

## FUNCTION TABLE

| INPUTS | | | | | | | | | | | | | | | | | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | $\overline{E}$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $D_8$ | $D_9$ | $D_{10}$ | $D_{11}$ | $D_{12}$ | $D_{13}$ | $D_{14}$ | $D_{15}$ | $\overline{Y}$ |
| X | X | X | X | H | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | L | L | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | L | L | L | H | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L |
| L | L | L | H | L | X | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | L | H | L | X | H | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L |
| L | L | H | L | L | X | X | L | X | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | H | L | L | X | X | H | X | X | X | X | X | X | X | X | X | X | X | X | X | L |
| L | L | H | H | L | X | X | X | L | X | X | X | X | X | X | X | X | X | X | X | X | H |
| L | L | H | H | L | X | X | X | H | X | X | X | X | X | X | X | X | X | X | X | X | L |
| L | H | L | L | L | X | X | X | X | L | X | X | X | X | X | X | X | X | X | X | X | H |
| L | H | L | L | L | X | X | X | X | H | X | X | X | X | X | X | X | X | X | X | X | L |
| L | H | L | H | L | X | X | X | X | X | L | X | X | X | X | X | X | X | X | X | X | H |
| L | H | L | H | L | X | X | X | X | X | H | X | X | X | X | X | X | X | X | X | X | L |
| L | H | H | L | L | X | X | X | X | X | X | L | X | X | X | X | X | X | X | X | X | H |
| L | H | H | L | L | X | X | X | X | X | X | H | X | X | X | X | X | X | X | X | X | L |
| L | H | H | H | L | X | X | X | X | X | X | X | L | X | X | X | X | X | X | X | X | H |
| L | H | H | H | L | X | X | X | X | X | X | X | H | X | X | X | X | X | X | X | X | L |
| H | L | L | L | L | X | X | X | X | X | X | X | X | L | X | X | X | X | X | X | X | H |
| H | L | L | L | L | X | X | X | X | X | X | X | X | H | X | X | X | X | X | X | X | L |
| H | L | L | H | L | X | X | X | X | X | X | X | X | X | L | X | X | X | X | X | X | H |
| H | L | L | H | L | X | X | X | X | X | X | X | X | X | H | X | X | X | X | X | X | L |
| H | L | H | L | L | X | X | X | X | X | X | X | X | X | X | L | X | X | X | X | X | H |
| H | L | H | L | L | X | X | X | X | X | X | X | X | X | X | H | X | X | X | X | X | L |
| H | L | H | H | L | X | X | X | X | X | X | X | X | X | X | X | L | X | X | X | X | H |
| H | L | H | H | L | X | X | X | X | X | X | X | X | X | X | X | H | X | X | X | X | L |
| H | H | L | L | L | X | X | X | X | X | X | X | X | X | X | X | X | L | X | X | X | H |
| H | H | L | L | L | X | X | X | X | X | X | X | X | X | X | X | X | H | X | X | X | L |
| H | H | L | H | L | X | X | X | X | X | X | X | X | X | X | X | X | X | L | X | X | H |
| H | H | L | H | L | X | X | X | X | X | X | X | X | X | X | X | X | X | H | X | X | L |
| H | H | H | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L | X | H |
| H | H | H | L | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H | X | L |
| H | H | H | H | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L | H |
| H | H | H | H | L | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

98

# 74151, LS151, S151
## Multiplexers

**8-Input Multiplexer**
*Product Specification*

## FEATURES
- **Multifunction capability**
- **Complementary outputs**
- **See '251 for 3-state version**

## DESCRIPTION
The '151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, $S_0$, $S_1$, $S_2$. True (Y) and Complement ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, the $\overline{Y}$ output is HIGH and the Y output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Y = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 +$$
$$I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 +$$
$$I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 +$$
$$I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2$$

In one package the '151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

| TYPE | TYPICAL PROPAGATION DELAY (ENABLE TO $\overline{Y}$) | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|------|------|
| 74151 | 18ns | 29mA |
| 74LS151 | 12ns | 6mA |
| 74S151 | 9ns | 45mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|------|------|
| Plastic DIP | N74151N, N74LS151N, N74S151N |
| Plastic SO | N74LS151D, N74S151D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|------|------|------|------|------|
| All | Inputs | 1ul | 1Sul | 1LSul |
| All | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, a 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and $-2.0$mA $I_{IL}$, and 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

# 74151, LS151, S151

## LOGIC DIAGRAM



LD01890S

$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers

## FUNCTION TABLE

| INPUTS | | | | | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\bar{E}$ | $S_2$ | $S_1$ | $S_0$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $\bar{Y}$ | Y |
| H | X | X | X | X | X | X | X | X | X | X | X | H | L |
| L | L | L | L | L | X | X | X | X | X | X | X | H | L |
| L | L | L | L | H | X | X | X | X | X | X | X | L | H |
| L | L | L | H | X | L | X | X | X | X | X | X | H | L |
| L | L | L | H | X | H | X | X | X | X | X | X | L | H |
| L | L | H | L | X | X | L | X | X | X | X | X | H | L |
| L | L | H | L | X | X | H | X | X | X | X | X | L | H |
| L | L | H | H | X | X | X | L | X | X | X | X | H | L |
| L | L | H | H | X | X | X | H | X | X | X | X | L | H |
| L | H | L | L | X | X | X | X | L | X | X | X | H | L |
| L | H | L | L | X | X | X | X | H | X | X | X | L | H |
| L | H | L | H | X | X | X | X | X | L | X | X | H | L |
| L | H | L | H | X | X | X | X | X | H | X | X | L | H |
| L | H | H | L | X | X | X | X | X | X | L | X | H | L |
| L | H | H | L | X | X | X | X | X | X | H | X | L | H |
| L | H | H | H | X | X | X | X | X | X | X | L | H | L |
| L | H | H | H | X | X | X | X | X | X | X | H | L | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

# 74153, LS153, S153
# Multiplexers

## Dual 4-Line To 1-Line Multiplexer
### *Product Specification*

**Logic Products**

## FEATURES
- **Non-inverting outputs**
- **Separate enable for each section**
- **Common select inputs**
- **See '253 for 3-state version**

## DESCRIPTION
The '153 is a dual 4-input multiplexer that can select 2 bits of data from up to eight (8) sources under control of the common Select inputs ($S_0$, $S_1$). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs ($Y_a$, $Y_b$) are forced LOW when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH.

$Y_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_2)$

$Y_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_2)$

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74153 | 18ns | 36mA |
| 74LS153 | 18ns | 6.2mA |
| 74S153 | 9ns | 45mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74153N, N74LS153N, N74S153N |
| Plastic SO | N74LS153D, N74S153D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| All | Inputs | 1ul | 1Sul | 1LSul |
| All | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



101

**74153, LS153, S153**
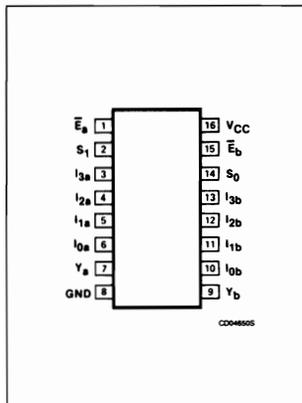
The '153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
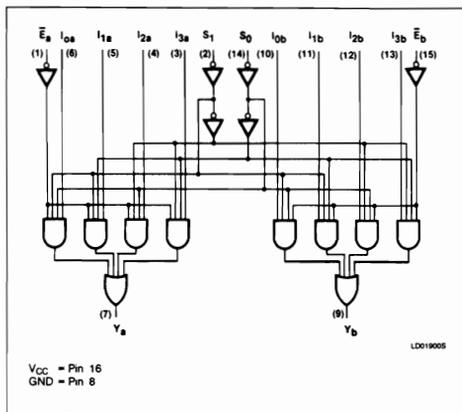
## FUNCTION TABLE

| SELECT INPUTS | | INPUTS (a or b) | | | | | OUTPUT |
|---|---|---|---|---|---|---|---|
| $S_0$ | $S_1$ | $\bar{E}$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | Y |
| X | X | H | X | X | X | X | L |
| L | L | L | L | X | X | X | L |
| L | L | L | H | X | X | X | H |
| H | L | L | X | L | X | X | L |
| H | L | L | X | H | X | X | H |
| L | H | L | X | X | L | X | L |
| L | H | L | X | X | H | X | H |
| H | H | L | X | X | X | L | L |
| H | H | L | X | X | X | H | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | 74S | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | −12 | | | −18 | | | −18 | | mA |
| $I_{OH}$ | HIGH-level output current | | −800 | | | −400 | | | −1000 | | μA |
| $I_{OL}$ | LOW-level output current | | 16 | | | 8 | | | 20 | | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | 0 | | 70 | °C |

102

# 74154, LS154
## Decoder/Demultiplexers

1-of-16 Decoder/Demultiplexer
*Product Specification*

**Logic Products**

## FEATURES
- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

## DESCRIPTION
The '154 decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The '154 can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 74154 | 21ns | 34mA |
| 74LS154 | 15ns | 9mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|---------------------------------------------------------------|
| Plastic DIP | N74154N, N74LS154N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|------|-------------|-----|------|
| All | Inputs | 1ul | 1LSul |
| All | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



CD05960S

## LOGIC SYMBOL



$V_{CC}$ = Pin 24
GND = Pin 12

LS06200S

## LOGIC SYMBOL (IEEE/IEC)



LS06210S

## LOGIC DIAGRAM



$V_{CC}$ = Pin 24
GND = Pin 12
( ) = Pin numbers

LD029705
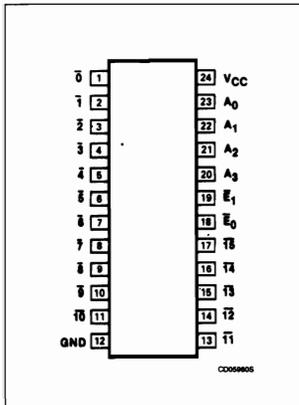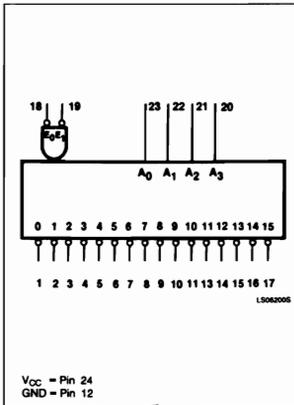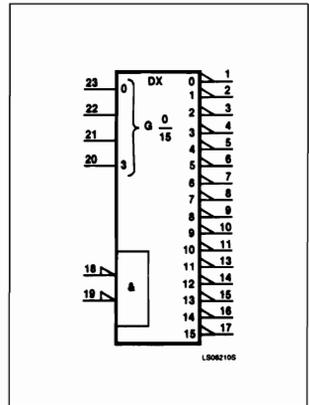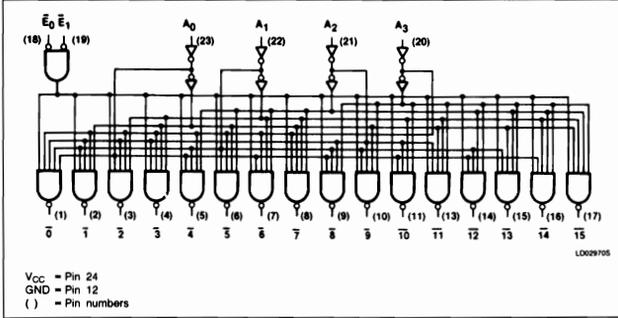
## FUNCTION TABLE

| INPUTS | | | | | | OUTPUT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $E_0$ | $E_1$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | | 0 to 70 | °C |

# 74155, LS155
## Decoders/Demultiplexers

**Dual 2-Line To 4-Line Decoder/Demultiplexer**
*Product Specification*

## FEATURES
- **Common Address Inputs**
- **True or complement data demultiplexing**
- **Dual 1-of-4 or 1-of-8 decoding**
- **Function generator applications**

## DESCRIPTION
The '155 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address input ($A_0$, $A_1$) and provide four mutually exclusive active-LOW outputs ($\overline{0}$ – $\overline{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74155 | 18ns | 25mA |
| 74LS155 | 17ns | 6.1mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74155N, N74LS155N |
| Plastic SO | N74LS155D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| All | Inputs | 1ul | 1LSul |
| All | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and – 1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8

Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input ($E_a \cdot \overline{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the $\overline{E}_a$ or $E_a$ inputs respectively. The decoder "b" enable gate requires two active-LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The device can be used as a 1-of-8 decoder/demultiplexer by tying $E_a$ to $\overline{E}_b$ and relabeling the common connection address as ($A_2$); forming the common enable by connecting the remaining $\overline{E}_b$ and $\overline{E}_a$.

## FUNCTION TABLE

| ADDRESS | | ENABLE "a" | | OUTPUT "a" | | | | ENABLE "b" | | OUTPUT "b" | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_0$ | $A_1$ | $E_a$ | $\overline{E}_a$ | $\overline{0}$ | $\overline{1}$ | $\overline{2}$ | $\overline{3}$ | $\overline{E}_b$ | $\overline{E}_b$ | $\overline{0}$ | $\overline{1}$ | $\overline{2}$ | $\overline{3}$ |
| X | X | L | X | H | H | H | H | H | X | H | H | H | H |
| X | X | X | H | H | H | H | H | X | H | H | H | H | H |
| L | L | H | L | L | H | H | H | L | L | L | H | H | H |
| H | L | H | L | H | L | H | H | L | L | H | L | H | H |
| L | H | H | L | H | H | L | H | L | L | H | H | L | H |
| H | H | H | L | H | H | H | L | L | L | H | H | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

# 74156, LS156
## Decoders/Demultiplexers

**Dual 2-Line To 4-Line Decoder/Demultiplexer (Open Collector)**
*Product Specification*

## FEATURES
- Common Address inputs
- True or complement data demultiplexing
- Dual 1-of-4 or 1-of-8 decoding
- Function generator applications
- Outputs can be tied together

## DESCRIPTION
The '156 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address inputs ($A_0$, $A_1$) and provide four mutually exclusive active-LOW outputs ($\overline{0} - \overline{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74156 | 20ns | 25mA |
| 74LS156 | 31ns | 6.1mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74156N, N74LS156N |
| Plastic SO | N74LS156D • |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| All | Inputs | 1ul | 1LSul |
| All | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and –1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20μA $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD05670S

## LOGIC SYMBOL



LS06290S

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



LS06280S

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8

LD02990S

Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input ($E_a \cdot \overline{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the $\overline{E}_a$ or $E_a$ inputs respectively. The decoder "b" enable gate requires two active-LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The device can be used as a 1-of-8 decoder/ demultiplexer by tying $E_a$ to $\overline{E}_b$ and relabeling the common connection address as ($A_2$); forming the common enable by connecting the remaining $\overline{E}_b$ and $\overline{E}_a$.

The '156 can be used to generate all four minterms of two variables. The four minterms are useful to replace multiple gate functions in some applications. A further advantage of the '156 is being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown in the formula below:

$$f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1)$$
$$\cdot (E + A_0 + \overline{A}_1) \cdot (E + A_0 + A_1)$$

where $E = E_a + E_a$; $E = E_b + E_b$.

## FUNCTION TABLE

| ADDRESS | | ENABLE "a" | | OUTPUT "a" | | | | ENABLE "b" | | OUTPUT "b" | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_0$ | $A_1$ | $E_a$ | $\overline{E}_a$ | $\overline{0}$ | $\overline{1}$ | $\overline{2}$ | $\overline{3}$ | $\overline{E}_b$ | $\overline{E}_b$ | $\overline{0}$ | $\overline{1}$ | $\overline{2}$ | $\overline{3}$ |
| X | X | L | X | H | H | H | H | H | X | H | H | H | H |
| X | X | X | H | H | H | H | H | X | H | H | H | H | H |
| L | L | H | L | L | H | H | H | L | L | L | H | H | H |
| H | L | H | L | H | L | H | H | L | L | H | L | H | H |
| L | H | H | L | H | H | L | H | L | L | H | H | L | H |
| H | H | H | L | H | H | H | L | L | L | H | H | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

# 74157, 74158, LS157, LS158, S157, S158
## Data Selectors/Multiplexers

'157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
'158 Quad 2-Input Data Selector/Multiplexer (Inverted)
**Product Specification**

## DESCRIPTION

The '157 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the '157. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74157 | 13ns | 30mA |
| 74LS157 | 13ns | 9.7mA |
| 74S157 | 7.4ns | 50mA |
| 74158 | 13ns | 30mA |
| 74LS158 | 13ns | 4.8mA |
| 74S158 | 6ns | 40mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74157N, N74LS158N, N74S157N N74LS157N, N74S158N, N74LS158N |
| Plastic SO | N74LS157D, N74S158D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| S, $\overline{E}$ | Inputs | 1ul | 2Sul | 2LSul |
| Data | Inputs | 1ul | 1Sul | 1LSul |
| All | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and $-1.6mA$ $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and $-2.0mA$ $I_{IL}$, and a74LS unit load (LSul) is 20µA $I_{IH}$ and $-0.4mA$ $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM, '157



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC DIAGRAM, '158



$V_{CC}$ = Pin 16
GND = Pin 8
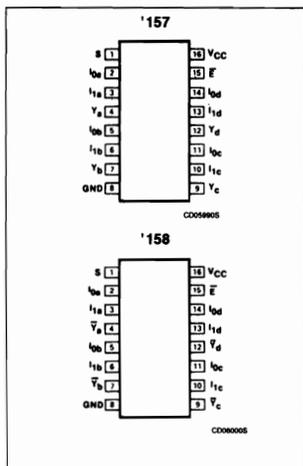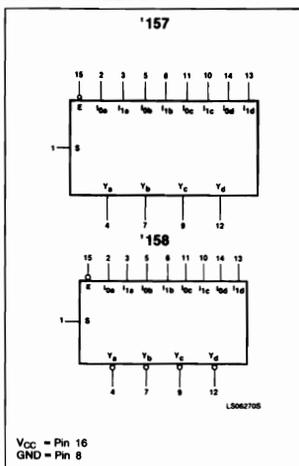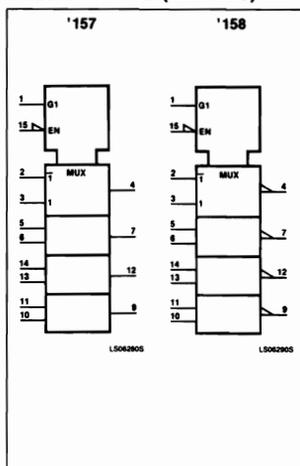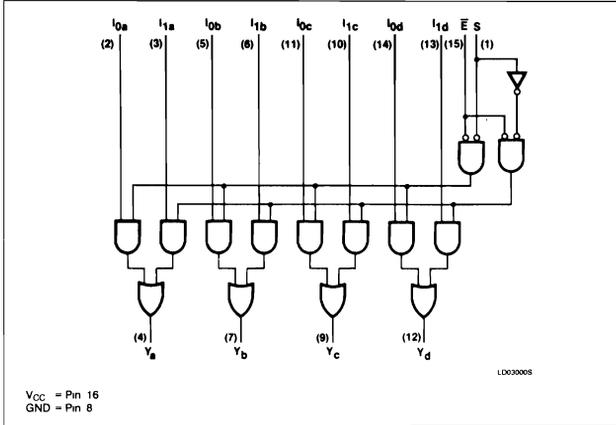
The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Y_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Y_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Y_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

The '158 is similar but has inverting outputs:

$$\overline{Y}_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$\overline{Y}_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Y}_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$\overline{Y}_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

### FUNCTION TABLE, '157

| ENABLE | SELECT INPUT | DATA INPUTS | | OUTPUT |
|---|---|---|---|---|
| $\overline{E}$ | S | $I_0$ | $I_1$ | Y |
| H | X | X | X | L |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
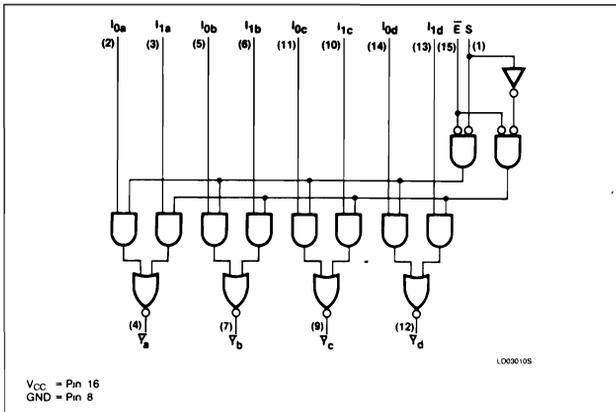
### FUNCTION TABLE, '158

| ENABLE | SELECT INPUT | DATA INPUTS | | OUTPUT |
|---|---|---|---|---|
| $\overline{E}$ | S | $I_0$ | $I_1$ | $\overline{Y}$ |
| H | X | X | X | H |
| L | L | L | X | H |
| L | L | H | X | L |
| L | H | X | L | H |
| L | H | X | H | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | 74S | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | | 0 to 70 | | °C |

110

# 74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A Counters

**'160, '162 BCD Decade Counter**
**'161, '163 4-Bit Binary Counter**
*Product Specification*

## FEATURES
- Synchronous counting and loading
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset ('160, '161)
- Synchronous reset ('162, '163)
- Hysteresis on Clock input (LS only)

## DESCRIPTION

Synchronous presettable decade (74160, 74LS160A, 74LS162A) and 4-bit (74161, 74LS161A, 74163, 74LS163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to HIGH or LOW level. A LOW level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the $D_0 - D_3$ inputs to be loaded into the counter on the positive-going edge of the clock (providing that the set-up and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.
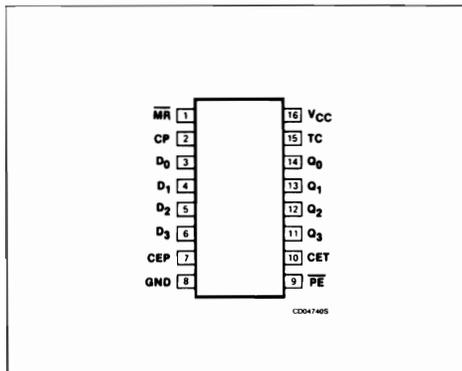
| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74160 – 74163 | 32MHz | 61mA |
| 74LS160A – 74LS163A | 32MHz | 19mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74160N, N74LS160AN, N74161N, N74LS161AN N74LS162AN, N74163N, N74LS163AN |
| Plastic SO | N74LS161AD, N74S163AD |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| CP, CET | Inputs | 2ul | 2LSul |
| D, CEP | Inputs | 1ul | 1LSul |
| $\overline{PE}$ | Input | 1ul | 2LSul |
| All | Outputs | 10ul | 10LSul |
| $\overline{MR}$ | Input ('160, '161) | 1ul | 1LSul |
| $\overline{MR}$ | Input ('162, '163) | 1ul | 2LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL
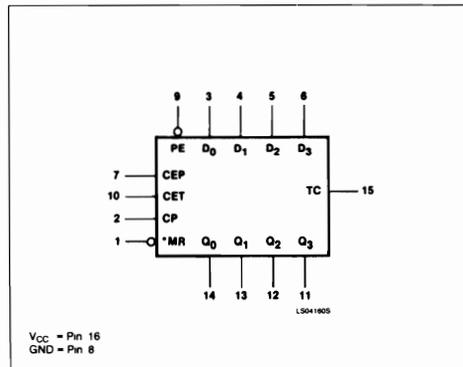


$V_{CC}$ = Pin 16
GND = Pin 8

# Counters
## 74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) in '160, 'LS160A, '161, and 'LS161A to LOW levels regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 'LS162A, '163, and LS163A, the clear function is synchronous. A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops ($Q_0 - Q_3$) to LOW levels after the next positive-going transition on the Clock (CP) input (providing that the set-up and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to the HIGH level output of $Q_0$. This pulse can be used to enable the next cascaded stage (see Figure B).

For conventional operation of 74160, 74161 and 74163, the following transitions should be avoided.

1  HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is LOW, if the count enables and $\overline{MR}$ are HIGH at or before the transition.

For 74163 there is an additional transition to be avoided.

3  LOW-to-HIGH transition on the $\overline{MR}$ input when clock is LOW, if the Enable and $\overline{PE}$ inputs are HIGH at or before the transition.

These restrictions are not applicable to 74LS160A, 74LS161A, 74LS162A and 74LS163A

## LOGIC SYMBOL (IEEE/IEC)
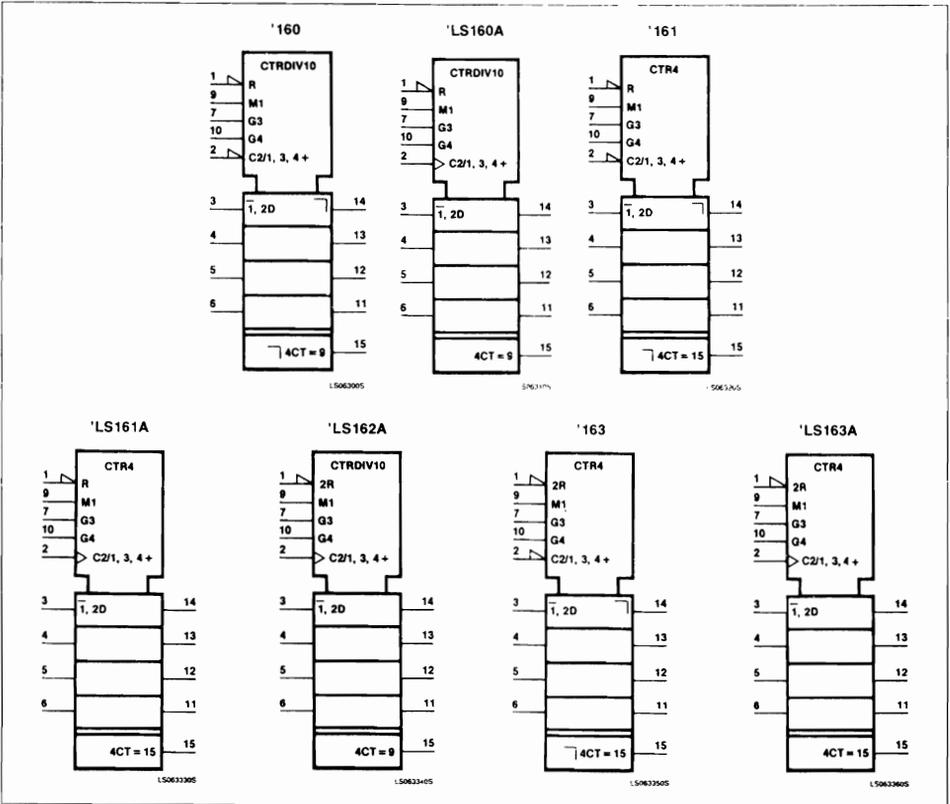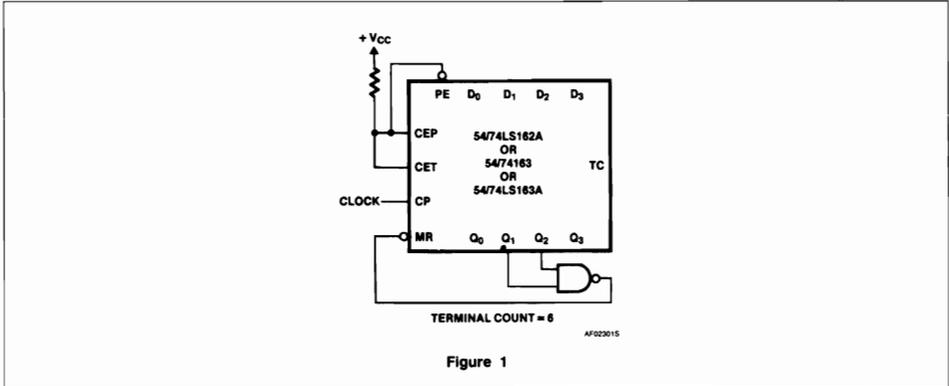
Figure 1
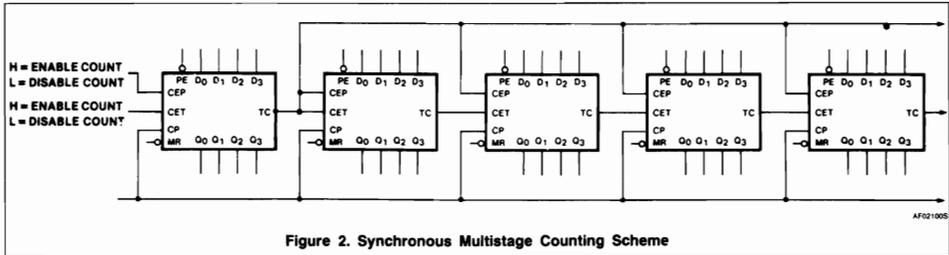


Figure 2. Synchronous Multistage Counting Scheme

## LOGIC DIAGRAM, 74160
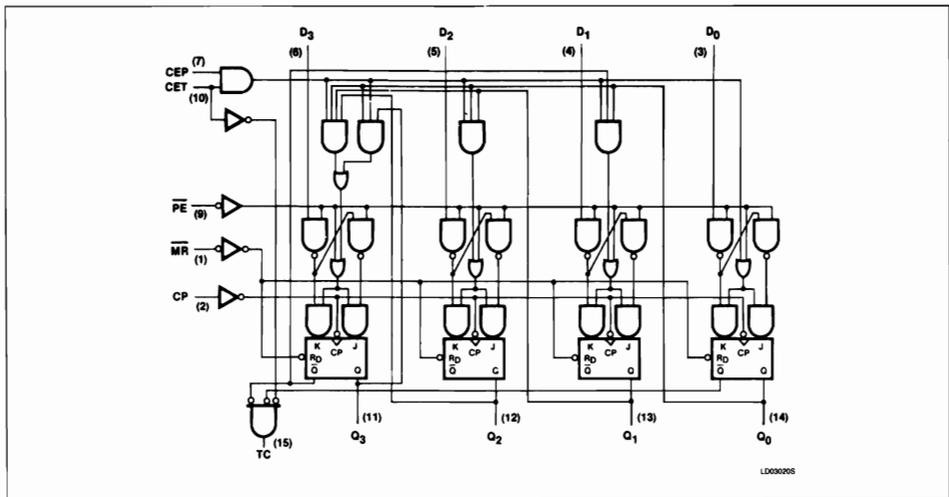


113

# Counters
## 74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

## LOGIC DIAGRAMS

'LS160A



LD03030S

'161



LD03040S

$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers

114
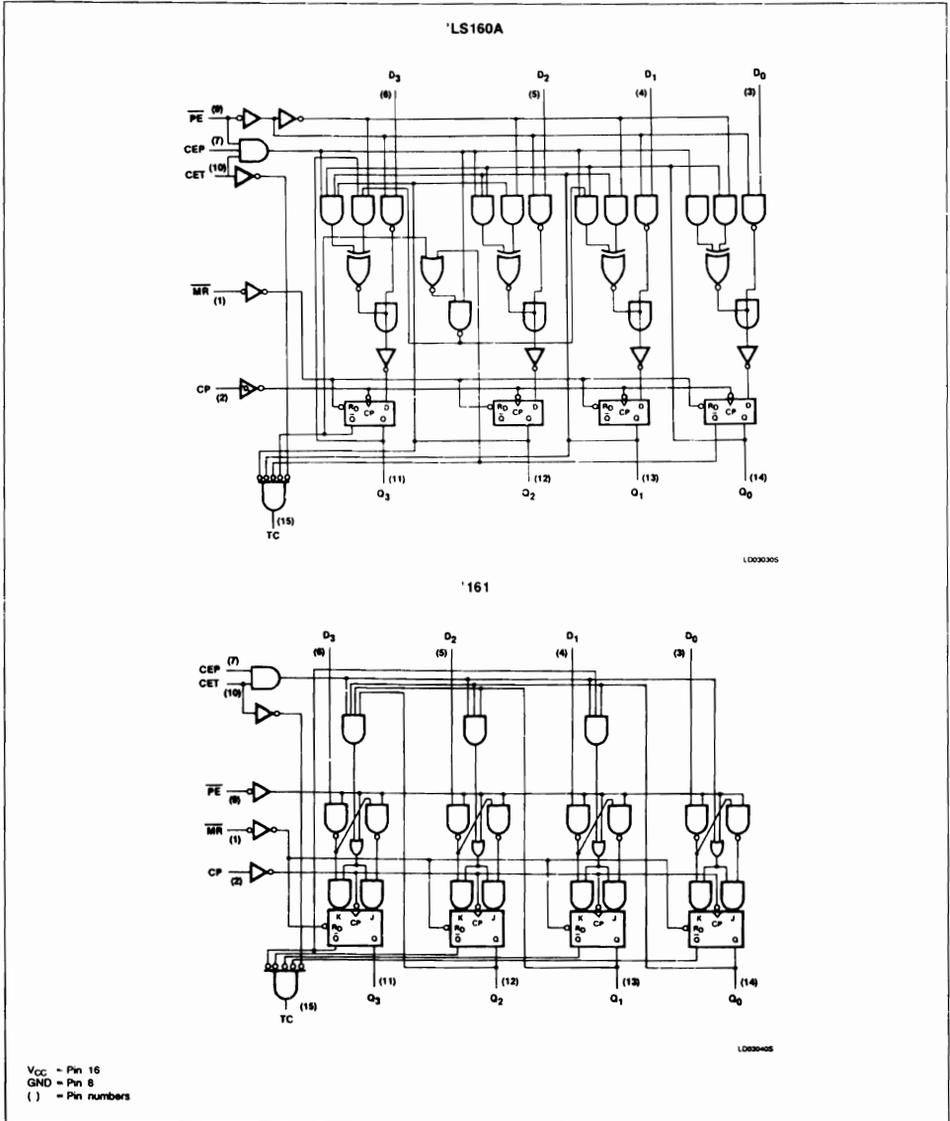
## Counters   74160, 74161, 74163, LS160A, S161A, LS162A, LS163A
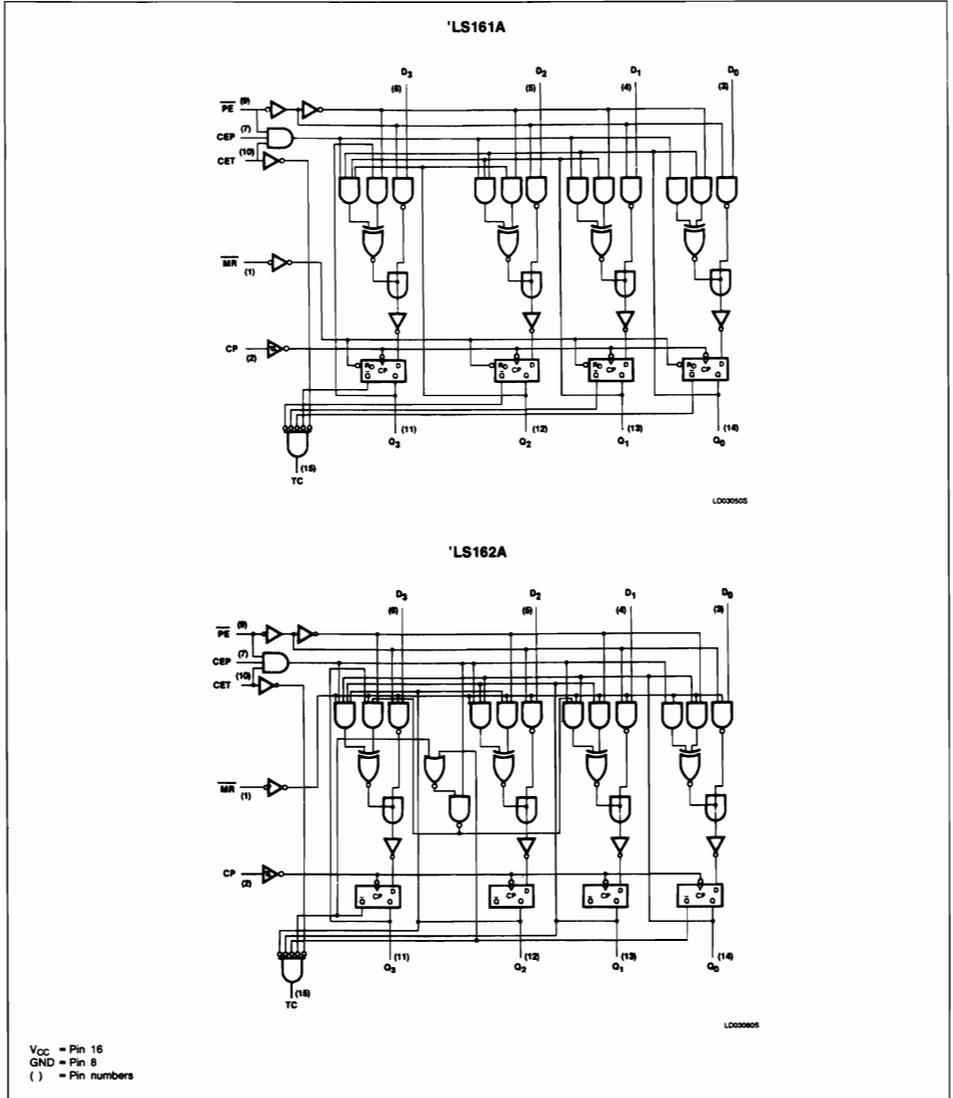
**LOGIC DIAGRAMS**

### 'LS161A



LD03050S

### 'LS162A



LD03080S

V_CC = Pin 16
GND = Pin 8
( ) = Pin numbers

115

# Counters     74160, 74161, 74163, LS160A, LS161A, LS162A, LS163A

## LOGIC DIAGRAMS

'163



LD03070S

'LS163A



LD03080S

V_CC = Pin 16
GND = Pin 8
( ) = Pin numbers

116
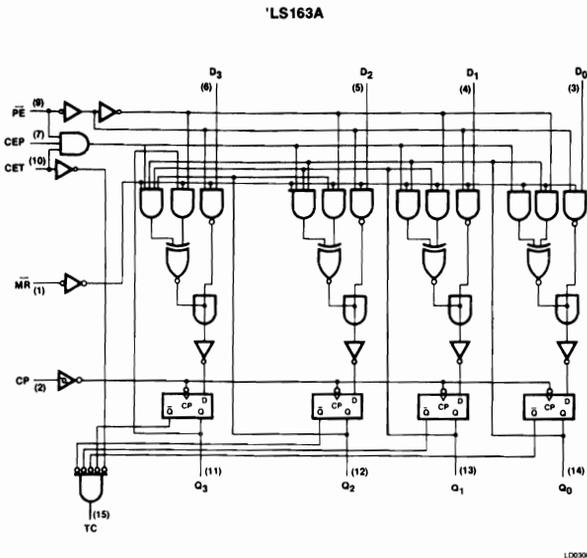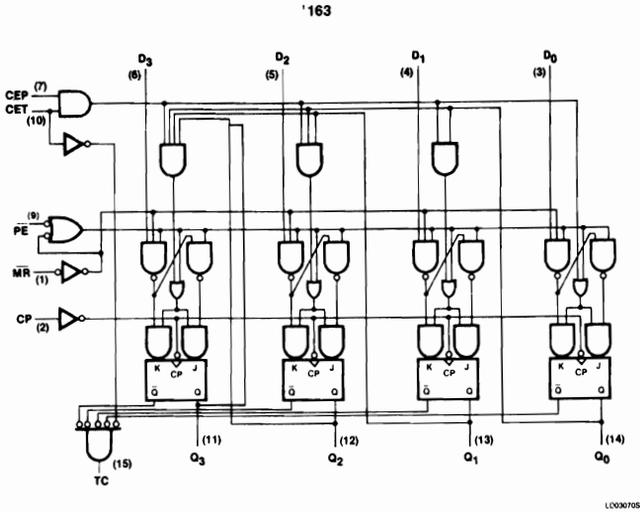
## MODE SELECT — FUNCTION TABLE, '160, '161

| OPERATING MODE | INPUTS | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | CEP | CET | $\overline{PE}$ | $D_n$ | $Q_n$ | TC |
| Reset (clear) | L | X | X | X | X | X | L | L |
| Parallel load | H | ↑ | X | X | I | I | L | L |
| | H | ↑ | X | X | I | h | H | (a) |
| Count | H | ↑ | h | h | h(c) | X | count | (a) |
| Hold (do nothing) | H | X | I(b) | X | h(c) | X | $q_n$ | (a) |
| | H | X | X | I(b) | h(c) | X | $q_n$ | L |

## MODE SELECT — FUNCTION TABLE, '162, '163

| OPERATING MODE | INPUTS | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | CEP | CET | $\overline{PE}$ | $D_n$ | $Q_n$ | TC |
| Reset (clear) | I | ↑ | X | X | X | X | L | L |
| Parallel load | h(f) | ↑ | X | X | I | I | L | L |
| | h(f) | ↑ | X | X | I | h | H | (d) |
| Count | h(f) | ↑ | h | h | h(f) | X | count | (d) |
| Hold (do nothing) | h(f) | X | I(e) | X | h(f) | X | $q_n$ | (d) |
| | h(f) | X | X | I(e) | h(f) | X | $q_n$ | L |

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

**NOTES:**
(a) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for '161 and HLLH for '160).
(b) The HIGH-to-LOW transition of CEP or CET on the 74161 and 74160 should only occur while CP is HIGH for conventional operation.
(c) The LOW-to-HIGH transition of $\overline{PE}$ on the 74161 and 74160 should only occur while CP is HIGH for conventional operation.
(d) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for '162 and HHHH for '163).
(e) The HIGH-to-LOW transition of CEP or CET on the 74163 should only occur while CP is HIGH for conventional operation.
(f) The LOW-to-HIGH transition of $\overline{PE}$ or $\overline{MR}$ on the 74163 should only occur while CP is HIGH for conventional operation.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

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# 74164, LS164
## Shift Registers

**8-Bit Serial-In Parallel-Out Shift Register**
*Product Specification*

**Logic Products**

## FEATURES
- Gated serial Data inputs
- Typical shift frequency of 36MHz
- Asynchronous Master Reset
- Fully buffered Clock and Data inputs

## DESCRIPTION
The '164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs ($D_{sa}$ or $D_{sb}$); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into $Q_0$ the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one set-up time before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74164 | 36MHz | 37mA |
| 74LS164 | 36MHz | 16mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74164N, N74LS164N |
| Plastic SO | N74LS164D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| All | Inputs | 1ul | 1LSul |
| All | Outputs | 5ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and −1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 14
GND = Pin 7

## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



$V_{CC}$ = Pin 14
GND = Pin 7
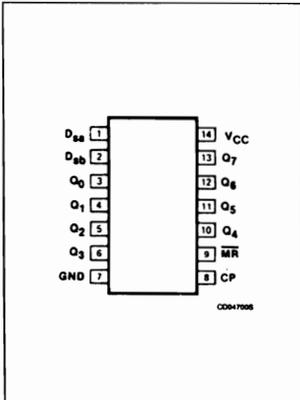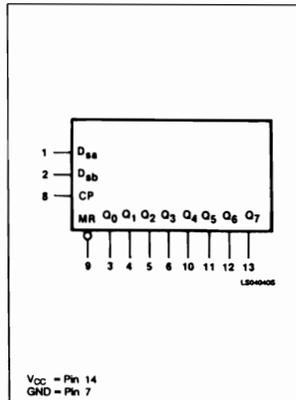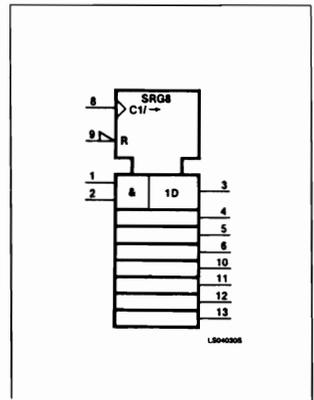
## MODE SELECT — TRUTH TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | $D_{sa}$ | $D_{sb}$ | $Q_0$ | $Q_1$ — | $Q_7$ |
| Reset (clear) | L | X | X | X | L | L — | L |
| Shift | H | ↑ | l | l | L | $q_0$ — | $q_6$ |
| | H | ↑ | l | h | L | $q_0$ — | $q_6$ |
| | H | ↑ | h | l | L | $q_0$ — | $q_6$ |
| | H | ↑ | h | h | H | $q_0$ — | $q_6$ |

H  = HIGH voltage level.
h  = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
L  = LOW voltage level.
l  = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
  = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the
q    LOW-to-HIGH Clock transition.
X  = Don't care.
↑  = LOW-to-HIGH Clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 8 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 74165
## Shift Register

**8-Bit Serial/Parallel-In, Serial-Out Shift Register**
*Product Specification*

**Logic Products**

- Asynchronous 8-bit parallel load
- Synchronous Serial input
- Clock Enable for "do nothing" mode
- See '166 for fully synchronous operation

## DESCRIPTION

The '165 is an 8-bit parallel load or serial-in shift register with complementary Serial outputs ($Q_7$ and $\overline{Q}_7$) available from the last stage. When the Parallel Load ($\overline{PL}$) input is LOW, parallel data from the $D_0 - D_7$ inputs are loaded into the register asynchronously. When the $\overline{PL}$ input is HIGH, data enters the register serially at the $D_S$ input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the $Q_7$ output to the $D_S$ input of the succeeding stage.

The Clock input is a gated-OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation. Also, the CP and $\overline{CE}$ inputs should be LOW before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is released.
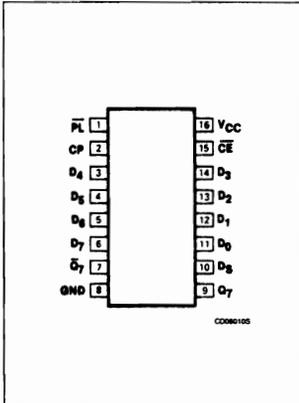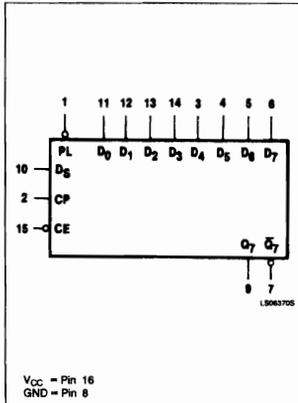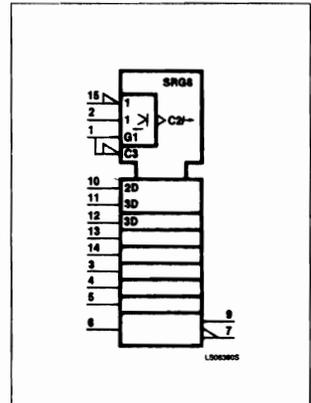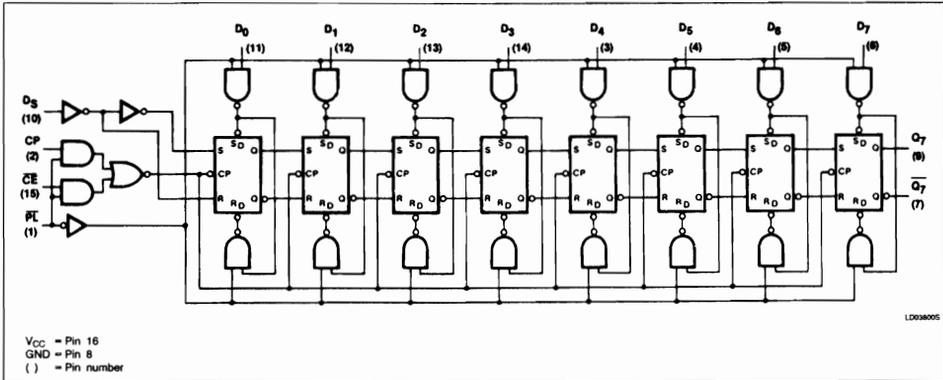
| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74165 | 26MHz | 42mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74165N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| $\overline{PL}$ | Input | 2ul |
| Other | Inputs | 1ul |
| All | Outputs | 10ul |

**NOTE:**
A 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



Vcc = Pin 16
GND = Pin 8
( ) = Pin number

## MODE SELECT — FUNCTION TABLE

| OPERATING MODES | INPUTS | | | | | $Q_n$ REGISTER | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{PL}$ | $\overline{CE}$ | CP | $D_S$ | $D_0 - D_7$ | $Q_0$ | $Q_1 - Q_6$ | $Q_7$ | $\overline{Q}_7$ |
| Parallel load | L | X | X | X | L | L | L – L | L | H |
| | L | X | X | X | H | H | H – H | H | L |
| Serial shift | H | L | ↑ | I | X | L | $q_0 - q_5$ | $q_6$ | $\overline{q}_6$ |
| | H | L | ↑ | h | X | H | $q_0 - q_5$ | $q_6$ | $\overline{q}_6$ |
| Hold "do nothing" | H | H | X | X | X | $q_0$ | $q_1 - q_6$ | $q_7$ | $\overline{q}_7$ |

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$q_n$ = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

# 74166
## Shift Register

**8-Bit Serial/Parallel-In, Serial-Out Shift Register**
*Product Specification*

**Logic Products**

## FEATURES
- Synchronous parallel to serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous Master Reset
- See '165 for asynchronous parallel data load

## DESCRIPTION
The '166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one set-up time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position $Q_0$ from Serial Data Input ($D_S$), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the $Q_7$ output is connected to the $D_S$ input of the succeeding stage.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74166 | 35MHz | 90mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74166N |
| Plastic SO | N74166D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|---|---|---|
| All | Inputs | 1ul |
| $Q_7$ | Output | 10ul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation. A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

## PIN CONFIGURATION
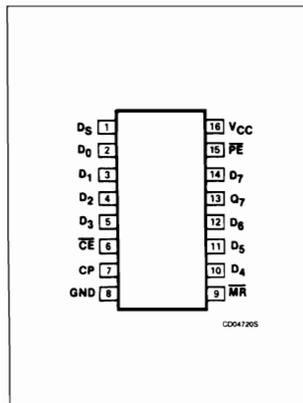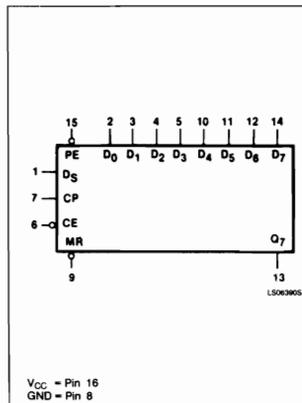


$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



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## LOGIC DIAGRAM



```
( )  = Pin number
Vcc  = Pin 16
GND  = Pin 8
```
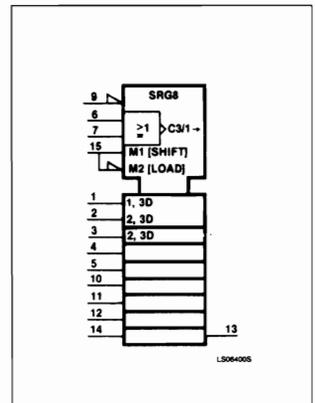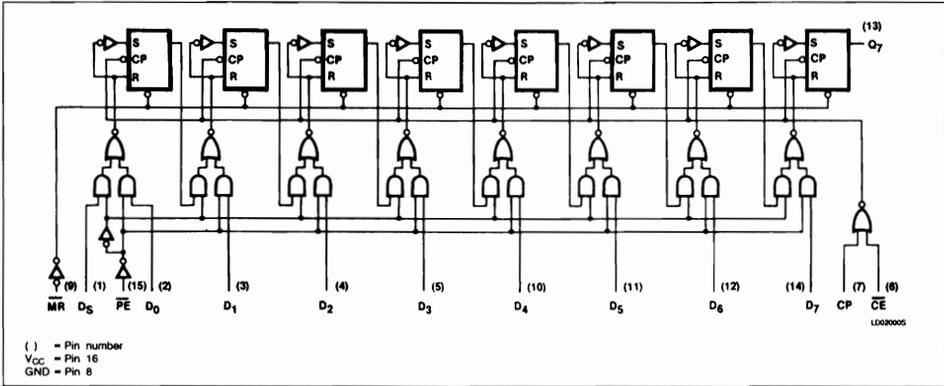
## MODE SELECT — FUNCTION TABLE

| OPERATING MODES | INPUTS | | | | | $Q_n$ REGISTER | | OUTPUT |
|---|---|---|---|---|---|---|---|---|
| | $\overline{PE}$ | $\overline{CE}$ | CP | $D_S$ | $D_0 - D_7$ | $Q_0$ | $Q_1 - Q_6$ | $Q_7$ |
| Parallel load | l | l | ↑ | X | H | L | L–L | L |
| | l | l | ↑ | X | h–h | H | H–H | H |
| Serial shift | h | l | ↑ | l | X–X | L | $q_0$–$q_5$ | $q_6$ |
| | h | l | ↑ | h | X–X | H | $q_0$–$q_5$ | $q_6$ |
| Hold (do nothing) | X | h | X | X | X–X | $q_0$ | $q_1$–$q_6$ | $q_7$ |

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
$q_n$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

## TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES
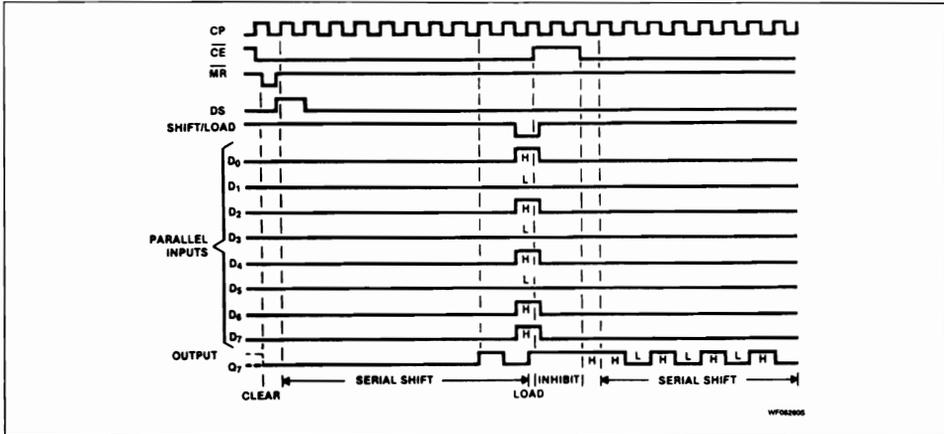
# 74LS168A, 74LS169A, S168A, S169A
## 4-Bit Bidirectional Counters

### 4-Bit Up/Down Synchronous Counter
*Product Specification*

Logic Products

## FEATURES
- **Synchronous counting and loading**
- **Up/down counting**
- **Modulo 16 binary counter — '169A**
- **BCD decade counter — '168A**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**

## DESCRIPTION
The '168A is a synchronous, presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|------|------|
| 74LS168A | 32MHz | 20mA |
| 74S168A | 70MHz | 100mA |
| 74LS169A | 32MHz | 20mA |
| 74S169A | 70MHz | 100mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|------|------|
| Plastic DIP | N74LS168AN, N74S168AN N74LS169AN, N74S169AN |
| Plastic SO | N74LS169AD, N74LS169AD, N74S169AD |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|------|------|------|------|
| $\overline{PE}$ | Input | 1Sul | 2LSul |
| $\overline{CET}$ | Input | 2Sul | 1LSul |
| Other | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 10LSul |

**NOTE:**
Where a 74S unit load (Sul) is understood to be 50$\mu$A $I_{IH}$ and $-2.0$mA $I_{IL}$ and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.
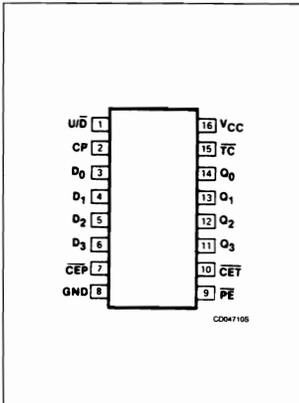
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



124
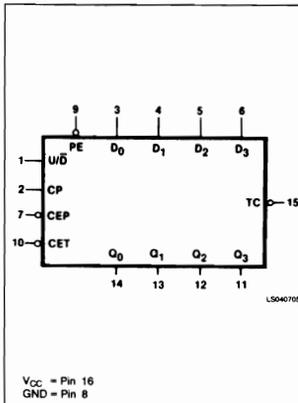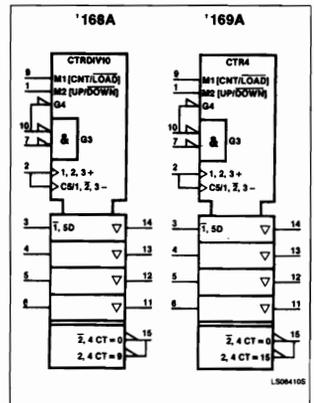
# 4-Bit Bidirectional Counters

# 74LS168A, 74LS169A, S168A, S169A

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the $D_n$ input to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the Up/Down (U/$\overline{D}$) input; a HIGH will cause the

count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET} \cdot \overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a LOW

output pulse with a duration approximately equal to the HIGH level portion of the $Q_0$ output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

The '169A is identical except that it is a Modulo 16 counter.

## LOGIC DIAGRAM, '168A



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers

LD01980S

125

**LOGIC DIAGRAM, '169A**



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers

LD01990S



LEAST SIGNIFICANT
4-BIT COUNTER

MOST SIGNIFICANT
4-BIT COUNTER

BD01810S
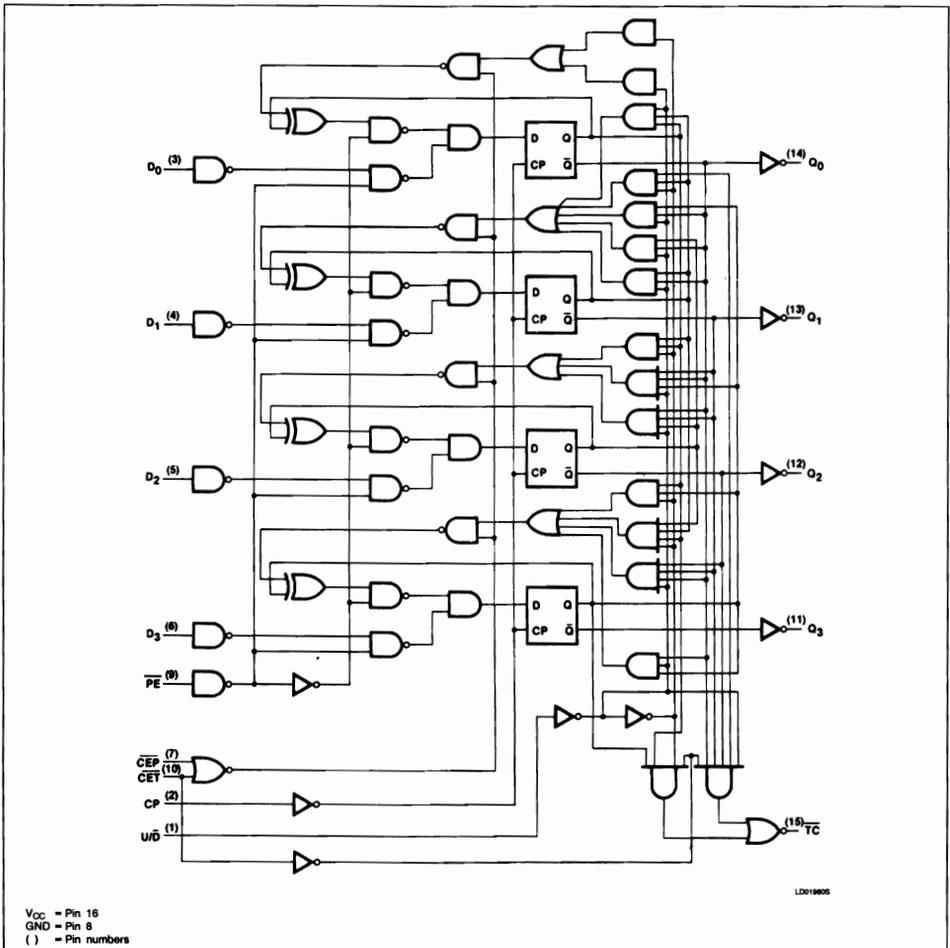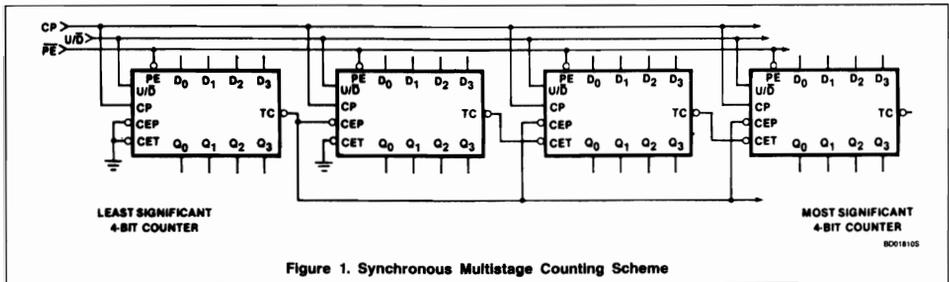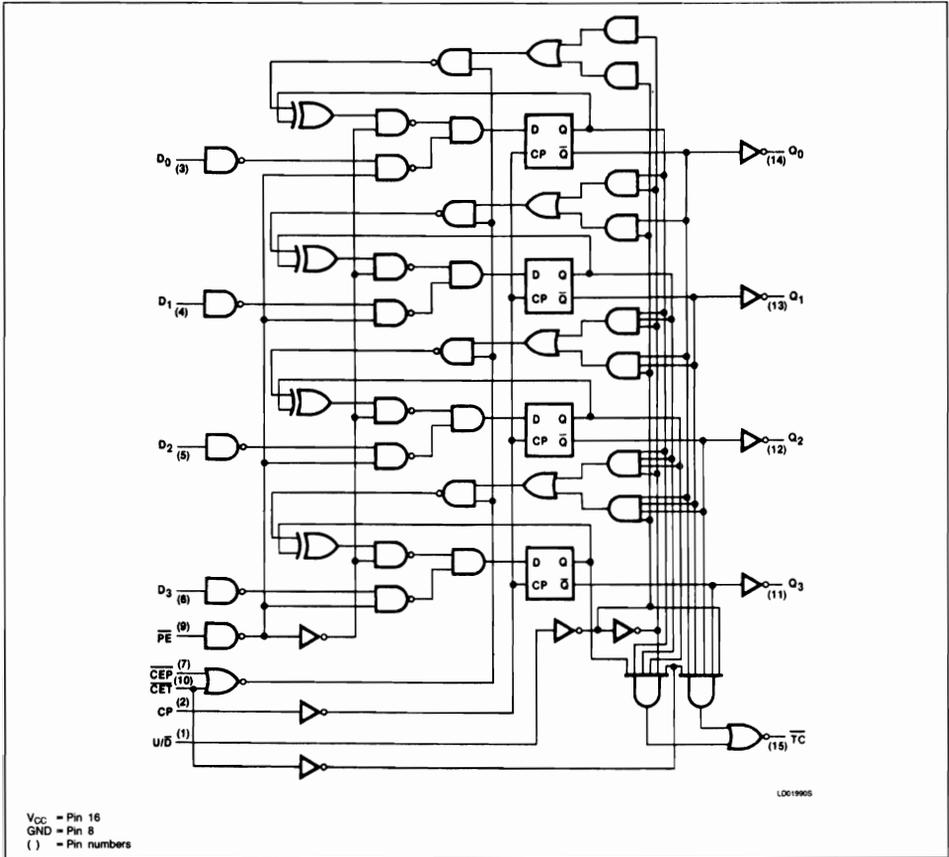
**Figure 1. Synchronous Multistage Counting Scheme**

# 4-Bit Bidirectional Counters

## 74LS168A, 74LS169A, S168A, S169A

## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| | CP | U/$\overline{\text{D}}$ | $\overline{\text{CEP}}$ | $\overline{\text{CET}}$ | $\overline{\text{PE}}$ | $D_n$ | $Q_n$ | $\overline{\text{TC}}$ |
| Parallel Load | ↑ | X | X | X | l | i | L | (1) |
| | ↑ | X | X | X | l | h | H | (1) |
| Count Up | ↑ | h | l | l | h | X | Count Up | (1) |
| Count Down | ↑ | l | l | l | h | X | Count Down | (1) |
| Hold (do nothing) | ↑ | X | h | X | h | X | $q_n$ | (1) |
| | ↑ | X | X | h | h | X | $q_n$ | H |

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
i = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

**NOTE:**
1. The $\overline{\text{TC}}$ is LOW when $\overline{\text{CET}}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169A.
   The $\overline{\text{TC}}$ is LOW when $\overline{\text{CET}}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168A.

## WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the '168A. The operation of the '169A is similar.

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



WF06680S

127
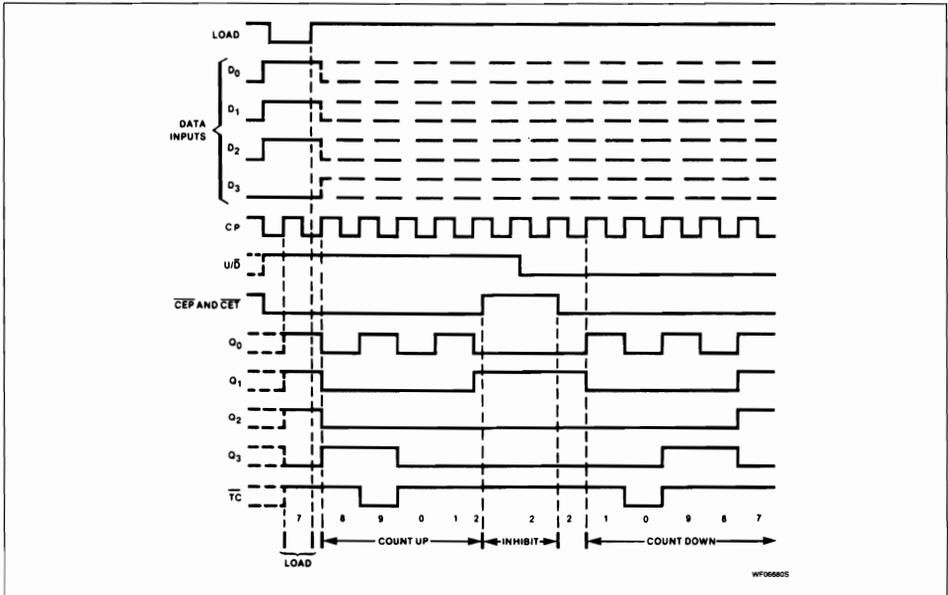
# 74170, LS170
## Register Files

### 4 x 4 Register File (Open Collector)
*Product Specification*

## FEATURES
- Simultaneous and independent Read and Write operations
- Expandable to 1024 words by n-bits
- Open Collector outputs for wired-AND expansion
- See '670 for 3-State output version

## DESCRIPTION
The '170 is a 16-bit register file organized as 4 words of 4 bits each, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs ($W_A$ and $W_B$) determine the location of the stored word. When the Write Enable ($\overline{WE}$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form. Data and Write Address inputs are inhibited when $\overline{WE}$ is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs ($R_A$ and $R_B$). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$)

| TYPE | TYPICAL PROPAGATION DELAY (RE to Q) | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74170 | 10ns ($t_{PLH}$) 20ns ($t_{PHL}$) | 127mA |
| 74LS170 | 20ns ($t_{PLH}$) 20ns ($t_{PHL}$) | 25mA |

### ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74170N, N74LS170N |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| D, $W_A$, $W_B$, $R_A$, $R_B$ | Inputs | 1ul | 1LSul |
| $\overline{WE}$, $\overline{RE}$ | Inputs | 1ul | 2LSul |
| All | Outputs | 10ul | 10LSul |

NOTE:
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$ and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

is LOW. Data outputs are inhibited and remain HIGH when the Read Enable input is HIGH. This permits simultaneous reading and writing, eliminates recovery times, and is limited in speed only by the read time and the write time.

Up to 256 devices can be stacked to increase the word size to 1024 locations by tying the Open Collector outputs together. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

## PIN CONFIGURATION



CD06040S

## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

LS06420S

## LOGIC SYMBOL (IEEE/IEC)



LS06430S
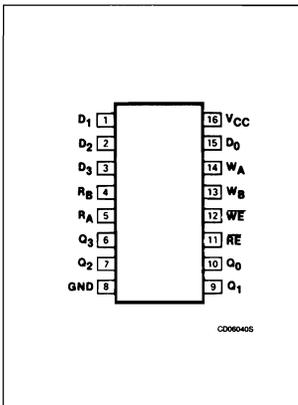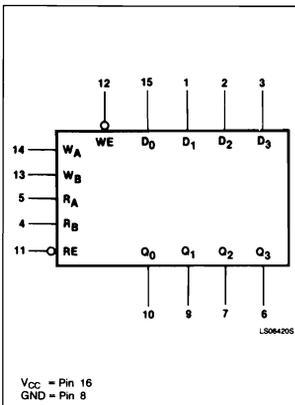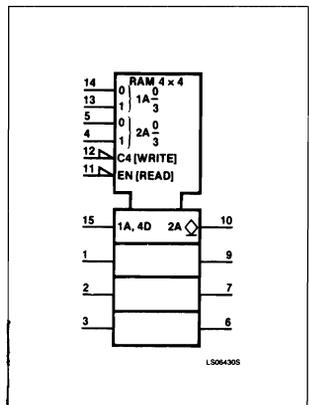
# 74173, LS173
# Flip-Flops

**Quad D-Type Flip-Flop With 3-State Outputs**
*Product Specification*

**Logic Products**

## FEATURES
- Edge-triggered D-type register
- Gated input enable for hold "do nothing" mode
- 3-State output buffers
- Gated output enable control
- Pin compatible with the 8T10 and DM8551

## DESCRIPTION
The '173 is a 4-bit parallel load register with clock enable control, 3-State buffered outputs and master reset. When the two Clock Enable ($\bar{E}_1$ and $\bar{E}_2$) inputs are LOW, the data on the D inputs is loaded into the register synchronously with the LOW-to-HIGH Clock (CP) transition. When one or both $\bar{E}$ inputs are HIGH one set-up time before the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and Clock Enable inputs are fully edge triggered and must be stable only one set-up time before the LOW-to-HIGH clock transition.

The Master Reset (MR) is an active HIGH asynchronous input. When the MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74173 | 35MHz | 50mA |
| 74LS173 | 50MHz | 20mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74173N, N74LS173N |
| Plastic SO-16 | N74LS173D |
| Plastic SOL-16 | CD7186D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| All | Inputs | 1ul | 1LSul |
| All | Outputs | 10ul | 30LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and – 1.6mA $I_{IL}$ and a 74LS unit load (LSul) is 20µA $I_{IH}$ and –0.4mA $I_{IL}$.

The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_1$ and $\overline{OE}_2$) inputs are LOW, the data in the register is presented at the Q outputs. When one or both $\overline{OE}$ inputs is HIGH, the outputs are forced to a HIGH impedance "off" state. The 3-State output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

## PIN CONFIGURATION

| | |
|---|---|
| $\overline{OE}_1$ [1] | [16] $V_{CC}$ |
| $\overline{OE}_2$ [2] | [15] MR |
| $Q_0$ [3] | [14] $D_0$ |
| $Q_1$ [4] | [13] $D_1$ |
| $Q_2$ [5] | [12] $D_2$ |
| $Q_3$ [6] | [11] $D_3$ |
| CP [7] | [10] $\bar{E}_2$ |
| GND [8] | [9] $\bar{E}_1$ |

CD08060S

## LOGIC SYMBOL

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)

129
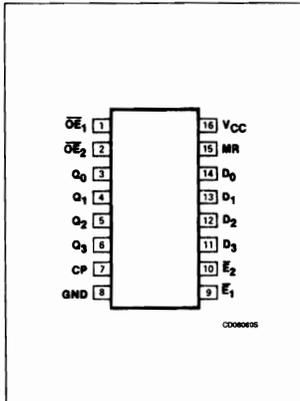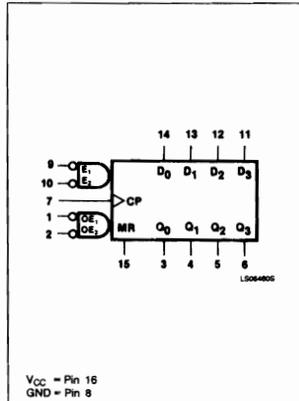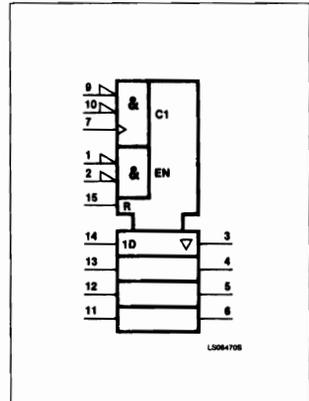
# 74173, LS173

## LOGIC DIAGRAM



V_CC = Pin 16
GND = Pin 8
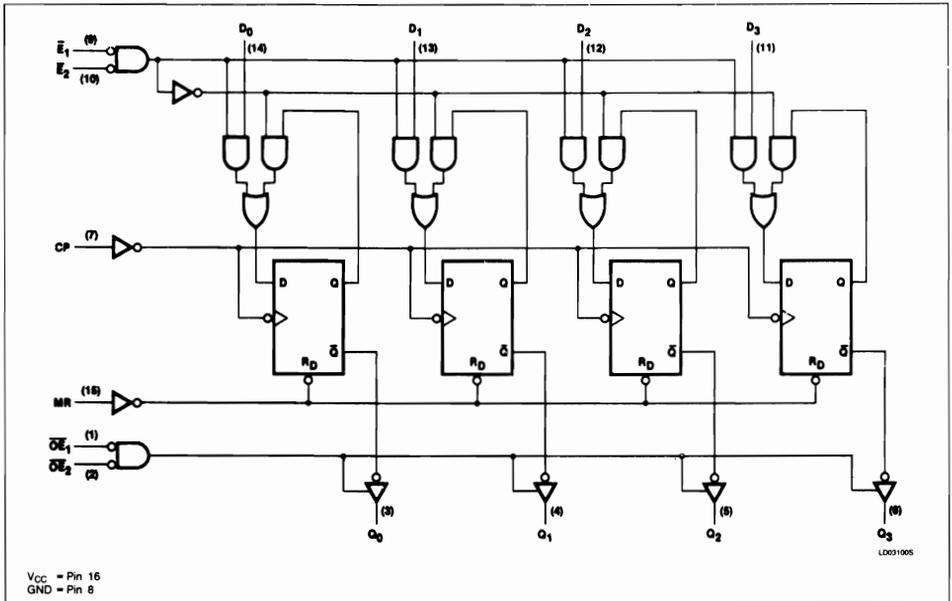
## MODE SELECT — FUNCTiON TABLE

| REGISTER OPERATING MODES | INPUTS | | | | | OUTPUTS |
|---|---|---|---|---|---|---|
| | MR | CP | $\bar{E}_1$ | $\bar{E}_2$ | $D_n$ | $Q_n$ (Register) |
| Reset (clear) | H | X | X | X | X | L |
| Parallel load | L | ↑ | l | l | l | L |
| | L | ↑ | l | l | h | H |
| Hold (no change) | L | X | h | X | X | $q_n$ |
| | L | X | X | h | X | $q_n$ |

| 3-STATE BUFFER OPERATING MODES | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $Q_n$ (Register) | $\overline{OE}_1$ | $\overline{OE}_2$ | $Q_0$, $Q_1$, $Q_2$, $Q_3$ |
| Read | L | L | L | L |
| | H | L | L | H |
| Disabled | X | H | X | (Z) |
| | X | X | H | (Z) |

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$q_n$ = Lower case letters indicate the state of the referenced input (or output) on set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
(Z) = HIGH impedance "off" state.
↑ = LOW-to-HIGH clock transition.

# 74174, LS174, S174
# Flip-Flops

**Hex D Flip-Flops**
*Product Specification*

## FEATURES
- Six edge-triggered D-type flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

## DESCRIPTION
The '174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74174 | 35MHz | 45mA |
| 74LS174 | 40MHz | 16mA |
| 74S174 | 110MHz | 90mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74174N, N74LS174N, N74S174N |
| Plastic SO-16 | N74LS174D, N74S174D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| All | Inputs | 1ul | 1Sul | 1LSul |
| $Q_0 - Q_5$ | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$, a 74S unit load (Sul) is $50\mu A$ $I_{IH}$ and $-2.0mA$ $I_{IL}$, and 74LS unit load (LSul) is $20\mu A$ $I_{IH}$ and $-0.4mA$ $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



131
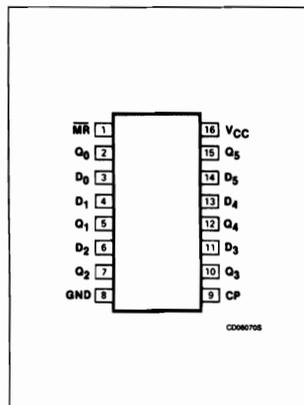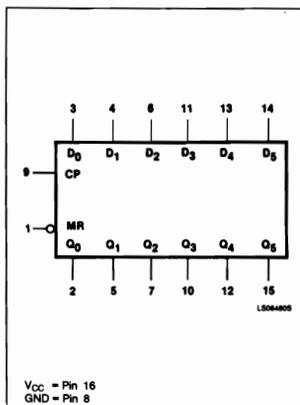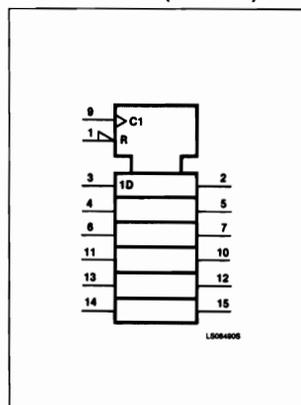
# 74174, LS174, S174

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin Numbers
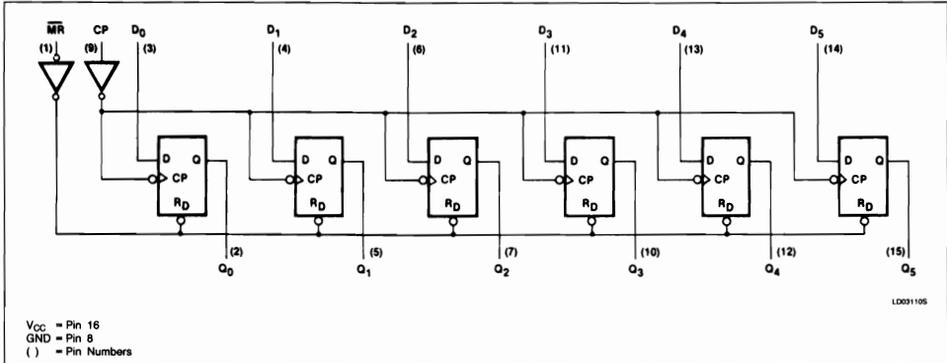
## FUNCTION TABLE

| OPERATING MODE | INPUTS | | | OUTPUTS |
|---|---|---|---|---|
| | $\overline{MR}$ | CP | $D_n$ | $Q_n$ |
| Reset (clear) | L | X | X | L |
| Load "1" | H | ↑ | h | H |
| Load "0" | H | ↑ | l | L |

H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | 74S | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74 | | | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | | | −400 | | | −1000 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | 0 | | 70 | °C |

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# 74175, LS175, S175
# Flip-Flops

**Quad D Flip-Flop**
*Product Specification*

## FEATURES
- Four edge-triggered D flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

## DESCRIPTION
The '175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|------|------|
| 74175 | 35MHz | 30mA |
| 74LS175 | 40MHz | 11mA |
| 74S175 | 110MHz | 60mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|------|
| Plastic DIP | N74175N, N74LS175N, N74S175N |
| Plastic SO-16 | N74LS175D, N74S175D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|------|------|------|------|------|
| All | Inputs | 1ul | 1Sul | 1LSul |
| All | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be $40\mu A$ $I_{IH}$ and $-1.6mA$ $I_{IL}$, a 74S unit load (Sul) is $50\mu A$ $I_{IH}$ and $-2.0mA$ $I_{IL}$, and a 74LS unit load (LSul) is $20\mu A$ $I_{IH}$ and $-0.4mA$ $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin number

## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | OUTPUTS | |
|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | $D_n$ | $Q_n$ | $\overline{Q}_n$ |
| Reset (clear) | L | X | X | L | H |
| Load "1" | H | ↑ | h | H | L |
| Load "0" | H | ↑ | l | L | H |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74 | 74LS | 74S | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | 74 | | | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ HIGH-level input voltage | 2.0 | | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ LOW-level input voltage | | | +0.8 | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ Input clamp current | | | −12 | | | −18 | | | −18 | mA |
| $I_{OH}$ HIGH-level output current | | | −800 | | | −400 | | | −1000 | μA |
| $I_{OL}$ LOW-level output current | | | 16 | | | 8 | | | 20 | mA |
| $T_A$ Operating free-air temperature | 0 | | 70 | 0 | | 70 | 0 | | 70 | °C |

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# 74180
# Parity Generator/Checker

**9-Bit Odd/Even Parity Generator/Checker**
*Product Specification*

## FEATURES
- **Word length easily expanded by cascading**
- **Generate even or odd parity**
- **Checks for parity errors**
- **See '280 for faster parity checker**

## DESCRIPTION
The '180 is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even and Odd parity enable inputs and parity outputs are available for generating or checking parity on 8-bits.

True active-HIGH or true active-LOW parity can be generated at both the Even and Odd outputs. True active-HIGH parity is established with Even Parity enable input ($P_E$) set HIGH and the Odd Parity enable input ($P_O$) set LOW. True active-LOW parity is established when $P_E$ is LOW and $P_O$ is HIGH. When both enable inputs are at the same logic level, both outputs will be forced to the opposite logic level.

Parity checking of a 9-bit word (8 bits plus parity) is possible by using the two enable inputs plus an inverter as the ninth data input. To check for true active-HIGH parity, the ninth data input is tied to the $P_O$ input and an inverter is connected between the $P_O$ and $P_E$ inputs. To check for true active-LOW parity, the ninth data input is tied to the $P_E$ input and an inverter is connected between the $P_E$ and $P_O$ inputs.

Expansion to larger word sizes is accomplished by serially cascading the '180 in 8-bit increments. The Even and Odd parity outputs of the first stage are connected to the corresponding $P_E$ and $P_O$ inputs, respectively, of the succeeding stage.

| TYPE | TYPICAL PROPAGATION DELAY, $P_O = 0V$ | TYPICAL SUPPLY CURRENT |
|------|------|------|
| 74180 | 36ns | 34mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|------|------|
| Plastic DIP | N74180N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|------|------|
| $I_0 - I_7$ | Data inputs | 1ul |
| $P_E$, $P_O$ | Parity inputs | 2ul |
| $\Sigma_E$, $\Sigma_O$ | Parity outputs | 10ul |

**NOTE:**
A 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$.

## PIN CONFIGURATION



| | |
|--|--|
| $I_6$ 1 | 14 $V_{CC}$ |
| $I_7$ 2 | 13 $I_5$ |
| $P_E$ 3 | 12 $I_4$ |
| $P_O$ 4 | 11 $I_3$ |
| $\Sigma_E$ 5 | 10 $I_2$ |
| $\Sigma_O$ 6 | 9 $I_1$ |
| GND 7 | 8 $I_0$ |

CD06080S

## LOGIC SYMBOL



$V_{CC}$ = Pin 14
GND = Pin 7

LS06500S

## LOGIC SYMBOL (IEEE/IEC)



LS06510S

## LOGIC DIAGRAM



```
I₀ (8)
I₁ (9)

I₂ (10)
I₃ (11)

I₄ (12)
I₅ (13)

I₆ (1)
I₇ (2)

Pₒ (4)
Pₑ (3)
```

(5) Σ_E

(6) Σ_O

( ) = Pin Numbers
$V_{CC}$ = Pin 14
GND = Pin 7

LD03120S

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| Number of HIGH Data Inputs ($I_0 - I_7$) | $P_E$ | $P_O$ | $\Sigma_E$ | $\Sigma_O$ |
| Even | H | L | H | L |
| Odd | H | L | L | H |
| Even | L | H | L | H |
| Odd | L | H | H | L |
| X | H | H | L | L |
| X | L | L | H | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

# 74181, LS181, S181
# Arithmetic Logic Units

**4-Bit Arithmetic Logic Unit**
*Product Specification*

**Logic Products**

## FEATURES
- **Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full lookahead carry for high-speed arithmetic operation on long words**

## DESCRIPTION
The '181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74181 | 22ns | 91mA |
| 74LS181 | 22ns | 21mA |
| 74S181 | 11ns | 120mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74181N, N74LS181N, N74S181N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|---|---|---|---|---|
| Mode | Input | 1ul | 1Sul | 1LSul |
| $\overline{A}$ or $\overline{B}$ | Inputs | 3ul | 3Sul | 3LSul |
| S | Inputs | 4ul | 4Sul | 4LSul |
| Carry | Input | 5ul | 5Sul | 5LSul |
| $F_0 - F_3$, = B, $C_{n+4}$ | Outputs | 10ul | 10Sul | 10LSul |
| $\overline{G}$ | Output | 10ul | 10Sul | 40LSul |
| $\overline{P}$ | Output | 10ul | 10Sul | 20LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD04240S

## LOGIC SYMBOL



LS03370S

$V_{CC}$ = Pin 24
GND = Pin 12

## LOGIC SYMBOL (IEEE/IEC)



LS06520S

137
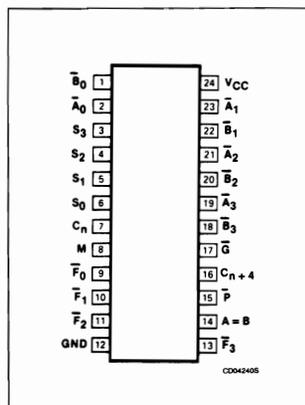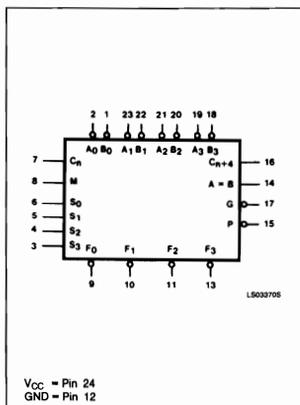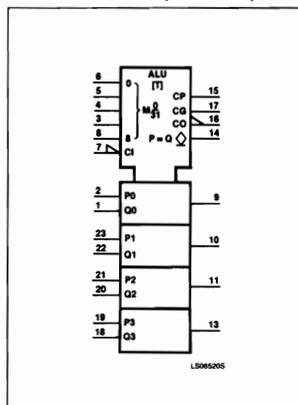
# Arithmetic Logic Units

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the $C_{n+4}$ output, or carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output ($C_{n+4}$) signal to the Carry input ($C_n$) of the next unit. For high-speed operation the device is used in conjunction with the

'182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the $C_{n+4}$ signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An

incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

## LOGIC DIAGRAM



Vcc = Pin 24
GND = Pin 12
( ) = Pin Numbers

LD031305

138
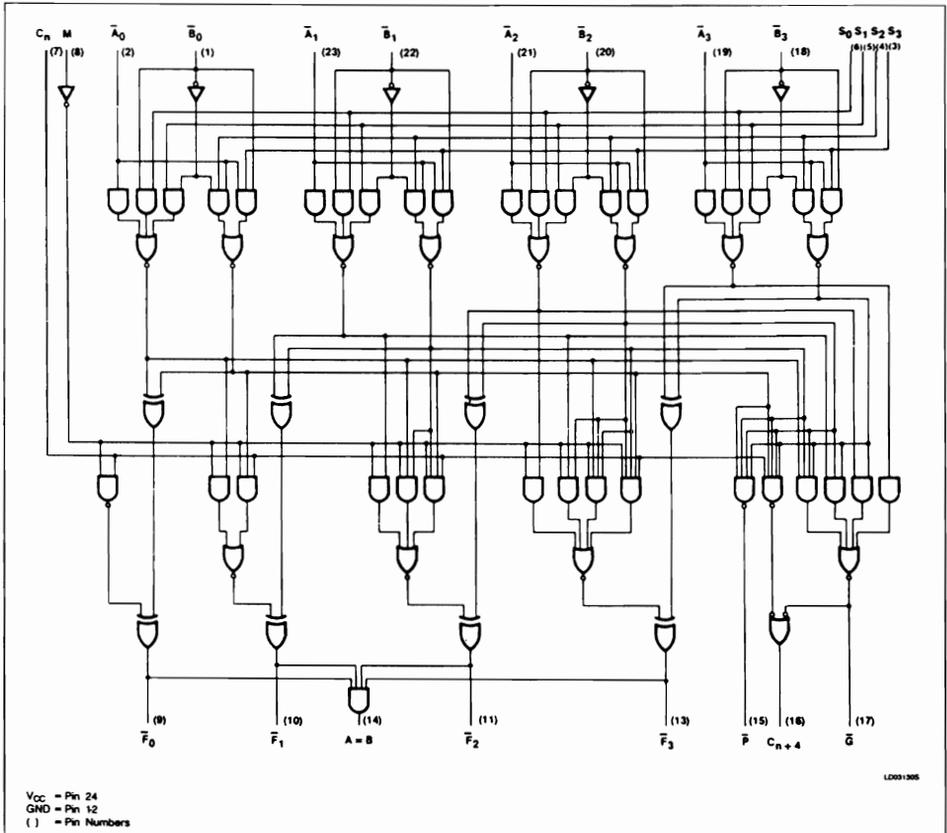
## MODE SELECT — FUNCTION TABLE

| MODE SELECT INPUTS | | | | ACTIVE HIGH INPUTS & OUTPUTS | |
|---|---|---|---|---|---|
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | Logic (M = H) | Arithmetic** (M = L) ($C_n$ = H) |
| L | L | L | L | $\overline{A}$ | A |
| L | L | L | H | $\overline{A + B}$ | A + B |
| L | L | H | L | $\overline{A}B$ | $A + \overline{B}$ |
| L | L | H | H | Logical 0 | minus 1 |
| L | H | L | L | $\overline{A\overline{B}}$ | A plus $A\overline{B}$ |
| L | H | L | H | $\overline{B}$ | (A + B) plus $A\overline{B}$ |
| L | H | H | L | A • B | A minus B minus 1 |
| L | H | H | H | $A\overline{B}$ | AB minus 1 |
| H | L | L | L | $\overline{A} + B$ | A plus AB |
| H | L | L | H | $A \bullet \overline{B}$ | A plus B |
| H | L | H | L | B | $(A + \overline{B})$ plus AB |
| H | L | H | H | AB | AB minus 1 |
| H | H | L | L | Logical 1 | A plus A* |
| H | H | L | H | $A + \overline{B}$ | (A + B) plus A |
| H | H | H | L | A + B | $(A + \overline{B})$ plus A |
| H | H | H | H | A | A minus 1 |

| MODE SELECT INPUTS | | | | ACTIVE LOW INPUTS & OUTPUTS | |
|---|---|---|---|---|---|
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | Logic (M = H) | Arithmetic** (M = L) ($C_n$ = L) |
| L | L | L | L | $\overline{A}$ | A minus 1 |
| L | L | L | H | $\overline{AB}$ | AB minus 1 |
| L | L | H | L | $\overline{A} + B$ | $A\overline{B}$ minus 1 |
| L | L | H | H | Logical 1 | minus 1 |
| L | H | L | L | $\overline{A + B}$ | A plus $(A + \overline{B})$ |
| L | H | L | H | $\overline{B}$ | AB plus $(A + \overline{B})$ |
| L | H | H | L | $\overline{A \bullet B}$ | A minus B minus 1 |
| L | H | H | H | $A + \overline{B}$ | $A + \overline{B}$ |
| H | L | L | L | $\overline{A}B$ | A plus (A + B) |
| H | L | L | H | $\overline{A \bullet B}$ | A plus B |
| H | L | H | L | B | $A\overline{B}$ (A + B) |
| H | L | H | H | A + B | A + B |
| H | H | L | L | Logical 0 | A plus A* |
| H | H | L | H | $A\overline{B}$ | AB plus A |
| H | H | H | L | AB | $A\overline{B}$ plus A |
| H | H | H | H | A | A |

L = LOW voltage
H = HIGH voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.



**Active High Operands**



**Active Low Operands**

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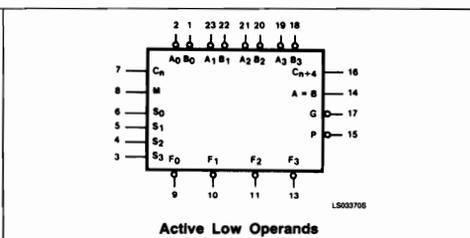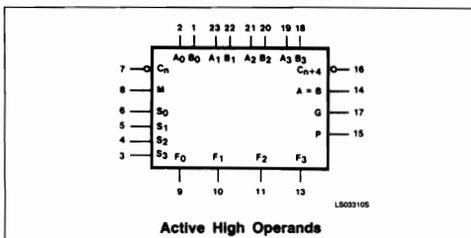
# 74S182
## Carry Generator

**Lookahead Carry Generator**
*Product Specification*

**Logic Products**

## FEATURES
- Provides carry lookahead across a group of four ALU's
- Multi-level lookahead for high-speed arithmetic operation over long word lengths

## DESCRIPTION
The '182 carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH Carry input ($C_n$) and provides anticipated active HIGH carries ($C_{n+x}$, $C_{n+y}$, $C_{n+z}$) across four groups of binary adders. The '182 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|--------------------------------|
| 74S182 | 5.8ns | 69mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|-----------------------------------------------------------------|
| Plastic DIP | N74S182N |
| Plastic SO-16 | N74S182D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S |
|------|-------------|-----|
| $C_n$ | Input | 1Sul |
| $\overline{P}_3$ | Input | 2Sul |
| $\overline{P}_2$ | Input | 3Sul |
| $\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$ | Inputs | 4Sul |
| $\overline{G}_0$, $\overline{G}_2$ | Inputs | 7Sul |
| $\overline{G}_1$ | Input | 8Sul |
| All | Outputs | 10Sul |

**NOTE:**
A 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and −2.0mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin Numbers
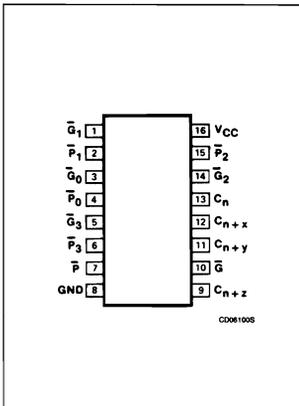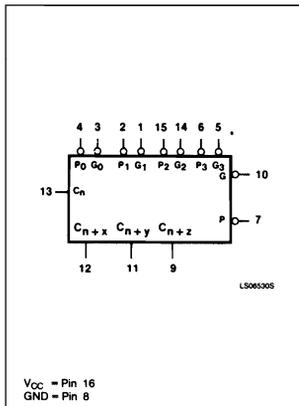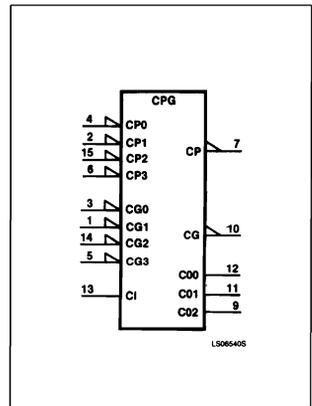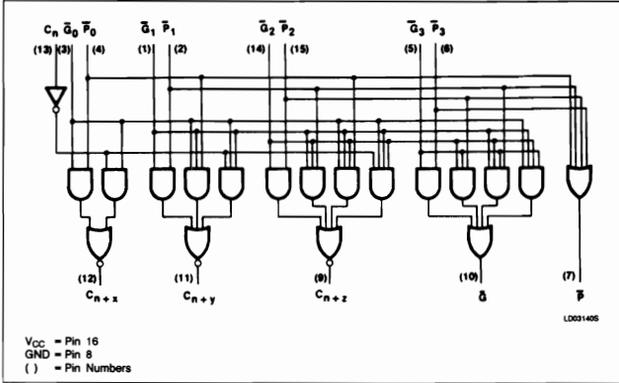
The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 = P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0$$

$$\overline{G} = \overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$$

$$\overline{P} = \overline{P_3 P_2 P_1 P_0}$$

The '182 can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

## FUNCTION TABLE

| INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $C_n$ | $\overline{G}_0$ | $\overline{P}_0$ | $\overline{G}_1$ | $\overline{P}_1$ | $\overline{G}_2$ | $\overline{P}_2$ | $\overline{G}_3$ | $\overline{P}_3$ | $C_{n+x}$ | $C_{n+y}$ | $C_{n+z}$ | $\overline{G}$ | $\overline{P}$ |
| X | H | H | | | | | | | L | | | | |
| L | H | X | | | | | | | L | | | | |
| X | L | X | | | | | | | H | | | | |
| H | X | L | | | | | | | H | | | | |
| X | X | X | H | H | | | | | | L | | | |
| X | H | H | H | X | | | | | | L | | | |
| L | H | X | H | X | | | | | | L | | | |
| X | X | X | L | X | | | | | | H | | | |
| X | L | X | X | L | | | | | | H | | | |
| H | X | L | X | L | | | | | | H | | | |
| X | X | X | X | X | H | H | | | | | L | | |
| X | X | X | H | H | H | X | | | | | L | | |
| X | H | H | H | X | H | X | | | | | L | | |
| L | H | X | H | X | H | X | | | | | L | | |
| X | X | X | X | X | L | X | | | | | H | | |
| X | X | X | L | X | X | L | | | | | H | | |
| X | L | X | X | L | X | L | | | | | H | | |
| H | X | L | X | L | X | L | | | | | H | | |
| | X | | X | X | X | X | H | H | | | | H | |
| | X | | X | X | H | H | H | X | | | | H | |
| | X | | H | H | H | X | H | X | | | | H | |
| | H | | H | H | X | H | X | X | | | | H | |
| | X | | X | X | X | X | L | X | | | | L | |
| | X | | X | X | L | X | X | L | | | | L | |
| | X | | L | X | X | L | X | L | | | | L | |
| | L | | X | L | X | L | X | L | | | | L | |
| | | H | | X | | X | | X | | | | | H |
| | | X | | H | | X | | X | | | | | H |
| | | X | | X | | H | | X | | | | | H |
| | | X | | X | | X | | H | | | | | H |
| | | L | | L | | L | | L | | | | | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

# 74190, 191, LS191
## Counters

'190 Presettable BCD/Decade Up/Down Counter
'191 Presettable 4-Bit Binary Up/Down Counter
*Product Specification*

**Logic Products**

## FEATURES
- Synchronous, reversible counting
- BCD/decade—'190
  4-bit binary—'191
- Synchronous, reversible counting
- Asynchronous parallel load capability
- Count enable control for synchronous expansion
- Single Up/Down control input

## DESCRIPTION
The '190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The '191 is similar, but is a 4-bit binary counter.

| TYPE | TYPICAL f$_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|-----------|---------------------------------|
| 74190 | 25MHz | 65mA |
| 74191 | 25MHz | 65mA |
| 74LS191 | 25MHz | 20mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE V$_{CC}$ = 5V ±5%; T$_A$ = 0°C to +70°C |
|----------|------------------------------------------------|
| Plastic DIP | N74190N, N74191N, N74LS191N |
| Plastic SOL-16 | N74LS191D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S |
|------|-------------|-----|-----|
| $\overline{CE}$ | Input | 3ul | 3LSul |
| Other | Inputs | 1ul | 1LSul |
| All | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA I$_{IH}$ and – 1.6mA I$_{IL}$, and a 74LS unit load (LSul) is 20µA I$_{IH}$ and – 0.4mA I$_{IL}$.

## PIN CONFIGURATION



CD06110S

## LOGIC SYMBOL



LS06550S

V$_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



LS06560S

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# Counters

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the Clock input. The Up/Down ($\overline{U}/D$) input signal determines the direction of counting as indicated in the Mode Select Table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}/D$ input should be changed only when either $\overline{CE}$ or CP is HIGH.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode for 74190,

and reaches "15" in the count-up mode for 74191/74LS191. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}/D$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the RC follows the Clock Pulse (CP) delayed by two gate delays. The $\overline{RC}$ output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it

ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure B shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The LOW state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

In Figure C, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure A and B does not apply.



Figure 1. N-Stage Counter Using Ripple Clock



Figure 2. Synchronous N-Stage Counter Using Ripple Carry Borrow

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Figure 3. Synchronous N-Stage Counter With Parallel Gated Carry Borrow

## LOGIC DIAGRAM '190
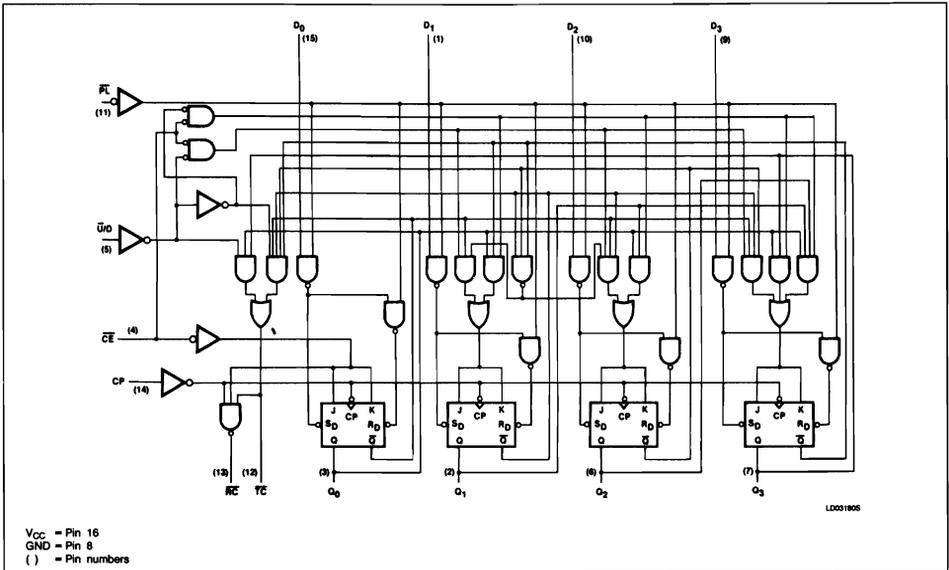


$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers

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# Counters

## LOGIC DIAGRAM '191



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers

LD03190S
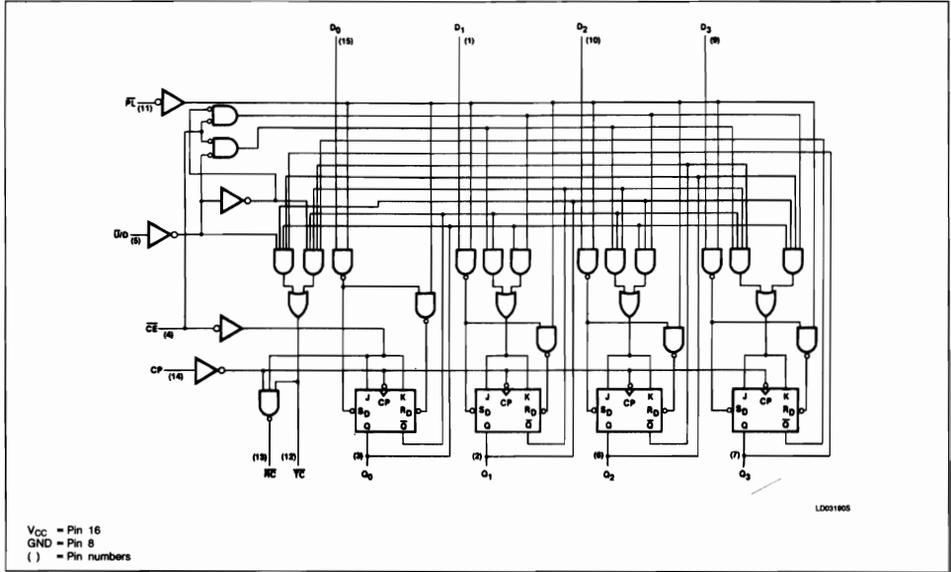
## MODE SELECT — FUNCTION TABLE, '190, '191

| OPERATING MODE | INPUTS | | | | | OUTPUTS |
|---|---|---|---|---|---|---|
| | $\overline{PL}$ | $\overline{U}/D$ | $\overline{CE}$ | CP | $D_n$ | $Q_n$ |
| Parallel load | L | X | X | X | L | L |
| | L | X | X | X | H | H |
| Count up | H | L | I | ↑ | X | count up |
| Count down | H | H | I | ↑ | X | count down |
| Hold "do nothing" | H | X | H | X | X | no change |

## TC AND $\overline{RC}$ FUNCTION TABLE, '190

| INPUTS | | | TERMINAL COUNT STATE | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| $\overline{U}/D$ | $\overline{CE}$ | CP | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | TC | $\overline{RC}$ |
| H | H | X | H | X | X | H | L | H |
| L | H | X | H | X | X | H | H | H |
| L | L | ⊔ | H | X | X | H | ⌐ | ⊔ |
| L | H | X | L | L | L | L | L | H |
| H | H | X | L | L | L | L | H | H |
| H | L | ⊔ | L | L | L | L | ⌐ | ⊔ |

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## TC AND $\overline{RC}$ FUNCTION TABLE, '191

| INPUTS | | | TERMINAL COUNT STATE | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| $\overline{U}/D$ | $\overline{CE}$ | CP | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | TC | $\overline{RC}$ |
| H | H | X | H | H | H | H | L | H |
| L | H | X | H | H | H | H | H | H |
| L | L | ⊔ | H | H | H | H | ⌐ | ⊔ |
| L | H | X | L | L | L | L | L | H |
| H | H | X | L | L | L | L | H | H |
| H | L | ⊔ | L | L | L | L | ⌐ | ⊔ |

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
⊔ = LOW pulse.
⌐ = TC goes LOW on a LOW-to-HIGH clock transition.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | 74LS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 16 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 74192, 74193, LS192, LS193
# Counters

**'192 Presettable BCD Decade Up/Down Counter**
**'193 Presettable 4-Bit Binary Up/Down Counter**
*Product Specification*

## FEATURES
- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

## DESCRIPTION
The '192 and '193 are 4-bit synchronous up/down counters — the '192 counts in BCD mode and the '193 counts in the binary mode. Separate up/down clocks, $CP_U$ and $CP_D$ respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either Clock input. If the $CP_U$ clock is pulsed while $CP_D$ is held HIGH, the device will count up . . . if $CP_D$ is pulsed while the $CP_U$ is held HIGH, the device will count down. Only one Clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT |
|------|------------------|------------------------|
| 74192 | 32MHz | 65mA |
| 74LS192 | 32MHz | 19mA |
| 74193 | 32MHz | 65mA |
| 74LS193 | 32MHz | 19mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|------------------------------------------------------------------|
| Plastic DIP | N74192N, N74LS192N, N74193N, N74LS193N |
| Plastic SO | N74LS193D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|------|-------------|-----|------|
| All | Inputs | 1ul | 1LSul |
| All | Outputs | 10ul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



```
D1   [1]      [16]  VCC
Q1   [2]      [15]  D0
Q0   [3]      [14]  MR
CPD  [4]      [13]  TCD
CPU  [5]      [12]  TCU
Q2   [6]      [11]  PL
Q3   [7]      [10]  D2
GND  [8]      [9]   D3
```
CD04730S

## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

LS04100S

## LOGIC SYMBOL (IEEE/IEC)



LS04110S
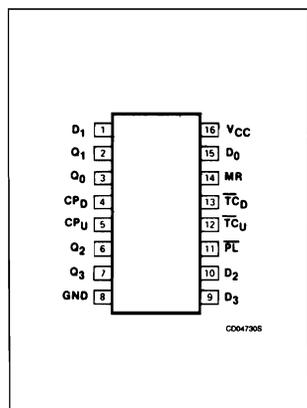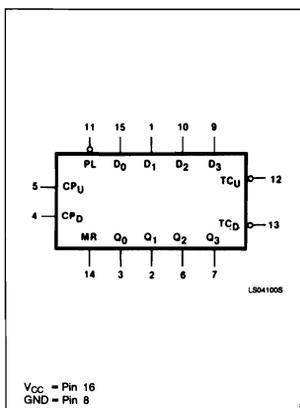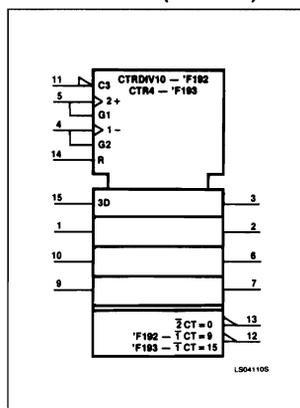
Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the $CP_D$ input will decrease the count by one, while a similar transition on the $CPU_U$ input will advance the count by one.

One clock should be held HIGH while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9 (for the '192 and 15 for the '193), the next HIGH-to-LOW transition of $CP_U$ will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until $CP_U$ goes HIGH again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the $CP_D$ goes LOW. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-

gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs ($D_0 - D_3$) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs LOW. If one of the Clock input is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

## LOGIC DIAGRAM, '192



Vcc = Pin 16
GND = Pin 8

## STATE DIAGRAM, '192



COUNT UP ————
COUNT DOWN – – – – –

LD02010S

$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$
$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

**Logic Equations For Terminal Count**
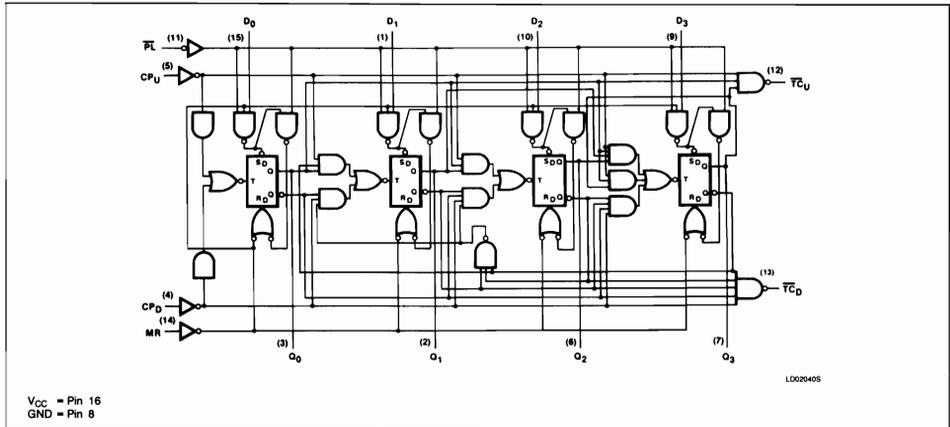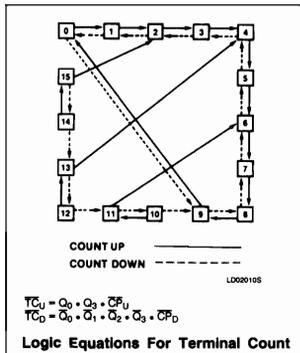
## MODE SELECT — FUNCTION TABLE, '192

| OPERATING MODE | INPUTS | | | | | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MR | $\overline{PL}$ | $CP_U$ | $CP_D$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $\overline{TC}_U$ | $\overline{TC}_D$ |
| Reset (clear) | H | X | X | L | X | X | X | X | L | L | L | L | H | L |
| | H | X | X | H | X | X | X | X | L | L | L | L | H | H |
| Parallel load | L | L | X | L | L | L | L | L | L | L | L | L | H | L |
| | L | L | X | H | L | L | L | L | L | L | L | L | H | H |
| | L | L | X | X | H | X | X | H | $Q_n = D_n$ | | | | L | H |
| | L | L | H | X | H | X | X | H | $Q_n = D_n$ | | | | H | H |
| Count up | L | H | ↑ | H | X | X | X | X | Count up | | | | H[a] | H |
| Count down | L | H | H | ↑ | X | X | X | X | Count down | | | | H | H[b] |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition
**NOTES:**
a. $\overline{TC}_U = CP_U$ at terminal count up (HLLH).
b. $\overline{TC}_D = CP_D$ at terminal count down (LLLL).

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# Counters

## LOGIC DIAGRAM, '193



$V_{CC}$ = Pin 16
GND = Pin 8

## STATE DIAGRAM, '193



COUNT UP ————
COUNT DOWN – – – –

LD02020S

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$
$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

**Logic Equations For Terminal Count**
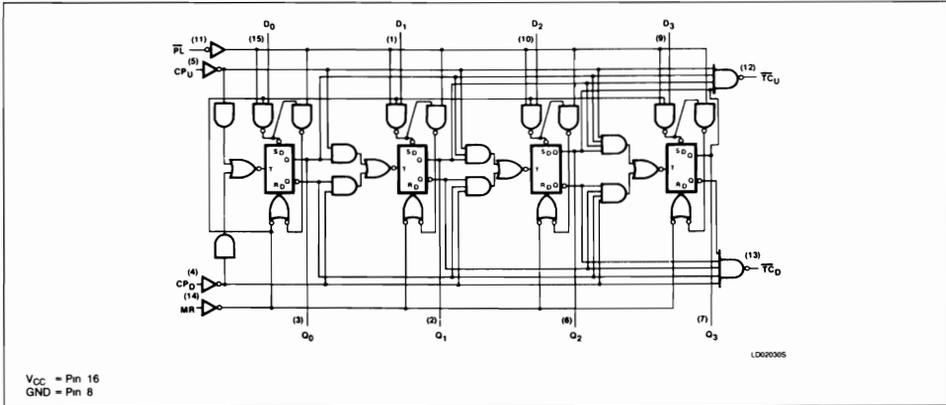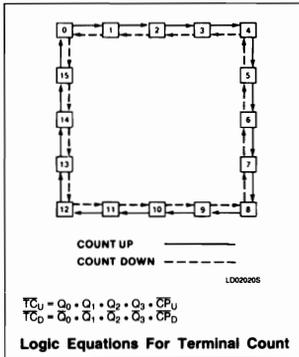
## MODE SELECT — FUNCTION TABLE, '193

| OPERATING MODE | INPUTS | | | | | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MR | $\overline{PL}$ | $CP_U$ | $CP_D$ | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $\overline{TC}_U$ | $\overline{TC}_D$ |
| Reset (clear) | H | X | X | L | X | X | X | X | L | L | L | L | H | L |
| | H | X | X | H | X | X | X | X | L | L | L | L | H | H |
| Parallel load | L | L | X | L | L | L | L | L | L | L | L | L | H | L |
| | L | L | X | H | L | L | L | L | L | L | L | L | H | H |
| | L | L | L | X | H | H | H | H | H | H | H | H | H | L |
| | L | L | H | X | H | H | H | H | H | H | H | H | H | H |
| Count up | L | H | ↑ | H | X | X | X | X | Count up | | | | H[c] | H |
| Count down | L | H | H | ↑ | X | X | X | X | Count down | | | | H | H[d] |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH clock transition

**NOTES:**
c. $TC_U = CP_U$ at terminal count up (HHHH).
d. $TC_D = CP_D$ at terminal count down (LLLL).

## FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



**NOTES:**
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

WF06700S

**'192 Decade Counter**

## FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



**NOTES:**
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

WF06710S

**'193 Binary Counter**

150
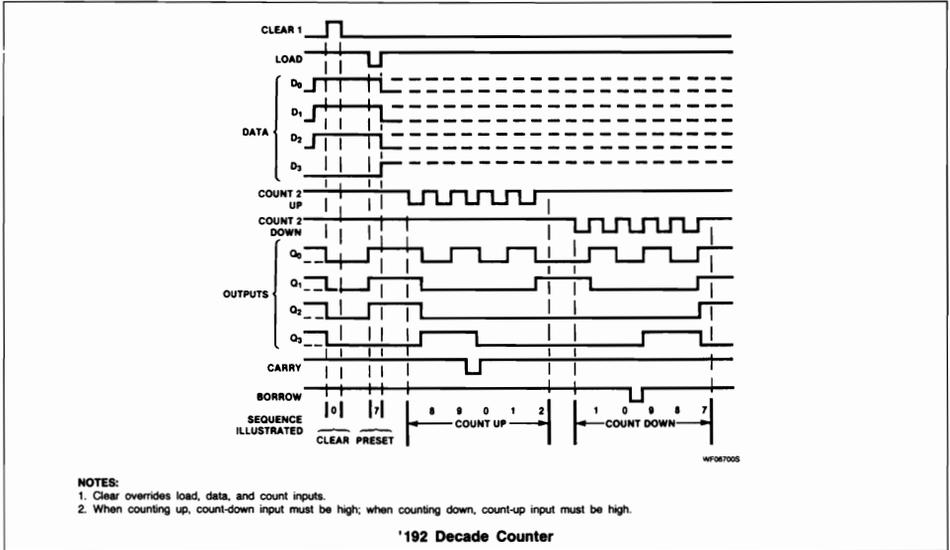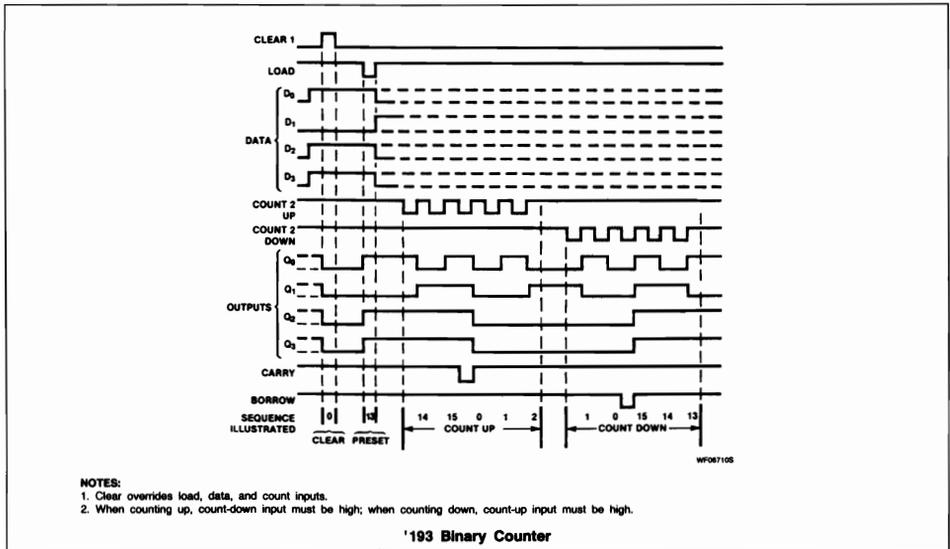
# 74194, LS194A, S194
## Shift Registers

**4-Bit Bidirectional Universal Shift Register**
*Product Specification*

- Buffered clock and control inputs
- Shift left and shift right capability
- Synchronous parallel and serial data transfers
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

## DESCRIPTION

The functional characteristics of the '194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 20ns (typical) for the 54/74 and 54LS/74LS, and 12ns (typical) for 54S/74S, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|------|------|
| 74194 | 36MHz | 39mA |
| 74LS194A | 36MHz | 15mA |
| 74S194 | 105MHz | 85mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|------|------|
| Plastic DIP | N74194N, N74LS194AN, N74S194N |
| Plastic SO-16 | N74LS194AD, N745194D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|------|------|------|------|------|
| All | Inputs | 1ul | 1Sul | 1LSul |
| $Q_0 - Q_3$ | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40μA $I_{IH}$ and $-1.6$mA $I_{IL}$, a 74S unit load (Sul) is 50μA $I_{IH}$ and $-2.0$mA $I_{IL}$, and 74LS unit load (LSul) is 20μA $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



CD04670S

## LOGIC SYMBOL



LS04010S

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



LS040205
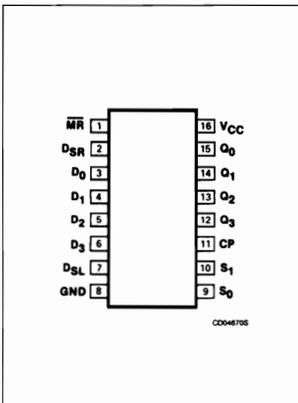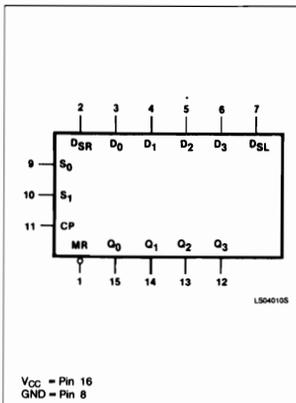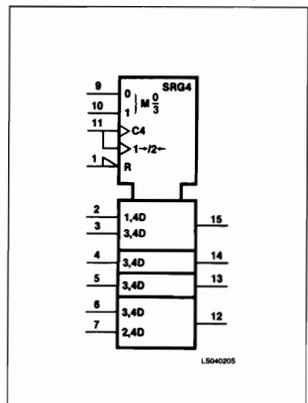
## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | CP | $\overline{MR}$ | $S_1$ | S | $D_{SR}$ | $D_{SL}$ | $D_n$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| Reset (clear) | X | L | X | X | X | X | X | L | L | L | L |
| Hold (do nothing) | X | H | l(a) | l(a) | X | X | X | $q_0$ | $q_1$ | $q_2$ | $q_3$ |
| Shift left | ↑ | H | h | l(a) | X | l | X | $q_1$ | $q_2$ | $q_3$ | L |
| | ↑ | H | h | l(a) | X | h | X | $q_1$ | $q_2$ | $q_3$ | H |
| Shift right | ↑ | H | l(a) | h | l | X | X | L | $q_0$ | $q_1$ | $q_2$ |
| | ↑ | H | l(a) | h | h | X | X | H | $q_0$ | $q_1$ | $q_2$ |
| Parallel load | ↑ | H | h | h | X | X | $d_n$ | $d_0$ | $d_1$ | $d_2$ | $d_3$ |

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the
LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
**NOTE:**
a. The HIGH-to-LOW transition of the $S_0$ and $S_1$ inputs on the 74194 should only take place while CP is HIGH
for conventional operation.

## TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES
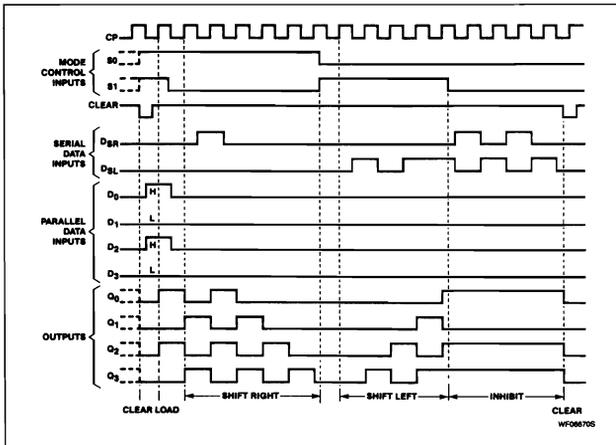


The '194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, $S_0$ and $S_1$. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, $Q_0 \to Q_1$, etc.) or, right to left (shift left, $Q_3 \to Q_2$, etc.) or, parallel data can be entered, loading all 4 bits of the register simultaneously. When both $S_0$ and $S_1$ are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs ($D_{SR}$, $D_{SL}$) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode Select and Data inputs on the 74S194 and 74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one set-up time prior to the positive transition of the clock pulse. The Mode Select inputs of the 74194 are gated with the clock and should be changed from HIGH-to-LOW only while the Clock input is HIGH.

The four parallel data inputs ($D_0 - D_3$) are D-type inputs. Data appearing on $D_0 - D_3$ inputs when $S_0$ and $S_1$ are HIGH is transferred to the $Q_0 - Q_3$ outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

# Shift Registers

## 74194, LS194A, S194

**LOGIC DIAGRAM**



$V_{CC}$ = Pin 16
GND = Pin 8

**74194**

**LOGIC DIAGRAM**



$V_{CC}$ = Pin 16
GND = Pin 8

**74S194, 74LS194A**

153
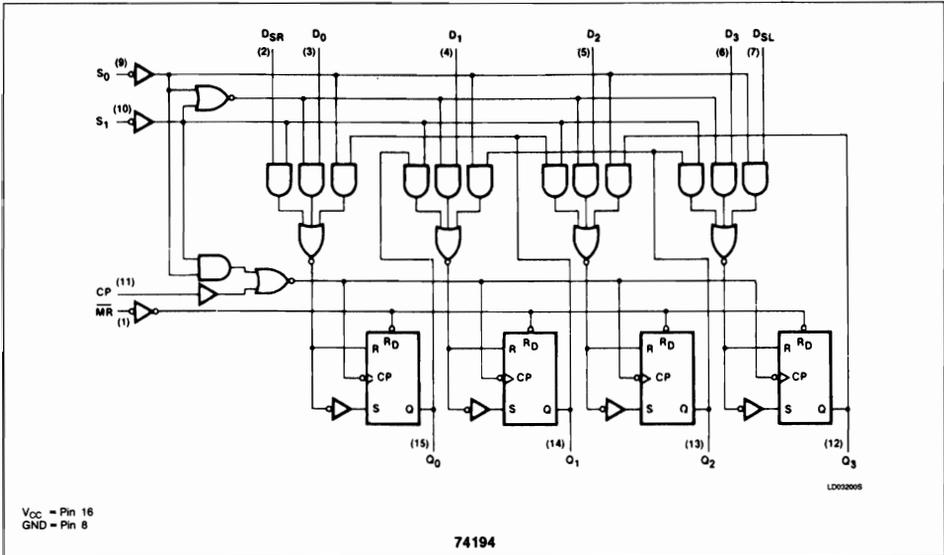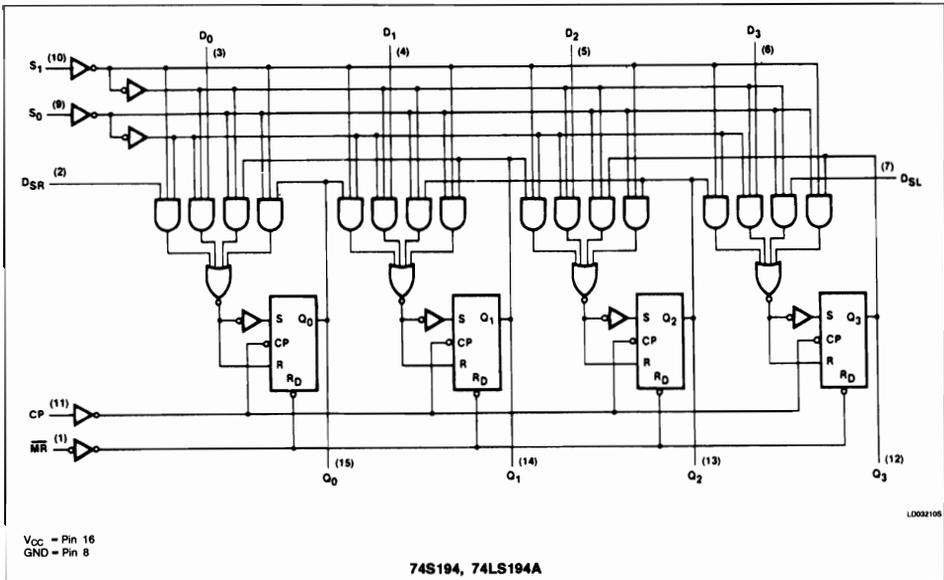
# 74195, LS195A, S195
## Shift Registers

**4-Bit Parallel Access Shift Register**
*Product Specification*

**Logic Products**

## FEATURES
- Buffered Clock and Control inputs
- Shift right and parallel load capability
- J-$\overline{K}$ (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset

## DESCRIPTION
The functional characteristics of the '195 4-Bit Parallel Access Shift register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The '195 operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop ($Q_0$) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition.

The J and $\overline{K}$ inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_3$) is transferred to the respective $Q_0 - Q_3$ outputs.
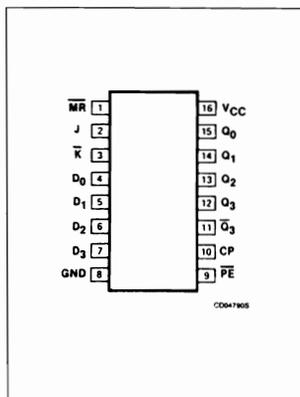
| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT |
|------|-------------------|------------------------|
| 74195 | 39MHz | 39mA |
| 74LS195A | 39MHz | 14mA |
| 74S195 | 105MHz | 70mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|------------------------------------------------------------------|
| Plastic DIP | N74195N, N74LS195N, N74S195N |
| Plastic SO-16 | N74LS195AD |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74S | 74LS |
|------|-------------|-----|------|-------|
| All | Inputs | 1ul | 1Sul | 1LSul |
| All | Outputs | 10ul | 10Sul | 10LSul |

**NOTE:**
Where a 74 unit load (ul) is understood to be 40µA $I_{IH}$ and −1.6mA $I_{IL}$, a 74S unit load (Sul) is 50µA $I_{IH}$ and −2.0mA $I_{IL}$, and 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION

| | | |
|---|---|---|
| $\overline{MR}$ | 1 | 16 | $V_{CC}$ |
| J | 2 | 15 | $Q_0$ |
| $\overline{K}$ | 3 | 14 | $Q_1$ |
| $D_0$ | 4 | 13 | $Q_2$ |
| $D_1$ | 5 | 12 | $Q_3$ |
| $D_2$ | 6 | 11 | $\overline{Q}_3$ |
| $D_3$ | 7 | 10 | CP |
| GND | 8 | 9 | $\overline{PE}$ |

CD04790S

## LOGIC SYMBOL

$V_{CC}$ = Pin 16
GND = Pin 8

LS04270S

## LOGIC SYMBOL (IEEE/IEC)

'S, 'LS195     '195

LS06570S     LS06580S

Shift left operation $(Q_3 \to Q_2)$ can be achieved by tying the $Q_n$ outputs to the $D_{n-1}$ inputs and holding the $\overline{PE}$ input low.

All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The '195 utilizes edge-trig-gering, therefore, there is no restriction on the activity of the J, $\overline{K}$, $D_n$, and $\overline{PE}$ inputs for logic operation, other than the set-up and release time requirements.

A LOW on the asynchronous Master Reset $(\overline{MR})$ input sets all Q outputs LOW, independent of any other input condition. The $\overline{MR}$ on the 54/74195 is gated with the clock. Therefore, the LOW-to-HIGH $\overline{MR}$ transition should only occur while the clock is LOW to avoid false clocking on the 54/74195.

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
*74195 only

LD03220S
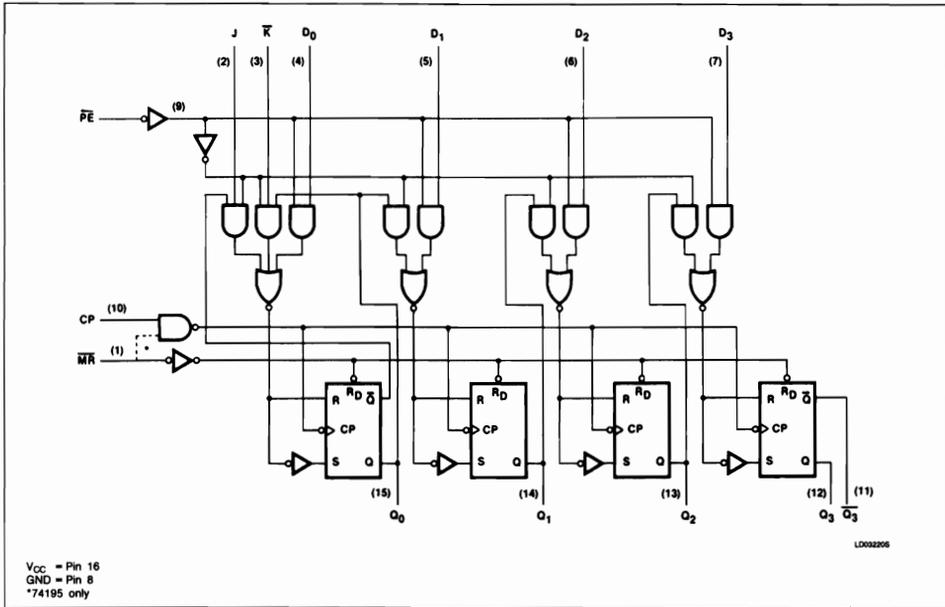
## MODE SELECT — FUNCTION TABLE

| OPERATING MODES | INPUTS | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | $\overline{PE}$ | J | $\overline{K}$ | $D_n$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $\overline{Q_3}$ |
| Asynchronous reset | L | X | X | X | X | X | L | L | L | L | H |
| Shift, set first stage | H | ↑ | h | h | h | X | H | $q_0$ | $q_1$ | $q_2$ | $\overline{q_2}$ |
| Shift, reset first stage | H | ↑ | h | l | l | X | L | $q_0$ | $q_1$ | $q_2$ | $\overline{q_2}$ |
| Shift, toggle first stage | H | ↑ | h | h | l | X | $\overline{q_0}$ | $q_0$ | $q_1$ | $q_2$ | $\overline{q_2}$ |
| Shift, retain first stage | H | ↑ | h | l | h | X | $q_0$ | $q_0$ | $q_1$ | $q_2$ | $\overline{q_2}$ |
| Parallel load | H | ↑ | l | X | X | $d_n$ | $d_0$ | $d_1$ | $d_2$ | $d_3$ | $\overline{d_3}$ |

H = HIGH voltage level.
L = LOW voltage level.
X = Don't care.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

155

# 74LS197
## Counter

**Presettable 4-Bit Binary Ripple Counter**
*Product Specification*

**Logic Products**

## FEATURES
- **High speed 4-bit binary counting**
- **Asynchronous parallel load for presetting counter**
- **Overriding Master Reset**
- **Buffered $Q_0$ output drives $\overline{CP}_1$ input plus standard fan-out**

## DESCRIPTION
The '197 is an asynchronously presettable binary ripple counter partitioned into divide-by-2 and divide-by-8 sections with each section having a separate Clock input. Stage changes are initiated in the counting modes by the HIGH-to-LOW transition of the Clock inputs, however, state changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock. The $Q_0$ flip-flop is triggered by the $\overline{CP}_0$ input while the $\overline{CP}_1$ input triggers the divide-by-8 section.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT |
|------|-------------------|------------------------|
| 74LS197 | 40MHz | 16mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|----------------------------------------------------------------|
| Plastic DIP | N74LS197N |
| Plastic SO-14 | N74LS197D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|------|-------------|------|
| $\overline{CP}_0$ | Clock input | 6LSul |
| $\overline{CP}_1$ | Clock input | 3.5LSul |
| All | Other inputs | 1LSul |
| $Q_0 - Q_3$ | Outputs | 10LSul |

**NOTE:**
Where a 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

The device has an asynchronous active-LOW Master Reset ($\overline{MR}$) input which overrides all other inputs and forces all outputs LOW. The counter is also asynchronously presettable. A LOW on the Parallel Load ($\overline{PL}$) input overrides the Clock inputs and loads the data from parallel Data ($D_0 - D_3$) inputs into the flip-flops. The counter acts as a transparent latch while the $\overline{PL}$ is LOW and any change in the $D_n$ inputs will be reflected in the outputs.

## PIN CONFIGURATION



CD06130S

## LOGIC SYMBOL



$V_{CC}$ = Pin 14
GND = Pin 7

LS06590S

## LOGIC SYMBOL (IEEE/IEC)



LS06600S

# Counters

## LOGIC DIAGRAM



( ) = Pin numbers
$V_{CC}$ = Pin 14
GND = Pin 7
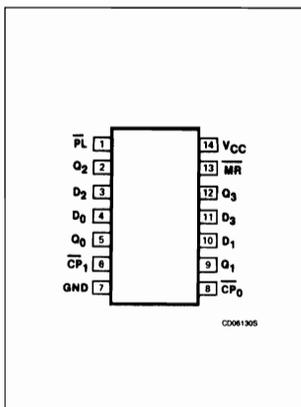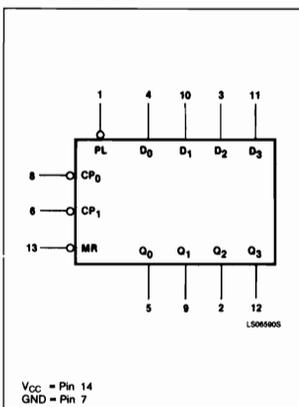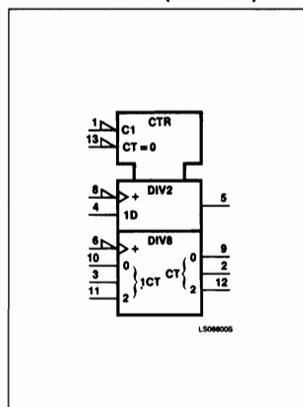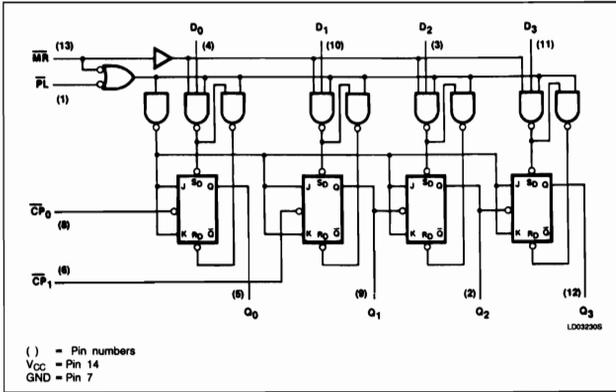
## COUNT SEQUENCE

| COUNT | 4-BIT BINARY[1] | | | |
|---|---|---|---|---|
| | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | L | L | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

**NOTE:**
1. $Q_0$ connected to input $\overline{CP}_1$; input applied to $\overline{CP}_0$.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74LS | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUT |
|---|---|---|---|---|---|
| | $\overline{MR}$ | $\overline{PL}$ | $\overline{CP}$ | $D_n$ | $Q_n$ |
| Reset (clear) | L | X | X | X | L |
| Parallel load | H | L | X | L | L |
| | H | L | X | H | H |
| Count | H | H | ↓ | X | count |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW clock transition

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74LS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | µA |
| $I_{OL}$ | LOW-level output current | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

# 74199
## Shift Register

### 8-Bit Parallel-Access Shift Register
*Product Specification*

**Logic Products**

## FEATURES
- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **Fully synchronous data transfers**
- **J-$\overline{K}$ (D) inputs to first stage**
- **Clock enable for hold (do nothing) mode**
- **Asynchronous Master Reset**

## DESCRIPTION

The functional characteristics of the '199 8-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT |
|------|-------------------|------------------------|
| 74199 | 35MHz | 90mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|--------------------------------|
| Plastic DIP | N74199N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 |
|------|-------------|-----|
| All | Inputs | 1ul |
| $Q_0 - Q_7$ | Parallel outputs | 10ul |

**NOTE:**
A 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ AND $-1.6$mA $I_{IL}$.

## PIN CONFIGURATION

## LOGIC SYMBOL

$V_{CC}$ = Pin 24
GND = Pin 12

## LOGIC SYMBOL (IEEE/IEC)

# Shift Register

## LOGIC DIAGRAM



$V_{CC}$ = Pin 24
GND = Pin 12
( ) = Pin number
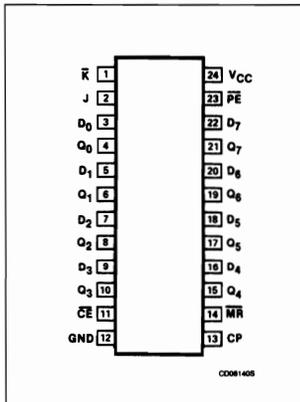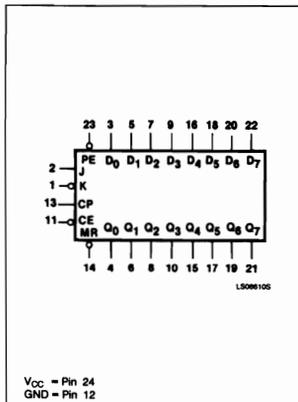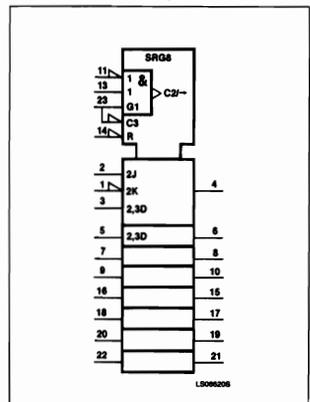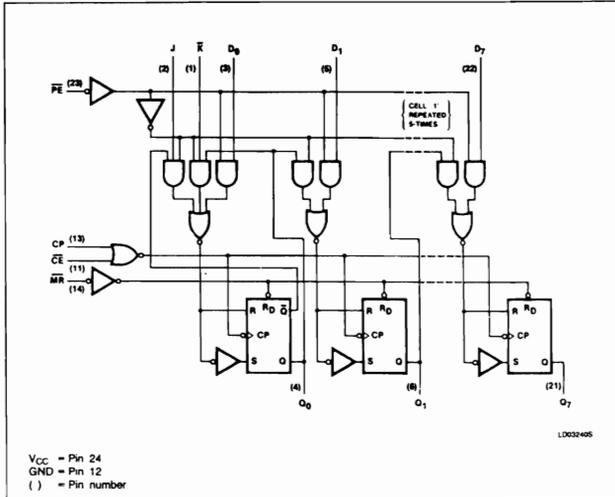
The '199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop ($Q_0$) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the J-K type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ($D_0 - D_7$) is transferred to the respective $Q_0 - Q_7$ outputs.

All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The '199 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, $D_n$, and $\overline{PE}$ inputs for logic operation, other than the set-up and release time requirements.

The clock input is a gated OR structure which allows one input to be used as an active-LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

## MODE SELECT — FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | $\overline{CE}$ | $\overline{PE}$ | J | $\overline{K}$ | $D_n$ | $Q_0$ | $Q_1$ | ...... $Q_6$ | $Q_7$ |
| Reset (clear) | L | X | X | X | X | X | X | L | L | ...... L | L |
| Shift, set first stage | H | ↑ | l | h | h | h | X | H | $q_0$ | ...... $q_5$ | $q_6$ |
| Shift, reset first stage | H | ↑ | l | h | l | l | X | L | $q_0$ | ...... $q_5$ | $q_6$ |
| Shift, toggle first stage | H | ↑ | l | h | h | l | X | $\overline{q_0}$ | $q_0$ | ...... $q_5$ | $q_6$ |
| Shift, retain first stage | H | ↑ | l | h | l | h | X | $q_0$ | $q_0$ | ...... $q_5$ | $q_6$ |
| Parallel load | H | ↑ | l | l | X | X | $d_n$ | $d_0$ | $d_1$ | ...... $d_6$ | $d_7$ |
| Hold (do nothing) | H | ↑ | h(a) | X | X | X | X | $q_0$ | $q_1$ | ...... $q_6$ | $q_7$ |

H = HIGH voltage level steady state.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
X = Don't care
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.
**NOTE:**
a. The LOW-to-HIGH transition of $\overline{CE}$ should only occur while CP is HIGH for conventional operation.

# Shift Registers

## TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



**ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74 | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −12 | mA |
| $I_{OH}$ | HIGH-level output current | | | −800 | V |
| $I_{OL}$ | LOW-level output current | | | 16 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

# 74LS245
## Transceiver

### Octal Transceiver (3-State)
**Product Specification**

**Logic Products**

## FEATURES
- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs

## DESCRIPTION
The 'LS245 is an octal transceiver fea-
turing non-inverting 3-State bus compati-
ble outputs in both send and receive
directions. The outputs are all capable of
sinking 24mA and sourcing up to 15mA,
producing very good capacitive drive
characteristics. The device features a
Chip Enable (CE) input for easy cascad-
ing and a Send/Receive (S/R) input for
direction control. All data inputs have
hysteresis built in to minimize AC noise
effects.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS245 | 8ns | 58mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS245N |
| Plastic SOL-20 | N74LS245D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| All | Inputs | 1LSul |
| All | Outputs | 30LSul |

**NOTE:**
Where a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



CD06710S

## LOGIC SYMBOL



LS06750S

## LOGIC SYMBOL (IEEE/IEC)



LS067605
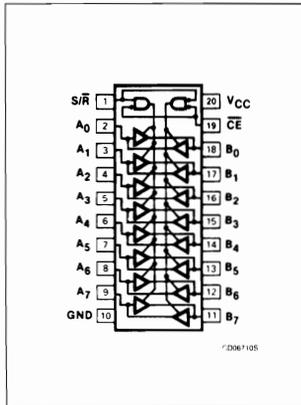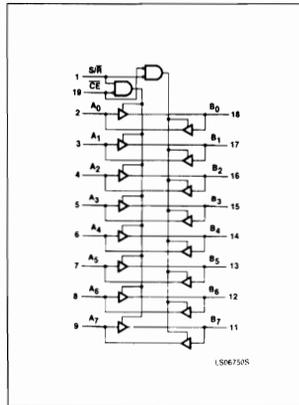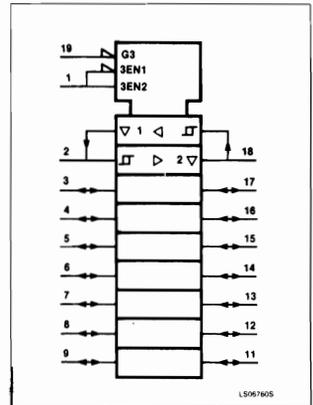
# 74LS251, S251
## Multiplexers

### 8-Input Multiplexer (3-State)
### *Product Specification*

**Logic Products**

## FEATURES
- **High speed 8-to-1 multiplexing**
- **True and complement outputs**
- **Both outputs are 3-State for further multiplexer expansion**
- **3-State outputs are buffer type with 12mA/24mA outputs for Military/Commercial applications**

## DESCRIPTION
The '251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs ($S_0$, $S_1$, $S_2$) controlling the switch position. Assertion (Y) and Negation ($\overline{Y}$) outputs are both provided. The Output Enable input ($\overline{OE}$) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \overline{OE} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2$$
$$+ I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2$$
$$+ I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2$$
$$+ I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

Both outputs are in the HIGH impedance (HIGH Z) state when the output enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the HIGH impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State devices are tied together. Design of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

| TYPE | TYPICAL PROPAGATION DELAY (DATA TO Y) | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS251 | 18ns | 9mA |
| 74S251 | 8ns | 55mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74S251N, N74LS251AN |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|---|---|---|---|
| All | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 10LSul |

**NOTE:**
A 74S unit load (Sul) is 50μA $I_{IH}$ and −2.0mA $I_{IL}$ and a 74LS unit load (LSul) is 20μA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD04870S

## LOGIC SYMBOL



LS04420S

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



LS04430S

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin number

LD02140S

## FUNCTION TABLE

| INPUTS | | | | | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | $S_2$ | $S_1$ | $S_0$ | $I_0$ | $I_1$ | $I_2$ | $I_3$ | $I_4$ | $I_5$ | $I_6$ | $I_7$ | $\overline{Y}$ | $Y$ |
| H | X | X | X | X | X | X | X | X | X | X | X | (Z) | (Z) |
| L | L | L | L | L | X | X | X | X | X | X | X | H | L |
| L | L | L | L | H | X | X | X | X | X | X | X | L | H |
| L | L | L | H | X | L | X | X | X | X | X | X | H | L |
| L | L | L | H | X | H | X | X | X | X | X | X | L | H |
| L | L | H | L | X | X | L | X | X | X | X | X | H | L |
| L | L | H | L | X | X | H | X | X | X | X | X | L | H |
| L | L | H | H | X | X | X | L | X | X | X | X | H | L |
| L | L | H | H | X | X | X | H | X | X | X | X | L | H |
| L | H | L | L | X | X | X | X | L | X | X | X | H | L |
| L | H | L | L | X | X | X | X | H | X | X | X | L | H |
| L | H | L | H | X | X | X | X | X | L | X | X | H | L |
| L | H | L | H | X | X | X | X | X | H | X | X | L | H |
| L | H | H | L | X | X | X | X | X | X | L | X | H | L |
| L | H | H | L | X | X | X | X | X | X | H | X | L | H |
| L | H | H | H | X | X | X | X | X | X | X | L | H | L |
| L | H | H | H | X | X | X | X | X | X | X | H | L | H |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74LS | 74S | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output for HIGH output state | −0.5 to +5.5 | −0.5 to +5.5 | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

# 74LS253, S253
## Multiplexers

**Dual 4-Input Multiplexer (3-State)**
*Product Specification*

**Logic Products**

## FEATURES
- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

## DESCRIPTION
The '253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs ($S_0$, $S_1$). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

| TYPE | TYPICAL PROPAGATION DELAY (From Data) | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|----------------------------------------|--------------------------------|
| 74LS253 | 15ns | 8mA |
| 74S253 | 8ns | 48mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|---------------------------------------------------------------|
| Plastic DIP | N74S253N, N74LS253N |
| Plastic SO-16 | N74LS253D, N74S253D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|------|-------------|-----|------|
| All | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 10LSul |

**NOTE:**
A 74S unit load (Sul) is 50µA $I_{IH}$ and –2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



164
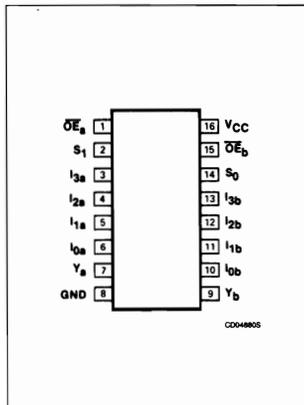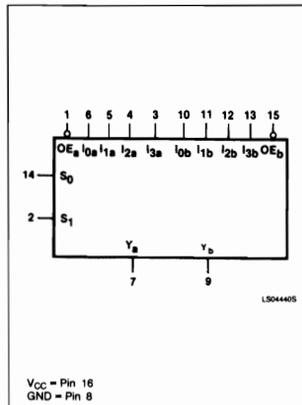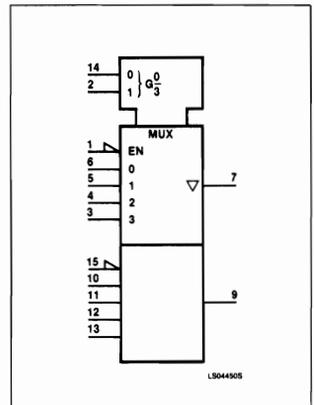
# 74LS256
## Latch

**Dual 4-Bit Addressable Latch**
*Product Specification*

**Logic Products**

## FEATURES
- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as dual 1-of-4 active HIGH decoder

## DESCRIPTION
The '256 dual addressable latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{CLR} = \overline{E} = LOW$), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS256 | 19ns | 22mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS256N |
| Plastic SO-16 | N74LS256D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| $\overline{E}$ | Input | 2LSul |
| Other | Inputs | 1LSul |
| All | Outputs | 10LSul |

**NOTE:**
A 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD04891S

## LOGIC SYMBOL



$V_{CC}$ = Pin 16
GND = Pin 8

LS04461S

## LOGIC SYMBOL (IEEE/IEC)



LS04470S
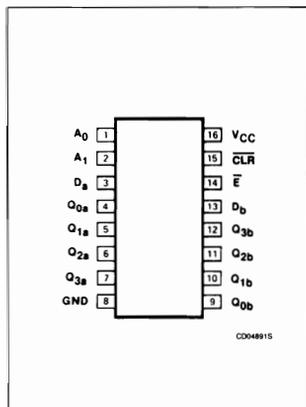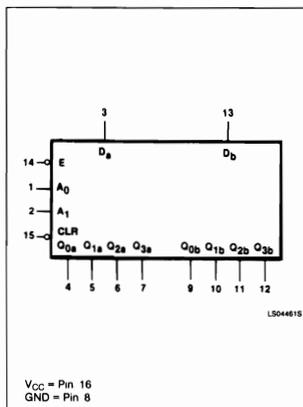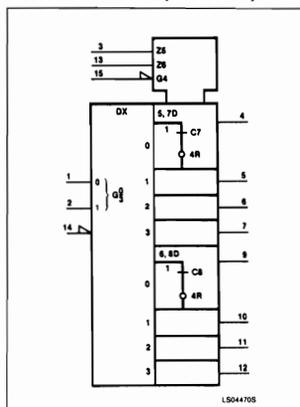
# 74LS258A, S258
# Data Selectors/Multiplexers

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)
*Product Specification*

Logic Products

## FEATURES
- Multifunction capability
- Inverting data path
- 3-State outputs
- See '257 for non-inverting version

## DESCRIPTION
The '258 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The $I_0$ inputs are selected when the Select input is LOW and the $I_1$ inputs are selected when the Select input is HIGH. Data appears at the outputs in inverted (complementary) form.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|------|---------------------------|-------------------------------|
| 74LS258A | 13ns | 9mA |
| 74S258 | 6ns | 48mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|----------|----------------------------------------------------------------|
| Plastic DIP | N74S258N, N74LS258AN |
| Plastic SOL-16 | N74LS258AD |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|------|-------------|-----|------|
| S | Input | 2Sul | 2LSul |
| Other | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 30LSul |

NOTE:
Where a 74S unit load (Sul) is to be 50µA $I_{IH}$ and –2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20µA $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



166
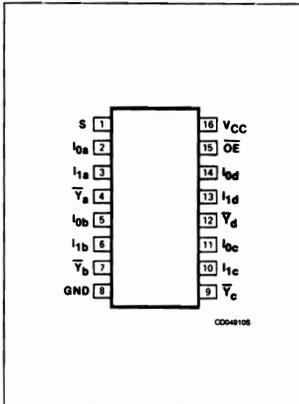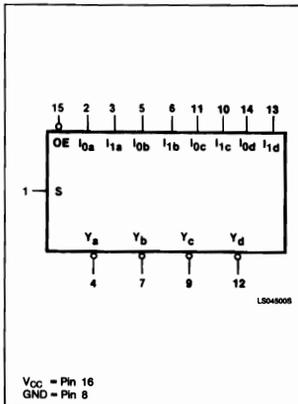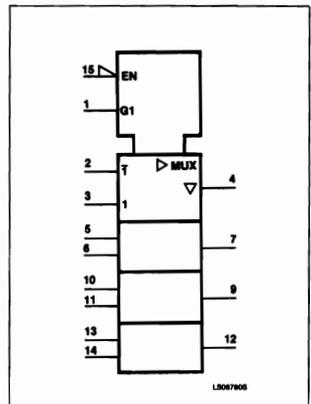
# 74LS258A, S258

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
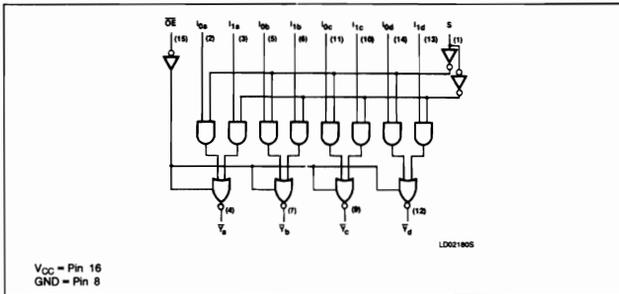
The '258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input ($\overline{OE}$) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-state devices are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

## FUNCTION TABLE

| OUTPUT ENABLE | SELECT INPUT | DATA INPUTS | | OUTPUTS |
|---|---|---|---|---|
| $\overline{OE}$ | S | $I_0$ | $I_1$ | $\overline{Y}$ |
| H | X | X | X | (Z) |
| L | H | X | L | H |
| L | H | X | H | L |
| L | L | L | X | H |
| L | L | H | X | L |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| | PARAMETER | 74S | 74S | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | −0.5 to +5.5 | V |
| $I_{IN}$ | Input current | −30 to +1 | −30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

## RECOMMENDED OPERATING CONDITIONS

| | PARAMETER | 74LS | | | 74S | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −2.6 | | | −6.5 | mA |
| $I_{OL}$ | LOW-level output current | | | 24 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | 0 | | 70 | °C |

# 74LS259
## Latch

**8-Bit Addressable Latch**
*Product Specification*

**Logic Products**

## FEATURES
- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as a 1-of-8 active HIGH decoder

## DESCRIPTION
The '259 addressable latch has four distinct modes of operation that are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{CLR} = \overline{E} = LOW$), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS259 | 19ns | 22mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS259N |
| Plastic SO-16 | N74LS259D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| All | Inputs | 1LSul |
| All | Outputs | 10LSul |

**NOTE:**
A 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION

A0 [1] 16 $V_{CC}$
A1 [2] 15 $\overline{CLR}$
A2 [3] 14 $\overline{E}$
Q0 [4] 13 D
Q1 [5] 12 Q7
Q2 [6] 11 Q6
Q3 [7] 10 Q5
GND [8] 9 Q4

CD04211S

## LOGIC SYMBOL

LS03251E

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)

LS03260S

168

# 74LS259

## LOGIC DIAGRAM



Vcc = Pin 16
GND = Pin 8
( ) = Pin number
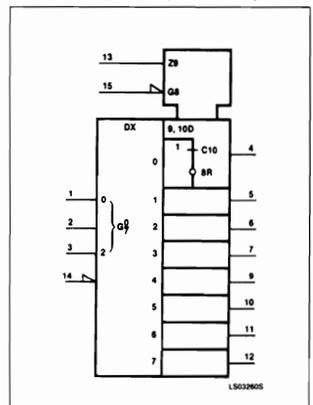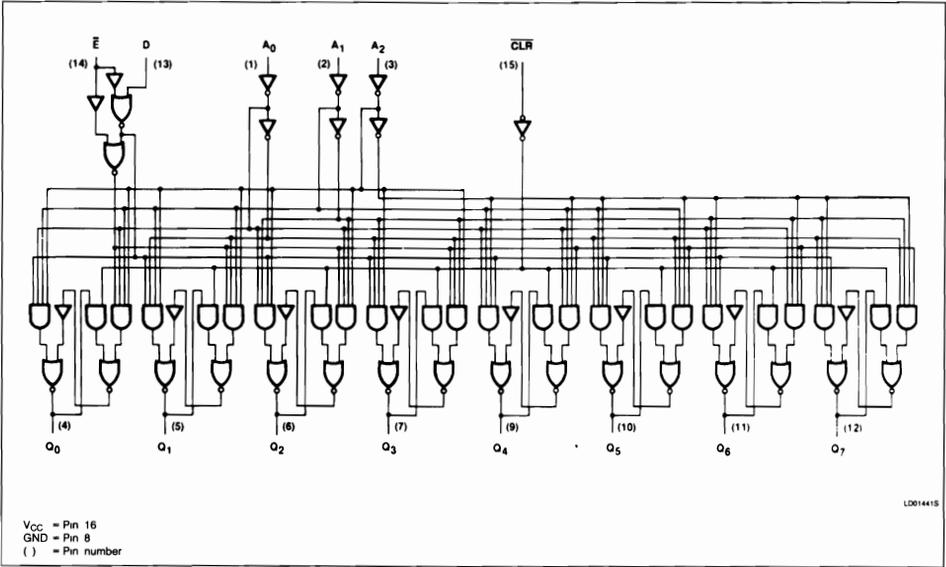
## MODE SELECT—FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CLR}$ | $\overline{E}$ | D | $A_0$ | $A_1$ | $A_2$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ |
| Clear | L | H | X | X | X | X | L | L | L | L | L | L | L | L |
| Demultiplex (active HIGH decoder when D = H) | L | L | d | L | L | L | Q = d | L | L | L | L | L | L | L |
| | L | L | d | H | L | L | L | Q = d | L | L | L | L | L | L |
| | L | L | d | L | H | L | L | L | Q = d | L | L | L | L | L |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | L | L | d | H | H | H | L | L | L | L | L | L | L | Q = d |
| Store (do nothing) | H | H | X | X | X | X | $q_0$ | $q_1$ | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $q_7$ |
| Addressable latch | H | L | d | L | L | L | Q = d | $q_1$ | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $q_7$ |
| | H | L | d | H | L | L | $q_0$ | Q = d | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $q_7$ |
| | H | L | d | L | H | L | $q_0$ | $q_1$ | Q = d | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $q_7$ |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | H | L | d | H | H | H | $q_0$ | $q_1$ | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | Q = d |

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care.
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

# 74LS266
# Gate

**Quad 2-Input Exclusive-NOR Gate (Open Collector)**
*Product Specification*

**Logic Products**

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS266 | 18ns | 8mA |

## FUNCTION TABLE

| INPUTS | | OUTPUT |
|---|---|---|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | H |

H = HIGH voltage level
L = LOW voltage level

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS266N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| A, B | Inputs | 2LSul |
| Y | Output | 10LSul |

**NOTE:**
A 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and –0.4mA $I_{IL}$.

## PIN CONFIGURATION



CD08740S

## LOGIC SYMBOL



LS08610S

## LOGIC SYMBOL (IEEE/IEC)



LS08820S

170
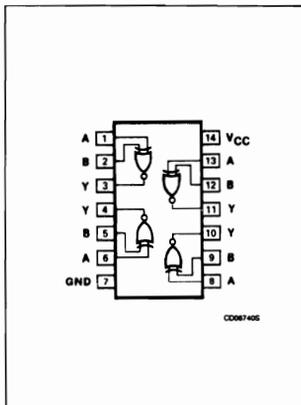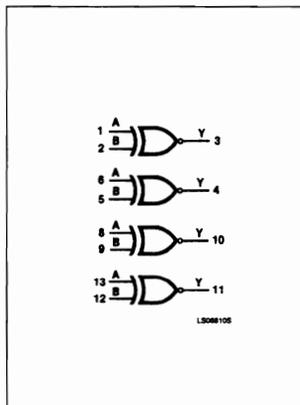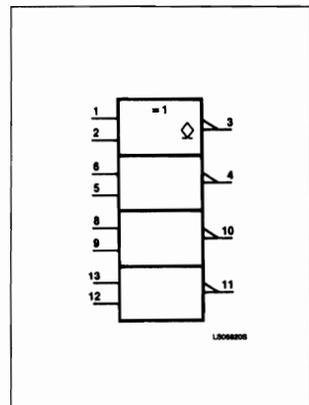
# 74LS273, S273
## Flip-Flops

### Octal D Flip-Flops
*Product Specification*

## FEATURES
- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- High speed Schottky version available
- Buffered common clock
- Buffered, asynchronous Master Reset
- Slim 20-pin plastic and ceramic DIP packages
- See '377 for Clock Enable version
- See '373 for transparent latch version
- See '374 for 3-state version

## DESCRIPTION
The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS273 | 40MHz | 17mA |
| 74S273 | 95MHz | 109mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74S273N, N74LS273N |
| Plastic SOL-20 | N74LS273D, N74S273D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|---|---|---|---|
| All | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 10LSul |

**NOTE:**
A 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and −2.0mA $I_{IL}$ and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



$V_{CC}$ = Pin 20
GND = Pin 10

## LOGIC SYMBOL (IEEE/IEC)

# 74LS283
## Adder

**4-Bit Full Adder With Fast Carry**
*Product Specification*

Logic Products

## FEATURES
- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal carry lookahead

## DESCRIPTION

The '283 adds two 4-bit binary words ($A_n$ plus $B_n$) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry ($C_{OUT}$) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4)$$
$$= \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where ( + ) = plus.

Due to the symmetry of the binary add function, the '283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic) – see Function Table. In case of all active LOW operands the results $\Sigma_1 - \Sigma_4$ and $C_{OUT}$ should be interpreted also as active LOW. With active HIGH inputs, $C_{IN}$ cannot be left open; it must be held LOW when no "carry in" is

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS283 | 13ns | 20mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS283N |
| Plastic SO-16 | N74LS283D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| A, B | Inputs | 2LSul |
| $C_{IN}$ | Input | 1LSul |
| All | Outputs | 10LSul |

**NOTE:**
A 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.

intended. Interchanging inputs of equal weight does not affect the operation, thus $C_{IN}$, $A_1$, $B_1$ can arbitrarily be assigned to pins 5, 6, 7, etc.

## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



172

# Adder

## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin Numbers
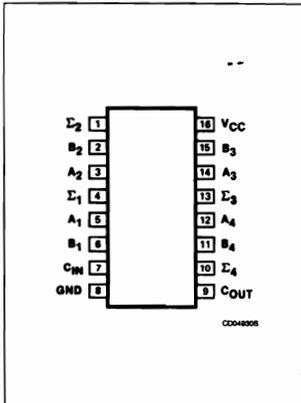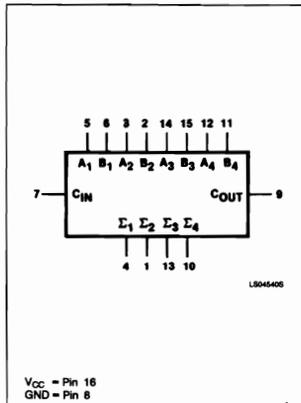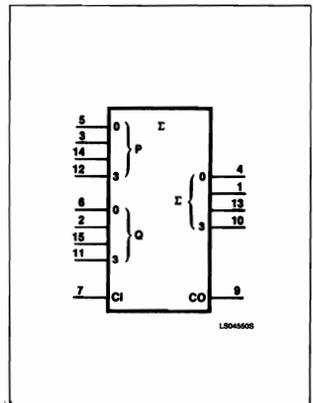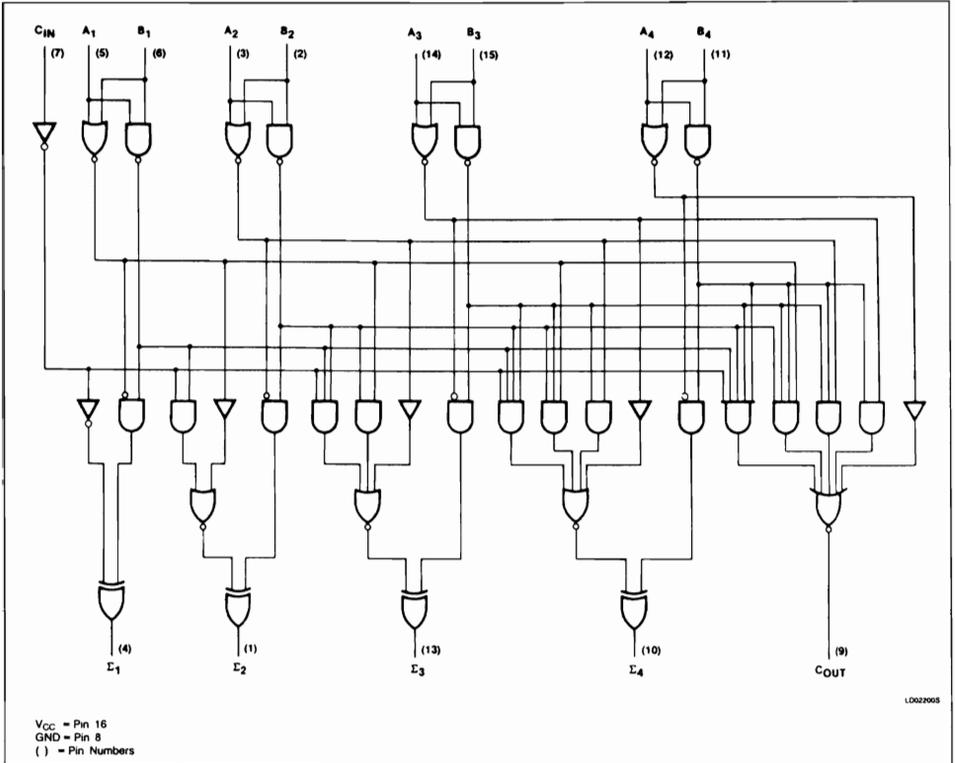
## FUNCTION TABLE

| PINS | $C_{IN}$ | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $\Sigma_1$ | $\Sigma_2$ | $\Sigma_3$ | $\Sigma_4$ | $C_{OUT}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Logic levels | L | L | H | L | H | H | L | L | H | H | H | L | L | H |
| Active HIGH | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| Active LOW | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

Example:
1001
1010
10011
(10 + 9 = 19)
(carry + 5 + 6 = 12)

H = HIGH voltage level
L = LOW voltage level

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74LS | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

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# 74LS290
## Counter

**Decade Counter**
*Product Specification*

## DESCRIPTION

The '290 is a 4-bit, ripple type decade counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the Clock and MR inputs, setting the outputs to nine (HLLH).

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS290 | 42MHz | 9mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS290N |
| Plastic SO-14 | N74LS290D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| MR, MS | Inputs | 1LSul |
| $\overline{CP}_0$ | Input | 4LSul |
| $\overline{CP}_1$ | Input | 8LSul |
| All | Outputs | 10LSul |

**NOTE:**
A 74LS unit load (LSul) is $20\mu A$ $I_{IH}$ and $-0.4mA$ $I_{IL}$.

## PIN CONFIGURATION



```
MS₁  1      14  Vcc
NC   2      13  MR₂
MS₂  3      12  MR₁
Q₂   4      11  CP₁
Q₁   5      10  CP₀
NC   6       9  Q₀
GND  7       8  Q₃
```
CD06780S

## LOGIC SYMBOL



$V_{CC}$ = Pin 14
GND = Pin 7

LS06850S

## LOGIC SYMBOL (IEEE/IEC)



LS06860S

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Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the $\overline{CP}_1$ input must be externally connected to the $Q_0$ output. The $\overline{CP}_0$ input receives the incoming count, producing a BCD count sequence. In a symmetrical bi-quinary divide-by-ten counter the $Q_3$ output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output $Q_0$. To operate as a divide-by-two and a divide-by-five counter, no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and $Q_0$ as the output). The $\overline{CP}_1$ input is used to obtain divide-by-five operation at the $Q_3$ output.

## LOGIC DIAGRAM



$V_{CC}$ = Pin 14
GND = Pin 7
( ) Pin numbers

## BCD COUNT SEQUENCE — FUNCTION TABLE

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |

NOTE:
Output $Q_0$ connected to input $\overline{CP}_1$.

## MODE SELECTION — FUNCTION TABLE

| RESET INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| MR$_1$ | MR$_2$ | MS$_1$ | MS$_2$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| L | X | L | X | | Count | | |
| X | L | X | L | | Count | | |
| L | X | X | L | | Count | | |
| X | L | L | X | | Count | | |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

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# 74LS293
## Counter

**4-Bit Binary Ripple Counter**
*Product Specification*

**Logic Products**

## DESCRIPTION
The '293 is a 4-bit ripple type binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR$_1$ MR$_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

| TYPE | TYPICAL f$_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS293 | 42MHz | 9mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE V$_{CC}$ = 5V ±5%; T$_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74LS293N |
| Plastic SO-14 | N74LS293D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| MR | Inputs | 1LSul |
| $\overline{CP}_0$ | Input | 6LSul |
| $\overline{CP}_1$ | Input | 4LSul |
| All | Outputs | 10LSul |

**NOTE:**
A 74LS unit load (LSul) is 20$\mu$A I$_{IH}$ and −0.4mA I$_{IL}$.

## PIN CONFIGURATION



## LOGIC SYMBOL



V$_{CC}$ = Pin 14
GND = Pin 7

## LOGIC SYMBOL (IEEE/IEC)



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# Counter

## LOGIC DIAGRAM



( ) = Pin numbers
$V_{CC}$ = Pin 14
GND = Pin 7

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output $Q_0$ must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are preformed at the $Q_0$, $Q_1$, $Q_2$ and $Q_3$ outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the $Q_1$, $Q_2$ and $Q_3$ outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

## FUNCTION TABLE

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |
| 10 | L | H | L | H |
| 11 | H | H | L | H |
| 12 | L | L | H | H |
| 13 | H | L | H | H |
| 14 | L | H | H | H |
| 15 | H | H | H | H |

NOTE:
Output $Q_0$ connected to input $\overline{CP}_1$.

## MODE SELECTION

| RESET INPUTS | | OUTPUTS | | | |
|---|---|---|---|---|---|
| $MR_1$ | $MR_2$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| H | H | L | L | L | L |
| L | H | | Count | | |
| H | L | | Count | | |
| L | L | | Count | | |

H = HIGH voltage level
L = LOW voltage level
X = Don't care

# 74LS364
## Flip-Flop

### Octal D Flip-Flop With 3-State Outputs
*Product Specification*

**Logic Products**

## FEATURES
- **8-bit positive edge-triggered register**
- **3-State MOS compatible output buffers**
- **Common Clock Input with hysteresis**
- **Common 3-State Output Enable control**
- **Independent register and 3-State buffer operation**

## DESCRIPTION
The '364 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transi-

| TYPE | TYPICAL f$_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS364 | 50MHz | 42mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE V$_{CC}$ = 5V ±5%; T$_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74LS364N |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| All | Inputs | 1LSul |
| All | Outputs | 30LSul |

**NOTE:**
A 74LS unit load (LSul) is 20μA I$_{IH}$ and −0.4mA I$_{IL}$.

tion, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

## PIN CONFIGURATION

## LOGIC SYMBOL

V$_{CC}$ = Pin 20
GND = Pin 10
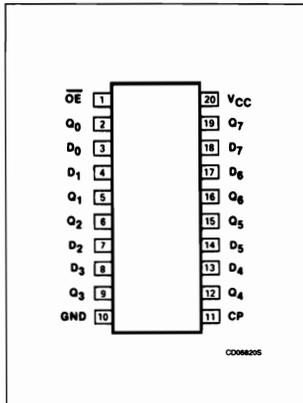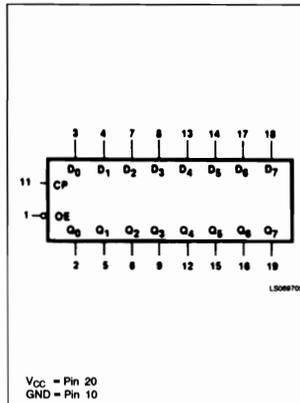
## LOGIC SYMBOL (IEEE/IEC)
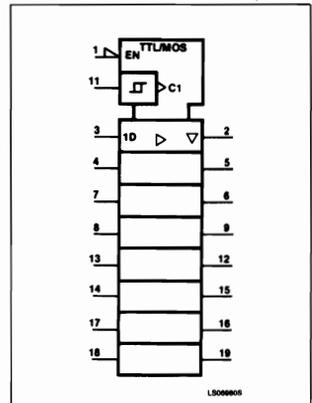
# 74365A, 366A, 367A, 368A, LS365A, LS366A, LS367A, LS368A Buffers/Drivers

'365A, '367A Hex Buffer/Driver (3-State)
'366A, '368A Hex Inverter Buffer (3-State)
*Product Specification*

## FUNCTION TABLE, '365A, '366A

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{OE}_1$ | $\overline{OE}_2$ | I | Y | $\overline{Y}$ |
| L | L | L | L | H |
| L | L | H | H | L |
| X | H | X | (Z) | (Z) |
| H | X | X | (Z) | (Z) |

## FUNCTION TABLE, '367A, '368A

| INPUTS | | OUTPUTS | |
|---|---|---|---|
| $\overline{OE}$ | I | Y | $\overline{Y}$ |
| L | L | L | H |
| L | H | H | L |
| H | X | (Z) | (Z) |

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74365A, 367A | 10ns | 65mA |
| 74LS365A, 367A | 10ns | 14mA |
| 74366A, 368A | 9ns | 59mA |
| 74LS366A, 368A | 10ns | 12mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74365AN, N74LS365AN, N74366AN, N74LS366AN N74367AN, N74LS367AN, N74368AN, N74LS368AN |
| Plastic SO-16 | N74LS365AD, N74LS367AD, N74LS368AD |

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74 | 74LS |
|---|---|---|---|
| All | Inputs | 1ul | 1LSul |
| All | Outputs | 20ul | 30LSul |

NOTE:
Where a 74 unit load (ul) is understood to be 40$\mu$A $I_{IH}$ and $-1.6$mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



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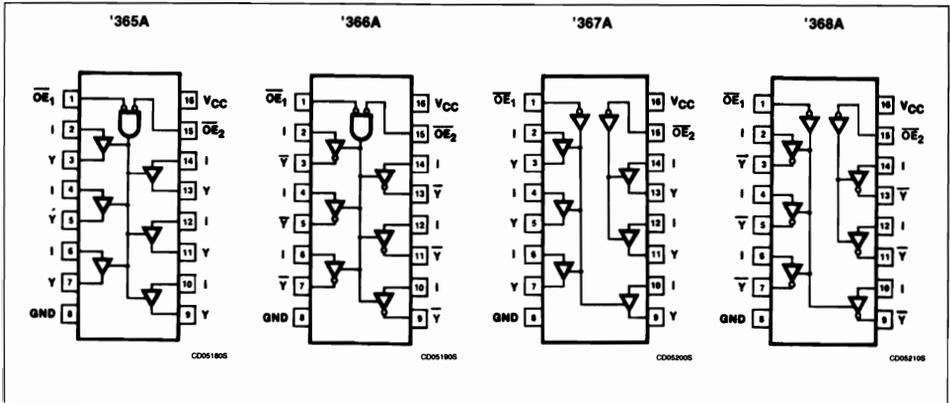
# 74365A, 366A, 367A, 368A, LS365A, LS366A, LS367A, LS368A

## LOGIC SYMBOL

'365A  '366A  '367A  '368A

LS04860S  LS04870S  LS04880S  LS04890S

## LOGIC SYMBOL (IEEE/IEC)

'365A  '366A  '367A  '368A

LS04900S  LS04910S  LS04920S  LS04930S

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74 | 74LS | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +5.5 | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +5 | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | | °C |

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# 74LS373, 74LS374, S373, S374
## Latches/Flip-Flops

**Logic Products**

'373 Octal Transparent Latch With 3-State Outputs
'374 Octal D Flip-Flop With 3-State Outputs
*Product Specification*

## FEATURES
- **8-bit transparent latch — '373**
- **8-bit positive, edge-triggered register — '374**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

## DESCRIPTION
The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS373 | 19ns | 24mA |
| 74S373 | 10ns | 105mA |
| 74LS374 | 19ns | 27mA |
| 74S374 | 8ns | 116mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74LS373N, N74S373N, N74LS374N, N74S374N |
| Plastic SOL-20 | N74LS373D, N74S373D, N74LS374D, N74S374D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74S | 74LS |
|---|---|---|---|
| All | Inputs | 1Sul | 1LSul |
| All | Outputs | 10Sul | 30LSul |

**NOTE:**
Where a 74S unit load (Sul) is 50$\mu$A $I_{IH}$ and −2.0mA $I_{IL}$, and a 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and −0.4mA $I_{IL}$.

## PIN CONFIGURATION
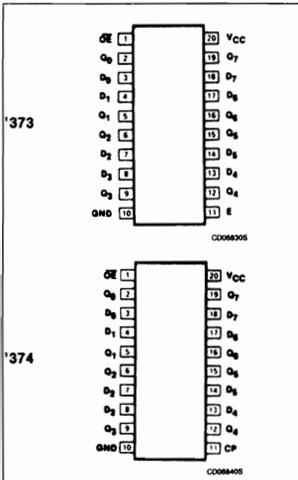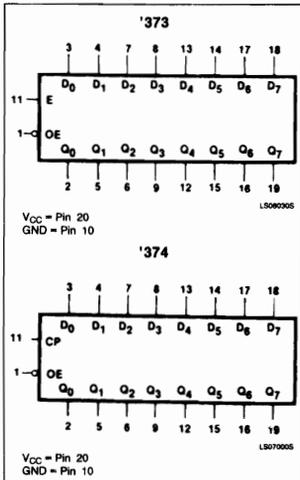


## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/EC)



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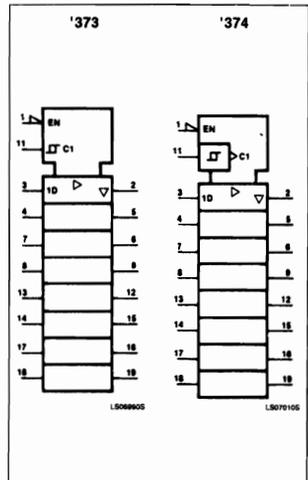
The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one set-up time before the HIGH-to-LOW enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (OE) controls all eight 3-State buffers independent of the latch

operation. When OE is LOW, the latched or transparent data appears at the outputs. When OE is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (OE) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred

to the corresponding flip-flop's Q output. The clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (OE) controls all eight 3-State buffers independent of the register appears at the outputs. When OE is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

## LOGIC DIAGRAM, '373



$V_{CC}$ = Pin 20
GND = Pin 10

## LOGIC DIAGRAM, '374



$V_{CC}$ = Pin 20
GND = Pin 10
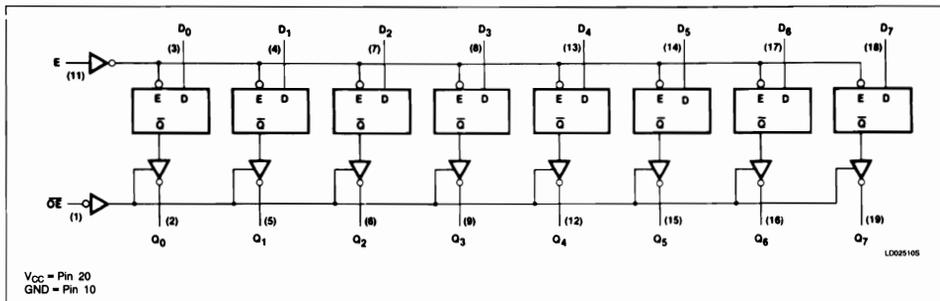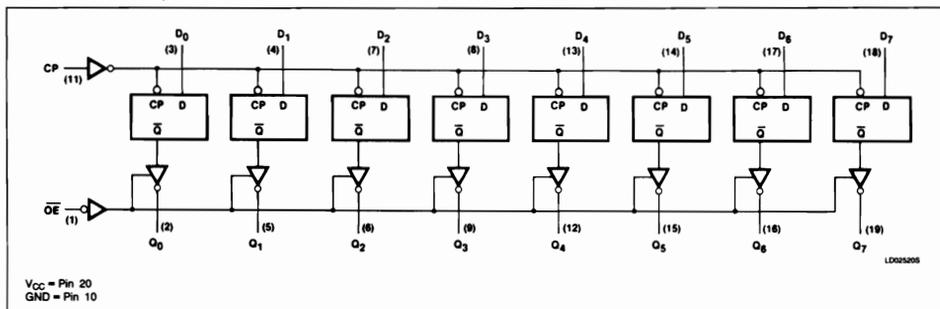
## MODE SELECT — FUNCTION TABLE '373

| OPERATING MODES | INPUTS | | | INTERNAL REGISTER | OUTPUTS |
| | OE | E | $D_n$ | | $Q_0 - Q_7$ |
|---|---|---|---|---|---|
| Enable and read register | L | H | L | L | L |
| | L | H | H | H | H |
| Latch and read register | L | L | l | L | L |
| | L | L | h | H | H |
| Latch register and disable outputs | H | L | l | L | (Z) |
| | H | L | h | H | (Z) |

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# 74LS390
## Counter

**Dual Decade Ripple Counter**
*Product Specification*

## FEATURES
- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two Master Resets to clear each decade counter individually

## DESCRIPTION
The '390 is a dual 4-bit decade ripple counter divided into four separately clocked sections. The counter has two divide-by-two sections and two divide-by-five sections. These sections are normally used in a BCD decade or a bi-quinary configuration, since they share a common Master Reset input. If the two Master Resets can be used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS390 | 55MHz | 15mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ |
|---|---|
| Plastic DIP | N74LS390N |
| Plastic SO-16 | N74LS390D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| MR | Inputs | 1LSul |
| $CP_0$ | Inputs | 4LSul |
| $CP_1$ | Inputs | 6LSul |
| All | Outputs | 10LSul |

**NOTE:**
A 74LS unit load (LSul) is 20$\mu$A $I_{IH}$ and $-0.4$mA $I_{IL}$.

## PIN CONFIGURATION



```
CF0a   1          16  VCC
MRa    2          15  CF0b
Q0a    3          14  MRb
CF1a   4          13  Q0b
Q1a    5          12  CF1b
Q2a    6          11  Q1b
Q3a    7          10  Q2b
GND    8           9  Q3b
```
CD06870S

## LOGIC SYMBOL



```
1, 15 ─○ CP0
                  1/2 '390
4, 12 ─○ CP1
          MR   Q0  Q1  Q2  Q3
        2, 14 3, 13 5, 11 6, 10  7, 9
```
LS07060S

$V_{CC}$ = Pin 16
GND = Pin 8

## LOGIC SYMBOL (IEEE/IEC)



LS07070S

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## LOGIC DIAGRAM



$V_{CC}$ = Pin 16
GND = Pin 8
( ) = Pin numbers
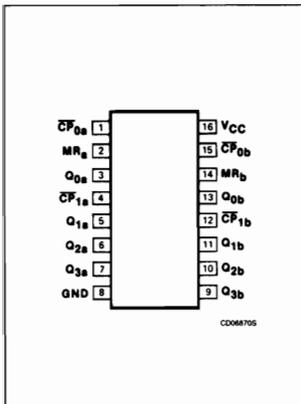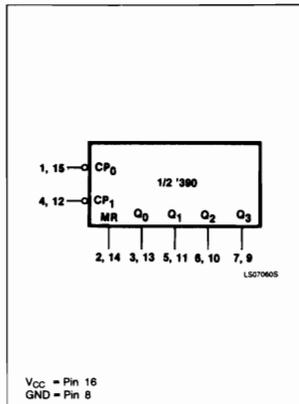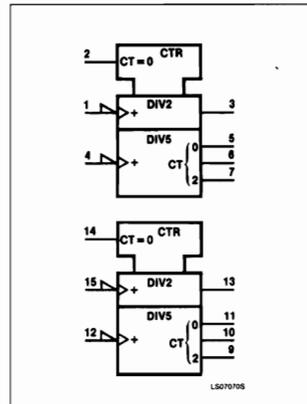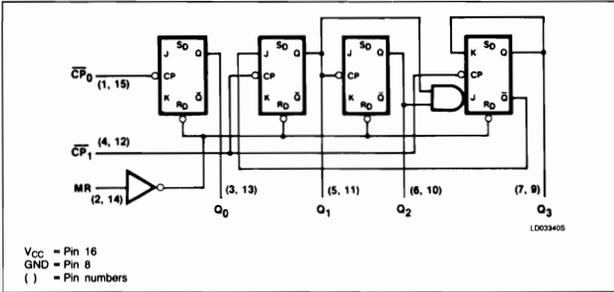
Each section is triggered by the HIGH-to-LOW transition of the Clock ($\overline{CP}$) inputs. For BCD decade operation, the $Q_0$ output is connected to the $\overline{CP}$, input of the divide-by-five section. For bi-quinary decade operation (50% duty cycle output), the $Q_3$ output is connected to the $CP_0$ input, and $Q_0$ becomes the decade output.

The Master Resets ($MR_a$ and $MR_b$) are active HIGH synchronous inputs to each decade counter which operate on the portion of the counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clocks and sets the four outputs LOW.

## BCD COUNT SEQUENCE FOR ½ THE '390

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |

H = HIGH voltage level
L = LOW voltage level
**NOTE:**
Output $Q_0$ is connected to input $\overline{CP}_1$ with Counter input on $\overline{CP}_0$.

## BI-QUINARY COUNT SEQUENCE FOR ½ THE '390

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | L | L | L | L |
| 1 | L | H | L | L |
| 2 | L | L | H | L |
| 3 | L | H | H | L |
| 4 | L | L | L | H |
| 5 | H | L | L | L |
| 6 | H | H | L | L |
| 7 | H | L | H | L |
| 8 | H | H | H | L |
| 9 | H | L | L | H |

**NOTE:**
Output $Q_3$ is connected to input $\overline{CP}_0$ with Counter input on $\overline{CP}_1$.

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74LS | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

**NOTE:**
$V_{IH}$ limited to 5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs.

# 74LS393
## Counter

### Dual 4-Bit Binary Ripple Counter
*Product Specification*

**Logic Products**

## FEATURES
- Two 4-bit binary counters
- Divide-by any binary module up to 28 in one package
- Two Master Resets to clear each 4-bit counter individually

## DESCRIPTION
The '393 is a Dual 4-bit Binary Ripple Counter with separate Clock and Master Reset inputs to each counter. The operation of each half of the '393 is the same as the '93 except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the Clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding.

| TYPE | TYPICAL $f_{MAX}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74LS393 | 35MHz | 15mA |

## ORDERING CODE

| PACKAGES | COMMERCIAL RANGE $V_{CC}$ = 5V ±5%; $T_A$ = 0°C to +70°C |
|---|---|
| Plastic DIP | N74LS393N |
| Plastic SO-14 | N74LS393D |

**NOTE:**
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS | DESCRIPTION | 74LS |
|---|---|---|
| MR | Master Reset input | 1LSul |
| $\overline{CP}$ | Clock input | 4LSul |
| Q | Output | 10LSul |

**NOTE:**
Where a 74LS unit load (LSul) is 20µA $I_{IH}$ and −0.4mA $I_{IL}$.
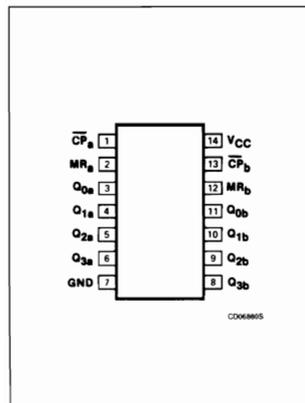
## PIN CONFIGURATION



## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)

## LOGIC DIAGRAM



$V_{CC}$ = Pin 14
GND = Pin 7
( ) = Pin number
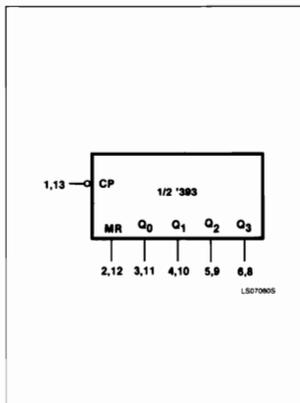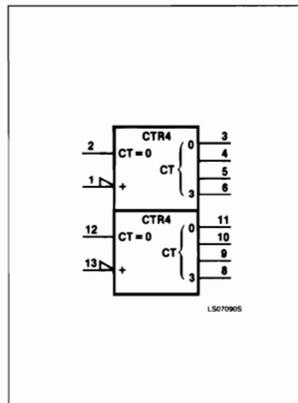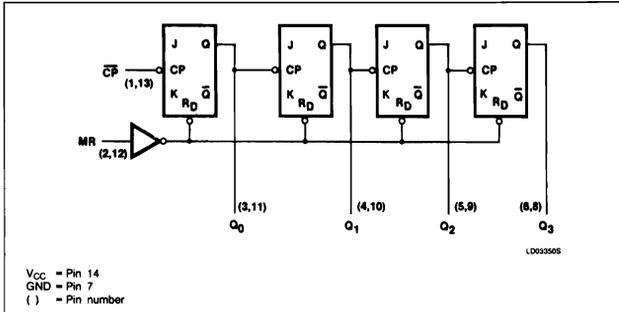
The Master Resets ($MR_a$ and $MR_b$) are active-HIGH asynchronous inputs to each 4-bit counter identified by the ''a'' and ''b'' suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clock and sets the outputs LOW.

## COUNT SEQUENCE
## FOR ½ THE '393

| COUNT | OUTPUTS | | | |
|---|---|---|---|---|
| | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| 0 | L | L | L | L |
| 1 | H | L | L | L |
| 2 | L | H | L | L |
| 3 | H | H | L | L |
| 4 | L | L | H | L |
| 5 | H | L | H | L |
| 6 | L | H | H | L |
| 7 | H | H | H | L |
| 8 | L | L | L | H |
| 9 | H | L | L | H |
| 10 | L | H | L | H |
| 11 | H | H | L | H |
| 12 | L | L | H | H |
| 13 | H | L | H | H |
| 14 | L | H | H | H |
| 15 | H | H | H | H |

H = HIGH voltage level
L = LOW voltage level

## ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

| PARAMETER | | 74LS | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 7.0 | V |
| $V_{IN}$ | Input voltage | −0.5 to +7.0 | V |
| $I_{IN}$ | Input current | −30 to +1 | mA |
| $V_{OUT}$ | Voltage applied to output in HIGH output state | −0.5 to +$V_{CC}$ | V |
| $T_A$ | Operating free-air temperature range | 0 to 70 | °C |

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | 74LS | | | UNIT |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{IH}$ | HIGH-level input voltage | 2.0 | | | V |
| $V_{IL}$ | LOW-level input voltage | | | +0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | mA |
| $I_{OH}$ | HIGH-level output current | | | −400 | μA |
| $I_{OL}$ | LOW-level output current | | | 8 | mA |
| $T_A$ | Operating free-air temperature | 0 | | 70 | °C |

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| | CD 4000 | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 00 | GATE |  |
| 01 | GATE |  |
| 02 | GATE |  |
| 03 | | |
| 06 | REGISTER |  |

| CD 4000 | | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 07 | INVERTER |  |
| 08 | ADDER |  |
| 09 | BUFFER |  |
| 10 | BUFFER |  |
| 11 | GATE |  |
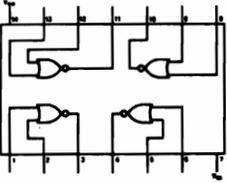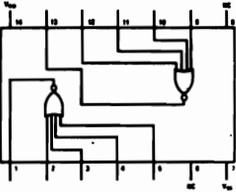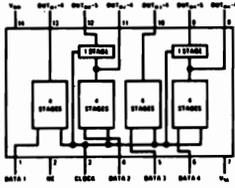
# CD 4000

| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
|---|---|---|
| 12 | GATE |  |
| 13 | FLIP-FLOP |  |
| 14 | REGISTER |  |
| 15 | REGISTER |  |
| 16 | SWITCH |  |

| | CD 4000 | |
|---|---|---|
| **PRODUCT NUMBER** | **PRODUCT DESCRIPTION** | **PIN OUT DIL CERAMIC+MOLDED** |
| 17 | COUNTER |  |
| 18 | COUNTER |  |
| 19 | GATE |  |
| 20 | COUNTER |  |
| 21 | REGISTER |  |

| | CD 4000 | |
|---|---|---|
| **PRODUCT NUMBER** | **PRODUCT DESCRIPTION** | **PIN OUT DIL CERAMIC+MOLDED** |
| 22 | COUNTER |  |
| 23 | GATE |  |
| 24 | COUNTER |  |
| 25 | GATE |  |
| 26 | | |

| CD 4000 | | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 27 | FLIP-FLOP |  |
| 28 | DECODER |  |
| 29 | COUNTER |  |
| 30 | GATE |  |
| 31 | REGISTER |  |

| CD 4000 | | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 34 | REGISTER |  |
| 35 | REGISTER |  |
| 38 | | |
| 40 | COUNTER |  |
| 41 | BUFFER |  |

| CD 4000 | | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 42 | LATCH |  |
| 43 | LATCH |  |
| 44 | LATCH |  |
| 46 | PLL |  |
| 47 | MULTIVIBRATOR |  |

| | CD 4000 | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 48 | GATE |  |
| 49 | BUFFER |  |
| 50 | BUFFER |  |
| 51 | DEMULTIPLEXER |  |
| 52 | DEMULTIPLEXER |  |
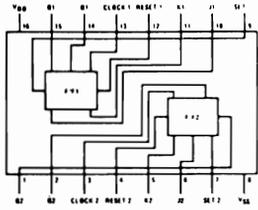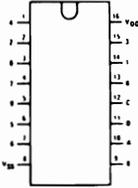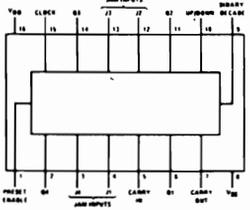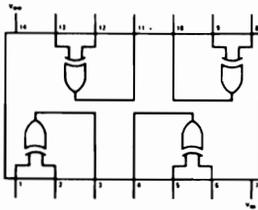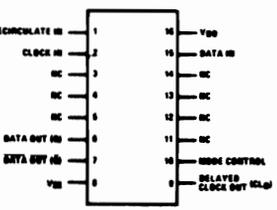
195

| CD 4000 | | |
|---|---|---|
| **PRODUCT NUMBER** | **PRODUCT DESCRIPTION** | **PIN OUT DIL CERAMIC+MOLDED** |
| 53 | DEMULTIPLEXER | |
| 60 | COUNTER | |
| 66 | SWITCH | |
| 69 | INVERTER | |
| 70 | GATE | |

| | CD 4000 | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 71 | GATE |  |
| 72 | GATE |  |
| 73 | GATE |  |
| 75 | GATE |  |
| 76 | FLIP-FLOP |  |

| CD 4000 | | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 81 | GATE |  |
| 82 | GATE |  |
| 84 | | |
| 89 | MULTIPLIER |  |
| 93 | SCHMITT TRIGGER |  |

| CD 4000 | | |
|---|---|---|
| PRODUCT NUMBER | PRODUCT DESCRIPTION | PIN OUT DIL CERAMIC+MOLDED |
| 99 | LATCHES |  |
| 106 | HEX SCHMITT TRIGGERS |  |
| 160 | COUNTER |  |
| 161 | COUNTER |  |
| 162 | COUNTER |  |

| | CD 4000 | |
|---|---|---|
| **PRODUCT NUMBER** | **PRODUCT DESCRIPTION** | **PIN OUT DIL CERAMIC+MOLDED** |
| 163 | COUNTER |  |
| 174 | FLIP-FLOP |  |
| 175 | FLIP-FLOP |  |
| 192 | COUNTER |  |
| 193 | COUNTER |  |

## SCL4510B

# CMOS
# BCD UP/DOWN COUNTER

### FEATURES
♦ Internally Synchronous for High Speed
♦ Asynchronous Preset Enable
♦ Asynchronous Reset
♦ Logic Edge-Clocked Design
♦ 6MHz Counting Rate @ 10Vdc
♦ Carry Output for Cascading Stages

### DESCRIPTION

The SCL4510B consists of a four-stage Up/Down Counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Reset, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A high on the Reset line resets all stages to the "zero" state. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode, provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable." The Carry-in terminal must be connected to $V_{SS}$ when not in use.

The counter counts Up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

This counter finds primary use in up/down and differential counting and frequency synthesizer applications. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

### CONNECTION DIAGRAM
(all packages)

| $V_{DD}$ | CL | Q3 | P3 | P2 | Q2 | U/D | R |
|---|---|---|---|---|---|---|---|
| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |

**SCL4510B**

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|
| PE | Q4 | P4 | P1 | $\overline{CI}$ | Q1 | $\overline{CO}$ | $V_{SS}$ |

**Add suffix for package:**

| C | 16-pin Cerdip |
|---|---|
| D | 16-pin Ceramic |
| E | 16-pin Epoxy |
| F | 16-pin Flat |
| H | Chip |

### RECOMMENDED OPERATING CONDITIONS

**For maximum reliability:**

| DC Supply Voltage | $V_{DD} - V_{SS}$ | 3 to 15 | Vdc |
|---|---|---|---|
| Operating Temperature | $T_A$ | | |
| C, D, F, H Device | | -55 to +125 | °C |
| E Device | | -40 to +85 | °C |

### BLOCK DIAGRAM



$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8

### TRUTH TABLE

| CARRY IN | UP/DOWN | PRESET ENABLE | RESET | ACTION |
|---|---|---|---|---|
| 1 | X | 0 | 0 | No Count |
| 0 | 1 | 0 | 0 | Count Up |
| 0 | 0 | 0 | 0 | Count Down |
| X | X | 1 | 0 | Preset |
| X | X | X | 1 | Reset |

X = Don't Care

## LOGIC DIAGRAM



## TIMING DIAGRAM

# SCL4511B

# CMOS BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

## FEATURES

♦ High-Current Sourcing Bipolar Outputs (Up to 25 mA)
♦ Latched Storage of Input Code
♦ Blanking Input for Display Intensity Modulation
♦ Lamp Test Provision
♦ Readout Blanking for Illegal Input Combinations

## DESCRIPTION

The SCL4511B provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability to source up to 25 mA of current. Lamp Test, Blanking, and Latch Enable inputs are used to test the display, turn off the display, and store a BCD code, respectively. It can be used with LED, incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include counter display drivers, seven-segment decimal display, and various clock, watch, and timer uses.

### CONNECTION DIAGRAM
(all packages)

Segment Outputs

| V_DD | f | g | a | b | c | d | e |
|------|---|---|---|---|---|---|---|
| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |
| | | | SCL4511B | | | | |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| B | C | LT | BI | LE | D | A | V_SS |

Add suffix for package:

| | |
|---|---|
| C | 16-pin Cerdip |
| D | 16-pin Ceramic |
| E | 16-pin Epoxy |
| F | 16-pin Flat |
| H | Chip |

## TRUTH TABLE

| LE | BI | LT | D | C | B | A | a | b | c | d | e | f | g | DISPLAY |
|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---------|
| x | x | 0 | x | x | x | x | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| x | 0 | 1 | x | x | x | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 9 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 1 | 1 | x | x | x | x | | | | * | | | | * |

X = Don't care
* Depends upon the BCD code applied during the 0 to 1 transition of LE.
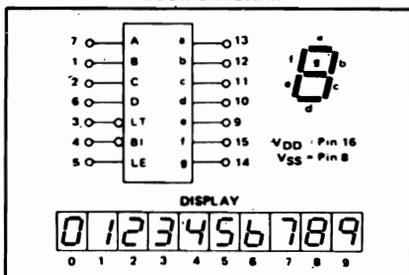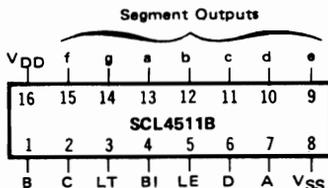
## RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

| | | | |
|---|---|---|---|
| DC Supply Voltage | V_DD - V_SS | 3 to 15 | Vdc |
| Operating Temperature | T_A | | |
| C, D, F, H Device | | -55 to +125 | °C |
| E Device | | -40 to +85 | °C |

## BLOCK DIAGRAM
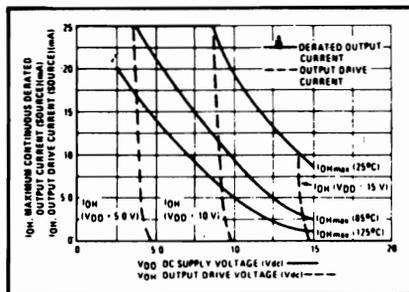




Typical P-Channel
Source Current Characteristics

The maximum continuous (worst case) derated output drive current applies to a single output with all other outputs sourcing an equal amount of current. Operation above the derating curve at a given temperature is not recommended.

## APPLICATIONS INFORMATION

### 32-INPUT MULTIPLEXER

Output terminals of several SCL4512B devices can be connected to a single data bus. One SCL4512B is selected by the 3-state Disable control, and the remaining devices are disabled into a high-impedance state. A 32-input multiplexer utilizing four SCL4512B data selectors and a single SCL4011B is shown.
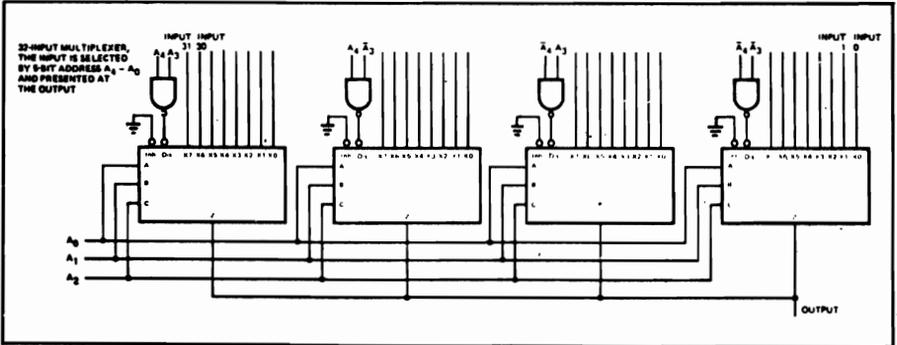


### LOGIC FUNCTION GENERATORS

In addition to the standard application of multiplexers in data conversion techniques, these circuits can also be used in generating logic functions, which in many cases can reduce system package count.

A multiplexer is a multiple-position single-pole switch. One set of inputs selects the position of the switch. The second set of inputs collects the input data, which is transferred through the circuit to one output. By using the binary select inputs and the data inputs, the SCL4512B can generate any of the 65,536 different functions of four variables.

Assume the four binary inputs are A, B, C, and D, and that Z is the desired function. Using the select inputs as the first three variables, any combination of A, B, and C will select a data input (assuming the output is enabled). For each combination of A, B, and C, the required output, as a function of the fourth variable D, can be HIGH or LOW or the same as D or the inverse of D. Therefore, the truth table may be examined and each data input of the SCL4512B is connected to $V_{DD}$, $V_{SS}$, D, or $\bar{D}$ as required. In such fashion, the function is generated.

In the example shown, the first two outputs are the inverse of D, so XO is connected to $\bar{D}$. The next two are HIGH, so X1 is connected to $V_{DD}$, etc.

| INPUT VARIABLES | | | | REQUIRED FUNCTION |
|---|---|---|---|---|
| A | B | C | D | Z |
| L | L | L | L | H |
| L | L | L | H | L |
| L | L | H | L | H |
| L | L | H | H | H |
| L | H | L | L | L |
| L | H | L | H | H |
| L | H | H | L | L |
| L | H | H | H | L |
| H | L | L | L | L |
| . | . | . | . | . |
| . | . | . | . | . |
| . | . | . | . | . |

H = HIGH Level
L = LOW Level
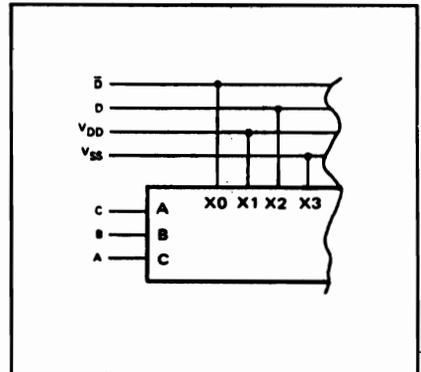
## SCL4514B
## SCL4515B

# CMOS 4-TO-16 LINE DECODERS WITH LATCH

## FEATURES

♦ Strobed Input Latch
♦ Inhibit Control
♦ Selected Output Active High (SCL4514B) or Active Low (SCL4515B)

## DESCRIPTION

The SCL4514B and SCL4515B are two output options of a 4-to-16 Line Decoder with Latched Inputs. The SCL4514B presents a logic "1" at the selected output, and the SCL4515B presents a logic "0" at the selected output. The latches hold the last input data presented prior to the Strobe transition from "1" to "0". Inhibit allows all outputs to be placed at "0" (SCL4514B), or "1" (SCL4515B), regardless of the state of the Data or Strobe inputs.

Applications include code conversion, address decoding, memory selection control, demultiplexing, and readout decoding.

### CONNECTION DIAGRAM
(all packages)



Add suffix for package:

D 24-pin Ceramic
E 24-pin Epoxy
H Chip

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage   $V_{DD} - V_{SS}$   3 to 15   Vdc

Operating Temperature   $T_A$
D, H Device   -55 to +125   °C
E Device   -40 to +85   °C
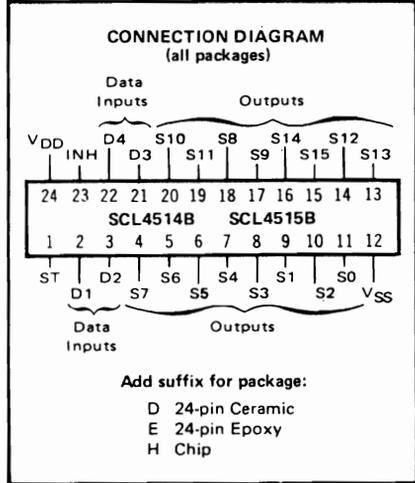
### TRUTH TABLE (Strobe = 1)

| Inhibit | Data Inputs | | | | Selected Output SCL4514B = Logic "1" SCL4515B = Logic "0" |
|---|---|---|---|---|---|
| | D | C | B | A | |
| 0 | 0 | 0 | 0 | 0 | S0 |
| 0 | 0 | 0 | 0 | 1 | S1 |
| 0 | 0 | 0 | 1 | 0 | S2 |
| 0 | 0 | 0 | 1 | 1 | S3 |
| 0 | 0 | 1 | 0 | 0 | S4 |
| 0 | 0 | 1 | 0 | 1 | S5 |
| 0 | 0 | 1 | 1 | 0 | S6 |
| 0 | 0 | 1 | 1 | 1 | S7 |
| 0 | 1 | 0 | 0 | 0 | S8 |
| 0 | 1 | 0 | 0 | 1 | S9 |
| 0 | 1 | 0 | 1 | 0 | S10 |
| 0 | 1 | 0 | 1 | 1 | S11 |
| 0 | 1 | 1 | 0 | 0 | S12 |
| 0 | 1 | 1 | 0 | 1 | S13 |
| 0 | 1 | 1 | 1 | 0 | S14 |
| 0 | 1 | 1 | 1 | 1 | S15 |
| 1 | X | X | X | X | All Outputs = "0", SCL4514B<br>All Outputs = "1", SCL4515B |

X = Don't Care

### BLOCK DIAGRAM



205
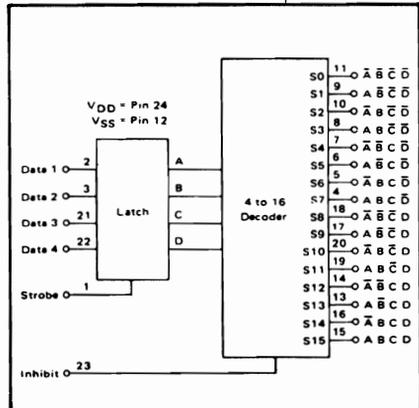
# CMOS
# BINARY UP/DOWN COUNTER

## FEATURES

♦ Internally Synchronous for High Speed
♦ Asynchronous Preset Enable
♦ Asynchronous Reset
♦ Logic Edge-Clocked Design
♦ 6MHz Counting Rate @ 10Vdc
♦ Carry Output for Cascading Stages

## DESCRIPTION

The SCL4516B consists of a four-stage Up/Down Counter with provisions for "look-ahead" carry in both counting modes. The inputs consist of a single Clock, Carry-in (Clock Enable), Reset, Up/Down, Preset Enable, and four individual Jam signals. Four separate buffered Q signals and a Carry-out signal are provided as outputs.

A high Preset Enable signal allows information on the Jam inputs to preset the counter to any state asynchronously with the Clock. A high on the Reset line resets all stages to the "zero" state. The counter is advanced one count at the positive transition of the Clock when the Carry-in and Preset Enable signals are low. Advancement is inhibited when the Carry-in or Preset Enable signals are high. The Carry-out signal is normally high and goes low when the counter reaches its maximum count in the Up mode or the minimum count in the Down mode, provided the Carry-in signal is low. The Carry-in signal in the low state can thus be considered a "Clock Enable." The Carry-in terminal must be connected to $V_{SS}$ when not in use.

The counter counts Up when the Up/Down input is high, and Down when the Up/Down input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

This counter finds primary use in up/down and differential counting and frequency synthesizer applications. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

## CONNECTION DIAGRAM
(all packages)

| $V_{DD}$ | CL | Q3 | P3 | P2 | Q2 | U/D | R |
|------|----|----|----|----|----|-----|---|
| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |

SCL4516B

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|
| PE | Q4 | P4 | P1 | $\overline{CI}$ | Q1 | $\overline{CO}$ | $V_{SS}$ |

Add suffix for package:

C  16-pin Cerdip
D  16-pin Ceramic
E  16-pin Epoxy
F  16-pin Flat
H  Chip

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

| | | | |
|---|---|---|---|
| DC Supply Voltage | $V_{DD} - V_{SS}$ | 3 to 15 | Vdc |
| Operating Temperature | $T_A$ | | |
| C, D, F, H Device | | -55 to +125 | °C |
| E Device | | -40 to +85 | °C |

## BLOCK DIAGRAM



## TRUTH TABLE

| CARRY IN | UP/DOWN | PRESET ENABLE | RESET | ACTION |
|----------|---------|---------------|-------|--------|
| 1 | x | 0 | 0 | No Count |
| 0 | 1 | 0 | 0 | Count Up |
| 0 | 0 | 0 | 0 | Count Down |
| x | x | 1 | 0 | Preset |
| x | x | x | 1 | Reset |

X = Don't Care

## LOGIC DIAGRAM



## TIMING DIAGRAM



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# SCL4518B
# SCL4520B

# CMOS DUAL UP COUNTERS

## FEATURES

♦ Two Independent 4-Bit Counters
♦ Internally Synchronous for High Speed
♦ Dual BCD (SCL4518B) and Dual Binary (SCL4520B) Configurations
♦ Direct Reset
♦ Logic Edge-Clocked Design
♦ Trigger from either Edge of Clock Signal
♦ Static Operation— DC to 5MHz @ 10Vdc

## DESCRIPTION

The SCL4518B Dual BCD Counter and the SCL4520B Dual Binary Counter are constructed with MOS P-channel and N-channel enhancement-mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type-D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the SCL4518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

## TRUTH TABLE

| CLOCK | ENABLE | RESET | ACTION |
|---|---|---|---|
| ⟋ | 1 | 0 | Increment Counter |
| 0 | ⟍ | 0 | Increment Counter |
| ⟋ | X | 0 | No Change |
| X | ⟋ | 0 | No Change |
| ⟋ | 0 | 0 | No Change |
| 1 | ⟍ | 0 | No Change |
| X | X | 1 | Q0 thru Q3 = 0 |

X = Don't Care

## TIMING DIAGRAM
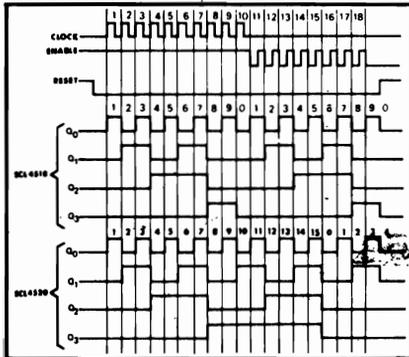


## CONNECTION DIAGRAM
(all packages)
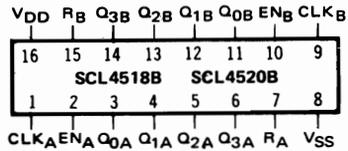


Add suffix for package:

| | |
|---|---|
| C | 16-pin Cerdip |
| D | 16-pin Ceramic |
| E | 16-pin Epoxy |
| F | 16-pin Flat |
| H | Chip |

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

| | | | |
|---|---|---|---|
| DC Supply Voltage | $V_{DD} - V_{SS}$ | 3 to 15 | Vdc |
| Operating Temperature | $T_A$ | | |
| C, D, F, H Device | | -55 to +125 | °C |
| E Device | | -40 to +85 | °C |

## BLOCK DIAGRAM
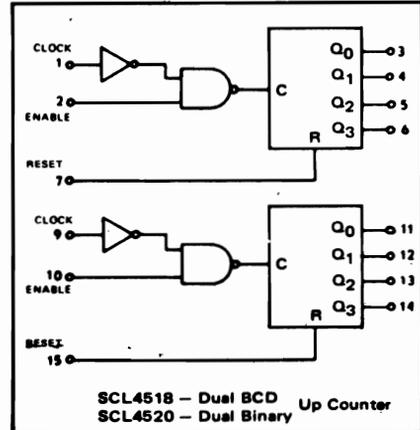


SCL4518 — Dual BCD  Up Counter
SCL4520 — Dual Binary

## SCL4528B

# CMOS DUAL MONOSTABLE MULTIVIBRATOR

## FEATURES

- ◆ Two Independent Multivibrators on One Chip
- ◆ Triggerable from Leading- or Trailing-Edge Pulse
- ◆ Retriggerable
- ◆ Resettable
- ◆ Q and $\overline{Q}$ Buffered Outputs Available
- ◆ Wide Range of Output Pulse Widths

## DESCRIPTION

The SCL4528B Dual Multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application. Timing for the circuit is controlled by an external resistor-capacitor combination ($R_X \cdot C_X$). Adjustment of these components permits generation of output pulse widths from nanoseconds to minutes. Leading-edge and trailing-edge Trigger inputs are provided, and both positive-going and negative-going pulses are available from complementary outputs.

Timing pulses may be terminated at any time by applying a low logic level to the Reset input $C_D$.

### CONNECTION DIAGRAM
(all packages)
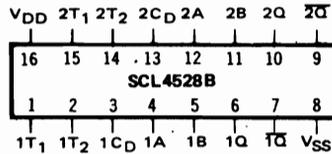
| $V_{DD}$ | $2T_1$ | $2T_2$ | $2C_D$ | 2A | 2B | 2Q | $\overline{2Q}$ |
|---|---|---|---|---|---|---|---|
| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |

**SCL4528B**

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|
| $1T_1$ | $1T_2$ | $1C_D$ | 1A | 1B | 1Q | $\overline{1Q}$ | $V_{SS}$ |

**Add suffix for package:**

| | |
|---|---|
| C | 16-pin Cerdip |
| D | 16-pin Ceramic |
| E | 16-pin Epoxy |
| F | 16-pin Flat |
| H | Chip |

## RECOMMENDED OPERATING CONDITIONS

**For maximum reliability:**

| | | | |
|---|---|---|---|
| DC Supply Voltage | $V_{DD} - V_{SS}$ | 3 to 15 | Vdc |
| Operating Temperature | $T_A$ | | |
| C, D, F, H Device | | -55 to +125 | °C |
| E Device | | -40 to +85 | °C |

### FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $C_D$ | A | B | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | ↑ | H | ⊓ | ⊔ |
| H | L | ↓ | ⊓ | ⊔ |

H = High Level (Steady State)
L = Low Level (Steady State)
↑ = Transition, Low-to-High
↓ = Transition, High-to-Low
X = Irrelevant (Inc. Transitions)
⊓ = One High-Level Pulse
⊔ = One Low-Level Pulse

### BLOCK DIAGRAM
(one of two devices)
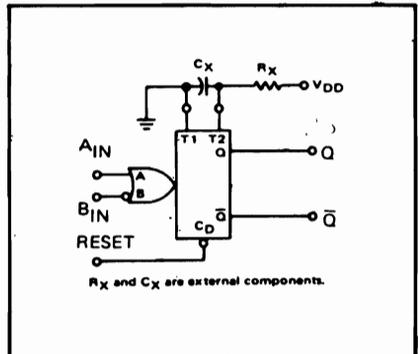


$R_X$ and $C_X$ are external components.

## SCL4543B
### Preliminary

# BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

## FEATURES

♦ Phase Input Signal Reproduced on Outputs for Liquid Crystal Display
♦ Latched Storage of Input Code
♦ Blanking Input for Display Intensity Modulation
♦ Readout Blanking for Illegal Input Combinations
♦ Pin Compatible with CD4056A (with Pin 7 Tied to $V_{SS}$)
♦ Balanced Output Drive Current Specifications

## DESCRIPTION

The SCL4543B BCD-to-7 Segment Latch/Decoder/Driver is designed for use with liquid crystal readouts and is constructed with complementary MOS (CMOS) enhancement-mode devices. The circuit provides the functions of a 4-bit storage latch and a 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The Phase (Ph), Blanking (BI), and Latch Disable (LD) inputs are used to reverse the truth-table phase, blank the display, and store a BCD code, respectively. For liquid crystal readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter,

DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

### CONNECTION DIAGRAM
(all packages)

Add suffix for package:

| | |
|---|---|
| C | 16-pin Cerdip |
| D | 16-pin Ceramic |
| E | 16-pin Epoxy |
| F | 16-pin Flat |
| H | Chip |

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

| | | | |
|---|---|---|---|
| DC Supply Voltage | $V_{DD} - V_{SS}$ | 3 to 15 | Vdc |
| Operating Temperature | $T_A$ | | |
| C, D, F, H Device | | -55 to +125 | °C |
| E Device | | -40 to +85 | °C |

### TRUTH TABLE

| INPUTS | | | | | | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LD | BI | Ph* | D | C | B | A | a | b | c | d | e | f | g | Display |
| X | 1 | 0 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 9 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 0 | 0 | X | X | X | X | ** | | | | | | | ** |
| ↑ | ↑ | 1 | | | ↑ | | Inverse of Output Combinations Above | | | | | | | Display as above |

X = Don't care
↑ = Above Combinations
* = For liquid crystal readouts, apply a square wave to Ph
   For common cathode LED readouts, select Ph = 0
   For common anode LED readouts, select Ph = 1
** = Depends upon the BCD code previously applied when LD = 1.

### BLOCK DIAGRAM

$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8

### DISPLAY

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## SCL4581B

# CMOS 4-BIT ARITHMETIC LOGIC UNIT

## FEATURES

♦ Function and Pinout Equivalent to 74181
♦ Provides 16 Logic Functions and 16 Arithmetic Functions
♦ Comparator Function
♦ Positive or Negative Logic
♦ Full Look-Ahead for High-Speed Operations on Long Words

## DESCRIPTION

The SCL4581B is a CMOS 4-Bit Arithmetic Logic Unit (ALU) capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the Mode Control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the Select inputs (S0 thru S3) with the Mode Control input high, while the desired arithmetic operation is selected by applying a low voltage to the Mode Control input, the required level to Carry in, and the appropriate word to the Select inputs. The Word inputs and Function outputs can be operated with either active-high or active-low data.

Carry propagate (P) and Carry generate (G) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the SCL4582B as a second-order look-ahead block. An inverted Ripple-Carry input ($C_n$) and a Ripple-Carry output ($C_{n+4}$) are included for ripple-through operation.

### CONNECTION DIAGRAM
(all packages)



Add suffix for package:

D   24-pin Ceramic
E   24-pin Epoxy
H   Chip

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage   $V_{DD} - V_{SS}$   3 to 15   Vdc

Operating Temperature   $T_A$
   D, H Device   -55 to +125   °C
   E Device   -40 to +85   °C

### BLOCK DIAGRAM



### ALU SIGNAL DESIGNATIONS

| Designation | Pin Nos. | Function |
|---|---|---|
| A3, A2, A1, A0 | 19, 21, 23, 2 | Word A Inputs |
| B3, B2, B1, B0 | 18, 20, 22, 1 | Word B Inputs |
| S3, S2, S1, S0 | 3, 4 5, 6 | Function-Select Inputs |
| $C_n$ | 7 | Inv. Carry Input |
| MC | 8 | Mode Control Input |
| F3, F2, F1, F0 | 13, 11, 10, 9 | Function Outputs |
| A = B | 14 | Comparator Output |
| P | 15 | Carry Propagate Output |
| $C_{n+4}$ | 16 | Inv. Carry Output |
| G | 17 | Carry Generate Output |
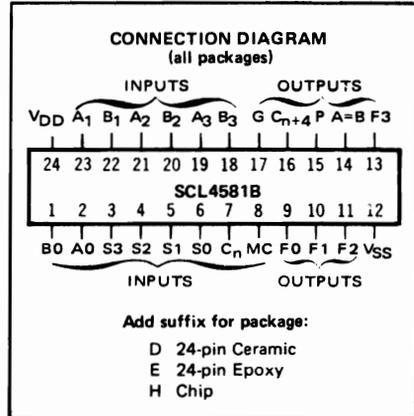
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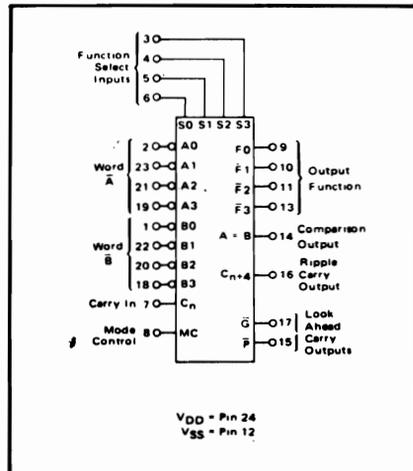
# ALU FUNCTION GENERATION

The SCL4581B can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.
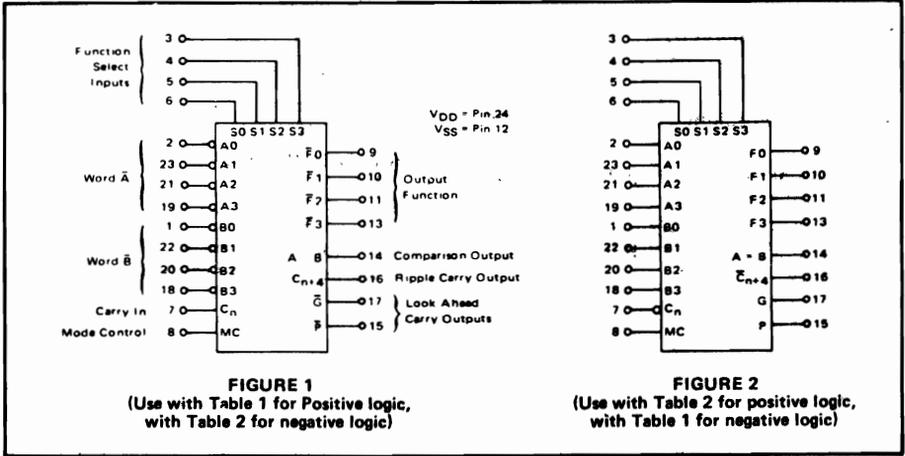


**FIGURE 1**
(Use with Table 1 for Positive logic,
with Table 2 for negative logic)

**FIGURE 2**
(Use with Table 2 for positive logic,
with Table 1 for negative logic)

## TABLE 1

| SELECTION | | | | MC = H | MC = L, ARITHMETIC OPERATIONS | |
|---|---|---|---|---|---|---|
| | | | | LOGIC | $C_n = L$ | $C_n = H$ |
| S3 | S2 | S1 | S0 | FUNCTIONS | (no carry) | (with carry) |
| L | L | L | L | F = $\bar{A}$ | F = A MINUS 1 | F = A |
| L | L | L | H | F = $\overline{AB}$ | F = AB MINUS 1 | F = AB |
| L | L | H | L | F = $\bar{A}$ + B | F = $A\bar{B}$ MINUS 1 | F = $A\bar{B}$ |
| L | L | H | H | F = 1 | F = MINUS 1 (2's COMP) | F = ZERO |
| L | H | L | L | F = $\overline{A+B}$ | F = A PLUS (A + $\bar{B}$) | F = A PLUS (A + $\bar{B}$) PLUS 1 |
| L | H | L | H | F = $\bar{B}$ | F = AB PLUS (A + $\bar{B}$) | F = AB PLUS (A + $\bar{B}$) PLUS 1 |
| L | H | H | L | F = A $\oplus$ B | F = A MINUS B MINUS 1 | F = A MINUS B |
| L | H | H | H | F = A + $\bar{B}$ | F = A + $\bar{B}$ | F = (A + $\bar{B}$) PLUS 1 |
| H | L | L | L | F = $\bar{A}$B | F = A PLUS (A + B) | F = A PLUS (A + B) PLUS 1 |
| H | L | L | H | F = A $\oplus$ B | F = A PLUS B | F = A PLUS B PLUS 1 |
| H | L | H | L | F = B | F = $A\bar{B}$ PLUS (A + B) | F = $A\bar{B}$ PLUS (A + B) PLUS 1 |
| H | L | H | H | F = A + B | F = (A + B) | F = (A + B) PLUS 1 |
| H | H | L | L | F = 0 | F = A PLUS A* | F = A PLUS A PLUS 1 |
| H | H | L | H | F = $A\bar{B}$ | F = AB PLUS A | F = AB PLUS A PLUS 1 |
| H | H | H | L | F = AB | F = $A\bar{B}$ PLUS A | F = $A\bar{B}$ PLUS A PLUS 1 |
| H | H | H | H | F = A | F = A | F = A PLUS 1 |

## TABLE 2

| SELECTION | | | | MC = H | MC = L; ARITHMETIC OPERATIONS | |
|---|---|---|---|---|---|---|
| | | | | LOGIC | $\bar{C}_n = H$ | $\bar{C}_n = L$ |
| S3 | S2 | S1 | S0 | FUNCTIONS | (no carry) | (with carry) |
| L | L | L | L | F = $\bar{A}$ | F = A | F = A PLUS 1 |
| L | L | L | H | F = $\bar{A}$+$\bar{B}$ | F = A + B | F = (A + B) PLUS 1 |
| L | L | H | L | F = $\bar{A}$B | F = A + $\bar{B}$ | F = (A + $\bar{B}$) PLUS 1 |
| L | L | H | H | F = 0 | F = MINUS 1 (2's COMPL) | F = ZERO |
| L | H | L | L | F = $\overline{AB}$ | F = A PLUS $A\bar{B}$ | F = A PLUS $A\bar{B}$ PLUS 1 |
| L | H | L | H | F = $\bar{B}$ | F = (A + B) PLUS $A\bar{B}$ | F = (A + B) PLUS $A\bar{B}$ PLUS 1 |
| L | H | H | L | F = A $\oplus$ B | F = A MINUS B MINUS 1 | F = A MINUS B |
| L | H | H | H | F = $A\bar{B}$ | F = $A\bar{B}$ MINUS 1 | F = $A\bar{B}$ |
| H | L | L | L | F = $\bar{A}$ + B | F = A PLUS AB | F = A PLUS AB PLUS 1 |
| H | L | L | H | F = A $\oplus$ B | F = A PLUS B | F = A PLUS B PLUS 1 |
| H | L | H | L | F = B | F = (A + $\bar{B}$) PLUS AB | F = (A + $\bar{B}$) PLUS AB PLUS 1 |
| H | L | H | H | F = AB | F = AB MINUS 1 | F = AB |
| H | H | L | L | F = 1 | F = A PLUS A* | F = A PLUS A PLUS 1 |
| H | H | L | H | F = A + $\bar{B}$ | F = (A + $\bar{B}$) PLUS A | F = (A + $\bar{B}$) PLUS A PLUS 1 |
| H | H | H | L | F = A + B | F = (A + $\bar{B}$) PLUS A | F = (A + $\bar{B}$) PLUS A PLUS 1 |
| H | H | H | H | F = A | F = A MINUS 1 | F = A |

*Each bit is shifted to the next more significant position.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the A and B inputs is provided using the A=B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the $C_{n+4}$ output can be used to indicate relative magnitude as shown in this table:

| Data Level | $C_n$ | $C_{n+4}$ | Magnitude |
|---|---|---|---|
| Active High | H | H | A ≤ B |
| | L | H | A < B |
| | H | L | A > B |
| | L | L | A ≥ B |
| Active Low | L | L | A ≤ B |
| | H | L | A < B |
| | L | H | A > B |
| | H | H | A ≥ B |

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# 8080A/8080A-1/8080A-2
# 8-BIT N-CHANNEL MICROPROCESSOR

- **TTL Drive Capability**

- **2 $\mu$s ( − 1:1.3 $\mu$s, − 2:1.5 $\mu$s) Instruction Cycle**

- **Powerful Problem Solving Instruction Set**

- **6 General Purpose Registers and an Accumulator**

- **16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**

- **16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**

- **Decimal, Binary, and Double Precision Arithmetic**

- **Ability to Provide Priority Vectored Interrupts**

- **512 Directly Addressed I/O Ports**

- **Available in EXPRESS**
  **− Standard Temperature Range**

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.

**NOTE:**
The 8080A is functionally and electrically compatible with the Intel® 8080.



**Figure 1. Block Diagram**



**Figure 2. Pin Configuration**

## Table 1. Pin Description

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| $A_{15}$-$A_0$ | O | **Address Bus:** The address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. $A_0$ is the least significant address bit. |
| $D_7$-$D_0$ | I/O | **Data Bus:** The data bus provides bi-directional communication betweeen the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. $D_0$ is the least significant bit. |
| SYNC | O | **Synchronizing Signal:** The SYNC pin provides a signal to indicate the beginning of each machine cycle. |
| DBIN | O | **Data Bus In:** The DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O. |
| READY | I | **Ready:** The READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU. |
| WAIT | O | **Wait:** The WAIT signal acknowledges that the CPU is in a WAIT state. |
| $\overline{WR}$ | O | **Write:** The $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0). |
| HOLD | I | **Hold:** The HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these busses for the current machine cycle. It is recognized under the following conditions:<br>• the CPU is in the HALT state.<br>• the CPU is in the T2 or TW state and the READY signal is active. As a result of entering the HOLD state the CPU ADDRESS BUS ($A_{15}$-$A_0$) and DATA BUS ($D_7$-$D_0$) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin. |
| HLDA | O | **Hold Acknowledge:** The HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:<br>• T3 for READ memory or input.<br>• The Clock Period following T3 for WRITE memory or OUTPUT operation.<br>In either case, the HLDA signal appears after the rising edge of $\phi_2$. |
| INTE | O | **Interrupt Enable:** Indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal. |
| INT | I | **Interrupt Request:** The CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request. |
| RESET[1] | I | **Reset:** While the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared. |
| $V_{SS}$ | | **Ground:** Reference. |
| $V_{DD}$ | | **Power:** +12 ±5% Volts. |
| $V_{CC}$ | | **Power:** +5 ±5% Volts. |
| $V_{BB}$ | | **Power:** −5 ±5% Volts. |
| $\phi_1$, $\phi_2$ | | **Clock Phases:** 2 externally supplied clock phases. (non TTL compatible) |

# INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to

increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

## Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

$$| D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0 |$$
DATA WORD
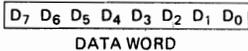
The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

| $D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0$ | OP CODE
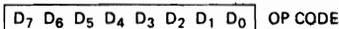
TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

| $D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0$ | OP CODE
| $D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0$ | OPERAND
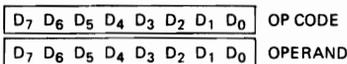
Immediate mode or I/O instructions

Three Byte Instructions

| $D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0$ | OP CODE
| $D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0$ | LOW ADDRESS OR OPERAND 1
| $D_7 \ D_6 \ D_5 \ D_4 \ D_3 \ D_2 \ D_1 \ D_0$ | HIGH ADDRESS OR OPERAND 2
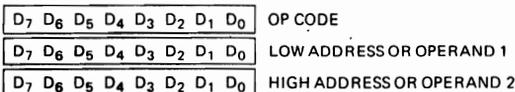
Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

## Table 2. Instruction Set Summary

| Mnemonic | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operations Description | Clock Cycles [2] |
|---|---|---|---|---|---|---|---|---|---|---|
| **MOVE, LOAD, AND STORE** | | | | | | | | | | |
| MOVr1,r2 | 0 | 1 | D | D | D | S | S | S | Move register to register | 5 |
| MOV M,r | 0 | 1 | 1 | 1 | 0 | S | S | S | Move register to memory | 7 |
| MOV r,M | 0 | 1 | D | D | D | 1 | 1 | 0 | Move memory to register | 7 |
| MVI r | 0 | 0 | D | D | D | 1 | 1 | 0 | Move immediate register | 7 |
| MVI M | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Move immediate memory | 10 |
| LXI B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Load immediate register Pair B & C | 10 |
| LXI D | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Load immediate register Pair D & E | 10 |
| LXI H | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Load immediate register Pair H & L | 10 |
| STAX B | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Store A indirect | 7 |
| STAX D | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Store A indirect | 7 |
| LDAX B | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Load A indirect | 7 |
| LDAX D | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | Load A indirect | 7 |
| STA | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Store A direct | 13 |
| LDA | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | Load A direct | 13 |
| SHLD | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | Store H & L direct | 16 |
| LHLD | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Load H & L direct | 16 |
| XCHG | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Exchange D & E, H & L Registers | 4 |
| **STACK OPS** | | | | | | | | | | |
| PUSH B | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Push register Pair B & C on stack | 11 |
| PUSH D | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | Push register Pair D & E on stack | 11 |
| PUSH H | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | Push register Pair H & L on stack | 11 |
| PUSH PSW | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | Push A and Flags on stack | 11 |
| POP B | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | Pop register Pair B & C off stack | 10 |
| POP D | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | Pop register Pair D & E off stack | 10 |
| POP H | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Pop register Pair H & L off stack | 10 |
| POP PSW | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | Pop A and Flags off stack | 10 |
| XTHL | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Exchange top of stack, H & L | 18 |
| SPHL | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | H & L to stack pointer | 5 |
| LXI SP | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | Load immediate stack pointer | 10 |
| INX SP | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Increment stack pointer | 5 |
| DCX SP | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | Decrement stack pointer | 5 |
| **JUMP** | | | | | | | | | | |
| JMP | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | Jump unconditional | 10 |
| JC | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Jump on carry | 10 |
| JNC | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | Jump on no carry | 10 |
| JZ | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | Jump on zero | 10 |
| JNZ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | Jump on no zero | 10 |
| JP | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | Jump on positive | 10 |
| JM | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | Jump on minus | 10 |
| JPE | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | Jump on parity even | 10 |

| Mnemonic | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operations Description | Clock Cycles [2] |
|---|---|---|---|---|---|---|---|---|---|---|
| JPO | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Jump on parity odd | 10 |
| PCHL | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | H & L to program counter | 5 |
| **CALL** | | | | | | | | | | |
| CALL | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | Call unconditional | 17 |
| CC | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Call on carry | 11/17 |
| CNC | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | Call on no carry | 11/17 |
| CZ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | Call on zero | 11/17 |
| CNZ | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Call on no zero | 11/17 |
| CP | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | Call on positive | 11/17 |
| CM | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Call on minus | 11/17 |
| CPE | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0. | Call on parity even | 11/17 |
| CPO | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | Call on parity odd | 11/17 |
| **RETURN** | | | | | | | | | | |
| RET | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | Return | 10 |
| RC | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | Return on carry | 5/11 |
| RNC | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | Return on no carry | 5/11 |
| RZ | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Return on zero | 5/11 |
| RNZ | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Return on no zero | 5/11 |
| RP | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Return on positive | 5/11 |
| RM | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Return on minus | 5/11 |
| RPE | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Return on parity even | 5/11 |
| RPO | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Return on parity odd | 5/11 |
| **RESTART** | | | | | | | | | | |
| RST | 1 | 1 | A | A | A | 1 | 1 | 1 | Restart | 11 |
| **INCREMENT AND DECREMENT** | | | | | | | | | | |
| INR r | 0 | 0 | D | D | D | 1 | 0 | 0 | Increment register | 5 |
| DCR r | 0 | 0 | D | D | D | 1 | 0 | 1 | Decrement register | 5 |
| INR M | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Increment memory | 10 |
| DCR M | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Decrement memory | 10 |
| INX B | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Increment B & C registers | 5 |
| INX D | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Increment D & E registers | 5 |
| INX H | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Increment H & L registers | 5 |
| DCX B | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | Decrement B & C | 5 |
| DCX D | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | Decrement D & E | 5 |
| DCX H | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Decrement H & L | 5 |
| **ADD** | | | | | | | | | | |
| ADD r | 1 | 0 | 0 | 0 | 0 | S | S | S | Add register to A | 4 |
| ADC r | 1 | 0 | 0 | 0 | 1 | S | S | S | Add register to A with carry | 4 |
| ADD M | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | Add memory to A | 7 |
| ADC M | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Add memory to A with carry | 7 |
| ADI | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | Add immediate to A | 7 |
| ACI | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | Add immediate to A with carry | 7 |
| DAD B | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | Add B & C to H & L | 10 |
| DAD D | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | Add D & E to H & L | 10 |
| DAD H | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | Add H & L to H & L | 10 |
| DAD SP | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Add stack pointer to H & L | 10 |

### Summary of Processor Instructions (Cont.)

| Mnemonic | Instruction Code [1] D7 D6 D5 D4 D3 D2 D1 D0 | Operations Description | Clock Cycles [2] |
|---|---|---|---|
| **SUBTRACT** | | | |
| SUB r | 1 0 0 1 0 S S S | Subtract register from A | 4 |
| SBB r | 1 0 0 1 1 S S S | Subtract register from A with borrow | 4 |
| SUB M | 1 0 0 1 0 1 1 0 | Subtract memory from A | 7 |
| SBB M | 1 0 0 1 1 1 1 0 | Subtract memory from A with borrow | 7 |
| SUI | 1 1 0 1 0 1 1 0 | Subtract immediate from A | 7 |
| SBI | 1 1 0 1 1 1 1 0 | Subtract immediate from A with borrow | 7 |
| **LOGICAL** | | | |
| ANA r | 1 0 1 0 0 S S S | And register with A | 4 |
| XRA r | 1 0 1 0 1 S S S | Exclusive Or register with A | 4 |
| ORA r | 1 0 1 1 0 S S S | Or register with A | 4 |
| CMP r | 1 0 1 1 1 S S S | Compare register with A | 4 |
| ANA M | 1 0 1 0 0 1 1 0 | And memory with A | 7 |
| XRA M | 1 0 1 0 1 1 1 0 | Exclusive Or memory with A | 7 |
| ORA M | 1 0 1 1 0 1 1 0 | Or memory with A | 7 |
| CMP M | 1 0 1 1 1 1 1 0 | Compare memory with A | 7 |
| ANI | 1 1 1 0 0 1 1 0 | And immediate with A | 7 |
| XRI | 1 1 1 0 1 1 1 0 | Exclusive Or immediate with A | 7 |
| ORI | 1 1 1 1 0 1 1 0 | Or immediate with A | 7 |
| CPI | 1 1 1 1 1 1 1 0 | Compare immediate with A | 7 |

| Mnemonic | Instruction Code [1] D7 D6 D5 D4 D3 D2 D1 D0 | Operations Description | Clock Cycles [2] |
|---|---|---|---|
| **ROTATE** | | | |
| RLC | 0 0 0 0 0 1 1 1 | Rotate A left | 4 |
| RRC | 0 0 0 0 1 1 1 1 | Rotate A right | 4 |
| RAL | 0 0 0 1 0 1 1 1 | Rotate A left through carry | 4 |
| RAR | 0 0 0 1 1 1 1 1 | Rotate A right through carry | 4 |
| **SPECIALS** | | | |
| CMA | 0 0 1 0 1 1 1 1 | Complement A | 4 |
| STC | 0 0 1 1 0 1 1 1 | Set carry | 4 |
| CMC | 0 0 1 1 1 1 1 1 | Complement carry | 4 |
| DAA | 0 0 1 0 0 1 1 1 | Decimal adjust A | 4 |
| **INPUT/OUTPUT** | | | |
| IN | 1 1 0 1 1 0 1 1 | Input | 10 |
| OUT | 1 1 0 1 0 0 1 1 | Output | 10 |
| **CONTROL** | | | |
| EI | 1 1 1 1 1 0 1 1 | Enable Interrupts | 4 |
| DI | 1 1 1 1 0 0 1 1 | Disable Interrupt | 4 |
| NOP | 0 0 0 0 0 0 0 0 | No-operation | 4 |
| HLT | 0 1 1 1 0 1 1 0 | Halt | 7 |

**NOTES:**
1. DDD or SSS: B=000, C=001, D=010, E=011, H=100, L=101, Memory=110, A=111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.
*All mnemonics copyright ©Intel Corporation 1977

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# 8085AH/8085AH-2/8085AH-1
## 8-BIT HMOS MICROPROCESSORS

- Single +5V Power Supply with 10% Voltage Margins
- 3 MHz, 5 MHz and 6 MHz Selections Available
- 20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz
- 1.3 $\mu$s Instruction Cycle (8085AH); 0.8 $\mu$s (8085AH-2); 0.67 $\mu$s (8085AH-1)
- 100% Compatible with 8085A
- 100% Software Compatible with 8080A
- On-Chip Clock Generator (with External Crystal, LC or RC Network)

- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an 8080A-Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel* 8085AH is a complete 8 bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085AH (CPU), 8156H (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085AH.

The 8085AH incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155H/8156H/8355/8755A memory products allow a direct interface with the 8085AH.
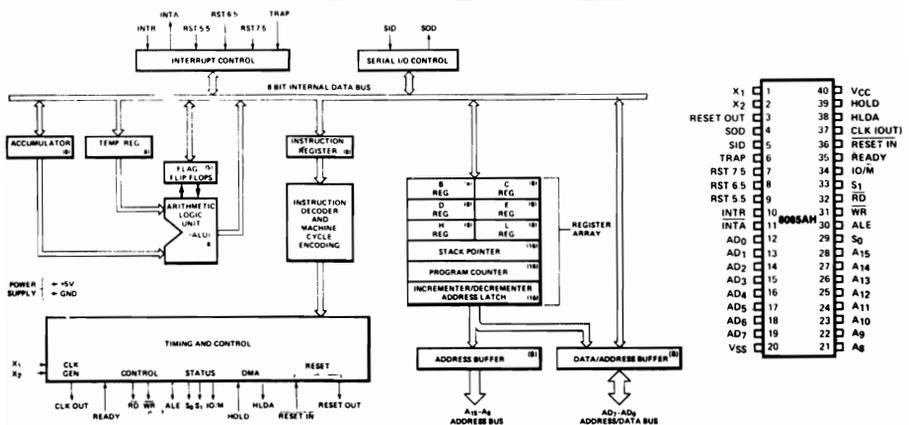


Figure 1. 8085AH CPU Functional Block Diagram
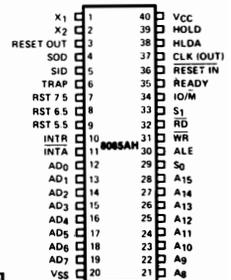
Figure 2. 8085AH Pin Configuration

### Table 1. Pin Description

| Symbol | Type | Name and Function |
|---|---|---|
| A₈–A₁₅ | O | **Address Bus:** The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET |
| AD₀—₇ | I/O | **Multiplexed Address/Data Bus:** Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles |
| ALE | O | **Address Latch Enable:** It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated. |
| S₀, S₁, and IO/M̄ | O | **Machine Cycle Status:** |

| IO/M̄ | S₁ | S₀ | Status |
|---|---|---|---|
| 0 | 0 | 1 | Memory write |
| 0 | 1 | 0 | Memory read |
| 1 | 0 | 1 | I/O write |
| 1 | 1 | 0 | I/O read |
| 0 | 1 | 1 | Opcode fetch |
| 1 | 1 | 1 | Opcode fetch |
| 1 | 1 | 1 | Interrupt Acknowledge |
| * | 0 | 0 | Halt |
| * | X | X | Hold |
| * | X | X | Reset |

* = 3-state (high impedance)
X = unspecified

S₁ can be used as an advanced R/W̄ status. IO/M̄, S₀ and S₁ become valid at the beginning of a machine cycle and remain stable throughout the cycle The falling edge of ALE may be used to latch the state of these lines.

| Symbol | Type | Name and Function |
|---|---|---|
| R̄D̄ | O | **Read Control:** A low level on R̄D̄ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET |
| W̄R̄ | O | **Write Control:** A low level on W̄R̄ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of W̄R̄. 3-stated during Hold and Halt modes and during RESET |
| READY | I | **Ready:** If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times. |
| HOLD | I | **Hold:** Indicates that another master is requesting the use of the address and data buses The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data R̄D̄, W̄R̄, and IO/M̄ lines are 3-stated. |
| HLDA | O | **Hold Acknowledge:** Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low. |
| INTR | I | **Interrupt Request:** Is used as a general purpose interrupt It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states If it is active, the Program Counter (PC) will be inhibited from incrementing and an ĪNT̄Ā will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted. |
| ĪNT̄Ā | O | **Interrupt Acknowledge:** Is used instead of (and has the same timing as) R̄D̄ during the Instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port. |
| RST 5.5 RST 6.5 RST 7.5 | I | **Restart Interrupts:** These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction. |

### Table 1. Pin Description (Continued)

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| TRAP | I | **Trap:** Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.) |
| RESET IN | I | **Reset In:** Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, RESET IN must remain low for at least 10 ms after minimum $V_{CC}$ has been reached. For proper reset operation after the power-up duration, RESET IN should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as RESET IN is applied. |

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| RESET OUT | O | **Reset Out:** Reset Out indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods. |
| $X_1$, $X_2$ | I | **$X_1$ and $X_2$:** Are connected to a crystal, LC, or RC network to drive the internal clock generator. $X_1$ can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency. |
| CLK | ` | **Clock:** Clock output for use as a system clock. The period of CLK is twice the $X_1$, $X_2$ input period. |
| SID | I | **Serial Input Data Line:** The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed. |
| SOD | O | **Serial Output Data Line:** The output SOD is set or reset as specified by the SIM instruction. |
| $V_{CC}$ | | **Power:** +5 volt supply. |
| $V_{SS}$ | | **Ground:** Reference. |

### Table 2. Interrupt Priority, Restart Address, and Sensitivity

| Name | Priority | Address Branched To (1) When Interrupt Occurs | Type Trigger |
|------|----------|-----------------------------------------------|--------------|
| TRAP | 1 | 24H | Rising edge AND high level until sampled. |
| RST 7.5 | 2 | 3CH | Rising edge (latched). |
| RST 6.5 | 3 | 34H | High level until sampled. |
| RST 5.5 | 4 | 2CH | High level until sampled. |
| INTR | 5 | See Note (2). | High level until sampled. |

**NOTES:**
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.



TYPICAL POWER-ON RESET RC VALUES*
$R_1$ = 75 KΩ
$C_1$ = 1 μF

*VALUES MAY HAVE TO VARY DUE TO APPLIED POWER SUPPLY RAMP UP TIME.
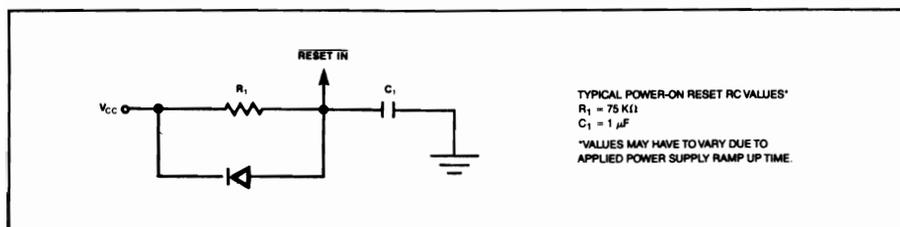
## FUNCTIONAL DESCRIPTION

The 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel, depletion load, silicon gate technology (HMOS), and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085AH), 5 MHz (8085AH-2), or 6 MHz (8085AH-1), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (8085AH), a RAM/IO (8156H), and a ROM or EPROM/IO chip (8355 or 8755A).

The 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085AH register set is as follows:

| Mnemonic | Register | Contents |
|---|---|---|
| ACC or A | Accumulator | 8 bits |
| PC | Program Counter | 16-bit address |
| BC,DE,HL | General-Purpose Registers; data pointer (HL) | 8 bits x 6 or 16 bits x 3 |
| SP | Stack Pointer | 16-bit address |
| Flags or F | Flag Register | 5 flags (8-bit space) |

The 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085AH provides $\overline{RD}$, $\overline{WR}$, $S_0$, $S_1$, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085AH has three maskable, vector interrupt pins, one nonmaskable TRAP interrupt, and a bus vectored interrupt, INTR.

## INTERRUPT AND SERIAL I/O

The 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 2.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive*.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request (a normally high level signal with a low going pulse is recommended for highest system noise immunity). The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$. (See SIM, Chapter 5 of the MCS-80/85 User's Manual.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive*. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 4 illustrates the TRAP interrupt request circuitry within the 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

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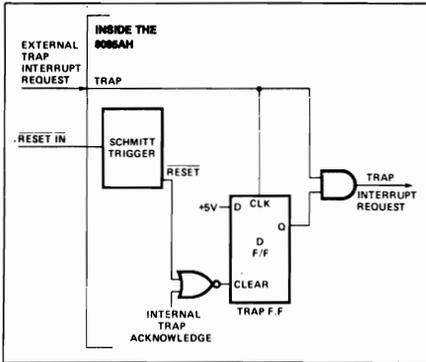
**Figure 4. TRAP and RESET IN Circuit**

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5–7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled. See the description of the RIM instruction in the MCS-80/85 Family User's Manual.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

## DRIVING THE $X_1$ AND $X_2$ INPUTS

You may drive the clock inputs of the 8085AH, 8085AH-2, or 8085AH-1 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The crystal frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the 8085AH is operated with a 6 MHz crystal (for 3 MHz clock), the 8085AH-2 operated with a 10 MHz crystal (for 5 MHz clock), and the 8085AH-1 can be operated with a 12 MHz crystal (for 6 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
$C_L$ (load capacitance) $\leqslant$ 30 pF
$C_S$ (shunt capacitance) $\leqslant$ 7 pF
$R_S$ (equivalent shunt resistance) $\leqslant$ 75 Ohms
Drive level: 10 mW
Frequency tolerance: $\pm$.005% (suggested)

Note the use of the 20 pF capacitor between $X_2$ and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the 8085AH, providing that its frequency tolerance of approximately $\pm$10% is acceptable. The components are chosen from the formula:

$$f = \frac{1}{2\pi\sqrt{L(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for $C_{ext}$ that is at least twice that of $C_{int}$, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

An RC circuit may be used as the frequency-determining network for the 8085AH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component cost. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

Figure 5 shows the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4V and maximum low level voltage of 0.8V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to $X_1$ and leave $X_2$ open-circuited (Figure 5D). If the driving frequency is from 6 MHz to 12 MHz, stability of the clock generator will be improved by driving both $X_1$ and $X_2$ with a push-pull source (Figure 5E). To prevent self-oscillation of the 8085AH, be sure that $X_2$ is not coupled back to $X_1$ through the driving circuit.

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a. Quartz Crystal Clock Driver

*20 pF CAPACITORS REQUIRED FOR CRYSTAL FREQUENCY ≤ 4 MHz ONLY.

b. LC Tuned Circuit Clock Driver

c. RC Circuit Clock Driver

d. 1-6 MHz Input Frequency External Clock Driver Circuit

*X₂ LEFT FLOATING

e. 1-12 MHz Input Frequency External Clock Driver Circuit
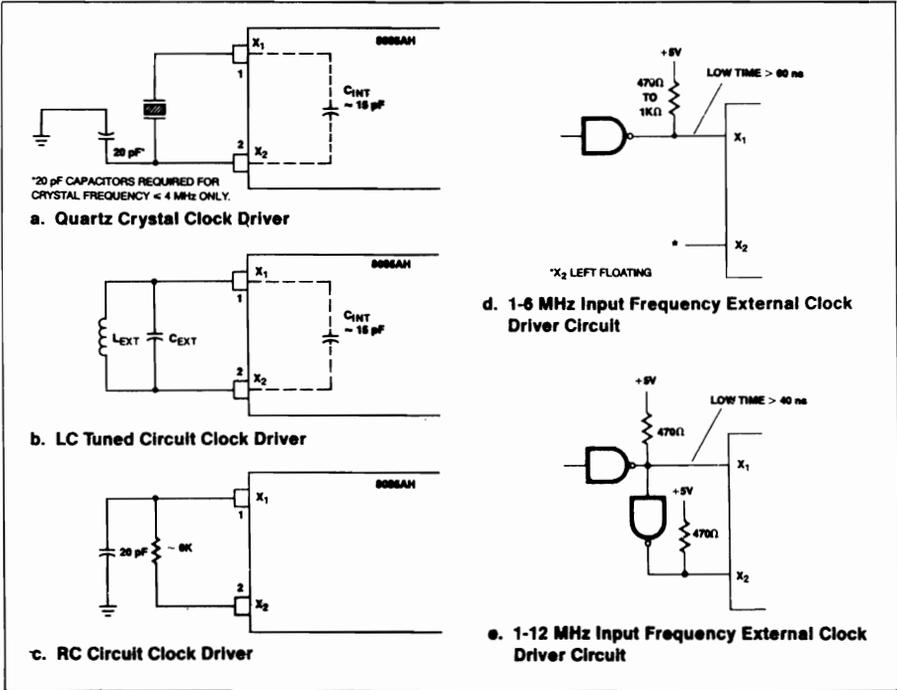
**Figure 5. Clock Driver Circuits**

## GENERATING AN 8085AH WAIT STATE

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in Figure 6 may be used to insert one WAIT state in each 8085AH machine cycle.

The D flip-flops should be chosen so that
• CLK is rising edge-triggered
• CLEAR is low-level active.



*ALE AND CLK (OUT) SHOULD BE BUFFERED IF CLK INPUT OF LATCH EXCEEDS 8085AH IOL OR IOH.
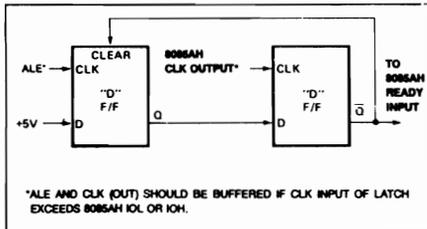
**Figure 6. Generation of a Wait State for 8085AH CPU**
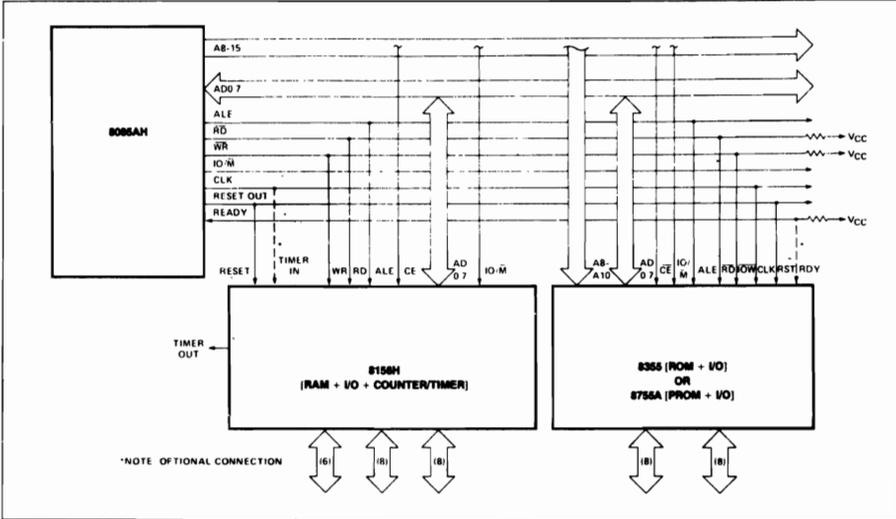
**Figure 8. MCS-85® Minimum System (Memory Mapped I/O)**
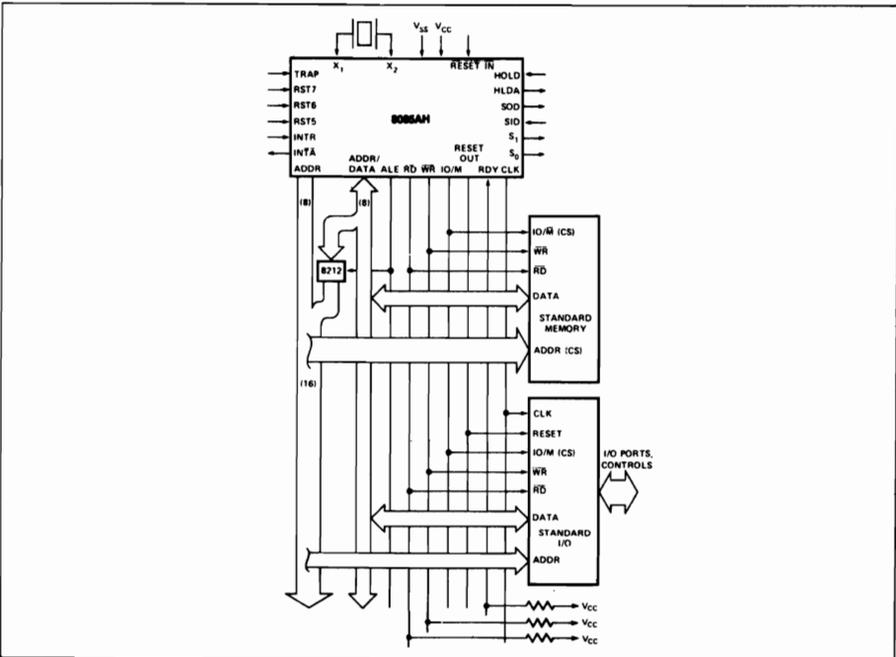


**Figure 9. MCS-85® System (Using Standard Memories)**

As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085AH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

## SYSTEM INTERFACE

The 8085AH family includes memory components, which are directly compatible to the 8085AH CPU. For example, a system consisting of the three chips, 8085AH, 8156H, and 8355 will have the following features:

- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in Figure 7.

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby; using the memory address for I/O manipulation. Figure 8 shows the system configuration of Memory Mapped I/O using 8085AH.

The 8085AH CPU can also interface with the standard memory that does *not* have the multiplexed address/data bus. It will require a simple 8212 (8-bit latch) as shown in Figure 9.



**Figure 7. 8085AH Minimum System (Standard I/O Technique)**

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## BASIC SYSTEM TIMING

The 8085AH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 10 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, $S_1$, $S_0$) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 3.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the $T_1$ state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of READY or HOLD inputs). Any T state must be one of ten possible states, shown in Table 4.

### Table 3. 8085AH Machine Cycle Chart

| MACHINE CYCLE | | STATUS | | | CONTROL | | |
|---|---|---|---|---|---|---|---|
| | | $IO/\overline{M}$ | S1 | S0 | $\overline{RD}$ | $\overline{WR}$ | $\overline{INTA}$ |
| OPCODE FETCH | (OF) | 0 | 1 | 1 | 0 | 1 | 1 |
| MEMORY READ | (MR) | 0 | 1 | 0 | 0 | 1 | 1 |
| MEMORY WRITE | (MW) | 0 | 0 | 1 | 1 | 0 | 1 |
| I/O READ | (IOR) | 1 | 1 | 0 | 0 | 1 | 1 |
| I/O WRITE | (IOW) | 1 | 0 | 1 | 1 | 0 | 1 |
| ACKNOWLEDGE OF INTR | (INA) | 1 | 1 | 1 | 1 | 1 | 0 |
| BUS IDLE | (BI). DAD | 0 | 1 | 0 | 1 | 1 | 1 |
| | ACK. OF RST,TRAP | 1 | 1 | 1 | 1 | 1 | 1 |
| | HALT | TS | 0 | 0 | TS | TS | 1 |

### Table 4. 8085AH Machine State Chart

| Machine State | Status & Buses | | | | Control | | |
|---|---|---|---|---|---|---|---|
| | S1,S0 | $IO/\overline{M}$ | $A_8$-$A_{15}$ | $AD_0$-$AD_7$ | $\overline{RD},\overline{WR}$ | $\overline{INTA}$ | ALE |
| $T_1$ | X | X | X | X | 1 | 1 | 1* |
| $T_2$ | X | X | X | X | X | X | 0 |
| $T_{WAIT}$ | X | X | X | X | X | X | 0 |
| $T_3$ | X | X | X | X | X | X | 0 |
| $T_4$ | 1 | 0' | X | TS | 1 | 1 | 0 |
| $T_5$ | 1 | 0' | X | TS | 1 | 1 | 0 |
| $T_6$ | 1 | 0' | X | TS | 1 | 1 | 0 |
| $T_{RESET}$ | X | TS | TS | TS | TS | 1 | 0 |
| $T_{HALT}$ | 0 | TS | TS | TS | TS | 1 | 0 |
| $T_{HOLD}$ | X | TS | TS | TS | TS | 1 | 0 |

0 = Logic "0"    TS = High Impedance
1 = Logic "1"    X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction
† $IO/\overline{M}$ = 1 during $T_4$-$T_6$ of INA machine cycle
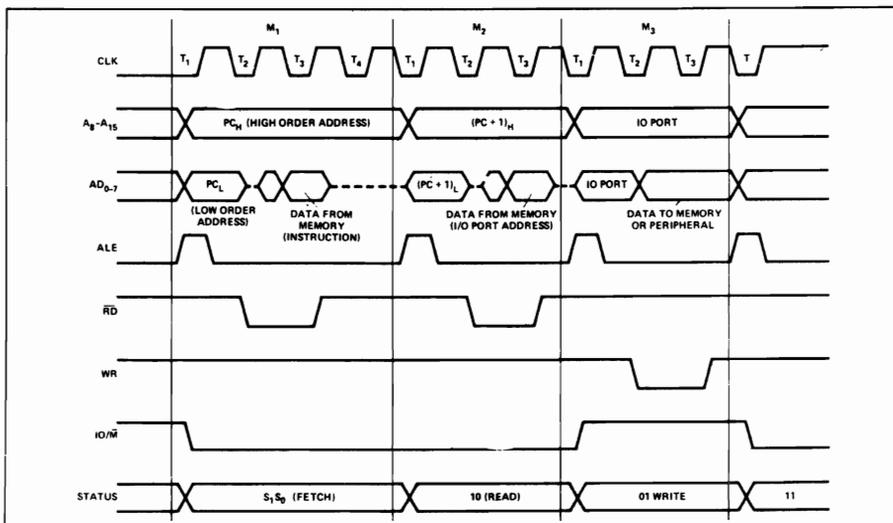


Figure 10. 8085AH Basic System Timing

## Table 6. Instruction Set Summary

| Mnemonic | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operations Description |
|---|---|---|---|---|---|---|---|---|---|
| **MOVE, LOAD, AND STORE** | | | | | | | | | |
| MOVr1 r2 | 0 | 1 | D | D | D | S | S | S | Move register to register |
| MOV M,r | 0 | 1 | 1 | 1 | 0 | S | S | S | Move register to memory |
| MOV r,M | 0 | 1 | D | D | D | 1 | 1 | 0 | Move memory to register |
| MVI r | 0 | 0 | D | D | D | 1 | 1 | 0 | Move immediate register |
| MVI M | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | Move immediate memory |
| LXI B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Load immediate register Pair B & C |
| LXI D | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | Load immediate register Pair D & E |
| LXI H | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Load immediate register Pair H & L |
| STAX B | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Store A indirect |
| STAX D | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Store A indirect |
| LDAX B | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | Load A indirect |
| LDAX D | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | Load A indirect |
| STA | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | Store A direct |
| LDA | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | Load A direct |
| SHLD | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | Store H & L direct |
| LHLD | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Load H & L direct |
| XCHG | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | Exchange D & E, H & L Registers |
| **STACK OPS** | | | | | | | | | |
| PUSH B | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Push register Pair B & C on stack |
| PUSH D | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | Push register Pair D & E on stack |
| PUSH H | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | Push register Pair H & L on stack |
| PUSH PSW | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | Push A and Flags on stack |
| POP B | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | Pop register Pair B & C off stack |
| POP D | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | Pop register Pair D & E off stack |
| POP H | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | Pop register Pair H & L off stack |
| POP PSW | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | Pop A and Flags off stack |
| XTHL | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Exchange top of stack, H & L |
| SPHL | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | H & L to stack pointer |
| LXI SP | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | Load immediate stack pointer |
| INX SP | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | Increment stack pointer |
| DCX SP | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | Decrement stack pointer |
| **JUMP** | | | | | | | | | |
| JMP | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | Jump unconditional |
| JC | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Jump on carry |
| JNC | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | Jump on no carry |
| JZ | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | Jump on zero |
| JNZ | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | Jump on no zero |
| JP | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | Jump on positive |
| JM | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | Jump on minus |
| JPE | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | Jump on parity even |
| JPO | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Jump on parity odd |
| PCHL | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | H & L to program counter |
| **CALL** | | | | | | | | | |
| CALL | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | Call unconditional |
| CC | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Call on carry |
| CNC | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | Call on no carry |

| Mnemonic | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Operations Description |
|---|---|---|---|---|---|---|---|---|---|
| CZ | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | Call on zero |
| CNZ | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Call on no zero |
| CP | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | Call on positive |
| CM | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Call on minus |
| CPE | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | Call on parity even |
| CPO | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | Call on parity odd |
| **RETURN** | | | | | | | | | |
| RET | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | Return |
| RC | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | Return on carry |
| RNC | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | Return on no carry |
| RZ | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Return on zero |
| RNZ | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Return on no zero |
| RP | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Return on positive |
| RM | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Return on minus |
| RPE | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | Return on parity even |
| RPO | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Return on parity odd |
| **RESTART** | | | | | | | | | |
| RST | 1 | 1 | A | A | A | 1 | 1 | 1 | Restart |
| **INPUT/OUTPUT** | | | | | | | | | |
| IN | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | Input |
| OUT | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | Output |
| **INCREMENT AND DECREMENT** | | | | | | | | | |
| INR r | 0 | 0 | D | D | D | 1 | 0 | 0 | Increment register |
| DCR r | 0 | 0 | D | D | D | 1 | 0 | 1 | Decrement register |
| INR M | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Increment memory |
| DCR M | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Decrement memory |
| INX B | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Increment B & C registers |
| INX D | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | Increment D & E registers |
| INX H | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Increment H & L registers |
| DCX B | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | Decrement B & C |
| DCX D | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | Decrement D & E |
| DCX H | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Decrement H & L |
| **ADD** | | | | | | | | | |
| ADD r | 1 | 0 | 0 | 0 | 0 | S | S | S | Add register to A |
| ADC r | 1 | 0 | 0 | 0 | 1 | S | S | S | Add register to A with carry |
| ADD M | 1 | 0 | C | 0 | 0 | 1 | 1 | 0 | Add memory to A |
| ADC M | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | Add memory to A with carry |
| ADI | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | Add immediate to A |
| ACI | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | Add immediate to A with carry |
| DAD B | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | Add B & C to H & L |
| DAD D | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | Add D & E to H & L |
| DAD H | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | Add H & L to H & L |
| DAD SP | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Add stack pointer to H & L |
| **SUBTRACT** | | | | | | | | | |
| SUB r | 1 | 0 | 0 | 1 | 0 | S | S | S | Subtract register from A |
| SBB r | 1 | 0 | 0 | 1 | 1 | S | S | S | Subtract register from A with borrow |
| SUB M | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | Subtract memory from A |
| SBB M | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | Subtract memory from A with borrow |
| SUI | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | Subtract immediate from A |
| SBI | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | Subtract immediate from A with borrow |

## Table 6. Instruction Set Summary (Continued)

| Mnemonic | Instruction Code D₇ D₆ D₅ D₄ D₃ D₂ D₁ D₀ | | | | | | | | Operations Description |
|---|---|---|---|---|---|---|---|---|---|
| LOGICAL | | | | | | | | | |
| ANA r | 1 | 0 | 1 | 0 | 0 | S | S | S | And register with A |
| XRA r | 1 | 0 | 1 | 0 | 1 | S | S | S | Exclusive OR register with A |
| ORA r | 1 | 0 | 1 | 1 | 0 | S | S | S | OR register with A |
| CMP r | 1 | 0 | 1 | 1 | 1 | S | S | S | Compare register with A |
| ANA M | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | And memory with A |
| XRA M | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Exclusive OR memory with A |
| ORA M | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | OR memory with A |
| CMP M | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | Compare memory with A |
| ANI | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | And immediate with A |
| XRI | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Exclusive OR immediate with A |
| ORI | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | OR immediate with A |
| CPI | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | Compare immediate with A |
| ROTATE | | | | | | | | | |
| RLC | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | Rotate A left |
| RRC | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | Rotate A right |
| RAL | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | Rotate A left through carry |
| RAR | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | Rotate A right through carry |

| Mnemonic | Instruction Code D₇ D₆ D₅ D₄ D₃ D₂ D₁ D₀ | | | | | | | | Operations Description |
|---|---|---|---|---|---|---|---|---|---|
| SPECIALS | | | | | | | | | |
| CMA | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | Complement A |
| STC | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Set carry |
| CMC | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | Complement carry |
| DAA | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | Decimal adjust A |
| CONTROL | | | | | | | | | |
| EI | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | Enable Interrupts |
| DI | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | Disable Interrupt |
| NOP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No-operation |
| HLT | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | Halt |
| NEW 8085A INSTRUCTIONS | | | | | | | | | |
| RIM | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Read Interrupt Mask |
| SIM | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Set Interrupt Mask |

**NOTES:**
1. DDS or SSS: B 000, C 001, D 010, E011, H.100, L 101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

*All mnemonics copyrighted ©Intel Corporation 1976.

# Unspecified 8085A Op Codes

NEW CONDITION CODES    V = bit 1
                       X5 = bit 5

| Condition code format | | | | | | | |
|---|---|---|---|---|---|---|---|
| S | Z | X5 | AC | 0 | P | V | C |

2's complement overflow
Underflow (DCX) or overflow (INX)
$X5 = O1 \cdot O2 + O1 \cdot R + O2 \cdot R$, where
$O1$ = sign of operand 1, $O2$ = sign of operand 2,
$R$ = sign of result. For subtraction and comparisons,
replace $O2$ with $\overline{O2}$.

**DSUB**    (double subtraction)

(H) (L) = (H) (L) − (B) (C)
The contents of register pair B and C are subtracted from the
contents of register pair H and L. The result is placed in
register pair H and L. All condition flags are affected.

| 0 0 0 0 1 0 0 0 | (08) |
|---|---|

cycles       3
states      10
addressing  register
flags.      Z, S, P, CY, AC, X5, V

**ARHL**    (arithmetic shift of H and L to the right)

(H7=H7), (Hn−1) = (Hn)
(L7=Ho), (Ln−1) = (Ln), (CY) = (Lo)

The contents of register pair H and L are shifted right one bit.
The uppermost bit is duplicated and the lowest bit is shifted
into the carry bit. The result is placed in register pair H and L.
Note: only the CY flag is affected.

| 0 0 0 1 0 0 0 0 | (10) |
|---|---|

cycles       2
states:      7
addressing   register
flags        CY

**RDEL**    (rotate D and E left through carry)

(Dn+1) = (Dn); (Do) = (E7)
(CY) = (D7), (En+1) = (En), (Eo) = (CY)

The contents of register pair D and E are rotated left one
position through the carry flag. The low-order bit is set equal
to the CY flag and the CY flag is set to the value shifted out
of the high-order bit. Only the CY and the V flags are affected.

| 0 0 0 1 1 0 0 0 | (18) |
|---|---|

cycles       3
states      10
addressing  register
flags       CY, V

**LDHI**    (load D and E with H and L plus immediate byte)

(D) (E) = (H) (L) + (byte 2)

The contents of register pair H and L are added to the
immediate byte. The result is placed in register pair D and E.
Note: no condition flags are affected.

| 0 0 1 0 1 0 0 0 | (28) |
| data | |
|---|---|

cycles       3
states:     10
addressing. immediate register
flags:      none

**LDSI**    (load D and E with SP plus immediate byte)

(D) (E) = (SPH)(SPL) + (byte 2)

The contents of register pair SP are added to the immediate
byte. The result is placed in register pair D and E. Note: no
condition flags are affected.

| 0 0 1 1 1 0 0 0 | (38) |
| data | |
|---|---|

cycles       3
states:     10
addressing  immediate register
flags.      none

**RSTV**    (restart on overflow)

If (V)
((SP)−1) = (PCH)
((SP)−2) = (PCL)
(SP) = (SP)−2
(PC) = 40 hex

If the overflow flag V is set, the actions specified above are
performed; otherwise control continues sequentially.

| 1 1 0 0 1 0 1 1 | (C8) |
|---|---|

cycles       1 or 3
states       6 or 12
addressing   register indirect
flags        none

**SHLX**    (store H and L indirect through D and E)

((D)(E)) = (L)
((D)(E)+1) = (H)

The contents of register L are moved to the memory location
whose address is in register pair D and E. The contents of
register H are moved to the succeeding memory location.

| 1 1 0 1 1 0 0 1 | (D9) |
|---|---|

cycles       3
states      10
addressing   register indirect
flags        none

**JNX5**    (jump on not X5)

If (not X5)
(PC) = (byte 3) (byte 2)

If the X5 flag is reset, control is transferred to the instruction
whose address is specified in byte 3 and byte 2 of the current
instruction, otherwise control continues sequentially.

| 1 1 0 1 1 1 0 1 | (DD) |
| low-order address | |
| high-order address | |
|---|---|

cycles:      2 or 3
states.      7 or 10
addressing   immediate
flags        none

**LHLX**    (load H and L indirect through D and E)

(L) = ((D)(E))
(H) = ((D)(E)+1)

The content of the memory location whose address is in D
and E, are moved to register L. The contents of the succeeding
memory location are moved to register H.

| 1 1 1 0 1 1 0 1 | (ED) |
|---|---|

cycles.      3
states.     10
addressing.  register indirect
flags:       none

**JX5**    (jump on X5)

If (X5)
(PC) = (byte 3) (byte 2)

If the X5 flag is set, control is transferred to the instruction
whose address is specified in byte 3 and byte 2 of the current
instruction, otherwise control continues sequentially.

| 1 1 1 1 1 1 0 1 | (FD) |
| low-order address | |
| high-order address | |
|---|---|

cycles:      2 or 3
states:      7 or 10
addressing:  immediate
flags:       none

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## WAVEFORMS

### CLOCK



### READ



### WRITE



### HOLD
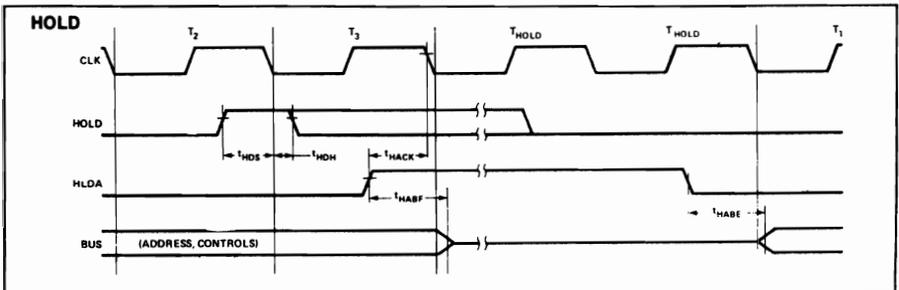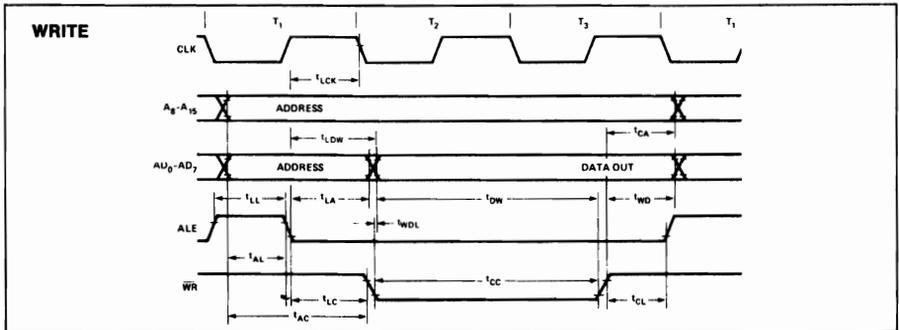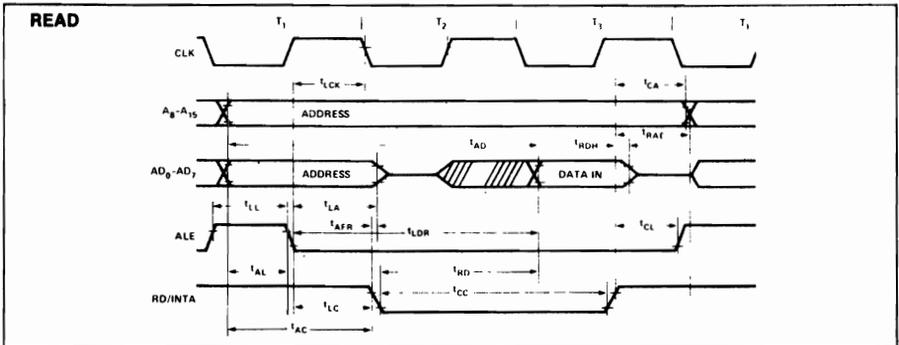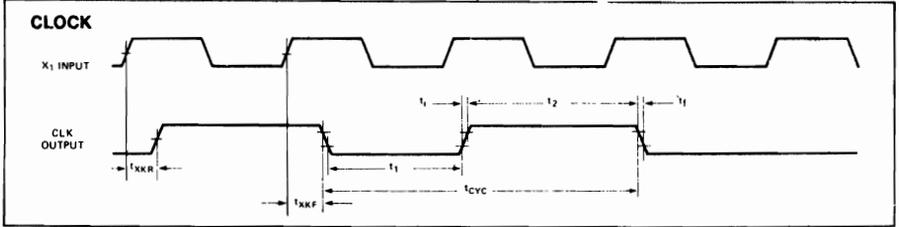
# 8155H/8156H/8155H-2/8156H-2
# 2048-BIT STATIC HMOS RAM
# WITH I/O PORTS AND TIMER

- **Single +5V Power Supply with 10% Voltage Margins**
- **30% Lower Power Consumption than the 8155 and 8156**
- **100% Compatible with 8155 and 8156**
- **256 Word x 8 Bits**
- **Completely Static Operation**
- **Internal Address Latch**
- **2 Programmable 8-Bit I/O Ports**

- **1 Programmable 6-Bit I/O Port**
- **Programmable 14-Bit Binary Counter/ Timer**
- **Compatible with 8085AH, 8085A and 8088 CPU**
- **Multiplexed Address and Data Bus**
- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**

The Intel® 8155H and 8156H are RAM and I/O chips implemented in N-Channel, depletion load, silicon gate technology (HMOS), to be used in the 8085AH and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085AH CPU. The 8155H-2 and 8156H-2 have maximum access times of 330 ns for use with the 8085AH-2 and the 5 MHz 8088 CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.



*8155H/8155H-2 = CE, 8156H/8156H-2 = CE

**Figure 1. Block Diagram**

**Figure 2. Pin Configuration**

## Table 1. Pin Description

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| RESET | I | **Reset:** Pulse provided by the 8085AH to initialize the system (connect to 8085AH RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should be typically be two 8085AH clock cycle times. |
| $AD_{0-7}$ | I/O | **Address/Data:** 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155H/56H on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the $IO/\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal. |
| CE or $\overline{CE}$ | I | **Chip Enable:** On the 8155H, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156H, this pin is CE and is ACTIVE HIGH. |
| $\overline{RD}$ | I | **Read Control:** Input low on this line with the Chip Enable active enables and $AD_{0-7}$ buffers. If $IO/\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus |
| $\overline{WR}$ | I | **Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on $IO/\overline{M}$. |
| ALE | I | **Address Latch Enable:** This control signal latches both the address on the $AD_{0-7}$ lines and the state of the Chip Enable and $IO/\overline{M}$ into the chip at the falling edge of ALE. |
| $IO/\overline{M}$ | I | **I/O Memory:** Selects memory if low and I/O and command/status registers if high. |
| $PA_{0-7}(8)$ | I/O | **Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register. |
| $PB_{0-7}(8)$ | I/O | **Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register. |
| $PC_{0-5}(6)$ | I/O | **Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When $PC_{0-5}$ are used as control signals, they will provide the following:<br>$PC_0$ — A INTR (Port A Interrupt)<br>$PC_1$ — ABF (Port A Buffer Full)<br>$PC_2$ — $\overline{A\ STB}$ (Port A Strobe)<br>$PC_3$ — B INTR (Port B Interrupt)<br>$PC_4$ — B BF (Port B Buffer Full)<br>$PC_5$ — $\overline{B\ STB}$ (Port B Strobe) |
| TIMER IN | I | **Timer Input:** Input to the counter-timer. |
| $\overline{TIMER\ OUT}$ | O | **Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode. |
| $V_{CC}$ | | **Voltage:** +5 volt supply. |
| $V_{SS}$ | | **Ground:** Ground reference. |

## FUNCTIONAL DESCRIPTION

The 8155H/8156H contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The $IO/\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, $PA_{0-7}$, $PB_{0-7}$, $PC_{0-5}$) or the memory (RAM) portion.

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and $IO/\overline{M}$ are all latched on-chip at the falling edge of ALE.
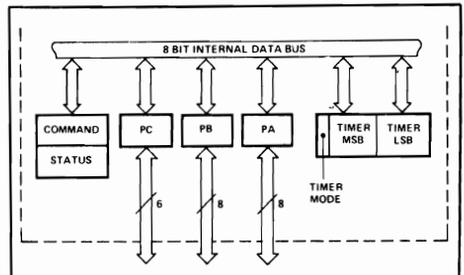


**Figure 3. 8155H/8156H Internal Registers**

NOTE: FOR DETAILED TIMING INFORMATION, SEE FIGURE 12 AND A.C. CHARACTERISTICS.
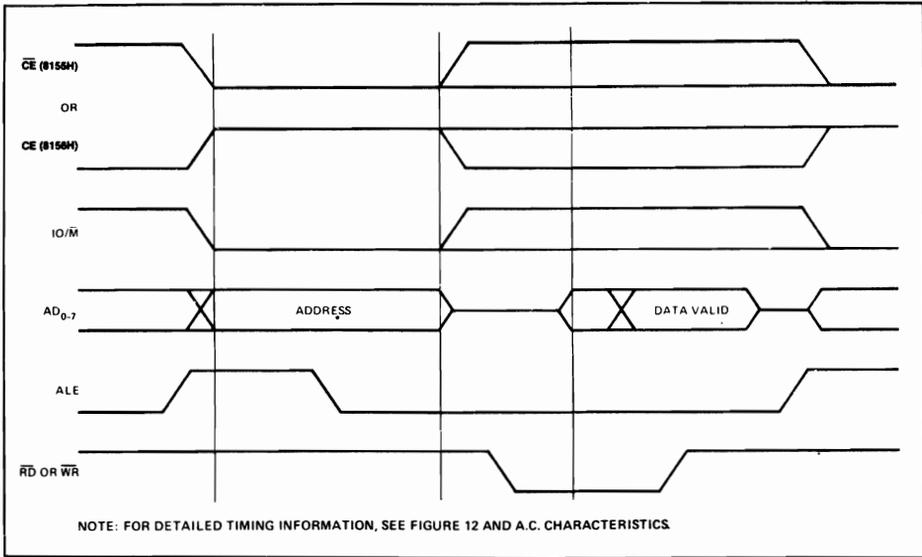
**Figure 4. 8155H/8156H On-Board Memory Read/Write Cycle**

## PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 5. The contents of the command register may never be read.

## READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit: six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 6. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.
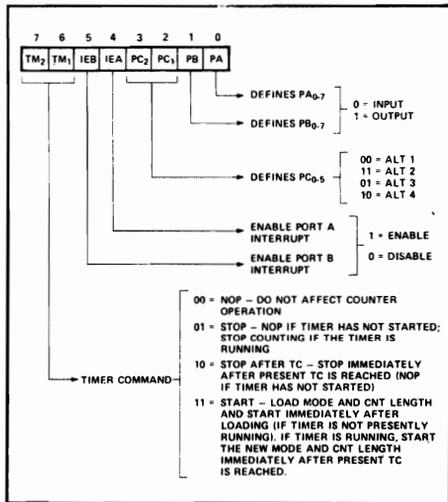


**Figure 5. Command Register Bit Assignment**

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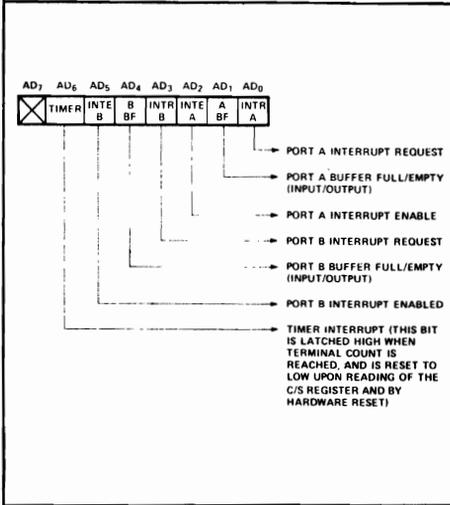
**Figure 6. Status Register Bit Assignment**

interrupt that the 8155H sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 2.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

| CONTROL | INPUT MODE | OUTPUT MODE |
|---------|-----------|-------------|
| BF | Low | Low |
| INTR | Low | High |
| STB | Input Control | Input Control |



| I/O ADDRESS† | | | | | | | | SELECTION |
|---|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| X | X | X | X | X | 0 | 0 | 0 | Internal Command/Status Register |
| X | X | X | X | X | 0 | 0 | 1 | General Purpose I O Port A |
| X | X | X | X | X | 0 | : | 0 | General Purpose I O Port B |
| X | X | X | X | X | 0 | 1 | 1 | Port C — General Purpose I O or Control |
| X | X | X | X | X | 1 | 0 | 0 | Low-Order 8 bits of Timer Count |
| X | X | X | X | X | 1 | 0 | 1 | High 6 bits of Timer Count and 2 bits of Timer Mode |
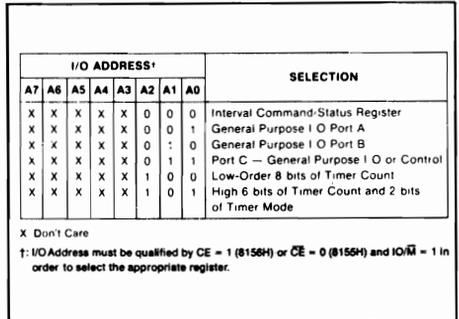
X  Don't Care

† I/OAddress must be qualified by CE = 1 (8156H) or C̄Ē = 0 (8155H) and IO/M̄ = 1 in order to select the appropriate register.

**Figure 7. I/O Port and Timer Addressing Scheme**

## INPUT/OUTPUT SECTION

The I/O section of the 8155H/8156H consists of five regis-ters: (See Figure 7.)

- **Command/Status Register (C/S)** — Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD$_{0-7}$ lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA$_{0-7}$. The address of this register is XXXXX001.

- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB$_{0-7}$. The address of this register is XXXXX010.

- **PC Register** — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be program-med to be either input ports, output ports or as control signals for PA and PB by properly programming the AD$_2$ and AD$_3$ bits of the C/S register.

  When PC$_{0-5}$ is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an

Figure 8 shows how I/O PORTS A and B are structured within the 8155H and 8156H:
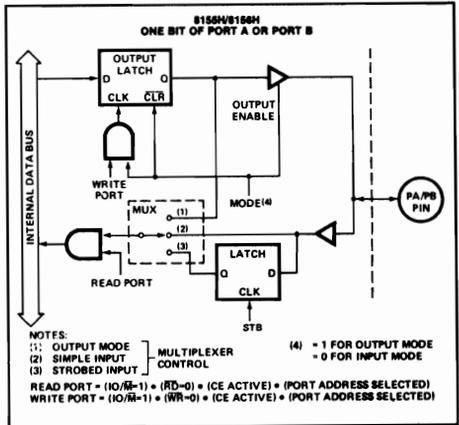


**Figure 8. 8155H/8156H Port Functions**

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**Table 2. Port Control Assignment**

| Pin | ALT 1 | ALT 2 | ALT 3 | ALT 4 |
|-----|-------|-------|-------|-------|
| PC0 | Input Port | Output Port | A INTR (Port A Interrupt) | A INTR (Port A Interrupt) |
| PC1 | Input Port | Output Port | A BF (Port A Buffer Full) | A BF (Port A Buffer Full) |
| PC2 | Input Port | Output Port | A $\overline{STB}$ (Port A Strobe) | A $\overline{STB}$ (Port A Strobe) |
| PC3 | Input Port | Output Port | Output Port | B INTR (Port B Interrupt) |
| PC4 | Input Port | Output Port | Output Port | B BF (Port B Buffer Full) |
| PC5 | Input Port | Output Port | Output Port | B $\overline{STB}$ (Port B Strobe) |

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the 8155H/8156H are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the 8155H/56H is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 9 shows how the 8155H/8156H I/O ports might be configured in a typical MCS-85 system.

## TIMER SECTION

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 7.)

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 10). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0–13.
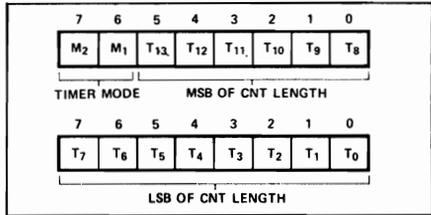


**Figure 10. Timer Format**

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 11.



**Figure 9. Example: Command Register = 00111001**
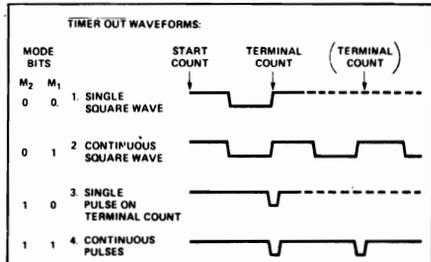


**Figure 11. Timer Modes**

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Bits 6-7 (TM2 and TM1) of command register contents are used to start and stop the counter. There are four commands to choose from:

| TM2 | TM1 | |
|-----|-----|---|
| 0 | 0 | NOP — Do not affect counter operation. |
| 0 | 1 | STOP — NOP if timer has not started; stop counting if the timer is running. |
| 1 | 0 | STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started) |
| 1 | 1 | START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached. |

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 12.



NOTE 5 AND 4 REFER TO THE NUMBER OF CLOCKS IN THAT TIME PERIOD
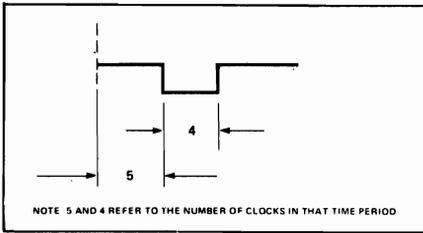
**Figure 12. Asymmetrical Square-Wave Output Resulting from Count of 9**

The counter in the 8155H is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the 8155H/8156H chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085AH be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count

2. Read in the 16-bit value from the count length registers

3. Reset the upper two mode bits

4. Reset the carry and rotate right one position all 16 bits through carry

5. If carry is set, add 1/2 of the full original count (1/2 full count — 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the 8155H/56H always counts out the right number of pulses in generating the TIMER OUT waveforms.

## 8085A MINIMUM SYSTEM CONFIGURATION

Figure 13a shows a minimum system using three chips, containing:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels
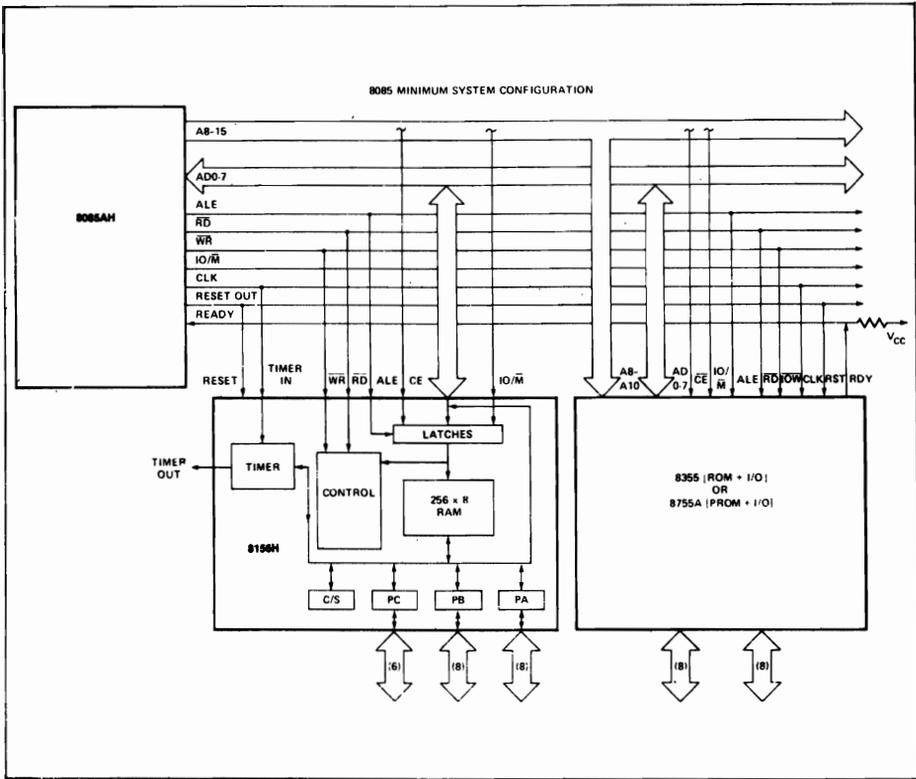


**Figure 13a. 8085AH Minimum System Configuration (Memory Mapped I/O)**

## 8088 FIVE CHIP SYSTEM

Figure 13b shows a five chip system containing:

- 1.25K Bytes RAM
- 2K Bytes ROM

- 38 I/O Pins
- 1 Interval Timer
- 2 Interrupt Levels
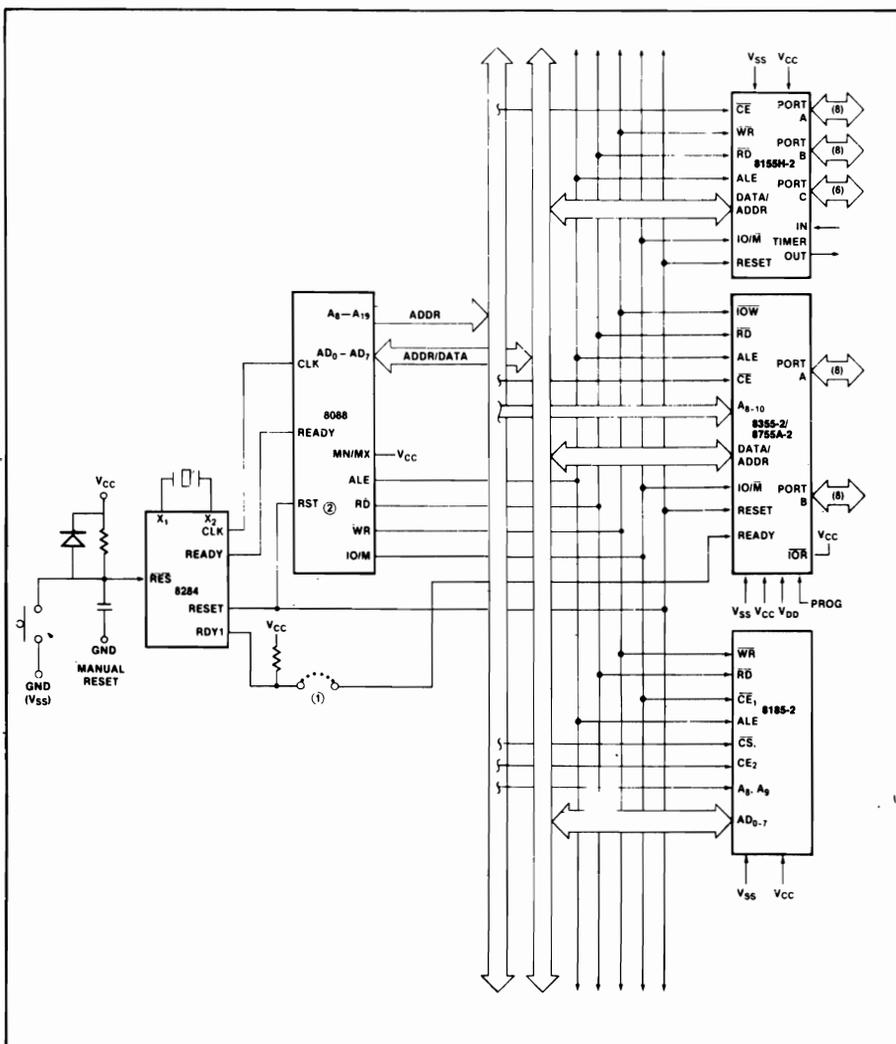


**Figure 13b. 8088 Five Chip System Configuration**

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# 8185/8185-2
# 1024 x 8-BIT STATIC RAM FOR MCS-85®

■ Multiplexed Address and Data Bus

■ Directly Compatible with 8085A and iAPX 88 Microprocessors

■ Low Operating Power Dissipation

■ Low Standby Power Dissipation

■ Single +5V Supply

■ High Density 18-Pin Package

The Intel® 8185 is an 8192-bit static random access memory (RAM) organized as 1024 words by 8-bits using N-channel Silicon-Gate MOS technology. The multiplexed address and data bus allows the 8185 to interface directly to the 8085A and iAPX 88 microprocessors to provide a maximum level of system integration.

The low standby power dissipation minimizes system power requirements when the 8185 is disabled.

The 8185-2 is a high-speed selected version of the 8185 that is compatible with the 5 MHz 8085A-2 and the 5 MHz iAPX 88.
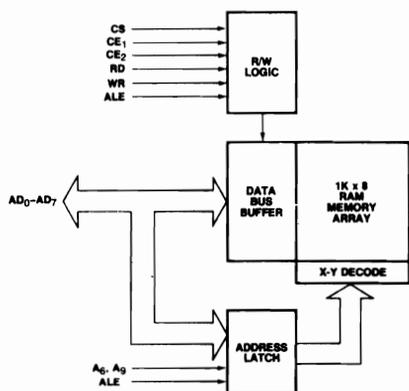


Figure 1. Block Diagram
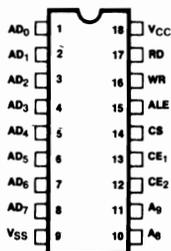


| AD₀-AD₇ | ADDRESS/DATA LINES |
| A₈, A₉ | ADDRESS LINES |
| CS | CHIP SELECT |
| CE₁ | CHIP ENABLE (IO/M) |
| CE₂ | CHIP ENABLE |
| ALE | ADDRESS LATCH ENABLE |
| WR | WRITE ENABLE |

Figure 2. Pin Configuration

## FUNCTIONAL DESCRIPTION

The 8185 has been designed to provide for direct interface to the multiplexed bus structure and bus timing of the 8085A microprocessor.

At the beginning of an 8185 memory access cycle, the 8-bit address on $AD_{0-7}$, $A_8$ and $A_9$, and the status of $\overline{CE_1}$ and $CE_2$ are all latched internally in the 8185 by the falling edge of ALE. If the latched status of both $\overline{CE_1}$ and $CE_2$ are active, the 8185 powers itself up, but no action occurs until the $\overline{CS}$ line goes low and the appropriate $\overline{RD}$ or $\overline{WR}$ control signal input is activated.

The $\overline{CS}$ input is not latched by the 8185 in order to allow the maximum amount of time for address decoding in selecting the 8185 chip. Maximum power consumption savings will occur, however, only when $\overline{CE_1}$ and $CE_2$ are activated selectively to power down the 8185 when it is not in use. A possible connection would be to wire the 8085A's $IO/\overline{M}$ line to the 8185's $\overline{CE_1}$ input, thereby keeping the 8185 powered down during I/O and interrupt cycles.

### Table 1.
### Truth Table for
### Power Down and Function Enable

| $\overline{CE_1}$ | $CE_2$ | $\overline{CS}$ | $(CS^*)^{[2]}$ | 8185 Status |
|---|---|---|---|---|
| 1 | X | X | 0 | Power Down and Function Disable[1] |
| X | 0 | X | 0 | Power Down and Function Disable[1] |
| 0 | 1 | 1 | 0 | Powered Up and Function Disable[1] |
| 0 | 1 | 0 | 1 | Powered Up and Enabled |

NOTES:
X: Don't Care.
1: Function Disable implies Data Bus in high impedance state and not writing.
2: $CS^* = (\overline{CE_1} = 0) \cdot (CE_2 = 1) \cdot \overline{CS} = 0)$
   $CS^* = 1$ signifies all chip enables and chip select active

### Table 2.
### Truth Table for
### Control and Data Bus Pin Status

| $(CS^*)$ | $\overline{RD}$ | $\overline{WR}$ | $AD_{0-7}$ During Data Portion of Cycle | 8185 Function |
|---|---|---|---|---|
| 0 | X | X | Hi-Impedance | No Function |
| 1 | 0 | 1 | Data from Memory | Read |
| 1 | 1 | 0 | Data to Memory | Write |
| 1 | 1 | 1 | Hi-Impedance | Reading, but not Driving Data Bus |

NOTE:
X: Don't Care.
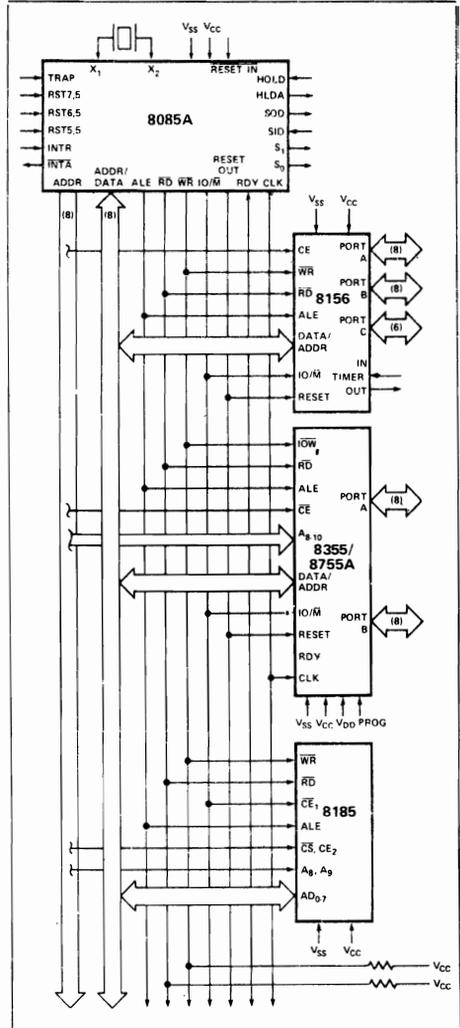


**Figure 3. 8185 in an MCS-85 System**

4 Chips:
2K Bytes ROM
1.25K Bytes RAM
38 I/O Lines
1 Counter/Timer
2 Serial I/O Lines
5 Interrupt Inputs

# 8202A
# DYNAMIC RAM CONTROLLER

- **Provides All Signals Necessary to Control 2117, or 2118 Dynamic Memories**

- **Directly Addresses and Drives Up to 64K Bytes Without External Drivers**

- **Provides Address Multiplexing and Strobes**

- **Provides a Refresh Timer and a Refresh Counter**

- **Refresh Cycles May be Internally or Externally Requested**

- **Provides Transparent Refresh Capability**

- **Fully Compatible with Intel® 8080A, 8085A, iAPX 88, and iAPX 86 Family Microprocessors**

- **Decodes CPU Status for Advanced Read Capability with the 8202A-1 or 8202A-3**

- **Provides System Acknowledge and Transfer Acknowledge Signals**

- **Internal Clock Capability with the 8202A-1 or 8202A-3**

The Intel® 8202A is a Dynamic Ram System Controller designed to provide all signals necessary to use 2117 or 2118 Dynamic RAMs in microcomputer systems. The 8202A provides multiplexed addresses and address strobes, as well as refresh/access arbitration. The 8202A-1 or 8202A-3 support an internal crystal oscillator.



| Figure 1. 8202A Block Diagram | Figure 2. Pin Configuration |
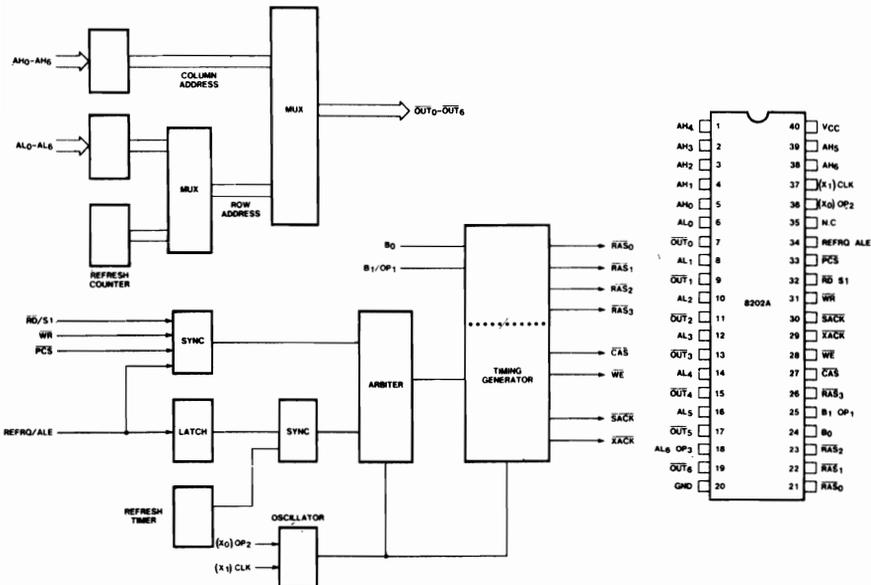
# 8203
# 64K DYNAMIC RAM CONTROLLER

- **Provides All Signals Necessary to Control 64K and 16K Dynamic Memories**

- **Directly Addresses and Drives Up to 64 Devices Without External Drivers**

- **Provides Address Multiplexing and Strobes**

- **Provides a Refresh Timer and a Refresh Counter**

- **Provides Refresh/Access Arbitration**

- **Internal Clock Capability with the 8203-1 and the 8203-3**

- **Fully Compatible with Intel® 8080A, 8085A, iAPX88, and iAPX 86 Family Microprocessors**

- **Decodes CPU Status for Advanced Read Capability in 16K Mode with the 8203-1 and the 8203-3.**

- **Provides System Acknowledge and Transfer Acknowledge Signals**

- **Refresh Cycles May be Internally or Externally Requested (For Transparent Refresh)**

- **Internal Series Damping Resistors on All RAM Outputs**

The Intel® 8203 is a Dynamic RAM System Controller designed to provide all signals necessary to use 64K or 16K Dynamic RAMs in microcomputer systems. The 8203 provides multiplexed addresses and address strobes, refresh logic, refresh/access arbitration. Refresh cycles can be started internally or externally. The 8203-1 and the 8203-3 support an internal crystal oscillator and Advanced Read Capability. The 8203-3 is a ±5% $V_{CC}$ part.
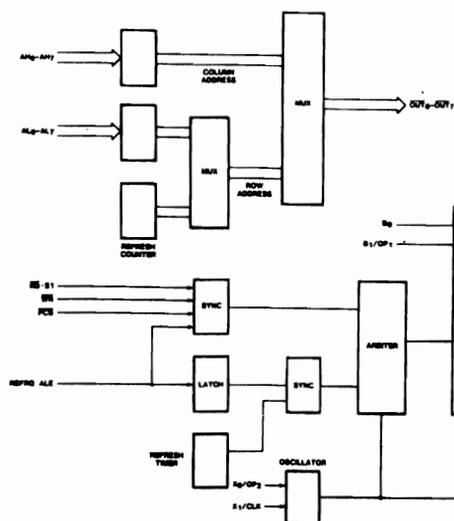


Figure 1. 8203 Block Diagram



**Figure 2.**
**Pin Configuration**

**Table 1. Pin Descriptions**

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| $AL_0$<br>$AL_1$<br>$AL_2$<br>$AL_3$<br>$AL_4$<br>$AL_5$<br>$AL_6$ | 6<br>8<br>10<br>12<br>14<br>16<br>18 | I<br>I<br>I<br>I<br>I<br>I<br>I | **ADDRESS LOW:** CPU address inputs used to generate memory row address. |
| $AH_0$<br>$AH_1$<br>$AH_2$<br>$AH_3$<br>$AH_4$<br>$AH_5$<br>$AH_6$ | 5<br>4<br>3<br>2<br>1<br>39<br>38 | I<br>I<br>I<br>I<br>I<br>I<br>I | **ADDRESS HIGH:** CPU address inputs used to generate memory column address. |
| $B_0/AL_7$<br>$B_1/OP_1/$<br>$AH_7$ | 24<br>25 | I<br>I | **BANK SELECT INPUTS:** Used to gate the appropriate $\overline{RAS}$ output for a memory cycle. $B_1/OP_1$ option used to select the Advanced Read Mode. (Not available in 64K mode.) See Figure 5.<br>When in 64K RAM Mode, pins 24 and 25 operate as the $AL_7$ and $AH_7$ address inputs. |
| $\overline{PCS}$ | 33 | I | **PROTECTED CHIP SELECT:** Used to enable the memory read and write inputs. Once a cycle is started, it will not abort even if $\overline{PCS}$ goes inactive before cycle completion. |
| $\overline{WR}$ | 31 | I | **MEMORY WRITE REQUEST.** |
| $\overline{RD}/S1$ | 32 | I | **MEMORY READ REQUEST:** S1 function used in Advanced Read mode selected by $OP_1$ (pin 25). |
| $\overline{REFRQ}/$<br>ALE | 34 | I | **EXTERNAL REFRESH REQUEST:** ALE function used in Advanced Read mode, selected by $OP_1$ (pin 25). |
| $\overline{OUT}_0$<br>$\overline{OUT}_1$<br>$\overline{OUT}_2$<br>$\overline{OUT}_3$<br>$\overline{OUT}_4$<br>$\overline{OUT}_5$<br>$\overline{OUT}_6$ | 7<br>9<br>11<br>13<br>15<br>17<br>19 | O<br>O<br>O<br>O<br>O<br>O<br>O | **OUTPUT OF THE MULTIPLEXER:** These outputs are designed to drive the addresses of the Dynamic RAM array. (Note that the $\overline{OUT}_{0-7}$ pins do not require inverters or drivers for proper operation.) |
| $\overline{WE}$ | 28 | O | **WRITE ENABLE:** Drives the Write Enable inputs of the Dynamic RAM array. |
| $\overline{CAS}$ | 27 | O | **COLUMN ADDRESS STROBE:** This output is used to latch the Column Address into the Dynamic RAM array. |
| $\overline{RAS}_0$<br>$\overline{RAS}_1$<br>$\overline{RAS}_2/$<br>$\overline{OUT}_7$<br>$\overline{RAS}_3/B_0$ | 21<br>22<br>23<br><br>26 | O<br>O<br>O<br><br>I/O | **ROW ADDRESS STROBE:** Used to latch the Row Address into the bank of dynamic RAM's, selected by the 8203 Bank Select pins ($B_0$, $B_1/OP_1$). In 64K mode, only $\overline{RAS}_0$ and $\overline{RAS}_1$ are available; pin 23 operates as $\overline{OUT}_7$ and pin 26 operates as the $B_0$ bank select input. |
| $\overline{XACK}$ | 29 | O | **TRANSFER ACKNOWLEDGE:** This output is a strobe indicating valid data during a read cycle or data written during a write cycle. $\overline{XACK}$ can be used to latch valid data from the RAM array. |

**Table 1. Pin Descriptions** (Continued)

| Symbol | Pin No. | Type | Name and Function |
|--------|---------|------|-------------------|
| $\overline{SAC}$ | 30 | O | **SYSTEM ACKNOWLEDGE:** This output indicates the beginning of a memory access cycle. It can be used as an advanced transfer acknowledge to eliminate wait states. (Note: If a memory access request is made during a refresh cycle, $\overline{SACK}$ is delayed until $\overline{XACK}$ in the memory access cycle). |
| $X_0/OP_2$ $X_1/CLK$ | 36 37 | I/O I/O | **OSCILLATOR INPUTS:** These inputs are designed for a quartz crystal to control the frequency of the oscillator. If $X_0/OP_2$ is shorted to pin 40 ($V_{CC}$) or if $X_0/OP_2$ is connected to $+12V$ through a 1 K$\Omega$ resistor then $X_1/CLK$ becomes a TTL input for an external clock. (Note: Crystal mode for the 8203-1 and the 8203-3 only). |
| $16K/\overline{64K}$ | 35 | I | **MODE SELECT:** This input selects 16K mode or 64K mode. Pins 23–26 change function based on the mode of operation. |
| $V_{CC}$ | 40 | | **POWER SUPPLY:** $+5V$. |
| GND | 20 | | **GROUND.** |

## FUNCTIONAL DESCRIPTION

The 8203 provides a complete dynamic RAM controller for microprocessor systems as well as expansion memory boards.

The 8203 has two modes, one for 16K dynamic RAMs and one for 64Ks, controlled by pin 35.



$C_S < 10$ pF
Fundamental XTAL

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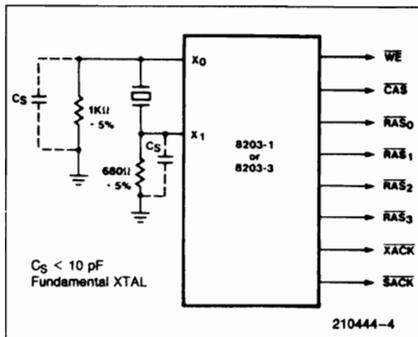
**Figure 3. Crystal Operation for the 8203-1 and 8203-3**

All 8203 timing is generated from a single reference clock. This clock is provided via an external oscillator or an on-chip crystal oscillator. All output signal transitions are synchronous with respect to this clock reference, except for the trailing edges of the CPU handshake signals $\overline{SACK}$ and $\overline{XACK}$.

CPU memory requests normally use the $\overline{RD}$ and $\overline{WR}$ inputs. The Advanced-Read mode allows ALE and S1 to be used in place of the $\overline{RD}$ input.

Failsafe refresh is provided via an internal timer which generates refresh requests. Refresh requests can also be generated via the REFRQ input.

An on-chip synchronizer/arbiter prevents memory and refresh requests from affecting a cycle in progress. The READ, WRITE, and external REFRESH requests may be asynchronous to the 8203 clock; on-chip logic will synchronize the requests, and the arbiter will decide if the requests should be delayed, pending completion of a cycle in progress.

## 16K/64 Option Selection

Pin 35 is a strap input that controls the two 8203 modes. Figure 4 shows the four pins that are multiplexed. In 16K mode (pin 35 tied to $V_{CC}$ or left open), the 8203 has two Bank Select inputs to select one of four $\overline{RAS}$ outputs. In this mode, the 8203 is exactly compatible with the Intel 8202A Dynamic RAM Controller. In 64K mode (pin 35 tied to GND), there is only one Bank Select input (pin 26) to select the two $\overline{RAS}$ outputs. More than two banks of 64K dynamic RAMs can be used with external logic.

## Other Option Selections

The 8203 has two strapping options. When $OP_1$ is selected (16K mode only), pin 32 changes from a $\overline{RD}$ input to an S1 input, and pin 34 changes from a REFRQ input to an ALE input. See "Refresh Cycles" and "Read Cycles" for more detail. $OP_1$ is selected by tying pin 25 to $+12V$ through a 5.1 K$\Omega$ resistor on the 8203-1 or 8203-3 only.

When $OP_2$ is selected, the internal oscillator is disabled and pin 37 changes from a crystal input ($X_1$) to a CLK input for an external TTL clock. $OP_2$ is selected by shorting pin 36 ($X_0/OP_2$) directly to pin 40 ($V_{CC}$). No current limiting resistor should be used. $OP_2$ may also be selected by tying pin 36 to $+12V$ through a 1 K$\Omega$ resistor.

## Refresh Timer

The refresh timer is used to monitor the time since the last refresh cycle occurred. When the appropriate amount of time has elapsed, the refresh timer will request a refresh cycle. External refresh requests will reset the refresh timer.

## Refresh Counter

The refresh counter is used to sequentially refresh all of the memory's rows. The 8-bit counter is incremented after every refresh cycle.

| Pin # | 16K Function | 64K Function |
|-------|--------------|--------------|
| 23 | $\overline{RAS}_2$ | Address Output ($\overline{OUT}_7$) |
| 24 | Bank Select ($B_0$) | Address Input ($AL_7$) |
| 25 | Bank Select ($B_1$) | Address Input ($AH_7$) |
| 26 | $\overline{RAS}_3$ | Bank Select ($B_0$) |

**Figure 4. 16K/64K Mode Selection**

| Inputs | | Outputs | | | |
|--------|--|---------|--|--|--|
| | $B_1$ | $B_0$ | $\overline{RAS}_0$ | $\overline{RAS}_1$ | $\overline{RAS}_2$ | $\overline{RAS}_3$ |

| | $B_1$ | $B_0$ | $\overline{RAS}_0$ | $\overline{RAS}_1$ | $\overline{RAS}_2$ | $\overline{RAS}_3$ |
|--|-------|-------|-----|-----|-----|-----|
| 16K | 0 | 0 | 0 | 1 | 1 | 1 |
| Mode | 0 | 1 | 1 | 0 | 1 | 1 |
| | 1 | 0 | 1 | 1 | 0 | 1 |
| | 1 | 1 | 1 | 1 | 1 | 0 |
| 64K | — | 0 | 0 | 1 | — | — |
| Mode | — | 1 | 1 | 0 | — | — |

**Figure 5. Bank Selection**

## Address Multiplexer

The address multiplexer takes the address inputs and the refresh counter outputs, and gates them onto the address outputs at the appropriate time. The address outputs, in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ outputs, determine the address used by the dynamic RAMs for read, write, and refresh cycles. During the first part of a read or write cycle, $AL_0$–$AL_7$ are gated to $\overline{OUT}_0$–$\overline{OUT}_7$, then $AH_0$–$AH_7$ are gated to the address outputs.

During a refresh cycle, the refresh counter is gated onto the address outputs. All refresh cycles are $\overline{RAS}$-only refresh ($\overline{CAS}$ inactive, $\overline{RAS}$ active).

To minimize buffer delay, the information on the address outputs is inverted from that on the address inputs.

$\overline{OUT}_0$–$\overline{OUT}_7$ do not need inverters or buffers unless additional drive is required.

## Synchronizer/Arbiter

The 8203 has three inputs, REFRQ/ALE (pin 34), $\overline{RD}$ (pin 32) and $\overline{WR}$ (pin 31). The $\overline{RD}$ and $\overline{WR}$ inputs allow an external CPU to request a memory read or write cycle, respectively. The REFRQ/ALE input allows refresh requests to be requested external to the 8203.

All three of these inputs may be asynchronous with respect to the 8203's clock. The arbiter will resolve conflicts between refresh and memory requests, for both pending cycles and cycles in progress. Read and write requests will be given priority over refresh requests.

## System Operation

The 8203 is always in one of the following states:
a) IDLE
b) TEST Cycle
c) REFRESH Cycle
d) READ Cycle
e) WRITE Cycle

The 8203 is normally in the IDLE state. Whenever one of the other cycles is requested, the 8203 will

| Description | Pin # | Normal Function | Option Function |
|-------------|-------|-----------------|-----------------|
| $B_1/OP_1$ (16K only)/$AH_7$ | 25 | Bank ($\overline{RAS}$) Select | Advanced-Read Mode (8203-1, -3) |
| $X_0/OP_2$ | 36 | Crystal Oscillator (8203-1 and 8203-3) | External Oscillator |

**Figure 6. 8203 Option Selection**

leave the IDLE state to perform the desired cycle. If no other cycles are pending, the 8203 will return to the IDLE state.

## Test Cycle

The TEST Cycle is used to check operation of several 8203 internal functions. TEST cycles are requested by activating the $\overline{PCS}$, $\overline{RD}$ and $\overline{WR}$ inputs. The TEST Cycle will reset the refresh address counter and perform a WRITE Cycle. The TEST Cycle should not be used in normal system operation, since it would affect the dynamic RAM refresh.

## Refresh Cycles

The 8203 has two ways of providing dynamic RAM refresh:

1) Internal (failsafe) refresh
2) External (hidden) refresh

Both types of 8203 refresh cycles activate all of the $\overline{RAS}$ outputs, while $\overline{CAS}$, $\overline{WE}$, $\overline{SACK}$, and $\overline{XACK}$ remain inactive.

Internal refresh is generated by the on-chip refresh timer. The timer uses the 8203 clock to ensure that refresh of all rows of the dynamic RAM occurs every 2 milliseconds (128 cycles) or every 4 milliseconds (256 cycles). If REFRQ is inactive, the refresh timer will request a refresh cycle every 10–16 microseconds.

External refresh is requested via the REFRQ input (pin 34). External refresh control is not available when the Advanced-Read mode is selected. External refresh requests are latched, then synchronized to the 8203 clock.

The arbiter will allow the refresh request to start a refresh cycle only if the 8203 is not in the middle of a cycle.

When the 8203 is in the idle state a simultaneous memory request and external refresh request will result in the memory request being honored first. This 8203 characteristic can be used to "hide" refresh cycles during system operation. A circuit similar to Figure 7 can be used to decode the CPU's instruction fetch status to generate an external refresh request. The refresh request is latched while the 8203 performs the instruction fetch; the refresh cycle will start immediately after the memory cycle is completed, even if the $\overline{RD}$ input has not gone inactive. If the CPU's instruction decode time is long enough, the 8203 can complete the refresh cycle before the next memory request is generated.

If the 8203 is not in the idle state then a simultaneous memory request and an external refresh request may result in the refresh request being honored first.



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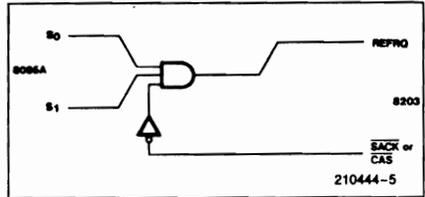
**Figure 7. Hidden Refresh**

Certain system configurations require complete external refresh requests. If external refresh is requested faster than the minimum internal refresh timer ($t_{REF}$), then, in effect, all refresh cycles will be caused by the external refresh request, and the internal refresh timer will never generate a refresh request.

## Read Cycles

The 8203 can accept two different types of memory Read requests:

1) Normal Read, via the $\overline{RD}$ input
2) Advanced Read, using the S1 and ALE inputs (16K mode only)

The user can select the desired Read request configuration via the $B_1/OP_1$ hardware strapping option on pin 25.

| | Normal Read | Advanced Read |
|---|---|---|
| Pin 25 | $B_1$ Input | $OP_1$ (+12V) |
| Pin 32 | RD Input | S1 Input |
| Pin 34 | REFRQ Input | ALE Input |
| # RAM Banks | 4 ($\overline{RAS}_{0-3}$) | 2 ($\overline{RAS}_{2-3}$) |
| Ext. Refresh | Yes | No |

**Figure 8. 8203 Read Options**

Normal Reads are requested by activating the $\overline{RD}$ input, and keeping it active until the 8203 responds with an $\overline{XACK}$ pulse. The $\overline{RD}$ input can go inactive as soon as the command hold time ($t_{CHS}$) is met.

Advanced Read cycles are requested by pulsing ALE while S1 is active; if S1 is inactive (low) ALE is ignored. Advanced Read timing is similar to Normal Read timing, except the falling edge of ALE is used as the cycle start reference.

If a Read cycle is requested while a refresh cycle is in progress, then the 8203 will set the internal delayed-$\overline{SACK}$ latch. When the Read cycle is eventually started, the 8203 will delay the active $\overline{SACK}$ transition until $\overline{XACK}$ goes active, as shown in the A.C. timing diagrams. This delay was designed to compensate for the CPU's READY setup and hold times. The delayed-$\overline{SACK}$ latch is cleared after every READ cycle.

Based on system requirements, either $\overline{SACK}$ or $\overline{XACK}$ can be used to generate the CPU READY signal. $\overline{XACK}$ will normally be used; if the CPU can tolerate an advanced READY, then $\overline{SACK}$ can be used, but only if the CPU can tolerate the amount of advance provided by $\overline{SACK}$. If $\overline{SACK}$ arrives too early to provide the appropriate number of WAIT states, then either $\overline{XACK}$ or a delayed form of $\overline{SACK}$ should be used.

## Write Cycles

Write cycles are similar to Normal Read cycles, except the $\overline{WE}$ output. $\overline{WE}$ is held inactive for Read cycles, but goes active for Write cycles. All 8203 Write cycles are "early-write" cycles; $\overline{WE}$ goes active before $\overline{CAS}$ goes active by an amount of time sufficient to keep the dynamic RAM output buffers turned off.

## General System Considerations

All memory requests (Normal Reads, Advanced Reads, Writes) are qualified by the $\overline{PCS}$ input. $\overline{PCS}$ should be stable, either active or inactive, prior to the leading edge of $\overline{RD}$, $\overline{WR}$, or ALE. Systems which use battery backup should pullup $\overline{PCS}$ to prevent erroneous memory requests.

In order to minimize propagation delay, the 8203 uses an inverting address multiplexer without latches. The system must provide adequate address set-up and hold times to guarantee $\overline{RAS}$ and $\overline{CAS}$ setup and hold times for the RAM. The $t_{AD}$ A.C. parameter should be used for this system calculation.

The $B_0 - B_1$ inputs are similar to the address inputs in that they are not latched. $B_0$ and $B_1$ should not be changed during a memory cycle, since they directly control which $\overline{RAS}$ output is activated.

The 8203 uses a two-stage synchronizer for the memory request inputs ($\overline{RD}$, $\overline{WR}$, ALE), and a separate two stage synchronizer for the external refresh input (REFRQ). As with any synchronizer, there is always a finite probability of metastable states inducing system errors. The 8203 synchronizer was designed to have a system error rate less than 1 memory cycle every three years based on the full operating range of the 8203.

A microprocessor system is concerned when the data is valid after $\overline{RD}$ goes low. See Figure 9. In order to calculate memory read access times, the dynamic RAM's A.C. specifications must be examined, especially the $\overline{RAS}$-access time ($t_{RAC}$) and the $\overline{CAS}$-access time ($t_{CAC}$). Most configurations will be $\overline{CAS}$-access limited; i.e., the data from the RAM will be stable $t_{cc,max}$ (8203) + $t_{CAC}$ (RAM) after a memory read cycle is started. Be sure to add any delays (due to buffers, data latches, etc.) to calculate the overall read access time.

Since the 8203 normally performs "early-write" cycles, the data must be stable at the RAM data inputs by the time $\overline{CAS}$ goes active, including the RAM's data setup time. If the system does not normally guarantee sufficient write data setup, you must either delay the $\overline{WR}$ input signal or delay the 8203 $\overline{WE}$ output.

Delaying the $\overline{WR}$ input will delay all 8203 timing, including the READY handshake signals, $\overline{SACK}$ and $\overline{XACK}$, which may increase the number of WAIT states generated by the CPU.
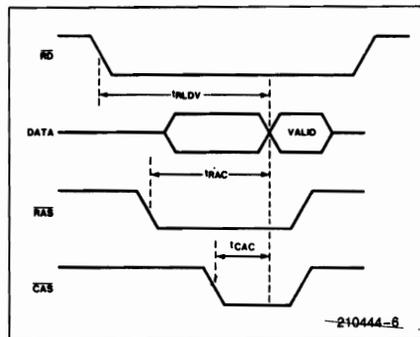


**Figure 9. Read Access Time**

If the $\overline{WE}$ output is externally delayed beyond the $\overline{CAS}$ active transition, then the RAM will use the falling edge of $\overline{WE}$ to strobe the write data into the RAM. This $\overline{WE}$ transition should not occur too late during the $\overline{CAS}$ active transition, or else the $\overline{WE}$ to $\overline{CAS}$ requirements of the RAM will not be met.

The $\overline{RAS}_{0-3}$, $\overline{CAS}$, $\overline{OUT}_{0-7}$, and $\overline{WE}$ outputs contain on-chip series damping resistors (typically 20$\Omega$) to minimize overshoot.

Some dynamic RAMs require more than 2.4V $V_{IH}$. Noise immunity may be improved for these RAMs by adding pull-up resistors to the 8203's outputs. Intel RAMs do not require pull-up resistors.



**Figure 10. Typical 8088 System**

# 8205
# HIGH SPEED 1 OUT OF 8 BINARY DECODER

- I/O Port or Memory Selector
- Simple Expansion — Enable Inputs
- High Speed Schottky Bipolar Technology — 18ns Max. Delay
- Directly Compatible with TTL Logic Circuits
- Low Input Load Current — .25 mA max., 1/6 Standard TTL Input Load
- Minimum Line Reflection — Low Voltage Diode Input Clamp
- Outputs Sink 10 mA min.
- 16-Pin Dual-In-Line Ceramic or Plastic Package

The Intel® 8205 decoder can be used for expansion of systems which utilize input ports, output ports, and memory components with active low chip select input. When the 8205 is enabled, one of its 8 outputs goes "low," thus a single row of a memory system is selected. The 3-chip enable inputs on the 8205 allow easy system expansion. For very large systems, 8205 decoders can be cascaded such that each decoder can drive 8 other decoders for arbitrary memory expansions.

The 8205 is packaged in a standard 16-pin dual in-line package. and its performance is specified over the temperature range of 0°C to +75°C, ambient. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than equivalent devices made with a gold diffussion process.
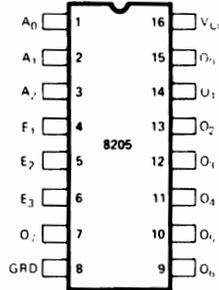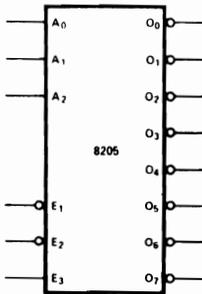


| ADDRESS | | | ENABLE | | | OUTPUTS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_0$ | $A_1$ | $A_2$ | $E_1$ | $E_2$ | $E_3$ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| L | L | L | L | L | H | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | L | H | H | H | L | H | H | H | H | H |
| H | H | L | L | L | H | H | H | H | L | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | L | H | H | H |
| H | L | H | L | L | H | H | H | H | H | H | L | H | H |
| L | H | H | L | L | H | H | H | H | H | H | H | L | H |
| H | H | H | L | L | H | H | H | H | H | H | H | H | L |
| X | X | X | L | L | L | H | H | H | H | H | H | H | H |
| X | X | X | H | L | L | H | H | H | H | H | H | H | H |
| X | X | X | L | H | L | H | H | H | H | H | H | H | H |
| X | X | X | H | H | L | H | H | H | H | H | H | H | H |
| X | X | X | H | L | H | H | H | H | H | H | H | H | H |
| X | X | X | L | H | H | H | H | H | H | H | H | H | H |
| X | X | X | H | H | H | H | H | H | H | H | H | H | H |

**Figure 1. Logic Symbol**



| $A_0$ $A_7$ | ADDRESS INPUTS |
|---|---|
| $\overline{E_1}$ $\overline{E_3}$ | ENABLE INPUTS |
| $\overline{O_0}$ $\overline{O_7}$ | DECODED OUTPUTS |

**Figure 2. Pin Configuration**

## Applications of the 8205

The 8205 can be used in a wide variety of applications in microcomputer systems. I/O ports can be decoded from the address bus, chip select signals can be generated to select memory devices and the type of machine state such as in 8008 systems can be derived from a simple decoding of the state lines (S0, S1, S2) of the 8008 CPU.

### I/O PORT DECODER

Shown in the figure below is a typical application of the 8205. Address input lines are decoded by a group of 8205s (3). Each input has a binary weight. For example, A0 is assigned a value of 1 and is the LSB; A4 is assigned a value of 16 and is the MSB. By connecting them to the decoders as shown, an active low signal that is exclusive in nature and represents the value of the input address lines, is available at the outputs of the 8205s.

This circuit can be used to generate enable signals for I/O ports or any other decoder related application.

Note that no external gating is required to decode up to 24 exclusive devices and that a simple addition of an inverter or two will allow expansion to even larger decoder networks.

### CHIP SELECT DECODER

Using a very similar circuit to the I/O port decoder, an ar-

ray of 8205s can be used to create a simple interface to a 24K memory system.
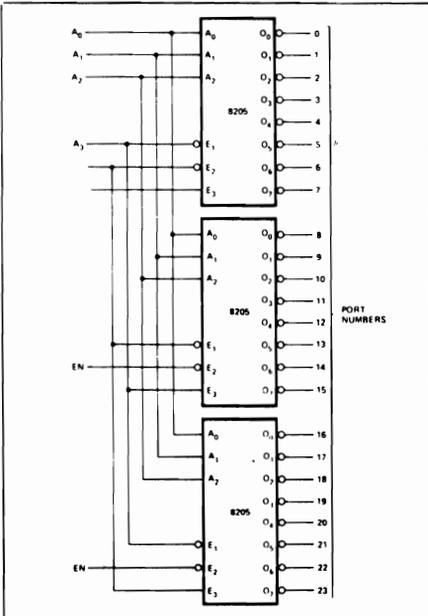
The memory devices used can be either ROM or RAM and are 1K in storage capacity. 2708s and 2114As are devices typically used for this application. This type of memory device has ten (10) address inputs and an active "low" chip select ($\overline{CS}$). The lower order address bits A0–A9 which come from the microprocessor are "bussed" to all memory elements and the chip select to enable a specific device or group of devices comes from the array of 8205s. The output of the 8205 is active low so it is directly compatible with the memory components.

Basic operation is that the CPU issues an address to identify a specific memory location in which it wishes to "write" or "read" data. The most significant address bits A10-A14 are decoded by the array of 8205s and an exclusive, active low, chip select is generated that enables a specific memory device. The least significant address bits A0-A9 identify a specific location within the selected device. Thus, all addresses throughout the entire memory array are exclusive in nature and are non-redundant.

This technique can be expanded almost indefinitely to support even larger systems with the addition of a few inverters and an extra decoder (8205).



Figure 4. I/O Port Decoder
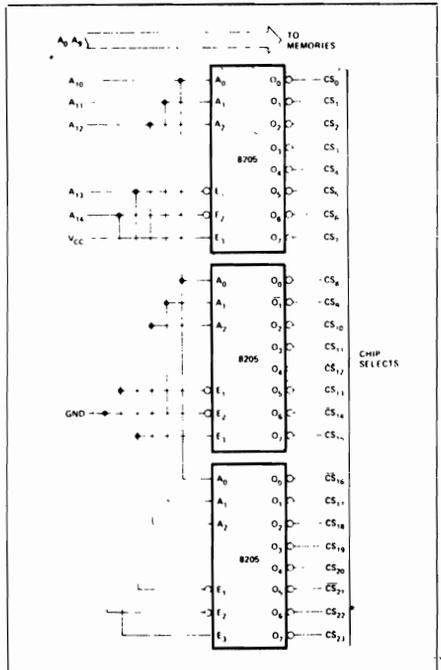


Figure 5. 24K Memory Interface

250

# 8206
# ERROR DETECTION AND CORRECTION UNIT

- **Detects All Single Bit, and Double Bit and Most Multiple Bit Errors**

- **Corrects All Single Bit Errors**

- 

| **3 Selections** | **8206-1** | **8206** |
|---|---|---|
| Detection | 35 ns | 42 ns |
| Correction | 55 ns | 67 ns |

- **Syndrome Outputs for Error Logging**

- **Automatic Error Scrubbing with 8207**

- **Expandable to Handle 80 Bit Memories**

- **Separate Input and Output Busses—No Timing Strobes Required**

- **Supports Read With and Without Correction, Writes, Partial (Byte) Writes, and Read-Modify-Writes**

- **HMOS III Technology for Low Power**

- **68 Pin Leadless JEDEC Package**

- **68 Pin Grid Array Package**

The HMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each 8206 handles 8 or 16 data bits and up to 8 check bits. 8206's can be cascaded to provide correction and detection for up to 80 bits of data. Other 8206 features include the ability to handle byte writes, memory initialization, and error logging.
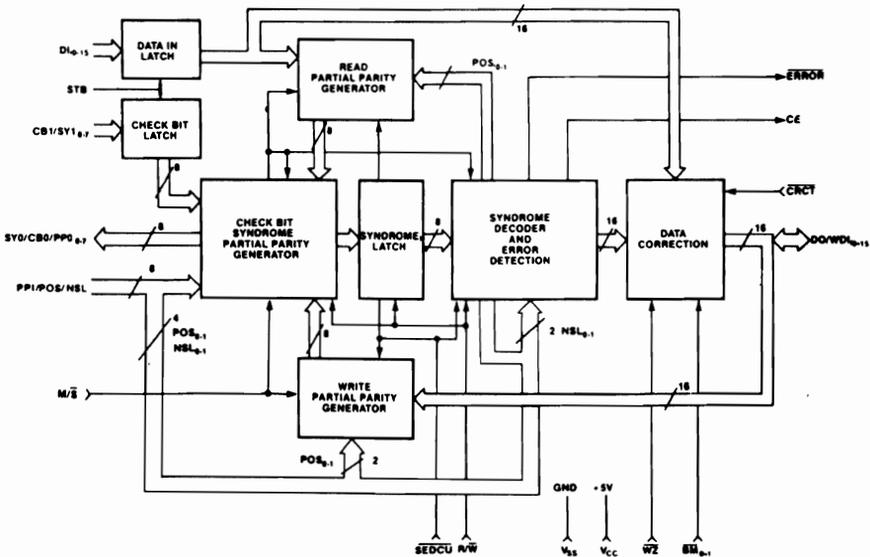


**Figure 1. 8206 Block Diagram**

205220-1

**Table 1. 8206 Pin Description**

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| $DI_{0-15}$ | 1, 68-61, 59-53 | I | **DATA IN:** These inputs accept a 16 bit data word from RAM for error detection and/or correction. |
| $CBI/SYI_0$<br>$CBI/SYI_1$<br>$CBI/SYI_2$<br>$CBI/SYI_3$<br>$CBI/SYI_4$<br>$CBI/SYI_5$<br>$CBI/SYI_6$<br>$CBI/SYI_7$ | 5<br>6<br>7<br>8<br>9<br>10<br>11<br>12 | I<br>I<br>I<br>I<br>I<br>I<br>I<br>I | **CHECK BITS IN/SYNDROME IN:** In a single 8206 system, or in the master in a multi-8206 system, these inputs accept the check bits (5 to 8) from the RAM. In a single 8206 16 bit system, $CBI_{0-5}$ are used. In slave 8206's these inputs accept the syndrome from the master. |
| $DO/WDI_0$<br>$DO/WDI_1$<br>$DO/WDI_2$<br>$DO/WDI_3$<br>$DO/WDI_4$<br>$DO/WDI_5$<br>$DO/WDI_6$<br>$DO/WDI_7$<br>$DO/WDI_8$<br>$DO/WDI_9$<br>$DO/WDI_{10}$<br>$DO/WDI_{11}$<br>$DO/WDI_{12}$<br>$DO/WDI_{13}$<br>$DO/WDI_{14}$<br>$DO/WDI_{15}$ | 51<br>50<br>49<br>48<br>47<br>46<br>45<br>44<br>42<br>41<br>40<br>39<br>38<br>37<br>36<br>35 | I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O | **DATA OUT/WRITE DATA IN:** In a read cycle, data accepted by $DI_{0-15}$ appears at these outputs corrected if $\overline{CRCT}$ is low, or uncorrected if $\overline{CRCT}$ is high. The $\overline{BM}$ inputs must be high to enable the output buffers during the read cycle. In a write cycle, data to be written into the RAM is accepted by these inputs for computing the write check bits. In a partial-write cycle, the byte not to be modified appears at either $DO_{0-7}$ if $\overline{BM}_0$ is high, or $DO_{8-15}$ if $\overline{BM}_1$ is high, for writing to the RAM. When $\overline{WZ}$ is active, it causes the 8206 to output all zeros at $DO_{0-15}$, with the proper write check bits on CBO. |
| $SYO/CBO/PPO_0$<br>$SYO/CBO/PPO_1$<br>$SYO/CBO/PPO_2$<br>$SYO/CBO/PPO_3$<br>$SYO/CBO/PPO_4$<br>$SYO/CBO/PPO_5$<br>$SYO/CBO/PPO_6$<br>$SYO/CBO/PPO_7$ | 23<br>24<br>25<br>27<br>28<br>29<br>30<br>31 | O<br>O<br>O<br>O<br>O<br>O<br>O<br>O | **SYNDROME OUT/CHECK BITS OUT/PARTIAL PARITY OUT:** In a single 8206 system, or in the master in a multi-8206 system, the syndrome appears at these outputs during a read. During a write, the write check bits appear. In slave 8206's the partial parity bits used by the master appear at these outputs. The syndrome is latched (during read-modify-writes) by R/$\overline{W}$ going low. |
| $PPI_0/POS_0$<br>$PPI_1/POS_1$ | 13<br>14 | I<br>I | **PARTIAL PARITY IN/POSITION:** In the master in a multi-8206 system, these inputs accept partial parity bits 0 and 1 from the slaves. In a slave 8206 these inputs inform it of its position within the system (1 to 4). Not used in a single 8206 system. |
| $PPI_2/NSL_0$<br>$PPI_3/NSL_1$ | 15<br>16 | I<br>I | **PARTIAL PARITY IN/NUMBER OF SLAVES:** In the master in a multi-8206 system, these inputs accept partial parity bits 2 and 3 from the slaves. In a multi-8206 system these inputs are used in slave number 1 to tell it the total number of slaves in the system (1 to 4). Not used in other slaves or in a single 8206 system. |
| $PPI_4CE$ | 17 | I/O | **PARTIAL PARITY IN/CORRECTABLE ERROR:** In the master in a multi-8206 system this pin accepts partial parity bit 4. In slave number 1 only, or in a single 8206 system, this pin outputs the correctable error flag. CE is latched by R/$\overline{W}$ going low. Not used in other slaves. |

# 8207
# DUAL-PORT DYNAMIC RAM CONTROLLER

- **Provides All Signals Necessary to Control 16K, 64K and 256K Dynamic RAMs**
- **Directly Addresses and Drives up to 2 Megabytes without External Drivers**
- **Supports Single and Dual-Port Configurations**
- **Automatic RAM Initialization in All Modes**
- **Four Programmable Refresh Modes**
- **Transparent Memory Scrubbing in ECC Mode**

- **Fast Cycle Support for 8 MHz 80286 with 8207-16**
- **Slow Cycle Support for 8 MHz, 10 MHz 8086/88, 80186/188 with 8207-8, 8207-10**
- **Provides Signals to Directly Control the 8206 Error Detection and Correction Unit**
- **Supports Synchronous or Asynchronous Operation on Either Port**
- **68 Lead JEDEC Type A Leadless Chip Carrier (LCC) and Pin Grid Array (PGA), Both in Ceramic.**

The Intel 8207 Dual-Port Dynamic RAM Controller is a high-performance, systems-oriented, Dynamic RAM controller that is designed to easily interface 16K, 64K and 256K Dynamic RAMs to Intel and other microprocessor systems. A dual-port interface allows two different busses to independently access memory. When configured with an 8206 Error Detection and Correction Unit the 8207 supplies the necessary logic for designing large error-corrected memory arrays. This combination provides automatic memory initialization and transparent memory error scrubbing.
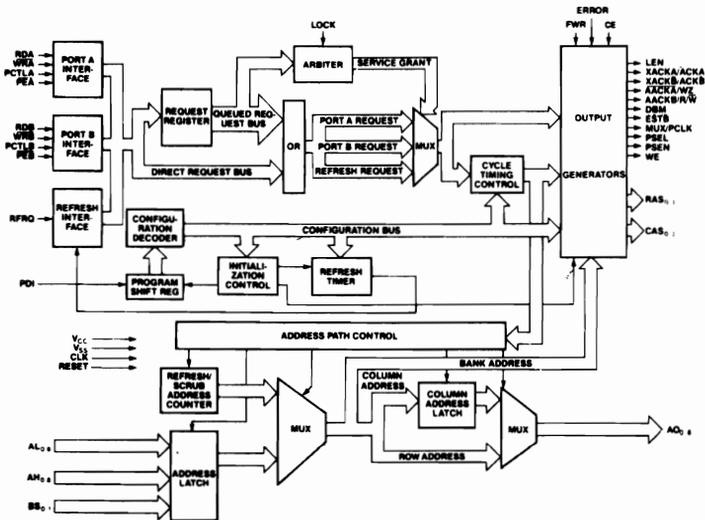


**Figure 1. 8207 Block Diagram**

210463–1

# 82C08
# CHMOS DYNAMIC RAM CONTROLLER

- **0 Wait State with INTEL μProcessors**

- **iAPX 286** ⎤  82C08-20 20 MHz
  **(10, 8 MHz)** ⎦  82C08-16 16 MHz
  **iAPX 186/88** ⎤  82C08-10 10 MHz
  **86/88** ⎦  82C08-8 8 MHz

- **Supports 64K and 256K DRAMs (256K x 1 and 256K x 4 Organizations)**

- **Power Down Mode with Programmable Memory Refresh using Battery Backup**

- **Directly Addresses and Drives up to 1 Megabyte without External Drivers**

- **Microprocessor Data Transfer and Advance Acknowledge Signals**

- **Five Programmable Refresh Modes**

- **Automatic RAM Warm-up**

- **Pin-Compatible with 8208**

- **48 Lead Plastic DIP; 68 Lead PLCC**

  (See Intel Packaging; Order Number: 231369-001)

- **Compatible with Normal Modes of Static Column and Ripplemode DRAMs**

The Intel 82C08 Dynamic RAM Controller is a CMOS, high performance, systems oriented, Dynamic RAM controller that is designed to easily interface 64K and 256K Dynamic RAMs to Intel and other microprocessors. The 82C08 also has a power down mode where only the refresh logic is activated using battery backup.
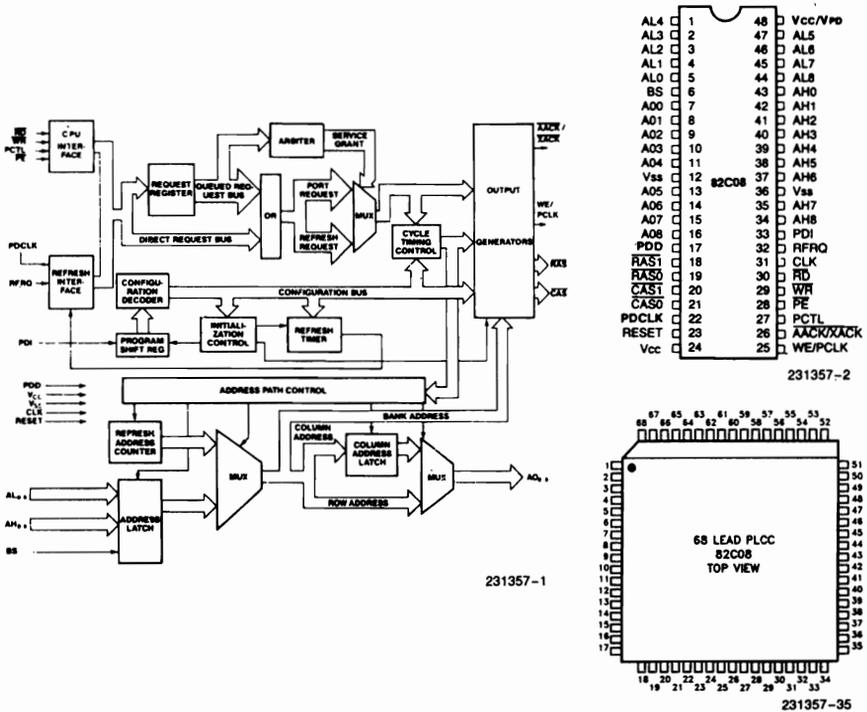


**Figure 1. Block Diagram and Pinout Diagrams**

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# 8212
# 8-BIT INPUT/OUTPUT PORT

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — .25mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8008, 8080A, or 8085A CPU

- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.



Figure 1. Logic Diagram
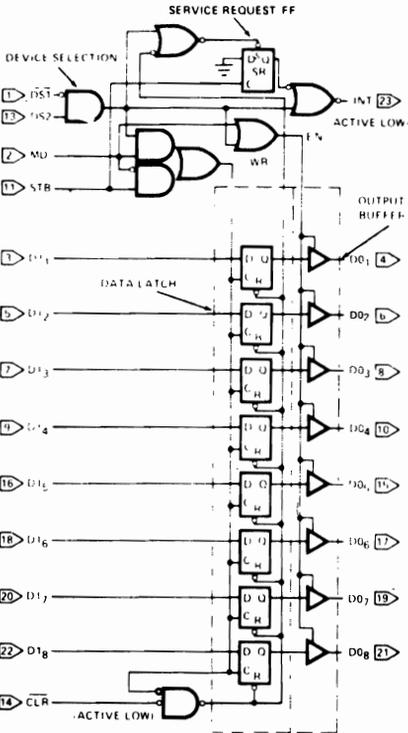


Figure 2. Pin Configuration
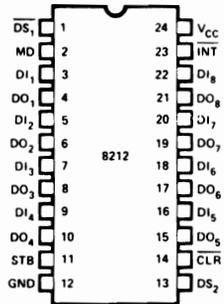
| DI₁-DI₈ | DATA IN |
|---|---|
| DO₁-DO₈ | DATA OUT |
| DS₁-DS₂ | DEVICE SELECT |
| MD | MODE |
| STB | STROBE |
| INT | INTERRUPT (ACTIVE LOW) |
| CLR | CLEAR (ACTIVE LOW) |

255

# FUNCTIONAL DESCRIPTION

## Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The latched data is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

## Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

The high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

## Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

## DS1, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

## MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

## STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

## Service Request Flip-Flop

The (SR) flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS1} \cdot DS2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.



| STB | MD | ($DS_1 \cdot DS_2$) | DATA OUT EQUALS | | CLR | ($\overline{DS_1} \cdot DS_2$) | STB | *SR | INT |
|-----|----|---------------------|-----------------|--|-----|------|-----|-----|-----|
| 0 | 0 | 0 | | 3 STATE | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | | 3 STATE | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | | DATA LATCH | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | | DATA LATCH | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | | DATA LATCH | 1 | 1 | _ | 0 | 1 |
| 1 | 0 | 1 | | DATA IN | 1 | 0 | _ | 1 | 1 |
| 0 | 1 | 1 | | DATA IN | | | | | |
| 1 | 1 | 1 | | DATA IN | | | *INTERNAL SR FLIP-FLOP | | |

$\overline{CLR}$ – RESETS DATA LATCH
SETS SR FLIP FLOP
(NO EFFECT ON OUTPUT BUFFER)

AFN-00731C
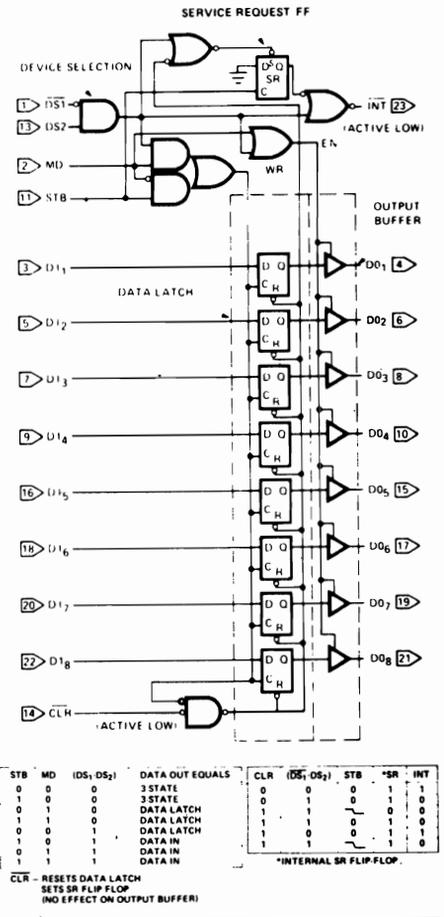
# 8216/8226
# 4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

- Data Bus Buffer Driver for 8080 CPU

- Low Input Load Current — 0.25 mA Maximum

- High Output Drive Capability for Driving System Bus

- 3.65V Output High Voltage for Direct Interface to 8080 CPU

- 3-State Outputs

- Reduces System Package Count

- Available in EXPRESS
  – Standard Temperature Range

The 8216/8226 is a 4-bit bidirectional bus driver/receiver. All inputs are low power TTL compatible. For driving MOS. the DO outputs provide a high 3.65V $V_{OH}$, and for high capacitance terminated bus structures, the DB outputs provide a high 50 mA $I_{OL}$ capability. A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

*Note: The specifications for the 3216/3226 are identical with those for the 8216/8226



| | | |
|---|---|---|
| $DB_0$-$DB_3$ | DATA BUS BIDIRECTIONAL | |
| $DI_0$-$DI_3$ | DATA INPUT | |
| $DO_0$-$DO_3$ | DATA OUTPUT | |
| $\overline{DIEN}$ | DATA IN ENABLE DIRECTION CONTROL | |
| $\overline{CS}$ | CHIP SELECT | |
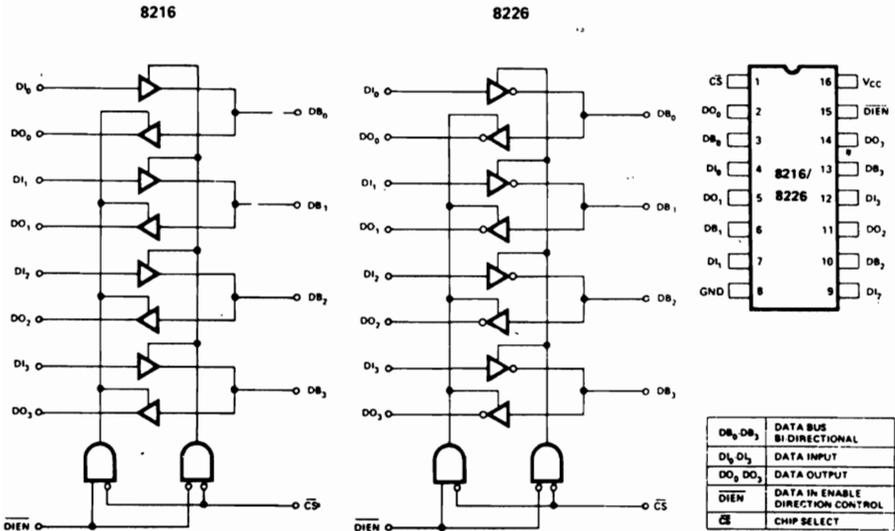
Figure 1. Block Diagrams                Figure 2. Pin Configuration

# 8218/8219
# BIPOLAR MICROCOMPUTER BUS
# CONTROLLERS FOR MCS-80® AND MCS-85® FAMILIES

- 8218 for Use in MCS-80® Systems
- 8219 for Use inMCS-85® Systems
- Coordinates the Sharing of a Common Bus Between Several CPU's
- Reduces Component Count in Multimaster Bus Arbitration Logic
- Single +5 Volt Power Supply
- 28 Pin Package

The 8218 and 8219 Microcomputer Bus Controllers consist of control logic which allows a bus master device such as a CPU or DMA channel to interface with other masters on a common bus, sharing memory and I/O devices. The 8218 and 8219 consist of:

1. Bus Arbitration Logic which operates from the Bus Clock ($\overline{BCLK}$) and resolves bus contention between devices sharing a common bus.
2. Timing Logic which when initiated by the bus arbitration logic generates timing signals for the memory and I/O command lines to guarantee set-up and hold times of the address/data lines onto the bus. The timing logic also signals to the bus arbitration logic when the current data transfer is completed and the bus is no longer needed.
3. Output Drive Logic which contains the logic and output drivers for the memory and I/O command lines.

An external RC time constant is used with the timing logic to generate the guaranteed address set-up and hold times on the bus. The 8219 can interface directly to the 8085A CPU and the 8218 interfaces to the 8080A CPU chip and the 8257 DMA controller.
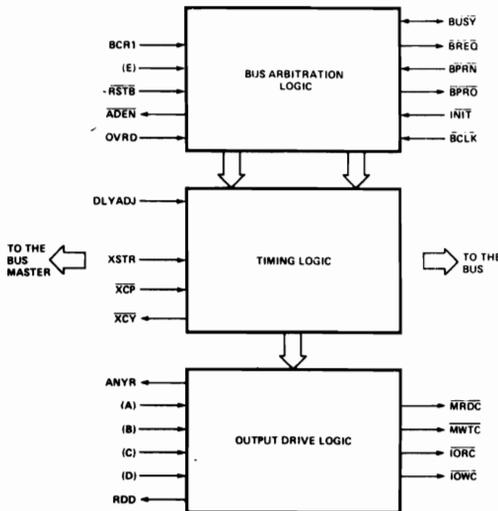


Figure 1. Block Diagram
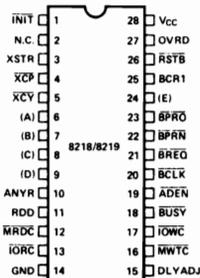


Figure 2. Pin Configuration

# 8224
# CLOCK GENERATOR AND DRIVER
# FOR 8080A CPU

- Single Chip Clock Generator/Driver for 8080A CPU

- Power-Up Reset for CPU

- Ready Synchronizing Flip-Flop

- Advanced Status Strobe

- Oscillator Output for External System Timing

- Crystal Controlled for Stable System Operation

- Reduces System Package Count

- Available in EXPRESS
  - Standard Temperature Range

The Intel* 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.
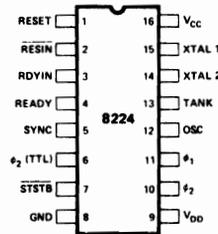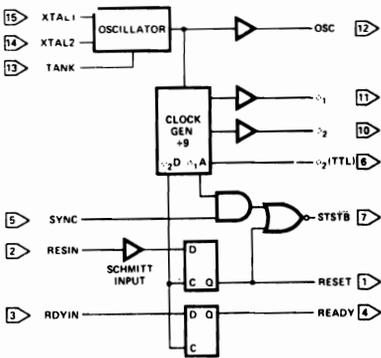


| RESIN | RESET INPUT |
| RESET | RESET OUTPUT |
| RDYIN | READY INPUT |
| READY | READY OUTPUT |
| SYNC | SYNC INPUT |
| STSTB | STATUS STB (ACTIVE LOW) |
| $\phi_1$ | 8080 |
| $\phi_2$ | CLOCKS |

| XTAL 1 | CONNECTIONS |
| XTAL 2 | FOR CRYSTAL |
| TANK | USED WITH OVERTONE XTAL |
| OSC | OSCILLATOR OUTPUT |
| $\phi_2$ (TTL) | $\phi_2$ CLK (TTL LEVEL) |
| $V_{CC}$ | +5V |
| $V_{DD}$ | +12V |
| GND | 0V |

Figure 1. Block Diagram                    Figure 2. Pin Configuration

# 8228/8238
# SYSTEM CONTROLLER AND BUS DRIVER
# FOR 8080A CPU

- **Single Chip System Control for MCS-80® Systems**

- **Built-In Bidirectional Bus Driver for Data Bus Isolation**

- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**

- **User Selected Single Level Interrupt Vector (RST 7)**

- **28-Pin Dual In-Line Package**

- **Reduces System Package Count**

- **8238 Had Advanced IOW/MEMW for Large System Timing Control**

- **Available in EXPRESS – Standard Temperature Range**

The Intel® 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable design of the MCS-80 systems.

Note: The specifications for the 3228/3238 are identical with those for the 8228/8238
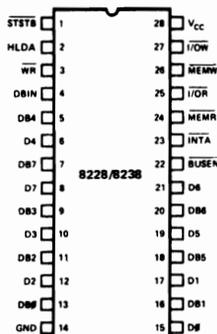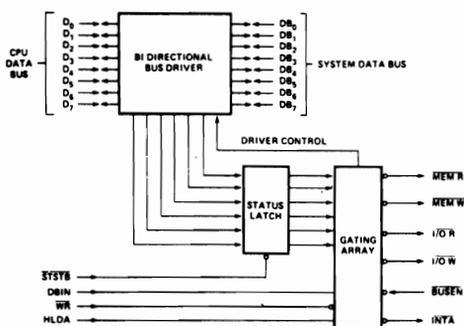


| D7 D0 | DATA BUS (8080 SIDE) |
|---|---|
| DB7 DB0 | DATA BUS (SYSTEM SIDE) |
| I/OR | I/O READ |
| I/OW | I/O WRITE |
| MEMR | MEMORY READ |
| MEMW | MEMORY WRITE |
| DBIN | DBIN (FROM 8080) |

| INTA | INTERRUPT ACKNOWLEDGE |
|---|---|
| HLDA | HLDA (FROM 8080) |
| WR | WR (FROM 8080) |
| BUSEN | BUS ENABLE INPUT |
| STSTB | STATUS STROBE (FROM 8224) |
| Vcc | +5V |
| GND | 0 VOLTS |

**Figure 1. Block Diagram**

**Figure 2. Pin Configuration**

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# 8231A
# ARITHMETIC PROCESSING UNIT

- ■ Fixed Point Single and Double Precision (16/32 Bit)
- ■ Floating Point Single Precision (32 Bit)
- ■ Binary Data Formats
- ■ Add, Subtract, Multiply and Divide
- ■ Trignometric and Inverse Trigonometric Functions
- ■ Square Roots, Logarithms, Exponentiation
- ■ Float to Fixed and Fixed to Float Conversions
- ■ Stack Oriented Operand Storage

- ■ Compatible with all Intel and most other Microprocessor Families
- ■ Direct Memory Access or Programmed I/O Data Transfers
- ■ End of Execution Signal
- ■ General Purpose 8-Bit Data Bus Interface
- ■ Standard 24 Pin Package
- ■ +12V and +5V Power Supplies
- ■ Advanced N-Channel Silicon Gate HMOS Technology

The Intel® 8231 Arithmetic Processing Unit (APU) is a monolithic HMOS LSI device that provides high performance fixed and floating point arithmetic and floating point trigonometric operations. It may be used to enhance the mathematical capability of a wide variety of processor-oriented systems. Chebyshev polynomials are used in the implementation of the APU algorithms.

All transfers, including operand, result, status and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and commands are issued to perform operations on the data and the stack. Results are then available to be retrieved from the stack.

Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end of execution signal that may be used as an interrupt by the CPU to help coordinate program execution.
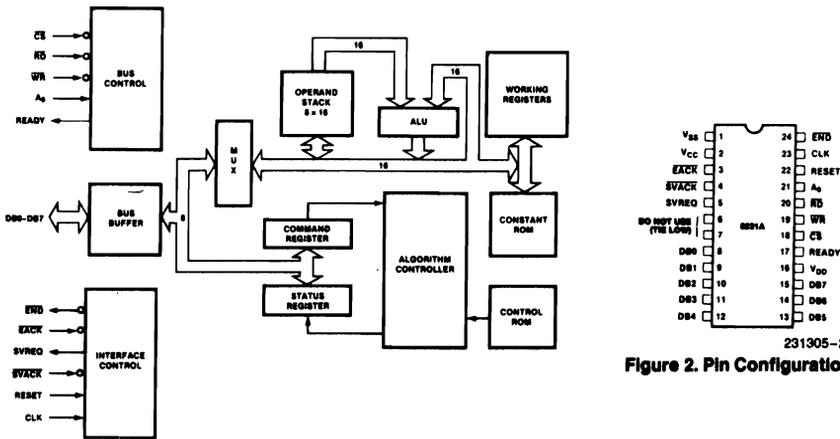


Figure 1. Block Diagram

231305-1



231305-2

Figure 2. Pin Configuration

261
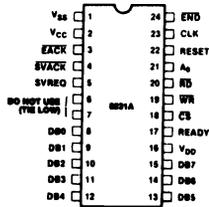
# 8232
# FLOATING POINT PROCESSING UNIT

- Compatible with Proposed IEEE Format and Existing Intel Floating Point Standard

- Single (32-Bit) and Double (64-Bit) Precision Capability

- Add, Subtract, Multiply and Divide Functions

- Stack Oriented Operand Storage

- General Purpose 8-Bit Data Bus Interface

- Standard 24-Pin Package

- 12V and 5V Power Supplies

- Compatible with MCS-80™, MCS-85™ and MCS-86™ Microprocessor Families

- Error Interrupt

- Direct Memory Access or Programmed I/O Data Transfers

- End of Execution Signal

- Advanced N-Channel Silicon Gate HMOS Technology

The Intel® 8232 is a high performance floating-point processor unit (FPU). It provides single precision (32-bit) and double precision (64-bit) add, subtract, multiply and divide operations. The 8232's floating point arithmetic is a subset of the proposed IEEE standard. It can be easily interfaced to enhance the computational capabilities of the host microprocessor.

The operand, result, status and command information transfers take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack by the host processor and a command is issued to perform an operation on the data stack. The results of the operation are available to the host processor from the stack.

Information transfers between the 8232 and the host processor can be handled by using programmed I/O or direct memory access techniques. After completing an operation, the 8232 activates an "end of execution" signal that can be used to interrupt the host processor.
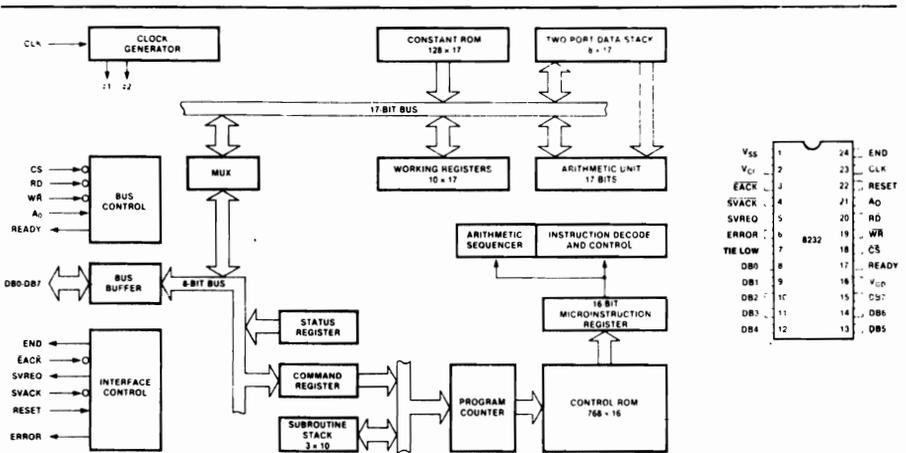


Figure 1. Block Diagram
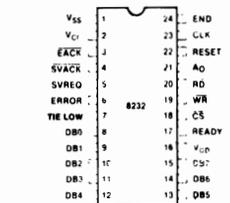
Figure 2. Pin Configuration

# 8237A/8237A-4/8237A-5
# HIGH PERFORMANCE
# PROGRAMMABLE DMA CONTROLLER

- **Enable/Disable Control of Individual DMA Requests**

- **Four Independent DMA Channels**

- **Independent Autoinitialization of all Channels**

- **Memory-to-Memory Transfers**

- **Memory Block Initialization**

- **Address Increment or Decrement**

- **High performance: Transfers up to 1.6M Bytes/Second with 5 MHz 8237A-5**

- **Directly Expandable to any Number of Channels**

- **End of Process Input for Terminating Transfers**

- **Software DMA Requests**

- **Independent Polarity Control for DREQ and DACK Signals**

- **Available in EXPRESS**
  **– Standard Temperature Range**

The 8237A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 8237A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The 8237A is designed to be used in conjunction with an external 8-bit address register such as the 8282. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process (EOP).

Each channel has a full 64K address and word count capability.

The 8237A-4 and 8237A-5 are 4 MHz and 5 MHz selected versions of the standard 3 MHz 8237A respectively.



**Figure 1. Block Diagram**



**Figure 2.**
**Pin Configuration**

## Table 1. Pin Description

| Symbol | Type | Name and Function |
|---|---|---|
| $V_{CC}$ | | **Power:** +5 volt supply. |
| $V_{SS}$ | | **Ground:** Ground. |
| CLK | I | **Clock Input:** Clock Input controls the internal operations of the 8237A and its rate of data transfers. The input may be driven at up to 3 MHz for the standard 8237A and up to 5 MHz for the 8237A-5. |
| CS | I | **Chip Select:** Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus. |
| RESET | I | **Reset:** Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle. |
| READY | I | **Ready:** Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time. |
| HLDA | I | **Hold Acknowledge:** The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses. |
| DREQ0–DREQ3 | I | **DMA Request:** The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset intializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. |
| DB0–DB7 | I/O | **Data Bus:** The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237A control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location. |
| IOR | I/O | **I/O Read:** I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237A to access data from a peripheral during a DMA Write transfer. |
| IOW | I/O | **I/O Write:** I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 8237A. In the Active cycle, it is an output control signal used by the 8237A to load data to the peripheral during a DMA Read transfer. |
| EOP | I/O | **End of Process:** End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional EOP pin. The 8237A allows an external signal to terminate an active DMA service. This is accomplished by pulling the EOP input low with an external EOP signal. The 8237A also generates a pulse when the terminal count (TC) for any channel is reached. This generates an EOP signal which is output through the EOP Line. The reception of EOP, either internal or external, will cause the 8237A to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by EOP unless the channel is programmed for Autoinitialize. In that case, the mask bit remains clear. During memory-to-memory transfers, EOP will be output when the TC for channel 1 occurs. EOP should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs. |
| A0–A3 | I/O | **Address:** The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the 8237A to address the control register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address. |

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## Table 1. Pin Description (Continued)

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| A4-A7 | O | **Address:** The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service. |
| HRQ | O | **Hold Request:** This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ. After HRQ goes active at least one clock cycle (TCY) must occur before HLDA goes active. |
| DACK0-DACK3 | O | **DMA Acknowledge:** DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low. |

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| AEN | O | **Address Enable:** Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH. |
| ADSTB | O | **Address Strobe:** The active high, Address Strobe is used to strobe the upper address byte into an external latch. |
| MEMR | O | **Memory Read:** The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer. |
| MEMW | O | **Memory Write:** The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer. |

## FUNCTIONAL DESCRIPTION

The 8237A block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The 8237A contains 344 bits of internal memory in the form of registers. Figure 3 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

| Name | Size | Number |
|------|------|--------|
| Base Address Registers | 16 bits | 4 |
| Base Word Count Registers | 16 bits | 4 |
| Current Address Registers | 16 bits | 4 |
| Current Word Count Registers | 16 bits | 4 |
| Temporary Address Register | 16 bits | 1 |
| Temporary Word Count Register | 16 bits | 1 |
| Status Register | 8 bits | 1 |
| Command Register | 8 bits | 1 |
| Temporary Register | 8 bits | 1 |
| Mode Registers | 6 bits | 4 |
| Mask Register | 4 bits | 1 |
| Request Register | 4 bits | 1 |

### Figure 3. 8237A Internal Registers

The 8237A contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the 8237A. The Program Command Control block decodes the various commands given to the 8237A by the microprocessor prior to servicing a DMA Request. It also decodes the Mode Control word used to select the type of DMA during the servicing. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In 8237A systems this input will usually

be the φ2 TTL clock from an 8224 or CLK from an 8085AH or 8284A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) does not satisfy 8237A-5 clock LOW and HIGH time requirements. In this case, an external clock should be used to drive the 8237A-5.

## DMA Operation

The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The 8237A can assume seven separate states, each composed of one full clock period. State I (SI) is the inactive state. It is entered when the 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State S0 (S0) is the first state of a DMA service. The 8237A has requested a hold but the processor has not yet returned an acknowledge. The 8237A may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the 8237A. Note that the data is transferred directly from the I/O device to memory (or vice versa) with IOR and MEMW (or MEMR and IOW) being active at the same time. The data is not read into or driven out of the 8237A in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half

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and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

## IDLE CYCLE

When no channel is requesting service, the 8237A will enter the Idle cycle and perform "SI" states. In this cycle the 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample CS, looking for an attempt by the microprocessor to write or read the internal registers of the 8237A. When CS is low and HLDA is low, the 8237A enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0–A3 are inputs to the device and select which registers will be read or written. The IOR and IOW lines are used to select and time reads or writes. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. This bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. A separate software command can also reset this flip-flop.

Special software commands can be executed by the 8237A in the Program Condition. These commands are decoded as sets of addresses with the CS and IOW. The commands do not make use of the data bus. Instructions include Clear First/Last Flip-FLop and Master Clear.

## ACTIVE CYCLE

When the 8237A is in the Idle cycle and a non-masked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

**Single Transfer Mode** — In Single Transfer mode the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, in 8080A, 8085AH, 8088, or 8086 system this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 8237A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

**Block Transfer Mode** — In Block Transfer mode the device is activated by DREQ to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process (EOP) is encountered. DREQ need only be held active until DACK

becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for it.

**Demand Transfer Mode** — In Demand Transfer mode the device is programmed to continue making transfers until a TC or external EOP is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 8237A Current Address and Current Word Count registers. Only an EOP can cause an Autoinitialize at the end of the service. EOP is generated either by TC or by an external signal.

**Cascade Mode** — This mode is used to cascade more than one 8237A together for simple system expansion. The HRQ and HLDA signals from the additional 8237A are connected to the DREQ and DACK signals of a channel of the initial 8237A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 8237A is used only for prioritizing the additional device, it does not output any address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The 8237A will respond to DREQ and DACK but all other outputs except HRQ will be disabled.

Figure 4 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More 8237As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.
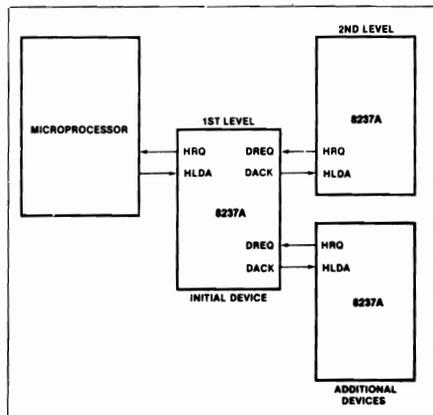


**Figure 4. Cascaded 8237As**

## TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating MEMW and IOR. Read transfers move data from memory to an I/O device by activating MEMR and IOW. Verify transfers are pseudo transfers. The 8237A operates as in Read or Write transfers generating addresses, and responding to EOP, etc. However, the memory and I/O control lines all remain inactive. Verify mode is not permitted during memory to memory operation.

**Memory-to-Memory** — To perform block moves of data from one memory address space to another with a minimum of program effort and time, the 8237A includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The 8237A requests a DMA service in the normal manner. After HLDA is true, the device, using eight-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 8237A internal Temporary register. Channel 1 then writes the data from the Temporary register to memory using the address in its Current Address register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count is decremented. When the word count of channel 1 goes to FFFFH, a TC is generated causing an EOP output terminating the service.

Channel 0 may be programmed to retain the same address for all transfers. This allows a single word to be written to a block of memory.

The 8237A will respond to external EOP signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 12. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

**Autoinitialize** — By programming a bit in the Mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialize initialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following EOP. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected.

**Priority** — The 8237A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interferring with that service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.
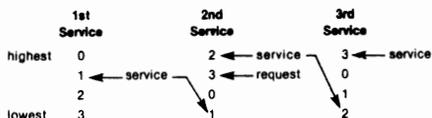


With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

**Compressed Timing** — In order to achieve even greater throughput where system characteristics permit, the 8237A can compress the transfer time to two clock cycles. From Figure 11 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8–A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 14.

**Address Generation** — In order to reduce pin count, the 8237A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 8237A directly. Lines A0–A7 should be connected to the address bus. Figure 11 shows the time relationships between CLK, AEN, ADSTB, DB0–DB7 and A0–A7.

During Block and Demand Transfer mode services, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 8237A executes S1 states only when updating of A8–A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

## REGISTER DESCRIPTION

**Current Address Register** — Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$.

**Current Word Register** — Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialization back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

**Base Address and Base Word Count Registers** — Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

**Command Register** — This 8-bit register controls the operation of the 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits. See Figure 6 for address coding.

**Mode Register** — Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

**Request Register** — The 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{EOP}$. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 5 for register address coding. In order to make a software request, the channel must be in Block Mode.
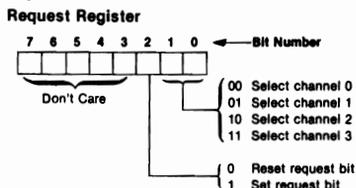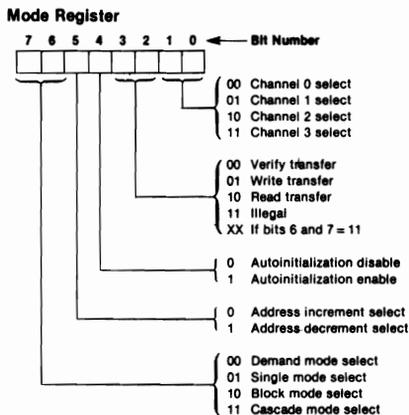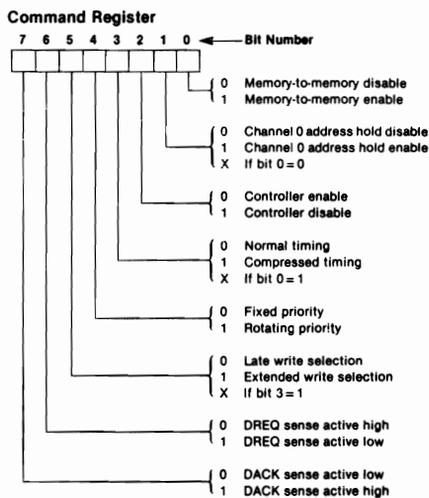
**Command Register**



**Mode Register**



**Request Register**



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**Mask Register** — Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 5 for instruction addressing.
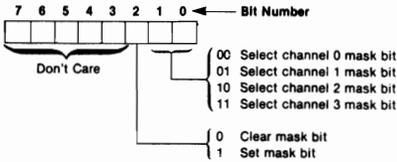


All four bits of the Mask register may also be written with a single command.





**Figure 5. Definition of Register Codes**

**Status Register** — The Status register is available to be read out of the 8237A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0–3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset and on each Status Read. Bits 4–7 are set whenever their corresponding channel is requesting service.
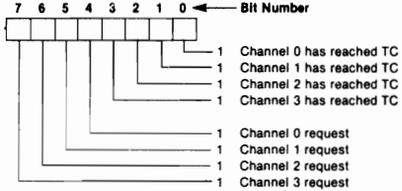


**Temporary Register** — The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

**Software Commands** — These are additional special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

*Clear First/Last Flip-Flop:* This command is executed prior to writing or reading new address or word count information to the 8237A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

*Master Clear:* This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers are cleared and the Mask register is set. The 8237A will enter the Idle cycle.

*Clear Mask Register:* This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Figure 6 lists the address codes for the software commands:



**Figure 6. Software Command Codes**

| Channel | Register | Operation | CS | IOR | IOW | A3 | A2 | A1 | A0 | Internal Flip-Flop | Data Bus DB0-DB7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | Base and Current Address | Write | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | A0–A7 |
|   |                          |       | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | A8–A15 |
|   | Current Address | Read | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0–A7 |
|   |                 |      | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A8–A15 |
|   | Base and Current Word Count | Write | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | W0–W7 |
|   |                             |       | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | W8–W15 |
|   | Current Word Count | Read | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | W0–W7 |
|   |                    |      | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | W8–W15 |
| 1 | Base and Current Address | Write | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | A0–A7 |
|   |                          |       | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | A8–A15 |
|   | Current Address | Read | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | A0–A7 |
|   |                 |      | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A8–A15 |
|   | Base and Current Word Count | Write | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | W0–W7 |
|   |                             |       | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | W8–W15 |
|   | Current Word Count | Read | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | W0–W7 |
|   |                    |      | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | W8–W15 |
| 2 | Base and Current Address | Write | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | A0–A7 |
|   |                          |       | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | A8–A15 |
|   | Current Address | Read | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A0–A7 |
|   |                 |      | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | A8–A15 |
|   | Base and Current Word Count | Write | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | W0–W7 |
|   |                             |       | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | W8–W15 |
|   | Current Word Count | Read | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | W0–W7 |
|   |                    |      | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | W8–W15 |
| 3 | Base and Current Address | Write | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | A0–A7 |
|   |                          |       | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | A8–A15 |
|   | Current Address | Read | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | A0–A7 |
|   |                 |      | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | A8–A15 |
|   | Base and Current Word Count | Write | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | W0–W7 |
|   |                             |       | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | W8–W15 |
|   | Current Word Count | Read | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | W0–W7 |
|   |                    |      | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | W8–W15 |

Figure 7. Word Count and Address Register Command Codes

## PROGRAMMING

The 8237A will accept programming from the host processor any time that HLDA is inactive; this is true even if HRQ is active. The responsibility of the host is to assure that programming and HLDA are mutually exclusive. Note that a problem can occur if a DMA request occurs, on an unmasked channel while the 8237A is being programmed. For instance, the CPU may be starting to reprogram the two byte Address register of channel 1 when channel 1 receives a DMA request. If the 8237A is enabled (bit 2 in the command register is 0) and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any other registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations, especially the Mode registers, be loaded with some valid value. This should be done even if some channels are unused.

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## APPLICATION INFORMATION

Figure 8 shows a convenient method for configuring a DMA system with the 8237A controller and an 8080A/8085AH microprocessor system. The multimode DMA controller issues a HRQ to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a HLDA signal, the 8237A takes control of the address bus, the data bus and the control bus. The address for the first transfer operation comes out in two bytes — the least significant 8 bits on the eight address outputs and the most significant 8 bits on the data bus. The contents of the data bus are then latched into the 8282 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high speed, 8-bit, three-state latch in a 20-pin package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one 8237A is used.
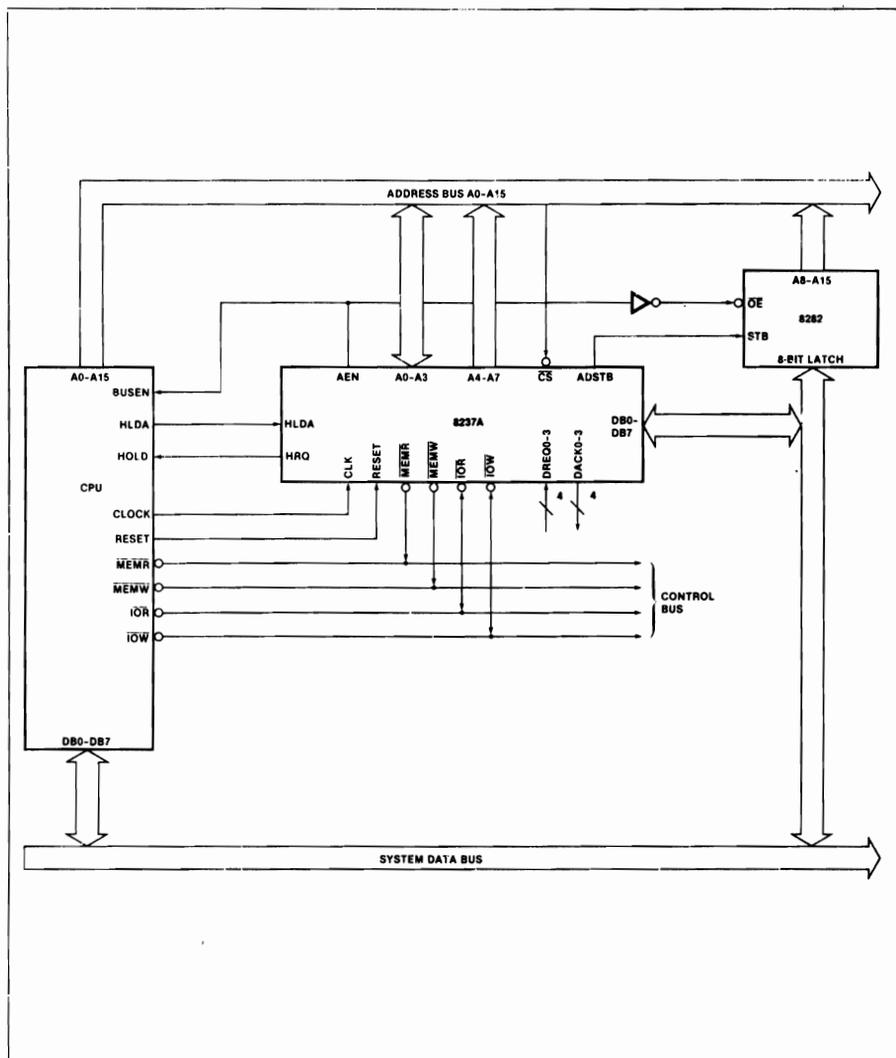


**Figure 8. 8237A System Interface**

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# UM8250A/B Asynchronous Communication Element (ACE)

## FEATURES:

- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to $(2^{16} - 1)$ and Generates the Internal 16X Clock
- Independent Receiver Clock Input
- Modem Control Functions (CTS, RTS, DSR, DTR, RI, and Carrier Detect)
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Single +5 Volt Power Supply
- Fully Programmable Serial Interface Characteristics
  - 5, 6, 7, or 8-bit Characters
  - Even, Odd, or No-parity Bit Generation and Detection
  - 1, 1½, or 2 Stops Bit Generation
  - Baud Rate Generation (DC to 56K Baud)
- INS 8250A Spec. Compatible
- False Start Bit Detection
- Complete Status Reporting Capabilities
- Easily Interfaces with Most Popular Microprocessors
- Line-Break Generation and Detection
- Fully Prioritized Interrupt System Controls.

## PIN CONFIGURATION

UM8250A

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 1 | D0 | | 40 | VDD |
| 2 | D1 | | 39 | RI |
| 3 | D2 | | 38 | RLSD |
| 4 | D3 | | 37 | DSR |
| 5 | D4 | | 36 | CTS |
| 6 | D5 | | 35 | MR |
| 7 | D6 | | 34 | OUT1 |
| 8 | D7 | | 33 | DTR |
| 9 | RCLK | | 32 | RTS |
| 10 | SIN | | 31 | OUT2 |
| 11 | SOUT | | 30 | INTRPT |
| 12 | CS0 | | 29 | NC |
| 13 | CS1 | | 28 | A0 |
| 14 | CS2 | | 27 | A1 |
| 15 | BAUDOUT | | 26 | A2 |
| 16 | XTAL 1 | | 25 | ADS |
| 17 | XTAL 2 | | 24 | CSOUT |
| 18 | DOSTR | | 23 | DDIS |
| 19 | DOSTR | | 22 | DISTR |
| 20 | VSS | | 21 | DISTR |

UM8250B

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 1 | D0 | | 40 | VDD |
| 2 | D1 | | 39 | RI |
| 3 | D2 | | 38 | RLSD |
| 4 | D3 | | 37 | DSR |
| 5 | D4 | | 36 | CTS |
| 6 | D5 | | 35 | MR |
| 7 | D6 | | 34 | OUT1 |
| 8 | D7 | | 33 | DTR |
| 9 | RCLK | | 32 | RTS |
| 10 | SIN | | 31 | OUT2 |
| 11 | SOUT | | 30 | INTRPT |
| 12 | CS0 | | 29 | NC |
| 13 | CS1 | | 28 | A0 |
| 14 | CS2 | | 27 | A1 |
| 15 | BAUDOUT | | 26 | A2 |
| 16 | XTAL1 | | 25 | ADS |
| 17 | XTAL2 | | 24 | CSOUT |
| 18 | DOSTR | | 23 | DDIS |
| 19 | DOSTR | | 22 | DISTR |
| 20 | VSS | | 21 | DISTR |

# 8251A
# PROGRAMMABLE COMMUNICATION INTERFACE

- Synchronous and Asynchronous Operation
- Synchronous 5–8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion
- Asynchronous 5–8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling
- Synchronous Baud Rate—DC to 64K Baud

- Asynchronous Baud Rate—DC to 19.2K Baud
- Full-Duplex, Double-Buffered Transmitter and Receiver
- Error Detection—Parity, Overrun and Framing
- Compatible with an Extended Range of Intel Microprocessors
- 28-Pin DIP Package
- All Inputs and Outputs are TTL Compatible
- Available in EXPRESS
  —Standard Temperature Range
  —Extended Temperature Range

The Intel® 8251A is the enhanced version of the industry standard, Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's microprocessor families such as MCS-68, 80, 85, and iAPX-86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using N-channel silicon gate technology.
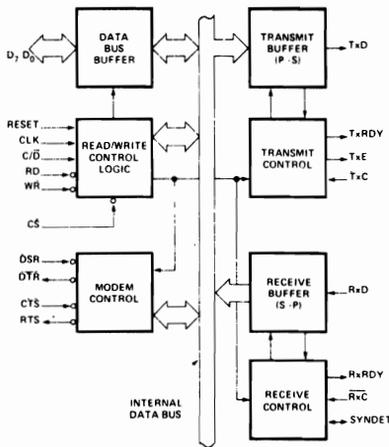


Figure 1. Block Diagram
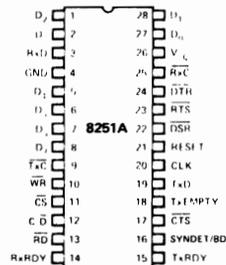


Figure 2. Pin Configuration

## FEATURES AND ENHANCEMENTS

The 8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.

- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.

- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.

- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.

- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.

- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.

- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.

- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.

- The 8251A Status can be read at any time but the status update will be inhibited during status read.

- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.

- Synchronous Baud rate from DC to 64K.

## FUNCTIONAL DESCRIPTION

### General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed for a wide range of Intel microcomputers such as 8048, 8080, 8085, 8086 and 8088. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support most serial data techniques in use, including IBM "bi-sync."

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

### Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-In and Data-Out registers are separate, 8-bit registers communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

### RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 $t_{CY}$ (clock must be running).

A command reset operation also puts the device into the "Idle" state.

## CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

## $\overline{WR}$ (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

## $\overline{RD}$ (Read)

A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.



**Figure 3. 8251A Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions**

| C/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 8251A DATA → DATA BUS |
| 0 | 1 | 0 | 0 | DATA BUS → 8251A DATA |
| 1 | 0 | 1 | 0 | STATUS → DATA BUS |
| 1 | 1 | 0 | 0 | DATA BUS → CONTROL |
| x | 1 | 1 | 0 | DATA BUS → 3-STATE |
| x | x | x | 1 | DATA BUS → 3-STATE |

## C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.

1 = CONTROL/STATUS; 0 = DATA.

## $\overline{CS}$ (Chip Select)

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus is in the float state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.

## Modem Control

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

## $\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test modem conditions such as Data Set Ready.

## $\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as Data Terminal Ready.

## $\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as Request to Send.

## $\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down.

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## Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable or $\overline{CTS}$ is off or the transmitter is empty.

## Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

## TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data Input Register.

## TxE (Transmitter Empty)

When the 8251A has no characters to send, the TxEMPTY output will go "high." It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplex operational mode.

In the Synchronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers." TxEMPTY does not go low when the SYNC characters are being shifted out.
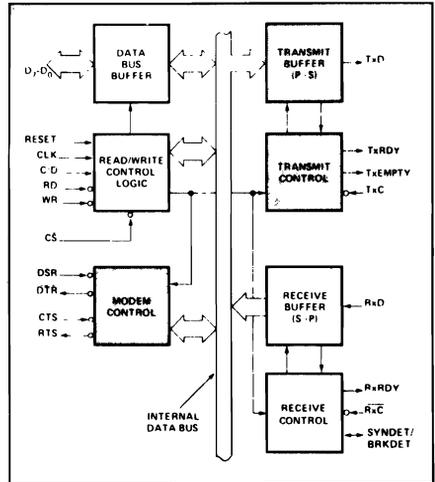


**Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions**

## $\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:

  If Baud Rate equals 110 Baud,
  $\overline{TxC}$ equals 110 Hz in the 1x mode.
  $\overline{TxC}$ equals 1.72 kHz in the 16x mode.
  $\overline{TxC}$ equals 7.04 kHz in the 64x mode.

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251A.

## Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of $\overline{RxC}$.

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## Receiver Control

This functional block manages all receiver-related activities which consists of the following features.

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition." Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

Parity error detection sets the corresponding status bit.

The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

## RxRDY (Receiver Ready)

This output indicates that the 8251A contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

RxEnable, when off, holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

## RxC (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of RxC. In Asynchronous Mode, the Baud Rate is a fraction of the actual RxC frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 the RxC.

For example:

Baud Rate equals 300 Baud, if
RxC equals 300 Hz in the 1x mode;
RxC equals 4800 Hz in the 16x mode;
RxC equals 19.2 kHz in the 64x mode.

Baud Rate equals 2400 Baud, if
RxC equals 2400 Hz in the 1x mode;
RxC equals 38.4 kHz in the 16x mode;
RxC equals 153.6 kHz in the 64x mode.

Data is sampled into the 8251A on the rising edge of RxC.

**NOTE:** In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both TxC and RxC will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.
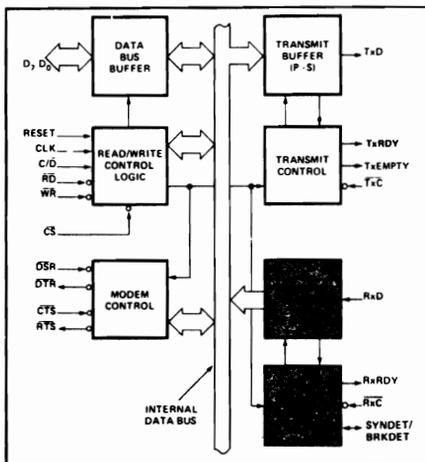


**Figure 5. 8251A Block Diagram Showing Receiver Buffer and Control Functions**

## SYNDET (SYNC Detect/ BRKDET Break Detect)

This pin is used in Synchronous Mode for SYN-DET and may be used as either input or output, programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251A to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. When External SYNC Detect is pro-grammed, Internal SYNC Detect is disabled.

## BREAK (Async Mode Only)

This output will go high whenever the receiver remains low through two consecutive stop bit se-quences (including the start bits, data bits, and parity bits). Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.
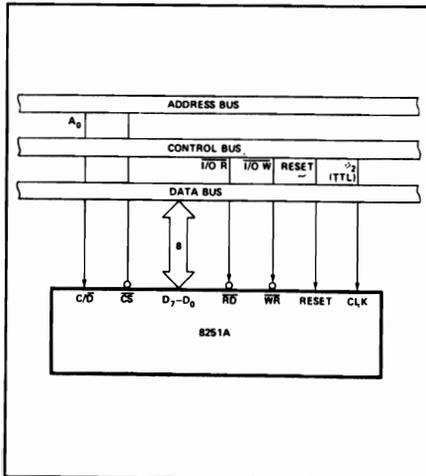


**Figure 6. 8251A Interface to 8080 Standard System Bus**

## DETAILED OPERATION DESCRIPTION

### General

The complete functional definition of the 8251A is programmed by the system's software. A set of con-trol words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPER-ATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251A. On the other hand, the 8251A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The 8251A cannot begin transmission until the Tx Enable (Transmitter Enable) bit is set in the Com-mand Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the mark-ing state upon Reset.
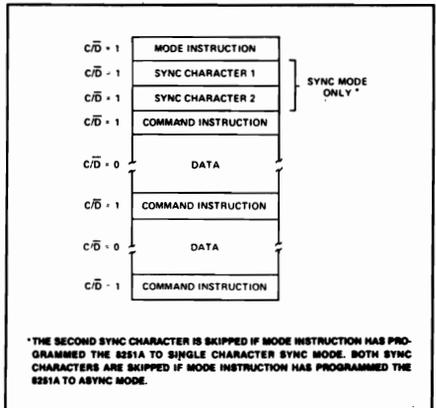


**Figure 7. Typical Data Block**

## Programming the 8251A

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

## Mode Instruction

This instruction defines the general operational characteristics of the 8251A. It must follow a Reset operation (internal or external). Once the Mode Instruction has been written into the 8251A by the CPU, SYNC characters or Command Instructions may be written.

## Command Instruction

This instruction defines a word that is used to control the actual operation of the 8251A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation (see Figure 7). The Mode Instruction must be written immediately following a Reset operation, prior to using the 8251A for data communication.

All control words written into the 8251A after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251A at any time in the data block during the operation of the 8251A. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251A back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

## Mode Instruction Definition

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components, one Asynchronous and the other Synchronous, sharing the same package. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

**NOTE:** When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

## Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A the TxD output reamins "high" (marking) unless a Break (continuously low) has been programmed.
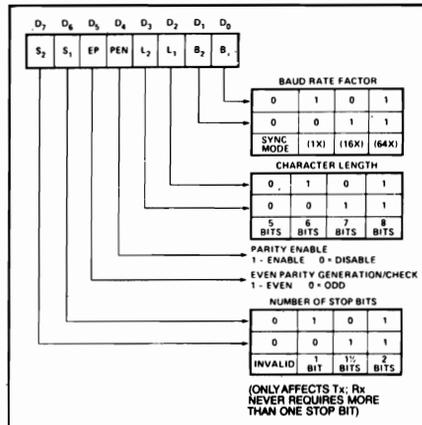


**Figure 8. Mode Instruction Format,
Asynchronous Mode**

## Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16X or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the *receiver* requires only *one* stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the 8251A.
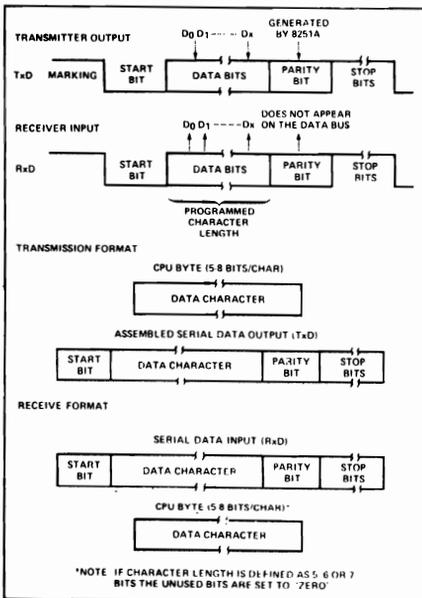


**Figure 9. Asynchronous Mode**

## Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251A which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251A with a data character before the 8251A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the 8251A.
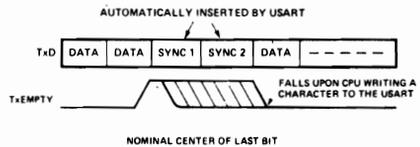


## Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the 8251A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the 8251A out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in Hunt, regardless of whether the Receiver is enabled or not.
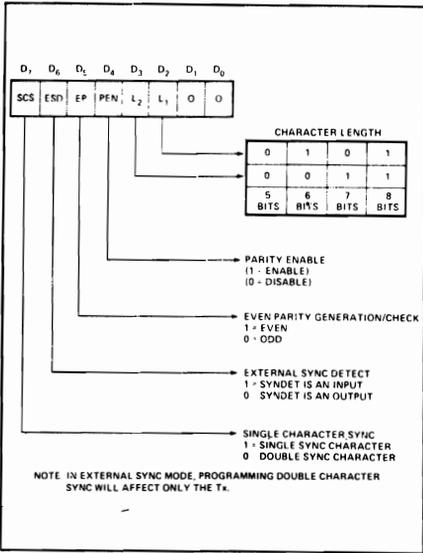


**Figure 10. Mode Instruction Format, Synchronous Mode**

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one," thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. Note that the SYNDET F/F is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the 8251A to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary.
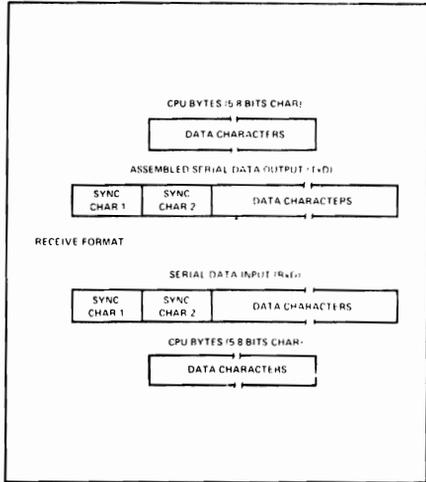


**Figure 11. Data Format, Synchronous Mode**

## COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the sync characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" (C/D = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.

**Note:** Internal Reset on Power-up

When power is first applied, the 8251A may come up in the Mode, Sync character or Command format. To guarantee that the device is in the Command Instruction format before the Reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with C/D̄ = 1 configures sync operation and writes two dummy 00H sync characters. An Internal Reset command (40H) may then be issued to return the device to the "Idle" state.

**Note:** Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.
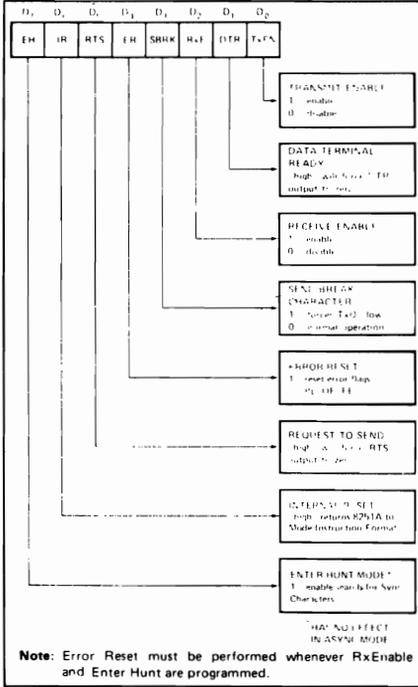
**Figure 12. Command Instruction Format**

## STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (Status update is inhibited during status read.)

A normal "read" command is issued by the CPU with $C/\overline{D} = 1$ to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.



Note 1   TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN, the latter is conditioned by both $\overline{CTS}$ and TxEN.
i.e. TxRDY status bit    DB Buffer Empty
TxRDY pin out    DB Buffer Empty · ($\overline{CTS}$ 0)·(TxEN 1)
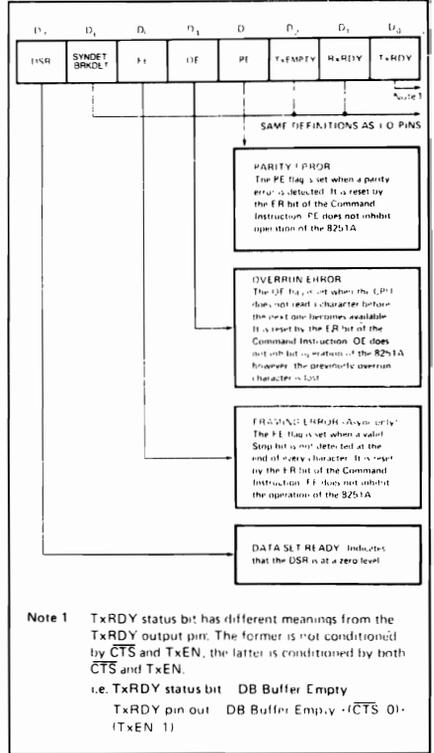
**Figure 13. Status Read Format**

## APPLICATIONS OF THE 8251A
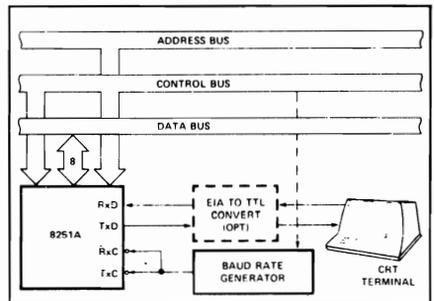


**Figure 14. Asynchronous Serial Interface to CRT Terminal, DC—9600 Baud**

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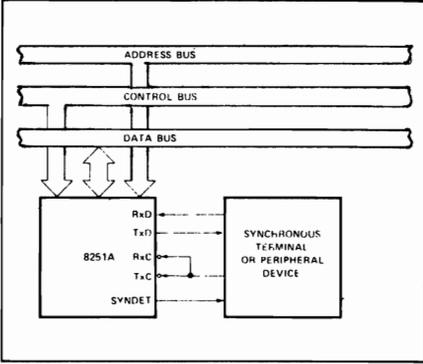
Figure 15. Synchronous Interface to Terminal or Peripheral Device



Figure 16. Asynchronous Interface to Telephone Lines



Figure 17. Synchronous Interface to Telephone Lines

# 8253/8253-5
# PROGRAMMABLE INTERVAL TIMER

- ■ **MCS-85™ Compatible 8253-5**
- ■ **3 Independent 16-Bit Counters**
- ■ **DC to 2.6 MHz**
- ■ **Programmable Counter Modes**

- ■ **Count Binary or BCD**
- ■ **Single +5V Supply**
- ■ **Available in EXPRESS**
  - **— Standard Temperature Range**
  - **— Extended Temperature Range**

The Intel® 8253 is a programmable counter/timer device designed for use as an Intel microcomputer peripheral. It uses NMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2.6 MHz. All modes of operation are software programmable.
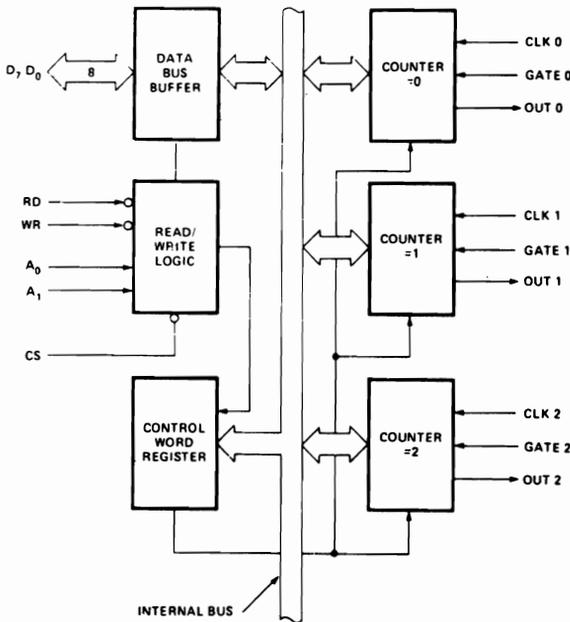


231306-1

**Figure 1. Block Diagram**



231306-2
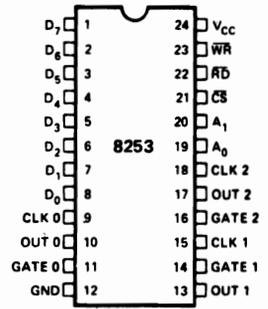
**Figure 2. Pin Configuration**

# 8254
# PROGRAMMABLE INTERVAL TIMER

- Compatible with All Intel and Most Other Microprocessors
- Handles Inputs from DC to 10 MHz
  - 5 MHz 8254-5
  - 8 MHz 8254
  - 10 MHz 8254-2
- Status Read-Back Command

- Six Programmable Counter Modes
- Three Independent 16-Bit Counters
- Binary or BCD Counting
- Single +5V Supply
- Available in EXPRESS
  - Standard Temperature Range

The Intel® 8254 is a counter/timer device designed to solve the common timing control problems in micro-computer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 is a superset of the 8253.

The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.
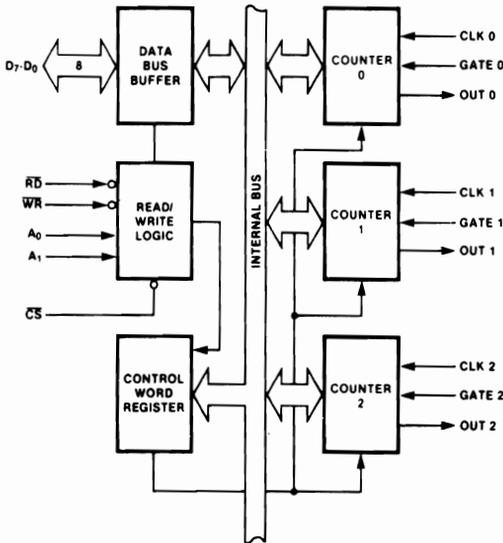


Figure 1. 8254 Block Diagram

231164-1
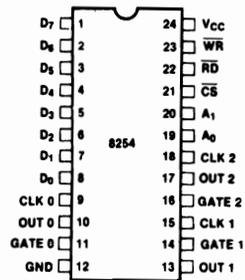


231164-2

Figure 2. Pin Configuration

# 8255A/8255A-5
# PROGRAMMABLE PERIPHERAL INTERFACE

- ■ **MCS-85™ Compatible 8255A-5**
- ■ **24 Programmable I/O Pins**
- ■ **Completely TTL Compatible**
- ■ **Fully Compatible with Intel Microprocessor Families**
- ■ **Improved Timing Characteristics**

- ■ **Direct Bit Set/Reset Capability Easing Control Application Interface**
- ■ **Reduces System Package Count**
- ■ **Improved DC Driving Capability**
- ■ **Available in EXPRESS**
  — **Standard Temperature Range**
  — **Extended Temperature Range**
- ■ **40 Pin DIP Package or 44 Lead PLCC**
  (See Intel Packaging Order Number: 231369)

The Intel 8255A is a general purpose programmable I/O device designed for use with Intel microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.
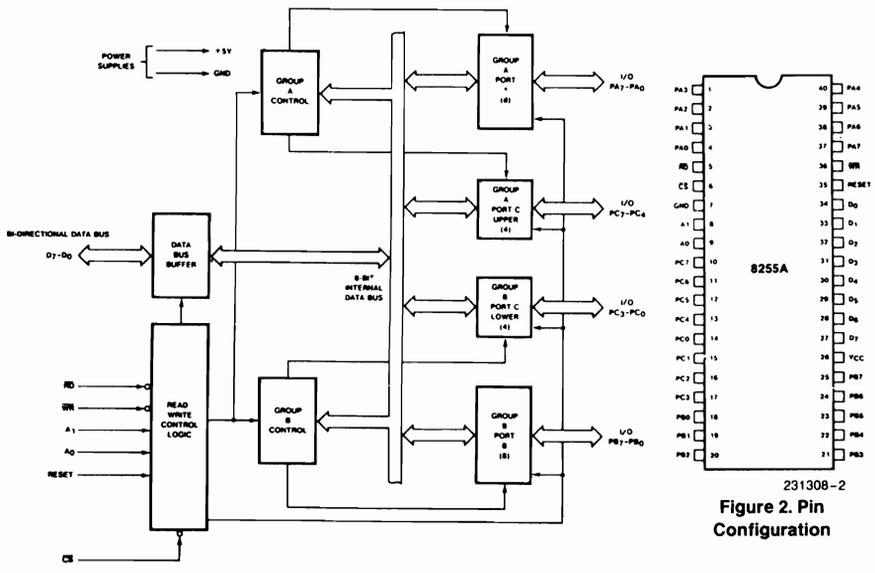


Figure 1. 8255A Block Diagram

231308–1



231308–2

**Figure 2. Pin Configuration**

## 8255A FUNCTIONAL DESCRIPTION

### General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

### Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

### Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the

CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

### (CS)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

### (RD)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

### (WR)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

### ($A_0$ and $A_1$)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus ($A_0$ and $A_1$).



231308-3
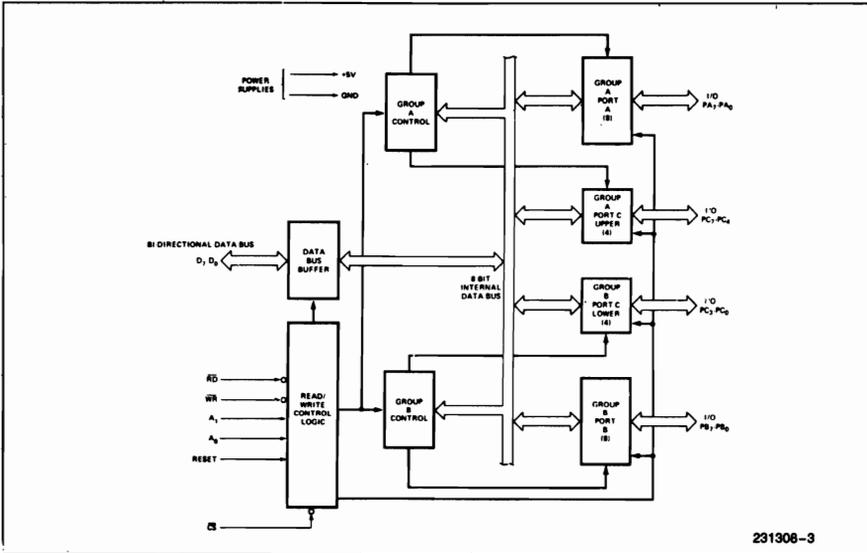
**Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions**

## 8255A BASIC OPERATION

| A₁ | A₀ | RD | WR | CS | Input Operation (READ) |
|----|----|----|----|----|------------------------|
| 0 | 0 | 0 | 1 | 0 | Port A → Data Bus |
| 0 | 1 | 0 | 1 | 0 | Port B → Data Bus |
| 1 | 0 | 0 | 1 | 0 | Port C → Data Bus |
| | | | | | **Output Operation (WRITE)** |
| 0 | 0 | 1 | 0 | 0 | Data Bus → Port A |
| 0 | 1 | 1 | 0 | 0 | Data Bus → Port B |
| 1 | 0 | 1 | 0 | 0 | Data Bus → Port C |
| 1 | 1 | 1 | 0 | 0 | Data Bus → Control |
| | | | | | **Disable Function** |
| X | X | X | X | 1 | Data Bus → 3-State |
| 1 | 1 | 0 | 1 | 0 | Illegal Condition |
| X | X | 1 | 1 | 0 | Data Bus → 3-State |

## (RESET)

**Reset.** A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

## Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A—Port A and Port C upper (C7–C4)
Control Group B—Port B and Port C lower (C3–C0)

The Control Word Register can **Only** be written into. No Read operation of the Control Word Register is allowed.

## Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

**Port A.** One 8-bit data output latch/buffer and one 8-bit data input latch.

**Port B.** One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

**Port C.** One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
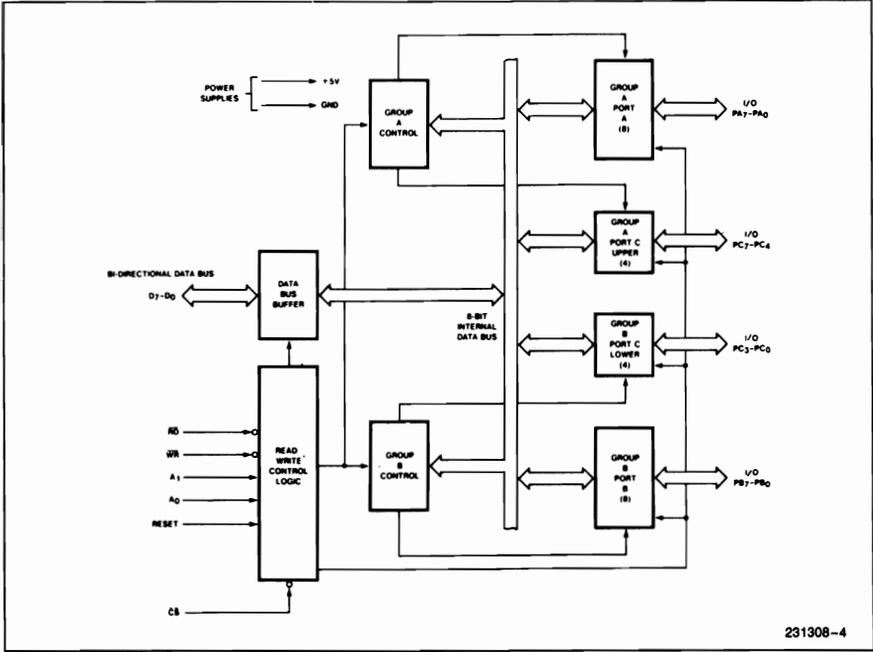
Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions

## Pin Configuration



231306-5
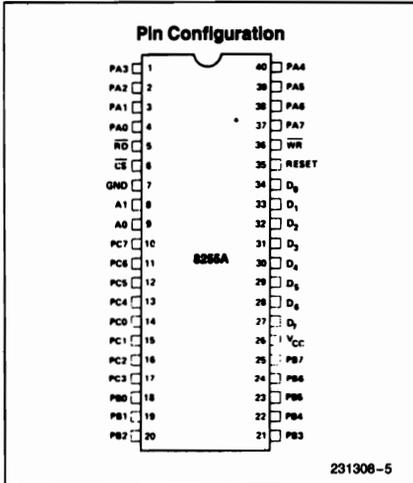
### Pin Names

| | |
|---|---|
| $D_7-D_0$ | Data Bus (Bi-Directional) |
| RESET | Reset Input |
| $\overline{CS}$ | Chip Select |
| $\overline{RD}$ | Read Input |
| $\overline{WR}$ | Write Input |
| A0, A1 | Port Address |
| PA7–PA0 | Port A (BIT) |
| PB7–PB0 | Port B (BIT) |
| PC7–PC0 | Port C (BIT) |
| $V_{CC}$ | +5 Volts |
| GND | 0 Volts |

## 8255A OPERATIONAL DESCRIPTION

### Mode Selection

There are three basic modes of operation that can be selected by the system software:

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Mode 0—Basic Input/Output

Mode 1—Strobed Input/Output

Mode 2—Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.
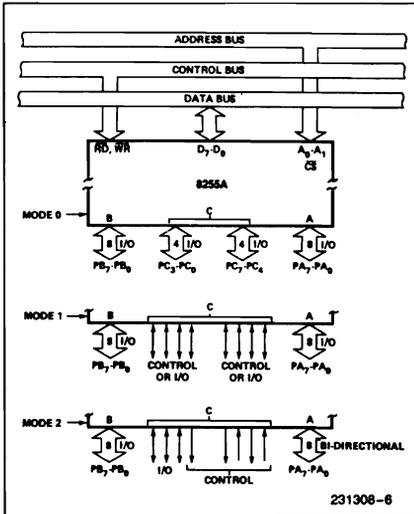


**Figure 5. Basic Mode Definitions and Bus Interface**
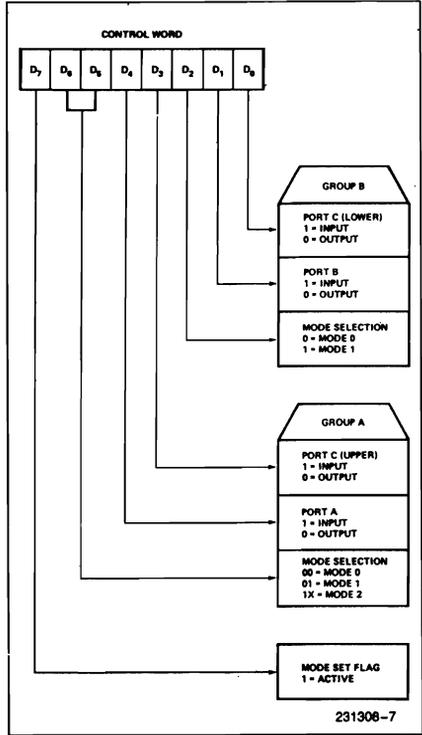


**Figure 6. Mode Definition Format**

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

## Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.
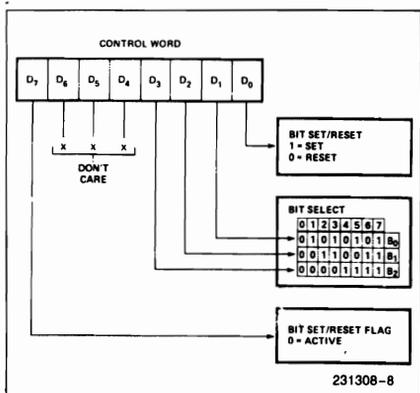
**Figure 7. Bit Set/Reset Format**

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

## Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is set—Interrupt enable

(BIT-RESET)—INTE is RESET—Interrupt disable

**NOTE:**
All Mask flip-flops are automatically reset during mode selection and device Reset.

## Operating Modes

**MODE 0 (Basic Input/Output).** This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

• Two 8-bit ports and two 4-bit ports.
• Any port can be input or output.
• Outputs are latched.
• Inputs are not latched.
• 16 different Input/Output configurations are possible in this Mode.

**MODE 0 (BASIC INPUT)**

## MODE 0 (BASIC OUTPUT)

$\overline{\text{WR}}$

$t_{WW}$

$D_7\text{-}D_0$

$t_{DW}$   $t_{WD}$

$\overline{\text{CS}}$, A1, A0

$t_{AW}$   $t_{WA}$

OUTPUT

$t_{WB}$

231308-10
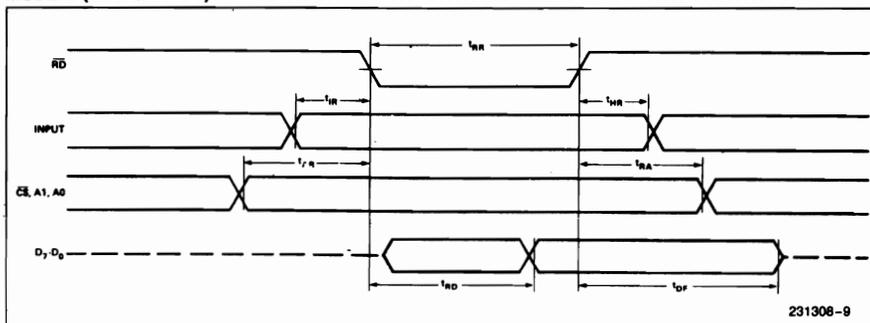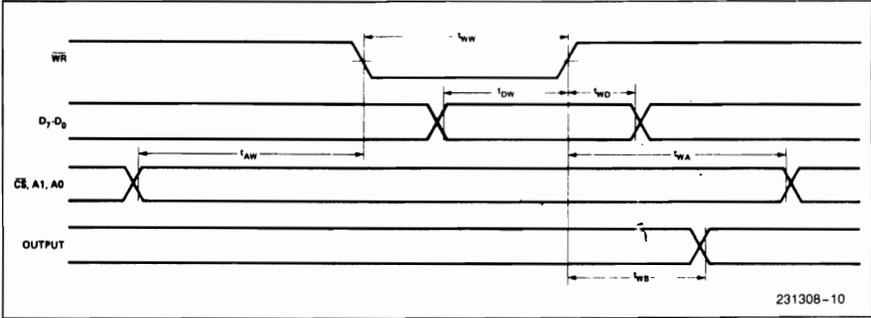
## MODE 0 PORT DEFINITION

| A | | B | | Group A | | | Group B | |
|---|---|---|---|---|---|---|---|---|
| $D_4$ | $D_3$ | $D_1$ | $D_0$ | Port A | Port C (Upper) | # | Port B | Port C (Lower) |
| 0 | 0 | 0 | 0 | OUTPUT | OUTPUT | 0 | OUTPUT | OUTPUT |
| 0 | 0 | 0 | 1 | OUTPUT | OUTPUT | 1 | OUTPUT | INPUT |
| 0 | 0 | 1 | 0 | OUTPUT | OUTPUT | 2 | INPUT | OUTPUT |
| 0 | 0 | 1 | 1 | OUTPUT | OUTPUT | 3 | INPUT | INPUT |
| 0 | 1 | 0 | 0 | OUTPUT | INPUT | 4 | OUTPUT | OUTPUT |
| 0 | 1 | 0 | 1 | OUTPUT | INPUT | 5 | OUTPUT | INPUT |
| 0 | 1 | 1 | 0 | OUTPUT | INPUT | 6 | INPUT | OUTPUT |
| 0 | 1 | 1 | 1 | OUTPUT | INPUT | 7 | INPUT | INPUT |
| 1 | 0 | 0 | 0 | INPUT | OUTPUT | 8 | OUTPUT | OUTPUT |
| 1 | 0 | 0 | 1 | INPUT | OUTPUT | 9 | OUTPUT | INPUT |
| 1 | 0 | 1 | 0 | INPUT | OUTPUT | 10 | INPUT | OUTPUT |
| 1 | 0 | 1 | 1 | INPUT | OUTPUT | 11 | INPUT | INPUT |
| 1 | 1 | 0 | 0 | INPUT | INPUT | 12 | OUTPUT | OUTPUT |
| 1 | 1 | 0 | 1 | INPUT | INPUT | 13 | OUTPUT | INPUT |
| 1 | 1 | 1 | 0 | INPUT | INPUT | 14 | INPUT | OUTPUT |
| 1 | 1 | 1 | 1 | INPUT | INPUT | 15 | INPUT | INPUT |

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## MODE CONFIGURATIONS

CONTROL WORD #0

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

8255A

$D_7$-$D_0$

A — 8 → $PA_7$-$PA_0$

C — 4 → $PC_7$-$PC_4$

— 4 → $PC_3$-$PC_0$

B — 8 → $PB_7$-$PB_0$

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CONTROL WORD #2

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

8255A

$D_7$-$D_0$

A — 8 → $PA_7$-$PA_0$

C — 4 → $PC_7$-$PC_4$

— 4 → $PC_3$-$PC_0$

B — 8 ← $PB_7$-$PB_0$

231308–12

CONTROL WORD #1

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

8255A

$D_7$-$D_0$

A — 8 → $PA_7$-$PA_0$

C — 4 → $PC_7$-$PC_4$

— 4 → $PC_3$-$PC_0$

B — 8 → $PB_7$-$PB_0$

231308–13

CONTROL WORD #3

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

8255A

$D_7$-$D_0$

A — 8 → $PA_7$-$PA_0$

C — 4 → $PC_7$-$PC_4$

— 4 → $PC_3$-$PC_0$

B — 8 ← $PB_7$-$PB_0$

231308–14

CONTROL WORD #4

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

8255A

$D_7$-$D_0$

A — 8 → $PA_7$-$PA_0$

C — 4 → $PC_7$-$PC_4$

— 4 → $PC_3$-$PC_0$

B — 8 → $PB_7$-$PB_0$

231308–15

CONTROL WORD #6

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

8255A

$D_7$-$D_0$

A — 8 ← $PA_7$-$PA_0$

C — 4 → $PC_7$-$PC_4$

— 4 → $PC_3$-$PC_0$

B — 8 → $PB_7$-$PB_0$

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CONTROL WORD #8

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

8255A
A → 8 → $PA_7$-$PA_0$
C → 4 → $PC_7$-$PC_4$
C → 4 → $PC_3$-$PC_0$
B → 8 → $PB_7$-$PB_0$
$D_7$-$D_0$

231308-17

CONTROL WORD #9

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

8255A
A ← 8 ← $PA_7$-$PA_0$
C → 4 → $PC_7$-$PC_4$
C → 4 → $PC_3$-$PC_0$
B → 8 → $PB_7$-$PB_0$
$D_7$-$D_0$

231308-18

CONTROL WORD #6

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

8255A
A → 8 → $PA_7$-$PA_0$
C → 4 → $PC_7$-$PC_4$
C → 4 → $PC_3$-$PC_0$
B ← 8 ← $PB_7$-$PB_0$
$D_7$-$D_0$

231308-19

CONTROL WORD #10

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

8255A
A ← 8 ← $PA_7$-$PA_0$
C → 4 → $PC_7$-$PC_4$
C → 4 → $PC_3$-$PC_0$
B ← 8 ← $PB_7$-$PB_0$
$D_7$-$D_0$

231308-20

CONTROL WORD #7

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

8255A
A → 8 → $PA_7$-$PA_0$
C → 4 → $PC_7$-$PC_4$
C → 4 → $PC_3$-$PC_0$
B ← 8 ← $PB_7$-$PB_0$
$D_7$-$D_0$

231308-21

CONTROL WORD #11

| $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

8255A
A ← 8 ← $PA_7$-$PA_0$
C → 4 → $PC_7$-$PC_4$
C ← 4 ← $PC_3$-$PC_0$
B ← 8 ← $PB_7$-$PB_0$
$D_7$-$D_0$

231308-22

CONTROL WORD #12

| D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

231308-23

CONTROL WORD #14

| D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

231308-24

CONTROL WORD #13

| D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

231308-25

CONTROL WORD #15

| D₇ | D₆ | D₅ | D₄ | D₃ | D₂ | D₁ | D₀ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

231308-26

## Operating Modes

**MODE 1 (Strobed Input/Output).** This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

## Input Control Signal Definition

$\overline{\text{STB}}$ **(Strobe Input).** A "low" on this input loads data into the input latch.

### IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

### INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{\text{STB}}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{\text{RD}}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

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**INTE A**

Controlled by bit set/reset of $PC_4$.

**INTE B**

Controlled by bit set/reset of $PC_2$.
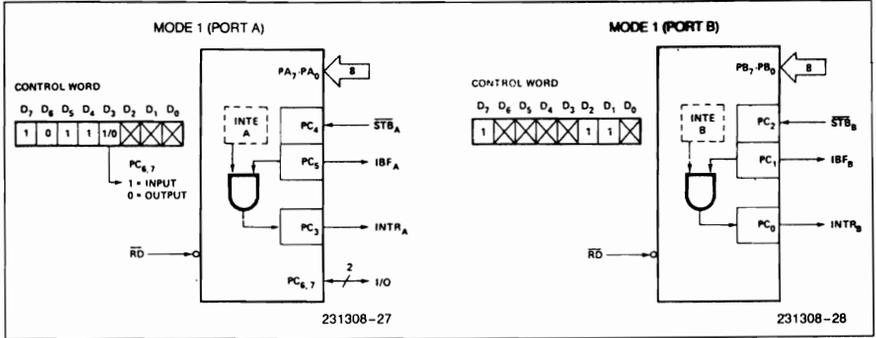


**Figure 8. MODE 1 Input**
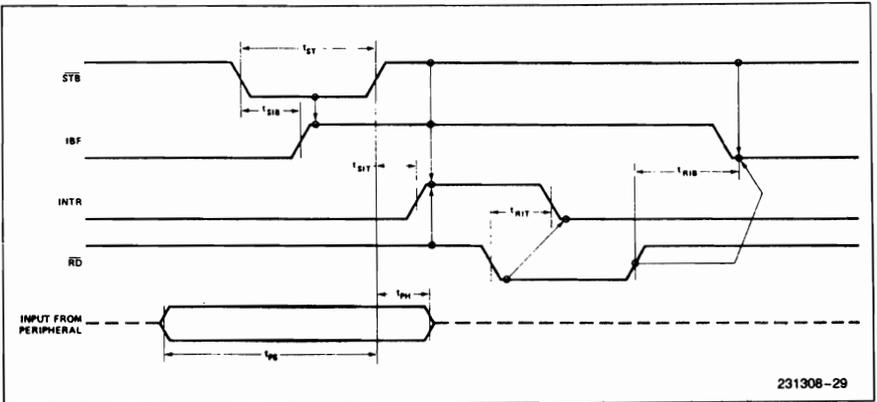


**Figure 9. MODE 1 (Strobed Input)**

## Output Control Signal Definition

$\overline{OBF}$ **(Output Buffer Full F/F).** The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ **(Acknowledge Input).** A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

**INTR (Interrupt Request).** A "high" on this output can be used to interrupt the CPU when an output

device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one", and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

### INTE A

Controlled by bit set/reset of $PC_6$.

### INTE B

Controlled by bit set/reset of $PC_2$.
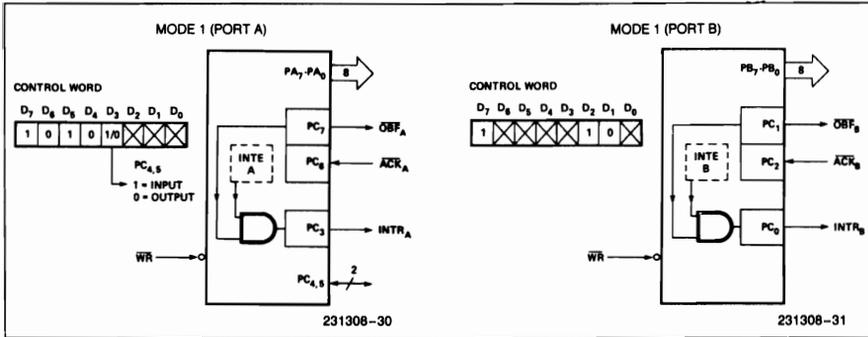


**Figure 10. MODE 1 Output**
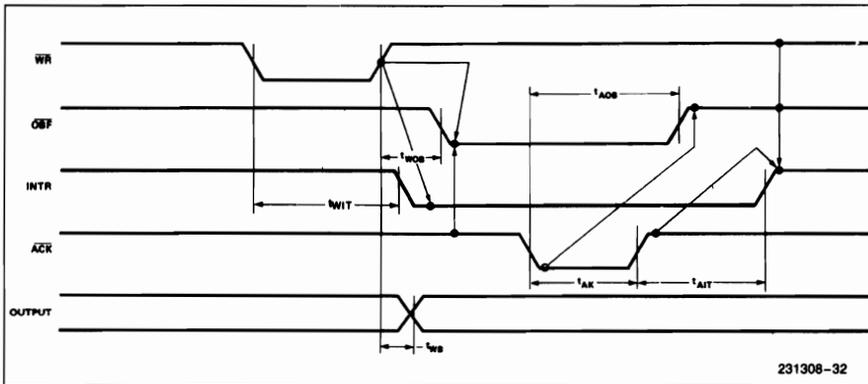


**Figure 11. MODE 1 (Strobed Output)**

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PORT A—(STROBED INPUT)
PORT B—(STROBED OUTPUT)
231308-33

PORT A—(STROBED OUTPUT)
PORT B—(STROBED INPUT)
231308-34
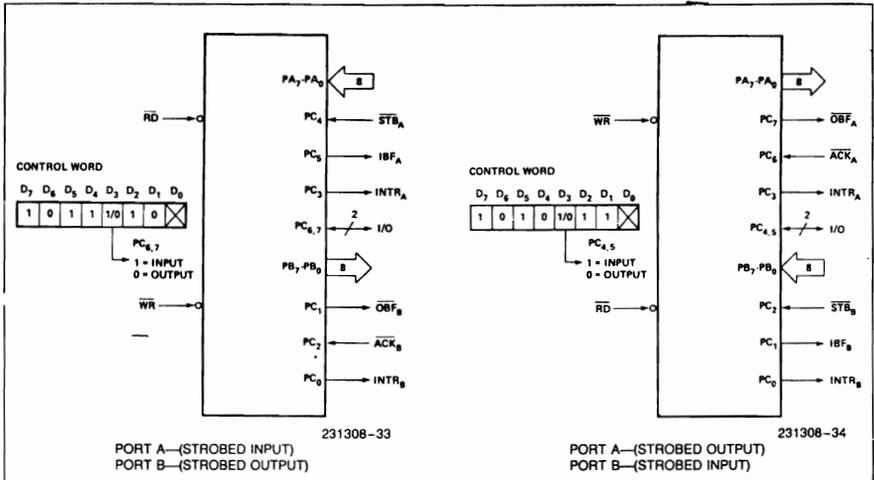
Figure 12. Combinations of MODE 1

## Combinations of MODE 1

Port A and Port B can be individually defined as input or output in MODE 1 to support a wide variety of strobed I/O applications.

## Operating Modes

**MODE 2 (Strobed Bidirectional Bus I/O).** This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A **only**.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

## Bidirectional Bus I/O Control Signal Definition

**INTR (Interrupt Request).** A high on this output can be used to interrupt the CPU for both input or output operations.

## Output Operations

**OBF (Output Buffer Full).** The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

**ACK (Acknowledge).** A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

**INTE 1 (The INTE Flip-Flop Associated with OBF).** Controlled by bit set/reset of $PC_6$.

## Input Operations

**STB (Strobe Input).** A "low" on this input loads data into the input latch.

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**IBF (Input Buffer Full F/F).** A "high" on this output indicates that data has been loaded into the input latch.

**INTE 2 (The INTE Flip-Flop Associated with IBF).** Controlled by bit set/reset of $PC_4$.
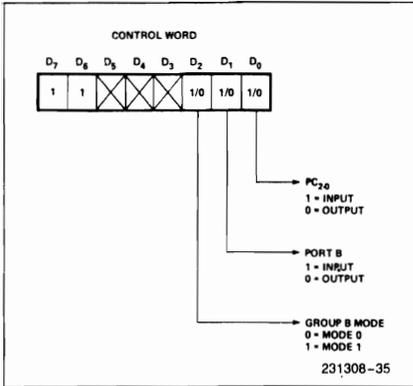


Figure 13. MODE Control Word



Figure 14. MODE 2
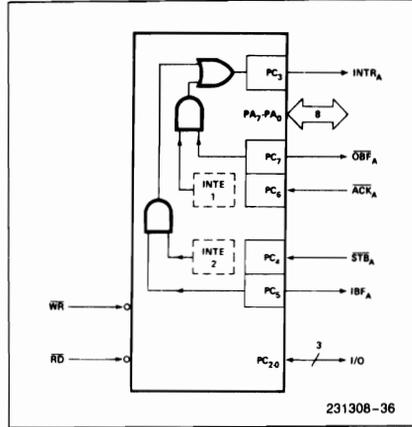


Figure 15. MODE 2 (Bidirectional)
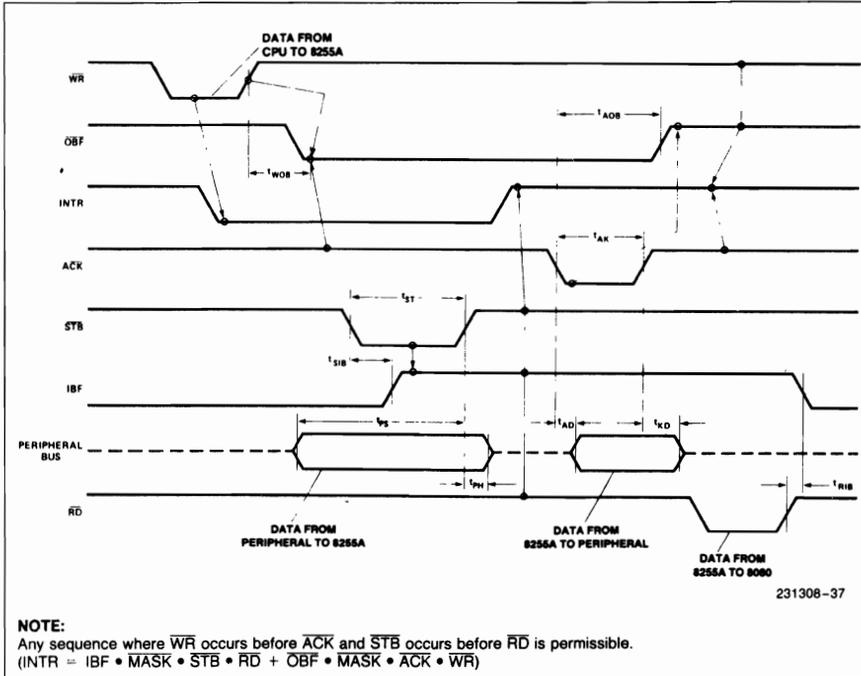
**NOTE:**
Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
$(INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR})$
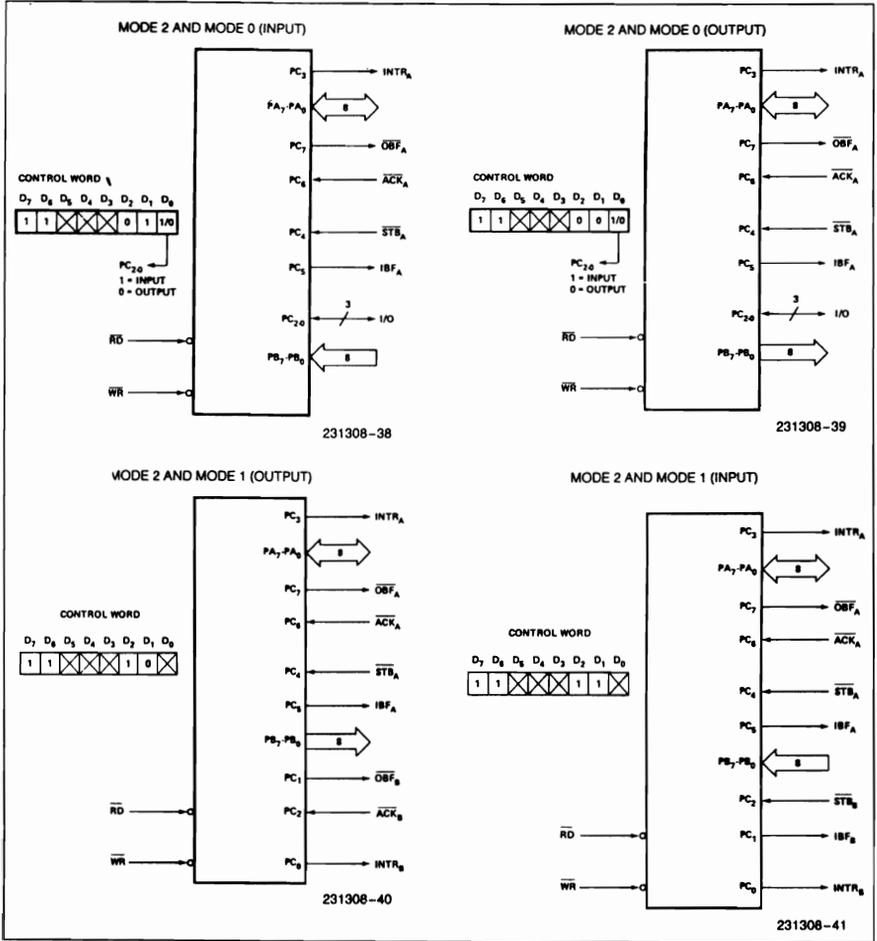
**Figure 16. MODE 1/4 Combinations**

## Mode Definition Summary

| | MODE 0 | | MODE 1 | | MODE 2 |
|---|---|---|---|---|---|
| | IN | OUT | IN | OUT | GROUP A ONLY |
| $PA_0$ | IN | OUT | IN | OUT | ←→ |
| $PA_1$ | IN | OUT | IN | OUT | ←→ |
| $PA_2$ | IN | OUT | IN | OUT | ←→ |
| $PA_3$ | IN | OUT | IN | OUT | ←→ |
| $PA_4$ | IN | OUT | IN | OUT | ←→ |
| $PA_5$ | IN | OUT | IN | OUT | ←→ |
| $PA_6$ | IN | OUT | IN | OUT | ←→ |
| $PA_7$ | IN | OUT | IN | OUT | ←→ |
| $PB_0$ | IN | OUT | IN | OUT | — |
| $PB_1$ | IN | OUT | IN | OUT | — |
| $PB_2$ | IN | OUT | IN | OUT | — |
| $PB_3$ | IN | OUT | IN | OUT | — |
| $PB_4$ | IN | OUT | IN | OUT | — |
| $PB_5$ | IN | OUT | IN | OUT | — |
| $PB_6$ | IN | OUT | IN | OUT | — |
| $PB_7$ | IN | OUT | IN | OUT | — |
| $PC_0$ | IN | OUT | $INTR_B$ | $INTR_B$ | I/O |
| $PC_1$ | IN | OUT | $IBF_B$ | $\overline{OBF}_B$ | I/O |
| $PC_2$ | IN | OUT | $\overline{STB}_B$ | $\overline{ACK}_B$ | I/O |
| $PC_3$ | IN | OUT | $INTR_A$ | $INTR_A$ | $INTR_A$ |
| $PC_4$ | IN | OUT | $\overline{STB}_A$ | I/O | $\overline{STB}_A$ |
| $PC_5$ | IN | OUT | $IBF_A$ | I/O | $IBF_A$ |
| $PC_6$ | IN | OUT | I/O | $\overline{ACK}_A$ | $\overline{ACK}_A$ |
| $PC_7$ | IN | OUT | I/O | $\overline{OBF}_A$ | $\overline{OBF}_A$ |

(PB rows in MODE 2: MODE 0 OR MODE 1 ONLY)

### Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs—

All input lines can be accessed during a normal Port C read.

If Programmed as Outputs—

Bits in C upper ($PC_7$–$PC_4$) must be individually accessed using the bit set/reset function.

Bits in C lower ($PC_3$–$PC_0$) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

### Source Current Capability on Port B and Port C

Any set of **eight** output buffers, selected randomly from Ports B and C can source 1 mA at 1.5 volts.

This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

### Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

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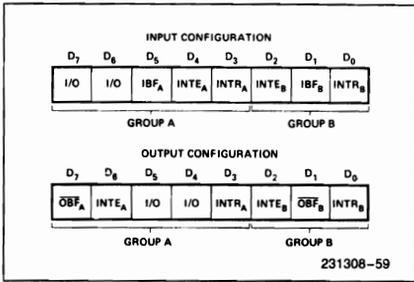
Figure 17. MODE 1 Status Word Format
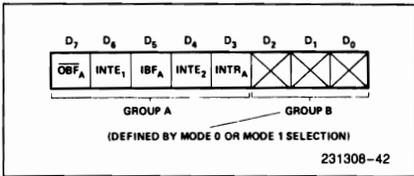


Figure 18. MODE 2 Status Word Format

## APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 represent a few examples of typical applications of the 8255A.
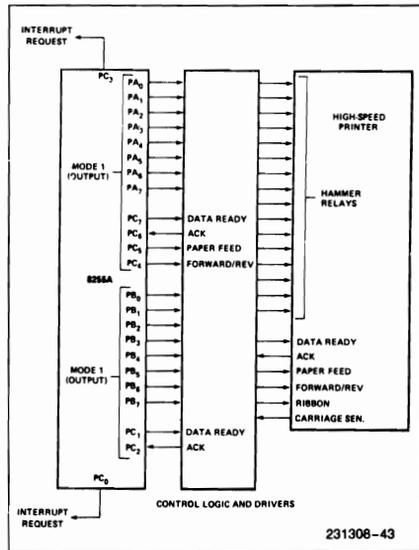


Figure 19. Printer Interface
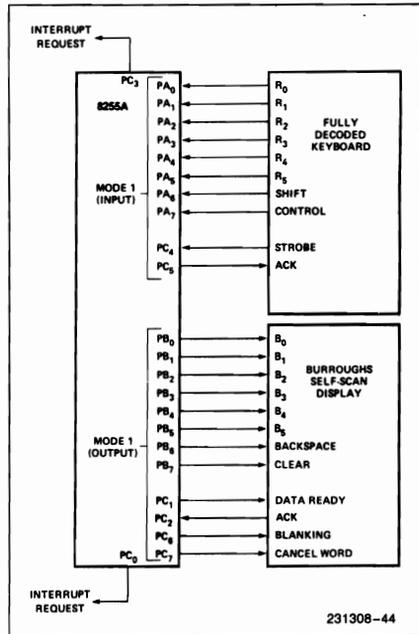


Figure 20. Keyboard and Display Interface

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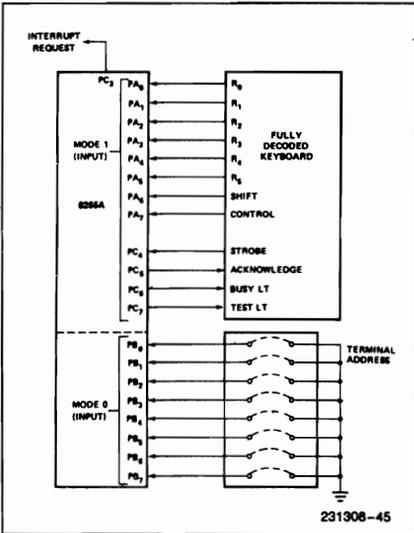
**Figure 21. Keyboard and Terminal Address Interface**

231306-45
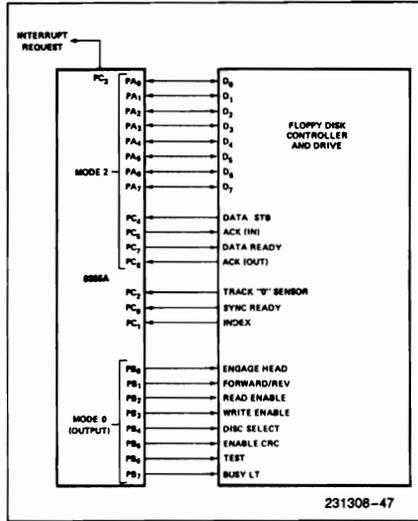


**Figure 23. Basic Floppy Disk Interface**

231306-47
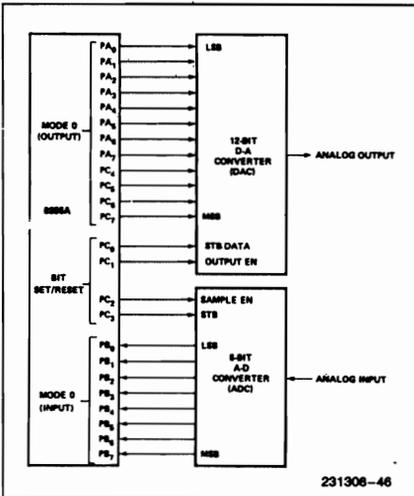


**Figure 22. Digital to Analog, Analog to Digital**

231306-46
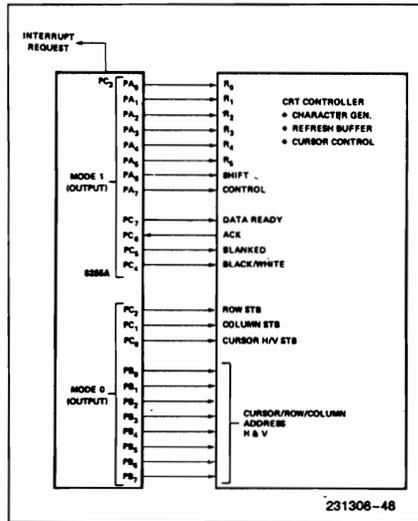


**Figure 24. Basic CRT Controller Interface**

231306-48

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# 8256AH
# MULTIFUNCTION MICROPROCESSOR
# SUPPORT CONTROLLER

- **Programmable Serial Asynchronous Communications Interface for 5-, 6-, 7-, or 8-Bit Characters, 1, 1½, or 2 Stop Bits, and Parity Generation**

- **On-Board Baud Rate Generator Programmable for 13 Common Baud Rates up to 19.2 KBits/Second, or an External Baud Clock Maximum of 1M Bit/Second**

- **Five 8-Bit Programmable Timer/ Counters; Four Can Be Cascaded to Two 16-Bit Timer/Counters**

- **Two 8-Bit Programmable Parallel I/O Ports; Port 1 Can Be Programmed for Port 2 Handshake Controls and Event Counter Inputs**

- **Eight-Level Priority Interrupt Controller Programmable for 8085 or iAPX 86, iAPX 88 Systems and for Fully Nested Interrupt Capability**

- **Programmable System Clock to 1 ×, 2 ×, 3 ×, or 5 × 1.024 MHz**

The Intel® 8256AH Multifunction Universal Asynchronous Receiver-Transmitter (MUART) combines five commonly used functions into a single 40-pin device. It is designed to interface to the 8086/88, iAPX 186/188, and 8051 to perform serial communications, parallel I/O, timing, event counting, and priority interrupt functions. All of these functions are fully programmable through nine internal registers. In addition, the five timer/counters and two parallel I/O ports can be accessed directly by the microprocessor.
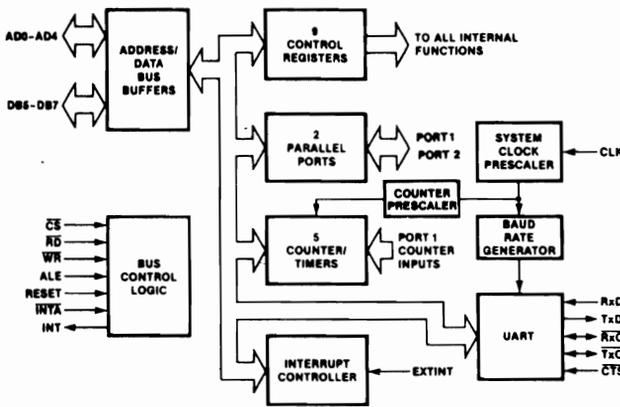


Figure 1. MUART Block Diagram

230759-1
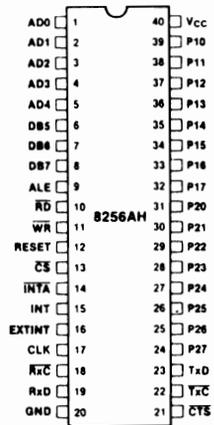


230759-2

Figure 2. MUART Pin Configuration

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# 8257/8257-5
# PROGRAMMABLE DMA CONTROLLER

- **MCS-85® Compatible 8257-5**
- **4-Channel DMA Controller**
- **Priority DMA Request Logic**
- **Channel Inhibit Logic**
- **Terminal Count and Modulo 128 Outputs**

- **Single TTL Clock**
- **Single +5V Supply**
- **Auto Load Mode**
- **Available in EXPRESS** **– Standard Temperature Range**

The Intel' 8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus in accomplished via the CPU's hold function. The 8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The 8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.
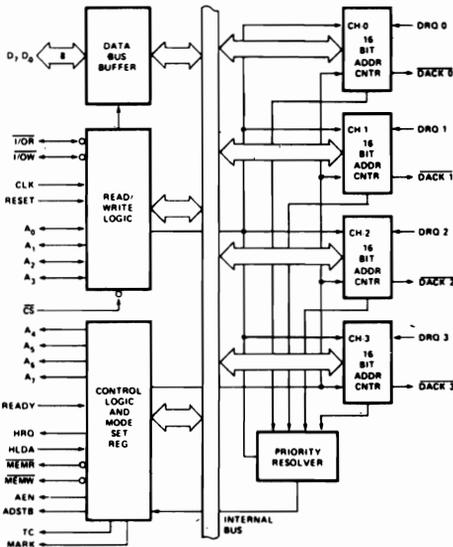


Figure 1. Block Diagram
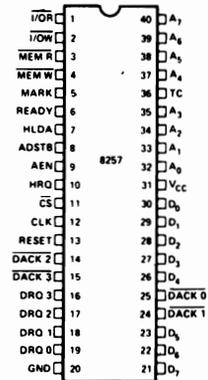
Figure 2. Pin Configuration

## FUNCTIONAL DESCRIPTION

### General

The 8257 is a programmable, Direct Memory Access (DMA) device which, when coupled with a single Intel* 8212 I/O port device, provides a complete four-channel DMA controller for use in Intel* microcomputer systems. After being initialized by software, the 8257 can transfer a block of data, containing up to 16,384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral, the 8257

1. Acquires control of the system bus.
2. Acknowledges that requesting peripheral which is connected to the highest priority channel
3. Outputs the least significant eight bits of the memory address onto system address lines $A_0$-$A_7$, outputs the most significant eight bits of the memory address to the 8212 I/O port via the data bus (the 8212 places these address bits on lines $A_8$-$A_{15}$), and
4. Generates the appropriate memory and I/O read/ write control signals that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

The 8257 will retain control of the system bus and repeat the transfer sequence, as long as a peripheral maintains its DMA request. Thus, the 8257 can transfer a block of data to/from a high speed peripheral (e.g., a sector of data on a floppy disk) in a single "burst" When the specified number of data bytes have been transferred, the 8257 activates its Terminal Count (TC) output, informing the CPU that the operation is complete.

The 8257 offers three different modes of operation: (1) DMA read, which causes data to be transferred from memory to a peripheral; (2) DMA write, which causes data to be transferred from a peripheral to memory, and (3) DMA verify, which does not actually involve the transfer of data When an 8257 channel is in the DMA verify mode, it will respond the same as described for transfer operations, except that no memory or I/O read/write control signals will be generated, thus preventing the transfer of data The 8257, however, will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) checkword. For example, a block of DMA verify cycles might follow a block of DMA read cycles (memory to peripheral) to allow the peripheral to verify its newly acquired data

### Block Diagram Description

#### 1. DMA Channels

The 8257 provides four separate DMA channels (labeled CH-0 to CH-3). Each channel includes two sixteen-bit registers (1) a DMA address register, and (2) a terminal count register Both registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) output is activated For instance, a terminal count of 0 would cause the TC output to be active in the first DMA cycle for that channel. In general, if N = the number of desired DMA cycles, load the value N-1 into the low-order 14-bits of the terminal count register The most significant two bits of the terminal count register specify the type of DMA operation for that channel
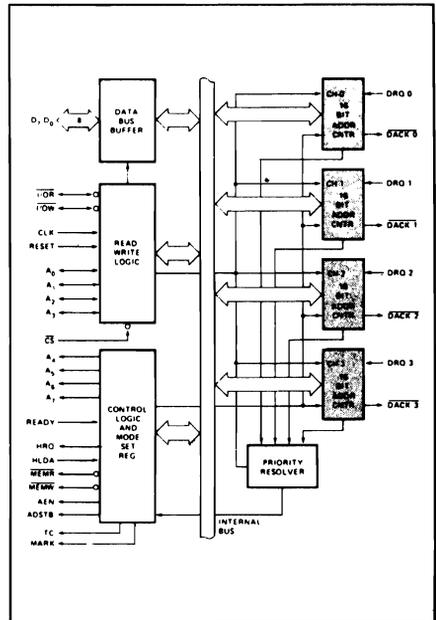


**Figure 3. 8257 Block Diagram Showing DMA Channels**

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These two bits are not modified during a DMA cycle, but can be changed between DMA blocks.

Each channel accepts a DMA Request (DRQn) input and provides a DMA Acknowledge (DACKn) output.

### (DRQ 0-DRQ 3)

DMA Request: These are individual asynchronous channel request inputs used by the peripherals to obtain a DMA cycle. If not in the rotating priority mode then DRQ 0 has the highest priority and DRQ 3 has the lowest. A request can be generated by raising the request line and holding it high until DMA acknowledge. For multiple DMA cycles (Burst Mode) the request line is held high until the DMA acknowledge of the last cycle arrives.

### (DACK 0 - DACK 3)

DMA Acknowledge: An active low level on the acknowledge output informs the peripheral connected to that channel that it has been selected for a DMA cycle. The DACK output acts as a "chip select" for the peripheral device requesting service. This line goes active (low) and inactive (high) once for each byte transferred even if a burst of data is being transferred.

### 2. Data Bus Buffer

This three-state, bi-directional, eight bit buffer interfaces the 8257 to the system data bus.

### (D₀-D₇)

Data Bus Lines: These are bi-directional three-state lines. When the 8257 is being programmed by the CPU, eight-bits of data for a DMA address register, a terminal count register or the Mode Set register are received on the data bus. When the CPU reads a DMA address register, a terminal count register or the Status register, the data is sent to the CPU over the data bus. During DMA cycles (when the 8257 is the bus master), the 8257 will output the most significant eight-bits of the memory address (from one of the DMA address registers) to the 8212 latch via the data bus. These address bits will be transferred at the beginning of the DMA cycle; the bus will then be released to handle the memory data transfer during the balance of the DMA cycle.

| BIT 15 | BIT 14 | TYPE OF DMA OPERATION |
|--------|--------|----------------------|
| 0 | 0 | Verify DMA Cycle |
| 0 | 1 | Write DMA Cycle |
| 1 | 0 | Read DMA Cycle |
| 1 | 1 | (Illegal) |
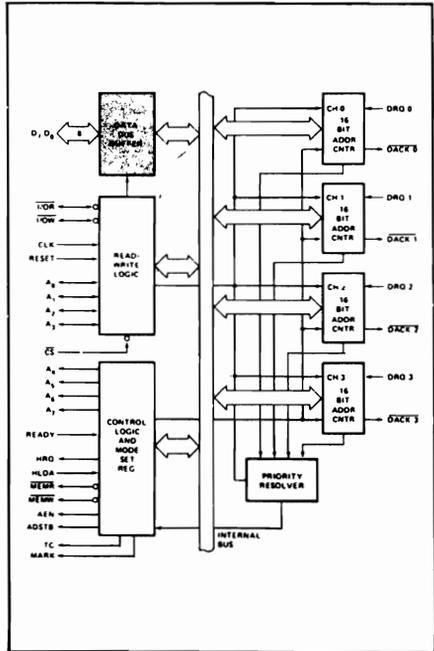


**Figure 4. 8257 Block Diagram Showing Data Bus Buffer**

## 3. Read/Write Logic

When the CPU is programming or reading one of the 8257's registers (i.e., when the 8257 is a "slave" device on the system bus), the Read/Write Logic accepts the I/O Read ($\overline{I/OR}$) or I/O Write ($\overline{I/OW}$) signal, decodes the least significant four address bits, ($A_0$-$A_3$), and either writes the contents of the data bus into the addressed register (if $\overline{I/OW}$ is true) or places the contents of the addressed register onto the data bus (if $\overline{I/OR}$ is true).

During DMA cycles (i.e., when the 8257 is the bus "master"), the Read/Write Logic generates the I/O read and memory write (DMA write cycle) or I/O Write and memory read (DMA read cycle) signals which control the data link with the peripheral that has been granted the DMA cycle.

Note that during DMA transfers Non-DMA I/O devices should be de-selected (disabled) using "AEN" signal to inhibit I/O device decoding of the memory address as an erroneous device address.

### ($\overline{I/OR}$)

I/O Read: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the 8-bit status register or the upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the "master" mode, $\overline{I/OR}$ is a control output which is used to access data from a peripheral during the DMA write cycle.

### ($\overline{I/OW}$)

I/O Write: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the contents of the data bus to be loaded into the 8-bit mode set register or the upper/lower byte of a 16-bit DMA address register or terminal count register. In the "master" mode, $\overline{I/OW}$ is a control output which allows data to be output to a peripheral during a DMA read cycle.

### (CLK)

Clock Input: Generally from an Intel® 8224 Clock Generator device. ($\phi2$ TTL) or Intel® 8085A CLK output.

### (RESET)

Reset: An asynchronous input (generally from an 8224 or 8085 device) which disables all DMA channels by clearing the mode register and 3-states all control lines.

### ($A_0$-$A_3$)

Address Lines: These least significant four address lines are bi-directional. In the "slave" mode they are inputs which select one of the registers to be read or programmed. In the "master" mode, they are outputs which constitute the least significant four bits of the 16-bit memory address generated by the 8257

### ($\overline{CS}$)

Chip Select An active-low input which enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode In the "master" mode, $\overline{CS}$ is automatically disabled to prevent the chip from selecting itself while performing the DMA function

## 4. Control Logic

This block controls the sequence of operations during all DMA cycles by generating the appropriate control signals and the 16-bit address that specifies the memory location to be accessed
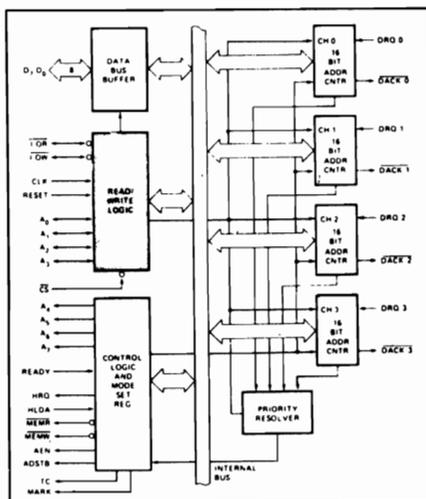


Figure 5. 8257 Block Diagram Showing
Read/Write Logic Function

**(A₄-A₇)**

Address Lines: These four address lines are three-state outputs which constitute bits 4 through 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.

**(READY)**

Ready: This asynchronous input is used to elongate the memory read and write cycles in the 8257 with wait states if the selected memory requires longer cycles. READY must conform to specified setup and hold times.

**(HRQ)**

Hold Request: This output requests control of the system bus In systems with only one 8257, HRQ will normally be applied to the HOLD input on the CPU. HRQ must conform to specified setup and hold times.

**(HLDA)**

Hold Acknowledge: This input from the CPU indicates that the 8257 has acquired control of the system bus.

**(MEMR)**

Memory Read: This active-low three-state output is used to read data from the addressed memory location during DMA Read cycles.

**(MEMW)**

Memory Write: This active-low three-state output is used to write data into the addressed memory location during DMA Write cycles.

**(ADSTB)**

Address Strobe: This output strobes the most significant byte of the memory address into the 8212 device from the data bus.

**(AEN)**

Address Enable. This output is used to disable (float) the System Data Bus and the System Control Bus. It may also be used to disable (float) the System Address Bus by use of an enable on the Address Bus drivers in systems to inhibit non-DMA devices from responding during DMA cycles. It may be further used to isolate the 8257 data bus from the System Data Bus to facilitate the transfer of the 8 most significant DMA address bits over the 8257 data I/O pins without subjecting the System Data Bus to any timing constraints for the transfer. When the 8257 is used in an I/O device structure (as opposed to memory mapped), this AEN output should be used to disable the selection of an I/O device when the DMA address is on the address bus. The I/O device selection should be determined by the DMA acknowledge outputs for the 4 channels.

**(TC)**

Terminal Count: This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block. If the TC STOP bit in the Mode Set register is set, the selected channel will be automatically disabled at the end of that DMA cycle. TC is activated when the 14-bit value in the selected channel's terminal count register equals zero. Recall that the low-order 14-bits of the terminal count register should be loaded with the values (n-1), where n = the desired number of the DMA cycles.

**(MARK)**

Modulo 128 Mark: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block. Only if the total number of DMA cycles (n) is evenly divisible by 128 (and the terminal count register was loaded with n-1), will MARK occur at 128 (and each succeeding multiple of 128) cycles from the beginning of the data block
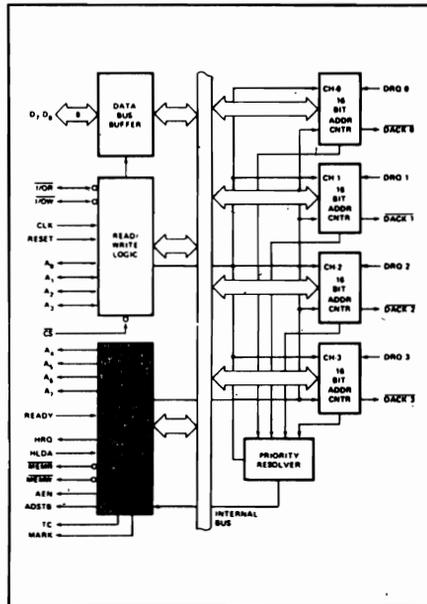


**Figure 6. 8257 Block Diagram Showing Control Logic and Mode Set Register**

### 5. Mode Set Register

When set, the various bits in the Mode Set register enable each of the four DMA channels, and allow four different options for the 8257:
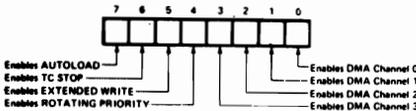


The Mode Set register is normally programmed by the CPU after the DMA address register(s) and terminal count register(s) are initialized. The Mode Set Register is cleared by the RESET input, thus disabling all options, inhibiting all channels, and preventing bus conflicts on power-up. A channel should not be left enabled unless its DMA address and terminal count registers contain valid values; otherwise, an inadvertent DMA request (DRQn) from a peripheral could initiate a DMA cycle that would destroy memory data.

The various options which can be enabled by bits in the Mode Set register are explained below:

### Rotating Priority Bit 4

In the Rotating Priority Mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority.
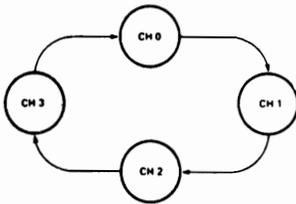


If the ROTATING PRIORITY bit is not set (set to a zero), each DMA channel has a fixed priority. In the fixed priority mode, Channel 0 has the highest priority and Channel 3 has the lowest priority. If the ROTATING PRIORITY bit is set to a one, the priority of each channel changes after each DMA cycle (not each DMA request). Each channel moves up to the next highest priority assignment, while the channel which has just been serviced moves to the lowest priority assignment:

| | CHANNEL→ JUST SERVICED | CH-0 | CH-1 | CH-2 | CH-3 |
|---|---|---|---|---|---|
| Priority → Assignments | Highest | CH-1 | CH-2 | CH-3 | CH-0 |
| | ↑ | CH-2 | CH-3 | CH-0 | CH-1 |
| | ↓ | CH-3 | CH-0 | CH-1 | CH-2 |
| | Lowest | CH-0 | CH-1 | CH-2 | CH-3 |

Note that rotating priority will prevent any one channel from monopolizing the DMA mode; consecutive DMA cycles will service different channels if more than one channel is enabled and requesting service. There is no overhead penalty associated with this mode of operation. All DMA operations began with Channel 0 initially assigned to the highest priority for the first DMA cycle.

### Extended Write Bit 5

If the EXTENDED WRITE bit is set, the duration of both the MEMW and I/OW signals is extended by activating them earlier in the DMA cycle. Data transfers within microcomputer systems proceed asynchronously to allow use of various types of memory and I/O devices with access times. If a device cannot be accessed specific amount of time it returns a "not ready" to the 8257 that causes the 8257 to insert one or more wait states in its internal sequencing. Some devices are fast enough to be accessed without the use of wait states, but if they generate their READY response with the leading edge of the I/OW or MEMW signal (which generally occurs late in the transfer sequence), they would normally cause the 8257 to enter a wait state because it does not receive READY in time. For systems with these types of devices, the Extended Write option provides alternative timing for the I/O and memory write signals which allows the devices to return an early READY and prevents the unnecessary occurrence of wait states in the 8257, thus increasing system throughput

### TC Stop Bit 6

If the TC STOP bit is set, a channel is disabled (i.e., its enable bit is reset) after the Terminal Count (TC) output goes true, thus automatically preventing further DMA operation on that channel. The enable bit for that channel must be re-programmed to continue or begin another DMA operation. If the TC STOP bit is not set, the occurrence of the TC output has no effect on the channel enable bits. In this case, it is generally the responsibility of the peripheral to cease DMA requests in order to terminate a DMA operation.

### Auto Load Bit 7

The Auto Load mode permits Channel 2 to be used for repeat block or block chaining operations, without immediate software intervention between blocks. Channel 2 registers are initialized as usual for the first data block; Channel 3 registers, however, are used to store the block re-initialization parameters (DMA starting address, terminal count and DMA transfer mode). After the first block of DMA cycles is executed by Channel 2 (i.e., after the TC output goes true), the parameters stored in the Channel 3 registers are transferred to Channel 2 during an "update" cycle. Note that the TC STOP feature, described above, has no effect on Channel 2 when the Auto Load bit is set.

If the Auto Load bit is set, the initial parameters for Channel 2 are automatically duplicated in the Channel 3 registers when Channel 2 is programmed. This permits repeat block operations to be set up with the programming of a single channel. Repeat block operations can be used in applications such as CRT refreshing. Channels 2 and 3 can still be loaded with separate values if Channel 2 is loaded before loading Channel 3. Note that in the Auto Load mode, Channel 3 is still available to the user if the Channel 3 enable bit is set, but use of this channel will change the values to be auto loaded into Channel 2 at update time. All that is necessary to use the Auto Load feature for chaining operations is to reload Channel 3 registers at the conclusion of each update cycle with the new parameters for the next data block transfer.

Each time that the 8257 enters an update cycle; the update flag in the status register is set and parameters in Channel 3 are transferred to Channel 2, non-destructively for Channel 3. The actual re-initialization of Channel 2 occurs at the beginning of the next channel 2 DMA cycle after the TC cycle. This will be the first DMA cycle of the new data block for Channel 2. The update flag is cleared at the conclusion of this DMA cycle. For chaining operations, the update flag in the status register can be monitored by the CPU to determine when the re-initialization process has been completed so that the next block parameters can be safely loaded into Channel 3.

### 6. Status Register

The eight-bit status register indicates which channels have reached a terminal count condition and includes the update flag described previously.
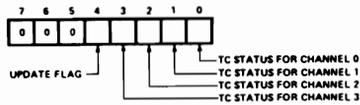


The TC status bits are set when the Terminal Count (TC) output is activated for that channel. These bits remain set until the status register is read or the 8257 is reset. The UPDATE FLAG, however, is not affected by a status register read operation. The UPDATE FLAG can be cleared by resetting the 8257, by changing to the non-auto load mode (i.e., by resetting the AUTO LOAD bit in the Mode Set register) or it can be left to clear itself at the completion of the update cycle. The purpose of the UPDATE FLAG is to prevent the CPU from inadvertently skipping a data block by overwriting a starting address or terminal count in the Channel 3 registers before those parameters are properly auto-loaded into Channel 2.

The user is cautioned against reading the TC status register and using this information to reenable channels that have not completed operation. Unless the DMA channels are inhibited a channel could reach terminal count (TC) between the status read and the mode write. DMA can be inhibited by a hardware gate on the HRQ line or by disabling channels with a mode word before reading the TC status.
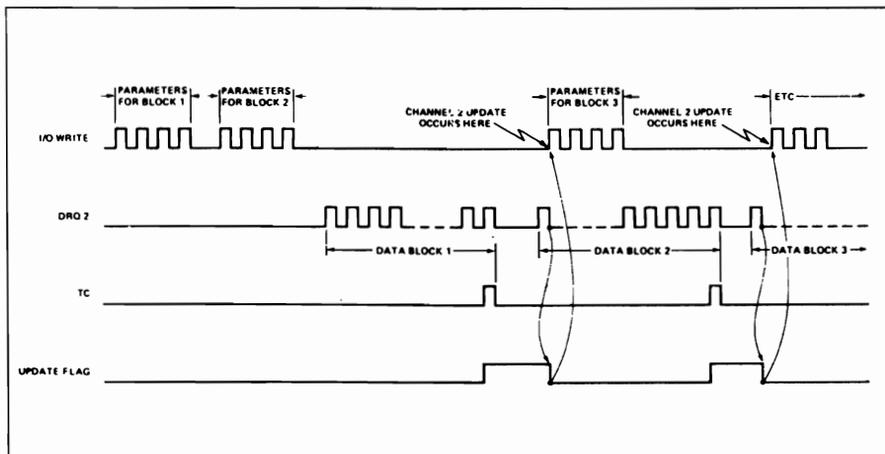


**Figure 7. Autoload Timing**

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## OPERATIONAL SUMMARY

### Programming and Reading the 8257 Registers

There are four pairs of "channel registers" each pair consisting of a 16-bit DMA address register and a 16-bit terminal count register (one pair for each channel) The 8257 also includes two "general registers" one 8-bit Mode Set register and one 8-bit Status register. The registers are loaded or read when the CPU executes a write or read instruction that addresses the 8257 device and the appropriate register within the 8257. The 8228 generates the appropriate read or write control signal (generally I/OR or I/OW while the CPU places a 16-bit address on the system address bus, and either outputs the data to be written onto the system data bus or accepts the data being read from the data bus All or some of the most significant 12 address bits $A_4$-$A_{15}$ (depending on the systems memory, I/O configuration) are usually decoded to produce the chip select ($\overline{CS}$) input to the 8257 An I/O Write input (or Memory Write in memory mapped I/O configurations, described below) specifies that the addressed register is to be programmed, while an I/O Read input (or Memory Read) specifies that the addressed register is to be read Address bit 3 specifies whether a "channel register" ($A_3 = 0$) or the Mode Set (program only)/Status (read only) register ($A_3 = 1$) is to be accessed

The least significant three address bits, $A_0$-$A_2$, indicate the specific register to be accessed. When accessing the Mode Set or Status register, $A_0$-$A_2$ are all zero When accessing a channel register bit $A_0$ differentiates between the DMA address register ($A_0 = 0$) and the terminal count register ($A_0 = 1$), while bits $A_1$ and $A_2$ specify one of the

| CONTROL INPUT | $\overline{CS}$ | $\overline{I/OW}$ | $\overline{I/OR}$ | A3 |
|---|---|---|---|---|
| Program Half of a Channel Register | 0 | 0 | 1 | 0 |
| Read Half of a Channel Register | 0 | 1 | 0 | 0 |
| Program Mode Set Register | 0 | 0 | 1 | 1 |
| Read Status Register | 0 | 1 | 0 | 1 |

four channels Because the "channel registers" are 16-bits, two program instruction cycles are required to load or read an entire register The 8257 contains a first/last (F/L) flip flop which toggles at the completion of each channel program or read operation. The F/L flip flop determines whether the upper or lower byte of the register is to be accessed The F/L flip flop is reset by the RESET input and whenever the Mode Set register is loaded. To maintain proper synchronization when accessing the "channel registers" all channel command instruction operations should occur in pairs, with the lower byte of a register always being accessed first. Do not allow $\overline{CS}$ to clock while either $\overline{I/OR}$ or $\overline{I/OW}$ is active, as this will cause an erroneous F/L flip flop state. In systems utilizing an interrupt structure, interrupts should be disabled prior to any paired programming operations to prevent an interrupt from splitting them The result of such a split would leave the F/L F/F in the wrong state. This problem is particularly obvious when other DMA channels are programmed by an interrupt structure

### 8257 Register Selection

| REGISTER | BYTE | ADDRESS INPUTS | | | | F/L | *BI-DIRECTIONAL DATA BUS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $A_3$ | $A_2$ | $A_1$ | $A_0$ | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| CH-0 DMA Address | LSB | 0 | 0 | 0 | 0 | 0 | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
| | MSB | 0 | 0 | 0 | 0 | 1 | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ |
| CH-0 Terminal Count | LSB | 0 | 0 | 0 | 1 | 0 | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ |
| | MSB | 0 | 0 | 0 | 1 | 1 | Rd | Wr | $C_{13}$ | $C_{12}$ | $C_{11}$ | $C_{10}$ | $C_9$ | $C_8$ |
| CH-1 DMA Address | LSB | 0 | 0 | 1 | 0 | 0 | Same as Channel 0 | | | | | | | |
| | MSB | 0 | 0 | 1 | 0 | 1 | | | | | | | | |
| CH-1 Terminal Count | LSB | 0 | 0 | 1 | 1 | 0 | | | | | | | | |
| | MSB | 0 | 0 | 1 | 1 | 1 | | | | | | | | |
| CH-2 DMA Address | LSB | 0 | 1 | 0 | 0 | 0 | Same as Channel 0 | | | | | | | |
| | MSB | 0 | 1 | 0 | 0 | 1 | | | | | | | | |
| CH-2 Terminal Count | LSB | 0 | 1 | 0 | 1 | 0 | | | | | | | | |
| | MSB | 0 | 1 | 0 | 1 | 1 | | | | | | | | |
| CH-3 DMA Address | LSB | 0 | 1 | 1 | 0 | 0 | Same as Channel 0 | | | | | | | |
| | MSB | 0 | 1 | 1 | 0 | 1 | | | | | | | | |
| CH-3 Terminal Count | LSB | 0 | 1 | 1 | 1 | 0 | | | | | | | | |
| | MSB | 0 | 1 | 1 | 1 | 1 | | | | | | | | |
| MODE SET (Program only) | — | 1 | 0 | 0 | 0 | 0 | AL | TCS | EW | RP | EN3 | EN2 | EN1 | EN0 |
| STATUS (Read only) | — | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | UP | TC3 | TC2 | TC1 | TC0 |

*$A_0$-$A_{15}$: DMA Starting Address, $C_0$-$C_{13}$: Terminal Count value (N-1), Rd and Wr: DMA Verify (00). Write (01) or Read (10) cycle selection, AL: Auto Load, TCS: TC STOP, EW: EXTENDED WRITE, RP: ROTATING PRIORITY, EN3-EN0: CHANNEL ENABLE MASK, UP: UPDATE FLAG, TC3-TC0: TERMINAL COUNT STATUS BITS.
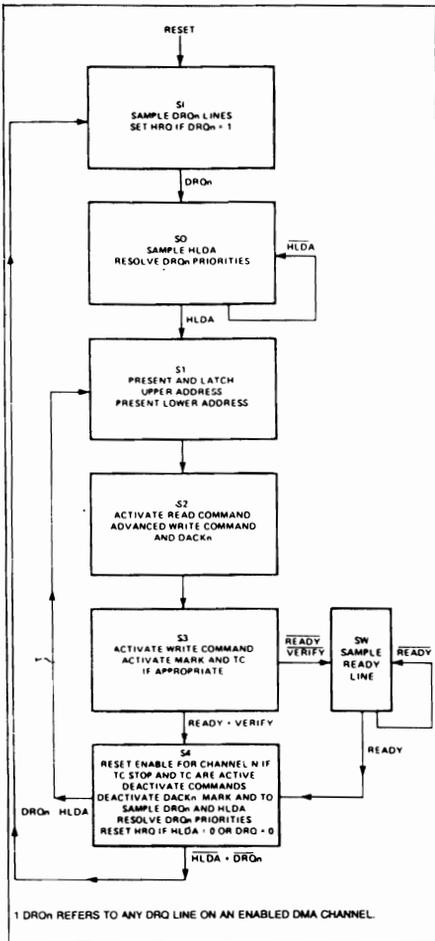
**Figure 8. DMA Operation State Diagram**

## DMA OPERATION

### Single Byte Transfers

A single byte transfer is initiated by the I/O device raising the DRQ line of one channel of the 8257. If the channel is enabled, the 8257 will output a HRQ to the CPU. The 8257 now waits until a HLDA is received insuring that the system bus is free for its use. Once HLDA is received the DACK line for the requesting channel is activated (LOW). The DACK line acts as a chip select for the requesting I/O device. The 8257 then generates the

read and write commands and byte transfer occurs between the selected I/O device and memory. After the transfer is complete, the DACK line is set HIGH and the HRQ line is set LOW to indicate to the CPU that the bus is now free for use. DRQ must remain HIGH until DACK is issued to be recognized and must go LOW before S4 of the transfer sequence to prevent another transfer from occuring. (See timing diagram.)

### Consecutive Transfers

If more than one channel requests service simultaneously, the transfer will occur in the same way a burst does. No overhead is incurred by switching from one channel to another. In each S4 the DRQ lines are sampled and the highest priority request is recognized during the next transfer. A burst mode transfer in a lower priority channel will be overridden by a higher priority request. Once the high priority transfer has completed control will return to the lower priority channel if its DRQ is still active. No extra cycles are needed to execute this sequence and the HRQ line remains active until all DRQ lines go LOW.

### Control Override

The continuous DMA transfer mode described above can be interrupted by an external device by lowering the HLDA line. After each DMA transfer the 8257 samples the HLDA line to insure that it is still active. If it is not active, the 8257 completes the current transfer, releases the HRQ line (LOW) and returns to the idle state. If DRQ lines are still active, the 8257 will raise the HRQ line in the third cycle and proceed normally. (See timing diagram.)

### Not Ready

The 8257 has a Ready input similar to the 8080A and the 8085A. The Ready line is sampled in State 3. If Ready is LOW the 8257 enters a wait state. Ready is sampled during every wait state. When Ready returns HIGH the 8257 proceeds to State 4 to complete the transfer. Ready is used to interface memory or I/O devices that cannot meet the bus set up times required by the 8257

### Speed

The 8257 uses four clock cycles to transfer a byte of data. No cycles are lost in the master to master transfer maximizing bus efficiency. A 2MHz clock input will allow the 8257 to transfer at a rate of 500K bytes/second.

### Memory Mapped I/O Configurations

The 8257 can be connected to the system bus as a memory device instead of as an I/O device for memory mapped I/O configurations by connecting the system memory control lines to the 8257's I/O control lines and the system I/O control lines to the 8257's memory control lines

This configuration permits use of the 8080's considerably larger repertoire of memory instructions when reading or loading the 8257's registers. Note that with this connection, the programming of the Read (bit 15) and Write (bit 14) bits in the terminal count register will have a different meaning
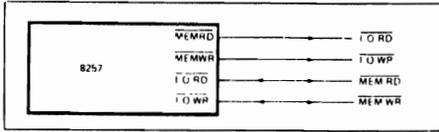
Figure 9. System Interface for Memory Mapped I/O

| BIT 15 READ | BIT 14 WRITE | |
|---|---|---|
| 0 | 0 | DMA Verify Cycle |
| 0 | 1 | DMA Read Cycle |
| 1 | 0 | DMA Write Cycle |
| 1 | 1 | Illegal |

Figure 10. TC Register for Memory Mapped I/O Only

## SYSTEM APPLICATION EXAMPLES
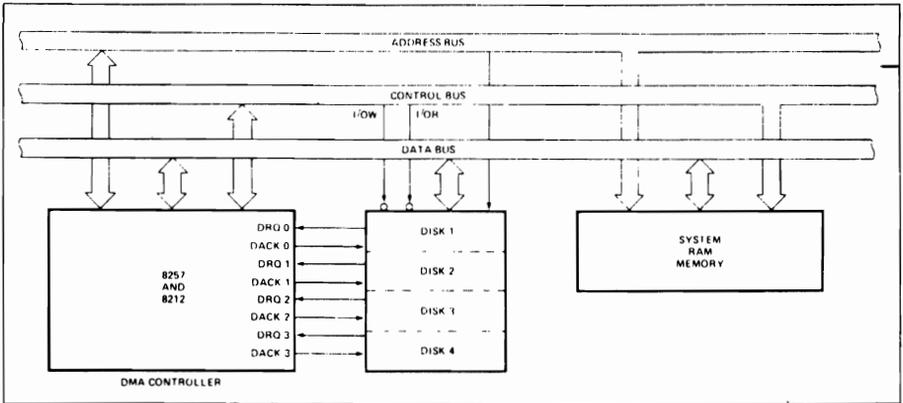


Figure 11. Floppy Disk Controller (4 Drives)
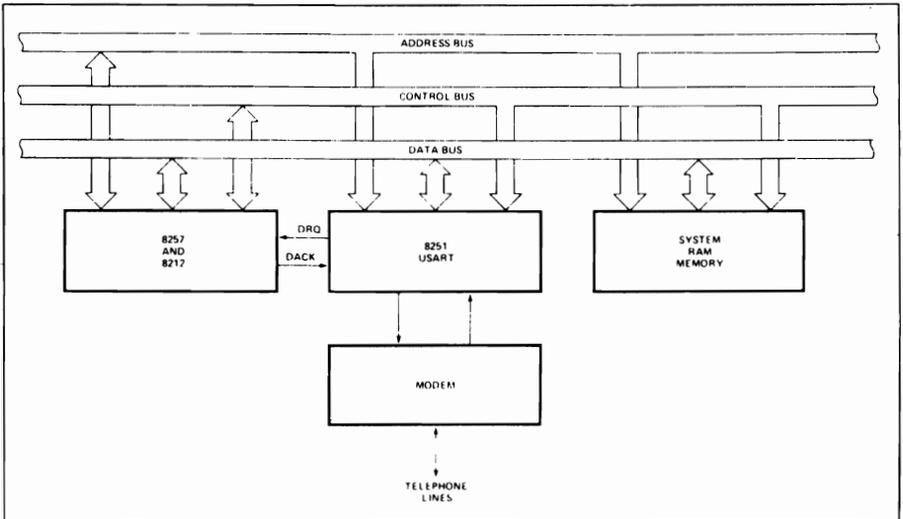


Figure 12. High-Speed Communication Controller

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# 8259A/8259A-2/8259A-8
# PROGRAMMABLE INTERRUPT CONTROLLER

- ■ iAPX 86, iAPX 88 Compatible
- ■ MCS-80®, MCS-85® Compatible
- ■ Eight-Level Priority Controller
- ■ Expandable to 64 Levels
- ■ Programmable Interrupt Modes

- ■ Individual Request Mask Capability
- ■ Single + 5V Supply (No Clocks)
- ■ 28-Pin Dual-In-Line Package
- ■ Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single + 5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel® 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).
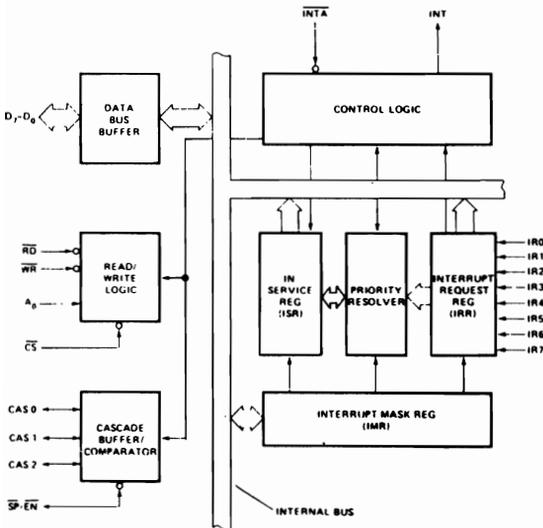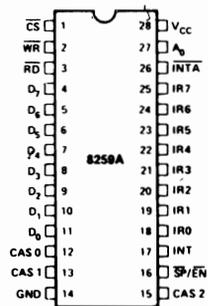


Figure 1. Block Diagram          Figure 2. Pin Configuration

# 8271/8271-6
## PROGRAMMABLE FLOPPY DISK CONTROLLER

- **IBM 3740 Soft Sectored Format Compatible**

- **Programmable Record Lengths**

- **Multi-Sector Capability**

- **Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives**

- **Automatic Read/Write Head Positioning and Verification**

- **Internal CRC Generation and Checking**

- **Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count**

- **Fully MCS-80™ and MCS-85™ Compatible**

- **Single +5V Supply**

- **40-Pin Package**

The Intel® 8271 Programmable Floppy Disk Controller (FDC) is an LSI component designed to interface one to 4 floppy disk drives to an 8-bit microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk controllers.
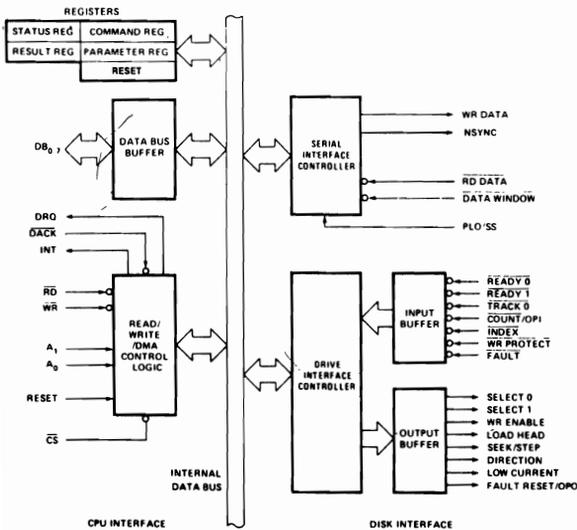


Figure 1. Block Diagram
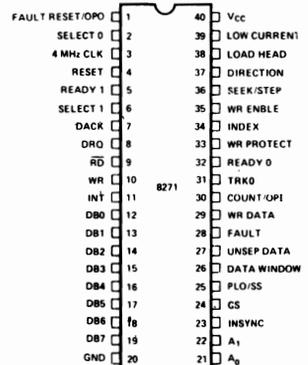
Figure 2. Pin Configuration

# 8272A
# SINGLE/DOUBLE DENSITY
# FLOPPY DISK CONTROLLER

- **IBM Compatible in Both Single and Double Density Recording Formats**
- **Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector**
- **Multi-Sector and Multi-Track Transfer Capability**
- **Drives Up to 4 Floppy or Mini-Floppy Disks**

- **Data Transfers in DMA or Non-DMA Mode**
- **Parallel Seek Operations on Up to Four Drives**
- **Compatible with all Intel and Most Other Microprocessors**
- **Single-Phase 8 MHz Clock**
- **Single +5 Volt Power Supply (±10%)**

The 8272A is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for inter-facing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The 8272A provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Drive Interface. The 8272A is a pin-compatible upgrade to the 8272.
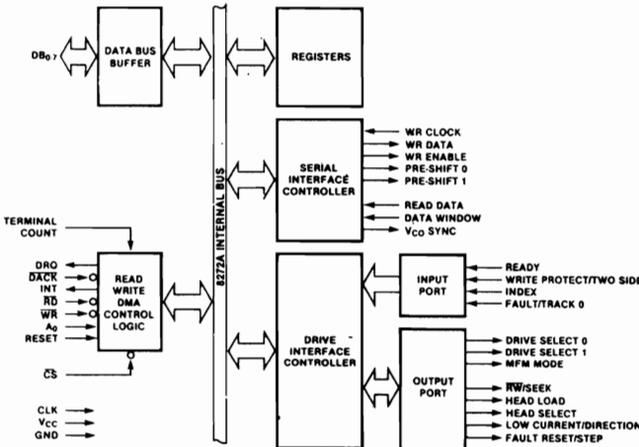


Figure 1. 8272A Internal Block Diagram
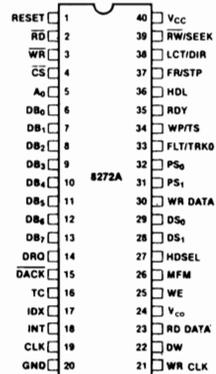


Figure 2. Pin Configuration

# 8273, 8273-4, 8273-8
## PROGRAMMABLE HDLC/SDLC PROTOCOL CONTROLLER

- CCITT X.25 Compatible
- HDLC/SDLC Compatible
- Full Duplex, Half Duplex, or Loop SDLC Operation
- Up to 64K Baud Synchronous Transfers
- Automatic FCS (CRC) Generation and Checking
- Up to 9.6K Baud with On-Board Phase Locked Loop

- Programmable NRZI Encode/Decode
- Two User Programmable Modem Control Ports
- Digital Phase Locked Loop Clock Recovery
- Minimum CPU Overhead
- Fully Compatible with 8048/8080/8085/8088/8086 CPUs
- Single +5V Supply

The Intel® 8273 Programmable HDLC/SDLC Protocol Controller is a dedicated device designed to support the ISO/CCITT's HDLC and IBM's SDLC communication line protocols. It is fully compatible with Intel's new high performance microcomputer systems such as the MCS-88/86™. A frame level command set is achieved by a unique microprogrammed dual processor chip architecture. The processing capability supported by the 8273 relieves the system CPU of the low level real-time tasks normally associated with controllers.



Figure 1. Block Diagram



Figure 2. Pin Configuration

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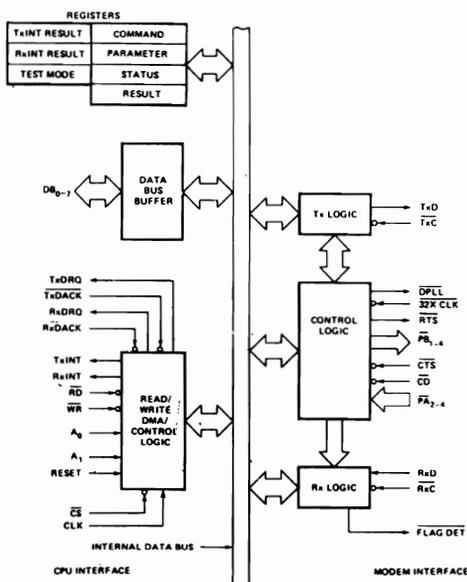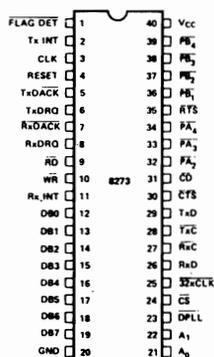
# 8275H
# PROGRAMMABLE CRT CONTROLLER

- **Programmable Screen and Character Format**
- **6 Independent Visual Field Attributes**
- **11 Visual Character Attributes (Graphic Capability)**
- **Cursor Control (4 Types)**
- **Light Pen Detection and Registers**

- **MCS-51®, MCS-85®, iAPX 86, and iAPX 88 Compatible**
- **Dual Row Buffers**
- **Programmable DMA Burst Mode**
- **Single +5V Supply**
- **High Performance HMOS-II**

The Intel® 8275H Programmable CRT Controller is a single chip device to interface CRT raster scan displays with Intel® microcomputer systems. It is manufactured on Intel's advanced HMOS-II process. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed in the 8275H will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.
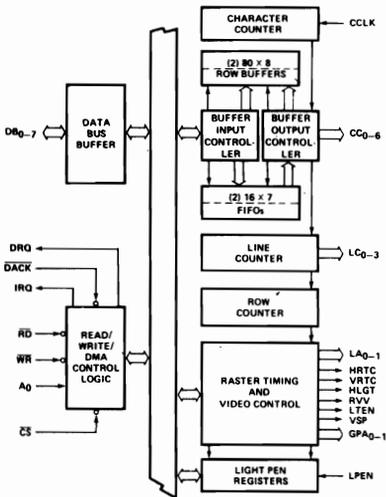


Figure 1. Block Diagram
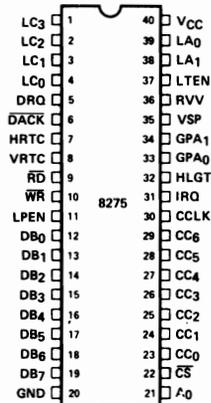


Figure 2. Pin Configuration

# 8276H
# SMALL SYSTEM CRT CONTROLLER

- **Programmable Screen and Character Format**
- **6 Independent Visual Field Attributes**
- **Cursor Control (4 Types)**
- **MCS-51®, MCS-85®, iAPX 86, and iAPX 88 Compatible**

- **Dual Row Buffers**
- **Single +5V Supply**
- **40-Pin Package**
- **3 MHz Clock with 8276-2**
- **High Performance HMOS-III**

The Intel 8276H Small System CRT Controller is a single chip device intended to interface CRT raster scan displays with Intel microcomputers in minimum device-count systems. Its primary function is to refresh the display by buffering character information from main memory and keeping track of the display position on the screen. The flexibility designed into the 8276H will allow simple interface to almost any raster scan CRT display. It can be used with the 8051 Single Chip Microcomputer for a minimum IC count design. It is manufactured on Intel's advanced HMOS-II processor.
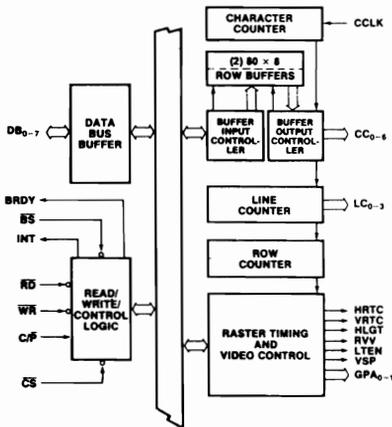


**Figure 1. Block Diagram**
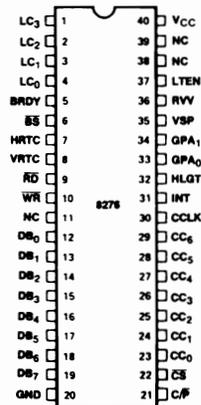


**Figure 2. Pin Configuration**

# 8279/8279-5
# PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

- **Simultaneous Keyboard Display Operations**
- **Scanned Keyboard Mode**
- **Scanned Sensor Mode**
- **Strobed Input Entry Mode**
- **8-Character Keyboard FIFO**
- **2-Key Lockout or N-Key Rollover with Contact Debounce**
- **Dual 8- or 16-Numerical Display**

- **Single 16-Character Display**
- **Right or Left Entry 16-Byte Display RAM**
- **Mode Programmable from CPU**
- **Programmable Scan Timing**
- **Interrupt Output on Key Entry**
- **Available in EXPRESS**
  **—Standard Temperature Range**
  **—Extended Temperature Range**

The Intel* 8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Intel* microprocessors. The keyboard portion can provide a scanned interface to a 64-contact key matrix. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the hall effect and ferrite variety. Key depressions can be 2-key lockout or N-key rollover. Keyboard entries are debounced and strobed in an 8-character FIFO. If more than 8 characters are entered, overrun status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The 8279 has 16X8 display RAM which can be organized into dual 16X4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.
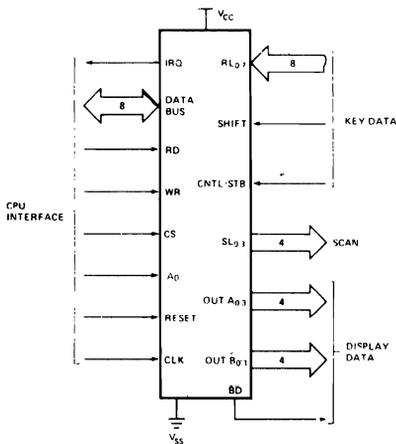


Figure 1. Logic Symbol
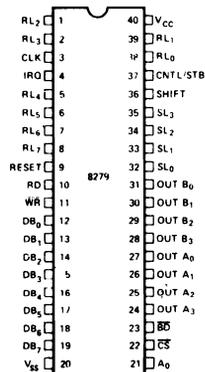


Figure 2. Pin Configuration

## HARDWARE DESCRIPTION

The 8279 is packaged in a 40 pin DIP. The following is a functional description of each pin.

### Table 1. Pin Descriptions

| Symbol | Pin No. | Name and Function |
|---|---|---|
| $DB_0$-$DB_7$ | 8 | **Bi-directional data bus:** All data and commands between the CPU and the 8279 are transmitted on these lines. |
| CLK | 1 | **Clock:** Clock from system used to generate internal timing. |
| RESET | 1 | **Reset:** A high signal on this pin resets the 8279. After being reset the 8279 is placed in the following mode:<br>1) 16 8-bit character display —left entry.<br>2) Encoded scan keyboard—2 key lockout.<br>Along with this the program clock prescaler is set to 31. |
| CS | 1 | **Chip Select:** A low on this pin enables the interface functions to receive or transmit. |
| $A_0$ | 1 | **Buffer Address:** A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data. |
| RD, WR | 2 | **Input/Output Read and Write:** These signals enable the data buffers to either send data to the external bus or receive it from the external bus. |
| IRQ | 1 | **Interrupt Request:** In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected. |
| $V_{SS}$, $V_{CC}$ | 2 | **Ground and power supply pins.** |
| $SL_0$-$SL_3$ | 4 | **Scan Lines:** Scan lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4). |
| $RL_0$-$RL_7$ | 8 | **Return Line:** Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode. |

| Symbol | Pin No. | Name and Function |
|---|---|---|
| SHIFT | 1 | **Shift:** The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low. |
| CNTL/STB | 1 | **Control/Strobed Input Mode:** For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in the Strobed Input mode.<br><br>(Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low. |
| OUT $A_0$-OUT $A_3$<br>OUT $B_0$-OUT $B_3$ | 4<br>4 | **Outputs:** These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines ($SL_0$-$SL_3$) for multiplexed digit displays. The two 4 bit ports may be blanked independently. These two ports may also be considered as one 8-bit port. |
| $\overline{BD}$ | 1 | **Blank Display:** This output is used to blank the display during digit switching or by a display blanking command. |

## FUNCTIONAL DESCRIPTION

Since data input and display are an integral part of many microprocessor designs, the system designer needs an interface that can control these functions without placing a large load on the CPU. The 8279 provides this function for 8-bit microprocessors.

The 8279 has two sections: keyboard and display. The keyboard section can interface to regular typewriter style keyboards or random toggle or thumb switches. The display section drives alphanumeric displays or a bank of indicator lights. Thus the CPU is relieved from scanning the keyboard or refreshing the display.

The 8279 is designed to directly connect to the microprocessor bus. The CPU can program all operating modes for the 8279. These modes include:

## Input Modes

- Scanned Keyboard — with encoded (8 x 8 key keyboard) or decoded (4 x 8 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.

- Scanned Sensor Matrix — with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Ke . status (open or closed) stored in RAM addressable by CPU.

- Strobed Input — Data on return lines during control line strobe is transferred to FIFO.

## Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit ($B_0 = D_0$, $A_3 = D_7$).

- Right entry or left entry display formats.

Other features of the 8279 include:

- Mode programming from the CPU.

- Clock Prescaler

- Interrupt output to signal CPU when there is keyboard or sensor data available.

- An 8 byte FIFO to store keyboard information.

- 16 byte internal Display RAM for display refresh. This RAM can also be read by the CPU.

## PRINCIPLES OF OPERATION

The following is a description of the major elements of the 8279 Programmable Keyboard/Display interface device. Refer to the block diagram in Figure 3.

### I/O Control and Data Buffers

The I/O control section uses the $\overline{CS}$, $A_0$, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers. All data flow to and from the 8279 is enabled by $\overline{CS}$. The character of the information, given or desired by the CPU, is identified by $A_0$. A logic one means the information is a command or status. A logic zero means the information is data. $\overline{RD}$ and $\overline{WR}$ determine the direction of data flow through the Data Buffers. The Data Buffers are bi-directional buffers that connect the internal bus to the external bus. When the chip is not selected ($\overline{CS}$ = 1), the devices are in a high impedance state. The drivers input during $\overline{WR} \bullet \overline{CS}$ and output during $\overline{RD} \bullet \overline{CS}$.

### Control and Timing Registers and Timing Control

These registers store the keyboard and display modes and other operating conditions programmed by the CPU. The modes are programmed by presenting the proper command on the data lines with $A_0 = 1$ and then sending a $\overline{WR}$. The command is latched on the rising edge of $\overline{WR}$.
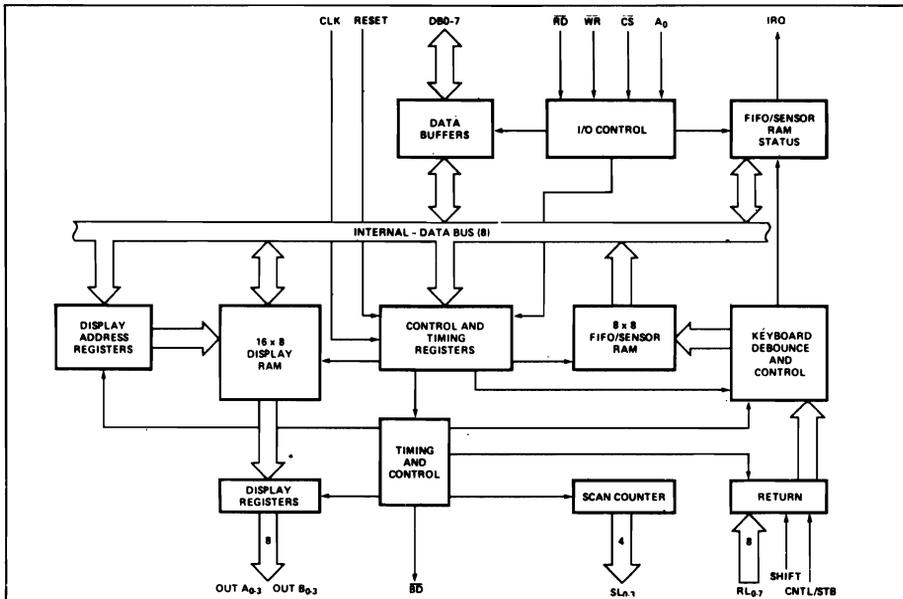


**Figure 3. Internal Block Diagram**

The command is then decoded and the appropriate function is set. The timing control contains the basic timing counter chain. The first counter is a ÷ N prescaler that can be programmed to yield an internal frequency of 100 kHz which gives a 5.1 ms keyboard scan time and a 10.3 ms debounce time. The other counters divide down the basic internal frequency to provide the proper key scan, row scan, keyboard matrix scan, and display scan times.

### Scan Counter

The scan counter has two modes. In the encoded mode, the counter provides a binary count that must be externally decoded to provide the scan lines for the keyboard and display. In the decoded mode, the scan counter decodes the least significant 2 bits and provides a decoded 1 of 4 scan. Note than when the keyboard is in decoded scan, so is the display. This means that only the first 4 characters ir the Display RAM are displayed.

In the encoded mode, the scan lines are active high outputs. In the decoded mode, the scan lines are active low outputs.

### Return Buffers and Keyboard Debounce and Control

The 8 return lines are buffered and latched by the Return Buffers. In the keyboard mode, these lines are scanned, looking for key closures in that row. If the debounce circuit detects a closed switch, it waits about 10 msec to check if the switch remains closed. If it does, the address of the switch in the matrix plus the status of SHIFT and CONTROL are transferred to the FIFO. In the scanned Sensor Matrix modes, the contents of the return lines is directly transferred to the corresponding row of the Sensor RAM (FIFO) each key scan time. In Strobed Input mode, the contents of the return lines are transferred to the FIFO on the rising edge of the CNTL/STB line pulse.

### FIFO/Sensor RAM and Status

This block is a dual function 8 x 8 RAM. In Keyboard or Strobed Input modes, it is a FIFO. Each new entry is written into successive RAM positions and each is then read in order of entry. FIFO status keeps track of the number of characters in the FIFO and whether it is full or empty. Too many reads or writes will be recognized as an error. The status can be read by an $\overline{RD}$ with $\overline{CS}$ low and A₀ high. The status logic also provides an IRQ signal when the FIFO is not empty. In Scanned Sensor Matrix mode, the memory is a Sensor RAM. Each row of the Sensor RAM is loaded with the status of the corresponding row of sensor in the sensor matrix. In this mode, IRQ is high if a change in a sensor is detected.

### Display Address Registers and Display RAM

The Display Address Registers hold the address of the word currently being written or read by the CPU and the two 4-bit nibbles being displayed. The read/write addresses are programmed by CPU command. They also can be set to auto increment after each read or write. The Display RAM can be directly read by the CPU after the correct mode and address is set. The addresses for the A and B nibbles are automatically updated by the 8279 to match data entry by the CPU. The A and B nibbles can be entered independently or as one word, according to the mode that is set by the CPU. Data entry to the display can be set to either left or right entry. See Interface Considerations for details.

## SOFTWARE OPERATION

### 8279 commands

The following commands program the 8279 operating modes. The commands are sent on the Data Bus with $\overline{CS}$ low and A₀ high and are loaded to the 8279 on the rising edge of $\overline{WR}$.

### Keyboard/Display Mode Set

MSB                        LSB

Code: | 0 | 0 | 0 | D | D | K | K | K |

Where DD is the Display Mode and KKK is the Keyboard Mode.

**DD**

0 0  8 8-bit character display — Left entry
0 1  16 8-bit character display — Left entry*
1 0  8 8-bit character display — Right entry
1 1  16 8-bit character display — Right entry

For description of right and left entry, see Interface Considerations. Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

**KKK**

0 0 0  Encoded Scan Keyboard — 2 Key Lockout*
0 0 1  Decoded Scan Keyboard — 2-Key Lockout
0 1 0  Encoded Scan Keyboard — N-Key Rollover
0 1 1  Decoded Scan Keyboard — N-Key Rollover
1 0 0  Encoded Scan Sensor Matrix
1 0 1  Decoded Scan Sensor Matrix
1 1 0  Strobed Input, Encoded Display Scan
1 1 1  Strobed Input, Decoded Display Scan

**Program Clock**

Code: | 0 | 0 | 1 | P | P | P | P | P |

All timing and multiplexing signals for the 8279 are generated by an internal prescaler. This prescaler divides the external clock (pin 3) by a programmable integer. Bits PPPPP determine the value of this integer which ranges from 2 to 31. Choosing a divisor that yields 100 kHz will give the specified scan and debounce times. For instance, if Pin 3 of the 8279 is being clocked by a 2 MHz signal, PPPPP should be set to 10100 to divide the clock by 20 to yield the proper 100 kHz operating frequency.

**Read FIFO/Sensor RAM**

Code: | 0 | 1 | 0 | AI | X | A | A | A |  X = Don't Care

The CPU sets up the 8279 for a read of the FIFO/Sensor RAM by first writing this command. In the Scan Key-

*Default after reset.

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board Mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read ($A_0 = 0$) in the same sequence in which the data first entered the FIFO. All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set (AI = 1), each successive read will be from the subsequent row of the sensor RAM.

### Read Display RAM

Code: | 0 | 1 | 1 | AI | A | A | A | A |

The CPU sets up the 8279 for a read of the Display RAM by first writing this command. The address bits AAAA select one of the 16 rows of the Display RAM. If the AI flag is set (AI = 1), this row address will be incremented after each following read *or write* to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read *or write* address and the sense of the Auto-Increment mode for both operations.

### Write Display RAM

Code: | 1 | 0 | 0 | AI | A | A | A | A |

The CPU sets up the 8279 for a write to the Display RAM by first writing this command. After writing the command with $A_0 = 1$, all subsequent writes with $A_0 = 0$ will be to the Display RAM. The addressing and Auto-Increment functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display or FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next Read location.

### Display Write Inhibit/Blanking

Code: | | | | A | B | A | B |
| 1 | 0 | 1 | X | IW | IW | BL | BL |

The IW Bits can be used to mask nibble A and nibble B in applications requiring separate 4-bit display ports. By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the Display RAM from the CPU do not affect that port. Thus, if each nibble is input to a BCD decoder, the CPU may write a digit to the Display RAM without affecting the other digit being displayed. It is important to note that bit $B_0$ corresponds to bit $D_0$ on the CPU bus, and that bit $A_3$ corresponds to bit $D_7$.

If the user wishes to blank the display, the BL flags are available for each nibble. The last Clear command issued determines the code to be used as a "blank." This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

### Clear

Code: | 1 | 1 | 0 | $C_D$ | $C_D$ | $C_D$ | $C_F$ | $C_A$ |

The $C_D$ bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows:

$C_D$ $C_D$ $C_D$

| 0 | X | All Zeros (X = Don't Care) |
| 1 | 0 | AB = Hex 20 (0010 0000) |
| 1 | 1 | All Ones |

Enable clear display when = 1 (or by $C_A$ = 1)
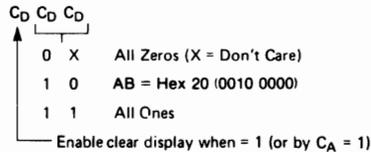
During the time the Display RAM is being cleared ($\sim$160 μs), it may not be written to. The most significant bit of the FIFO status word is set during this time. When the Display RAM becomes available again, it automatically resets.

If the $C_F$ bit is asserted ($C_F$ = 1), the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

$C_A$, the Clear All bit, has the combined effect of $C_D$ and $C_F$; it uses the $C_D$ clearing code on the Display RAM and also clears FIFO status. Furthermore, it resynchronizes the internal timing chain.

### End Interrupt/Error Mode Set

Code: | 1 | 1 | 1 | E | X | X | X | X |   X = Don't care.

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM. (The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset).

For the N-key rollover mode — if the E bit is programmed to "1" the chip will operate in the special Error mode. (For further details, see Interface Considerations Section.)

### Status Word

The status word contains the FIFO status, error, and display unavailable signals. This word is read by the CPU when $A_0$ is high and $\overline{CS}$ and $\overline{RD}$ are low. See Interface Considerations for more detail on status word.

### Data Read

Data is read when $A_0$, $\overline{CS}$ and $\overline{RD}$ are all low. The source of the data is specified by the Read FIFO or Read Display commands. The trailing edge of $\overline{RD}$ will cause the address of the RAM being read to be incremented if the Auto-Increment flag is set. FIFO reads always increment (if no error occurs) independent of AI.

### Data Write

Data that is written with $A_0$, $\overline{CS}$ and $\overline{WR}$ low is always written to the Display RAM. The address is specified by the latest Read Display or Write Display command. Auto-Incrementing on the rising edge of $\overline{WR}$ occurs if AI set by the latest display command.

## INTERFACE CONSIDERATIONS

### Scanned Keyboard Mode, 2-Key Lockout

There are three possible combinations of conditions that can occur during debounce scanning. When a key is depressed, the debounce logic is set. Other depressed keys are looked for during the next two scans. If none are encountered, it is a single key depression and the key position is entered into the FIFO along with the status of CNTL and SHIFT lines. If the FIFO was empty, IRQ will be set to signal the CPU that there is an entry in the FIFO. If the FIFO was full, the key will not be entered and the error flag will be set. If another closed switch is encountered, no entry to the FIFO can occur. If all other keys are released before this one, then it will be entered to the FIFO. If this key is released before any other, it will be entirely ignored. A key is entered to the FIFO only once per depression, no matter how many keys were pressed along with it or in what order they were released. If two keys are depressed within the debounce cycle, it is a simultaneous depression. Neither key will be recognized until one key remains depressed alone. The last key will be treated as a single key depression.

### Scanned Keyboard Mode, N-Key Rollover

With N-key Rollover each key depression is treated independently from all others. When a key is depressed, the debounce circuit waits 2 keyboard scans and then checks to see if the key is still down If it is, the key is entered into the FIFO Any number of keys can be depressed and another can be recognized and entered into the FIFO. If a simultaneous depression occurs, the keys are recognized and entered according to the order the keyboard scan found them.

### Scanned Keyboard — Special Error Modes

For N-key rollover mode the user can program a special error mode. This is done by the "End Interrupt/Error Mode Set" command. The debounce cycle and key-validity check are as in normal N-key mode If during a single debounce cycle, two keys are found depressed, this is considered a simultaneous multiple depression, and sets an error flag. This flag will prevent any further writing into the FIFO and will set interrupt (if not yet set) The error flag could be read in this mode by reading the FIFO STATUS word (See "FIFO STATUS" for further details.) The error flag is reset by sending the normal CLEAR command with C$_F$   1

### Sensor Matrix Mode

In Sensor Matrix mode, the debounce logic is inhibited. The status of the sensor switch is inputted directly to the Sensor RAM. In this way the Sensor RAM keeps an image of the state of the switches in the sensor matrix. Although debouncing is not provided, this mode has the advantage that the CPU knows how long the sensor was closed and when it was released. A keyboard mode can only indicate a validated closure To make the software easier the designer should functionally group the sensors by row since this is the format in which the CPU will read them.

The IRQ line goes high if any sensor value change is detected at the end of a sensor matrix scan. The IRQ line is cleared by the first data read operation if the Auto-

Increment flag is set to zero, or by the End Interrupt command if the Auto-Increment flag is set to one.

Note: Multiple changes in the matrix Addressed by (SL$_{0-3}$ = 0) may cause multiple interrupts. (SL$_0$ = 0 in the Decoded Mode). Reset may cause the 8279 to see multiple changes.

### Data Format

In the Scanned Keyboard mode, the character entered into the FIFO corresponds to the position of the switch in the keyboard plus the status of the CNTL and SHIFT lines (non-inverted). CNTL is the MSB of the character and SHIFT is the next most significant bit. The next three bits are from the scan counter and indicate the row the key was found in. The last three bits are from the column counter and indicate to which return line the key was connected.

| MSB | | | | LSB |
|------|-------|------|------|
| CNTL | SHIFT | SCAN | RETURN |

SCANNED KEYBOARD DATA FORMAT
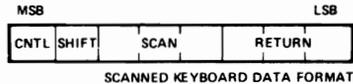
In Sensor Matrix mode, the data on the return lines is entered directly in the row of the Sensor RAM that corresponds to the row in the matrix being scanned. Therefore, each switch postion maps directly to a Sensor RAM position. The SHIFT and CNTL inputs are ignored in this mode. Note that switches are not necessarily the only thing that can be connected to the return lines in this mode. Any logic that can be triggered by the scan lines can enter data to the return line inputs. Eight multiplexed input ports could be tied to the return lines and scanned by the 8279.

| MSB | | | | | | | LSB |
|------|------|------|------|------|------|------|------|
| RL$_7$ | RL$_6$ | RL$_5$ | RL$_4$ | RL$_3$ | RL$_2$ | RL$_1$ | RL$_0$ |

In Strobed Input mode, the data is also entered to the FIFO from the return lines. The data is entered by the rising edge of a CNTL/STB line pulse. Data can come from another encoded keyboard or simple switch matrix. The return lines can also be used as a general purpose strobed input.

| MSB | | | | | | | LSB |
|------|------|------|------|------|------|------|------|
| RL$_7$ | RL$_6$ | RL$_5$ | RL$_4$ | RL$_3$ | RL$_2$ | RL$_1$ | RL$_0$ |

### Display

#### Left Entry

Left Entry mode is the simplest display format in that each display position directly corresponds to a byte (or nibble) in the Display RAM. Address 0 in the RAM is the left-most display character and address 15 (or address 7 in 8 character display) is the right most display character. Entering characters from position zero causes the display to fill from the left The 17th (9th) character is entered back in the left most position and filling again proceeds from there.

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1st entry

| 0 | 1 | | 14 | 15 | ← Display RAM Address |
| 1 | | | | |

2nd entry

| 0 | 1 | | 14 | 15 |
| 1 | 2 | | | |

16th entry

| 0 | 1 | | 14 | 15 |
| 1 | 2 | | 15 | 16 |

17th entry

| 0 | 1 | | 14 | 15 |
| 17 | 2 | | 15 | 16 |

18th entry

| 0 | 1 | | 14 | 15 |
| 17 | 18 | | 15 | 16 |

LEFT ENTRY MODE
(AUTO INCREMENT)
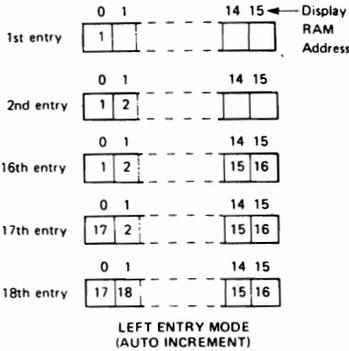
### Right Entry

Right entry is the method used by most electronic calculators. The first entry is placed in the right most display character. The next entry is also placed in the right most character after the display is shifted left one character. The left most character is shifted off the end and is lost.

1st entry

| 1 | 2 | | 14 | 15 | 0 | ← Display RAM Address |
| | | | | | 1 |

2nd entry

| 2 | 3 | | 15 | 0 | 1 |
| | | | | 1 | 2 |

3rd entry

| 3 | 4 | | 0 | 1 | 2 |
| | | | 1 | 2 | 3 |

16th entry

| 0 | 1 | | 13 | 14 | 15 |
| 1 | 2 | | 14 | 15 | 16 |

17th entry

| 1 | 2 | | 14 | 15 | 0 |
| 2 | 3 | | 15 | 16 | 17 |

18th entry

| 2 | 3 | | 15 | 0 | 1 |
| 3 | 4 | | 16 | 17 | 18 |

RIGHT ENTRY MODE
(AUTO INCREMENT)
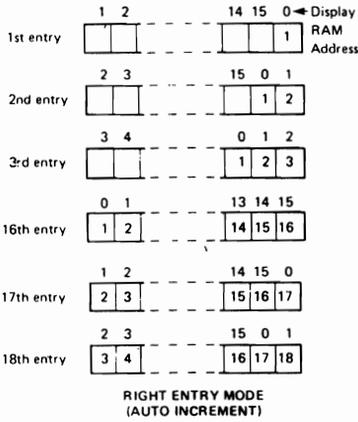
Note that now the display position and register address do not correspond. Consequently, entering a character to an arbitrary position in the Auto Increment mode may have unexpected results. Entry starting at Display RAM address 0 with sequential entry is recommended.

### Auto Increment

In the Left Entry mode, Auto Incrementing causes the address where the CPU will next write to be incremented by one and the character appears in the next location. With non-Auto Incrementing the entry is both to the same RAM address and display position. Entry to an arbitrary address in the Auto Increment mode has no undesirable side effects and the result is predictable:

1st entry

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | ← Display RAM Address |
| 1 | | | | | | | |

2nd entry

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 | 2 | | | | | | |

Command 10010101

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 | 2 | | | | | | |

Enter next at Location 5 Auto Increment

3rd entry

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 | 2 | | | | 3 | | |

4th entry

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 | 2 | | | | 3 | 4 | |

LEFT ENTRY MODE
(AUTO INCREMENT)
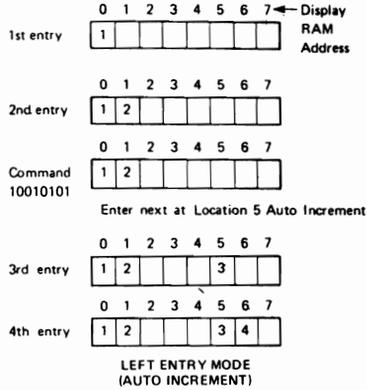
In the Right Entry mode, Auto Incrementing and non Incrementing have the same effect as in the Left Entry except if the address sequence is interrupted:

1st entry

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | ← Display RAM Address |
| | | | | | | | 1 |

2nd entry

| 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 |
| | | | | | | 1 | 2 |

Command 10010101

| 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 |
| | | | | | | 1 | 2 |

Enter next at Location 5 Auto Increment

3rd entry

| 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 |
| | 3 | | | | 1 | 2 | |

4th entry

| 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 3 | 4 | | 1 | 2 | | | |

RIGHT ENTRY MODE
(AUTO INCREMENT)
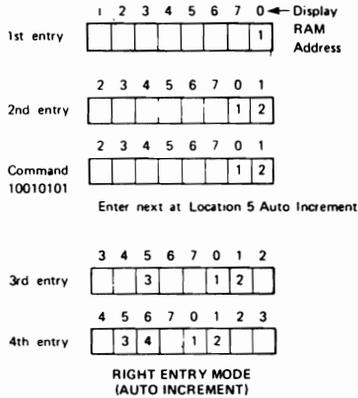
Starting at an arbitrary location operates as shown below:

Command 10010101

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | ← Display RAM Address |
| | | | | | | | |

Enter next at Location 5 Auto Increment

1st entry

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 |
| | | | | 1 | | | |

2nd entry

| 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 |
| | | | 1 | 2 | | | |

8th entry

| 4 | 5 | 6 | 7 | 8 | 1 | 2 | 3 |

9th entry

| 5 | 6 | 7 | 8 | 9 | 2 | 3 | 4 |

RIGHT ENTRY MODE
(AUTO INCREMENT)
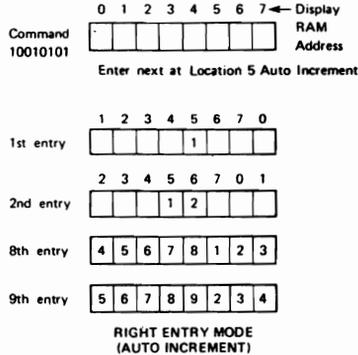
Entry appears to be from the initial entry point.

### 8/16 Character Display Formats

If the display mode is set to an 8 character display, the on duty-cycle is double what it would be for a 16 character display (e.g., 5.1 ms scan time for 8 characters vs. 10.3 ms for 16 characters with 100 kHz internal frequency).

### G. FIFO Status

FIFO status is used in the Keyboard and Strobed Input modes to indicate the number of characters in the FIFO and to indicate whether an error has occurred. There are two types of errors possible: overrun and underrun. Overrun occurs when the entry of another character into a full FIFO is attempted. Underrun occurs when the CPU tries to read an empty FIFO.

The FIFO status word also has a bit to indicate that the Display RAM was unavailable because a Clear Display or Clear All command had not completed its clearing operation.

In a Sensor Matrix mode, a bit is set in the FIFO status word to indicate that at least one sensor closure indication is contained in the Sensor RAM.

In Special Error Mode the S/E bit is showing the error flag and serves as an indication to whether a simultaneous multiple closure error has occurred.

FIFO STATUS WORD
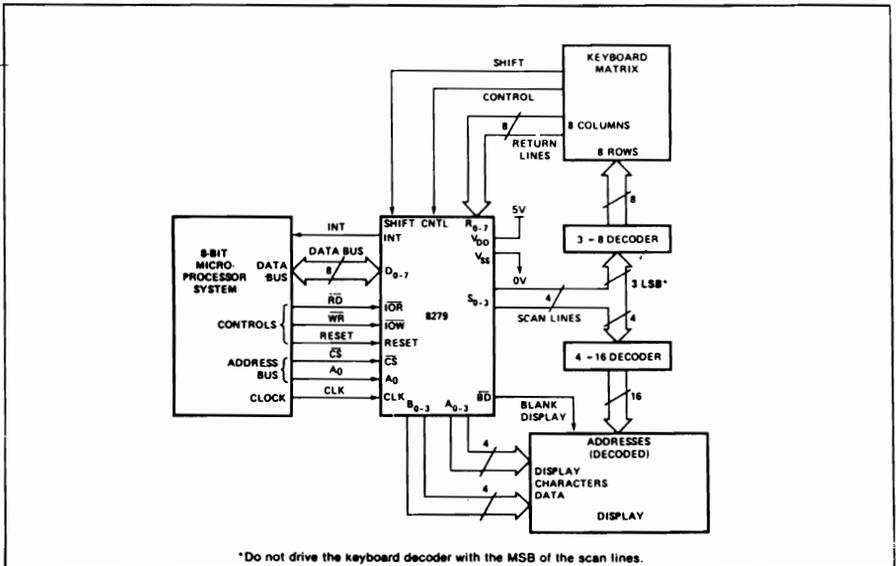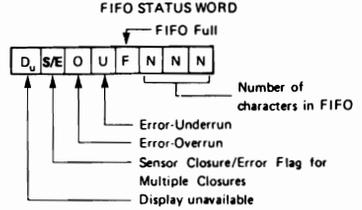


Figure 4. System Block Diagram

*Do not drive the keyboard decoder with the MSB of the scan lines.

# 8355/8355-2
# 16,384-BIT ROM WITH I/O

- **2048 Words × 8 Bits**
- **Single + 5V Power Supply**
- **Directly Compatible with 8085A and iAPX 88 Microprocessors**
- **2 General Purpose 8-Bit I/O Ports**

- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **Internal Address Latch**
- **40-Pin DIP**

The Intel® 8355 is a ROM and I/O chip to be used in the 8085A and iAPX 88 microprocessor systems. The ROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in the 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 lines and each I/O port line is individually programmable as input or output.

The 8355-2 has a 300 ns access time for compatibility with the 8085A-2 and 5 MHz iAPX 88 microprocessors.
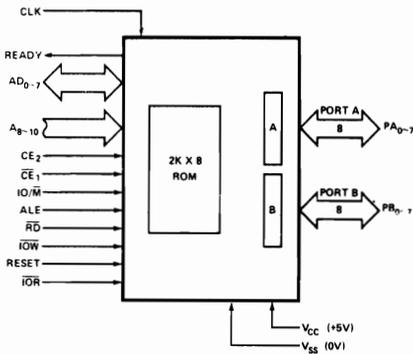


**Figure 1. Block Diagram**
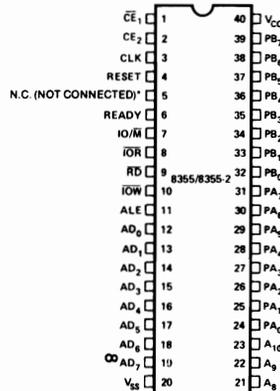


*For 8755A compatibility, pin 5 should be directly tied to VCC.

**Figure 2. Pin Configuration**

## FUNCTIONAL DESCRIPTION

### ROM Section

The 8355 contains an 8-bit address latch which allows it to interface directly to MCS-48. MCS-85, and iAPX 88/10 Microcomputers without additional hardware.

The ROM section of the chip is addressed by an 11-bit address and the Chip Enables. The address and levels on the Chip Enable pins are latched into the address latches on the falling edge of ALE. If the latched Chip Enables are active and IO/$\overline{\text{M}}$ is low when $\overline{\text{RD}}$ goes low, the contents of the ROM location addressed by the latched address are put out through AD$_{0-7}$ output buffers

### I/O Section

The I/O section of the chip is addressed by the latched value of AD$_{0-1}$. Two 8-bit Data Direction Registers DDR in 8355 determine the input/output status of each pin in the corresponding ports. A "0" in a particular bit position of a DDR signifies that the corresponding I/O port bit is in the input mode. A "1" in a particular bit position signifies that the corresponding I/O port bit is in the output mode. In this manner the I/O ports of the 8355 are bit-by-bit programmable as inputs or outputs. The table summarizes port and DDR designation. DDR's cannot be read.

| AD$_1$ | AD$_0$ | Selection |
|---|---|---|
| 0 | 0 | Port A |
| 0 | 1 | Port B |
| 1 | 0 | Port A Data Direction Register DDR A |
| 1 | 1 | Port B Data Direction Register DDR B |

When $\overline{\text{IOW}}$ goes low and the Chip Enables are active, the data on the AD$_{0-7}$ is written into I/O port selected by the latched value of AD$_{0-1}$. During this operation all I/O bits of the selected port are affected, regardless of their I/O mode and the state of IO/$\overline{\text{M}}$ The actual output level does not change until $\overline{\text{IOW}}$ returns high glitch free output

A port can be read out when the latched Chip Enables are active and either $\overline{\text{RD}}$ goes low with IO/$\overline{\text{M}}$ high, or $\overline{\text{IOR}}$ goes low. Both input and output mode bits of a selected port will appear on lines AD$_{0-7}$.

To clarify the function of the I/O ports and Data Direction Registers, the following diagram shows the configuration of one bit of PORT A and DDR A. The same logic applies to PORT B and DDR B.

Note that hardware RESET or writing a zero to the DDR latch will cause the output latch's output buffer to be disabled, preventing the data in the output latch from being passed through to the pin. This is equivalent to putting the port in the input mode. Note also that the data can be written to the Output Latch even though the Output Buffer has been disabled. This enables a port to be initialized with a value prior to enabling the output.

The diagram also shows that the contents of PORT A and PORT B can be read even when the ports are configured as outputs.

WRITE PA (IOW 0) • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)
WRITE DDR A (IOW 0) • (CHIP ENABLES ACTIVE) • (DDR A ADDRESS SELECTED)
READ PA [(IO M 1) • RD 0) • (IOR 0) • (CHIP ENABLES ACTIVE) • (PORT A ADDRESS SELECTED)
NOTE WRITE PA IS NOT QUALIFIED BY IO/M
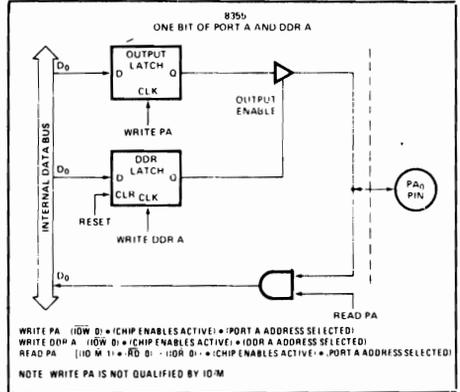
**Figure 3. 8355 One Bit of Port A and DDR A**

## SYSTEM APPLICATIONS

### System Interface with 8085A and iAPX 88

A system using the 8355 can use either one of the two I/O Interface techniques

- Standard I/O
- Memory Mapped I/O

If a standard I/O technique is used, the system can use the feature of both CE$_2$ and $\overline{\text{CE}}_1$. By using a combination of unused address lines A$_{11-15}$ and the Chip Enable inputs, the system can use up to 5 each 8355's without requiring a CE decoder. See Figure 5a and 5b.

If a memory mapped I/O approach is used the 8355 will be selected by the combination of both the Chip Enables and IO/$\overline{\text{M}}$ using AD$_{8-15}$ address lines. See Figure 4.
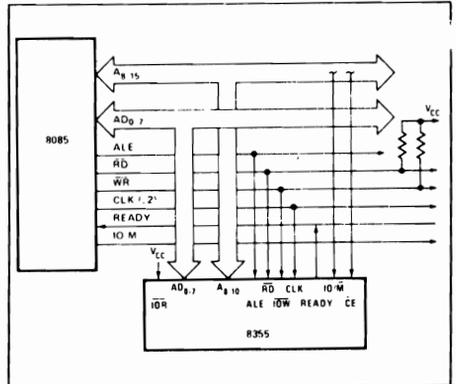


**Figure 4. 8355 in 8085A System (Memory-Mapped I/O)**

# 8755A/8755A-2
# 16,384-BIT EPROM WITH I/O

- **2048 Words × 8 Bits**

- **Single +5V Power Supply (V_CC)**

- **Directly Compatible with 8085A and 8088 Microprocessors**

- **U.V. Erasable and Electrically Reprogrammable**

- **Internal Address Latch**

- **2 General Purpose 8-Bit I/O Ports**

- **Each I/O Port Line Individually Programmable as Input or Output** `

- **Multiplexed Address and Data Bus**

- **40-Pin DIP**

- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**

The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the 8085A and iAPX 88 microprocessor systems. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

The 8755A-2 is a high speed selected version of the 8755A compatible with the 5 MHz 8085A-2 and the 5 MHz iAPX 88 microprocessor.



**Figure 1. Block Diagram**



**Figure 2. Pin Configuration**

331
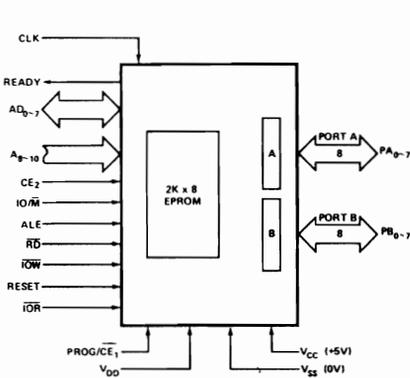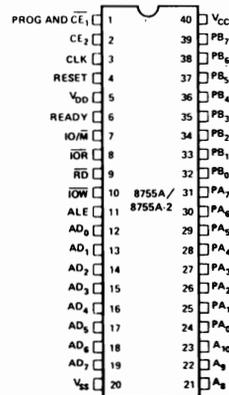
# 8282/8283
# OCTAL LATCH

- **Address Latch for iAPX 86, 88, 186, 188, MCS-80®, MCS-85®, MCS-48® Families**

- **High Output Drive Capability for Driving System Data Bus**

- **Fully Parallel 8-Bit Data Register and Buffer**

- **Transparent during Active Strobe**

- **3-State Outputs**

- **20-Pin Package with 0.3" Center**

- **No Output Low Noise when Entering or Leaving High Impedance State**

- **Available in EXPRESS**
  - **Standard Temperature Range**
  - **Extended Temperature Range**

The 8282 and 8283 are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers, or multiplexers. The 8283 inverts the input data at its outputs while the 8282 does not. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with these devices.
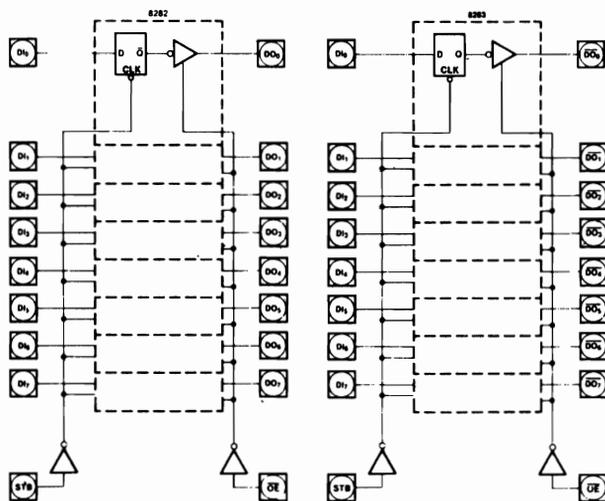
**Figure 1. Logic Diagrams**

**Figure 2. Pin Configurations**

# 8284A/8284A-1
# CLOCK GENERATOR AND DRIVER FOR
# iAPX 86, 88 PROCESSORS

- Generates the System Clock for the iAPX 86, 88 Processors:
  5 MHz, 8 MHz with 8284A
  10 MHz with 8284A-1
- Uses a Crystal or a TTL Signal for Frequency Source
- Provides Local READY and Multibus™ READY Synchronization
- 18-Pin Package

- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other 8284As
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range



8284A/8284A-1 Block Diagram

8284A/8284A-1 Pin Configuration
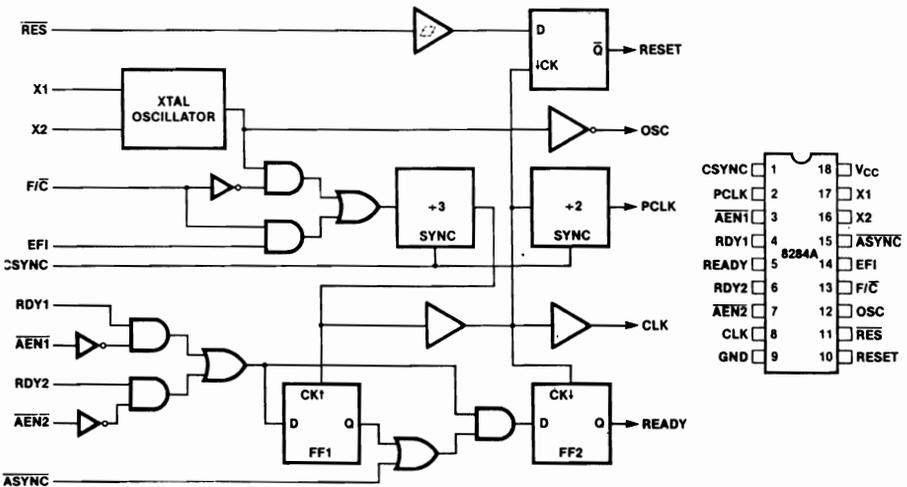
# 8286/8287
# OCTAL BUS TRANSCEIVER

- Data Bus Buffer Driver for iAPX 86,88,186,188, MCS-80™, MCS-85™, and MCS-48™ Families

- High Output Drive Capability for Driving System Data Bus

- Fully Parallel 8-Bit Transceivers

- 3-State Outputs

- 20-Pin Package with 0.3" Center

- No Output Low Noise when Entering or Leaving High Impedance State

- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The 8286 and 8287 are 8-bit bipolar transceivers with 3-state outputs. The 8287 inverts the input data at its outputs while the 8286 does not. Thus, a wide variety of applications for buffering in microcomputer systems can be met.
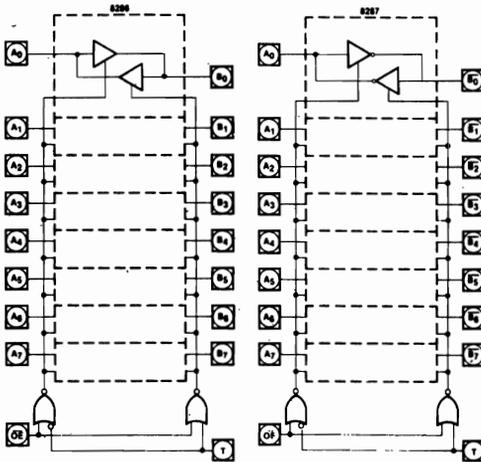


Figure 1. Logic Diagrams
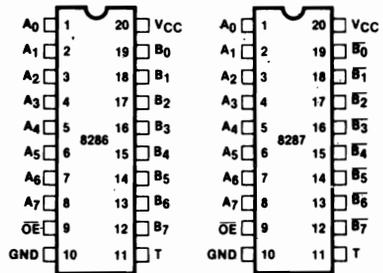


Figure 2. Pin Configurations

# 8288
# BUS CONTROLLER
# FOR iAPX 86, 88 PROCESSORS

- Bipolar Drive Capability
- Provides Advanced Commands
- Provides Wide Flexibility in System Configurations
- 3-State Command Output Drivers

- Configurable for Use with an I/O Bus
- Facilitates Interface to One or Two Multi-Master Busses
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8288 Bus Controller is a 20-pin bipolar component for use with medium-to-large iAPX 86, 88 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.
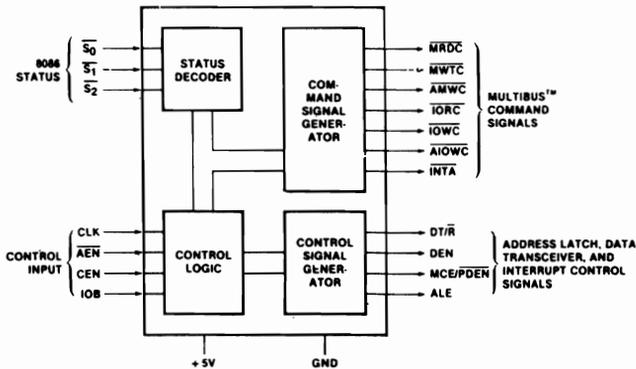


Figure 1. Block Diagram
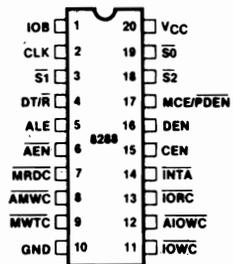


Figure 2.
Pin Configuration

# 8289
# BUS ARBITER

- Provides Multi-Master System Bus Protocol

- Synchronizes iAPX 86, 88 Processors with Multi-Master Bus

- Provides Simple Interface with 8288 Bus Controller

- Four Operating Modes for Flexible System Configuration

- Compatible with Intel Bus Standard MULTIBUS™

- Provides System Bus Arbitration for 8089 IOP in Remote Mode

- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel 8289 Bus Arbiter is a 20-pin, 5-volt-only bipolar component for use with medium to large iAPX 86, 88 multi-master/multiprocessing systems. The 8289 provides system bus arbitration for systems with multiple bus masters, such as an 8086 CPU with 8089 IOP in its REMOTE mode, while providing bipolar buffering and drive capability.
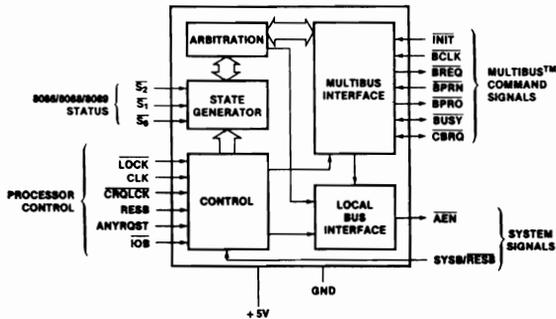


Figure 1. Block Diagram
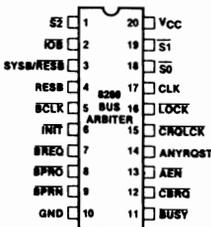


Figure 2. Pin Diagram
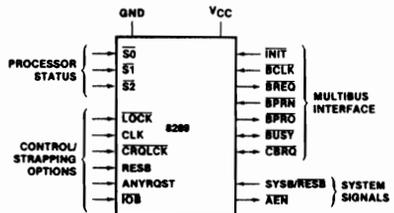
Figure 3. Functional Pinout

# 8291A
# GPIB TALKER/LISTENER

- Designed to Interface Microprocessors (e.g., 8048/49, 8051, 8080/85, 8086/88) to an IEEE Standard 488 Digital Interface Bus
- Programmable Data Transfer Rate
- Complete Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local Functions
- Selectable Interrupts
- On-Chip Primary and Secondary Address Recognition
- Automatic Handling of Addressing and Handshake Protocol
- Provision for Software Implementation of Additional Features

- 1–8 MHz Clock Range
- 16 Registers (8 Read, 8 Write), 2 for Data Transfer, the Rest for Interface Function Control, Status, etc.
- Directly Interfaces to External Non-Inverting Transceivers for Connection to the GPIB
- Provides Three Addressing Modes, Allowing the Chip to be Addressed Either as a Major or a Minor Talker/Listener with Primary or Secondary Addressing
- DMA Handshake Provision Allows for Bus Transfers without CPU Intervention
- Trigger Output Pin
- On-Chip EOS (End of Sequence) Message Recognition Facilitates Handling of Multi-Byte Transfers

The 8291A is an enhanced version of the 8291 GPIB Talker/Listener designed to interface microprocessors to an IEEE Standard 488 Instrumentation Interface Bus. It implements all of the Standard's interface functions except for the controller. The controller function can be added with the 8292 GPIB Controller, and the 8293 GPIB Transceiver performs the electrical interface for Talker/Listener and Talker/Listener/Controller configurations.
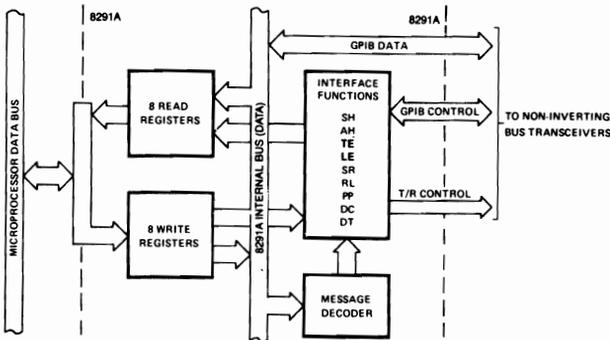


Figure 1. Block Diagram
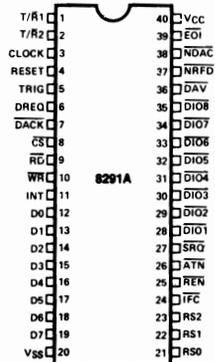


Figure 2. Pin Configuration

# 8292
# GPIB CONTROLLER

- **Complete IEEE Standard 488 Controller Function**

- **Interface Clear (IFC) Sending Capability Allows Seizure of Bus Control and/or Initialization of the Bus**

- **Responds to Service Requests (SRQ)**

- **Sends Remote Enable (REN), Allowing Instruments to Switch to Remote Control**

- **Complete Implementation of Transfer Control Protocol**

- **Synchronous Control Seizure Prevents the Destruction of Any Data Transmission in Progress**

- **Connects with the 8291 to Form a Complete IEEE Standard 488 Interface Talker/Listener/Controller**

The 8292 GPIB Controller is a microprocessor-controlled chip designed to function with the 8291 GPIB Talker/Listener to implement the full IEEE Standard 488 controller function, including transfer control protocol. The 8292 is a preprogrammed Intel® 8041A.
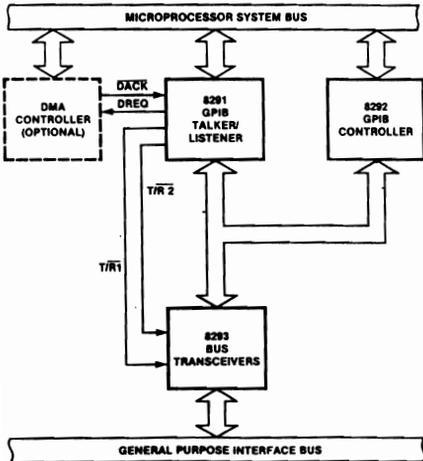


Figure 1. 8291, 8292 Block Diagram
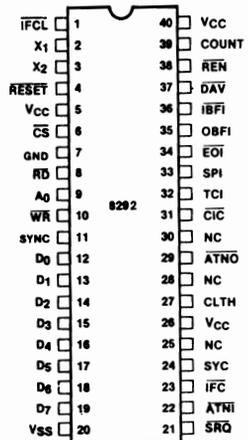


Figure 2. Pin Configuration

# 8293
# GPIB TRANSCEIVER

- Nine Open-collector or Three-state Line Drivers

- 48 mA Sink Current Capability on Each Line Driver

- Nine Schmitt-type Line Receivers

- High Capacitance Load Drive Capability

- Single 5V Power Supply

- 28-Pin Package

- Low Power HMOS Design

- On-chip Decoder for Mode Configuration

- Power Up/Power Down Protection to Prevent Disrupting the IEEE Bus

- Connects with the 8291A and 8292 to Form an IEEE Standard 488 Interface Talker/Listener/Controller with no Additional Components

- Only Two 8293's Required per GPIB Interface

- On-Chip IEEE-488 Bus Terminations

The Intel® 8293 GPIB Transceiver is a high-current, non-inverting buffer chip designed to interface the 8291A GPIB Talker/Listener, or the 8291A/8292 GPIB Talker/Listener/Controller combination, to the IEEE Standard 488-1978 Instrumentation Interface Bus. Each GPIB interface would contain two 8293 Bus Transceivers. In addition, the 8293 can also be used as a general-purpose bus driver.
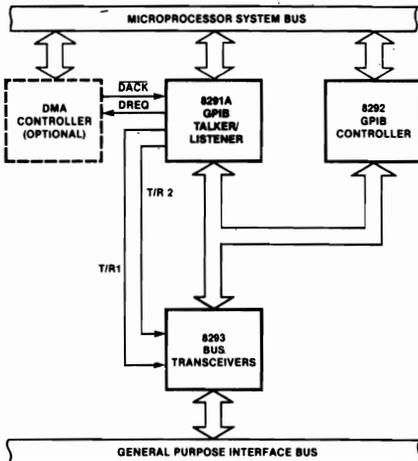


Figure 1. 8291A, 8292, 8293 Block Diagram
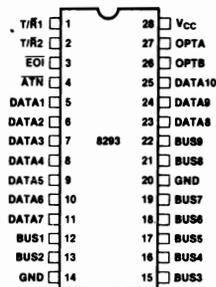


Figure 2. Pin Configuration

# 8294A
# DATA ENCRYPTION UNIT

- Certified by National Bureau of Standards

- 400 Byte/Sec Data Conversion Rate

- 64-Bit Data Encryption Using 56-Bit Key

- DMA Interface

- 3 Interrupt Outputs to Aid in Loading and Unloading Data

- 7-Bit User Output Port

- Single 5V ± 10% Power Supply

- Fully Compatible with iAPX-86,88, MCS-85™, MCS-80™, MCS-51™, and MCS-48™ Processors

- Implements Federal Information Processing Data Encryption Standard

- Encrypt and Decrypt Modes Available

The Intel® 8294A Data Encryption Unit (DEU) is a microprocessor peripheral device designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard. The DEU operates on 64-bit text words using a 56-bit user-specified key to produce 64-bit cipher words. The operation is reversible: if the cipher word is operated upon, the original text word is produced. The algorithm itself is permanently contained in the 8294A; however, the 56-bit key is user-defined and may be changed at any time.

The 56-bit key and 64-bit message data are transferred to and from the 8294A in 8-bit bytes by way of the system data bus. A DMA interface and three interrupt outputs are available to minimize software overhead associated with data transfer. Also, by using the DMA interface two or more DEUs may be operated in parallel to achieve effective system conversion rates which are virtually any multiple of 400 bytes/second. The 8294A also has a 7-bit TTL compatible output port for user-specified functions.

Because the 8294A implements the NBS encryption algorithm it can be used in a variety of Electronic Funds Transfer applications as well as other electronic banking and data handling applications where data must be encrypted.



Figure 1. Block Diagram



Figure 2. Pin Configuration

340
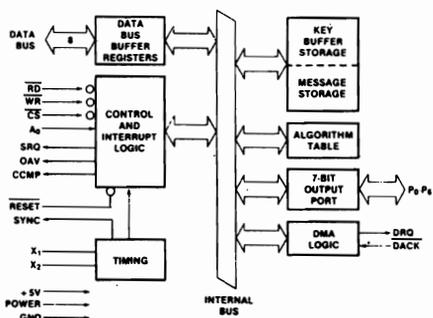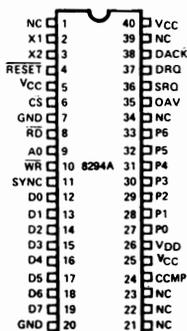
# 8295
# DOT MATRIX PRINTER CONTROLLER

- ■ **Interfaces Dot Matrix Printers to MCS-48™, MCS-80/85™, MCS-86™ Systems**
- ■ **40 Character Buffer On Chip**
- ■ **Serial or Parallel Communication with Host**
- ■ **DMA Transfer Capability**
- ■ **Programmable Character Density (10 or 12 Chararcters/Inch)**

- ■ **Programmable Print Intensity**
- ■ **Single or Double Width Printing**
- ■ **Programmable Multiple Line Feeds**
- ■ **3 Tabulations**
- ■ **2 General Purpose Outputs**

The Intel® 8295 Dot Matrix Printer Controller provides an interface for microprocessors to the LRC 7040 Series dot matrix impact printers. It may also be used as an interface to other similar printers.

The chip may be used in a serial or parallel communication mode with the host processor. In parallel mode, data transfers are based on polling, interrupts, or DMA. Furthermore, it provides internal buffering of up to 40 characters and contains a 7 × 7 matrix character generator accommodating 64 ASCII characters.
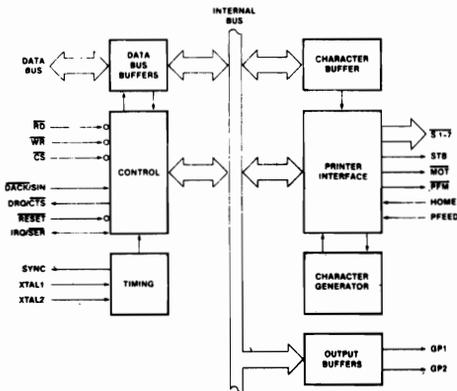


**Figure 1. Block Diagram**
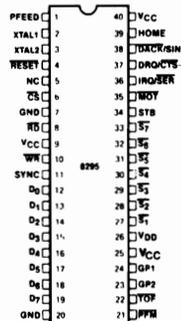
**Figure 2. Pin Configuration**

# 8041A/8641A/8741A
## UNIVERSAL PERIPHERAL INTERFACE
## 8-BIT MICROCOMPUTER

- **8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package**

- **One 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface**

- **DMA, Interrupt, or Polled Operation Supported**

- **1024 × 8 ROM/EPROM, 64 × 8 RAM, 8-Bit Timer/Counter, 18 Programmable I/O Pins**

- **Fully Compatible with All Microprocessor Families**

- **Interchangeable ROM and EPROM Versions**

- **3.6 MHz 8741A-8 Available**

- **Expandable I/O**

- **RAM Power-Down Capability**

- **Over 90 Instructions: 70% Single Byte**

- **Available in EXPRESS**
  **—Standard Temperature Range**
  **—Extended Temperature Range**

The Intel® 8041A/8741A is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS-48™, MCS-80™, MCS-85™, MCS-86™, and other 8-bit systems.

The UPI-41A™ has 1K words of program memory and 64 words of data memory on-chip. To allow full user flexibility the program memory is available as ROM in the 8041A version or as UV-erasable EPROM in the 8741A version. The 8741A and the 8041A are fully pin compatible for easy transition from prototype to production level designs. The 8641A is a one-time programmable (at the factory) 8741A which can be ordered as the first 25 pieces of a new 8041A order. The substitution of 8641A's for 8041A's allows for very fast turnaround for initial code verification and evaluation results.

The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8041A), single-step mode for debug (in the 8741A), and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

**PIN CONFIGURATION**       **BLOCK DIAGRAM**
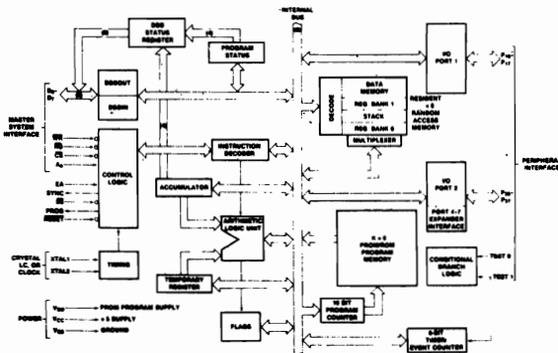
# 8048AH/8035AHL/8049AH
# 8039AHL/8050AH/8040AHL
# HMOS SINGLE-COMPONENT 8-BIT MICROCOMPUTER

- High Performance HMOS II
- Interval Timer/Event Counter
- Two Single Level Interrupts
- Single 5-Volt Supply
- Over 96 Instructions; 90% Single Byte

- Reduced Power Consumption
- Compatible with 8080/8085 Peripherals
- Easily Expandable Memory and I/O
- Up to 1.36 μSec Instruction Cycle
  All Instructions 1 or 2 cycles

The Intel MCS®-48 family are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

The family contains 27 I/O lines, an 8-bit timer/counter, and on-board oscillator/clock circuits. For systems that require extra capability, the family can be expanded using MCS³-80/MCS³-85 peripherals.

To minimize development problems and provide maximum flexibility, a logically and functionally pin-compatible version of the ROM devices with UV-erasable user-programmable EPROM program memory is available with minor differences.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

| Device | Internal Memory | | RAM Standby |
|--------|-----------------|---|-------------|
| 8050AH | 4K × 8 ROM | 256 × 8 RAM | yes |
| 8049AH | 2K × 8 ROM | 128 × 8 RAM | yes |
| 8048AH | 1K × 8 ROM | 64 × 8 RAM | yes |
| 8040AHL | none | 256 × 8 RAM | yes |
| 8039AHL | none | 128 × 8 RAM | yes |
| 8035AHL | none | 64 × 8 RAM | yes |
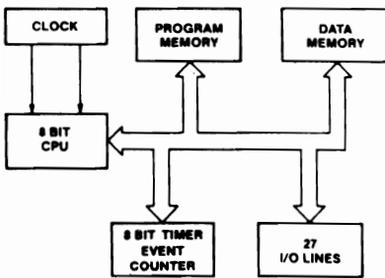


Figure 1.
Block Diagram
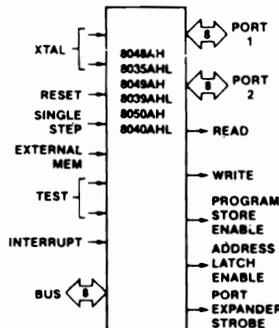
Figure 2.
Logic Symbol
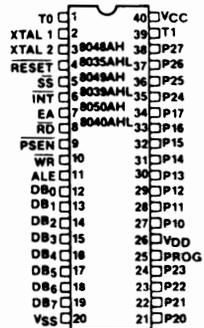
Figure 3.
Pin Configuration

## Table 1. Pin Description

| Symbol | Pin No. | Function |
|---|---|---|
| V$_{SS}$ | 20 | Circuit GND potential |
| V$_{DD}$ | 26 | +5V during normal operation. |
| | | Low power standby pin. |
| V$_{CC}$ | 40 | Main power supply; +5V during operation. |
| PROG | 25 | Output strobe for 8243 I/O expander. |
| P10-P17 Port 1 | 27-34 | 8-bit quasi-bidirectional port. |
| P20-P23 P24-P27 Port 2 | 21-24 35-38 | 8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243. |
| DB0-DB7 BUS | 12-19 | True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. |
| | | Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$. |
| T0 | 1 | Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction |
| T1 | 39 | Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction. |
| $\overline{INT}$ | 6 | Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) interrupt must remain low for at least 3 machine cycles for proper operation. |

| Symbol | Pin No. | Function |
|---|---|---|
| $\overline{RD}$ | 8 | Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. |
| | | Used as a read strobe to external data memory. (Active low) |
| $\overline{RESET}$ | 4 | Input which is used to initialize the processor. (Active low) (Non TTL V$_{IH}$) |
| | | Used during power down. |
| | | Used during ROM verification. |
| $\overline{WR}$ | 10 | Output strobe during a bus write. (Active low) |
| | | Used as write strobe to external data memory. |
| ALE | 11 | Address latch enable. This signal occurs once during each cycle and is useful as a clock output. |
| | | The negative edge of ALE strobes address into external data and program memory. |
| $\overline{PSEN}$ | 9 | Program store enable. This output occurs only during a fetch to external program memory. (Active low) |
| $\overline{SS}$ | 5 | Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active Low) |
| | | Used in sync mode |
| EA | 7 | External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug. (Active high) |
| | | Used during ROM verification (12V) |
| XTAL1 | 2 | One side of crystal input for internal oscillator. Also input for external source. (Non TTL V$_{IH}$) |
| XTAL2 | 3 | Other side of crystal input. |

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**Table 2. Instruction Set**

### Accumulator

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| ADD A, R | Add register to A | 1 | 1 |
| ADD A, @R | Add data memory to A | 1 | 1 |
| ADD A, # data | Add immediate to A | 2 | 2 |
| ADDC A, R | Add register with carry | 1 | 1 |
| ADDC A, @R | Add data memory with carry | 1 | 1 |
| ADDC A, # data | Add immediate with carry | 2 | 2 |
| ANL A, R | And register to A | 1 | 1 |
| ANL A, @R | And data memory to A | 1 | 1 |
| ANL A, # data | And immediate to A | 2 | 2 |
| ORL A, R | Or register to A | 1 | 1 |
| ORL A @R | Or data memory to A | 1 | 1 |
| ORL A, # data | Or immediate to A | 2 | 2 |
| XRL A, R | Exclusive or register to A | 1 | 1 |
| XRL A, @R | Exclusive or data memory to A | 1 | 1 |
| XRL, A, # data | Exclusive or immediate to A | 2 | 2 |
| INC A | Increment A | 1 | 1 |
| DEC A | Decrement A | 1 | 1 |
| CLR A | Clear A | 1 | 1 |
| CPL A | Complement A | 1 | 1 |
| DA A | Decimal adjust A | 1 | 1 |
| SWAP A | Swap nibbles of A | 1 | 1 |
| RL A | Rotate A left | 1 | 1 |
| RLC A | Rotate A left through carry | 1 | 1 |
| RR A | Rotate A right | 1 | 1 |
| RRC A | Rotate A right through carry | 1 | 1 |

### Input/Output

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| IN A, P | Input port to A | 1 | 2 |
| OUTL P, A | Output A to port | 1 | 2 |
| ANL P, # data | And immediate to port | 2 | 2 |
| ORL P, # data | Or immediate to port | 2 | 2 |
| INS A, BUS | Input BUS to A | 1 | 2 |
| OUTL BUS, A | Output A to BUS | 1 | 2 |
| ANL BUS, # data | And immediate to BUS | 2 | 2 |
| ORL BUS, # data | Or immediate to BUS | 2 | 2 |
| MOVD A, P | Input expander port to A | 1 | 2 |
| MOVD P, A | Output A to expander port | 1 | 2 |
| ANLD P, A | And A to expander port | 1 | 2 |
| ORLD P, A | Or A to expander port | 1 | 2 |

### Registers

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| INC R | Increment register | 1 | 1 |
| INC @R | Increment data memory | 1 | 1 |
| DEC R | Decrement register | 1 | 1 |

### Branch

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| JMP addr | Jump unconditional | 2 | 2 |
| JMPP @A | Jump indirect | 1 | 2 |
| DJNZ R, addr | Decrement register and skip | 2 | 2 |
| JC addr | Jump on carry = 1 | 2 | 2 |
| JNC addr | Jump on carry = 0 | 2 | 2 |
| JZ addr | Jump on A zero | 2 | 2 |
| JNZ addr | Jump on A not zero | 2 | 2 |
| JT0 addr | Jump on T0 = 1 | 2 | 2 |
| JNT0 addr | Jump on T0 = 0 | 2 | 2 |
| JT1 addr | Jump on T1 = 1 | 2 | 2 |
| JNT1 addr | Jump on T1 = 0 | 2 | 2 |
| JF0 addr | Jump on F0 = 1 | 2 | 2 |
| JF1 addr | Jump on F1 = 1 | 2 | 2 |
| JTF addr | Jump on timer flag | 2 | 2 |
| JNI addr | Jump on INT = 0 | 2 | 2 |
| JBb addr | Jump on accumulator bit | 2 | 2 |

### Subroutine

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| CALL addr | Jump to subroutine | 2 | 2 |
| RET | Return | 1 | 2 |
| RETR | Return and restore status | 1 | 2 |

### Flags

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| CLR C | Clear carry | 1 | 1 |
| CPL C | Complement carry | 1 | 1 |
| CLR F0 | Clear flag 0 | 1 | 1 |
| CPL F0 | Complement flag 0 | 1 | 1 |
| CLR F1 | Clear flag 1 | 1 | 1 |
| CPL F1 | Complement flag 1 | 1 | 1 |

## Table 2. Instruction Set (Continued)

**Data Moves**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| MOV A, R | Move register to A | 1 | 1 |
| MOV A, @R | Move data memory to A | 1 | 1 |
| MOV A, # data | Move immediate to A | 2 | 2 |
| MOV R, A | Move A to register | 1 | 1 |
| MOV @R, A | Move A to data memory | 1 | 1 |
| MOV R, # data | Move immediate to register | 2 | 2 |
| MOV @R, # data | Move immediate to data memory | 2 | 2 |
| MOV A, PSW | Move PSW to A | 1 | 1 |
| MOV PSW, A | Move A to PSW | 1 | 1 |
| XCH A, R | Exchange A and register | 1 | 1 |
| XCH A, @R | Exchange A and data memory | 1 | 1 |
| XCHD A, @R | Exchange nibble of A and register | 1 | 1 |
| MOVX A, @R | Move external data memory to A | 1 | 2 |
| MOVX @R, A | Move A to external data memory | 1 | 2 |
| MOVP A, @A | Move to A from current page | 1 | 2 |
| MOVP3 A, @ | Move to A from page 3 | 1 | 2 |

**Timer/Counter**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| MOV A, T | Read timer/counter | 1 | 1 |
| MOV T, A | Load timer/counter | 1 | 1 |
| STRT T | Start timer | 1 | 1 |
| STRT CNT | Start timer | 1 | 1 |
| STOP TCNT | Stop timer/counter | 1 | 1 |
| EN TCNTI | Enable timer/counter interrupt | 1 | 1 |
| DIS TCNTI | Disable timer/counter interrupt | 1 | 1 |

**Control**

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| EN I | Enable external interrupt | 1 | 1 |
| DIS I | Disable external interrupt | 1 | 1 |
| SEL RB0 | Select register bank 0 | 1 | 1 |
| SEL RB1 | Select register bank 1 | 1 | 1 |
| SEL MB0 | Select memory bank 0 | 1 | 1 |
| SEL MB1 | Select memory bank 1 | 1 | 1 |
| ENT0 CLK | Enable clock output on T0 | 1 | 1 |

| Mnemonic | Description | Bytes | Cycles |
|---|---|---|---|
| NOP | No operation | 1 | 1 |
| IDL | Select Idle Operation | 1 | 1 |

# MCS®-51
# 8-BIT CONTROL-ORIENTED MICROCOMPUTERS

8031/8051
8031AH/8051AH
8032AH/8052AH
8751H/8751H-12

- High Performance HMOS Process
- Internal Timers/Event Counters
- 2-Level Interrupt Priority Structure
- 32 I/O Lines (Four 8-Bit Ports)
- 64K Program Memory Space

- Boolean Processor
- Bit-Addressable RAM
- Programmable Full Duplex Serial Channel
- 111 Instructions (64 Single-Cycle)
- 64K Data Memory Space

- Security Feature Protects EPROM Parts Against Software Piracy

The MCS*-51 products are optimized for control applications. Byte-processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide in structions. Extensive on-chip support is provided for one-bit variables as a separate data type, allowing direct bit manipulation and testing in control and logic systems that require Boolean processing.

| Device | Internal Memory | | Timers/ Event Counters | Interrupts |
| | Program | Data | | |
|---|---|---|---|---|
| 8052AH | 8K × 8 ROM | 256 × 8 RAM | 3 × 16-Bit | 6 |
| 8051AH | 4K × 8 ROM | 128 × 8 RAM | 2 × 16-Bit | 5 |
| 8051 | 4K × 8 ROM | 128 × 8 RAM | 2 × 16-Bit | 5 |
| 8032AH | none | 256 × 8 RAM | 3 × 16-Bit | 6 |
| 8031AH | none | 128 × 8 RAM | 2 × 16-Bit | 5 |
| 8031 | none | 128 × 8 RAM | 2 × 16-Bit | 5 |
| 8751H | 4K × 8 EPROM | 128 × 8 RAM | 2 × 16-Bit | 5 |
| 8751H-12 | 4K × 8 EPROM | 128 × 8 RAM | 2 × 16-Bit | 5 |

The 8751H is an EPROM version of the 8051AH; that is, the on-chip Program Memory can be electrically programmed, and can be erased by exposure to ultraviolet light. It is fully compatible with its predecessor, the 8751-8, but incorporates two new features: a Program Memory Security bit that can be used to protect the EPROM against unauthorized read-out, and a programmable baud rate modification bit (SMOD). SMOD is not present in the 8751H-12.
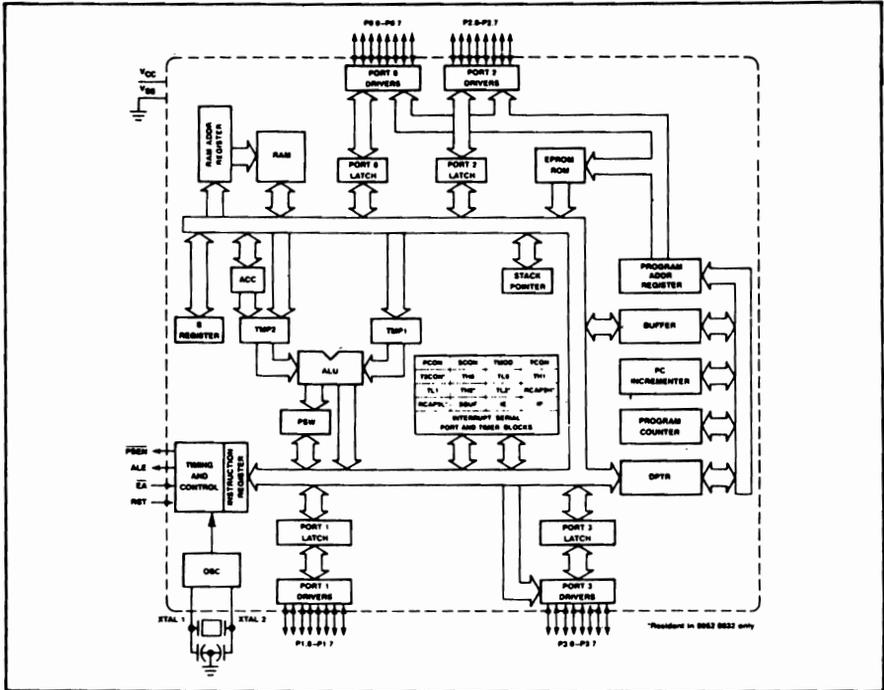
**Figure 1. MCS⁻-51 Block Diagram**

## PIN DESCRIPTIONS

### VCC

Supply voltage.

### VSS

Circuit ground.

### Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s, and can source and sink 8 LS TTL inputs.

Port 0 also receives the code bytes during programming of the EPROM parts, and outputs the code bytes during program verification of the ROM and EPROM parts. External pullups are required during program verification.

### Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source 4 LS TTL inputs. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs, As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during programming of the EPROM parts and during program verification of the ROM and EPROM parts.
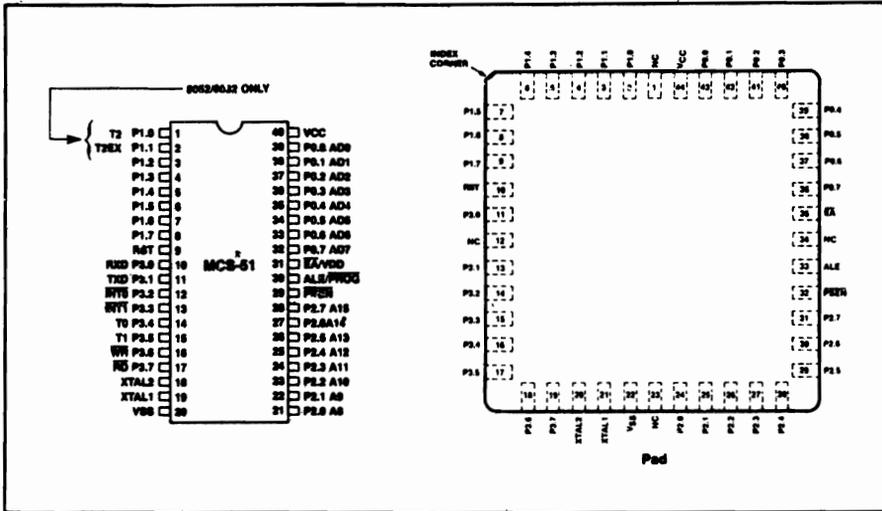
**Figure 2. MCS²-51 Pin Connections**

In the 8032AH and 8052AH, Port 1 pins P1.0 and P1.1 also serve the T2 and T2EX functions, respectively.

## Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits during programming of the EPROM parts and during program verification of the ROM and EPROM parts.

## Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

| Port Pin | Alternative Function |
|----------|---------------------|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | INT0 (external interrupt 0) |
| P3.3 | INT1 (external interrupt 1) |
| P3.4 | T0 (Timer 0 external input) |
| P3.5 | T1 (Timer 1 external input) |
| P3.6 | WR (external data memory write strobe) |
| P3.7 | RD (external data memory read strobe) |

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## RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

## ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. ALE can drive 8 LS TTL inputs. This pin is also the program pulse input (PROG) during programming of the EPROM parts.

In normal operation ALE is emitted at a constant rate of ⅙ the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

## PSEN

Program Store Enable is the read strobe to external Program Memory. PSEN can drive 8 LS TTL inputs.

When the device is executing code from external Program Memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external Data Memory.

## EA/VPP

External Access enable EA must be externally held low in order to enable any MCS-51 device to fetch code from external Program Memory locations 0 to 0FFFH (0 to 1FFFH, in the 8032AH and 8052AH).

Note, however, that if the Security Bit in the EPROM devices is programmed, the device will not fetch code from any location in external Program Memory.

This pin also receives the 21V programming supply voltage (VPP) during programming of the EPROM parts.

## XTAL1

Input to the inverting oscillator amplifier.

## XTAL2

Output from the inverting oscillator amplifier.

## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. Either a quartz crystal or ceramic resonator may be used. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillators for Microcontrollers."

To drive the device from an external clock source, XTAL1 should be grounded, while XTAL2 is driven, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

C1, C2 = 30 pF ± 10 pF FOR CRYSTALS
= 40 pF ± 10 pF FOR CERAMIC RESONATORS

**Figure 3. Oscillator Connections**

**Figure 4. External Drive Configuration**

# 8052AH-BASIC

- Full BASIC Interpreter in ROM on a Single Chip
- BCD Floating Point Math
- Generates All Timing Necessary to Program EPROMS and E2PROMS
- Fast Tokenized Interpreter
- "Stand Alone" Software Development
- All Arithmetic and Utility Routines Can Be Called From Assembly Language

- Interrupts Can Be Handled By BASIC or Assembly Language
- Built-In Accurate REAL TIME CLOCK
- Multiple User Programs
- Programs May Reside in RAM, EPROM or E2PROM
- Built in Radix Conversion — Hex to Decimal and Decimal to Hex

8052AH-BASIC is an 8052AH microcontroller with a complete full-featured BASIC interpreter, MCS® BASIC-52, resident in the 8K of available ROM. This Software-On-Silicon product is specifically designed to address the needs of process control, measurement, and instrumentation applications. MCS BASIC-52 allows 8052AH users to write programs in the popular BASIC language, which is much simpler to write and easier to understand than assembly language.

In addition to the standard BASIC commands and functions, such as floating point arithmetic and transcendental operations, MCS BASIC-52 contains many unique features that allow the user to perform tasks that usually require assembly language. Bit-wise logical operators, such as AND, OR. and EXCLUSIVE-OR are supported as well as hexadecimal arithmetic.

A minimum amount of hardware is required to support MCS BASIC-52. Small systems can be constructed with only a latch, 1K bytes of external memory, and the appropriate serial port drivers. With the addition of a transistor, a gate, and a couple of passive components, MCS BASIC-52 can program EPROM or E2PROM devices with the users application program. Both the standard and the int₀ligent Programming™ algorithms are supported.

MCS BASIC-52 is an interpreted language. This allows the user to develop a program interactively without the cumbersome and repetitive process of editing, assembling, loading, and running which is required by assemblers and compilers. MCS BASIC-52 was designed to permit the programmer to develop resident high level language software using the high performance 8052AH device.



System Block Diagram

# FEATURES

## COMMAND SET

MCS BASIC-52 contains all standard BASIC commands, statements, and operators. Figure 1 list the software feature set of MCS BASIC-52.

## DATA FORMAT

The range of numbers that can be represented in MCS BASIC-52 is:

$$\pm 1E - 127 \text{ to } \pm .99999999E + 127$$

## CONTROL ORIENTED FEATURES

MCS BASIC-52 contains many unique features to perform task that usually require assembly language programming. The XBY and DBY operators can read and/or write external and internal memory respectively. The CBY operator is used to read program memory. Additionally, virtually all of the special function registers on the 8052AH can be accessed with MCS BASIC-52. This allows the user to set the timer or interrupt modes within the constructs of a BASIC program. An accurate interrupt driven REAL TIME CLOCK that has a 5 millisecond resolution is also implemented in MCS BASIC-52. This clock can be enabled, disabled, and used to generate interrupts. Finally, a CALL statement that allows the programmer to CALL assembly language routines is available in MCS BASIC-52. Parameters can be passed in a number of different ways.

## EPROM/E2PROM FILE

Most Basic interpreters allow only one program to be resident in memory, and many require that the program reside in RAM. MCS BASIC-52 allows programs to reside in both RAM and EPROM/E2PROM. Additionally, up to 255 programs may reside in EPROM/E2PROM. Programs may also be transfered (XFER) from EPROM/E2PROM to RAM for editing purposes.

## EPROM/E2PROM PROGRAMMING

A powerful feature of MCS BASIC-52 is that it generates all of the timing necessary to program any standard EPROM or E2PROM device with the users' program (PROG/FPROG). Additionally, very little external hardware is required to implement this feature. Saving programs in EPROM/E2PROM is much more attractive and reliable than other alternatives, such as cassette tape, especially in control and/or other noisy environments.

## AUTOSTART

After the user programs an EPROM or E2PROM with the desired BASIC program. The PROG2 or FPROG2 commands may be used to enable the unique AUTOSTART feature of MCS BASIC-52. When AUTOSTART is enabled, MCS BASIC-52 will execute the user program after RESET or a power-up condition. This permits the user to RUN a program without connecting the MCS BASIC-52 device to a console — a powerful feature for control environments.

## USER ACCESSABLE FUNCTION LIBRARY

Another unique feature of MCS BASIC-52 is that it contains a complete library of functions that can be accessed with assembly language. All floating point, radix conversion, and I/O routines contained in MCS BASIC-52 can be accessed with assembly language CALL instructions. These complex arithmetic routines can be used by the programmer in applications requiring the speed of assembly language, but also the complex arithmetics offered by BASIC.

## 8052AH-BASIC PIN DESCRIPTION (FIGURE 2)

8052AH-BASIC is an 8052AH device, however, MCS BASIC-52 assumes a particular hardware configuration. The following pin description outlines the pin functions defined by MCS BASIC-52.

## VSS

Circuit ground potential.

## VCC

Circuit supply voltage. 5 volts ± 10% relative to VSS.

## AD0–AD7

The multiplexed low-order address and data bus used during accesses to external memory. External pullup devices ($\sim 10K\ \Omega$) are required on these pins if the MCS BASIC-52 EPROM/E2PROM programming feature is used.

## A8–A15

The high order address bus used during accesses to external memory.

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| Commands | Statements | Operators |
|----------|-----------|-----------|
| RUN | BAUD | ADD ( + ) |
| LIST | CALL | DIVIDE (/) |
| LIST# | CLEAR | EXPONENTIATION (**) |
| NEW | CLEARS | MULTIPLY (*) |
| NULL | CLEARI | SUBTRACT ( − ) |
| RAM | CLOCK0 | LOGICAL AND (.AND.) |
| ROM | CLOCK1 | LOGICAL OR (.OR.) |
| XFER | DATA | LOGICAL X-OR (.XOR.) |
| PROG | READ | LOGICAL NOT |
| PROG1 | RESTORE | ABS ( ) |
| PROG2 | DIM | INT ( ) |
| FPROG | DO-WHILE | SGN ( ) |
| FPROG1 | DO-UNTIL | SQR ( ) |
| FPROG2 | END | RND |
| | FOR-TO-STEP | LOG ( ) |
| | NEXT | EXP ( ) |
| | GOSUB | SIN ( ) |
| | RETURN | COS ( ) |
| | GOTO | TAN ( ) |
| | ON-GOTO | ATN ( ) |
| | ON-GOSUB | =, >, > =, |
| | | <, < =, <> |
| | IF-THEN-ELSE | ASC ( ) |
| | INPUT | CHR ( ) |
| | LET | CBY ( ) |
| | ONERR | DBY ( ) |
| | ONEXT1 | XBY ( ) |
| | ONTIME | GET |
| | PRINT | IE |
| | PRINT# | IP |
| | PH0. | PORT1 |
| | PH0.# | PCON |
| | PH1 | RCAP2 |
| | PH1.# | T2CON |
| | PUSH | TCON |
| | POP | TMOD |
| | PWM | TIME |
| | REM | TIMER0 |
| | RET1 | TIMER1 |
| | STOP | TIMER2 |
| | STRING | TIME |
| | UI0 | XTAL |
| | UI1 | MTOP |
| | UO0 | LEN |
| | UO1 | FREE |
| | | PI |

**Figure 1. MCS® BASIC-52 Software Feature Set**

## PORT 1

A general purpose quasi-bidirectional 8-bit input/output port. The individual pins on PORT 1 all have alternate functions which may or may not be implemented by the user. The alternate functions are as follows:

## PORT 1.0 (T2)

Can be used as the trigger input to TIMER/COUNTER 2. A one (1) must be written to this port pin output latch in order for this function to operate. Details of
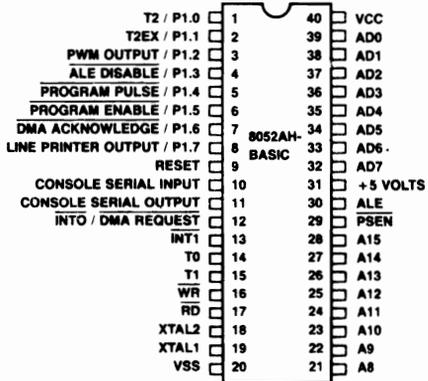


**Figure 2. Configuration**

the T2 trigger function are covered in the Microcontrollers Handbook. Order Number 210918-002.

## PORT 1.1 (T2EX)

Can be used as the external input to TIMER/COUNTER 2. A one (1) must be written to this port pin output latch in order for this function to operate. Details of the T2 trigger function are covered in the Microcontroller Users Manual.

## PORT 1.2 (PWM OUTPUT)

This pin is used as the PWM output port when the PWM statement is executed. PWM stands for Pulse Width Modulation and is used to generate pulses of varying duty cycle and frequency.

## PORT 1.3 (ALE DISABLE)

This pin is used to disable the ALE signal to the external address latch when the EPROM/E2PROM programming feature is used. In a system, this pin is logically anded with ALE.

## PORT 1.4 (PROGRAMMING PULSE)

When the EPROM/E2PROM programming feature is used, this pin provides the proper programming pulse width to program EPROM and INTELligent EPROM® devices. MCS BASIC-52 actually calculates the proper programming pulse width from the system crystal value (XTAL) to assure the proper timing of this pulse. When used to program E2PROM devices, the length of this pulse is not critical. This pin is active in the logical zero (0) state

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## PORT 1.5 (PROGRAMMING ENABLE)

When the EPROM/E$^2$PROM programming feature is implemented, this pin is used to enable the EPROM programming voltage. This pin remains active (logically low (0)) during the entire EPROM programming process. On E$^2$PROM devices that do not require any special programming voltage, this pin is not used.

## PORT 1.6 (DMA ACKNOWLEDGE)

When the DMA feature is implemented as described in the MCS* BASIC-52 users manual, this pin functions as an active low DMA ACKNOWLEDGE output.

## PORT 1.7 (LINE PRINTER OUTPUT)

This pin functions as a serial output port when the LIST# or PRINT# command and/or statement is used. This enables the user to make a "hard copy" of a program or to print out results of a calculation.

## RESET

A high (2.5 volts) on this pin for two machine cycles while the oscillator is running resets the device. An external pulldown resistor (~8.2K) from RESET to VSS permits power-on reset when a capacitor (~10 uf) is connected from this pin to VCC.

## ALE

ALE (address latch enable) is an output pin that is used to latch the low order address byte during Read, Write, or program fetch operations to external memory.

## PSEN

This pin (Program Store ENable) is a control signal that is used to enable external program memory. In MCS® BASIC-52, this pin will always remain inactive (logically high (1)) unless the user is running an assembly language program in external memory.

## XTAL1

Input to the inverting amplifier that forms the oscillator.

## XTAL2

Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator signal when an external oscillator is used.

## RD

A control signal that is used to enable READ operations to external data memory. This pin is active low (0).

## WR

A control signal that is used to enable WRITE operations to external data memory. This pin is active low (0).

## T1

This pin can be programmed to be an external input to TIMER/COUNTER 1.

## T0

This pin can be programmed to be an external input to TIMER/COUNTER 0.

## INT1

This pin is the external interrupt 1 pin. It is active low and interrupts on this pin may be handled in either BASIC or in assembly language.

## INT0/DMA REQUEST

This is the external interrupt 0 pin. It is active low and may be optionally programmed to function as a DMA request input pin. The DMA REQUEST pin is used by E$^2$PROM devices during programming.

## CONSOLE SERIAL OUTPUT

This is the serial output pin to the console device. Standard ASCII codes are used as well as a standard asynchronous frame.

## CONSOLE SERIAL INPUT

This is the serial input pin that receives data from the console device. Standard ASCII codes are assumed to be the input and the data is assumed to be transmitted using a standard asynchronous frame.

## NOTES

If pin 31 is grounded the 8052AH-BASIC will operate as a standard 8032AH. The tolerances on this pin are described under DC characteristics.

For detailed information concerning this product please refer to the MCS BASIC-52 Users Manual (Order Number 210918-002).

# 8094/8095/8096/8097
# 8394/8395/8396/8397
# 16-BIT MICROCONTROLLERS

- **839X: an 809X with 8K Bytes of On-chip ROM**

| | |
|---|---|
| ■ **High Speed Pulse I/O** | ■ **232 Byte Register File** |
| ■ **10-bit A/D Converter** | ■ **Memory-to-Memory Architecture** |
| ■ **8 Interrupt Sources** | ■ **Full Duplex Serial Port** |
| ■ **Pulse-Width Modulated Output** | ■ **Five 8-bit I/O Ports** |
| ■ **Four 16-bit Software Timers** | ■ **Watchdog Timer** |

The MCS-96 family of 16-bit microcontrollers consists of 8 members, all of which are designed for high-speed control functions.

The CPU supports bit, byte, and word operations. 32-bit double-words are supported for a subset of the instruction set. With a 12 MHz input frequency the 8096 can do a 16-bit addition in 1.0 $\mu$sec and a 16 x 16-bit multiply or 32/16-bit divide in 6.5 $\mu$sec. Instruction execution times average 1 to 2 $\mu$sec in typical applications.

Four high-speed trigger inputs are provided to record the times at which external events occur. Six high-speed pulse generator outputs are provided to trigger external events at preset times. The high-speed output unit can simultaneously perform timer functions. Up to four such 16-bit Software Timers can be in operation at once.

An on-chip A/D Converter converts up to 4 (in the 48-pin version) or 8 (in the 68-pin version) analog input channels to 10-bit digital values. This feature is only available on the 8095, 8395, 8097 and 8397

Also provided on-chip are a serial port, a watchdog timer, and a pulse-width modulated output signal.



**Figure 1. Block Diagram** (For simplicity, lines connecting port registers to port buffers are not shown.)

**Figure 2. 48-Pin Package**

Figure 1 shows a block diagram of the MCS-96 parts, generally referred to as the 8096. The 8096 is available in 48-pin and 68-pin packages, with and without A/D, and with and without on-chip ROM. The MCS-96 numbering system is shown below:

| OPTIONS | | 68 PIN | 48 PIN |
|---|---|---|---|
| DIGITAL I/O | ROMLESS | 8096 | 8094 |
| | ROM | 8396 | 8394 |
| ANALOG AND DIGITAL I/O | ROMLESS | 8097 | 8095 |
| | ROM | 8397 | 8395 |

Figures 2, 3 & 4 show the pinouts for the 48- and 68-pin packages. The 48-pin version is offered in Dual-In-Line package while the 68-pin version comes in a Flat-pack and a Pin Grid Array.
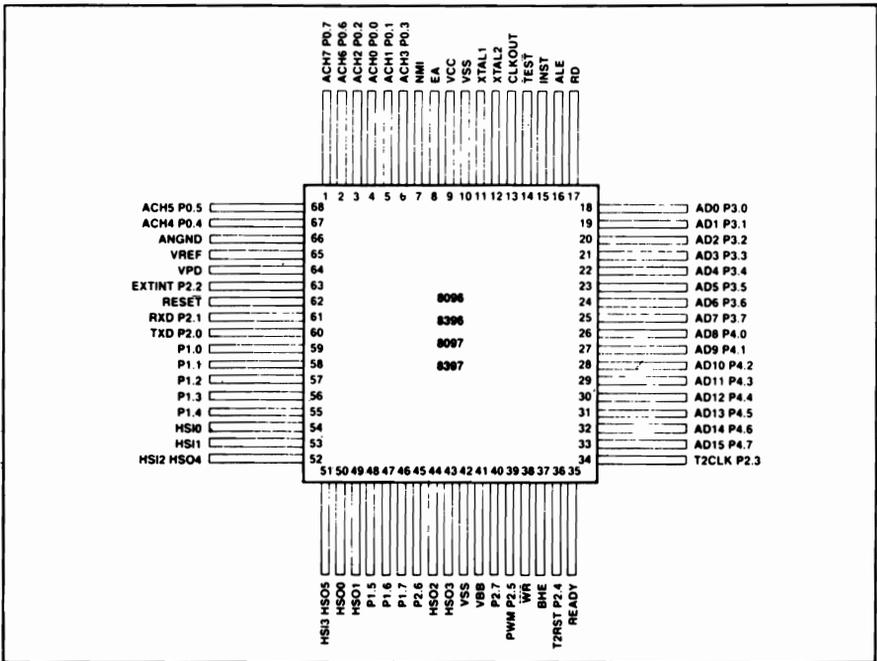


**Figure 3. 68-Pin Package (Flat Pack-Top View)**

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## 8-BIT MICROPROCESSING UNIT (MPU)

The MC6800 is a monolithic 8-bit microprocessor forming the central control function for Motorola's M6800 family. Compatible with TTL, the MC6800, as with all M6800 system parts, requires only one +5.0-volt power supply, and no external TTL devices for bus interface.

The MC6800 is capable of addressing 64K bytes of memory with its 16-bit address lines. The 8-bit data bus is bidirectional as well as three-state, making direct memory addressing and multiprocessing applications realizable.

- 8-Bit Parallel Processing
- Bidirectional Data Bus
- 16-Bit Address Bus — 64K Bytes of Addressing
- 72 Instructions — Variable Length
- Seven Addressing Modes — Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt — Internal Registers Saved in Stack
- Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Addressing (DMA) and Multiple Processor Capability
- Simplified Clocking Characteristics
- Clock Rates as High as 2.0 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

# MC6800

## MOS
(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

## MICROPROCESSOR

**S SUFFIX**
CERDIP PACKAGE
CASE 734

**P SUFFIX**
PLASTIC PACKAGE
CASE 711

**L SUFFIX**
CERAMIC PACKAGE
CASE 715

### ORDERING INFORMATION

| Package Type | Frequency (MHz) | Temperature | Order Number |
|---|---|---|---|
| Ceramic | 1.0 | 0°C to 70°C | MC6800L |
| L Suffix | 1.0 | −40°C to 85°C | MC6800CL |
| | 1.5 | 0°C to 70°C | MC68A00L |
| | 1.5 | −40°C to 85°C | MC68A00CL |
| | 2.0 | 0°C to 70°C | MC68B00L |
| Cerdip | 1.0 | 0°C to 70°C | MC6800S |
| S Suffix | 1.0 | −40°C to 85°C | MC6800CS |
| | 1.5 | 0°C to 70°C | MC68A00S |
| | 1.5 | −40°C to 85°C | MC68A00CS |
| | 2.0 | 0°C to 70°C | MC68B00S |
| Plastic | 1.0 | 0°C to 70°C | MC6800P |
| P Suffix | 1.0 | −40°C to 85°C | MC6800CP |
| | 1.5 | 0°C to 70°C | MC68A00P |
| | 1.5 | −40°C to 85°C | MC68A00CP |
| | 2.0 | 0°C to 70°C | MC68B00P |

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| VSS | 1 | 40 | RESET |
| HALT | 2 | 39 | TSC |
| $\phi1$ | 3 | 38 | N.C. |
| IRQ | 4 | 37 | $\phi2$ |
| VMA | 5 | 36 | DBE |
| NMI | 6 | 35 | N.C. |
| BA | 7 | 34 | R/W |
| VCC | 8 | 33 | D0 |
| A0 | 9 | 32 | D1 |
| A1 | 10 | 31 | D2 |
| A2 | 11 | 30 | D3 |
| A3 | 12 | 29 | D4 |
| A4 | 13 | 28 | D5 |
| A5 | 14 | 27 | D6 |
| A6 | 15 | 26 | D7 |
| A7 | 16 | 25 | A15 |
| A8 | 17 | 24 | A14 |
| A9 | 18 | 23 | A13 |
| A10 | 19 | 22 | A12 |
| A11 | 20 | 21 | VSS |

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# The 6800 Instruction Set

## Table B-1
### Accumulator and Memory Instructions

| OPERATIONS | MNEMONIC | IMMED OP ~ = | DIRECT OP ~ = | INDEX OP ~ = | EXTND OP ~ = | IMPLIED OP ~ = | BOOLEAN/ARITHMETIC OPERATION (All register labels refer to contents) | 5 H | 4 I | 3 N | 2 Z | 1 V | 0 C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Add | ADDA | 8B 2 2 | 9B 3 2 | AB 5 2 | BB 4 3 | | A + M → A | : | • | : | : | : | : |
| | ADDB | CB 2 2 | DB 3 2 | EB 5 2 | FB 4 3 | | B + M → B | : | • | : | : | : | : |
| Add Acmltrs | ABA | | | | | 1B 2 1 | A + B → A | : | • | : | : | : | : |
| Add with Carry | ADCA | 89 2 2 | 99 3 2 | A9 5 2 | B9 4 3 | | A + M + C → A | : | • | : | : | : | : |
| | ADCB | C9 2 2 | D9 3 2 | E9 5 2 | F9 4 3 | | B + M + C → B | : | • | : | : | : | : |
| And | ANDA | 84 2 2 | 94 3 2 | A4 5 2 | B4 4 3 | | A · M → A | • | • | : | : | R | • |
| | ANDB | C4 2 2 | D4 3 2 | E4 5 2 | F4 4 3 | | B · M → B | • | • | : | : | R | • |
| Bit Test | BITA | 85 2 2 | 95 3 2 | A5 5 2 | B5 4 3 | | A · M | • | • | : | : | R | • |
| | BITB | C5 2 2 | D5 3 2 | E5 5 2 | F5 4 3 | | B · M | • | • | : | : | R | • |
| Clear | CLR | | | 6F 7 2 | 7F 6 3 | | 00 → M | • | • | R | S | R | R |
| | CLRA | | | | | 4F 2 1 | 00 → A | • | • | R | S | R | R |
| | CLRB | | | | | 5F 2 1 | 00 → B | • | • | R | S | R | R |
| Compare | CMPA | 81 2 2 | 91 3 2 | A1 5 2 | B1 4 3 | | A − M | • | • | : | : | : | : |
| | CMPB | C1 2 2 | D1 3 2 | E1 5 2 | F1 4 3 | | B − M | • | • | : | : | : | : |
| Compare Acmltrs | CBA | | | | | 11 2 1 | A − B | • | • | : | : | : | : |
| Complement, 1's | COM | | | 63 7 2 | 73 6 3 | | M̄ → M | • | • | : | : | R | S |
| | COMA | | | | | 43 2 1 | Ā → A | • | • | : | : | R | S |
| | COMB | | | | | 53 2 1 | B̄ → B | • | • | : | : | R | S |
| Complement, 2's (Negate) | NEG | | | 60 7 2 | 70 6 3 | | 00 − M → M | • | • | : | : | ① | ② |
| | NEGA | | | | | 40 2 1 | 00 − A → A | • | • | : | : | ① | ② |
| | NEGB | | | | | 50 2 1 | 00 − B → B | • | • | : | : | ① | ② |
| Decimal Adjust, A | DAA | | | | | 19 2 1 | Converts Binary Add of BCD Characters into BCD Format | • | • | : | : | : | ③ |
| Decrement | DEC | | | 6A 7 2 | 7A 6 3 | | M − 1 → M | • | • | : | : | 4 | • |
| | DECA | | | | | 4A 2 1 | A − 1 → A | • | • | : | : | 4 | • |
| | DECB | | | | | 5A 2 1 | B − 1 → B | • | • | : | : | 4 | • |
| Exclusive OR | EORA | 88 2 2 | 98 3 2 | A8 5 2 | B8 4 3 | | A ⊕ M → A | • | • | : | : | R | • |
| | EORB | C8 2 2 | D8 3 2 | E8 5 2 | F8 4 3 | | B ⊕ M → B | • | • | : | : | R | • |
| Increment | INC | | | 6C 7 2 | 7C 6 3 | | M + 1 → M | • | • | : | : | ⑤ | • |
| | INCA | | | | | 4C 2 1 | A + 1 → A | • | • | : | : | ⑤ | • |
| | INCB | | | | | 5C 2 1 | B + 1 → B | • | • | : | : | ⑤ | • |
| Load Acmltr | LDAA | 86 2 2 | 96 3 2 | A6 5 2 | B6 4 3 | | M → A | • | • | : | : | R | • |
| | LDAB | C6 2 2 | D6 3 2 | E6 5 2 | F6 4 3 | | M → B | • | • | : | : | R | • |
| Or, Inclusive | ORAA | 8A 2 2 | 9A 3 2 | AA 5 2 | BA 4 3 | | A + M → A | • | • | : | : | R | • |
| | ORAB | CA 2 2 | DA 3 2 | EA 5 2 | FA 4 3 | | B + M → B | • | • | : | : | R | • |
| Push Data | PSHA | | | | | 36 4 1 | A → Msp SP − 1 → SP | • | • | • | • | • | • |
| | PSHB | | | | | 37 4 1 | B → Msp SP − 1 → SP | • | • | • | • | • | • |
| Pull Data | PULA | | | | | 32 4 1 | SP + 1 → SP, Msp → A | • | • | • | • | • | • |
| | PULB | | | | | 33 4 1 | SP + 1 → SP, Msp → B | • | • | • | • | • | • |
| Rotate Left | ROL | | | 69 7 2 | 79 6 3 | | M } | • | • | : | : | ⑥ | : |
| | ROLA | | | | | 49 2 1 | A } ←□←□□□□□□□□ | • | • | : | : | ⑥ | : |
| | ROLB | | | | | 59 2 1 | B } C b7 ─ b0 | • | • | : | : | ⑥ | : |
| Rotate Right | ROR | | | 66 7 2 | 76 6 3 | | M } | • | • | : | : | ⑥ | : |
| | RORA | | | | | 46 2 1 | A } □→□□□□□□□→□ | • | • | : | : | ⑥ | : |
| | RORB | | | | | 56 2 1 | B } C b7 ─ b0 | • | • | : | : | ⑥ | : |
| Shift Left, Arithmetic | ASL | | | 68 7 2 | 78 6 3 | | M } | • | • | : | : | ⑥ | : |
| | ASLA | | | | | 48 2 1 | A } □←□□□□□□□←0 | • | • | : | : | ⑥ | : |
| | ASLB | | | | | 58 2 1 | B } C b7 ─ b0 | • | • | : | : | ⑥ | : |
| Shift Right, Arithmetic | ASR | | | 67 7 2 | 77 6 3 | | M } | • | • | : | : | ⑥ | : |
| | ASRA | | | | | 47 2 1 | A } □□□□□□□□→□ | • | • | : | : | ⑥ | : |
| | ASRB | | | | | 57 2 1 | B } b7 ─ b0 C | • | • | : | : | ⑥ | : |
| Shift Right, Logic | LSR | | | 64 7 2 | 74 6 3 | | M } | • | • | R | : | ⑥ | : |
| | LSRA | | | | | 44 2 1 | A } 0→□□□□□□□→□ | • | • | R | : | ⑥ | : |
| | LSRB | | | | | 54 2 1 | B } b7 ─ b0 C | • | • | R | : | ⑥ | : |
| Store Acmltr | STAA | | 97 4 2 | A7 6 2 | B7 5 3 | | A → M | • | • | : | : | R | • |
| | STAB | | D7 4 2 | E7 6 2 | F7 5 3 | | B → M | • | • | : | : | R | • |
| Subtract | SUBA | 80 2 2 | 90 3 2 | A0 5 2 | B0 4 3 | | A − M → A | • | • | : | : | : | : |
| | SUBB | C0 2 2 | D0 3 2 | E0 5 2 | F0 4 3 | | B − M → B | • | • | : | : | : | : |
| Subtract Acmltrs | SBA | | | | | 10 2 1 | A − B → A | • | • | : | : | : | : |
| Subtr with Carry | SBCA | 82 2 2 | 92 3 2 | A2 5 2 | B2 4 3 | | A − M − C → A | • | • | : | : | : | : |
| | SBCB | C2 2 2 | D2 3 2 | E2 5 2 | F2 4 3 | | B − M − C → B | • | • | : | : | : | : |
| Transfer Acmltrs | TAB | | | | | 16 2 1 | A → B | • | • | : | : | R | • |
| | TBA | | | | | 17 2 1 | B → A | • | • | : | : | R | • |
| Test, Zero or Minus | TST | | | 6D 7 2 | 7D 6 3 | | M − 00 | • | • | : | : | R | R |
| | TSTA | | | | | 4D 2 1 | A − 00 | • | • | : | : | R | R |
| | TSTB | | | | | 5D 2 1 | B − 00 | • | • | : | : | R | R |
| | | | | | | | | H | I | N | Z | V | C |

LEGEND
OP Operation Code (Hexadecimal)
~ Number of MPU Cycles
= Number of Program Bytes
+ Arithmetic Plus
· Boolean AND
Msp Contents of memory location pointed to be Stack Pointer

+ Boolean Inclusive OR
⊕ Boolean Exclusive OR
■ Complement of M
→ Transfer Into
0 Bit Zero
00 Byte Zero

CONDITION CODE SYMBOLS
H Half carry from bit 3;
I Interrupt mask
N Negative (sign bit)
Z Zero (byte)
V Overflow 2's complement
C Carry from bit 7
R Reset Always
S Set Always
: Test and set if true, cleared otherwise
• Not Affected

Note   Accumulator addressing mode instructions are included in the column for IMPLIED addressing

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## Table B-2
## Index Register and Stack Manipulation

| POINTER OPERATIONS | MNEMONIC | IMMED OP | ~ | = | DIRECT OP | ~ | = | INDEX OP | ~ | = | EXTND OP | ~ | = | IMPLIED OP | ~ | = | BOOLEAN/ARITHMETIC OPERATION | 5 H | 4 I | 3 N | 2 Z | 1 V | 0 C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Compare Index Reg | CPX | 8C | 3 | 3 | 9C | 4 | 2 | AC | 6 | 2 | BC | 5 | 1 | | | | $X_H - M, X_L - (M+1)$ | • | • | ⑦ | ⑦ | ⑧ | • |
| Decrement Index Reg | DEX | | | | | | | | | | | | | 09 | 4 | 1 | $X - 1 \cdot X$ | • | • | • | ⑦ | • | • |
| Decrement Stack Pntr | DES | | | | | | | | | | | | | 34 | 4 | 1 | $SP - 1 \cdot SP$ | • | • | • | • | • | • |
| Increment Index Reg | INX | | | | | | | | | | | | | 08 | 4 | 1 | $X + 1 \cdot X$ | • | • | • | ⑦ | • | • |
| Increment Stack Pntr | INS | | | | | | | | | | | | | 31 | 4 | 1 | $SP + 1 \cdot SP$ | • | • | • | • | • | • |
| Load Index Reg | LDX | CE | 3 | 3 | DE | 4 | 2 | EE | 6 | 2 | FE | 5 | 3 | | | | $M \cdot X_H, (M+1) \cdot X_L$ | • | • | ⑨ | • | R | • |
| Load Stack Pntr | LDS | 8E | 3 | 3 | 9E | 4 | 2 | AE | 6 | 2 | BE | 5 | 3 | | | | $M \cdot SP_H, (M+1) \cdot SP_L$ | • | • | ⑨ | • | R | • |
| Store Index Reg | STX | | | | DF | 5 | 2 | EF | 7 | 2 | FF | 6 | 3 | | | | $X_H - M, X_L - (M+1)$ | • | • | ⑨ | • | R | • |
| Store Stack Pntr | STS | | | | 9F | 5 | 2 | AF | 7 | 2 | BF | 6 | 3 | | | | $SP_H - M, SP_L - (M+1)$ | • | • | ⑨ | • | R | • |
| Indx Reg → Stack Pntr | TXS | | | | | | | | | | | | | 35 | 4 | 1 | $X - 1 \cdot SP$ | • | • | • | • | • | • |
| Stack Pntr → Indx Reg | TSX | | | | | | | | | | | | | 30 | 4 | 1 | $SP + 1 \cdot X$ | • | • | • | • | • | • |

| OPERATIONS | MNEMONIC | RELATIVE OP | ~ | = | INDEX OP | ~ | = | EXTND OP | ~ | = | IMPLIED OP | ~ | = | BRANCH TEST | 5 H | 4 I | 3 N | 2 Z | 1 V | 0 C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Branch Always | BRA | 20 | 4 | 2 | | | | | | | | | | None | • | • | • | • | • | • |
| Branch If Carry Clear | BCC | 24 | 4 | 2 | | | | | | | | | | $C = 0$ | • | • | • | • | • | • |
| Branch If Carry Set | BCS | 25 | 4 | 2 | | | | | | | | | | $C = 1$ | • | • | • | • | • | • |
| Branch If Zero | BEQ | 27 | 4 | 2 | | | | | | | | | | $Z = 1$ | • | • | • | • | • | • |
| Branch If Zero | BGE | 2C | 4 | 2 | | | | | | | | | | $N \odot V = 0$ | • | • | • | • | • | • |
| Branch If Zero | BGT | 2E | 4 | 2 | | | | | | | | | | $Z + (N \odot V) = 0$ | • | • | • | • | • | • |
| Branch If Higher | BHI | 22 | 4 | 2 | | | | | | | | | | $C + Z = 0$ | • | • | • | • | • | • |
| Branch If Zero | BLE | 2F | 4 | 2 | | | | | | | | | | $Z + (N \odot V) = 1$ | • | • | • | • | • | • |
| Branch If Lower Or Same | BLS | 23 | 4 | 2 | | | | | | | | | | $C + Z = 1$ | • | • | • | • | • | • |
| Branch If Zero | BLT | 2D | 4 | 2 | | | | | | | | | | $N \odot V = 1$ | • | • | • | • | • | • |
| Branch If Minus | BMI | 2B | 4 | 2 | | | | | | | | | | $N = 1$ | • | • | • | • | • | • |
| Branch If Not Equal Zero | BNE | 26 | 4 | 2 | | | | | | | | | | $Z = 0$ | • | • | • | • | • | • |
| Branch If Overflow Clear | BVC | 28 | 4 | 2 | | | | | | | | | | $V = 0$ | • | • | • | • | • | • |
| Branch If Overflow Set | BVS | 29 | 4 | 2 | | | | | | | | | | $V = 1$ | • | • | • | • | • | • |
| Branch If Plus | BPL | 2A | 4 | 2 | | | | | | | | | | $N = 0$ | • | • | • | • | • | • |
| Branch To Subroutine | BSR | 8D | 8 | 2 | | | | | | | | | | | • | • | • | • | • | • |
| Jump | JMP | | | | 6E | 4 | 2 | 7E | 3 | 3 | | | | See Special Operations | • | • | • | • | • | • |
| Jump To Subroutine | JSR | | | | AD | 8 | 2 | BD | 9 | 3 | | | | | • | • | • | • | • | • |
| No Operation | NOP | | | | | | | | | | 01 | 2 | 1 | Advances Prog Cntr Only | • | • | • | • | • | • |
| Return From Interrupt | RTI | | | | | | | | | | 3B | 10 | 1 | | | | | ⑩ | | |
| Return From Subroutine | RTS | | | | | | | | | | 39 | 5 | 1 | | • | • | • | • | • | • |
| Software Interrupt | SWI | | | | | | | | | | 3F | 12 | 1 | See Special Operations | • | • | • | • | • | • |
| Wait for Interrupt * | WAI | | | | | | | | | | 3E | 9 | 1 | | • | ⑪ | • | • | • | • |

*WAI puts Address Bus, R/W, and Data Bus in the three state mode while VMA is held low

## Table B-3
## Jump and Branch Instructions

| OPERATIONS | MNEMONIC | IMPLIED OP | ~ | = | BOOLEAN OPERATION | COND. CODE REG. 5 H | 4 I | 3 N | 2 Z | 1 V | 0 C |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear Carry | CLC | 0C | 2 | 1 | $0 \to C$ | • | • | • | • | • | R |
| Clear Interrupt Mask | CLI | 0E | 2 | 1 | $0 \to I$ | • | R | • | • | • | • |
| Clear Overflow | CLV | 0A | 2 | 1 | $0 \to V$ | • | • | • | • | R | • |
| Set Carry | SEC | 0D | 2 | 1 | $1 \to C$ | • | • | • | • | • | S |
| Set Interrupt Mask | SEI | 0F | 2 | 1 | $1 \to I$ | • | S | • | • | • | • |
| Set Overflow | SEV | 0B | 2 | 1 | $1 \to V$ | • | • | • | • | S | • |
| Acmltr A → CCR | TAP | 06 | 2 | 1 | $A \to CCR$ | | | | ⑫ | | |
| CCR → Acmltr A | TPA | 07 | 2 | 1 | $CCR \to A$ | • | • | • | • | • | • |

**CONDITION CODE REGISTER NOTES:** (Bit set if test is true and cleared otherwise)

| | | | | | |
|---|---|---|---|---|---|
| 1 | (Bit V) | Test: Result = 10000000? | 7 | (Bit N) | Test Sign bit of most significant (MS) byte = 1? |
| 2 | (Bit C) | Test: Result = 00000000? | 8 | (Bit V) | Test: 2's complement overflow from subtraction of MS bytes? |
| 3 | (Bit C) | Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.) | 9 | (Bit N) | Test: Result less than zero? (Bit 15 = 1) |
| 4 | (Bit V) | Test: Operand = 10000000 prior to execution? | 10 | (All) | Load Condition Code Register from Stack. (See Special Operations) |
| 5 | (Bit V) | Test: Operand = 01111111 prior to execution? | 11 | (Bit I) | Set when interrupt occurs. If previously set, a Non-Maskable Interrupt is required to exit the wait state. |
| 6 | (Bit V) | Test: Set equal to result of N⊙C after shift has occurred | 12 | (All) | Set according to the contents of Accumulator A. |

# Table of Cycle by Cycle Operation for Each 6800 Instruction

Table 8 provides a detailed description of the information present on the Address Bus, Data Bus, Valid Memory Address line (VMA), and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to Addressing Mode and Number of Cycles per instruction. (In general, instructions with the same Addressing Mode and Number of Cycles execute in the same manner; exceptions are indicated in the table.)

**TABLE 8 – OPERATION SUMMARY**

| Address Mode and Instructions | Cycles | Cycle # | VMA Line | Address Bus | R/W Line | Data Bus |
|---|---|---|---|---|---|---|
| **IMMEDIATE** | | | | | | |
| ADC EOR ADD LDA AND ORA BIT SBC CMP SUB | 2 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Operand Data |
| CPX LDS LDX | 3 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Operand Data (High Order Byte) |
| | | 3 | 1 | Op Code Address + 2 | 1 | Operand Data (Low Order Byte) |
| **DIRECT** | | | | | | |
| ADC EOR ADD LDA AND ORA BIT SBC CMP SUB | 3 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Address of Operand |
| | | 3 | 1 | Address of Operand | 1 | Operand Data |
| CPX LDS LDX | 4 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Address of Operand |
| | | 3 | 1 | Address of Operand | 1 | Operand Data (High Order Byte) |
| | | 4 | 1 | Operand Address + 1 | 1 | Operand Data (Low Order Byte) |
| STA | 4 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Destination Address |
| | | 3 | 0 | Destination Address | 1 | Irrelevant Data (Note 1) |
| | | 4 | 1 | Destination Address | 0 | Data from Accumulator |
| STS STX | 5 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Address of Operand |
| | | 3 | 0 | Address of Operand | 1 | Irrelevant Data (Note 1) |
| | | 4 | 1 | Address of Operand | 0 | Register Data (High Order Byte) |
| | | 5 | 1 | Address of Operand + 1 | 0 | Register Data (Low Order Byte) |
| **INDEXED** | | | | | | |
| JMP | 4 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Offset |
| | | 3 | 0 | Index Register | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | Index Register Plus Offset (w/o Carry) | 1 | Irrelevant Data (Note 1) |
| ADC EOR ADD LDA AND ORA BIT SBC CMP SUB | 5 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Offset |
| | | 3 | 0 | Index Register | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | Index Register Plus Offset (w/o Carry) | 1 | Irrelevant Data (Note 1) |
| | | 5 | 1 | Index Register Plus Offset | 1 | Operand Data |
| CPX LDS LDX | 6 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Offset |
| | | 3 | 0 | Index Register | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | Index Register Plus Offset (w/o Carry) | 1 | Irrelevant Data (Note 1) |
| | | 5 | 1 | Index Register Plus Offset | 1 | Operand Data (High Order Byte) |
| | | 6 | 1 | Index Register Plus Offset + 1 | 1 | Operand Data (Low Order Byte) |

## TABLE OF CYCLE BY CYCLE OPERATION FOR EACH 6800 INSTRUCTION

| Address Mode and Instructions | Cycles | Cycle # | VMA Line | Address Bus | R/W Line | Data Bus |
|---|---|---|---|---|---|---|
| **INDEXED (Continued)** | | | | | | |
| STA | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Offset |
| | 6 | 3 | 0 | Index Register | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | Index Register Plus Offset (w/o Carry) | 1 | Irrelevant Data (Note 1) |
| | | 5 | 0 | Index Register Plus Offset | 1 | Irrelevant Data (Note 1) |
| | | 6 | 1 | Index Register Plus Offset | 0 | Operand Data |
| ASL  LSR<br>ASR  NEG<br>CLR  ROL<br>COM  ROR<br>DEC  TST<br>INC | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Offset |
| | 7 | 3 | 0 | Index Register | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | Index Register Plus Offset (w/o Carry) | 1 | Irrelevant Data (Note 1) |
| | | 5 | 1 | Index Register Plus Offset | 1 | Current Operand Data |
| | | 6 | 0 | Index Register Plus Offset | 1 | Irrelevant Data (Note 1) |
| | | 7 | 1/0 (Note 3) | Index Register Plus Offset | 0 | New Operand Data (Note 3) |
| STS<br>STX | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Offset |
| | 7 | 3 | 0 | Index Register | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | Index Register Plus Offset (w/o Carry) | 1 | Irrelevant Data (Note 1) |
| | | 5 | 0 | Index Register Plus Offset | 1 | Irrelevant Data (Note 1) |
| | | 6 | 1 | Index Register Plus Offset | 0 | Operand Data (High Order Byte) |
| | | 7 | 1 | Index Register Plus Offset + 1 | 0 | Operand Data (Low Order Byte) |
| JSR | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Offset |
| | | 3 | 0 | Index Register | 1 | Irrelevant Data (Note 1) |
| | 8 | 4 | 1 | Stack Pointer | 0 | Return Address (Low Order Byte) |
| | | 5 | 1 | Stack Pointer − 1 | 0 | Return Address (High Order Byte) |
| | | 6 | 0 | Stack Pointer − 2 | 1 | Irrelevant Data (Note 1) |
| | | 7 | 0 | Index Register | 1 | Irrelevant Data (Note 1) |
| | | 8 | 0 | Index Register Plus Offset (w/o Carry) | 1 | Irrelevant Data (Note 1) |
| **EXTENDED** | | | | | | |
| JMP | | 1 | 1 | Op Code Address | 1 | Op Code |
| | 3 | 2 | 1 | Op Code Address + 1 | 1 | Jump Address (High Order Byte) |
| | | 3 | 1 | Op Code Address + 2 | 1 | Jump Address (Low Order Byte) |
| ADC  EOR<br>ADD  LDA<br>AND  ORA<br>BIT  SBC<br>CMP  SUB | | 1 | 1 | Op Code Address | 1 | Op Code |
| | 4 | 2 | 1 | Op Code Address + 1 | 1 | Address of Operand (High Order Byte) |
| | | 3 | 1 | Op Code Address + 2 | 1 | Address of Operand (Low Order Byte) |
| | | 4 | 1 | Address of Operand | 1 | Operand Data |
| CPX<br>LDS<br>LDX | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Address of Operand (High Order Byte) |
| | 5 | 3 | 1 | Op Code Address + 2 | 1 | Address of Operand (Low Order Byte) |
| | | 4 | 1 | Address of Operand | 1 | Operand Data (High Order Byte) |
| | | 5 | 1 | Address of Operand + 1 | 1 | Operand Data (Low Order Byte) |
| STA A<br>STA B | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Destination Address (High Order Byte) |
| | 5 | 3 | 1 | Op Code Address + 2 | 1 | Destination Address (Low Order Byte) |
| | | 4 | 0 | Operand Destination Address | 1 | Irrelevant Data (Note 1) |
| | | 5 | 1 | Operand Destination Address | 0 | Data from Accumulator |
| ASL  LSR<br>ASR  NEG<br>CLR  ROL<br>COM  ROR<br>DEC  TST<br>INC | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Address of Operand (High Order Byte) |
| | 6 | 3 | 1 | Op Code Address + 2 | 1 | Address of Operand (Low Order Byte) |
| | | 4 | 1 | Address of Operand | 1 | Current Operand Data |
| | | 5 | 0 | Address of Operand | 1 | Irrelevant Data (Note 1) |
| | | 6 | 1/0 (Note 3) | Address of Operand | 0 | New Operand Data (Note 3) |

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| Address Mode and Instructions | Cycles | Cycle # | VMA Line | Address Bus | R/W Line | Data Bus |
|---|---|---|---|---|---|---|
| **EXTENDED (Continued)** | | | | | | |
| STS STX | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Address of Operand (High Order Byte) |
| | 6 | 3 | 1 | Op Code Address + 2 | 1 | Address of Operand (Low Order Byte) |
| | | 4 | 0 | Address of Operand | 1 | Irrelevant Data (Note 1) |
| | | 5 | 1 | Address of Operand | 0 | Operand Data (High Order Byte) |
| | | 6 | 1 | Address of Operand + 1 | 0 | Operand Data (Low Order Byte) |
| JSR | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Address of Subroutine (High Order Byte) |
| | | 3 | 1 | Op Code Address + 2 | 1 | Address of Subroutine (Low Order Byte) |
| | | 4 | 1 | Subroutine Starting Address | 1 | Op Code of Next Instruction |
| | 9 | 5 | 1 | Stack Pointer | 0 | Return Address (Low Order Byte) |
| | | 6 | 1 | Stack Pointer − 1 | 0 | Return Address (High Order Byte) |
| | | 7 | 0 | Stack Pointer − 2 | 1 | Irrelevant Data (Note 1) |
| | | 8 | 0 | Op Code Address + 2 | 1 | Irrelevant Data (Note 1) |
| | | 9 | 1 | Op Code Address + 2 | 1 | Address of Subroutine (Low Order Byte) |
| **INHERENT** | | | | | | |
| ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA | 2 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Op Code of Next Instruction |
| DES DEX INS INX | | 1 | 1 | Op Code Address | 1 | Op Code |
| | 4 | 2 | 1 | Op Code Address + 1 | 1 | Op Code of Next Instruction |
| | | 3 | 0 | Previous Register Contents | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | New Register Contents | 1 | Irrelevant Data (Note 1) |
| PSH | | 1 | 1 | Op Code Address | 1 | Op Code |
| | 4 | 2 | 1 | Op Code Address + 1 | 1 | Op Code of Next Instruction |
| | | 3 | 1 | Stack Pointer | 0 | Accumulator Data |
| | | 4 | 0 | Stack Pointer − 1 | 1 | Accumulator Data |
| PUL | | 1 | 1 | Op Code Address | 1 | Op Code |
| | 4 | 2 | 1 | Op Code Address + 1 | 1 | Op Code of Next Instruction |
| | | 3 | 0 | Stack Pointer | 1 | Irrelevant Data (Note 1) |
| | | 4 | 1 | Stack Pointer + 1 | 1 | Operand Data from Stack |
| TSX | | 1 | 1 | Op Code Address | 1 | Op Code |
| | 4 | 2 | 1 | Op Code Address + 1 | 1 | Op Code of Next Instruction |
| | | 3 | 0 | Stack Pointer | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | New Index Register | 1 | Irrelevant Data (Note 1) |
| TXS | | 1 | 1 | Op Code Address | 1 | Op Code |
| | 4 | 2 | 1 | Op Code Address + 1 | 1 | Op Code of Next Instruction |
| | | 3 | 0 | Index Register | 1 | Irrelevant Data |
| | | 4 | 0 | New Stack Pointer | 1 | Irrelevant Data |
| RTS | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Irrelevant Data (Note 2) |
| | 5 | 3 | 0 | Stack Pointer | 1 | Irrelevant Data (Note 1) |
| | | 4 | 1 | Stack Pointer + 1 | 1 | Address of Next Instruction (High Order Byte) |
| | | 5 | 1 | Stack Pointer + 2 | 1 | Address of Next Instruction (Low Order Byte) |

| Address Mode and Instructions | Cycles | Cycle # | VMA Line | Address Bus | R/W Line | Data Bus |
|---|---|---|---|---|---|---|
| **INHERENT (Continued)** | | | | | | |
| WAI | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Op Code of Next Instruction |
| | | 3 | 1 | Stack Pointer | 0 | Return Address (Low Order Byte) |
| | | 4 | 1 | Stack Pointer − 1 | 0 | Return Address (High Order Byte) |
| | 9 | 5 | 1 | Stack Pointer − 2 | 0 | Index Register (Low Order Byte) |
| | | 6 | 1 | Stack Pointer − 3 | 0 | Index Register (High Order Byte) |
| | | 7 | 1 | Stack Pointer − 4 | 0 | Contents of Accumulator A |
| | | 8 | 1 | Stack Pointer − 5 | 0 | Contents of Accumulator B |
| | | 9 | 1 | Stack Pointer − 6 (Note 4) | 1 | Contents of Cond. Code Register |
| RTI | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Irrelevant Data (Note 2) |
| | | 3 | 0 | Stack Pointer | 1 | Irrelevant Data (Note 1) |
| | | 4 | 1 | Stack Pointer + 1 | 1 | Contents of Cond. Code Register from Stack |
| | 10 | 5 | 1 | Stack Pointer + 2 | 1 | Contents of Accumulator B from Stack |
| | | 6 | 1 | Stack Pointer + 3 | 1 | Contents of Accumulator A from Stack |
| | | 7 | 1 | Stack Pointer + 4 | 1 | Index Register from Stack (High Order Byte) |
| | | 8 | 1 | Stack Pointer + 5 | 1 | Index Register from Stack (Low Order Byte) |
| | | 9 | 1 | Stack Pointer + 6 | 1 | Next Instruction Address from Stack (High Order Byte) |
| | | 10 | 1 | Stack Pointer + 7 | 1 | Next Instruction Address from Stack (Low Order Byte) |
| SWI | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Irrelevant Data (Note 1) |
| | | 3 | 1 | Stack Pointer | 0 | Return Address (Low Order Byte) |
| | | 4 | 1 | Stack Pointer − 1 | 0 | Return Address (High Order Byte) |
| | | 5 | 1 | Stack Pointer − 2 | 0 | Index Register (Low Order Byte) |
| | 12 | 6 | 1 | Stack Pointer − 3 | 0 | Index Register (High Order Byte) |
| | | 7 | 1 | Stack Pointer − 4 | 0 | Contents of Accumulator A |
| | | 8 | 1 | Stack Pointer − 5 | 0 | Contents of Accumulator B |
| | | 9 | 1 | Stack Pointer − 6 | 0 | Contents of Cond. Code Register |
| | | 10 | 0 | Stack Pointer − 7 | 1 | Irrelevant Data (Note 1) |
| | | 11 | 1 | Vector Address FFFA (Hex) | 1 | Address of Subroutine (High Order Byte) |
| | | 12 | 1 | Vector Address FFFB (Hex) | 1 | Address of Subroutine (Low Order Byte) |
| **RELATIVE** | | | | | | |
| BCC BHI BNE<br>BCS BLE BPL<br>BEQ BLS BRA<br>BGE BLT BVC<br>BGT BMI BVS | 4 | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Branch Offset |
| | | 3 | 0 | Op Code Address + 2 | 1 | Irrelevant Data (Note 1) |
| | | 4 | 0 | Branch Address | 1 | Irrelevant Data (Note 1) |
| BSR | | 1 | 1 | Op Code Address | 1 | Op Code |
| | | 2 | 1 | Op Code Address + 1 | 1 | Branch Offset |
| | | 3 | 0 | Return Address of Main Program | 1 | Irrelevant Data (Note 1) |
| | 8 | 4 | 1 | Stack Pointer | 0 | Return Address (Low Order Byte) |
| | | 5 | 1 | Stack Pointer − 1 | 0 | Return Address (High Order Byte) |
| | | 6 | 0 | Stack Pointer − 2 | 1 | Irrelevant Data (Note 1) |
| | | 7 | 0 | Return Address of Main Program | 1 | Irrelevant Data (Note 1) |
| | | 8 | 0 | Subroutine Address | 1 | Irrelevant Data (Note 1) |

Note 1    If device which is addressed during this cycle uses VMA, then the Data Bus will go to the high impedance three-state condition. Depending on bus capacitance, data from the previous cycle may be retained on the Data Bus.

Note 2.    Data is ignored by the MPU.

Note 3.    For TST, VMA = 0 and Operand data does not change.

Note 4    While the MPU is waiting for the interrupt, Bus Available will go high indicating the following states of the control lines: VMA is low, Address Bus, R/W, and Data Bus are all in the high impedance state.

# MC6801

## Advance Information

### MICROCOMPUTER UNIT (MCU)

The MC6801 MCU is an 8-bit microcomputer system which is compatible with the M6800 family of parts. The MC6801 MCU is object code compatible with the MC6800 with improved execution times of key instructions plus several new 16-bit and 8-bit instructions including an 8 X 8 unsigned multiply with 16-bit result. The MC6801 MCU can operate as a single chip microcomputer or be expanded to 65K words. The MC6801 MCU is TTL compatible and requires one +5.0 volt power supply. The MC6801 MCU has 2K bytes of ROM and 128 bytes of RAM on chip. Serial Communications Interface (S.C.I.), and parallel I/O as well as three function 16-bit timer. Block diagram is shown in Figure 1. Features of the MC6801 include the following:

- Expanded M6800 Instruction Set
- 8 X 8 Multiply
- On-Chip Serial Communications Interface (S.C.I.)
- Object Code Compatible With The MC6800 MPU
- 16-Bit Timer
- Single Chip Or Expandable To 65K Words
- 2K Bytes Of ROM
- 128 Bytes Of RAM (64 Bytes Retainable On Power Down)
- 31 Parallel I/O Lines
- Internal Clock/Divided-By-Four
- TTL Compatible Inputs And Outputs
- Interrupt Capability
- External Clock/Divide-By-One Mask Option (MC6801E) And EPROM Versions MC68701 And MC68701E Available Soon.

## MOS

(N-CHANNEL, SILICON-GATE
DEPLETION LOAD)

### MICROCOMPUTER



L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711

### FIGURE 1 - SINGLE-CHIP MICROCOMPUTER BLOCK DIAGRAM
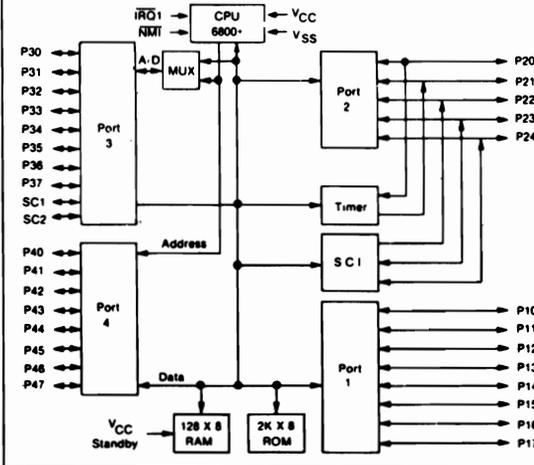


### FIGURE 2 — PIN ASSIGNMENT
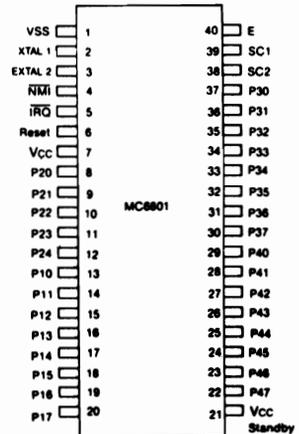


This is advance information and specifications are subject to change without notice.

## Advance Information

### MICROPROCESSOR WITH CLOCK AND RAM

The MC6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present MC6800 plus an internal clock oscillator and driver on the same chip. In addition, the MC6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007F. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing $V_{CC}$ standby, thus facilitating memory retention during a power-down situation.

The MC6802 is completely software compatible with the MC6800 as well as the entire M6800 family of parts. Hence, the MC6802 is expandable to 65K words.

- On-Chip Clock Circuit
- 128 x 8 Bit On-Chip RAM
- 32 Bytes of RAM Are Retainable
- Software-Compatible with the MC6800
- Expandable to 65K words
- Standard TTL-Compatible Inputs and Outputs
- 8 Bit Word Size
- 16 Bit Memory Addressing
- Interrupt Capability

**MOS**

(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

**MICROPROCESSOR WITH CLOCK AND RAM**

L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711-03

FIGURE 1 — TYPICAL MICROCOMPUTER
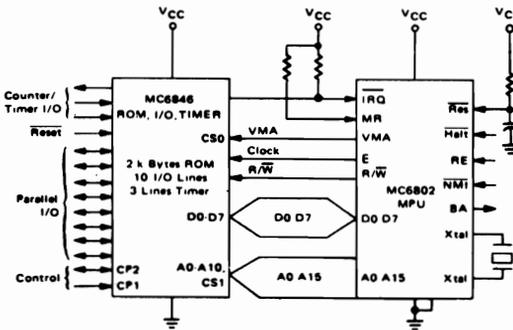


Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the M6800 Microcomputer family.

This is advance information and specifications are subject to change without notice.

**PIN ASSIGNMENT**

| | | | | |
|---|---|---|---|---|
| 1 | Vss | | Reset | 40 |
| 2 | Halt | | EXtal | 39 |
| 3 | MR | | Xtal | 38 |
| 4 | IRQ | | E | 37 |
| 5 | VMA | | RE | 36 |
| 6 | NMI | | Vcc Standby | 35 |
| 7 | BA | | R/W | 34 |
| 8 | Vcc | | D0 | 33 |
| 9 | A0 | | D1 | 32 |
| 10 | A1 | | D2 | 31 |
| 11 | A2 | | D3 | 30 |
| 12 | A3 | | D4 | 29 |
| 13 | A4 | | D5 | 28 |
| 14 | A5 | | D6 | 27 |
| 15 | A6 | | D7 | 26 |
| 16 | A7 | | A15 | 25 |
| 17 | A8 | | A14 | 24 |
| 18 | A9 | | A13 | 23 |
| 19 | A10 | | A12 | 22 |
| 20 | A11 | | Vss | 21 |

# MC6809

## 8-BIT MICROPROCESSING UNIT

The MC6809 is a revolutionary high-performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the M6800 Family has major architectural improvements which include additional registers, instructions, and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The MC6809 has the most complete set of addressing modes available on any 8-bit microprocessor today.

The MC6809 has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications.

### MC6800 COMPATIBLE
- Hardware — Interfaces with All M6800 Peripherals
- Software — Upward Source Code Compatible Instruction Set and Addressing Modes

### ARCHITECTURAL FEATURES
- Two 16-Bit Index Registers
- Two 16-Bit Indexable Stack Pointers
- Two 8-Bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

### HARDWARE FEATURES
- On-Chip Oscillator (Crystal Frequency = 4 × E)
- DMA/BREQ Allows DMA Operation on Memory Refresh
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- MRDY Input Extends Data Access Times for Use with Slow Memory
- Interrupt Acknowledge Output Allows Vectoring by Devices
- Sync Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle RESET
- Single 5-Volt Supply Operation
- NMI Inhibited After RESET Until After First Load of Stack Pointer
- Early Address Valid Allows Use with Slower Memories
- Early Write Data for Dynamic Memories

### SOFTWARE FEATURES
- 10 Addressing Modes
  - 6800 Upward Compatible Addressing Modes
  - Direct Addressing Anywhere in Memory Map
  - Long Relative Branches
  - Program Counter Relative
  - True Indirect Addressing
  - Expanded Indexed Addressing:
    - 0-, 5-, 8-, or 16-Bit Constant Offsets
    - 8- or 16-Bit Accumulator Offsets
    - Auto Increment/Decrement by 1 or 2
- Improved Stack Manipulation
- 1464 Instructions with Unique Addressing Modes
- 8 × 8 Unsigned Multiply
- 16-Bit Arithmetic
- Transfer/Exchange All Registers
- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

## HMOS

(HIGH DENSITY N-CHANNEL, SILICON-GATE)

### 8-BIT MICROPROCESSING UNIT

**L SUFFIX**
CERAMIC PACKAGE
CASE 715

**P SUFFIX**
PLASTIC PACKAGE
CASE 711

**S SUFFIX**
CERDIP PACKAGE
CASE 734

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| V_SS | 1 | 40 | HALT |
| NMI | 2 | 39 | XTAL |
| IRQ | 3 | 38 | EXTAL |
| FIRQ | 4 | 37 | RESET |
| BS | 5 | 36 | MRDY |
| BA | 6 | 35 | Q |
| V_CC | 7 | 34 | E |
| A0 | 8 | 33 | DMA/BREQ |
| A1 | 9 | 32 | R/W |
| A2 | 10 | 31 | D0 |
| A3 | 11 | 30 | D1 |
| A4 | 12 | 29 | D2 |
| A5 | 13 | 28 | D3 |
| A6 | 14 | 27 | D4 |
| A7 | 15 | 26 | D5 |
| A8 | 16 | 25 | D6 |
| A9 | 17 | 24 | D7 |
| A10 | 18 | 23 | A15 |
| A11 | 19 | 22 | A14 |
| A12 | 20 | 21 | A13 |
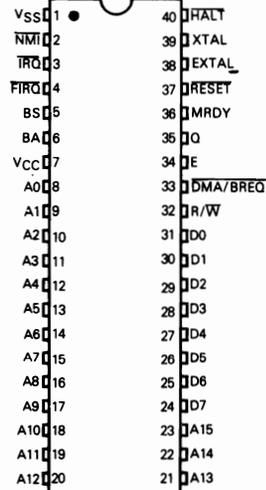
# MC6809

FIGURE 2 — MC6809 EXPANDED BLOCK DIAGRAM



*Internal Three-State Control
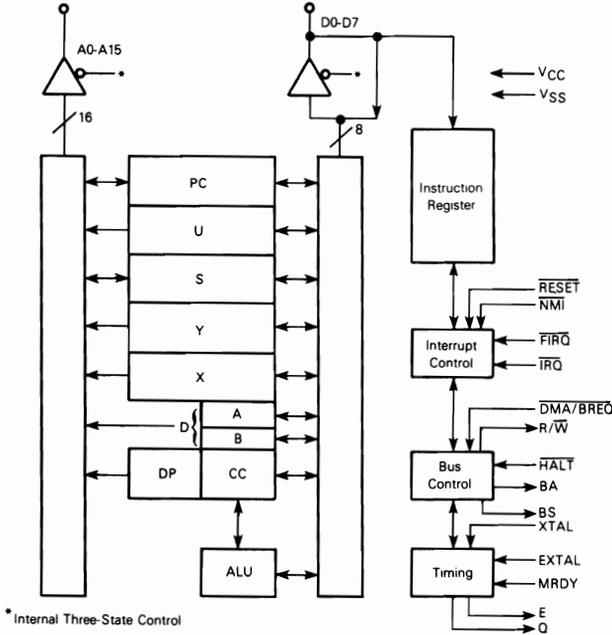
FIGURE 3 — BUS TIMING TEST LOAD
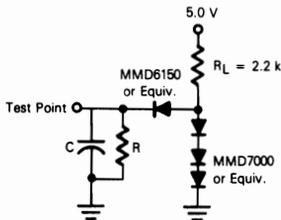


C = 30 pF for BA, BS
130 pF for D0-D7, E, Q
90 pF for A0-A15, R/$\overline{W}$

R = 11.7 kΩ for D0-D7
16.5 kΩ for A0-A15, E, Q, R/$\overline{W}$
24 kΩ for BA, BS

## PROGRAMMING MODEL

As shown in Figure 4, the MC6809 adds three registers to the set available in the MC6800. The added registers include a direct page register, the user stack pointer, and a second index register.

### ACCUMULATORS (A, B, D)

The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D register, and is formed with the A register as the most significant byte.

### DIRECT PAGE REGISTER (DP)

The direct page register of the MC6809 serves to enhance the direct addressing mode. The content of this register appears at the higher address outputs (A8-A15) during direct addressing instruction execution. This allows the direct mode to be used at any place in memory, under program control. To ensure M6800 compatibility, all bits of this register are cleared during processor reset.

# MC6809

FIGURE 4 — PROGRAMMING MODEL OF THE MICROPROCESSING UNIT



FIGURE 4 — PROGRAMMING MODEL OF THE MICROPROCESSING UNIT
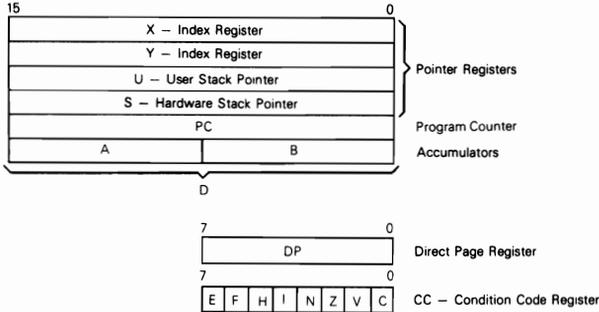
## INDEX REGISTERS (X, Y)

The index registers are used in indexed mode of addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register offset. During some indexed modes, the contents of the index register are incremented or decremented to point to the next item of tabular type data. All four pointer registers (X, Y, U, S) may be used as index registers.

## STACK POINTER (U,S)

The hardware stack pointer (S) is used automatically by the processor during subroutine calls and interrupts. The stack pointers of the MC6809 point to the top of the stack, in contrast to the MC6800 stack pointer, which pointed to the next free location on the stack. The user stack pointer (U) is controlled exclusively by the programmer. This allows arguments to be passed to and from subroutines with ease. Both stack pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support **Push** and **Pull** instructions. This allows the MC6809 to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and modular programming.

## PROGRAM COUNTER

The program counter is used by the processor to point to the address of the next instruction to be executed by the processor. Relative addressing is provided allowing the program counter to be used like an index register in some situations.

## CONDITION CODE REGISTER

The condition code register defines the state of the processor at any given time. See Figure 5.

FIGURE 5 — CONDITION CODE REGISTER FORMAT
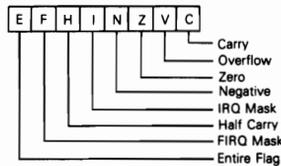


## CONDITION CODE REGISTER DESCRIPTION

### BIT 0 (C)

Bit 0 is the carry flag, and is usually the carry from the binary ALU. C is also used to represent a 'borrow' from subtract-like instructions (CMP, NEG, SUB, SBC) and is the complement of the carry from the binary ALU.

### BIT 1 (V)

Bit 1 is the overflow flag, and is set to a one by an operation which causes a signed twos complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB-1

### BIT 2 (Z)

Bit 2 is the zero flag, and is set to a one if the result of the previous operation was identically zero.

# MC6809

## BIT 3 (N)

Bit 3 is the negative flag, which contains exactly the value of the MSB of the result of the preceding operation. Thus, a negative twos-complement result will leave N set to a one

## BIT 4 (I)

Bit 4 is the $\overline{IRQ}$ mask bit. The processor will not recognize interrupts from the $\overline{IRQ}$ line if this bit is set to a one. $\overline{NMI}$, $\overline{FIRQ}$, $\overline{IRQ}$, $\overline{RESET}$, and SWI all set I to a one. SWI2 and SWI3 do not affect I.

## BIT 5 (H)

Bit 5 is the half-carry bit, and is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ADC or ADD). This flag is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is undefined in all subtract-like instructions.

## BIT 6 (F)

Bit 6 is the $\overline{FIRQ}$ mask bit. The processor will not recognize interrupts from the $\overline{FIRQ}$ line if this bit is a one. $\overline{NMI}$, $\overline{FIRQ}$, SWI, and $\overline{RESET}$ all set F to a one. $\overline{IRQ}$, SWI2, and SWI3 do not affect F.

## BIT 7 (E)

Bit 7 is the entire flag, and when set to a one indicates that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the stacked CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the condition code register represents past action.

## PIN DESCRIPTIONS

### POWER (VSS, VCC)

Two pins are used to supply power to the part: $V_{SS}$ is ground or 0 volts, while $V_{CC}$ is +5.0 V ±5%.

### ADDRESS BUS (A0-A15)

Sixteen pins are used to output address information from the MPU onto the address bus. When the processor does not require the bus for a data transfer, it will output address FFFF$_{16}$, R/$\overline{W}$ = 1, and BS = 0; this is a "dummy access" or $\overline{VMA}$ cycle. Addresses are valid on the rising edge of Q. All address bus drivers are made high impedance when output bus available (BA) is high. Each pin will drive one Schottky TTL load or four LSTTL loads, and 90 pF.

### DATA BUS (D0-D7)

These eight pins provide communication with the system bidirectional data bus. Each pin will drive one Schottky TTL load or four LSTTL loads, and 130 pF.

## READ/WRITE (R/$\overline{W}$)

This signal indicates the direction of data transfer on the data bus. A low indicates that the MPU is writing data onto the data bus. R/$\overline{W}$ is made high impedance when BA is high. R/$\overline{W}$ is valid on the rising edge of Q

## $\overline{RESET}$

A low level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU, as shown in Figure 6. The reset vectors are fetched from locations FFFE$_{16}$ and FFFF$_{16}$ (Table 1) when interrupt acknowledge is true, ($\overline{BA} \bullet BS = 1$). During initial power on, the $\overline{RESET}$ line should be held low until the clock oscillator is fully operational. See Figure 7

Because the MC6809 $\overline{RESET}$ pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage ensures that all peripherals are out of the reset state before the processor

## $\overline{HALT}$

A low level on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When halted, the BA output is driven high indicating the buses are high impedance. BS is also high which indicates the processor is in the halt or bus grant state. While halted, the MPU will not respond to external real-time requests ($\overline{FIRQ}$, $\overline{IRQ}$) although $\overline{DMA}/\overline{BREQ}$ will always be accepted, and $\overline{NMI}$ or $\overline{RESET}$ will be latched for later response. During the halt state, Q and E continue to run normally. If the MPU is not running ($\overline{RESET}$, $\overline{DMA}/\overline{BREQ}$), a halted state (BA•BS = 1) can be achieved by pulling $\overline{HALT}$ low while $\overline{RESET}$ is still low. If $\overline{DMA}/\overline{BREQ}$ and $\overline{HALT}$ are both pulled low, the processor will reach the last cycle of the instruction (by reverse cycle stealing) where the machine will the become halted. See Figure 8.

## BUS AVAILABLE, BUS STATUS (BA, BS)

The bus available output is an indication of an internal control signal which makes the MOS buses of the MPU high impedance. This signal does not imply that the bus will be available for more than one cycle. When BA goes low, a dead cycle will elapse before the MPU acquires the bus

The bus status output signal, when decoded with BA, represents the MPU state (valid with leading edge of Q)

| MPU State | | MPU State Definition |
|---|---|---|
| BA | BS | |
| 0 | 0 | Normal (Running) |
| 0 | 1 | Interrupt or Reset Acknowledge |
| 1 | 0 | Sync Acknowledge |
| 1 | 1 | Halt or Bus Grant Acknowledge |

## MCM6810
### (1.0 MHz)
## MCM68A10
### (1.5 MHz)
## MCM68B10
### (2.0 MHz)

### 128 × 8-BIT STATIC RANDOM ACCESS MEMORY

The MCM6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the M6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bidirectional Three-State Data Input/Output
- Six Chip Select Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 450 ns — MCM6810
  360 ns — MCM68A10
  250 ns — MCM68B10

### MOS
#### (N-CHANNEL, SILICON-GATE)

### 128 × 8-BIT STATIC RANDOM ACCESS MEMORY



**P SUFFIX**
PLASTIC PACKAGE
CASE 709

**L SUFFIX**
CERAMIC PACKAGE
CASE 716

**S SUFFIX**
CERDIP PACKAGE
CASE 623

### MCM6810 RANDOM ACCESS MEMORY BLOCK DIAGRAM
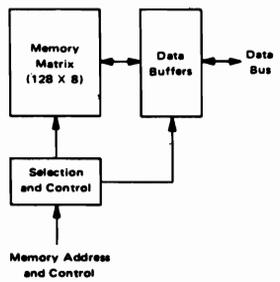


### M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| Gnd | 1 | 24 | VCC |
| D0 | 2 | 23 | A0 |
| D1 | 3 | 22 | A1 |
| D2 | 4 | 21 | A2 |
| D3 | 5 | 20 | A3 |
| D4 | 6 | 19 | A4 |
| D5 | 7 | 18 | A5 |
| D6 | 8 | 17 | A6 |
| D7 | 9 | 16 | R/$\overline{W}$ |
| CS0 | 10 | 15 | $\overline{CS5}$ |
| $\overline{CS1}$ | 11 | 14 | $\overline{CS4}$ |
| $\overline{CS2}$ | 12 | 13 | CS3 |

MC6821
(1.0 MHz)

MC68A21
(1.5 MHz)

MC68B21
(2.0 MHz)
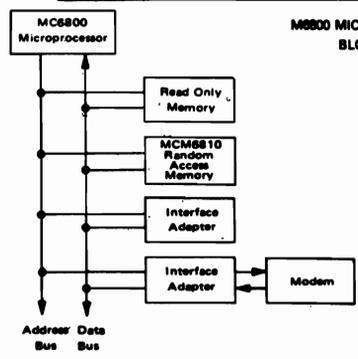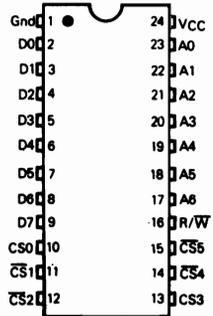
## PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the MC6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation

## MOS

(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

### PERIPHERAL INTERFACE ADAPTER



L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711

### ORDERING INFORMATION

| Speed | Device | Temperature Range |
|---|---|---|
| 1.0 MHz | MC6821P, L | 0 to +70°C |
| | MC6821CP, CL | −40 to +85°C |
| MIL-STD-8838 MIL-STD-883C | MC6821BQCS MC6821CQCS | − 55 to +125°C |
| 1.5 MHz | MC68A21P, L | 0 to +70°C |
| | MC68A21CP, CL | −40 to +85°C |
| 2.0 MHz | MC68B21P, L | 0 to +70°C |

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| 1 | VSS | CA1 | 40 |
| 2 | PA0 | CA2 | 39 |
| 3 | PA1 | IRQA | 38 |
| 4 | PA2 | IRQB | 37 |
| 5 | PA3 | RS0 | 36 |
| 6 | PA4 | RS1 | 35 |
| 7 | PA5 | Reset | 34 |
| 8 | PA6 | D0 | 33 |
| 9 | PA7 | D1 | 32 |
| 10 | PB0 | D2 | 31 |
| 11 | PB1 | D3 | 30 |
| 12 | PB2 | D4 | 29 |
| 13 | PB3 | D5 | 28 |
| 14 | PB4 | D6 | 27 |
| 15 | PB5 | D7 | 26 |
| 16 | PB6 | E | 25 |
| 17 | PB7 | CS1 | 24 |
| 18 | CB1 | CS2 | 23 |
| 19 | CB2 | CS0 | 22 |
| 20 | VCC | R/W | 21 |

# MC6843

## Advance Information

### FLOPPY DISK CONTROLLER (FDC)

The MC6843 Floppy Disk Controller performs the complex MPU/Floppy interface function. The FDC was designed to optimize the balance between the "Hardware/Software" in order to achieve integration of all key functions and maintain flexibility.

The FDC can interface a wide range of drives with a minimum of external hardware. Multiple drives can be controlled with the addition of external multiplexing rather than additional FDC's.

- Format compatible with IBM3740
- User Programmable read/write format
- Ten powerful macro commands
- Macro End Interrupt allows parallel processing of MPU and FDC
- Controls multiple Floppies with external multiplexing
- Direct interface with MC6800
- Programmable step and settling times enable operation with a wide range of Floppy drives
- Offers both Programmed Controlled I/O (PCIO) and DMA data transfer mode
- Free-Format read or write
- Single 5-volt power supply
- All registers directly accessible

## MOS
### (N-Channel, Silicon-Gate)

### FLOPPY DISK CONTROLLER

P SUFFIX
PLASTIC PACKAGE
CASE 711

L SUFFIX
CERAMIC PACKAGE
CASE 715

FIGURE 1 — SYSTEM BLOCK DIAGRAM
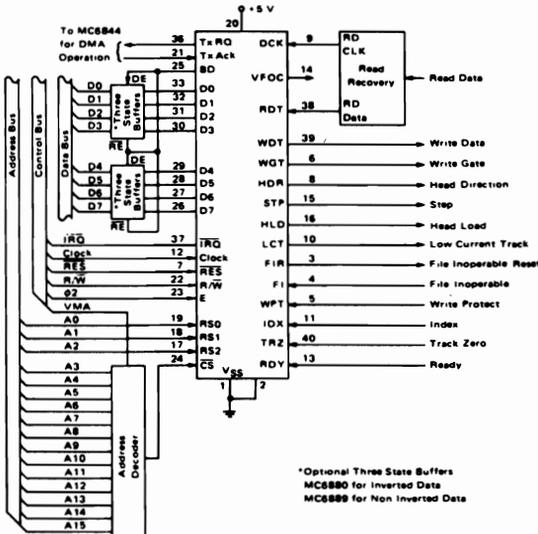


FIGURE 2 — PIN ASSIGNMENT
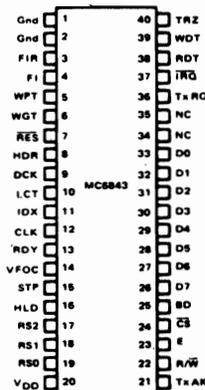


*Optional Three State Buffers
MC6880 for Inverted Data
MC6889 for Non Inverted Data

This is advance information and specifications are subject to change without notice

# MC6845

## CRT CONTROLLER (CRTC)

The MC6845 CRT controller performs the interface between an MPU and a raster-scan CRT display. It is intended for use in MPU-based controllers for CRT terminals in stand-alone or cluster configurations.

The CRTC is optimized for the hardware/software balance required for maximum flexibility. All keyboard functions, reads, writes, cursor movements, and editing are under processor control. The CRTC provides video timing and refresh memory addressing.

- Useful in Monochrome or Color CRT Applications
- Applications Include "Glass-Teletype," Smart, Programmable, Intelligent CRT Terminals; Video Games; Information Displays
- Alphanumeric, Semi-Graphic, and Full-Graphic Capability
- Fully Programmable Via Processor Data Bus. Timing May Be Generated for Almost Any Alphanumeric Screen Format, e.g., 80 × 24, 72 × 64, 132 × 20
- Single + 5 V Supply
- M6800 Compatible Bus Interface
- TTL-Compatible Inputs and Outputs
- Start Address Register Provides Hardware Scroll (by Page or Character)
- Programmable Cursor Register Allows Control of Cursor Format and Blink Rate
- Light Pen Register
- Refresh (Screen) Memory May be Multiplexed Between the CRTC and the MPU Thus Removing the Requirements for Line Buffers or External DMA Devices
- Programmable Interlace or Non-Interlace Scan Modes
- 14-Bit Refresh Address Allows Up to 16K of Refresh Memory for Use in Character or Semi-Graphic Displays
- 5-Bit Row Address Allows Up to 32 Scan-Line Character Blocks
- By Utilizing Both the Refresh Addresses and the Row Addresses, a 512K Address Space is Available for Use in Graphics Systems
- Refresh Addresses are Provided During Retrace, Allowing the CRTC to Provide Row Addresses to Refresh Dynamic RAMs
- Pin Compatible with the MC6835

## MOS
(N-CHANNEL, SILICON-GATE)

## CRT CONTROLLER
(CRTC)

**L SUFFIX**
CERAMIC PACKAGE
CASE 715

**S SUFFIX**
CERDIP PACKAGE
CASE 734

**P SUFFIX**
PLASTIC PACKAGE
CASE 711

### PIN ASSIGNMENT

| Pin | | Pin |
|---|---|---|
| GND □ 1 | ● | 40 □ VS |
| RESET □ 2 | | 39 □ HS |
| LPSTB □ 3 | | 38 □ RA0 |
| MA0 □ 4 | | 37 □ RA1 |
| MA1 □ 5 | | 36 □ RA2 |
| MA2 □ 6 | | 35 □ RA3 |
| MA3 □ 7 | | 34 □ RA4 |
| MA4 □ 8 | | 33 □ D0 |
| MA5 □ 9 | | 32 □ D1 |
| MA6 □ 10 | | 31 □ D2 |
| MA7 □ 11 | | 30 □ D3 |
| MA8 □ 12 | | 29 □ D4 |
| MA9 □ 13 | | 28 □ D5 |
| MA10 □ 14 | | 27 □ D6 |
| MA11 □ 15 | | 26 □ D7 |
| MA12 □ 16 | | 25 □ C̄S̄ |
| MA13 □ 17 | | 24 □ RS |
| DE □ 18 | | 23 □ E |
| CURSOR □ 19 | | 22 □ R/W̄ |
| VCC □ 20 | | 21 □ CLK |

## ORDERING INFORMATION

| Package Type | Frequency (MHz) | Temperature | Order Number |
|---|---|---|---|
| Ceramic | 1 0 | 0°C to 70°C | MC6845L |
| L Suffix | 1.0 | −40°C to 85°C | MC6845CL |
| | 1 5 | 0°C to 70°C | MC68A45L |
| | 1.5 | −40°C to 85°C | MC68A45CL |
| | 2.0 | 0°C to 70°C | MC68B45L |
| Cerdip | 1 0 | 0°C to 70°C | MC6845S |
| S Suffix | 1.0 | −40°C to 85°C | MC6845CS |
| | 1 5 | 0°C to 70°C | MC68A45S |
| | 1 5 | −40°C to 85°C | MC68A45CS |
| | 2 0 | 0°C to 70°C | MC68B45S |
| Plastic | 1 0 | 0°C to 70°C | MC6845P |
| P Suffix | 1.0 | −40°C to 85°C | MC6845CP |
| | 1.5 | 0°C to 70°C | MC68A45P |
| | 1 5 | −40°C to 85°C | MC68A45CP |
| | 2 0 | 0°C to 70°C | MC68B45P |

# MC6845

FIGURE 1 — TYPICAL CRT CONTROLLER APPLICATION
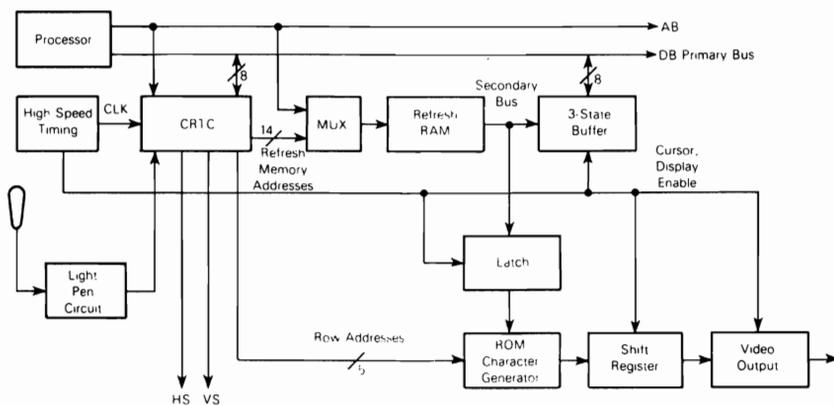


## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to -7.0 | V |
| Input Voltage | $V_{in}$ | -0.3 to -7.0 | V |
| Operating Temperature Range<br>MC6845, MC68A45, MC68B45<br>MC6845C, MC68A45C | $T_A$ | $T_L$ to $T_H$<br>0 to 70<br>-40 to -85 | C |
| Storage Temperature Range | $T_{stg}$ | -55 to -150 | C |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Rating |
|---|---|---|---|
| Thermal Resistance<br>Plastic Package<br>Cerdip Package<br>Ceramic Package | $\theta_{JA}$ | 100<br>60<br>50 | C/W |

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$

## RECOMMENDED OPERATING CONDITIONS

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | -- | 0.8 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | - | $V_{CC}$ | V |

## MC6847/MC6847Y VIDEO DISPLAY GENERATOR (VDG)

The video display generator (VDG) provides a means of interfacing the M6800 microprocessor family (or similar products) to a standard color or black and white NTSC television receiver. Applications of the VDG include video games, process control displays, home computers, education, communications, and graphics applications.

The VDG reads data from memory and produces a video signal which will allow the generation of alphanumeric or graphic displays. The generated video signal may be modulated to either channel 3 or 4 by using the compatible MC1372 (TV chroma and video modulator). This modulated signal is suitable for reception by a standard unmodified television receiver. A typical TV game is shown in Figure 1

- Compatible with the M6800 Family, the M68000 Family, and Other Microprocessor Families

- Generates Four Different Alphanumeric Display Modes, Two Semigraphic Modes, and Eight Graphic Display Modes

- The Alphanumeric Modes Display 32 Characters Per Line by 16 Lines Using Either the Internal ROM or an External Character Generator

- Alphanumeric and Semigraphic Modes May Be Mixed on a Character-by-Character Basis

- Alphanumeric Modes Support Selectable Inverse on a Character-by-Character Basis

- Internal ROM May Be Mask Programmed with a Custom Pattern

- Full Graphic Modes Offer $64 \times 64$, $128 \times 64$, $128 \times 96$, $128 \times 192$, or $256 \times 192$ Densities

- Full Graphic Modes Use One of Two 4-Color Sets or One of Two 2-Color Sets

- Compatible with the MC1372 and MC1373 Modulators Via Y, R-Y ($\phi$A), and B-Y ($\phi$B) Interface

- Compatible with the MC6883 (74LS783) Synchronous-Address Multiplexer

- Available in Either an Interlace (NTSC Standard) or Non-interlace Version

## MOS
### (N-CHANNEL, SILICON-GATE)

## VIDEO DISPLAY GENERATOR

**L SUFFIX**
CERAMIC PACKAGE
CASE 715

**P SUFFIX**
PLASTIC PACKAGE
CASE 711

**S SUFFIX**
CERDIP PACKAGE
CASE 734

### PIN ASSIGNMENT

| | | | | |
|---|---|---|---|---|
| V$_{SS}$ | 1 | | 40 | DD7 |
| DD6 | 2 | | 39 | CSS |
| DD0 | 3 | | 38 | $\overline{HS}$ |
| DD1 | 4 | | 37 | $\overline{FS}$ |
| DD2 | 5 | | 36 | $\overline{RP}$ |
| DD3 | 6 | | 35 | $\overline{A}$/G |
| DD4 | 7 | | 34 | $\overline{A}$/S |
| DD5 | 8 | | 33 | CLK |
| CHB | 9 | | 32 | INV |
| $\phi$B | 10 | | 31 | $\overline{INT}$/EXT |
| $\phi$A | 11 | | 30 | GM0 |
| $\overline{MS}$ | 12 | | 29 | GM1 |
| DA5 | 13 | | 28 | Y |
| DA6 | 14 | | 27 | GM2 |
| DA7 | 15 | | 26 | DA4 |
| DA8 | 16 | | 25 | DA3 |
| V$_{CC}$ | 17 | | 24 | DA2 |
| DA9 | 18 | | 23 | DA1 |
| DA10 | 19 | | 22 | DA0 |
| DA11 | 20 | | 21 | DA12 |

# MC6847 • MC6847Y

FIGURE 1 — BLOCK DIAGRAM OF A TV GAME USING THE VDG AND THE MC6809E MPU
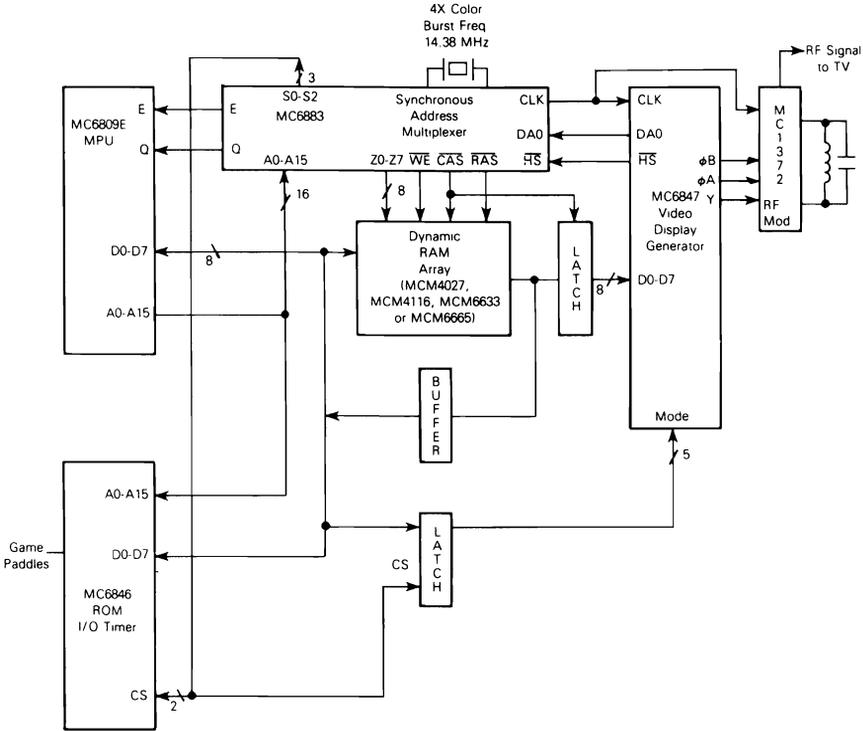


## ELECTRICAL SPECIFICATIONS
### ABSOLUTE MAXIMUM RATINGS

| Characteristics | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | V |
| Input Voltage Any Pin | $V_{in}$ | −0.3 to +7.0 | V |
| Operating Temperature | $T_A$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |

### THERMAL CHARACTERISTICS

| Characteristics | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance<br>  Ceramic<br>  Plastic<br>  Cerdip | $\theta_{JA}$ | 50<br>100<br>60 | °C/W |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (e.g., either $V_{SS}$ or $V_{CC}$).

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# MC6850

## ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

- 8- and 9-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 1.0 Mbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One- or Two-Stop Bit Operation

## MOS
### (N-CHANNEL, SILICON-GATE)

## ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER



S SUFFIX
CERDIP PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 709
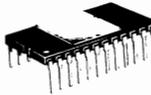
L SUFFIX
CERAMIC PACKAGE
CASE 716

### MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER BLOCK DIAGRAM



### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| V$_{SS}$ | 1 | 24 | $\overline{CTS}$ |
| Rx Data | 2 | 23 | $\overline{DCD}$ |
| Rx CLK | 3 | 22 | D0 |
| Tx CLK | 4 | 21 | D1 |
| $\overline{RTS}$ | 5 | 20 | D2 |
| Tx Data | 6 | 19 | D3 |
| $\overline{IRQ}$ | 7 | 18 | D4 |
| CS0 | 8 | 17 | D5 |
| $\overline{CS2}$ | 9 | 16 | D6 |
| CS1 | 10 | 15 | D7 |
| RS | 11 | 14 | E |
| V$_{CC}$ | 12 | 13 | R/$\overline{W}$ |

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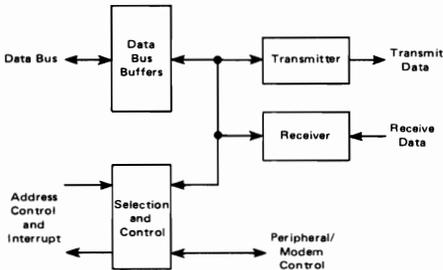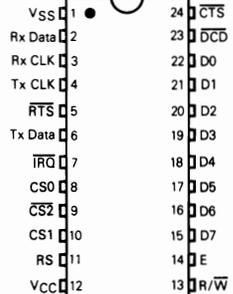
## Specifications and Applications Information

### M6800 CLOCK GENERATOR

Intended to supply the non-overlapping $\phi 1$ and $\phi 2$ clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.

**M6800 TWO-PHASE CLOCK GENERATOR/DRIVER**

**SCHOTTKY MONOLITHIC INTEGRATED CIRCUIT**
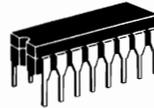


**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

### Typical MPU System with Bus Extenders



**PIN CONNECTIONS**
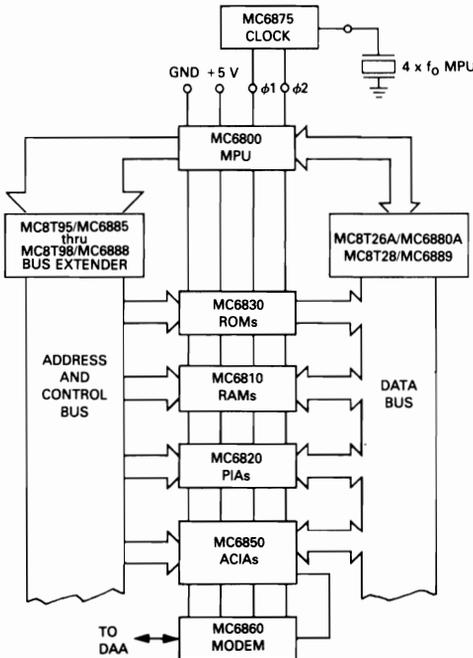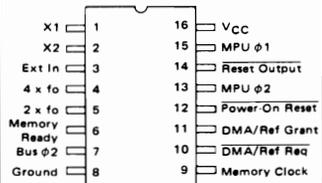
| | | | |
|---|---|---|---|
| X1 | 1 | 16 | $V_{CC}$ |
| X2 | 2 | 15 | MPU $\phi 1$ |
| Ext In | 3 | 14 | Reset Output |
| 4 x fo | 4 | 13 | MPU $\phi 2$ |
| 2 x fo | 5 | 12 | Power-On Reset |
| Memory Ready | 6 | 11 | DMA/Ref Grant |
| Bus $\phi 2$ | 7 | 10 | DMA/Ref Req |
| Ground | 8 | 9 | Memory Clock |

| ORDERING INFORMATION | | |
|---|---|---|
| Device | Temperature Range | Package |
| MC6875L | 0 to +70°C | Ceramic Dip |
| MC6875AL | -55 to +125°C | Ceramic Dip |

## MC6875, MC6875A

| TANK CIRCUIT PARAMETERS | | APPROXIMATE CRYSTAL PARAMETERS | | | | CTS KNIGHTS 400 REIMANN AVE. SANDWICH, IL 60548 (815) 786-8411 | McCOY ELECT. CO. WATTS & CHESTNUTS STS. MT. HOLLY SPRING, PA 17065 (717) 486-3411 | TYCO CRYSTAL PRODUCTS 3940 W. MONTECITO PHOENIX, AZ 85019 (602) 272-7945 |
|---|---|---|---|---|---|---|---|---|
| $L_T$ μH | $C_T$ pF | $R_S$ Ohms | $C_0$ pF | $C_1$ mpF | $f_0$ MHz | | | |
| 10 | 150 | 15-75 | 3-6 | 12 | 4.0 | MP-04A * 390 pF | 113-31 | 150-3260 |
| 4 7 | 82 | 8-45 | 4-7 | 23 | 8 0 | MP-080 * 47 pF | 113-32 | 150-3270 |

Inductors may be obtained from Coilcraft, Cary, IL 60013 (312) 639 2361

FIGURE 13



RC OPERATION

EXTERNAL INPUT
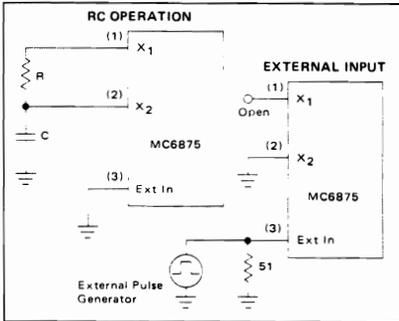
To precisely time a crystal to desired frequency, a variable trimmer capacitor in the range of 7 to 40 pF would typically be used. Note it is not a recommended practice to tune the crystal with a parallel load capacitance.

The table above shows typical values for $C_T$ and $L_T$, typical crystal characteristics, and manufacturers' part numbers for 4.0 and 8.0 megahertz operation.

The MC6875 will function as an R-C oscillator when connected as shown in Figure 13. The desired output frequency (M$\phi$1) is approximately:

Formula
$$4 \times f_0 \approx \frac{320}{C (R+ .27) + 23}$$

C in picofarads
R in K ohms
4 x fo in Megahertz

(See Figure 11)

It would be desirable to select a capacitor greater than 15 pF to minimize the effects of stray capacitance. It is also desirable to keep the resistor in the 1 to 5 k $\Omega$ range. There is a nominal 270 $\Omega$ resistor internally at $X_1$ in series with the external R. By keeping the external R as large as possible, the effects due to process variations of the internal resistor on the frequency will be reduced. There will, however, still be some variation in frequency in a production lot both from the resistance variations, external and internal, and process variations of the input switching thresholds. Therefore, in a production system, it is recommended a potentiometer be placed in series with a fixed R between $X_1$ and $X_2$.

### POWER-ON RESET

As the power to the MC6875 comes up, the Reset Output will be in a high impedance state and will not give a solid $V_{OL}$ output level until $V_{CC}$ has reached 3.5 to 4.0 V. During this time transients may appear on the clock outputs as the oscillator begins to start. This happens at approximately $V_{CC}$ = 3 V. At some $V_{CC}$ level above that, where Reset Output goes low, all the clock outputs will begin functioning normally. This phenomenon of the start-up sequence should not cause any problems except possibly in systems with battery back-up memory. The transients on the clock lines during the time the Reset Output is high impedance could initiate the system in some unknown mode and possibly write into the backup memory system. Therefore in battery backup systems, more elaborate reset circuitry will be required.

Please note that the Power-On Reset input pin of the MC6875 is not suitable for use with a manual MPU reset switch if the DMA/Ref Req or Memory Ready inputs are going to be used. The power on reset circuitry is used to initialize the internal control logic and whenever the input is switched low, the MC6875 is irresponsive to the DMA/Ref Req or Memory Ready inputs. This may result in the loss of dynamic memory and/or possibly a byte of slow static memory. The circuit of Figure 14 is recommended for applications which do not utilize the DMA/Ref Req or Memory Ready inputs. The circuit of Figure 15 is recommended for those applications that do.

FIGURE 14 – MANUAL RESET FOR APPLICATIONS NOT USING DMA/REFRESH REQUEST OR MEMORY READY INPUTS
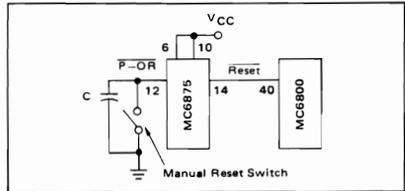


FIGURE 15 – MANUAL RESET FOR SYSTEMS USING DYNAMIC RAM OR SLOW STATIC RAM IN CONJUNCTION WITH MEMORY READY OR DMA/REFRESH REQUEST INPUTS

# QUAD THREE-STATE BUS TRANSCEIVER

This quad three state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

QUAD THREE-STATE
BUS TRANSCEIVER

MONOLITHIC SCHOTTKY
INTEGRATED CIRCUITS
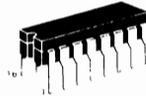
**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

## MICROPROCESSOR BUS EXTENDER APPLICATION
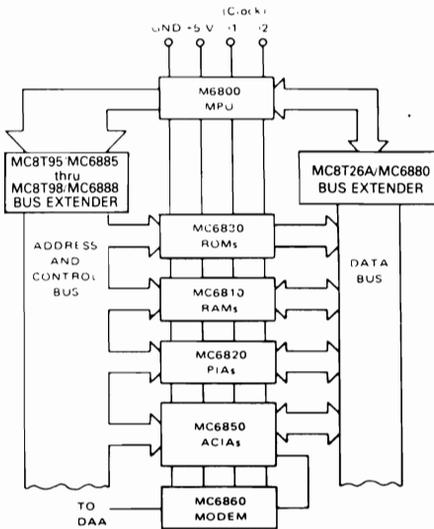


## PIN CONNECTIONS — MC8T26A
## MC6880A



| Receiver Enable Input | 1 | | 16 | V_CC |
| Receiver Output 1 | 2 | | 15 | Driver Enable Input |
| Bus 1 | 3 | | 14 | Receiver Output 4 |
| Driver Input 1 | 4 | | 13 | Bus 4 |
| Receiver Output 2 | 5 | | 12 | Driver Input 4 |
| Bus 2 | 6 | | 11 | Receiver Output 3 |
| Driver Input 2 | 7 | | 10 | Bus 3 |
| Gnd | 8 | | 9 | Driver Input 3 |
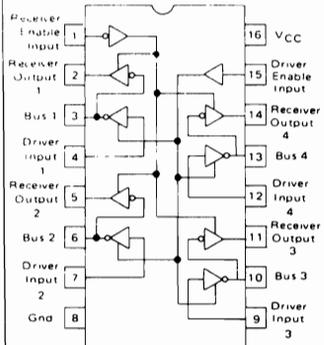
### ORDERING INFORMATION

| Device | Alternate | Temperature Range | Package |
|---|---|---|---|
| MC6880AL | MC8T26AL | 0 to +75°C | Ceramic DIP |
| MC6880AP | MC8T26AP | 0 to +75°C | Plastic DIP |

## OCTAL THREE-STATE BUFFER/LATCH

This series of devices combines four features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows for high-speed operation; 4) 48 mA drive capability.

- Inverting and Non-Inverting Options of Data
- SN74S373 Function Pinouts
- Eight Transparent Latches/Buffers in a Single Package
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- All Inputs Have Hysteresis to Improve Noise Rejection
- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74S Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

### OCTAL THREE-STATE BUFFER/LATCH
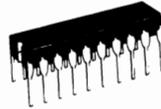


**L SUFFIX**
CASE 732-03
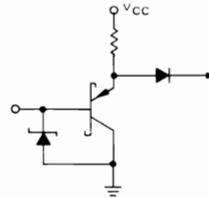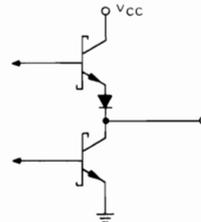
### MICROPROCESSOR BUS EXTENDER APPLICATION



**INPUT EQUIVALENT CIRCUIT**



**OUTPUT EQUIVALENT CIRCUIT**



### ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C.)

| Device | Alternate | Package |
|--------|-----------|---------|
| MC3482AL | MC6882AL | Ceramic DIP |
| MC3482BL | MC6882BL | Ceramic DIP |
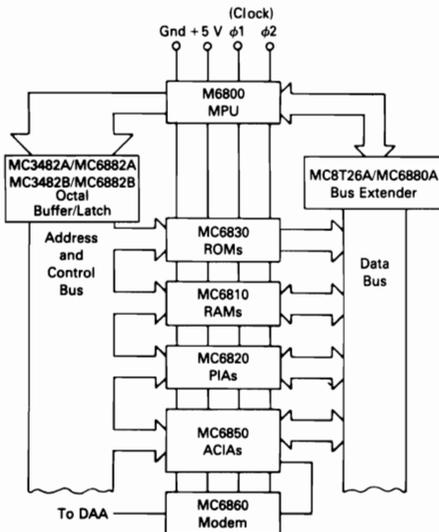
# MC6882A, MC6882B, MC3482A, MC3482B

## PIN CONNECTIONS AND TRUTH TABLES

### MC3482A/MC6882A
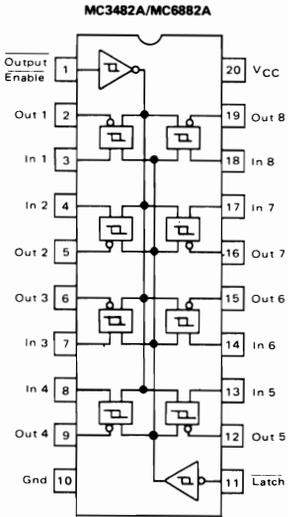
| Pin | Signal | | Pin | Signal |
|-----|--------|---|-----|--------|
| 1 | Output Enable | | 20 | V_CC |
| 2 | Out 1 | | 19 | Out 8 |
| 3 | In 1 | | 18 | In 8 |
| 4 | In 2 | | 17 | In 7 |
| 5 | Out 2 | | 16 | Out 7 |
| 6 | Out 3 | | 15 | Out 6 |
| 7 | In 3 | | 14 | In 6 |
| 8 | In 4 | | 13 | In 5 |
| 9 | Out 4 | | 12 | Out 5 |
| 10 | Gnd | | 11 | Latch |

| Output Enable | Latch | Input | Output |
|---------------|-------|-------|--------|
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 0 | 0 | x | $Q_O$ |
| 1 | x | x | Z |

### MC3482B/MC6882B
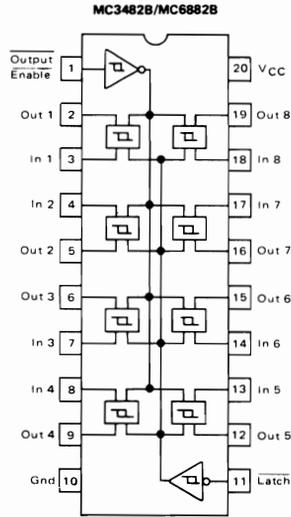
| Pin | Signal | | Pin | Signal |
|-----|--------|---|-----|--------|
| 1 | Output Enable | | 20 | V_CC |
| 2 | Out 1 | | 19 | Out 8 |
| 3 | In 1 | | 18 | In 8 |
| 4 | In 2 | | 17 | In 7 |
| 5 | Out 2 | | 16 | Out 7 |
| 6 | Out 3 | | 15 | Out 6 |
| 7 | In 3 | | 14 | In 6 |
| 8 | In 4 | | 13 | In 5 |
| 9 | Out 4 | | 12 | Out 5 |
| 10 | Gnd | | 11 | Latch |

| Output Enable | Latch | Input | Output |
|---------------|-------|-------|--------|
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | x | $Q_O$ |
| 1 | x | x | Z |

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## Advance Information

### SYNCHRONOUS ADDRESS MULTIPLEXER

The SN74LS783/MC6883 brings together the MC6809E (MPU), the MC6847 (Color Video Display Generator) and dynamic RAM to form a highly effective, compact and cost effective computer and display system.

- MC6809E, MC6800, MC6801E, MC68000 and MC6847 (VDG) Compatible
- Transparent MPU/VDG/Refresh
- RAM size — 4K, 8K, 16K, 32K or 64K Bytes (Dynamic or Static)
- Addressing Range — 96K Bytes
- Single Crystal Provides All Timing
- Register Programmable:
  VDG Addressing Modes
  VDG Offset (0 to 64K)
  RAM Size
  Page Switch
  MPU Rate (Crystal ÷ 16 or ÷ 8)
  MPU Rate (Address Dependent or Independent)
- System "Device Selects" Decoded 'On Chip'
- Timing is Optimized for Standard Dynamic RAMs
- +5.0 V Only Operation
- Easy Synchronization of Multiple SAM Systems
- DMA Mode

**SYNCHRONOUS ADDRESS MULTIPLEXER**

**LOW POWER SCHOTTKY**



N SUFFIX
PLASTIC PACKAGE
CASE 711

J SUFFIX
CERAMIC PACKAGE
CASE 734

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| 1 | A11 | V<sub>CC</sub> | 40 |
| 2 | A10 | A12 | 39 |
| 3 | A9 | A13 | 38 |
| 4 | A8 | A14 | 37 |
| 5 | Osc<sub>in</sub> | A15 | 36 |
| 6 | Osc<sub>Out</sub> | Z7 | 35 (RAS1) |
| 7 | VClk | Z6 | 34 |
| 8 | DA0 | Z5 | 33 |
| 9 | HS | Z4 | 32 |
| 10 | WE | Z3 | 31 |
| 11 | CAS | Z2 | 30 |
| 12 | RAS0 | Z1 | 29 |
| 13 | Q | Z0 | 28 |
| 14 | E | S0 | 27 |
| 15 | R/W | S1 | 26 |
| 16 | A0 | S2 | 25 |
| 17 | A1 | A7 | 24 |
| 18 | A2 | A6 | 23 |
| 19 | A3 | A5 | 22 |
| 20 | Gnd | A4 | 21 |

### SYSTEM BLOCK DIAGRAM
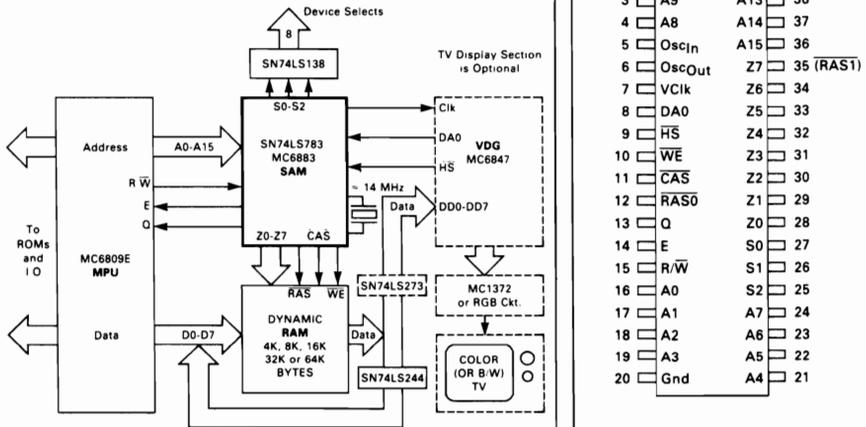


This document contains information on a new product. Specifications and information herein are subject to change without notice.

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## HEX THREE-STATE BUFFER INVERTERS

This series of devices combines three features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows high-speed operation.

The devices differ in that the non-inverting MC8T95/MC6885 and inverting MC8T96/MC6886 provide a two-input Enable which controls all six buffers, while the non-inverting MC8T97/MC6887 and inverting MC8T98/MC6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

The units are well-suited for Address buffers on the M6800 or similar microprocessor application.

- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

## HEX THREE-STATE BUFFER/INVERTERS



CASE 620          CASE 648
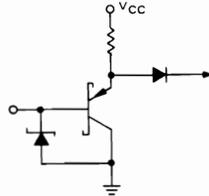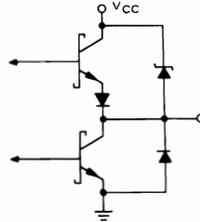
### MICROPROCESSOR BUS EXTENDER APPLICATION



### INPUT EQUIVALENT CIRCUIT



### OUTPUT EQUIVALENT CIRCUIT
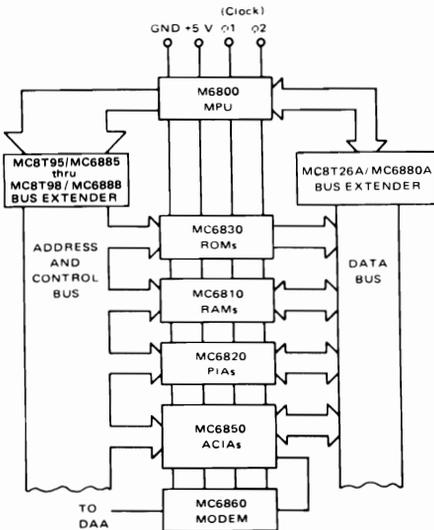


### ORDERING INFORMATION
(Temperature Range for the following devices = 0 to +75°C)

| DEVICE | ALTERNATE | PACKAGE |
|--------|-----------|---------|
| MC8T95L | MC6885L | Ceramic DIP |
| MC8T96L | MC6886L | Ceramic DIP |
| MC8T97L | MC6887L | Ceramic DIP |
| MC8T98L | MC6888L | Ceramic DIP |
| MC8T95P | MC6885P | Plastic DIP |
| MC8T96P | MC6886P | Plastic DIP |
| MC8T97P | MC6887P | Plastic DIP |
| MC8T98P | MC6888P | Plastic DIP |

# MC8T95–98/MC6885–88

## PIN CONNECTIONS AND TRUTH TABLES

### MC8T95/MC6885
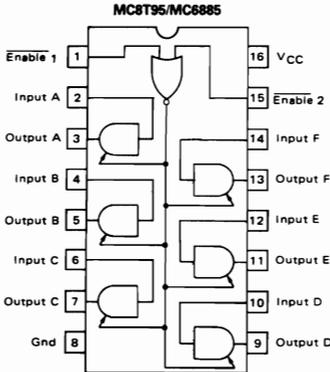


| Enable 1 | 1 | | 16 | $V_{CC}$ |
| Input A | 2 | | 15 | Enable 2 |
| Output A | 3 | | 14 | Input F |
| Input B | 4 | | 13 | Output F |
| Output B | 5 | | 12 | Input E |
| Input C | 6 | | 11 | Output E |
| Output C | 7 | | 10 | Input D |
| Gnd | 8 | | 9 | Output D |

| Enable 2 | Enable 1 | Input | Output |
|---|---|---|---|
| L | L | L | L |
| L | L | H | H |
| L | H | X | Z |
| H | L | X | Z |
| H | H | X | Z |

### MC8T96/MC6886
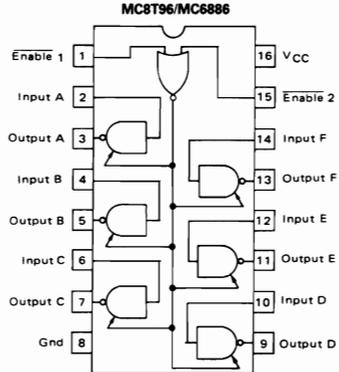


| Enable 1 | 1 | | 16 | $V_{CC}$ |
| Input A | 2 | | 15 | Enable 2 |
| Output A | 3 | | 14 | Input F |
| Input B | 4 | | 13 | Output F |
| Output B | 5 | | 12 | Input E |
| Input C | 6 | | 11 | Output E |
| Output C | 7 | | 10 | Input D |
| Gnd | 8 | | 9 | Output D |

| Enable 2 | Enable 1 | Input | Output |
|---|---|---|---|
| L | L | L | H |
| L | L | H | L |
| L | H | X | Z |
| H | L | X | Z |
| H | H | X | Z |

### MC8T97/MC6887
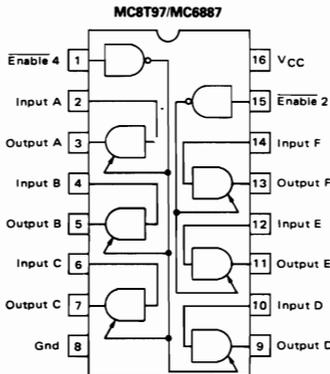


| Enable 4 | 1 | | 16 | $V_{CC}$ |
| Input A | 2 | | 15 | Enable 2 |
| Output A | 3 | | 14 | Input F |
| Input B | 4 | | 13 | Output F |
| Output B | 5 | | 12 | Input E |
| Input C | 6 | | 11 | Output E |
| Output C | 7 | | 10 | Input D |
| Gnd | 8 | | 9 | Output D |

| Enable | Input | Output |
|---|---|---|
| L | L | L |
| L | H | H |
| H | X | Z |

### MC8T98/MC6888



| Enable 4 | 1 | | 16 | $V_{CC}$ |
| Input A | 2 | | 15 | Enable 2 |
| Output A | 3 | | 14 | Input F |
| Input B | 4 | | 13 | Output F |
| Output B | 5 | | 12 | Input E |
| Input C | 6 | | 11 | Output E |
| Output C | 7 | | 10 | Input D |
| Gnd | 8 | | 9 | Output D |

| Enable | Input | Output |
|---|---|---|
| L | L | H |
| L | H | L |
| H | X | Z |

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
X = Irrelevant

## MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 8.0 | Vdc |
| Input Voltage | $V_I$ | 5.5 | Vdc |
| Operating Ambient Temperature Range | $T_A$ | 0 to +75 | °C |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Operating Junction Temperature | $T_J$ | | °C |
| Plastic Package | | 150 | |
| Ceramic Package | | 175 | |

## MC8T28
## MC6889

## NONINVERTING
## QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the –48 mA driver and –20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

Propagation delay times for the driver portion are 17 ns maximum while the receiver portion runs 17 ns. The MC8T28 is identical to the NE8T28 and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor
- Non-Inverting

## NONINVERTING
## BUS TRANSCEIVER

### MONOLITHIC SCHOTTKY
### INTEGRATED CIRCUITS



**L SUFFIX**
CERAMIC PACKAGE
CASE 620-02

**P SUFFIX**
PLASTIC PACKAGE
CASE 648-05

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MICROPROCESSOR BUS EXTENDER APPLICATION
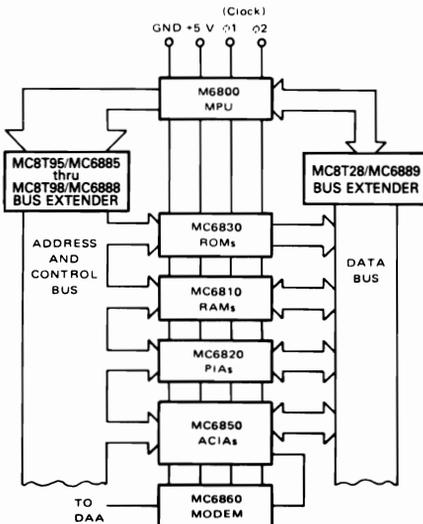


PIN CONNECTIONS — MC8T28
MC6889



| | Receiver Enable Input | 1 | | 16 | $V_{CC}$ | |
| Receiver Output 1 | 2 | | | 15 | Driver Enable Input | |
| Bus 1 | 3 | | | 14 | Receiver Output 4 | |
| Driver Input 1 | 4 | | | 13 | Bus 4 | |
| Receiver Output 2 | 5 | | | 12 | Driver Input 4 | |
| Bus 2 | 6 | | | 11 | Receiver Output 3 | |
| Driver Input 2 | 7 | | | 10 | Bus 3 | |
| Gnd | 8 | | | 9 | Driver Input 3 | |
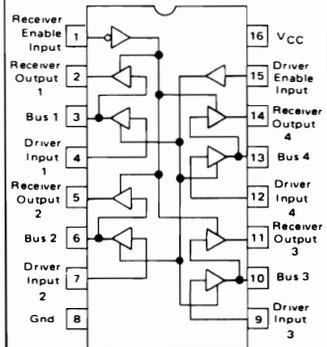
### ORDERING INFORMATION

| Device | Alternate | Temperature Range | Package |
|--------|-----------|-------------------|---------|
| MC8T28L | MC6889L | 0 to +75°C | Ceramic DIP |
| MC8T28P | MC6889P | 0 to +75°C | Plastic DIP |

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# MC6890

## Advance Information

### MPU-BUS-COMPATIBLE
### 8-BIT D-TO-A CONVERTER

The MC6890 is a self-contained, bus-compatible, 8 bit (±0.19% accuracy) D-to-A converter system capable of interfacing directly with 8-bit microprocessors.

Available in both commercial and military temperature ranges, this monolithic converter contains master/slave registers to prevent transparency to data transitions during active enable; a laser-trimmed, low-TC, 2.5 V precision bandgap reference; and high stability, laser-trimmed, thin-film resistors for both reference input and output span and bipolar offset control.

A reset pin provides for overriding stored data and forcing $I_{out}$ to zero.

● Direct Data Bus Link with All Popular TTL Level MPU's

● ±1/2 LSB Nonlinearity Over Temperature

● Fast Settling Time: 200 ns Typ

● Internal 2.5-V Precision Laser-Trimmed Voltage Reference (May Also Be Used Externally)

● Minimum Enable Pulse Width 70 ns

● Fast Enable: 10 ns Maximum Data Hold Time

● Reset Pin to Override Data

● Output Voltage Ranges: +5, +10, +20, or ±2.5, ±5, ±10 Volts

● Low Power: 90 mW Typ

● +5 V and −5 V to −15 V Supplies
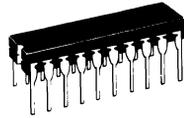
**L SUFFIX**
CASE 732-03

### OPERATION WITH AN MPU



### PIN CONNECTIONS



| | | |
|---|---|---|
| (LSB) D0 1 | | 20 $V_{CC}$ |
| D1 2 | | 19 $REF_{OUT}$ |
| D2 3 | | 18 $REF_{IN}$ |
| D3 4 | | 17 Analog Gnd |
| D4 5 | | 16 20 V Span |
| D5 6 | | 15 10 V Span |
| D6 7 | | 14 $I_{out}$ |
| (MSB) D7 8 | | 13 Bipolar Offset |
| Reset 9 | | 12 Enable |
| Digital Gnd 10 | | 11 $V_{EE}$ |
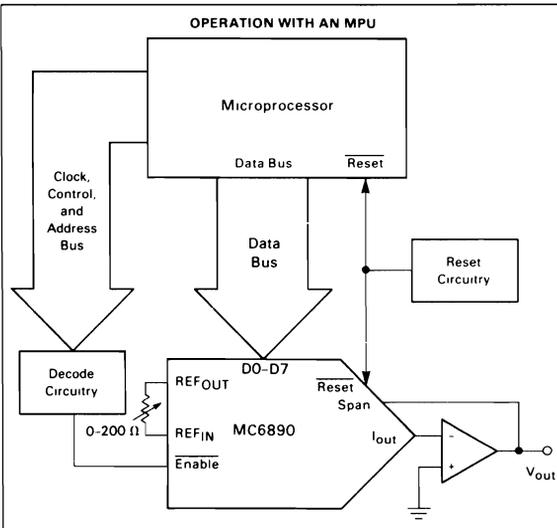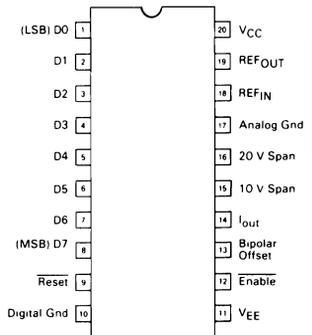
### ORDERING INFORMATION

| Device | Temperature Range | Package |
|---|---|---|
| MC6890L | 0° to +70°C | Ceramic DIP |
| MC6890AL | −55° to +125°C | Ceramic DIP |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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# Z840C
# Z80® CPU Central
# Processing Unit

# Product
# Specification

April 1985

## FEATURES

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.

- Eight MHz, 6 MHz, 4 MHz, and 2.5 MHz clocks for the Z80H, Z80B, Z80A, and Z80 CPU result in rapid instruction execution with consequent high data throughput.

- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers, together with indexed and relative addressing, result in the most powerful data handling capabilities in the microcomputer industry.

- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.

- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays.

- There are three modes of high speed interrupt processing: 8080 similar, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.

- On-chip dynamic memory refresh counter.



**Figure 1. Pin Functions**



**Figure 2a. 40-Pin Dual-In-Line Package (DIP) Pin Assignments**

Address bus

Data bus

INTERNAL ADDRESS BUS

Address multiplexer/ driver

Data multiplexer/driver

INTERNAL ADDRESS BUS

INTERNAL DATA BUS

| Flags Register F | Stack pointer SP | B | C | B' | C' | Accumulator A | | Program counter PC | Instruction register | | Refresh counter R |
|---|---|---|---|---|---|---|---|---|---|---|---|
| F' | | D | E | D' | E' | A' | | | | | |
| | | H | L | H' | L' | | | | Instruction decoder | | |

Index register IX

Index register IY

Input 1   Input 2
Arithmetic logic unit
ALU

Interrupt logic

Interrupt page address I

Timing and control logic

φ  HALT RFSH WAIT WR  RD BUSAK MREQ

Internal architecture Z80

BUSRQ

INT NMI

RESET

Sign
Zero
Half carry
Parity/overflow  } Flags
Subtract
Carry

| A | (8) | | F | S | Z | | H | | P/V | | N | C | | Main register set |
| B | | | C | | | | | | | | | | | |
| D | | | E | | | | | | | | | | | |
| H | | | L | | | | | | | | | | | |

Bank switches { ☐ Selects AF or A'F'
              ☐ Selects BCDEHL or B'C'D'E'H'L

| A' | (8) | | F' |  |  |  |  |  |  |  |  | | Alternate register set |
| B' | | | C' | | | | | | | | | | |
| D' | | | E' | | | | | | | | | | |
| H' | | | L' | | | | | | | | | | |

IX [ (16) ]  } Index registers

IY [ (16) ]

PC [ (16) ]   Program counter

SP [ (16) ]   Stack pointer

R [ (7) ]   Memory refresh

I [ (8) ]   Interrupt vector
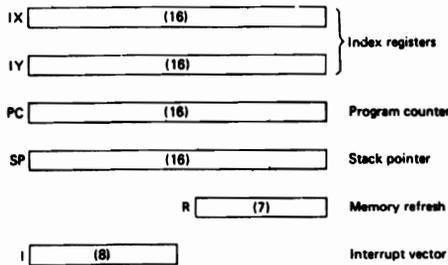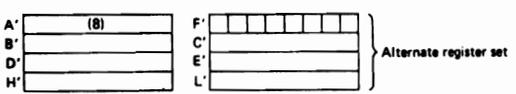
IFF ☐   Interrupt enable flipflop

IM [ ☐ ]   Interrupt mode

Zilog Z80 CPU registers.

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# Z80 Microprocessor Instruction Set

| INSTRUCTION | | OBJECT CODE | BYTES- | CLOCK PERIODS |
|---|---|---|---|---|
| ADC | data | CE yy | 2 | 7 |
| ADC | (HL) | 8E | 1 | 7 |
| ADC | HL,rp | ED 01xx1010 | 2 | 15 |
| ADC | (IX + disp) | DD 8E yy | 3 | 19 |
| ADC | (IY + disp) | FD 8E yy | 3 | 19 |
| ADC | reg | 10001xxx | 1 | 4 |
| ADD | data | C6 yy | 2 | 7 |
| ADD | (HL) | 86 | 1 | 7 |
| ADD | HL,rp | 00xx1001 | 1 | 11 |
| ADD | (IX + disp) | DD 86 yy | 3 | 19 |
| ADD | IX,pp | DD 00xx1001 | 2 | 15 |
| ADD | (IY + disp) | FD 88 yy | 3 | 19 |
| ADD | IY,rr | FD 00xx1001 | 2 | 15 |
| ADD | reg | 10000xxx | 1 | 4 |
| AND | data | E6 yy | 2 | 7 |
| AND | (HL) | A6 | 1 | 7 |
| AND | (IX + disp) | DD A6 yy | 3 | 19 |
| AND | (IY + disp) | FD A6 yy | 3 | 19 |
| AND | reg | 10100xxx | 1 | 4 |
| BIT | b,(HL) | CB 01bbb110 | 2 | 12 |
| BIT | b,(IX + disp) | DD CB yy 01bbb110 | 4 | 20 |
| BIT | b,(IY + disp) | FD CB yy 01bbb110 | 4 | 20 |
| BIT | b,reg | CB 01bbbxxx | 2 | 9 |
| CALL | label | CD ppqq | 3 | 17 |
| CALL | C,label | DC ppqq | 3 | 10/17 |
| CALL | M,label | FC ppqq | 3 | 10/17 |
| CALL | NC,label | D4 ppqq | 3 | 10/17 |
| CALL | NZ,label | C4 ppqq | 3 | 10/17 |
| CALL | P,label | F4 ppqq | 3 | 10/17 |
| CALL | PE,label | EC ppqq | 3 | 10/17 |
| CALL | PO,label | E4 ppqq | 3 | 10/17 |
| CALL | Z,label | CC ppqq | 3 | 10/17 |
| CCF | | 3F | 1 | 4 |
| CP | data | FE yy | 2 | 7 |
| CP | (HL) | BE | 1 | 7 |
| CP | (IX + disp) | DD BE yy | 3 | 19 |
| CP | (IY + disp) | FD BE yy | 3 | 19 |
| CP | reg | 10111xxx | 1 | 4 |
| CPD | | ED A9 | 2 | 16 |
| CPDR | | ED B9 | 2 | 21/16* |
| CPI | | ED A1 | 2 | 16 |
| CPIR | | ED B1 | 2 | 21/16* |
| CPL | | 2F | 1 | 4 |
| DAA | | 27 | 1 | 4 |
| DEC | (HL) | 35 | 1 | 11 |
| DEC | IX | DD 2B | 2 | 10 |
| DEC | (IX + disp) | DD 35 yy | 3 | 23 |
| DEC | IY | FD 2B | 2 | 10 |
| DEC | (IY + disp) | FD 35 yy | 3 | 23 |
| DEC | rp | 00xx1011 | 1 | 6 |
| DEC | reg | 00xxx101 | 1 | 4 |
| DI | | F3 | 1 | 4 |
| DJNZ | disp | 10 yy | 2 | 8/13 |
| EI | | FB | 1 | 4 |
| EX | AF,AF | 08 | 1 | 4 |
| EX | DE,HL | EB | 1 | 4 |
| EX | (SP),HL | E3 | 1 | 19 |
| EX | (SP),IX | DD E3 | 2 | 23 |

| INSTRUCTION | | OBJECT CODE | BYTES | CLOCK PERIODS |
|---|---|---|---|---|
| EX | (SP),IY | FD E3 | 2 | 23 |
| EXX | | D9 | 1 | 4 |
| HALT | | 76 | 1 | 4 |
| IM | 0 | ED 46 | 2 | 8 |
| IM | 1 | ED 56 | 2 | 8 |
| IM | 2 | ED 5E | 2 | 8 |
| IN | A,port | DB yy | 2 | 10 |
| IN | reg,(C) | ED 01ddd000 | 2 | 11 |
| INC | (HL) | 34 | 1 | 11 |
| INC | IX | DD 23 | 2 | 10 |
| INC | (IX + disp) | DD 34 yy | 3 | 23 |
| INC | IY | FD 23 | 2 | 10 |
| INC | (IY + disp) | FD 34 yy | 3 | 23 |
| INC | rp | 00xx0011 | 1 | 6 |
| INC | reg | 00xxx100 | 1 | 4 |
| IND | | ED AA | 2 | 15 |
| INDR | | ED BA | 2 | 20/15 |
| INI | | ED A2 | 2 | 15 |
| INIR | | ED B2 | 2 | 20/15 |
| JP | label | C3 ppqq | 3 | 10 |
| JP | C,label | DA ppqq | 3 | 10 |
| JP | (HL) | E9 | 1 | 4 |
| JP | (IX) | DD E9 | 2 | 8 |
| JP | (IY) | FD E9 | 2 | 8 |
| JP | M,label | FA ppqq | 3 | 10 |
| JP | NC,label | D2 ppqq | 3 | 10 |
| JP | NZ,label | C2 ppqq | 3 | 10 |
| JP | P,label | F2 ppqq | 3 | 10 |
| JP | PE,label | EA ppqq | 3 | 10 |
| JP | PO,label | E2 ppqq | 3 | 10 |
| JP | Z,label | CA ppqq | 3 | 10 |
| JR | C,disp | 38 yy | 2 | 7/12 |
| JR | disp | 18 yy | 2 | 12 |
| JR | NC,disp | 30 yy | 2 | 7/12 |
| JR | NZ,disp | 20 yy | 2 | 7/12 |
| JR | Z,disp | 28 yy | 2 | 7/12 |
| LD | A,(addr) | 3A ppqq | 3 | 13 |
| LD | A,(BC) | 0A | 1 | 7 |
| LD | A,(DE) | 1A | 1 | 7 |
| LD | A,I | ED 57 | 2 | 9 |
| LD | A,R | ED 5F | 2 | 9 |
| LD | (addr),A | 32 ppqq | 3 | 13 |
| LD | (addr),BC | ED 43 ppqq | 4 | 20 |
| LD | (addr),DE | ED 53 ppqq | 4 | 20 |
| LD | (addr),HL | 22 ppqq | 3 | 16 |
| LD | (addr),IX | DD 22 ppqq | 4 | 20 |
| LD | (addr),IY | FD 22 ppqq | 4 | 20 |
| LD | (addr),SP | ED 73 ppqq | 4 | 20 |
| LD | (BC),A | 02 | 1 | 7 |
| LD | (DE),A | 12 | 1 | 7 |
| LD | HL,(addr) | 2A ppqq | 3 | 16 |
| LD | (HL),data | 36 yy | 2 | 10 |
| LD | (HL),reg | 01110sss | 1 | 7 |
| LD | I,A | ED 47 | 2 | 9 |
| LD | IX,(addr) | DD 2A ppqq | 4 | 20 |
| LD | IX,data 16 | DD 21 yyyy | 4 | 14 |
| LD | (IX + disp),data | DD 36 yy yy | 4 | 19 |
| LD | (IX + disp),reg | DD 01110sss yy | 3 | 19 |
| LD | IY,(addr) | FD 2A ppqq | 4 | 20 |
| LD | IY,data 16 | FD 21 yyyy | 4 | 14 |

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| INSTRUCTION | | OBJECT CODE | BYTES | CLOCK PERIODS |
|---|---|---|---|---|
| LD | (IY+disp),data | FD 36 yyyy | 4 | 19 |
| LD | (IY+disp),reg | FD 01110sss yy | 3 | 19 |
| LD | R,A | ED 4F | 2 | 9 |
| LD | reg,data | 00ddd110 yy | 2 | 7 |
| LD | reg,(HL) | 01ddd110 | 1 | 7 |
| LD | reg,(IX+disp) | DD 01ddd110 yy | 3 | 19 |
| LD | reg,(IY+disp) | FD 01ddd110 yy | 3 | 19 |
| LD | reg,reg | 01ddddsss | 1 | 4 |
| LD | rp,(addr) | ED 01xx1011 ppqq | 4 | 20 |
| LD | rp,data16 | 00xx0001 yyyy | 3 | 10 |
| LD | SP,HL | F9 | 1 | 6 |
| LD | SP,IX | DD F9 | 2 | 10 |
| LD | SP,IY | FD F9 | 2 | 10 |
| LDD | | ED A8 | 2 | 16 |
| LDDR | | ED B8 | 2 | 21/16* |
| LDI | | ED A0 | 2 | 16 |
| LDIR | | ED B0 | 2 | 21/16* |
| NEG | | ED 44 | 2 | 8 |
| NOP | | 00 | 1 | 4 |
| OR | data | F6 yy | 2 | 7 |
| OR | (HL) | B6 | 1 | 7 |
| OR | (IX+disp) | DD B6 yy | 3 | 19 |
| OR | (IY+disp) | FD B6 yy | 3 | 19 |
| OR | reg | 10110xxx | 1 | 4 |
| OTDR | | ED B8 | 2 | 20/15* |
| OTIR | | ED B3 | 2 | 20/15* |
| OUT | (C),reg | ED 01sss001 | 2 | 12 |
| OUT | port,A | D3 yy | 2 | 11 |
| OUTD | | ED AB | 2 | 15 |
| OUTI | | ED A3 | 2 | 15 |
| POP | IX | DD E1 | 2 | 14 |
| POP | IY | FD E1 | 2 | 14 |
| POP | pr | 11xx0001 | 1 | 10 |
| PUSH | IX | DD E5 | 2 | 15 |
| PUSH | IY | FD E5 | 2 | 15 |
| PUSH | pr | 11xx0101 | 1 | 11 |
| RES | b,(HL) | CB 10bbb110 | 2 | 15 |
| RES | b,(IX+disp) | DD CB yy 10bbb110 | 4 | 23 |
| RES | b,(IY+disp) | FD CB yy 10bbb110 | 4 | 23 |
| RES | b,reg | CB 10bbbxxx | 2 | 8 |
| RET | | C9 | 1 | 10 |
| RET | C | D8 | 1 | 5/11 |
| RET | M | F8 | 1 | 5/11 |
| RET | NC | D0 | 1 | 5/11 |
| RET | NZ | C0 | 1 | 5/11 |
| RET | P | F0 | 1 | 5/11 |
| RET | PE | E8 | 1 | 5/11 |
| RET | PO | E0 | 1 | 5/11 |
| RET | Z | C8 | 1 | 5/11 |
| RETI | | ED 4D | 2 | 14 |

* Execution time shown is for one iteration.

| INSTRUCTION | | OBJECT CODE | BYTES | CLOCK PERIODS |
|---|---|---|---|---|
| RETN | | ED 45 | 2 | 14 |
| RL | (HL) | CB 16 | 2 | 15 |
| RL | (IX+disp) | DD CB yy 16 | 4 | 23 |
| RL | (IY+disp) | FD CB yy 16 | 4 | 23 |
| RL | reg | CB 00010xxx | 2 | 8 |
| RLA | | 17 | 1 | 4 |
| RLC | (HL) | CB 06 | 2 | 15 |
| RLC | (IX+disp) | DD CB yy 06 | 4 | 23 |
| RLC | (IY+disp) | FD CB yy 06 | 4 | 23 |
| RLC | reg | CB 00000xxx | 2 | 8 |
| RLCA | | 07 | 1 | 4 |
| RLD | | ED 6F | 2 | 18 |
| RR | (HL) | CB 1E | 2 | 15 |
| RR | (IX+disp) | DD CB yy 1E | 4 | 23 |
| RR | (IY+disp) | FD CB yy 1E | 4 | 23 |
| RR | reg | CB 00011xxx | 2 | 8 |
| RRA | | 1F | 1 | 4 |
| RRC | (HL) | CB 0E | 2 | 15 |
| RRC | (IX+disp) | DD CB yy 0E | 4 | 23 |
| RRC | (IY+disp) | FD CB yy 0E | 4 | 23 |
| RRC | reg | CB 00001xxx | 2 | 8 |
| RRCA | | 0F | 1 | 4 |
| RRD | | ED 67 | 2 | 18 |
| RST | n | 11xxx111 | 1 | 11 |
| SBC | data | DE yy | 2 | 7 |
| SBC | (HL) | 9E | 1 | 7 |
| SBC | HL,rp | ED 01xx0010 | 2 | 15 |
| SBC | (IX+disp) | DD 9E yy | 3 | 19 |
| SBC | (IY+disp) | FD 9E yy | 3 | 19 |
| SBC | reg | 10011xxx | 1 | 4 |
| SCF | | 37 | 1 | 4 |
| SET | b,(HL) | CB 11bbb110 | 2 | 15 |
| SET | b,(IX+disp) | DD CB yy 11bbb110 | 4 | 23 |
| SET | b,(IY+disp) | FD CB yy 11bbb110 | 4 | 23 |
| SET | b,reg | CB 11bbbxxx | 2 | 8 |
| SLA | (HL) | CB 26 | 2 | 15 |
| SLA | (IX+disp) | DD CB yy 26 | 4 | 23 |
| SLA | (IY+disp) | FD CB yy 26 | 4 | 23 |
| SLA | reg | CB 00100xxx | 2 | 8 |
| SRA | (HL) | CB 2E | 2 | 15 |
| SRA | (IX+disp) | DD CB yy 2E | 4 | 23 |
| SRA | (IY+disp) | FD CB yy 2E | 4 | 23 |
| SRA | reg | CB 00101xxx | 2 | 8 |
| SRL | (HL) | CB 3E | 2 | 15 |
| SRL | (IX+disp) | DD CB yy 3E | 4 | 23 |
| SRL | (IY+disp) | FD CB yy 3E | 4 | 23 |
| SRL | reg | CB 00111xxx | 2 | 8 |
| SUB | data | D6 yy | 2 | 7 |
| SUB | (HL) | 96 | 1 | 7 |
| SUB | (IX+disp) | DD 96 yy | 3 | 19 |
| SUB | (IY+disp) | FD 96 yy | 3 | 19 |
| SUB | reg | 10010xxx | 1 | 4 |
| XOR | data | EE yy | 2 | 7 |
| XOR | (HL) | AE | 1 | 7 |
| XOR | (IX+disp) | DD AE yy | 3 | 19 |
| XOR | (IY+disp) | FD AE yy | 3 | 19 |
| XOR | reg | 10101xxx | 1 | 4 |

x      represents an optional binary digit.
bbb    represents optional binary digits identifying a bit location in a register or memory byte. (000 LSB, 111 MSB)
ddd    represents optional binary digits identifying a destination register.
       111 = A    000 = B    001 = C    010 = D    011 = E    100 = H    101 = L
sss    represents optional binary digits identifying a source register—same coding as ddd.
ppqq   represents a four hexadecimal digit memory address.
yy     represents two hexadecimal data digits.
yyyy   represents four hexadecimal data digits.

When two possible execution times are shown (i.e., 5/11), it indicates that the number of clock periods depends on condition flags.

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# Z8410 Z80® DMA
# Direct Memory Access
# Controller

# Product
# Specification

April 1985

## FEATURES

■ Transfers, searches, and search/transfers in Byte-at-a-Time, Burst, or Continuous modes. Cycle length and edge timing can be programmed to match the speed of any port.

■ Dual port addresses (source and destination) generated for memory-to-I/O, memory-to-memory, or I/O-to-I/O operations. Addresses may be fixed or automatically incremented/decremented.

■ Next-operation loading without disturbing current operations via buffered starting-address registers. An entire previous sequence can be repeated automatically.

■ Extensive programmability of functions. CPU can read complete channel status.

■ Standard Z80 Family bus-request and prioritized interrupt-request daisy chains implemented without external logic. Sophisticated, internally modifiable interrupt vectoring.

■ Direct interfacing to system buses without external logic.

## GENERAL DESCRIPTION

The Z80 DMA (Direct Memory Access) is a powerful and versatile device for controlling and processing transfers of data. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control with little or no external logic in systems using an 8- or 16-bit data bus and a 16-bit address bus.
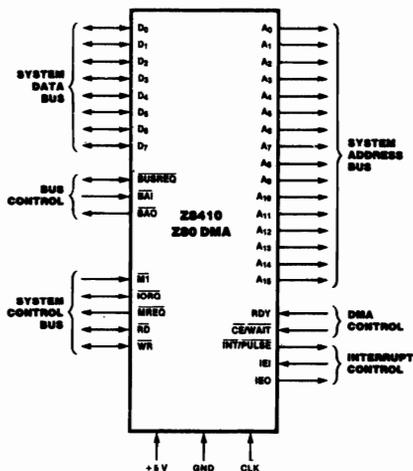


**Figure 1. Pin Functions**



**Figure 2. 40-pin Dual-In-Line Package (DIP), Pin Assignments**

# Z8420 Z80® PIO Parallel Input/Output Controller

# Product Specification

April 1985

## FEATURES

- Provides a direct interface between Z80 microcomputer systems and peripheral devices.

- Two ports with interrupt-driven handshake for fast response.

- Four programmable operating modes: Output, Input, Bidirectional (Port A only), and Bit Control

- Programmable interrupts on peripheral status conditions.

- Standard Z80 Family bus-request and prioritized interrupt-request daisy chains implemented without external logic.

- The eight Port B outputs can drive Darlington transistors (1.5 mA at 1.5V).

## GENERAL DESCRIPTION

The Z80 PIO Parallel I/O Circuit is a programmable, dual-port device that provides a TTL-compatible interface between peripheral devices and the Z80 CPU (Figures 1 and 2). The CPU configures the Z80 PIO to interface with a wide range of peripheral devices with no other external logic. Typical peripheral devices that are compatible with the Z80 PIO include most keyboards, paper tape readers and punches, printers, and PROM programmers.
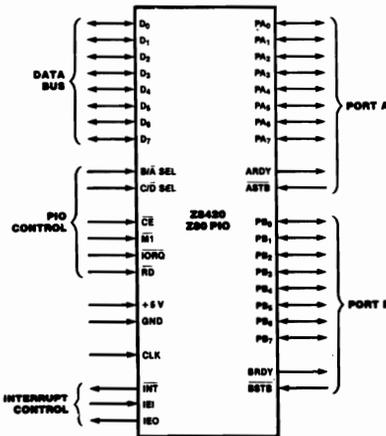


**Figure 1. Pin Functions**
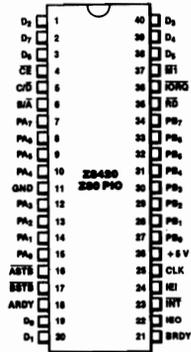


**Figure 2a. 40-pin Dual-In-Line Package (DIP), Pin Assignments**

# Z8430
# Z80® CTC
# Counter/Timer Circuit

# Product
# Specification

## FEATURES

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.

- Selectable positive or negative trigger initiates timer operation.

- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors.

- Interfaces directly to the Z80 CPU or—for baud rate generation—to the Z80 SIO.

- Standard Z80 Family daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller.

## GENERAL DESCRIPTION

The Z80 CTC four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straightforward: each channel is programmed with two bytes; a third is necessary when
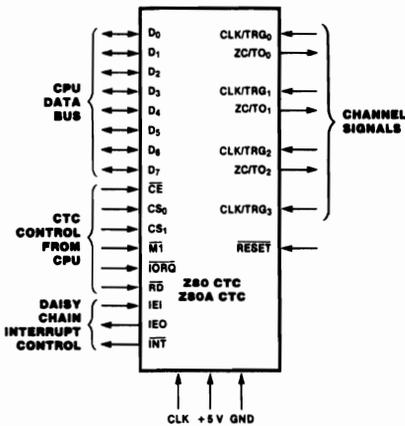


**Figure 1. Pin Functions**



**Figure 2a. 40-pin Dual-In-Line Package (DIP), Pin Assignments**

2041-001, 002
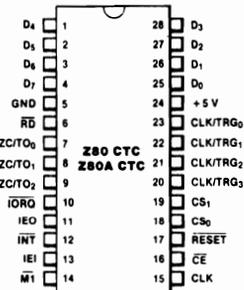
# Z8440/1/2/4 Z80® SIO
# Serial Input/Output
# Controller

# Product
# Specification

April 1985

## FEATURES

- Two independent full-duplex channels, with separate control and status lines for modems or other devices.

- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5 MHz clock (Z80 SIO), or 0 to 800K bits/second with a 4.0 MHz clock (Z80A SIO).

- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7, or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.

- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7, or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection, and flag insertion.

- Receiver data registers quadruply buffered, transmitter registers doubly buffered.

- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

## GENERAL DESCRIPTION

The Z80 SIO Serial Input/Output Controller is a dual-channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs, and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels,

with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast, slow, peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

The Z80 SIO is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic or ceramic DIP. It uses a single +5V power supply and the standard Z80 family single-phase clock. The Z8444 is packaged in a 44-pin ceramic LCC.

## PIN DESCRIPTION

Figures 1 through 6 illustrate the three 40-pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together:

- Z80 SIO/2 lacks $\overline{SYNCB}$
- Z80 SIO/1 lacks $\overline{DTRB}$
- Z80 SIO/0 has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The 44-pin package, the Z80 SIO/4, has all options (Figure 7).

The first bonding option above (SIO/2) is the preferred version for most applications. The pin descriptions are as follows:

**B/$\overline{A}$.** Channel A or B Select (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit $A_0$ from the CPU is often used for the selection function.

**C/$\overline{D}$.** Control or Data Select (input, High selects Control). This input defines the type of information transfer performed

# Z8470 Z80® DART
# Dual Asynchronous
# Receiver/Transmitter

# Product
# Specification

## FEATURES

■ Two independent full-duplex channels with separate modem controls. Modem status can be monitored.

■ In x1 clock mode, data rates are 0 to 500K bits/second with a 2.5 MHz clock, or 0 to 800K bits/second with a 4.0 MHz clock.

■ Receiver data registers are quadruply buffered; the transmitter is doubly buffered.

■ Programmable options include 1, 1½, or 2 stop bits; even, odd, or no parity; and x1, x16, x32, and x64 clock modes.

■ Break generation and detection as well as parity-, overrun-, and framing-error detection are available.

■ Interrupt features include a programmable interrupt vector, a "status affects vector" mode for fast interrupt processing, and the standard Z80 peripheral daisy-chain interrupt structure that provides automatic interrupt vectoring with no external logic.

■ On-chip logic for ring indication and carrier-detect status.

## GENERAL DESCRIPTION

The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.
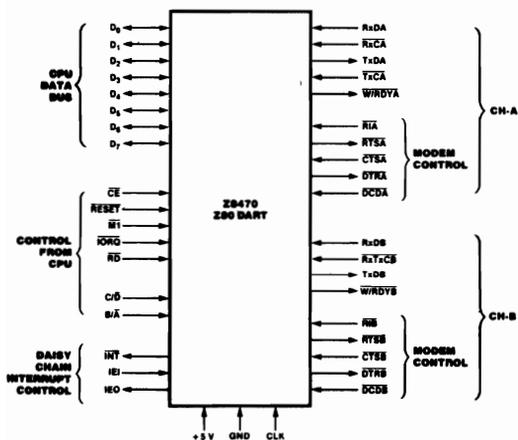


**Figure 1. Pin Functions**



**Figure 2. 40-Pin Dual-In-Line Package (DIP), Pin Assignments**

2044-001, 002
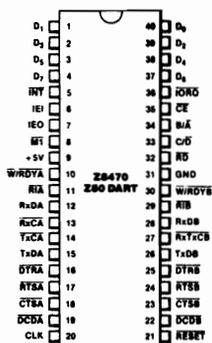
# 6502 Microprocessor Instruction Set

## 1 ALPHABETICAL ORDER

| | | | |
|---|---|---|---|
| ADC | Add with carry | JSR | Jump to subroutine |
| AND | Logical AND | LDA | Load accumulator |
| ASL | Arithmetic shift left | LDX | Load X |
| BCC | Branch if carry clear | LDY | Load Y |
| BCS | Branch if carry set | LSR | Logical shift right |
| BEQ | Branch if result = 0 | NOP | No operation |
| BIT | Test bit | ORA | Logical OR |
| BMI | Branch if minus | PHA | Push A |
| BNE | Branch if not equal to 0 | PHP | Push P status |
| BPL | Branch if plus | PLA | Pull A |
| BRK | Break | PLP | Pull P status |
| BVC | Branch if overflow clear | ROL | Rotate left |
| BVS | Branch if overflow set | ROR | Rotate right |
| CLC | Clear carry | RTI | Return from interrupt |
| CLD | Clear decimal flag | RTS | Return from subroutine |
| CLI | Clear interrupt disable | SBC | Subtract with carry |
| CLV | Clear overflow | SEC | Set carry |
| CMP | Compare to accumulator | SED | Set decimal |
| CPX | Compare to X | SEI | Set interrupt disable |
| CPY | Compare to Y | STA | Store accumulator |
| DEC | Decrement memory | STX | Store X |
| DEX | Decrement X | STY | Store Y |
| DEY | Decrement Y | TAX | Transfer A to X |
| EOR | Exclusive OR | TAY | Transfer A to Y |
| INC | Increment memory | TSX | Transfer SP to X |
| INX | Increment X | TXA | Transfer X to A |
| INY | Increment Y | TXS | Transfer X to SP |
| JMP | Jump | TYA | Transfer Y to A |

# 2 OP CODE AND TIMING FOR 6502

(n = number of clock cycles    # = number of bytes per instruction)

| MNEMONIC | IMPLIED OP n # | ACCUM OP n # | ABSOLUTE OP n # | ZERO PAGE OP n # | IMMEDIATE OP n # | ABS,X OP n # | ABS,Y OP n # | (IND,X) OP n # | (IND),Y OP n # | Z.PAGE,X OP n # | RELATIVE OP n # | INDIRECT OP n # | Z.PAGE,Y OP n # | N | V | B | D | I | Z | C | MNEMONIC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC (1) | | | 6D 4 3 | 65 3 2 | 69 2 2 | 7D 4 3 | 79 4 3 | 61 6 2 | 71 5 2 | 75 4 2 | | | | • | • | | | | • | • | ADC |
| AND (1) | | | 2D 4 3 | 25 3 2 | 29 2 2 | 3D 4 3 | 39 4 3 | 21 6 2 | 31 5 2 | 35 4 2 | | | | • | | | | | • | | AND |
| ASL (2) | | 0A 2 1 | 0E 6 3 | 06 5 2 | | 1E 7 3 | | | | 16 6 2 | | | | • | | | | | • | • | ASL |
| BCC (2) | | | | | | | | | | | 90 2 2 | | | | | | | | | | BCC |
| BCS (2) | | | | | | | | | | | B0 2 2 | | | | | | | | | | BCS |
| BEQ (2) | | | | | | | | | | | F0 2 2 | | | | | | | | | | BEQ |
| BIT | | | 2C 4 3 | 24 3 2 | | | | | | | | | | M7 | M6 | | | | • | | BIT |
| BMI (2) | | | | | | | | | | | 30 2 2 | | | | | | | | | | BMI |
| BNE (2) | | | | | | | | | | | D0 2 2 | | | | | | | | | | BNE |
| BPL (2) | | | | | | | | | | | 10 2 2 | | | | | | | | | | BPL |
| BRK | 00 7 1 | | | | | | | | | | | | | | | 1 | | | | | BRK |
| BVC (2) | | | | | | | | | | | 50 2 2 | | | | | | | | | | BVC |
| BVS (2) | | | | | | | | | | | 70 2 2 | | | | | | | | | | BVS |
| CLC | 18 2 1 | | | | | | | | | | | | | | | | | | | 0 | CLC |
| CLD | D8 2 1 | | | | | | | | | | | | | | | | 0 | | | | CLD |
| CLI | 58 2 1 | | | | | | | | | | | | | | | | | 0 | | | CLI |
| CLV | B8 2 1 | | | | | | | | | | | | | | 0 | | | | | | CLV |
| CMP (1) | | | CD 4 3 | C5 3 2 | C9 2 2 | DD 4 3 | D9 4 3 | C1 6 2 | D1 5 2 | D5 4 2 | | | | • | | | | | • | • | CMP |
| CPX | | | EC 4 3 | E4 3 2 | E0 2 2 | | | | | | | | | • | | | | | • | • | CPX |
| CPY | | | CC 4 3 | C4 3 2 | C0 2 2 | | | | | | | | | • | | | | | • | • | CPY |
| DEC | | | CE 6 3 | C6 5 2 | | DE 7 3 | | | | D6 6 2 | | | | • | | | | | • | | DEC |
| DEX | CA 2 1 | | | | | | | | | | | | | • | | | | | • | | DEX |
| DEY | 88 2 1 | | | | | | | | | | | | | • | | | | | • | | DEY |
| EOR (1) | | | 4D 4 3 | 45 3 2 | 49 2 2 | 5D 4 3 | 59 4 3 | 41 6 2 | 51 5 2 | 55 4 2 | | | | • | | | | | • | | EOR |
| INC | | | EE 6 3 | E6 5 2 | | FE 7 3 | | | | F6 6 2 | | | | • | | | | | • | | INC |
| INX | E8 2 1 | | | | | | | | | | | | | • | | | | | • | | INX |
| INY | C8 2 1 | | | | | | | | | | | | | • | | | | | • | | INY |
| JMP | | | 4C 3 3 | | | | | | | | | 6C 5 3 | | | | | | | | | JMP |
| JSR | | | 20 6 3 | | | | | | | | | | | | | | | | | | JSR |
| LDA (1) | | | AD 4 3 | A5 3 2 | A9 2 2 | BD 4 3 | B9 4 3 | A1 6 2 | B1 5 2 | B5 4 2 | | | | • | | | | | • | | LDA |
| LDX (1) | | | AE 4 3 | A6 3 2 | A2 2 2 | | BE 4 3 | | | | | | B6 4 2 | • | | | | | • | | LDX |
| LDY (1) | | | AC 4 3 | A4 3 2 | A0 2 2 | BC 4 3 | | | | B4 4 2 | | | | • | | | | | • | | LDY |
| LSR | | 4A 2 1 | 4E 6 3 | 46 5 2 | | 5E 7 3 | | | | 56 6 2 | | | | 0 | | | | | • | • | LSR |
| NOP | EA 2 1 | | | | | | | | | | | | | | | | | | | | NOP |
| ORA (1) | | | 0D 4 3 | 05 3 2 | 09 2 2 | 1D 4 3 | 19 4 3 | 01 6 2 | 11 5 2 | 15 4 2 | | | | • | | | | | • | | ORA |
| PHA | 48 3 1 | | | | | | | | | | | | | | | | | | | | PHA |
| PHP | 08 3 1 | | | | | | | | | | | | | | | | | | | | PHP |
| PLA | 68 4 1 | | | | | | | | | | | | | • | | | | | • | | PLA |
| PLP | 28 4 1 | | | | | | | | | | | | | • | • | • | • | • | • | • | PLP |
| ROL | | 2A 2 1 | 2E 6 3 | 26 5 2 | | 3E 7 3 | | | | 36 6 2 | | | | • | | | | | • | • | ROL |
| ROR | | 6A 2 1 | 6E 6 3 | 66 5 2 | | 7E 7 3 | | | | 76 6 2 | | | | • | | | | | • | • | ROR |
| RTI | 40 6 1 | | | | | | | | | | | | | • | • | • | • | • | • | • | RTI |
| RTS | 60 6 1 | | | | | | | | | | | | | | | | | | | | RTS |
| SBC (1) | | | ED 4 3 | E5 3 2 | E9 2 2 | FD 4 3 | F9 4 3 | E1 6 2 | F1 5 2 | F5 4 2 | | | | • | • | | | | • | • | SBC |
| SEC | 38 2 1 | | | | | | | | | | | | | | | | | | | 1 | SEC |
| SED | F8 2 1 | | | | | | | | | | | | | | | | 1 | | | | SED |
| SEI | 78 2 1 | | | | | | | | | | | | | | | | | 1 | | | SEI |
| STA | | | 8D 4 3 | 85 3 2 | | 9D 5 3 | 99 5 3 | 81 6 2 | 91 6 2 | 95 4 2 | | | | | | | | | | | STA |
| STX | | | 8E 4 3 | 86 3 2 | | | | | | | | | 96 4 2 | | | | | | | | STX |
| STY | | | 8C 4 3 | 84 3 2 | | | | | | 94 4 2 | | | | | | | | | | | STY |
| TAX | AA 2 1 | | | | | | | | | | | | | • | | | | | • | | TAX |
| TAY | A8 2 1 | | | | | | | | | | | | | • | | | | | • | | TAY |
| TSX | BA 2 1 | | | | | | | | | | | | | • | | | | | • | | TSX |
| TXA | 8A 2 1 | | | | | | | | | | | | | • | | | | | • | | TXA |
| TXS | 9A 2 1 | | | | | | | | | | | | | | | | | | | | TXS |
| TYA | 98 2 1 | | | | | | | | | | | | | • | | | | | • | | TYA |

(1) Add 1 to n if crossing page boundary    (2) Add 2 to n if branch within page; Add 3 to n if branch within another page
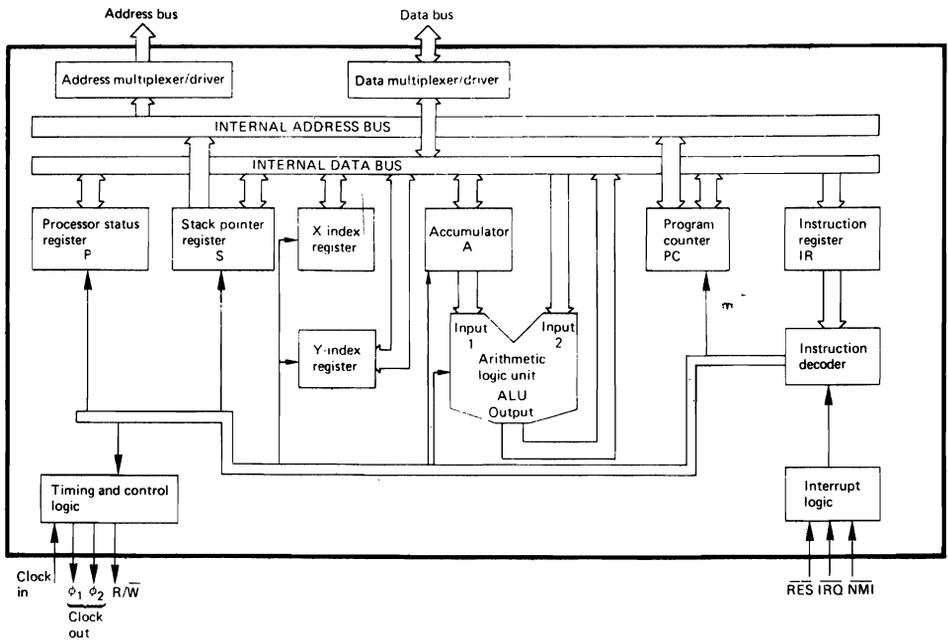
, Internal
**architecture 6502**

Pin-out
connections 6502



| | | |
|---|---|---|
| GND | 1 | 40 | RES |
| RDY | 2 | 39 | φ2 (OUT) |
| φ1 (OUT) | 3 | 38 | S.O. |
| IRQ | 4 | 37 | φ0 (IN) |
| N.C. | 5 | 36 | N.C. |
| NMI | 6 | 35 | N.C. |
| SYNC | 7 | 34 | R/W |
| +5V | 8 | 33 | DB0 |
| AB0 | 9 | 32 | DB1 |
| AB1 | 10 | 31 | DB2 |
| AB2 | 11 | 30 | DB3 |
| AB3 | 12 | 29 | DB4 |
| AB4 | 13 | 28 | DB5 |
| AB5 | 14 | 27 | DB6 |
| AB6 | 15 | 26 | DB7 |
| AB7 | 16 | 25 | AB15 |
| AB8 | 17 | 24 | AB14 |
| AB9 | 18 | 23 | AB13 |
| AB10 | 19 | 22 | AB12 |
| AB11 | 20 | 21 | GND |

6502
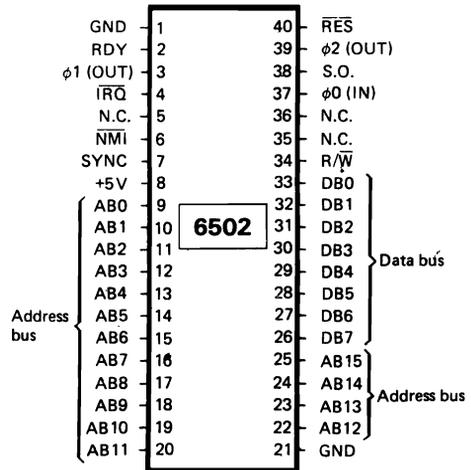
N.C. = NOT CONNECTED

# VERSATILE INTERFACE ADAPTER (VIA)

## SYSTEM ABSTRACT

The 8 bit R6500 microcomputer system is produced with N-channel, silicon-gate, depletion-load technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips -- the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, memory and I/O devices . . as well as low-cost design aids and documentation.

## DESCRIPTION

The R6522 VIA adds two powerful, flexible Interval Timers, a serial-to-parallel/parallel-to-serial shift register and input latching on the peripheral ports to the capabilities of the R6520 Peripheral Interface Adapter (PIA) device. Handshaking capability is expanded to allow control of bidirectional data transfers between VIAs in multiple processor systems and between peripherals.

Control of peripherals is primarily through two 8-bit bidirectional ports. Each of these ports can be programmed to act as an input or an output. Peripheral I/O lines can be selectively controlled by the Interval Timers to generate programmable-frequency square waves and/or to count externally generated pulses. Positive control of VIA functions is gained through its internal register organization; Interrupt Flag Register, Interrupt Enable Register, and two Function Control Registers

## FEATURES

- Organized for simplified software control of many functions
- Compatible with the R650X and R651X family of microprocessors (CPUs)
- Bi-directional, 8-bit data bus for communication with microprocessor
- Two Bi-directional, 8-bit input/output ports for interface with peripheral devices
- CMOS and TTL compatible input/output peripheral ports
- Data Direction Registers allow each peripheral pin to act as either an input or an output
- Interrupt Flag Register allows the microprocessor to readily determine the source of an interrupt and provides convenient control of the interrupts within the chip
- Handshake control logic for input/output peripheral data transfer operations
- Data latching on peripheral input/output ports
- Two fully-programmable interval timers/counters
- Eight-bit Shift Register for serial interface
- Forty-pin plastic or ceramic DIP package.

### Ordering Information

| Order Number | Package Type | Frequency | Temperature Range |
|---|---|---|---|
| R6522P | Plastic | 1 MHz | $0^{\circ}$C to $+70^{\circ}$C |
| R6522AP | Plastic | 2 MHz | $0^{\circ}$C to $+70^{\circ}$C |
| R6522C | Ceramic | 1 MHz | $0^{\circ}$C to $+70^{\circ}$C |
| R6522AC | Ceramic | 2 MHz | $0^{\circ}$C to $+70^{\circ}$C |
| R6522PE | Plastic | 1 MHz | $-40^{\circ}$C to $+85^{\circ}$C |
| R6522APE | Plastic | 2 MHz | $-40^{\circ}$C to $+85^{\circ}$C |
| R6522CE | Ceramic | 1 MHz | $-40^{\circ}$C to $+85^{\circ}$C |
| R6522ACE | Ceramic | 2 MHz | $-40^{\circ}$C to $+85^{\circ}$C |
| R6522CMT | Ceramic | 1 MHz | $-55^{\circ}$C to $+125^{\circ}$C |
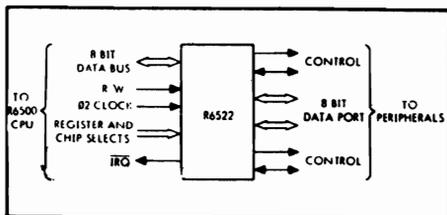


**Basic R6522 Interface Diagram**

Pin Configuration

| Pin | | Pin | |
|---|---|---|---|
| VSS | 1 | 40 | CA1 |
| PA0 | 2 | 39 | CA2 |
| PA1 | 3 | 38 | RS0 |
| PA2 | 4 | 37 | RS1 |
| PA3 | 5 | 36 | RS2 |
| PA4 | 6 | 35 | RS3 |
| PA5 | 7 | 34 | RES |
| PA6 | 8 | 33 | D0 |
| PA7 | 9 | 32 | D1 |
| PB0 | 10 | 31 | D2 |
| PB1 | 11 | 30 | D3 |
| PB2 | 12 | 29 | D4 |
| PB3 | 13 | 28 | D5 |
| PB4 | 14 | 27 | D6 |
| PB5 | 15 | 26 | D7 |
| PB6 | 16 | 25 | $\Phi$2 |
| PB7 | 17 | 24 | CS1 |
| CB1 | 18 | 23 | CS2 |
| CB2 | 19 | 22 | R/W |
| VCC | 20 | 21 | IRQ |
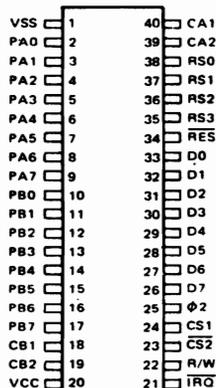
## OPERATION SUMMARY

### Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal R6522 register which is to be accessed   The sixteen possible combinations access the registers as follows:

| RS3 | RS2 | RS1 | RS0 | Register | Remarks | RS3 | RS2 | RS1 | RS0 | Register | Remarks |
|-----|-----|-----|-----|----------|---------|-----|-----|-----|-----|----------|---------|
| L | L | L | L | ORB | | H | L | L | L | T2L-L | Write Latch |
| L | L | L | H | ORA | Controls Handshake | | | | | T2C-L | Read Counter |
| L | L | H | L | DDRB | | H | L | L | H | T2C-H | Triggers T2L-L/T2C-L |
| L | L | H | H | DDRA | | | | | | | Transfer |
| L | H | L | L | T1L-L | Write Latch | H | L | H | | SR | |
| | | | | T1C-L | Read Counter | H | L | H | H | ACR | |
| L | H | L | H | T1C-H | Trigger T1L-L/T1C-L | H | H | L | L | PCR | |
| | | | | | Transfer | H | H | L | H | IFR | |
| L | H | H | L | T1L-L | | H | H | H | L | IER | |
| L | H | H | H | T1L-H | | H | H | H | H | ORA | No Effect on Handshake |

Note   L = 0 4V DC, H = 2.4V DC.

### Timer 2 Control

| RS3 | RS2 | RS1 | RS0 | R/W = L | R/W = H |
|-----|-----|-----|-----|---------|---------|
| H | L | L | L | Write T2L-L | Read T2C-L Clear Interrupt flag |
| H | L | L | H | Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag | Read T2C-H |

### Writing the Timer 1 Register

The operations which take place when writing to each of the four T1 addresses are as follows:

| RS3 | RS2 | RS1 | RS0 | Operation (R/W = L) |
|-----|-----|-----|-----|---------------------|
| L | H | L | L | Write into low order latch |
| L | H | L | H | Write into high order latch Write into high order counter Transfer low order latch into low order counter Reset T1 interrupt flag |
| L | H | H | L | Write low order latch |
| X | H | H | H | Write high order latch Reset T1 interrupt flag |

### Reading the Timer 1 Registers

For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

| RS3 | RS2 | RS1 | RS0 | Operation (R/W = H) |
|-----|-----|-----|-----|---------------------|
| L | H | L | L | Read T1 low order counter Reset T1 interrupt flag |
| L | H | L | H | Read T1 high order counter |
| L | H | H | L | Read T1 low order latch |
| L | H | H | H | Read T1 high order latch |

402

# CRT CONTROLLER (CRTC)

## DESCRIPTION

The R6545-1 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500 products.

The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows non-interlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The RES input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

## FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 ±5% Volt Power Supply

## ORDERING INFORMATION

| Part Number | Package Type | Frequency | Temperature Range |
|---|---|---|---|
| R6545-1P | Plastic | 1 MHz | 0°C to +70°C |
| R6545-1AP | Plastic | 2 MHz | 0°C to +70°C |
| R6545-1C | Ceramic | 1 MHz | 0°C to +70°C |
| R6545-1AC | Ceramic | 2 MHz | 0°C to +70°C |

| | | | |
|---|---|---|---|
| VSS | 1 | 40 | VSYNC |
| RES | 2 | 39 | HSYNC |
| LPEN | 3 | 38 | RA0 |
| CC0/MA0 | 4 | 37 | RA1 |
| CC1/MA1 | 5 | 36 | RA2 |
| CC2/MA2 | 6 | 35 | RA3 |
| CC3/MA3 | 7 | 34 | RA4 |
| CC4/MA4 | 8 | 33 | D0 |
| CC5/MA5 | 9 | 32 | D1 |
| CC6/MA6 | 10 | 31 | D2 |
| CC7/MA7 | 11 | 30 | D3 |
| CR0/MA8 | 12 | 29 | D4 |
| CR1/MA9 | 13 | 28 | D5 |
| CR2/MA10 | 14 | 27 | D6 |
| CR3/MA11 | 15 | 26 | D7 |
| CR4/MA12 | 16 | 25 | CS |
| CR5/MA13 | 17 | 24 | RS |
| DISPLAY ENABLE | 18 | 23 | φ2 |
| CURSOR | 19 | 22 | R/W |
| VCC | 20 | 21 | CCLK |
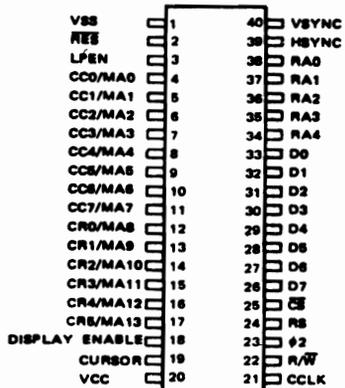
**R6545-1 Pin Configuration**

## INTERFACE SIGNAL DESCRIPTION

### CPU INTERFACE

#### φ2 (Phase 2 Clock)

The input clock is the system Phase 2 (φ2) clock and is used to trigger all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable φ2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

#### R/W̄ (Read/Write)

The R/W̄ input signal generated by the processor is used to control the direction of data transfers. A high on the R/W̄ pin allows the processor to read the data supplied by the R6545-1, a low on the R/W̄ pin allows data on data lines D0-D7 to be written into the R6545-1.

#### C̄S̄ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when C̄S̄ is low.

#### RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes (R/W̄ = low) into the Address Register and reads (R/W̄ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

#### D0-D7 (Data Bus)

D0-D7 are the eight data lines used to transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected (C̄S̄ = low).

### VIDEO INTERFACE

#### HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

#### VSYNC (Vertical Sync)

The VSYNC signal is an active high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

#### DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE signal is an active-high output used to indicate when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE can be delayed one character time by setting bit 4 of R8 equal to 1.

### CURSOR (Cursor Coincidence)

The CURSOR signal is an active-high output used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed, to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to A "1".

### LPEN (Light Pen Strobe)

The LPEN signal is an edge-sensitive input used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

### CCLK (Clock)

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

### R̄ĒS̄

The R̄ĒS̄ signal is an active-low input used to initialize all internal scan counter circuits. When R̄ĒS̄ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. R̄ĒS̄ must stay low for at least one CCLK period. All scan timing is initiated when R̄ĒS̄ goes high. In this way, R̄ĒS̄ can be used to synchronize display frame timing with line frequency. R̄ĒS̄ may also be used to synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

### REFRESH RAM AND CHARACTER ROM INTERFACE

#### MA0-MA13 (Refresh RAM Address Lines)

These 14 signals are active-high outputs used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = "0"), characters are stored in successive memory locations. Thus, the software must be designed such that row and column character coordinates are translated into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = "1"), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

#### RA0-RA4 (Raster Address Lines)

These 5 signals are active-high outputs used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

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# INTERNAL ORGANIZATION



**R6551 Block Diagram**

## Transmitter/Receiver

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the R6551.



**Transmitter/Receiver Clock Circuits**

## Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.

- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.

- Unused data bits are the high-order bits and are "0" for the receiver.

- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0"

## Control Register

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.



**R6551 Control Register**

## Command Register

The Command Register controls specific modes and functions.



**R6551 Command Register**

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# Asynchronous Communication Interface Adapter (ACIA)

The R6551 Asynchronous Communication Interface Adapter (ACIA) provides a program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems

With its on-chip baud rate generator, the R6551 is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.

With the R6551, a crystal is the only required external support component — eliminating the multiple-component support that is typically needed.

In addition, the R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to easily select the R6551's operating modes and check data, parameters and status.

## FEATURES

- Compatible with 8-bit microprocessors
- Full duplex or half duplex operation with buffered receiver and transmitter
- 15 programmable Baud Rates (50 to 19,200)
- Receiver data rate may be identical to baud rate or may be 16 times the external clock input
- Data set/modem control functions
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Software reset
- Program-selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz clock rate
- Single +5V ±5% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

## Ordering Information

| Order Number | Package Type | Frequency | Temperature Range |
|---|---|---|---|
| R6551P | Plastic | 1 MHz | 0°C to +70°C |
| R6551AP | Plastic | 2 MHz | 0°C to +70°C |
| R6551C | Ceramic | 1 MHz | 0°C to +70°C |
| R6551AC | Ceramic | 2 MHz | 0°C to +70°C |

| | |
|---|---|
| VSS ◻ 1 | 28 ◻ R/W̄ |
| CS0 ◻ 2 | 27 ◻ ∅2 |
| C̄S̄1̄ ◻ 3 | 26 ◻ ĪR̄Q̄ |
| R̄Ē̄S̄ ◻ 4 | 25 ◻ D7 |
| RxC ◻ 5 | 24 ◻ D6 |
| XTLI ◻ 6 | 23 ◻ D5 |
| XTLO ◻ 7 | 22 ◻ D4 |
| R̄T̄S̄ ◻ 8 | 21 ◻ D3 |
| C̄T̄S̄ ◻ 9 | 20 ◻ D2 |
| TxD ◻ 10 | 19 ◻ D1 |
| D̄T̄R̄ ◻ 11 | 18 ◻ D0 |
| RxD ◻ 12 | 17 ◻ D̄S̄R̄ |
| RS0 ◻ 13 | 16 ◻ D̄C̄D̄ |
| RS1 ◻ 14 | 15 ◻ VCC |

**R6551 Pin Configuration**

**R6551 Interface Diagram**

DR3

# CMOS 8-Bit Microprocessor

**Features:**

- *Minimum instruction fetch-execute time of 5 µs or 7.5 µs at $V_{DD}=5$ V: 2.5 µs or 3.75 µs at $V_{DD}=10$ V*
- *Any combination of standard RAM and ROM up to 65,536 bytes*
- *Operates with slow memories, up to 1 µs access time at $f_{CL}=4$ MHz*
- *8-bit parallel organization with bidirectional data bus and multiplexed address bus*
- *16 x 16 matrix of registers for use as multiple program counters, data pointers, or data registers*
- *On-chip DMA, interrupt, and flag inputs*
- *Programmable single-bit output port*
- *91 easy-to-use instructions*

**Terminal Assignment**

The RCA-CDP1802A LSI CMOS 8-bit register-oriented central-processing unit (CPU) is designed for use as a general-purpose computing or control element in a wide range of stored-program systems or products.

The CDP1802A includes all of the circuits required for fetching, interpreting, and executing instructions which have been stored in standard types of memories. Extensive input/output (I/O) control features are also provided to facilitate system design.

The 1800 series architecture is designed with emphasis on the total microcomputer system as an integral entity so that systems having maximum flexibility and minimum cost can be realized. The 1800 series CPU also provides a synchronous interface to memories and external controllers for I/O devices, and minimizes the cost of interface controllers. Further, the I/O interface is capable of supporting devices operating in polled, interrupt-driven, or direct memory-access modes.

The CDP1802A and CDP1802AC are functionally identical. They differ in that the CDP1802A has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1802AC a recommended operating voltage range of 4 to 6.5 volts.

These types are supplied in 40-lead dual-in-line side-brazed ceramic packages (D suffix), and 40-lead dual-in-line plastic packages (E suffix). The CDP1802AC is also available in chip form (H suffix).



Fig. 1 - Typical CDP1802A small microprocessor system.

Fig. 6 - Typical power dissipation as a function of clock frequency for BRANCH instruction and IDLE instruction.



Fig. 7 - Typical change in propagation delay as a function of a change in load capacitance.
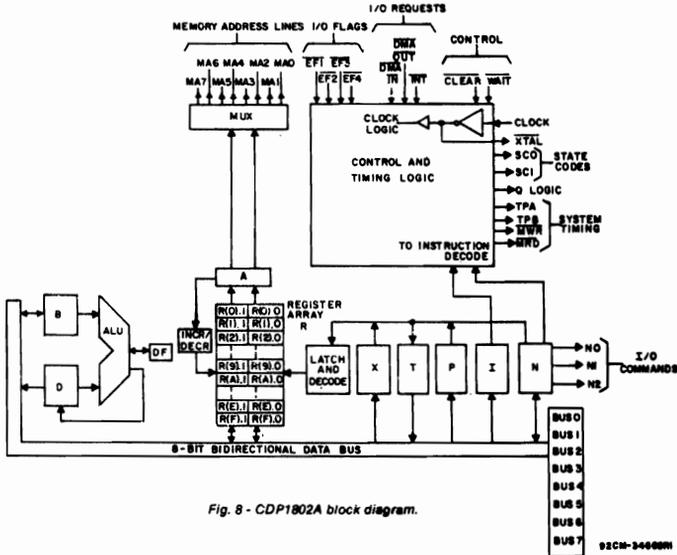


Fig. 8 - CDP1802A block diagram.
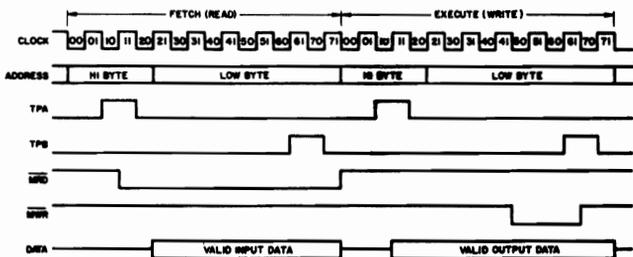


Fig. 9 - Basic dc timing waveforms, one instruction cycle.

# CDP1802A, CDP1802AC

**BUS 0 to BUS 7 (Data Bus):**

8-bit bidirectional DATA BUS lines. These lines are used for transferring data between the memory, the microprocessor, and I/O devices.

**N0 to N2 (I/O) Lines):**

Activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes or device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register.

The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

$\overline{\text{MRD}}$=$V_{CC}$: Data from I/O to CPU and Memory
$\overline{\text{MRD}}$=$V_{SS}$: Data from Memory to I/O

**$\overline{\text{EF1}}$ to $\overline{\text{EF4}}$ (4 Flags):**

These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

**INTERRUPT, DMA-IN, DMA-OUT (3 I/O Requests)**

These inputs are sampled by the CDP1802A during the interval between the leading edge of TPB and the leading edge of TPA.

**Interrupt Action:** X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

**DMA Action:** Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

Note: In the event of concurrent DMA and Interrupt requests, DMA-IN has priority followed by DMA-OUT and then Interrupt.

**SC0, SC1, (2 State Code Lines):**

These outputs indicate that the CPU is: 1) fetching an instruction, or 2) executing an instruction, or 3) processing a DMA request, or 4) acknowledging an interrupt request. The levels of state code are tabulated below. All states are valid at TPA. H=$V_{CC}$, L=$V_{SS}$.

| State Type | State Code Lines | |
|---|---|---|
| | SC1 | SC0 |
| S0 (Fetch) | L | L |
| S1 (Execute) | L | H |
| S2 (DMA) | H | L |
| S3 (Interrupt) | H | H |

**TPA, TPB (2 Timing Pulses):**

Positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. TPA is suppressed in IDLE when the CPU is in the load mode.

**MA0 to MA7 (8 Memory Address Lines):**

In each cycle, the higher-order byte of a 16-bit CPU memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system can be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all 8 higher-order address bits would permit a memory system of 64K bytes.

**MWR (Write Pulse):**

A negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

**MRD (Read Level):**

A low level on $\overline{\text{MRD}}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, $\overline{\text{MRD}}$ is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction. For additional information see Table I.

**Q:**

Single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

**CLOCK:**

Input for externally generated single-phase clock. A typical clock frequency is 6.4 MHz at $V_{CC}$= $V_{DD}$=10 volts. The clock is counted down internally to 8 clock pulses per machine cycle.

**XTAL:**

Connection to be used with clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (10 megohms typ.). Frequency trimming capacitors may be required at terminals 1 and 39. For additional information, see ICAN-6565.

**WAIT, CLEAR (2 Control Lines):**

Provide four control modes as listed in the following truth table:

| CLEAR | WAIT | MODE |
|---|---|---|
| L | L | LOAD |
| L | H | RESET |
| H | L | PAUSE |
| H | H | RUN |

**$V_{DD}$, $V_{SS}$, $V_{CC}$ (Power Levels):**

The internal voltage supply $V_{DD}$ is isolated from the Input/Output voltage supply $V_{CC}$ so that the processor may operate at maximum speed while interfacing with peripheral devices operating at lower voltage. $V_{CC}$ must be less than or equal to $V_{DD}$. All outputs swing from $V_{SS}$ to $V_{CC}$. The recommended input voltage swing is $V_{SS}$ to $V_{CC}$.

# Terminal Assignment Diagrams

## CDP1802 COSMAC Microprocessor

| | | | |
|---|---|---|---|
| CLOCK | 1 | 40 | V_DD |
| WAIT | 2 | 39 | XTAL |
| CLEAR | 3 | 38 | DMA IN |
| Q | 4 | 37 | DMA OUT |
| SC1 | 5 | 36 | INTERRUPT |
| SC0 | 6 | 35 | MWR |
| MRD | 7 | 34 | TPA |
| BUS 7 | 8 | 33 | TPB |
| BUS 6 | 9 | 32 | MA7 |
| BUS 5 | 10 | 31 | MA6 |
| BUS 4 | 11 | 30 | MA5 |
| BUS 3 | 12 | 29 | MA4 |
| BUS 2 | 13 | 28 | MA3 |
| BUS 1 | 14 | 27 | MA2 |
| BUS 0 | 15 | 26 | MA1 |
| V_CC | 16 | 25 | MA0 |
| N2 | 17 | 24 | EF1 |
| N1 | 18 | 23 | EF2 |
| N0 | 19 | 22 | EF3 |
| V_SS | 20 | 21 | EF4 |

TOP VIEW
92CS-29554

## CDP1804 COSMAC Microcomputer

SIGNAL NAME ... SIGNAL NAME

| | | | |
|---|---|---|---|
| CLOCK | 1 | 40 | V_DD |
| WAIT | 2 | 39 | XTAL |
| CLEAR | 3 | 38 | DMA IN |
| Q | 4 | 37 | DMA OUT |
| SC1 | 5 | 36 | INTERRUPT |
| SC0 | 6 | 35 | MWR |
| MRD | 7 | 34 | TPA |
| BUS 7 | 8 | 33 | TPB |
| BUS 6 | 9 | 32 | MA7 |
| BUS 5 | 10 | 31 | MA6 |
| BUS 4 | 11 | 30 | MA5 |
| BUS 3 | 12 | 29 | MA4 |
| BUS 2 | 13 | 28 | MA3 |
| BUS 1 | 14 | 27 | MA2 |
| BUS 0 | 15 | 26 | MA1 |
| EMS | 16 | 25 | MA0 |
| N2 | 17 | 24 | EF1 |
| N1 | 18 | 23 | EF2 |
| N0 | 19 | 22 | EF3 |
| V_SS | 20 | 21 | EF4 |

CONTROL { WAIT, CLEAR }
STATE CODES { SC1, SC0 }
DATA BUS
I/O REQUESTS
TIMING PULSES
MEMORY ADDRESS
I/O COMMANDS { N2, N1, N0 }
I/O FLAGS

TOP VIEW
92CS-31059

## CDP1821 1024 x 1 RAM

| | | | |
|---|---|---|---|
| CS | 1 | 16 | V_DD |
| AA0 | 2 | 15 | DI |
| MA1 | 3 | 14 | MWR |
| MA2 | 4 | 13 | MA9 |
| MA3 | 5 | 12 | MA8 |
| MA4 | 6 | 11 | MA7 |
| DO | 7 | 10 | MA6 |
| V_SS | 8 | 9 | MA5 |

TOP VIEW
92CS-27598

## CDP1822 256 x 4 RAM

| | | | |
|---|---|---|---|
| MA3 | 1 | 22 | V_DD |
| MA2 | 2 | 21 | MA4 |
| MA1 | 3 | 20 | R/W |
| MA0 | 4 | 19 | CS1 |
| MA5 | 5 | 18 | DO |
| MA6 | 6 | 17 | CS2 |
| MA7 | 7 | 16 | DO4 |
| VSS | 8 | 15 | DI4 |
| DI1 | 9 | 14 | DO3 |
| DO1 | 10 | 13 | DI3 |
| DI2 | 11 | 12 | DO2 |

TOP VIEW
92CS-27592R1

## CDP1823 128 x 8 RAM

| | | | |
|---|---|---|---|
| BUS 0 | 1 | 24 | V_DD |
| BUS 1 | 2 | 23 | MA0 |
| BUS 2 | 3 | 22 | MA1 |
| BUS 3 | 4 | 21 | MA2 |
| BUS 4 | 5 | 20 | MA3 |
| BUS 5 | 6 | 19 | MA4 |
| BUS 6 | 7 | 18 | MA5 |
| BUS 7 | 8 | 17 | MA6 |
| CS1 | 9 | 16 | MWR |
| CS2 | 10 | 15 | MRD |
| CS3 | 11 | 14 | CS5 |
| V_SS | 12 | 13 | CS4 |

TOP VIEW
92CS-28703

## CDP1824 32 x 8 RAM

| | | | |
|---|---|---|---|
| MA4 | 1 | 18 | V_DD |
| MA3 | 2 | 17 | MWR |
| MA2 | 3 | 16 | MRD |
| MA1 | 4 | 15 | CS |
| MA0 | 5 | 14 | DO |
| D7 | 6 | 13 | DI |
| D6 | 7 | 12 | D2 |
| D5 | 8 | 11 | D3 |
| V_SS | 9 | 10 | D4 |

TOP VIEW
92CS-27598

## CDP1831 512 x 8 ROM

| | | | |
|---|---|---|---|
| MA7 | 1 | 24 | V_DD |
| MA6 | 2 | 23 | CLOCK |
| MA5 | 3 | 22 | NC |
| MA4 | 4 | 21 | CSI |
| MA3 | 5 | 20 | CS2 |
| MA2 | 6 | 19 | MRD |
| MA1 | 7 | 18 | CE0 |
| MA0 | 8 | 17 | BUS7 |
| BUS 0 | 9 | 16 | BUS6 |
| BUS1 | 10 | 15 | BUS5 |
| BUS2 | 11 | 14 | BUS4 |
| V_SS | 12 | 13 | BUS3 |

TOP VIEW
NC = NO CONNECTION    92CS 27594

## CDP1832 512 x 8 ROM

| | | | |
|---|---|---|---|
| A7 | 1 | 24 | V_DD |
| A6 | 2 | 23 | A8 |
| A5 | 3 | 22 | NC |
| A4 | 4 | 21 | NC |
| A3 | 5 | 20 | CS |
| A2 | 6 | 19 | NC |
| A1 | 7 | 18 | NC |
| BUS0 | 8 | 17 | BUS8 |
| BUS1 | 9 | 16 | BUS7 |
| BUS2 | 10 | 15 | BUS6 |
| BUS3 | 11 | 14 | BUS5 |
| V_SS | 12 | 13 | BUS4 |

TOP VIEW
NC = NO CONNECTION
92CS-27579R1

## CDP1833 1024 x 8 ROM

| | | | |
|---|---|---|---|
| MA7 | 1 | 24 | V_DD |
| MA6 | 2 | 23 | MUX |
| MA5 | 3 | 22 | CE1 |
| MA4 | 4 | 21 | CSI |
| MA3 | 5 | 20 | CS2 |
| MA2 | 6 | 19 | MRD |
| MA1 | 7 | 18 | CE0 |
| MA0 | 8 | 17 | BUS7 |
| BUS 0 | 9 | 16 | BUS6 |
| BUS1 | 10 | 15 | BUS5 |
| BUS2 | 11 | 14 | BUS4 |
| V_SS | 12 | 13 | BUS3 |

TOP VIEW
NC = NO CONNECTION    92CS-28889

## CDP1834
## 1024 x 8 ROM



```
MA7  — 1      24 — VDD
MA6  — 2      23 — MA8
MA5  — 3      22 — MA9
MA4  — 4      21 — NC
MA3  — 5      20 — CS1
MA2  — 6      19 — NC
MA1  — 7      18 — CS2
MA0  — 8      17 — BUS7
BUS0 — 9      16 — BUS6
BUS1 — 10     15 — BUS5
BUS2 — 11     14 — BUS4
Vss  — 12     13 — BUS3
        TOP VIEW
```

NC = NO CONNECTION    92CS 28727

## CDP1852
## Byte I/O



```
CSI/CSI — 1    24 — VDD
MODE  — 2      23 — SR/SR
DI0   — 3      22 — DI7
DO0   — 4      21 — DO7
DI1   — 5      20 — DI6
DO1   — 6      19 — DO6
DI2   — 7      18 — DI5
DO2   — 8      17 — DO5
DI3   — 9      16 — DI4
DO3   — 10     15 — DO4
CLOCK — 11     14 — CLEAR
Vss   — 12     13 — CS2
         TOP VIEW
```

92CS-27572

## CDP1855
## 8-Bit Programmable
## Multiply/Divide Unit



```
CE    — 1      28 — VDD
CLEAR — 2      27 — CN0
CTL   — 3      26 — CN1
C.Q/OF — 4     25 — CI
YL    — 5      24 — YR
ZL    — 6      23 — ZR
SHIFT — 7      22 — BUS 7
CLK   — 8      21 — BUS 6
STB   — 9      20 — BUS 5
RD/WE — 10     19 — BUS 4
RA2   — 11     18 — BUS 3
RA1   — 12     17 — BUS 2
RA0   — 13     16 — BUS 1
Vss   — 14     15 — BUS 0
          TOP VIEW
```

92CS-29965R2

## CDP1835
## 2048 X 8 ROM



```
MA7  — 1      24 — VDD
MA6  — 2      23 — TPA
MA5  — 3      22 — CEI
MA4  — 4      21 — CSI
MA3  — 5      20 — CS2
MA2  — 6      19 — MRD
MA1  — 7      18 — CEO
MA0  — 8      17 — BUS7
BUS0 — 9      16 — BUS6
BUS1 — 10     15 — BUS5
BUS2 — 11     14 — BUS4
Vss  — 12     13 — BUS3
        TOP VIEW
       CDP1835     92CS-32376
```

## CDP1853
## N-Bit Decoder



```
CLOCK A — 1    16 — VDD
N0    — 2      15 — CLOCK B
N1    — 3      14 — N2
OUT 0 — 4      13 — CE
OUT 1 — 5      12 — OUT 4
OUT 2 — 6      11 — OUT 5
OUT 3 — 7      10 — OUT 6
Vss   — 8       9 — OUT 7
          TOP VIEW
```

92CS-28726

## CDP1856
## Bus Buffer (Memory)
## Separator



```
DI0  — 1      16 — VDD
DI1  — 2      15 — CS
DO0  — 3      14 — DB0
DO1  — 4      13 — DB1
DO2  — 5      12 — DB2
DO3  — 6      11 — DB3
DI2  — 7      10 — MRD
Vss  — 8       9 — DI3
        TOP VIEW
```

92CS-28097

## CDP1851
## Programmable
## I/O Interface



```
CLOCK    — 1    40 — VDD
CS       — 2    39 — RD/WE
RA0      — 3    38 — WR/RE
RA1      — 4    37 — TPB
BUS0     — 5    36 — A RDY
BUS1     — 6    35 — A STROBE
BUS2     — 7    34 — A0
BUS3     — 8    33 — A1
BUS4     — 9    32 — A2
BUS5     — 10   31 — A3
BUS6     — 11   30 — A4
BUS7     — 12   29 — A5
CLEAR    — 13   28 — A6
A INT    — 14   27 — A7
B INT    — 15   26 — B7
B RDY    — 16   25 — B6
B STROBE — 17   24 — B5
B0       — 18   23 — B4
B1       — 19   22 — B3
Vss      — 20   21 — B2
           TOP VIEW
```

92CS-31926

## CDP1854A
## UART
## Mode O



```
VDD        — 1    40 — T CLOCK
MODE(Vss)  — 2    39 — EPE
VSS        — 3    38 — WLS 1
RRD        — 4    37 — WLS 2
R BUS 7    — 5    36 — SBS
R BUS 6    — 6    35 — PI
R BUS 5    — 7    34 — CRL
R BUS 4    — 8    33 — T BUS 7
R BUS 3    — 9    32 — T BUS 6
R BUS 2    — 10   31 — T BUS 5
R BUS 1    — 11   30 — T BUS 4
R BUS 0    — 12   29 — T BUS 3
PE         — 13   28 — T BUS 2
FE         — 14   27 — T BUS 1
OE         — 15   26 — T BUS 0
SFD        — 16   25 — SDO
R CLOCK    — 17   24 — TSRE
DAR        — 18   23 — THRL
DA         — 19   22 — THRE
SDI        — 20   21 — MR
            TOP VIEW
```

92CS-28455R1

## CDP1857
## I/O Bus Buffer



```
DI0  — 1      16 — VDD
DI1  — 2      15 — CS
DO0  — 3      14 — DB0
DO1  — 4      13 — DB1
DO2  — 5      12 — DB2
DO3  — 6      11 — DB3
DI2  — 7      10 — MRD
Vss  — 8       9 — DI3
        TOP VIEW
```

92CS-28097

## CDP1858
4-Bit Latch

```
CLOCK   1      16  VDD
MAO     2      15  ENABLE
MAI     3      14  MA2
CSO     4      13  MA3
CS1     5      12  CEO
CS2     6      11  CE1
CS3     7      10  CE2
VSS     8       9  CE3
        TOP VIEW
                        92CS-31953
```

## CDP1862
Color Generator
Controller

```
RD      1      24  VDD
RESET   2      23  R LUM
CON     3      22  G LUM
B CHR   4      21  GD
B LUM   5      20  BLG LUM
BKG     6      19  G CHR
LD CLK  7      18  R CHR
STP     8      17  BKG CHR
CLK OUT 9      16  BD
SYNC   10      15  BURST
LUM IN 11      14  XTAL
VSS    12      13  XTAL
        TOP VIEW
                        92CS-31665
```

## CDP1866
4-Bit Latch and Decoder
Memory Interface

```
MAO     1      18  VDD
MAI     2      17  CLOCK
MA2     3      16  CE1
MA3     4      15  CE2
MRD     5      14  CE3
MWR     6      13  CSO
A8      7      12  CS1
A9      8      11  CS2
VSS     9      10  CS3
        TOP VIEW
                        92CS-30797RI
```

## CDP1859
4-Bit Latch

```
CLOCK   1      16  VDD
MAO     2      15  ENABLE
MAI     3      14  MA2
A8      4      13  MA3
A8      5      12  CEO
A9      6      11  CE1
A9      7      10  CE2
VSS     8       9  CE3
        TOP VIEW
```

## CDP1863
Programmable
Frequency Generator

```
RESET   1      16  VDD
CLK 2   2      15  OE
CLK 1   3      14  OUT
STR     4      13  DI7
DIO     5      12  DI6
DI1     6      11  DI5
DI2     7      10  DI4
VSS     8       9  DI3
        TOP VIEW
                        92CS-31696
```

## CDP1867
4-Bit Latch and Decoder
Memory Interface

```
MAO     1      18  VDD
MAI     2      17  CLOCK
MA2     3      16  CE1
MA3     4      15  CE2
MRD     5      14  CE3
MWR     6      13  CE4
A8      7      12  CS
A9      8      11  AII
VSS     9      10  AIO
        TOP VIEW
                        92CS-30798RI
```

## CDP1861
Video Display
Controller

```
CLOCK       1      24  VDD
DMA REQ     2      23  CLEAR
INT REQ     3      22  CONTROL A
SYNC REF    4      21  CONTROL B
LOAD        5      20  DI7
COMP SYNC   6      19  DI6
VIDEO       7      18  DI5
RESET IN    8      17  DI4
DISP-STATUS 9      16  DI3
DISP ON    10      15  DI2
DISP OFF   11      14  DI1
VSS        12      13  DIO
        TOP VIEW
                        92CS-29730
```

## CDP1864
PAL-Compatible
TV Interface

```
INLACE   1      40  VDD
CLK IN   2      39  AUD
CLR OUT  3      38  CLR IN
AOE      4      37  DMAO
SCI      5      36  INT
SCO      6      35  TPA
MRD      7      34  TPB
BUS 7    8      33  EVS
BUS 6    9      32  V SYNC
BUS 5   10      31  H SYNC
BUS 4   11      30  C SYNC
BUS 3   12      29  RED
BUS 2   13      28  BLUE
BUS 1   14      27  GREEN
BUS 0   15      26  BCK GND
CON     16      25  BURST
N2      17      24  ALT
EF      18      23  R DATA
NO      19      22  B DATA
VSS     20      21  G DATA
        TOP VIEW
                        92CS-31899
```

## CDP1868
4-Bit Latch and Decoder
Memory Interface

```
MAO     1      18  VDD
MA1     2      17  CLOCK
MA2     3      16  CE1
MA3     4      15  CE2
MRD     5      14  CE3
MWR     6      13  CSO
A8      7      12  CS1
A9      8      11  CS2
VSS     9      10  CS3
        TOP VIEW
                        92CS-30797RI
```

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# CDP1869
## Address and Sound Generator

| Pin | | | Pin |
|---|---|---|---|
| TPA | 1 | 40 | V_DD |
| TPB | 2 | 39 | PMSEL |
| MRD | 3 | 38 | PMWR |
| MWR | 4 | 37 | CMSEL* |
| MA0/8 | 5 | 36 | CMWR |
| MA1/9 | 6 | 35 | PMA0 |
| MA2/10 | 7 | 34 | PMA1 |
| MA3/11 | 8 | 33 | PMA2 |
| MA4/12 | 9 | 32 | PMA3 |
| MA5/13 | 10 | 31 | PMA4 |
| MA6/14 | 11 | 30 | PMA5 |
| MA7/15 | 12 | 29 | PMA6 |
| N0 | 13 | 28 | PMA7 |
| N1 | 14 | 27 | PMA8 |
| N2 | 15 | 26 | PMA9 |
| *H SYNC | 16 | 25 | CMA3/PMA10 |
| *DISPLAY | 17 | 24 | CMA2 |
| *ADDRSTB | 18 | 23 | CMA1 |
| SOUND | 19 | 22 | CMA0 |
| V_SS | 20 | 21 | N·3* |

*INTERCHIP CONNECTIONS

TOP VIEW

92CM-31913

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# CDP1872
## Hi-Speed 8-Bit Address Latch

| Pin | | | Pin |
|---|---|---|---|
| DS_1 | 1 | 22 | V_DD |
| DI_1 | 2 | 21 | DI_8 |
| DO_1 | 3 | 20 | DO_8 |
| DI_2 | 4 | 19 | DI_7 |
| DO_2 | 5 | 18 | DO_7 |
| DI_3 | 6 | 17 | DI_6 |
| DO_3 | 7 | 16 | DO_6 |
| DI_4 | 8 | 15 | DI_5 |
| DO_4 | 9 | 14 | DO_5 |
| CLOCK | 10 | 13 | CLR |
| V_SS | 11 | 12 | DS_2 |

TOP VIEW

92CS-32373

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# CDP18U43
## 1K x 8 UV EPROM

| Pin | | | Pin |
|---|---|---|---|
| MA7 | 1 | 24 | V_DD |
| MA6 | 2 | 23 | TPA |
| MA5 | 3 | 22 | Vpp |
| MA4 | 4 | 21 | CS1 |
| MA3 | 5 | 20 | CS2/PGM |
| MA2 | 6 | 19 | MRD |
| MA1 | 7 | 18 | V_SAT |
| MA0 | 8 | 17 | BUS7 |
| BUS0 | 9 | 16 | BUS6 |
| BUS1 | 10 | 15 | BUS5 |
| BUS2 | 11 | 14 | BUS4 |
| V_SS | 12 | 13 | BUS3 |

TOP VIEW

92CS-32367

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# CDP1870
## Color Video Generator

| Pin | | | Pin |
|---|---|---|---|
| PREDISPLAY | 1 | 40 | V_DD |
| *DISPLAY | 2 | 39 | PAL/NTSC |
| PCB | 3 | 38 | CPUCLK |
| CCB1 | 4 | 37 | XTAL (DOT) |
| BUS7 | 5 | 36 | XTAL (DOT) |
| CCB0 | 6 | 35 | ADDRSTB* |
| BUS6 | 7 | 34 | MRD |
| CDB5 | 8 | 33 | TPB |
| BUS5 | 9 | 32 | CMSEL* |
| BUS4 | 10 | 31 | BURST |
| CDB4 | 11 | 30 | H SYNC* |
| CDB3 | 12 | 29 | COMPSYNC |
| BUS3 | 13 | 28 | LUM |
| CDB2 | 14 | 27 | PAL CHROM |
| BUS2 | 15 | 26 | NTSC CHROM |
| CDB1 | 16 | 25 | XTAL (CHROM) |
| BUS1 | 17 | 24 | XTAL (CHROM) |
| CDB0 | 18 | 23 | CHS |
| BUS0 | 19 | 22 | CVS |
| V_SS | 20 | 21 | N·3* |

*INTERCHIP CONNECTIONS

TOP VIEW
COLOR VIDEO GENERATOR

92CM-31913

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# CDP1873
## Hi-Speed 1 of 8 Decoder

| Pin | | | Pin |
|---|---|---|---|
| A_0 | 1 | 16 | V_DD |
| A_1 | 2 | 15 | DO_0 |
| A_2 | 3 | 14 | DO_1 |
| E_1 | 4 | 13 | DO_2 |
| E_2 | 5 | 12 | DO_3 |
| E_3 | 6 | 11 | DO_4 |
| DO_7 | 7 | 10 | DO_5 |
| V_SS | 8 | 9 | DO_6 |
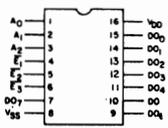
TOP VIEW

92CS-32374

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# CDP27C58
## 1K x 8 UV EROM

| Pin | | | Pin |
|---|---|---|---|
| A7 | 1 | 24 | V_DD |
| A6 | 2 | 23 | A8 |
| A5 | 3 | 22 | A9 |
| A4 | 4 | 21 | Vpp |
| A3 | 5 | 20 | OE |
| A2 | 6 | 19 | V_SAT |
| A1 | 7 | 18 | PGM/CE |
| A0 | 8 | 17 | O_7 |
| O_0 | 9 | 16 | O_6 |
| O_1 | 10 | 15 | O_5 |
| O_2 | 11 | 14 | O_4 |
| V_SS | 12 | 13 | O_3 |
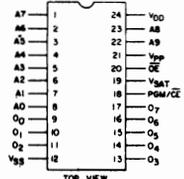
TOP VIEW

92CS-32377

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# CDP1871
## Keyboard Encoder

| Pin | | | Pin |
|---|---|---|---|
| D1 | 1 | 40 | V_DD |
| D2 | 2 | 39 | SHIFT |
| D3 | 3 | 38 | CONTROL |
| D4 | 4 | 37 | ALPHA |
| D5 | 5 | 36 | DEBOUNCE |
| D6 | 6 | 35 | EFXB |
| D7 | 7 | 34 | TPB |
| D8 | 8 | 33 | EFXA |
| D9 | 9 | 32 | BUS7 |
| D10 | 10 | 31 | BUS6 |
| D11 | 11 | 30 | BUS5 |
| S1 | 12 | 29 | BUS4 |
| S2 | 13 | 28 | BUS3 |
| S3 | 14 | 27 | BUS2 |
| S4 | 15 | 26 | BUS1 |
| S5 | 16 | 25 | BUS0 |
| S6 | 17 | 24 | MRD |
| S7 | 18 | 23 | NXC |
| S8 | 19 | 22 | NXB |
| V_SS | 20 | 21 | NXA |

92CS-32581

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# CDP18U42CD
## 256 x 8 UV EPROM

| Pin | | | Pin |
|---|---|---|---|
| MA2 | 1 | 24 | V_SS |
| MA1 | 2 | 23 | V_DD |
| MA0 | 3 | 22 | V_SAT |
| BUS0 | 4 | 21 | MA3 |
| BUS1 | 5 | 20 | MA4 |
| BUS2 | 6 | 19 | MA5 |
| BUS3 | 7 | 18 | MA6 |
| BUS4 | 8 | 17 | MA7 |
| BUS5 | 9 | 16 | CS3 |
| BUS6 | 10 | 15 | CS2 |
| BUS7 | 11 | 14 | CS1 |
| V_CC | 12 | 13 | PRB |
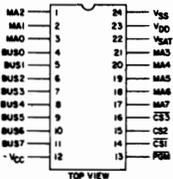
TOP VIEW

92CS-31960

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# MWS5101, MWS5101A
## 256 x 4 RAM

| Pin | | | Pin |
|---|---|---|---|
| A5 | 1 | 22 | V_DD |
| A2 | 2 | 21 | A4 |
| A1 | 3 | 20 | R/W |
| A0 | 4 | 19 | CE |
| A6 | 5 | 18 | DO 0 |
| A7 | 6 | 17 | CS2 |
| V_SS | 7 | 16 | DO4 |
| DI1 | 8 | 15 | DO3 |
| DO1 | 9 | 14 | DI3 |
| DI2 | 10 | 13 | DI3 |
| DI2 | 11 | 12 | DO2 |

TOP VIEW

92CS-28076A

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# F8 Central Processing Unit MK 3850

## FEATURES

☐ N-channel Isoplanar MOS technology

☐ 2 μs cycle time

☐ 64 byte RAM on the CPU chip

☐ Two bi-directional, 8-bit I/O ports

☐ 8-bit arithmetic and logic unit, supporting both binary and decimal arithmetic

☐ Interrupt control logic

☐ Both external and crystal clock generating modes

☐ Over 70 instructions

☐ Low power dissipation—typically less than 330mW

## GENERAL DESCRIPTION

The MK3850 is the Central Processing Unit (CPU) for the F8 Microprocessor family. It is used in conjunction with other F8 family devices to configure the optimal microprocessor system for the amount of RAM, ROM/PROM, and I/O required in the users application. A minimum system may be configured with as few as two devices (CPU & PSU), while larger systems may have up to 64K bytes of memory, 128 I/O ports, direct memory acccess, and even multiple processors. Single chip microcomputer systems are also possible using the MK3870

| PIN NAME | DESCRIPTION | TYPE |
|---|---|---|
| DB0-DB7 | Data Bus Lines | Bi-directional (3-State) |
| Φ, WRITE | Clock Lines | Output |
| I/O 00-I/O 07 | I/O Port Zero | Input/Output |
| I/O 10-I/O 17 | I/O Port One | Input/Output |
| RC | RC Network Pin | Input |
| ROMC0-ROMC4 | Control Lines | Output |
| EXT RES | External Reset | Input |
| INT REQ | Interrupt Request | Input |
| ICB | Interrupt Control Bit | Output |
| XTLX | Crystal Clock Line | Output |
| XTLY | External Clock Line | Input |
| VSS, VDD, VGG | Power Lines | Input |

### SINGLE CHIP MK3870



### F8 FAMILY
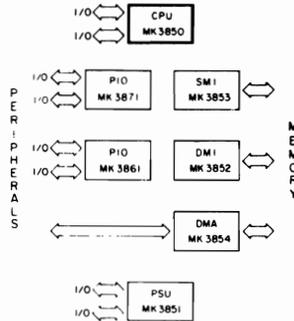


## PIN CONNECTIONS
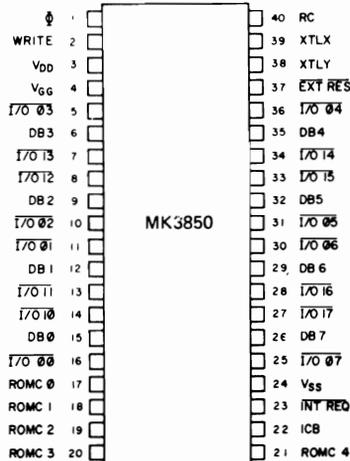
# 8086
## 16-BIT HMOS MICROPROCESSOR
### 8086/8086-2/8086-1*

- Direct Addressing Capability 1 MByte of Memory
- Architecture Designed for Powerful Assembly Language and Efficient High Level Languages
- 14 Word, by 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Operations
- 8 and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide

- Range of Clock Rates:
  5 MHz for 8086,
  8 MHz for 8086-2,
  10 MHz for 8086-1
- MULTIBUS® System Compatible Interface
- Available in EXPRESS
  — Standard Temperature Range
  — Extended Temperature Range
- Available in 40-Lead Cerdip and Plastic Package
  (See Packaging Spec. Order #231369)

The Intel 8086 high performance 16-bit CPU is available in three clock rates: 5, 8 and 10 MHz. The CPU is implemented in N-Channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CERDIP or plastic package. The 8086 operates in both single processor and multiple processor configurations to achieve high performance levels.

*Changes from the 1985 handbook specification have been made for the 8086-1. See A.C. Characteristics TGVCH and TCLGL.
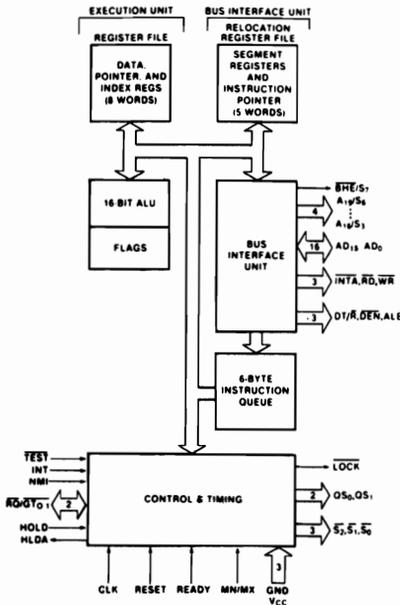


Figure 1. 8086 CPU Block Diagram          231455-1
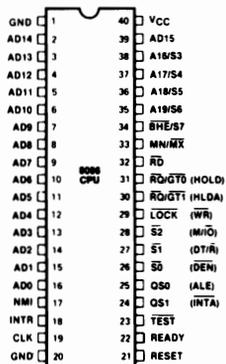


231455-2

**40 Lead**

**Figure 2. 8086 Pin Configuration**

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## Table 1. Pin Description

*The following pin function descriptions are for 8086 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 8086 (without regard to additional bus buffers).*

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| $AD_{15}-AD_0$ | 2–16, 39 | I/O | **ADDRESS DATA BUS:** These lines constitute the time multiplexed memory/IO address ($T_1$), and data ($T_2$, $T_3$, $T_W$, $T_4$) bus. $A_0$ is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins $D_7-D_0$. It is LOW during $T_1$ when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use $A_0$ to condition chip select functions. (See $\overline{BHE}$.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge". |
| $A_{19}/S_6$, $A_{18}/S_5$, $A_{17}/S_4$, $A_{16}/S_3$ | 35–38 | O | **ADDRESS/STATUS:** During $T_1$ these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during $T_2$, $T_3$, $T_W$, $T_4$. The status of the interrupt enable FLAG bit ($S_5$) is updated at the beginning of each CLK cycle. $A_{17}/S_4$ and $A_{16}/S_3$ are encoded as shown. This information indicates which relocation register is presently being used for data accessing. These lines float to 3-state OFF during local bus "hold acknowledge." |

| $A_{17}/S_4$ | $A_{16}/S_3$ | Characteristics |
|---|---|---|
| 0 (LOW) | 0 | Alternate Data |
| 0 | 1 | Stack |
| 1 (HIGH) | 0 | Code or None |
| 1 | 1 | Data |
| $S_6$ is 0 (LOW) | | |

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| $\overline{BHE}/S_7$ | 34 | O | **BUS HIGH ENABLE/STATUS:** During $T_1$ the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins $D_{15}-D_8$. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during $T_1$ for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The $S_7$ status information is available during $T_2$, $T_3$, and $T_4$. The signal is active LOW, and floats to 3-state OFF in "hold". It is LOW during $T_1$ for the first interrupt acknowledge cycle. |

| $\overline{BHE}$ | $A_0$ | Characteristics |
|---|---|---|
| 0 | 0 | Whole word |
| 0 | 1 | Upper byte from/to odd address |
| 1 | 0 | Lower byte from/to even address |
| 1 | 1 | None |

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| $\overline{RD}$ | 32 | O | **READ:** Read strobe indicates that the processor is performing a memory of I/O read cycle, depending on the state of the $S_2$ pin. This signal is used to read devices which reside on the 8086 local bus. $\overline{RD}$ is active LOW during $T_2$, $T_3$ and $T_W$ of any read cycle, and is guaranteed to remain HIGH in $T_2$ until the 8086 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge". |

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**Table 1. Pin Description** (Continued)

| Symbol | Pin No. | Type | Name and Function |
|--------|---------|------|-------------------|
| READY | 22 | I | **READY:** is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/IO is synchronized by the 8284A Clock Generator to form READY. This signal is active HIGH. The 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met. |
| INTR | 18 | I | **INTERRUPT REQUEST:** is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH. |
| TEST | 23 | I | **TEST:** input is examined by the "Wait" instruction. If the $\overline{\text{TEST}}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK. |
| NMI | 17 | I | **NON-MASKABLE INTERRUPT:** an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized. |
| RESET | 21 | I | **RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized. |
| CLK | 19 | I | **CLOCK:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing. |
| $V_{CC}$ | 40 | | $V_{CC}$: +5V power supply pin. |
| GND | 1, 20 | | **GROUND** |
| MN/$\overline{\text{MX}}$ | 33 | I | **MINIMUM/MAXIMUM:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections. |

*The following pin function descriptions are for the 8086/8288 system in maximum mode (i.e., MN/$\overline{MX}$ = $V_{SS}$). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.*

| $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ | 26–28 | O | **STATUS:** active during $T_4$, $T_1$, and $T_2$ and is returned to the passive state (1, 1, 1) during $T_3$ or during $T_W$ when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$, or $\overline{S_0}$ during $T_4$ is used to indicate the beginning of a bus cycle, and the return to the passive state in $T_3$ or $T_W$ is used to indicate the end of a bus cycle. |

**Table 1. Pin Description** (Continued)

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ (Continued) | 26–28 | O | These signals float to 3-state OFF in "hold acknowledge". These status lines are encoded as shown. |
| $\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$ | 30, 31 | I/O | **REQUEST/GRANT:** pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ pins have internal pull-up resistors and may be left unconnected. The request/grant sequence is as follows (see Figure 9): 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 8086 (pulse 1). 2. During a $T_4$ or $T_1$ clock cycle, a pulse 1 CLK wide from the 8086 to the requesting master (pulse 2), indicates that the 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". 3. A pulse 1 CLK wide from the requesting master indicates to the 8086 (pulse 3) that the "hold" request is about to end and that the 8086 can reclaim the local bus at the next CLK. Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during $T_4$ of the cycle when all the following conditions are met: 1. Request occurs on or before $T_2$. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied. |
| $\overline{LOCK}$ | 29 | O | **$\overline{LOCK}$:** output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge". |

| $\overline{S_2}$ | $\overline{S_1}$ | $\overline{S_0}$ | Characteristics |
|---|---|---|---|
| 0 (LOW) | 0 | 0 | Interrupt Acknowledge |
| 0 | 0 | 1 | Read I/O Port |
| 0 | 1 | 0 | Write I/O Port |
| 0 | 1 | 1 | Halt |
| 1 (HIGH) | 0 | 0 | Code Access |
| 1 | 0 | 1 | Read Memory |
| 1 | 1 | 0 | Write Memory |
| 1 | 1 | 1 | Passive |

### Table 1. Pin Description (Continued)

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| QS$_1$, QS$_0$ | 24, 25 | O | **QUEUE STATUS:** The queue status is valid during the CLK cycle after which the queue operation is performed.<br>QS$_1$ and QS$_0$ provide status to allow external tracking of the internal 8086 instruction queue. |

| QS$_1$ | QS$_0$ | Characteristics |
|---|---|---|
| 0 (LOW) | 0 | No Operation |
| 0 | 1 | First Byte of Op Code from Queue |
| 1 (HIGH) | 0 | Empty the Queue |
| 1 | 1 | Subsequent Byte from Queue |

*The following pin function descriptions are for the 8086 in minimum mode (i.e., MN/$\overline{MX}$ = V$_{CC}$). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.*

| | | | |
|---|---|---|---|
| M/$\overline{IO}$ | 28 | O | **STATUS LINE:** logically equivalent to S$_2$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T$_4$ preceding a bus cycle and remains valid until the final T$_4$ of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ floats to 3-state OFF in local bus "hold acknowledge". |
| $\overline{WR}$ | 29 | O | **WRITE:** indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T$_2$, T$_3$ and T$_W$ of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge". |
| $\overline{INTA}$ | 24 | O | **$\overline{INTA}$:** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T$_2$, T$_3$ and T$_W$ of each interrupt acknowledge cycle. |
| ALE | 25 | O | **ADDRESS LATCH ENABLE:** provided by the processor to latch the address into the 8282/8283 address latch. It is a HIGH pulse active during T$_1$ of any bus cycle. Note that ALE is never floated. |
| DT/$\overline{R}$ | 27 | O | **DATA TRANSMIT/RECEIVE:** needed in minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to $\overline{S_1}$ in the maximum mode, and its timing is the same as for M/$\overline{IO}$. (T = HIGH, R = LOW.) This signal floats to 3-state OFF in local bus "hold acknowledge". |
| $\overline{DEN}$ | 26 | O | **DATA ENABLE:** provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T$_2$ until the middle of T$_4$, while for a write cycle it is active from the beginning of T$_2$ until the middle of T$_4$. $\overline{DEN}$ floats to 3-state OFF in local bus "hold acknowledge". |
| HOLD, HLDA | 31, 30 | I/O | **HOLD:** indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T$_1$ clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer the HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines.<br>The same rules as for $\overline{RQ}$/$\overline{GT}$ apply regarding when the local bus will be released.<br>HOLD is not asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time. |

# FUNCTIONAL DESCRIPTION

## General Operation

The internal functions of the 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 1.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage. See the Instruction Set description and architectural descriptions.

### MEMORY ORGANIZATION

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 3a.)

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. This performance penalty does not occur for instruction fetches, only word operands.

Physically, the memory is organized as a high bank $(D_{15}-D_8)$ and a low bank $(D_7-D_0)$ of 512K 8-bit bytes addressed in parallel by the processor's address lines $A_{19}-A_1$. Byte data with even addresses is transferred on the $D_7-D_0$ bus lines while odd addressed byte data $(A_0$ HIGH) is transferred on the $D_{15}-D_8$ bus lines. The processor provides two enable signals, $\overline{BHE}$ and $A_0$, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor to the byte level as necessary.

| Memory Reference Need | Segment Register Used | Segment Selection Rule |
|---|---|---|
| Instructions | CODE (CS) | Automatic with all instruction prefetch. |
| Stack | STACK (SS) | All stack pushes and pops. Memory references relative to BP base register except data references. |
| Local Data | DATA (DS) | Data references when: relative to stack, destination of string operation, or explicitly overridden. |
| External (Global) Data | EXTRA (ES) | Destination of string operations: explicitly selected using a segment override. |

**Figure 3a. Memory Organization**

In referencing word data the BIU requires one or two memory cycles depending on whether or not the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.
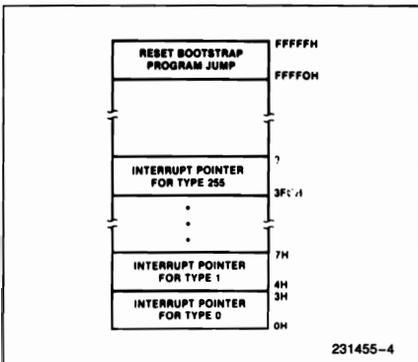


**Figure 3b. Reserved Memory Locations**

Certain locations in memory are reserved for specific CPU operations (see Figure 3b). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt types has its service routine pointed to by a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

## MINIMUM AND MAXIMUM MODES

The requirements for supporting minimum and maximum 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8086 is equipped with a strap pin (MN/$\overline{\text{MX}}$) which defines the system configuration. The definition of a certain subset of the pins changes dependent on the condition of the strap pin. When MN/$\overline{\text{MX}}$ pin is strapped to GND, the 8086 treats pins 24 through 31 in maximum mode. An 8288 bus controller interprets status information coded into $\overline{S_0}$, $\overline{S_2}$, $\overline{S_2}$ to generate bus timing and control signals compatible with the MULTIBUS® architecture. When the MN/$\overline{\text{MX}}$ pin is strapped to $V_{CC}$, the 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 2. Examples of minimum mode and maximum mode systems are shown in Figure 4.

### BUS OPERATION

The 8086 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as $T_1$, $T_2$, $T_3$ and $T_4$ (see Figure 5). The address is emitted from the processor during $T_1$ and data transfer occurs on the bus during $T_3$ and $T_4$. $T_2$ is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states ($T_W$) are inserted between $T_3$ and $T_4$. Each inserted "Wait" state is of the same duration as a CLK cycle. Periods
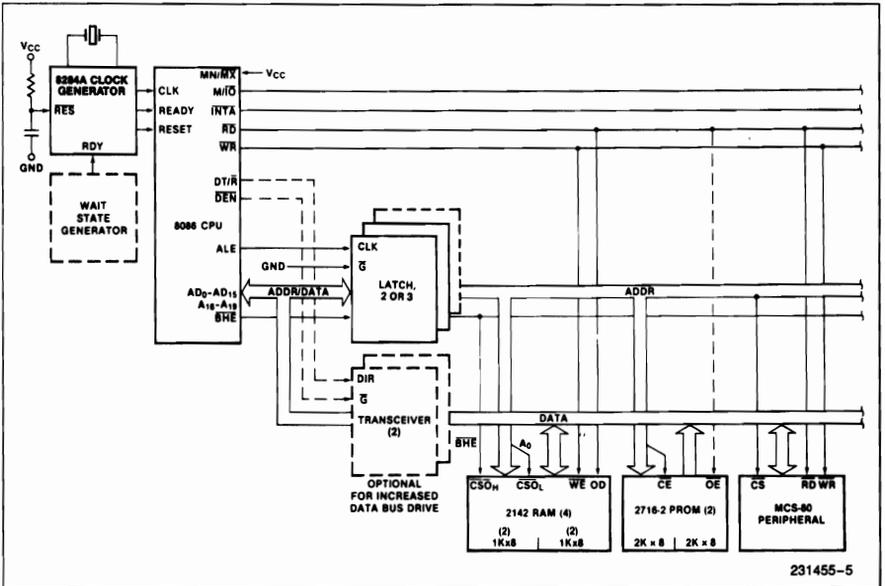
**Figure 4a. Minimum Mode 8086 Typical Configuration**
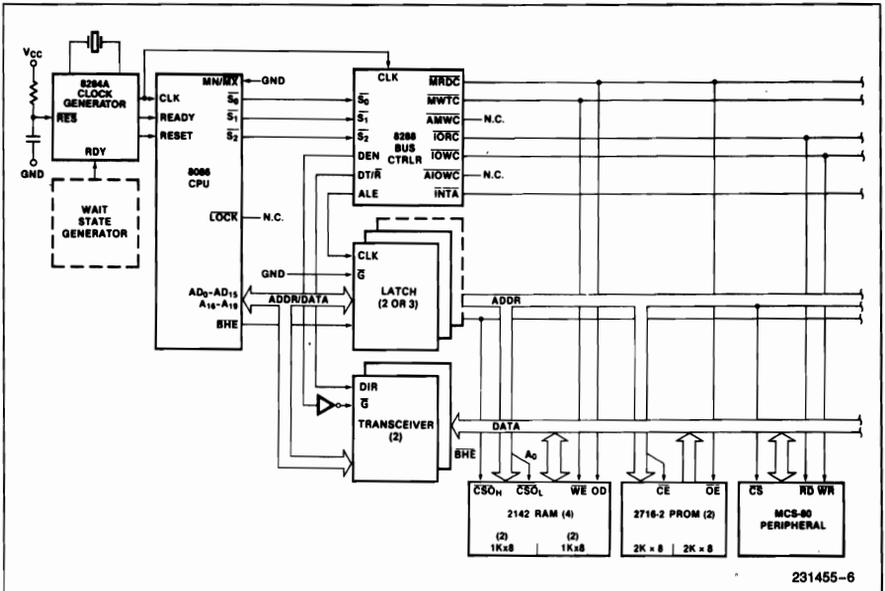


**Figure 4b. Maximum Mode 8086 Typical Configuration**

can occur between 8086 bus cycles. These are re-ferred to as "Idle" states (T$_I$) or inactive CLK cycles. The processor uses these cycles for internal house-keeping.

During T$_1$ of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid ad-dress and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

| $\overline{S_2}$ | $\overline{S_1}$ | $\overline{S_0}$ | Characteristics |
|---|---|---|---|
| 0 (LOW) | 0 | 0 | Interrupt Acknowledge |
| 0 | 0 | 1 | Read I/O |
| 0 | 1 | 0 | Write I/O |
| 0 | 1 | 1 | Halt |
| 1 (HIGH) | 0 | 0 | Instruction Fetch |
| 1 | 0 | 1 | Read Data from Memory |
| 1 | 1 | 0 | Write Data to Memory |
| 1 | 1 | 1 | Passive (no bus cycle) |



Figure 5. Basic System Timing

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Status bits $S_3$ through $S_7$ are multiplexed with high-order address bits and the $\overline{BHE}$ signal, and are therefore valid during $T_2$ through $T_4$. $S_3$ and $S_4$ indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

| $S_4$ | $S_3$ | Characteristics |
|-------|-------|-----------------|
| 0 (LOW) | 0 | Alternate Data (extra segment) |
| 0 | 1 | Stack |
| 1 (HIGH) | 0 | Code or None |
| 1 | 1 | Data |

$S_5$ is a reflection of the PSW interrupt enable bit. $S_6 = 0$ and $S_7$ is a spare status bit.

## I/O ADDRESSING

In the 8086, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines $A_{15}$–$A_0$. The address lines $A_{19}$–$A_{16}$ are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the $D_7$–$D_0$ bus lines and odd addressed bytes on $D_{15}$–$D_8$. Care must be taken to assure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

## External Interface

### PROCESSOR RESET AND INITIALIZATION

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 8086 RESET is required to be HIGH for greater than 4 CLK cycles. The 8086 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 10 CLK cycles. After this interval the 8086 operates normally beginning with the instruction in absolute location FFFF0H (see Figure 3b). The details of this operation are specified in the Instruction Set description of the MCS-86 Family User's Manual. The RESET input is internally synchronized to the processor clock. At initialization the HIGH-to-LOW transition of RESET must occur no sooner than 50 μs after power-up, to allow complete initialization of the 8086.

NMI asserted prior to the 2nd clock after the end of RESET will not be honored. If NMI is asserted after that point and during the internal reset sequence, the processor may execute one instruction before responding to the interrupt. A hold request active immediately after RESET will be honored before the first instruction fetch.

All 3-state outputs float to 3-state OFF during RESET. Status is active in the idle state for the first clock after RESET becomes active and then floats to 3-state OFF. ALE and HLDA are driven low.

## INTERRUPT OPERATIONS

Interrupt operations fall into two classes; software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see Figure 3b), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location.

## NON-MASKABLE INTERRUPT (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt. (See Instruction Set description.)

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any high-going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

## MASKABLE NTERRUPT (INTR)

The 8086 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable FLAG status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block-type instruction. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 6) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 8086 emits the LOCK signal from $T_2$ of the first bus cycle until $T_2$ of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle a byte is fetched from the external interrupt system (e.g., 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when it restores the FLAGS.

## HALT

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode, the processor issues appropriate HALT status on $\overline{S}_2$, $\overline{S}_1$, and $\overline{S}_0$; and the 8288 bus controller issues one ALE. The 8086 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator. An interrupt request or RESET will force the 8086 out of the "HALT" state.

## READ/MODIFY/WRITE (SEMAPHORE) OPERATIONS VIA LOCK

The $\overline{LOCK}$ status information is provided by the processor when directly consecutive bus cycles are required during the execution of an instruction. This provides the processor with the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without the possibility of another system bus master receiving intervening memory cycles. This is useful in multi-processor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (forced LOW) in the clock cycle following the one in which the software "LOCK" prefix instruction is decoded by the EU. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While $\overline{LOCK}$ is active a request on a RQ/GT pin will be recorded and then honored at the end of the LOCK.
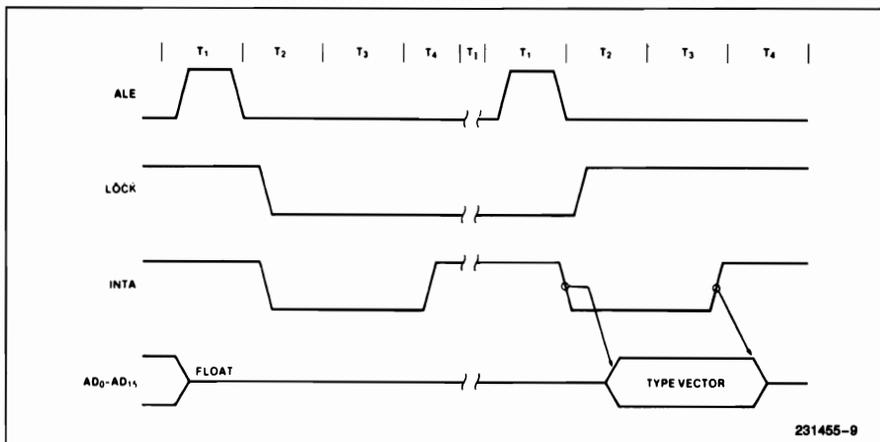


**Figure 6. Interrupt Acknowledge Sequence**

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## EXTERNAL SYNCHRONIZATION VIA TEST

As an alternative to the interrupts and general I/O capabilities, the 8086 provides a single software-testable input known as the $\overline{TEST}$ signal. At any time the program may execute a WAIT instruction. If at that time the $\overline{TEST}$ signal is inactive (HIGH), program execution becomes suspended while the processor waits for $\overline{TEST}$ to become active. It must remain active for at least 5 CLK cycles. The WAIT instruction is re-executed repeatedly until that time. This activity does not consume bus cycles. The processor remains in an idle state while waiting. All 8086 drivers go to 3-state OFF if bus "Hold" is entered. If interrupts are enabled, they may occur while the processor is waiting. When this occurs the processor fetches the WAIT instruction one extra time, processes the interrupt, and then re-fetches and re-executes the WAIT instruction upon returning from the interrupt.

## Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 4a and 4b, respectively. In minimum mode, the MN/$\overline{MX}$ pin is strapped to $V_{CC}$ and the processor emits bus control signals in a manner similar to the 8085. In maximum mode, the MN/$\overline{MX}$ pin is strapped to $V_{SS}$ and the processor emits coded status information which the 8288 bus controller uses to generate MULTIBUS compatible bus control signals. Figure 5 illustrates the signal timing relationships.



| AX | AH | AL | ACCUMULATOR |
|----|----|----|-------------|
| BX | BH | BL | BASE |
| CX | CH | CL | COUNT |
| DX | DH | DL | DATA |

| | SP | | STACK POINTER |
|--|----|--|---------------|
| | BP | | BASE POINTER |
| | SI | | SOURCE INDEX |
| | DI | | DESTINATION INDEX |

| IP | | INSTRUCTION POINTER |
|----|--|---------------------|
| FLAGS$_H$ | FLAGS$_L$ | STATUS FLAGS |

| CS | | CODE SEGMENT |
|----|--|--------------|
| DS | | DATA SEGMENT |
| SS | | STACK SEGMENT |
| ES | | EXTRA SEGMENT |

231455-10
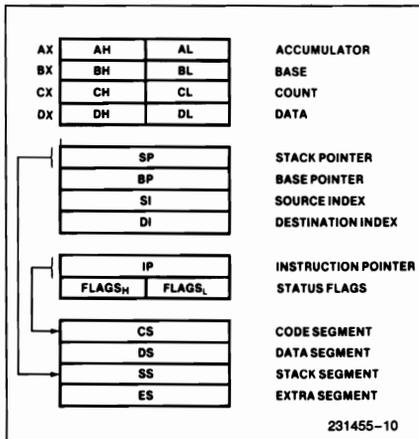
**Figure 7. 8086 Register Model**

## SYSTEM TIMING—MINIMUM SYSTEM

The read cycle begins in $T_1$ with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the local bus at this time, into the address latch. The $\overline{BHE}$ and $A_0$ signals address the low, high, or both bytes. From $T_1$ to $T_4$ the M/$\overline{IO}$ signal indicates a memory or I/O operation. At $T_2$ the address is removed from the local bus and the bus goes to a high impedance state. The read control signal is also asserted at $T_2$. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver is required to buffer the 8086 local bus, signals DT/$\overline{R}$ and $\overline{DEN}$ are provided by the 8086.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/$\overline{IO}$ signal is again asserted to indicate a memory or I/O write operation. In the $T_2$ immediately following the address emission the processor emits the data to be written into the addressed location. This data remains valid until the middle of $T_4$. During $T_2$, $T_3$, and $T_W$ the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of $T_2$ as opposed to the read which is delayed somewhat into $T_2$ to provide time for the bus to float.

The $\overline{BHE}$ and $A_0$ signals are used to select the proper byte(s) of the memory/IO word to be read or written according to the following table:

| $\overline{BHE}$ | A0 | Characteristics |
|------------------|-----|-----------------|
| 0 | 0 | Whole word |
| 0 | 1 | Upper byte from/to odd address |
| 1 | 0 | Lower byte from/to even address |
| 1 | 1 | None |

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the $D_7$–$D_0$ bus lines and odd addressed bytes on $D_{15}$–$D_8$.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal ($\overline{INTA}$) is asserted in place of the read ($\overline{RD}$) signal and the address bus is floated. (See Figure 6.) In the second of two successive INTA cycles, a byte of information is read from bus

lines $D_7 - D_0$ as supplied by the inerrupt system logic (i.e., 8259A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

## BUS TIMING—MEDIUM SIZE SYSTEMS

For medium size systems the MN/$\overline{\text{MX}}$ pin is connected to $V_{SS}$ and the 8288 Bus Controller is added to the system as well as a latch for latching the system address, and a transceiver to allow for bus loading greater than the 8086 is capable of handling. Signals ALE, DEN, and DT/$\overline{\text{R}}$ are generated by the 8288 instead of the processor in this configuration although their timing remains relatively the same. The 8086 status outputs ($\overline{S_2}$, $\overline{S_1}$, and $\overline{S_0}$) provide type-of-cycle information and become 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence data isn't valid at the leading edge of write. The transceiver receives the usual DIR and $\overline{\text{G}}$ inputs from the 8288's DT/$\overline{\text{R}}$ and DEN.

The pointer into the interrupt vector table, which is passed during the second INTA cycle, can derive from an 8259A located on either the local bus or the system bus. If the master 8259A Priority Interrupt Controller is positioned on the local bus, a TTL gate is required to disable the transceiver when reading from the master 8259A during the interrupt acknowledge sequence and software "poll".

## Table 2. Instruction Set Summary

| Mnemonic and Description | Instruction Code | | | |
|---|---|---|---|---|
| **DATA TRANSFER** | | | | |
| **MOV = Move:** | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 |
| Register/Memory to/from Register | 1 0 0 0 1 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 1 0 0 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1 |
| Immediate to Register | 1 0 1 1 w reg | data | data if w = 1 | |
| Memory to Accumulator | 1 0 1 0 0 0 0 w | addr-low | addr-high | |
| Accumulator to Memory | 1 0 1 0 0 0 1 w | addr-low | addr-high | |
| Register/Memory to Segment Register | 1 0 0 0 1 1 1 0 | mod 0 reg r/m | | |
| Segment Register to Register/Memory | 1 0 0 0 1 1 0 0 | mod 0 reg r/m | | |
| **PUSH = Push:** | | | | |
| Register/Memory | 1 1 1 1 1 1 1 1 | mod 1 1 0 r/m | | |
| Register | 0 1 0 1 0 reg | | | |
| Segment Register | 0 0 0 reg 1 1 0 | | | |
| **POP = Pop:** | | | | |
| Register/Memory | 1 0 0 0 1 1 1 1 | mod 0 0 0 r/m | | |
| Register | 0 1 0 1 1 reg | | | |
| Segment Register | 0 0 0 reg 1 1 1 | | | |
| **XCHG = Exchange:** | | | | |
| Register/Memory with Register | 1 0 0 0 0 1 1 w | mod reg r/m | | |
| Register with Accumulator | 1 0 0 1 0 reg | | | |
| **IN = Input from:** | | | | |
| Fixed Port | 1 1 1 0 0 1 0 w | port | | |
| Variable Port | 1 1 1 0 1 1 0 w | | | |
| **OUT = Output to:** | | | | |
| Fixed Port | 1 1 1 0 0 1 1 w | port | | |
| Variable Port | 1 1 1 0 1 1 1 w | | | |
| **XLAT** = Translate Byte to AL | 1 1 0 1 0 1 1 1 | | | |
| **LEA** = Load EA to Register | 1 0 0 0 1 1 0 1 | mod reg r/m | | |
| **LDS** = Load Pointer to DS | 1 1 0 0 0 1 0 1 | mod reg r/m | | |
| **LES** = Load Pointer to ES | 1 1 0 0 0 1 0 0 | mod reg r/m | | |
| **LAHF** = Load AH with Flags | 1 0 0 1 1 1 1 1 | | | |
| **SAHF** = Store AH into Flags | 1 0 0 1 1 1 1 0 | | | |
| **PUSHF** = Push Flags | 1 0 0 1 1 1 0 0 | | | |
| **POPF** = Pop Flags | 1 0 0 1 1 1 0 1 | | | |

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## Table 2. Instruction Set Summary (Continued)

| Mnemonic and Description | Instruction Code | | | |
|---|---|---|---|---|
| **ARITHMETIC** | 76543210 | 76543210 | 76543210 | 76543210 |
| **ADD = Add:** | | | | |
| Reg./Memory with Register to Either | 000000dw | mod reg r/m | | |
| Immediate to Register/Memory | 100000sw | mod 0 0 0 r/m | data | data if s: w = 01 |
| Immediate to Accumulator | 0000010w | data | data if w = 1 | |
| **ADC = Add with Carry:** | | | | |
| Reg./Memory with Register to Either | 000100dw | mod reg r/m | | |
| Immediate to Register/Memory | 100000sw | mod 0 1 0 r/m | data | data if s: w = 01 |
| Immediate to Accumulator | 0001010w | data | data if w = 1 | |
| **INC = Increment:** | | | | |
| Register/Memory | 1111111w | mod 0 0 0 r/m | | |
| Register | 0 1 0 0 0 reg | | | |
| **AAA** = ASCII Adjust for Add | 0 0 1 1 0 1 1 1 | | | |
| **BAA** = Decimal Adjust for Add | 0 0 1 0 0 1 1 1 | | | |
| **SUB = Subtract:** | | | | |
| Reg./Memory and Register to Either | 001010dw | mod reg r/m | | |
| Immediate from Register/Memory | 100000sw | mod 1 0 1 r/m | data | data if s w = 01 |
| Immediate from Accumulator | 0010110w | data | data if w = 1 | |
| **SSB = Subtract with Borrow** | | | | |
| Reg./Memory and Register to Either | 000110dw | mod reg r/m | | |
| Immediate from Register/Memory | 100000sw | mod 0 1 1 r/m | data | data if s w = 01 |
| Immediate from Accumulator | 000111w | data | data if w = 1 | |
| **DEC = Decrement:** | | | | |
| Register/memory | 1111111w | mod 0 0 1 r/m | | |
| Register | 0 1 0 0 1 reg | | | |
| **NEG** = Change sign | 1111011w | mod 0 1 1 r/m | | |
| **CMP = Compare:** | | | | |
| Register/Memory and Register | 001110dw | mod reg r/m | | |
| Immediate with Register/Memory | 100000sw | mod 1 1 1 r/m | data | data if s w = 01 |
| Immediate with Accumulator | 0011110w | data | data if w = 1 | |
| **AAS** = ASCII Adjust for Subtract | 0 0 1 1 1 1 1 1 | | | |
| **DAS** = Decimal Adjust for Subtract | 0 0 1 0 1 1 1 1 | | | |
| **MUL** = Multiply (Unsigned) | 1111011w | mod 1 0 0 r/m | | |
| **IMUL** = Integer Multiply (Signed) | 1111011w | mod 1 0 1 r/m | | |
| **AAM** = ASCII Adjust for Multiply | 1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0 | | |
| **DIV** = Divide (Unsigned) | 1111011w | mod 1 1 0 r/m | | |
| **IDIV** = Integer Divide (Signed) | 1111011w | mod 1 1 1 r/m | | |
| **AAD** = ASCII Adjust for Divide | 1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0 | | |
| **CBW** = Convert Byte to Word | 1 0 0 1 1 0 0 0 | | | |
| **CWD** = Convert Word to Double Word | 1 0 0 1 1 0 0 1 | | | |

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## Table 2. Instruction Set Summary (Continued)

| Mnemonic and Description | Instruction Code | | | |
|---|---|---|---|---|
| **LOGIC** | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 | 7 6 5 4 3 2 1 0 |
| **NOT** = Invert | 1 1 1 1 0 1 1 w | mod 0 1 0 r/m | | |
| **SHL/SAL** = Shift Logical/Arithmetic Left | 1 1 0 1 0 0 v w | mod 1 0 0 r/m | | |
| **SHR** = Shift Logical Right | 1 1 0 1 0 0 v w | mod 1 0 1 r/m | | |
| **SAR** = Shift Arithmetic Right | 1 1 0 1 0 0 v w | mod 1 1 1 r/m | | |
| **ROL** = Rotate Left | 1 1 0 1 0 0 v w | mod 0 0 0 r/m | | |
| **ROR** = Rotate Right | 1 1 0 1 0 0 v w | mod 0 0 1 r/m | | |
| **RCL** = Rotate Through Carry Flag Left | 1 1 0 1 0 0 v w | mod 0 1 0 r/m | | |
| **RCR** = Rotate Through Carry Right | 1 1 0 1 0 0 v w | mod 0 1 1 r/m | | |
| **AND = And:** | | | | |
| Reg./Memory and Register to Either | 0 0 1 0 0 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w = 1 |
| Immediate to Accumulator | 0 0 1 0 0 1 0 w | data | data if w = 1 | |
| **TEST = And Function to Flags, No Result:** | | | | |
| Register/Memory and Register | 1 0 0 0 0 1 0 w | mod reg r/m | | |
| Immediate Data and Register/Memory | 1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1 |
| Immediate Data and Accumulator | 1 0 1 0 1 0 0 w | data | data if w = 1 | |
| **OR = Or:** | | | | |
| Reg./Memory and Register to Either | 0 0 0 0 1 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w = 1 |
| Immediate to Accumulator | 0 0 0 0 1 1 0 w | data | data if w = 1 | |
| **XOR = Exclusive or:** | | | | |
| Reg./Memory and Register to Either | 0 0 1 1 0 0 d w | mod reg r/m | | |
| Immediate to Register/Memory | 1 0 0 0 0 0 0 w | mod 1 1 0 r/m | data | data if w = 1 |
| Immediate to Accumulator | 0 0 1 1 0 1 0 w | data | data if w = 1 | |
| **STRING MANIPULATION** | | | | |
| **REP** = Repeat | 1 1 1 1 0 0 1 z | | | |
| **MOVS** = Move Byte/Word | 1 0 1 0 0 1 0 w | | | |
| **CMPS** = Compare Byte/Word | 1 0 1 0 0 1 1 w | | | |
| **SCAS** = Scan Byte/Word | 1 0 1 0 1 1 1 w | | | |
| **LODS** = Load Byte/Wd to AL/AX | 1 0 1 0 1 1 0 w | | | |
| **STOS** = Stor Byte/Wd from AL/A | 1 0 1 0 1 0 1 w | | | |
| **CONTROL TRANSFER** | | | | |
| **CALL = Call:** | | | | |
| Direct within Segment | 1 1 1 0 1 0 0 0 | disp-low | disp-high | |
| Indirect within Segment | 1 1 1 1 1 1 1 1 | mod 0 1 0 r/m | | |
| Direct intersegment | 1 0 0 1 1 0 1 0 | offset-low | offset-high | |
| | | seg-low | seg-high | |
| Indirect intersegment | 1 1 1 1 1 1 1 1 | mod 0 1 1 r/m | | |

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## Table 2. Instruction Set Summary (Continued)

| Mnemonic and Description | Instruction Code | | |
|---|---|---|---|
| **JMP = Unconditional Jump:** | 76543210 | 76543210 | 76543210 |
| Direct within Segment | 11101001 | disp-low | disp-high |
| Direct within Segment-Short | 11101011 | disp | |
| Indirect within Segment | 11111111 | mod 1 0 0 r/m | |
| Direct Intersegment | 11101010 | offset-low | offset-high |
| | | seg-low | seg-high |
| Indirect Intersegment | 11111111 | mod 1 0 1 r/m | |
| **RET = Return from CALL:** | | | |
| Within Segment | 11000011 | | |
| Within Seg Adding Immed to SP | 11000010 | data-low | data-high |
| Intersegment | 11001011 | | |
| Intersegment Adding Immediate to SP | 11001010 | data-low | data-high |
| **JE/JZ** = Jump on Equal/Zero | 01110100 | disp | |
| **JL/JNGE** = Jump on Less/Not Greater or Equal | 01111100 | disp | |
| **JLE/JNG** = Jump on Less or Equal/ Not Greater | 01111110 | disp | |
| **JB/JNAE** = Jump on Below/Not Above or Equal | 01110010 | disp | |
| **JBE/JNA** = Jump on Below or Equal/ Not Above | 01110110 | disp | |
| **JP/JPE** = Jump on Parity/Parity Even | 01111010 | disp | |
| **JO** = Jump on Overflow | 01110000 | disp | |
| **JS** = Jump on Sign | 01111000 | disp | |
| **JNE/JNZ** = Jump on Not Equal/Not Zero | 01110101 | disp | |
| **JNL/JGE** = Jump on Not Less/Greater or Equal | 01111101 | disp | |
| **JNLE/JG** = Jump on Not Less or Equal/ Greater | 01111111 | disp | |
| **JNB/JAE** = Jump on Not Below/Above or Equal | 01110011 | disp | |
| **JNBE/JA** = Jump on Not Below or Equal/Above | 01110111 | disp | |
| **JNP/JPO** = Jump on Not Par/Par Odd | 01111011 | disp | |
| **JNO** = Jump on Not Overflow | 01110001 | disp | |
| **JNS** = Jump on Not Sign | 01111001 | disp | |
| **LOOP** = Loop CX Times | 11100010 | disp | |
| **LOOPZ/LOOPE** = Loop While Zero/Equal | 11100001 | disp | |
| **LOOPNZ/LOOPNE** = Loop While Not Zero/Equal | 11100000 | disp | |
| **JCXZ** = Jump on CX Zero | 11100011 | disp | |
| **INT = Interrupt** | | | |
| Type Specified | 11001101 | type | |
| Type 3 | 11001100 | | |
| **INTO** = Interrupt on Overflow | 11001110 | | |
| **IRET** = Interrupt Return | 11001111 | | |

## Table 2. Instruction Set Summary (Continued)

| Mnemonic and Description | Instruction Code | |
|---|---|---|
| | 76543210 | 76543210 |
| **PROCESSOR CONTROL** | | |
| CLC = Clear Carry | 11111000 | |
| CMC = Complement Carry | 11110101 | |
| STC = Set Carry | 11111001 | |
| CLD = Clear Direction | 11111100 | |
| STD = Set Direction | 11111101 | |
| CLI = Clear Interrupt | 11111010 | |
| STI = Set Interrupt | 11111011 | |
| HLT = Halt | 11110100 | |
| WAIT = Wait | 10011011 | |
| ESC = Escape (to External Device) | 11011xxx | mod x x x r/m |
| LOCK = Bus Lock Prefix | 11110000 | |

**NOTES:**
AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16 bits, disp-high is absent
if mod = 10 then DISP = disp-high; disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)
*except if mod = 00 and r/m = 110 then EA = disp-high; disp-low.

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if s w = 01 then 16 bits of immediate data form the operand
if s w = 11 then an immediate data byte is sign extended to form the 16-bit operand
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG

**SEGMENT OVERRIDE PREFIX**

| 0 0 1 reg 1 1 0 |
|---|

REG is assigned according to the following table:

| 16-Bit (w = 1) | | 8-Bit (w = 0) | | Segment | |
|---|---|---|---|---|---|
| 000 | AX | 000 | AL | 00 | ES |
| 001 | CX | 001 | CL | 01 | CS |
| 010 | DX | 010 | DL | 10 | SS |
| 011 | BX | 011 | BL | 11 | DS |
| 100 | SP | 100 | AH | | |
| 101 | BP | 101 | CH | | |
| 110 | SI | 110 | DH | | |
| 111 | DI | 111 | BH | | |

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:
FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

# 8088
# 8-BIT HMOS MICROPROCESSOR
## 8088/8088-2

- **8-Bit Data Bus Interface**
- **16-Bit Internal Architecture**
- **Direct Addressing Capability to 1 Mbyte of Memory**
- **Direct Software Compatibility with 8086 CPU**
- **14-Word by 16-Bit Register Set with Symmetrical Operations**
- **24 Operand Addressing Modes**

- **Byte, Word, and Block Operations**
- **8-Bit and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal, including Multiply and Divide**
- **Two Clock Rates:**
  **— 5 MHz for 8088**
  **— 8 MHz for 8088-2**
- **Available in EXPRESS**
  **— Standard Temperature Range**
  **— Extended Temperature Range**

The Intel® 8088 is a high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CERDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It is directly compatible with 8086 software and 8080/8085 hardware and peripherals.
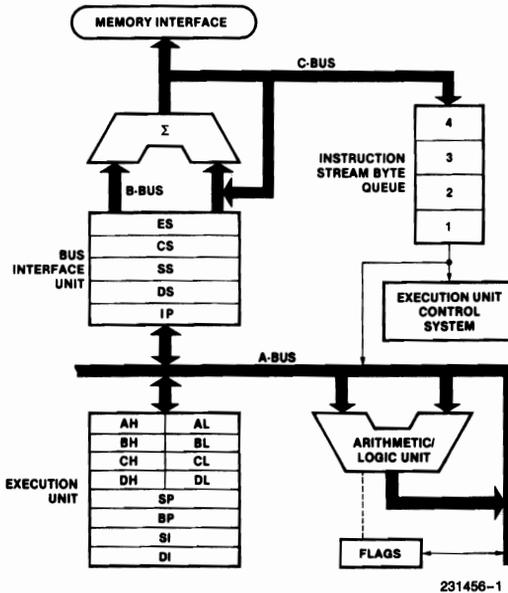


Figure 1. 8088 CPU Functional Block Diagram
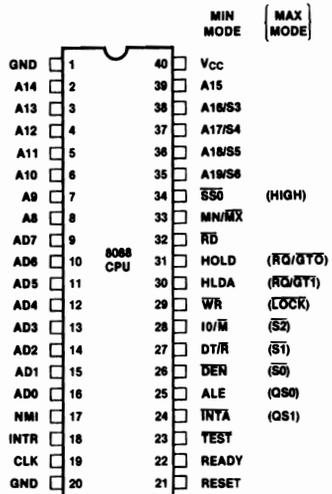


Figure 2. 8088 Pin Configuration

**Table 1. Pin Description**

*The following pin function descriptions are for 8088 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 8088 (without regard to additional bus buffers).*

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| AD7–AD0 | 9–16 | I/O | **ADDRESS DATA BUS:** These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, Tw, T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge". |
| A15–A8 | 2–8, 39 | O | **ADDRESS BUS:** These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge". |
| A19/S6, A18/S5, A17/S4, A16/S3 | 35–38 | O | **ADDRESS/STATUS:** During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines float to 3-state OFF during local bus "hold acknowledge". |

| S4 | S3 | Characteristics |
|---|---|---|
| 0 (LOW) | 0 | Alternate Data |
| 0 | 1 | Stack |
| 1 (HIGH) | 0 | Code or None |
| 1 | 1 | Data |
| S6 is 0 (LOW) | | |

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| $\overline{RD}$ | 32 | O | **READ:** Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or S2. This signal is used to read devices which reside on the 8088 local bus. $\overline{RD}$ is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 8088 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge". |
| READY | 22 | I | **READY:** is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 8284 clock generator to form READY. This signal is active HIGH. The 8088 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met. |
| INTR | 18 | I | **INTERRUPT REQUEST:** is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH. |
| TEST | 23 | I | **TEST:** input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK. |

**Table 1. Pin Description** (Continued)

| Symbol | Pin No. | Type | Name and Function |
|--------|---------|------|-------------------|
| NMI | 17 | I | **NON-MASKABLE INTERRUPT:** is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized. |
| RESET | 21 | I | **RESET:** causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized. |
| CLK | 19 | I | **CLOCK:** provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing. |
| V$_{CC}$ | 40 | | V$_{CC}$: is the +5V ±10% power supply pin. |
| GND | 1, 20 | | **GND:** are the ground pins. |
| MN/$\overline{MX}$ | 33 | I | **MINIMUM/MAXIMUM:** indicates what mode the processor is to operate in. The two modes are discussed in the following sections. |

*The following pin function descriptions are for the 8088 minimum mode (i.e., MN/$\overline{MX}$ = V$_{CC}$). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.*

| Symbol | Pin No. | Type | Name and Function |
|--------|---------|------|-------------------|
| IO/$\overline{M}$ | 28 | O | **STATUS LINE:** is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ floats to 3-state OFF in local bus "hold acknowledge". |
| $\overline{WR}$ | 29 | O | **WRITE:** strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. WR is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge". |
| $\overline{INTA}$ | 24 | O | **INTA:** is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle. |
| ALE | 25 | O | **ADDRESS LATCH ENABLE:** is provided by the processor to latch the address into an address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated. |
| DT/$\overline{R}$ | 27 | O | **DATA TRANSMIT/RECEIVE:** is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal floats to 3-state OFF in local "hold acknowledge". |
| $\overline{DEN}$ | 26 | O | **DATA ENABLE:** is provided as an output enable for the data bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to 3-state OFF during local bus "hold acknowledge". |

### Table 1. Pin Description (Continued)

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| HOLD, HLDA | 31, 30 | I, O | **HOLD:** indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines.<br><br>Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time. |
| $\overline{SSO}$ | 34 | O | **STATUS LINE:** is logically equivalent to $\overline{S0}$ in the maximum mode. The combination of $\overline{SSO}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status. |

| IO/$\overline{M}$ | DT/$\overline{R}$ | $\overline{SSO}$ | Characteristics |
|---|---|---|---|
| 1(HIGH) | 0 | 0 | Interrupt Acknowledge |
| 1 | 0 | 1 | Read I/O Port |
| 1 | 1 | 0 | Write I/O Port |
| 1 | 1 | 1 | Halt |
| 0(LOW) | 0 | 0 | Code Access |
| 0 | 0 | 1 | Read Memory |
| 0 | 1 | 0 | Write Memory |
| 0 | 1 | 1 | Passive |

*The following pin function descriptions are for the 8088/8288 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.*

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ | 26–28 | O | **STATUS:** is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 8288 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 and Tw is used to indicate the end of a bus cycle.<br><br>These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they float to 3-state OFF. |

| $\overline{S2}$ | $\overline{S1}$ | $\overline{S0}$ | Characteristics |
|---|---|---|---|
| 0(LOW) | 0 | 0 | Interrupt Acknowledge |
| 0 | 0 | 1 | Read I/O Port |
| 0 | 1 | 0 | Write I/O Port |
| 0 | 1 | 1 | Halt |
| 1(HIGH) | 0 | 0 | Code Access |
| 1 | 0 | 1 | Read Memory |
| 1 | 1 | 0 | Write Memory |
| 1 | 1 | 1 | Passive |

**Table 1. Pin Description** (Continued)

| Symbol | Pin No. | Type | Name and Function |
|--------|---------|------|-------------------|
| R̄Q̄/ḠT̄0, R̄Q̄/ḠT̄1 | 30, 31 | I/O | **REQUEST/GRANT:** pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with R̄Q̄/ḠT̄0 having higher priority than R̄Q̄/ḠT̄1. R̄Q̄/ḠT̄ has an internal pull-up resistor, so may be left unconnected. The request/grant sequence is as follows (See Figure 8): 1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the 8088 (pulse 1). 2. During a T4 or TI clock cycle, a pulse one clock wide from the 8088 to the requesting master (pulse 2), indicates that the 8088 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply as for when the bus is released. 3. A pulse one CLK wide from the requesting master indicates to the 8088 (pulse 3) that the "hold" request is about to end and that the 8088 can reclaim the local bus at the next CLK. The CPU then enters T4. Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met: 1. Request occurs on or before T2. 2. Current cycle is not the low bit of a word. 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next clock. 2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied. |
| L̄O̅C̅K̅ | 29 | O | **L̄O̅C̅K̅:** indicates that other system bus masters are not to gain control of the system bus while L̄O̅C̅K̅ is active (LOW). The L̄O̅C̅K̅ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state off in "hold acknowledge". |
| QS1, QS0 | 24, 25 | O | **QUEUE STATUS:** provide status to allow external tracking of the internal 8088 instruction queue. The queue status is valid during the CLK cycle after which the queue operation is performed. |

| QS1 | QS0 | Characteristics |
|-----|-----|-----------------|
| 0(LOW) | 0 | No Operation |
| 0 | 1 | First Byte of Opcode from Queue |
| 1(HIGH) | 0 | Empty the Queue |
| 1 | 1 | Subsequent Byte from Queue |

| — | 34 | O | Pin 34 is always high in the maximum mode. |

**Figure 3. Memory Organization**

## FUNCTIONAL DESCRIPTION

### Memory Organization

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries (See Figure 3).

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the ad-

dressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU will automatically execute two fetch or write cycles for 16-bit operands.

| Memory Reference Used | Segment Register Used | Segment Selection Rule |
|---|---|---|
| Instructions | CODE (CS) | Automatic with all instruction prefetch. |
| Stack | STACK (SS) | All stack pushes and pops. Memory references relative to BP base register except data references. |
| Local Data | DATA (DS) | Data references when: relative to stack, destination of string operation, or explicitly overridden. |
| External (Global) Data | EXTRA (ES) | Destination of string operations: Explicitly selected using a segment override. |

Certain locations in memory are reserved for specific CPU operations (See Figure 4). Locations from addresses FFFF0H through FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Four-byte pointers consisting of a 16-bit segment address and a 16-bit offset address direct program flow to one of the 256 possible interrupt service routines. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

## Minimum and Maximum Modes

The requirements for supporting minimum and maximum 8088 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8088 is equipped with a strap pin (MN/$\overline{\text{MX}}$) which defines the system con-



**Figure 4. Reserved Memory Locations**

figuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{\text{MX}}$ pin is strapped to GND, the 8088 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{\text{MX}}$ pin is strapped to $V_{CC}$, the 8088 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 8088 can be used with either a multiplexed or demultiplexed bus. The multiplexed bus configuration is compatible with the MCS-85™ multiplexed bus peripherals. This configuration (See Figure 5) provides the user with a minimum chip count system. This architecture provides the 8088 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). A third latch can be used for buffering if the address bus loading requires it. A transceiver can also be used if data bus buffering is required (See Figure 6). The 8088 provides $\overline{\text{DEN}}$ and DT/$\overline{\text{R}}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 8288 bus controller (See Figure 7). The 8288 decodes status lines $\overline{\text{S0}}$, $\overline{\text{S1}}$, and $\overline{\text{S2}}$, and provides the system with all bus control signals. Moving the bus control to the 8288 provides better source and sink current capability to the control lines, and frees the 8088 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 8088 in maximum mode. These features allow co-processors in local bus and remote bus configurations.

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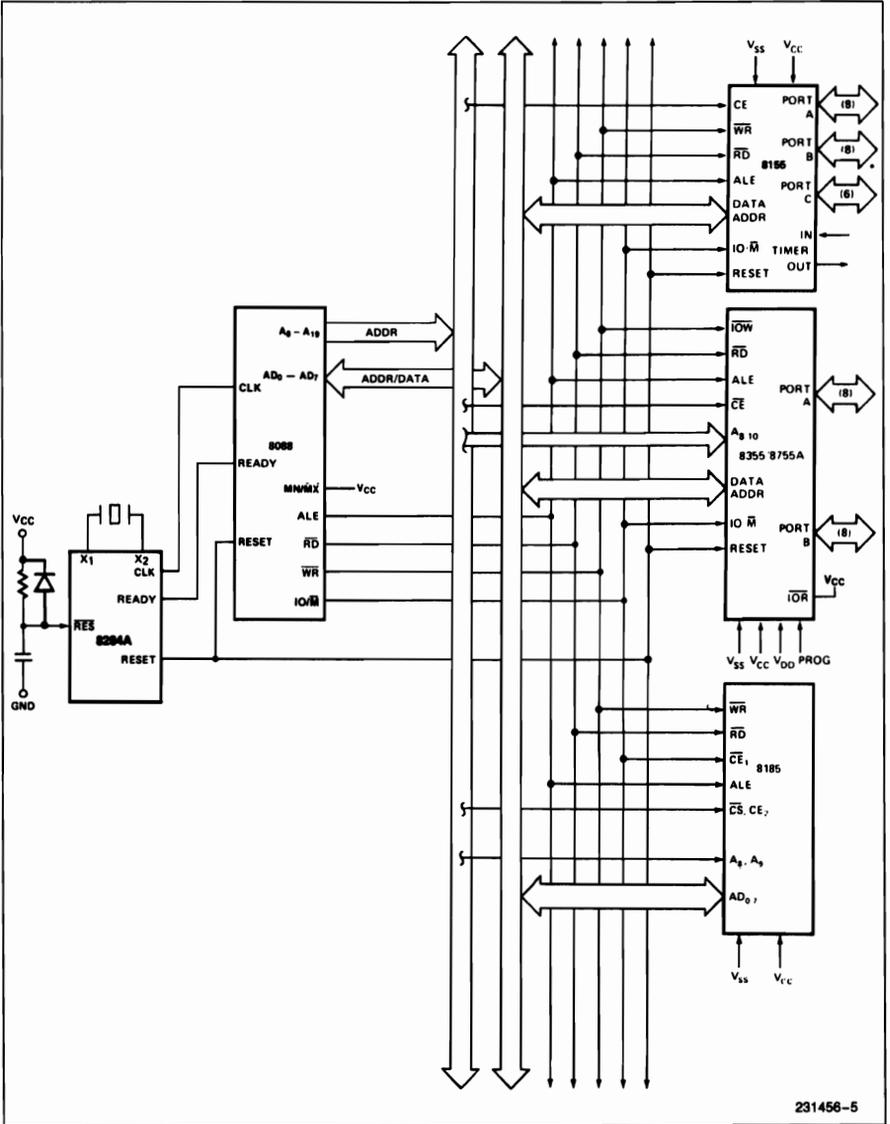
Figure 5. Multiplexed Bus Configuration

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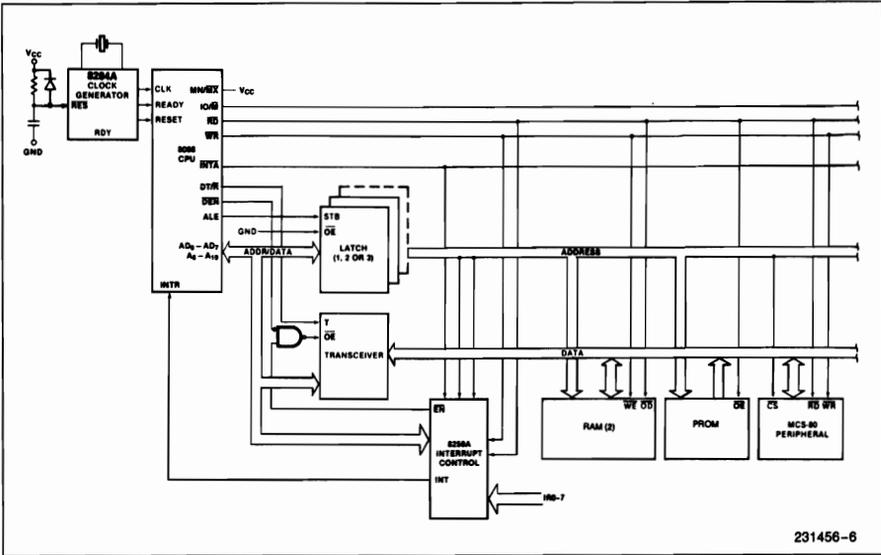
Figure 6. Demultiplexed Bus Configuration
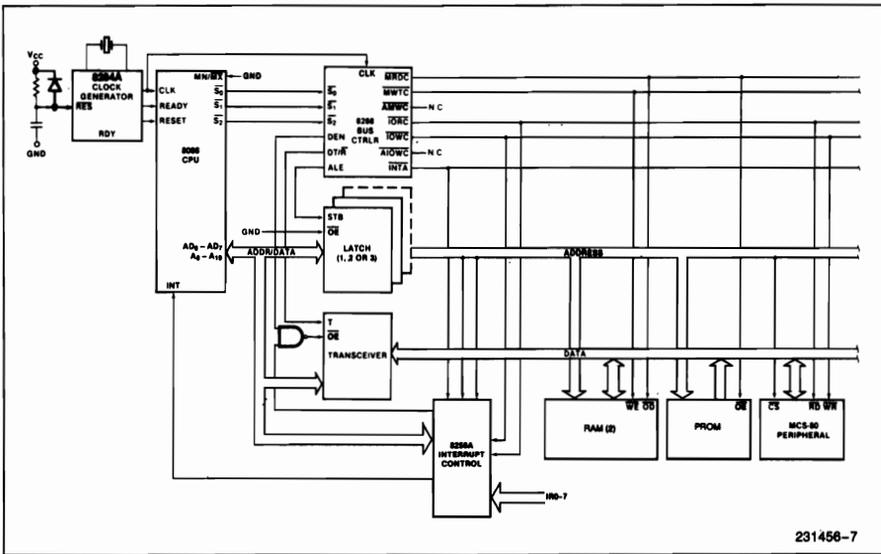


Figure 7. Fully Buffered System Using Bus Controller

## Bus Operation

The 8088 address/data bus is broken into three parts—the lower eight address/data bits (AD0–AD7), the middle eight address bits (A8–A15), and the upper four address bits (A16–A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain val-id throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3, and T4 (See Figure 8). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for chang-
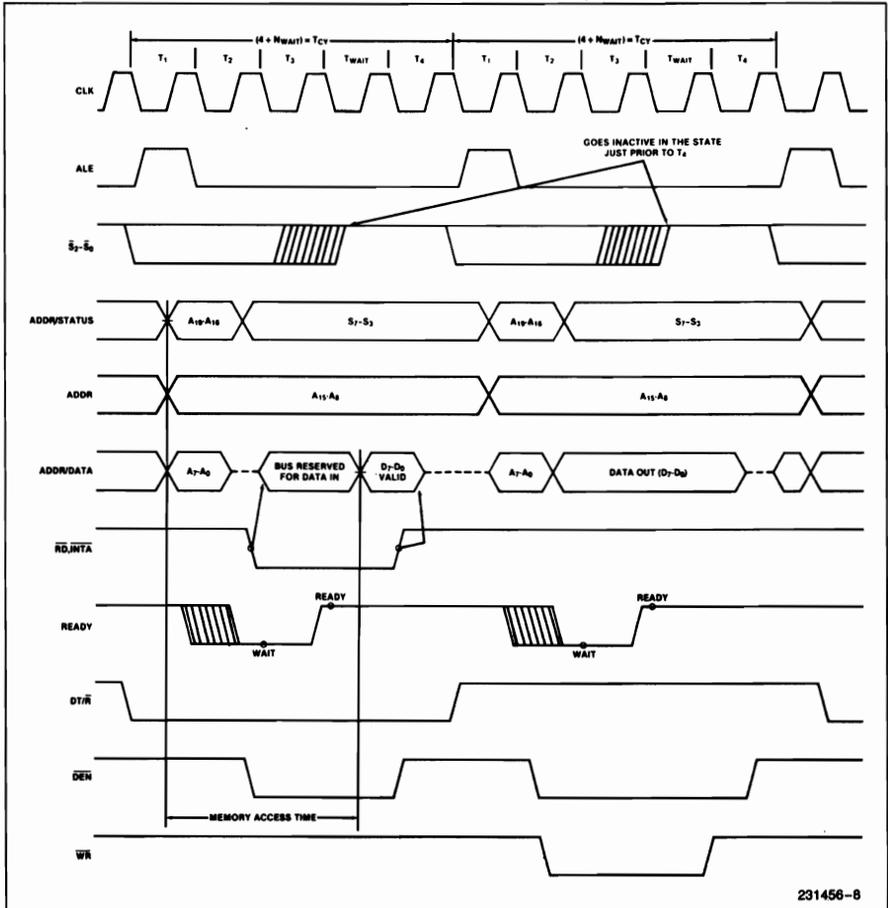


**Figure 8. Basic System Timing**

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ing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "wait" states (Tw) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between 8088 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the 8288 bus controller, depending on the MN/$\overline{\text{MX}}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to the following table:

| $\overline{S2}$ | $\overline{S1}$ | $\overline{S0}$ | Characteristics |
|---|---|---|---|
| 0(LOW) | 0 | 0 | Interrupt Acknowledge |
| 0 | 0 | 1 | Read I/O |
| 0 | 1 | 0 | Write I/O |
| 0 | 1 | 1 | Halt |
| 1(HIGH) | 0 | 0 | Instruction Fetch |
| 1 | 0 | 1 | Read Data from Memory |
| 1 | 1 | 0 | Write Data to Memory |
| 1 | 1 | 1 | Passive (No Bus Cycle) |

Status bits S3 through S6 are multiplexed with high order address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

| $S_4$ | $S_3$ | Characteristics |
|---|---|---|
| 0(LOW) | 0 | Alternate Data (Extra Segment) |
| 0 | 1 | Stack |
| 1(HIGH) | 0 | Code or None |
| 1 | 1 | Data |

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

## I/O Addressing

In the 8088, I/O operations can address up to a maximum of 64K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15–A0. The address lines A19–A16 are zero in I/O operations. The variable I/O instructions,

which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the 8085 or upgrading an 8085 design should note that the 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The 8088 uses a full 16-bit address on its lower 16 address lines.

## EXTERNAL INTERFACE

### Processor Reset and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 8088 RESET is required to be HIGH for greater than four clock cycles. The 8088 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the 8088 operates normally, beginning with the instruction in absolute locations FFFF0H (See Figure 4). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50 μs after power up, to allow complete initialization of the 8088.

NMI asserted prior to the 2nd clock after the end of RESET will not be honored. If NMI is asserted after that point and during the internal reset sequence, the processor may execute one instruction before responding to the interrupt. A hold request active immediately after RESET will be honored before the first instruction fetch.

All 3-state outputs float to 3-state OFF during RESET. Status is active in the idle state for the first clock after RESET becomes active and then floats to 3-state OFF. ALE and HLDA are driven low.

### Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description in the iAPX 88 book or the iAPX 86,88 User's Manual. Hardware interrupts can be classified as nonmaskable or maskable.

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Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (See Figure 4), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type." An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

## Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. Any higher going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2 bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

## Maskable Interrupt (INTR)

The 8088 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored, the enable bit will be zero unless specifically set by an instruction.

During the response sequence (See Figure 9), the processor executes two successive (back to back) interrupt acknowledge cycles. The 8088 emits the LOCK signal (maximum mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is fetched from the external interrupt system (e.g., 8259A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

## HALT

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on IO/$\overline{M}$, DT/$\overline{R}$, and $\overline{SSO}$. In maximum mode, the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, and $\overline{S0}$, and the 8288 bus controller issues one ALE. The 8088 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the 8088 out of the HALT state.

## Read/Modify/Write (Semaphore) Operations via LOCK

The LOCK status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (LOW) in the clock cycle following decoding of the LOCK prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the LOCK prefix. While $\overline{LOCK}$ is active, a request on a $\overline{RQ}$/$\overline{GT}$ pin will be recorded, and then honored at the end of the LOCK.

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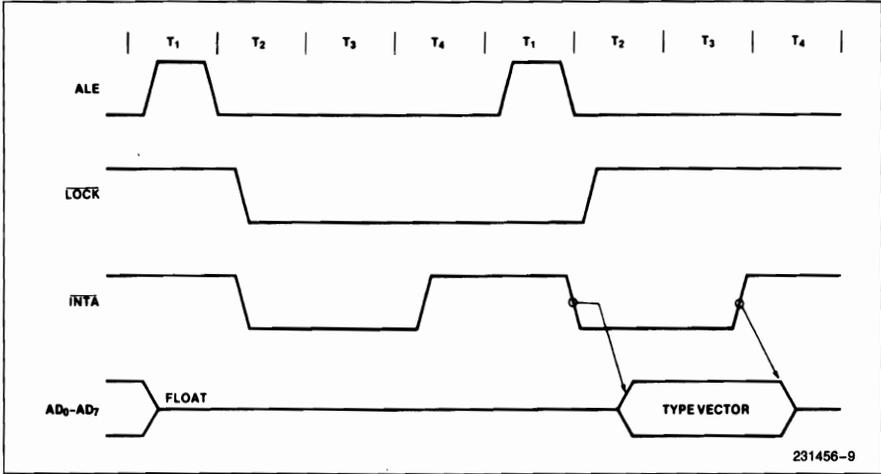
**Figure 9. Interrupt Acknowledge Sequence**

## External Synchronization via TEST

As an alternative to interrupts, the 8088 provides a single software-testable input pin (TEST). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the TEST input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 8088 3-states all output drivers. If interrupts are enabled, the 8088 will recognize interrupts and process them. The WAIT instruction is then refetched, and reexecuted.

## Basic System Timing

In minimum mode, the MN/MX pin is strapped to $V_{CC}$ and the processor emits bus control signals compatible with the 8085 bus structure. In maximum mode, the MN/MX pin is strapped to GND and the processor emits coded status information which the 8288 bus controller uses to generate MULTIBUS compatible bus control signals.

## System Timing—Minimum System

(See Figure 8)

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal. The trailing (low

going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0–AD7) at this time, into the 8282/8283 latch. Address lines A8 through A15 do not need to be latched because they remain valid throughout the bus cycle. From T1 to T4 the IO/M signal indicates a memory or I/O operation. At T2 the address is removed from the address/data bus and the bus goes to a high impedance state. The read control signal is also asserted at T2. The read (RD) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver is required to buffer the 8088 local bus, signals DT/R and DEN are provided by the 8088.

A write cycle also begins with the assertion of ALE and the emission of the address. The IO/M signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3, and Tw, the processor asserts the write control signal. The write (WR) signal becomes active at the beginning of T2, as opposed to the read, which is delayed somewhat into T2 to provide time for the bus to float.

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The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge ($\overline{INTA}$) signal is asserted in place of the read ($\overline{RD}$) signal and the address bus is floated. (See Figure 9) In the second of two successive $\overline{INTA}$ cycles, a byte of information is read from the data bus, as supplied by the interrupt system logic (i.e. 8259A priority interrupt controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into the interrupt vector lookup table, as described earlier.

## Bus Timing—Medium Complexity Systems

(See Figure 10)

For medium complexity systems, the MN/$\overline{MX}$ pin is connected to GND and the 8288 bus controller is added to the system, as well as a latch for latching the system address, and a transceiver to allow for bus loading greater than the 8088 is capable of handling. Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 8288 instead of the processor in this configuration, although their timing remains relatively the same. The 8088 status outputs ($\overline{S2}$, $\overline{S1}$, and $\overline{S0}$) provide type of cycle information and become 8288 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 8288 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 8288 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The transceiver receives the usual T and $\overline{OE}$ inputs from the 8288's DT/$\overline{R}$ and $\overline{DEN}$ outputs.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can derive from an 8259A located on either local bus or the system bus, If the master 8289A priority interrupt controller is positioned on the local bus, a TTL gate is required to disable the transceiver when reading from the master 8259A during the interrupt acknowledge sequence and software "poll".

## The 8088 Compared to the 8086

The 8088 CPU is an 8-bit processor designed around the 8086 internal structure. Most internal functions of the 8088 are identical to the equivalent 8086 functions. The 8088 handles the external bus the same way the 8086 does with the distinction of handling only 8 bits at a time. Sixteen-bit operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. The differences between the 8088 and 8086 are outlined below. The engineer who is unfamiliar with the 8086 is referred to the iAPX 86, 88 User's Manual, Chapters 2 and 4, for function description and instruction set information. Internally, there are three differences between the 8088 and the 8086. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the 8088, whereas the 8086 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.

- To further optimize the queue, the prefetching algorithm was changed. The 8088 BIU will fetch a new instruction to load into the queue each time there is a 1 byte hole (space available) in the queue. The 8086 waits until a 2-byte space is available.

- The internal execution time of the instruction set is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU is also limited by the speed of instruction fetches. This latter problem only occurs when a series of simple operations occur. When the more sophisticated instructions of the 8088 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The 8088 and 8086 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally as well on an 8088 and an 8086.

The hardware interface of the 8088 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes:

- A8–A15—These pins are only address outputs on the 8088. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.

- $\overline{BHE}$ has no meaning on the 8088 and has been eliminated.

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- $\overline{SSO}$ provides the $\overline{SO}$ status information in the minimum mode. This output occurs on pin 34 in minimum mode only. DT/$\overline{R}$, IO/$\overline{M}$, and $\overline{SSO}$ provide the complete bus status in minimum mode.

- IO/$\overline{M}$ has been inverted to be compatible with the MCS-85 bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.
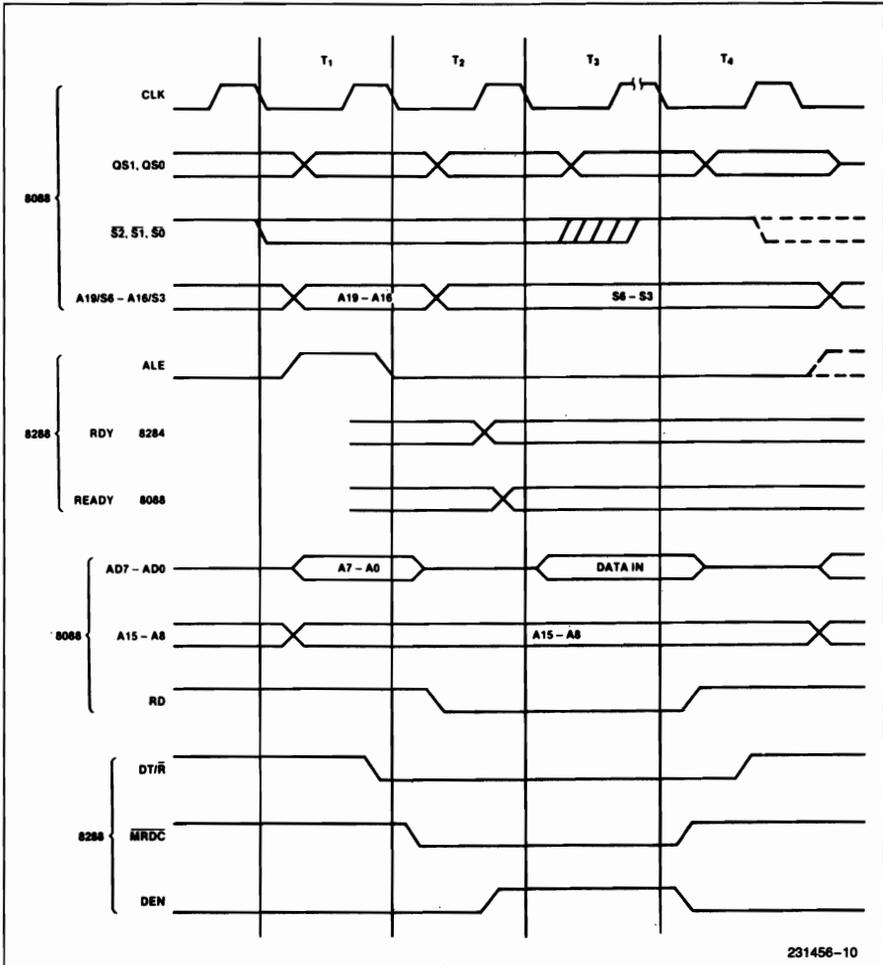


**Figure 10. Medium Complexity System Timing**

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# iAPX 186
# HIGH INTEGRATION 16-BIT MICROPROCESSOR

- Integrated Feature Set
  - —Enhanced 8086-2 CPU
  - —Clock Generator
  - —2 Independent, High-Speed DMA Channels
  - —Programmable Interrupt Controller
  - —3 Programmable 16-bit Timers
  - —Programmable Memory and Peripheral Chip-Select Logic
  - —Programmable Wait State Generator
  - —Local Bus Controller
- Available in 8 MHz (80186) and cost effective 6 MHz (80186-6) versions.
- High-Performance Processor
  - —2 Times the Performance of the Standard iAPX 86
  - —4 MByte/Sec Bus Bandwidth Interface

- Direct Addressing Capability to 1 MByte of Memory

- Completely Object Code Compatible with All Existing iAPX 86, 88 Software
  - —10 New Instruction Types

- Complete System Development Support
  - —Development Software: Assembler, PL/M, Pascal, Fortran, and System Utilities
  - —In-Circuit-Emulator (I²ICE™-186)
  - —iRMX™ 86, 88 Compatible (80130 OSF)

- High Performance Numerical Coprocessing Capability Through 8087 Interface
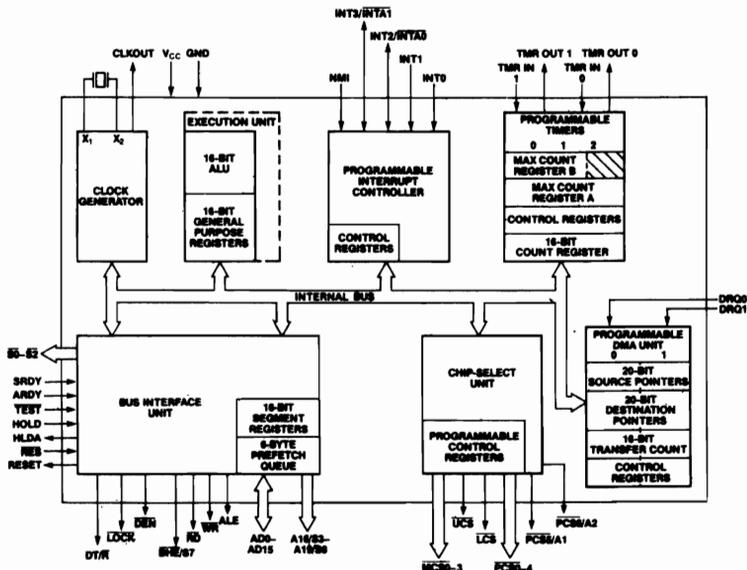


**Figure 1. iAPX 186 Block Diagram**

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The Intel iAPX 186 (80186 part number) is a highly integrated 16-bit microprocessor. The iAPX 186 effectively combines 15–20 of the most common iAPX 86 system components onto one. The 80186 provides two times greater throughput than the standard 5 MHz iAPX 86. The iAPX 186 is upward compatible with iAPX 86 and 88 software and adds 10 new instruction types to the existing set.
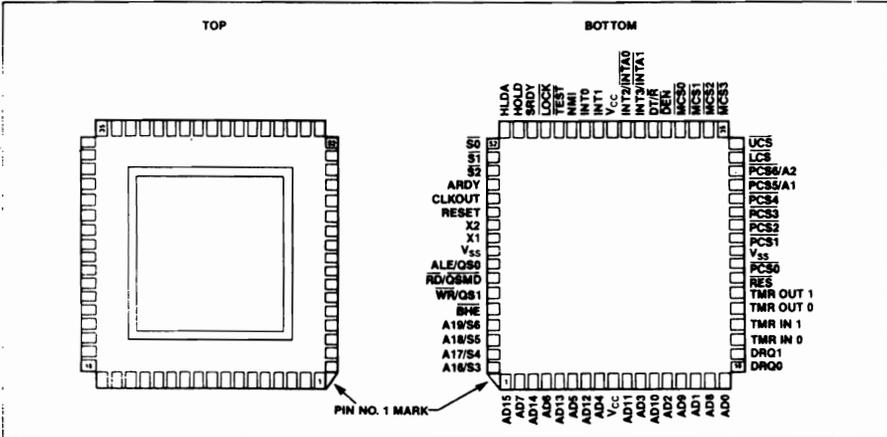


**Figure 2. 80186 Pinout Diagram**

**Table 1. 80186 Pin Description**

| Symbol | Pin No. | Type | Name and Function |
|--------|---------|------|-------------------|
| V$_{CC}$, V$_{CC}$ | 9, 43 | I | System Power: + 5 volt power supply. |
| V$_{SS}$, V$_{SS}$ | 26,60 | I | System Ground. |
| RESET | 57 | O | Reset Output indicates that the 80186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the RES signal. |
| X1, X2 | 59,58 | I | Crystal Inputs, X1 and X2, provide an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT). |
| CLKOUT | 56 | O | Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT has sufficient MOS drive capabilities for the 8087 Numeric Processor Extension. |
| RES | 24 | I | System Reset causes the 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80186 clock. The 80186 begins fetching instructions approximately 7 clock cycles after RES is returned HIGH. RES is required to be LOW for greater than 4 clock cycles and is internally synchronized. For proper initialization, the LOW-to-HIGH transition of RES must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt-trigger to facilitate power-on RES generation via an RC network. When RES occurs, the 80186 will drive the status lines to an inactive level for one clock, and then tri-state them. |

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## Table 1. 80186 Pin Description (Continued)

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| TEST | 47 | I | $\overline{\text{TEST}}$ is examined by the WAIT instruction. If the $\overline{\text{TEST}}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{\text{TEST}}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80186 is waiting for $\overline{\text{TEST}}$, interrupts will be serviced. This input is synchronized internally. |
| TMR IN 0, TMR IN 1 | 20 21 | I I | Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized. |
| TMR OUT 0, TMR OUT 1 | 22 23 | O O | Timer outputs are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected. |
| DRQ0 DRQ1 | 18 19 | I I | DMA Request is driven HIGH by an external device when it desires that a DMA channel (Channel 0 or 1) perform a transfer. These signals are active HIGH, level-triggered, and internally synchronized. |
| NMI | 46 | I | Non-Maskable Interrupt is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a LOW to HIGH initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized. |
| INT0, INT1, INT2/$\overline{\text{INTA0}}$ INT3/$\overline{\text{INTA1}}$ | 45,44 42 41 | I I/O I/O | Maskable Interrupt Requests can be requested by strobing one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowleged. When iRMX mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet). |
| A19/S6, A18/S5, A17/S4, A16/S3 | 65 66 67 68 | O O O O | Address Bus Outputs (16–19) and Bus Cycle Status (3–6) reflect the four most significant address bits during $T_1$. These signals are active HIGH. During $T_2$, $T_3$, $T_W$, and $T_4$, status information is available on these lines as encoded below: <br><br> | | Low | High | <br> | S6 | Processor Cycle | DMA Cycle | <br><br> S3, S4, and S5 are defined as LOW during $T_2$–$T_4$. |
| AD15–AD0 | 10–17 1–8 | I/O | Address/Data Bus (0–15) signals constitute the time mutiplexed memory or I/O address ($T_1$) and data ($T_2$, $T_3$, $T_W$, and $T_4$) bus. The bus is active HIGH. $A_0$ is analogous to $\overline{\text{BHE}}$ for the lower byte of the data bus, pins $D_7$ through $D_0$. It is LOW during $T_1$ when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations. |
| $\overline{\text{BHE}}$/S7 | 64 | O | During $T_1$ the Bus High Enable signal should be used to determine if data is to be enabled onto the most significant half of the data bus, pins $D_{15}$–$D_8$. $\overline{\text{BHE}}$ is LOW during $T_1$ for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The $S_7$ status information is available during $T_2$, $T_3$, and $T_4$. $S_7$ is logically equivalent to $\overline{\text{BHE}}$. The signal is active LOW, and is tristated OFF during bus HOLD. <br><br> | $\overline{\text{BHE}}$ and A0 Encodings | | | <br> | $\overline{\text{BHE}}$ Value | A0 Value | Function | <br> | 0 | 0 | Word Transfer | <br> | 0 | 1 | Byte Transfer on upper half of data bus (D15–D8) | <br> | 1 | 0 | Byte Transfer on lower half of data bus ($D_7$–$D_0$) | <br> | 1 | 1 | Reserved | |

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**Table 1. 80186 Pin Description (Continued)**

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| ALE/QS0 | 61 | · O | Address Latch Enable/Queue Status 0 is provided by the 80186 to latch the address into the 8282/8283 address latches. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T$_1$ of the associated bus cycle, effectively one-half clock cycle earlier than in the standard 8086. The trailing edge is generated off the CLKOUT rising edge in T$_1$ as in the 8086. Note that ALE is never floated. |
| $\overline{WR}$/QS1 | 63 | O | Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T$_2$, T$_3$, and T$_W$ of any write cycle. It is active LOW, and floats during "HOLD." It is driven HIGH for one clock during Reset, and then floated. When the 80186 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.<br><br>| QS1 | QS0 | Queue Operation |<br>|---|---|---|<br>| 0 | 0 | No queue operation |<br>| 0 | 1 | First opcode byte fetched from the queue |<br>| 1 | 1 | Subsequent byte fetched from the queue |<br>| 1 | 0 | Empty the queue | |
| $\overline{RD}$/QSMD | 62 | O | Read Strobe indicates that the 80186 is performing a memory or I/O read cycle. $\overline{RD}$ is active LOW for T$_2$, T$_3$, and T$_W$ of any read cycle. It is guaranteed not to go LOW in T$_2$ until after the Address Bus is floated. $\overline{RD}$ is active LOW, and floats during "HOLD." $\overline{RD}$ is driven HIGH for one clock during Reset, and then the output driver is floated. A weak internal pull-up mechanism on the $\overline{RD}$ line holds it HIGH when the line is not driven. During RESET the pin is sampled to determine whether the 80186 should provide ALE, $\overline{WR}$ and $\overline{RD}$, or if the Queue-Status should be provided. $\overline{RD}$ should be connected to GND to provide Queue-Status data. |
| ARDY | 55 | I | Asynchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active HIGH. Only the rising edge is internally synchronized by the 80186. This means that the falling edge of ARDY must be synchronized to the 80186 clock. If connected to V$_{CC}$, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied LOW. |
| SRDY | 49 | I | Synchronous Ready must be synchronized externally to the 80186. The use of SRDY provides a relaxed system-timing specification on the Ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active HIGH. If this line is connected to V$_{CC}$, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied LOW. |
| $\overline{LOCK}$ | 48 | · O | $\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of the instruction following the LOCK prefix. No prefetches will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ is active LOW, is driven HIGH for one clock during RESET, and then floated. |

## Table 1. 80186 Pin Description (Continued)

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| S̄0,S̄1,S̄2 | 52–54 | O | Bus cycle status S̄0–S̄2 are encoded to provide bus-transaction information: |

| 80186 Bus Cycle Status Information | | | |
|---|---|---|---|
| S̄2 | S̄1 | S̄0 | Bus Cycle Initiated |
| 0 | 0 | 0 | Interrupt Acknowledge |
| 0 | 0 | 1 | Read I/O |
| 0 | 1 | 0 | Write I/O |
| 0 | 1 | 1 | Halt |
| 1 | 0 | 0 | Instruction Fetch |
| 1 | 0 | 1 | Read Data from Memory |
| 1 | 1 | 0 | Write Data to Memory |
| 1 | 1 | 1 | Passive (no bus cycle) |

The status pins float during "HOLD."

S̄2 may be used as a logical M/IŌ indicator, and S̄1 as a DT/R̄ indicator.

The status lines are driven HIGH for one clock during Reset, and then floated until a bus cycle begins.

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| HOLD (input)<br>HLDA (output) | 50<br>51 | I<br>O | HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80186 clock. The 80186 will issue a HLDA (HIGH) in response to a HOLD request at the end of T4 or T1. Simultaneous with the issuance of HLDA, the 80186 will float the local bus and control lines. After HOLD is detected as being LOW, the 80186 will lower HLDA. When the 80186 needs to run another bus cycle, it will again drive the local bus and control lines. |
| U̅C̅S̅ | 34 | O | Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. This line is not floated during bus HOLD. The address range activating U̅C̅S̅ is software programmable. |
| L̅C̅S̅ | 33 | O | Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. This line is not floated during bus HOLD. The address range activating L̅C̅S̅ is software programmable. |
| M̅C̅S̅0–3 | 38,37,36,35 | O | Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating M̅C̅S̅0–3 are software programmable. |
| P̅C̅S̅0<br>P̅C̅S̅1-4 | 25<br>27,28,29,30 | O<br>O | Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating P̅C̅S̅0–4 are software programmable. |
| P̅C̅S̅5/A1 | 31 | O | Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating P̅C̅S̅5 is software programmable. When programmed to provide latched A1, rather than P̅C̅S̅5, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active HIGH. |
| P̅C̅S̅6/A2 | 32 | O | Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating P̅C̅S̅6 is software programmable. When programmed to provide latched A2, rather than P̅C̅S̅6, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active HIGH. |
| DT/R̄ | 40 | O | Data Transmit/Receive controls the direction of data flow through the external 8286/8287 data bus transceiver. When LOW, data is transferred to the 80186. When HIGH the 80186 places write data on the data bus. |
| D̅E̅N̅ | 39 | O | Data Enable is provided as an 8286/8287 data bus transceiver output enable. D̅E̅N̅ is active LOW during each memory and I/O access. D̅E̅N̅ is HIGH whenever DT/R̄ changes state. |

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# FUNCTIONAL DESCRIPTION

## Introduction

The following Functional Description describes the base architecture of the iAPX 186. This architecture is common to the iAPX 86, 88, and 286 microprocessor families as well. The iAPX 186 is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip while providing twice the performance of the standard iAPX 86. The 80186 is object code compatible with the iAPX 86, 88 microprocessors and adds 10 new instruction types to the existing iAPX 86, 88 instruction set.

## iAPX 186 BASE ARCHITECTURE

The iAPX 86, 88, 186, and 286 family all contain the same basic set of registers, instructions, and addressing modes. The 80186 processor is upward compatible with the 8086, 8088, and 80286 CPUs.

## Register Set

The 80186 base architecture has fourteen registers as shown in Figures 3a and 3b. These registers are grouped into the following categories.

### General Registers

Eight 16-bit general purpose registers may be used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

### Segment Registers

Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

### Base and Index Registers

Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

### Status and Control Registers

Two 16-bit special purpose registers record or alter certain aspects of the 80186 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Figures 3a and 3b).

## Status Word Description

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80186 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.
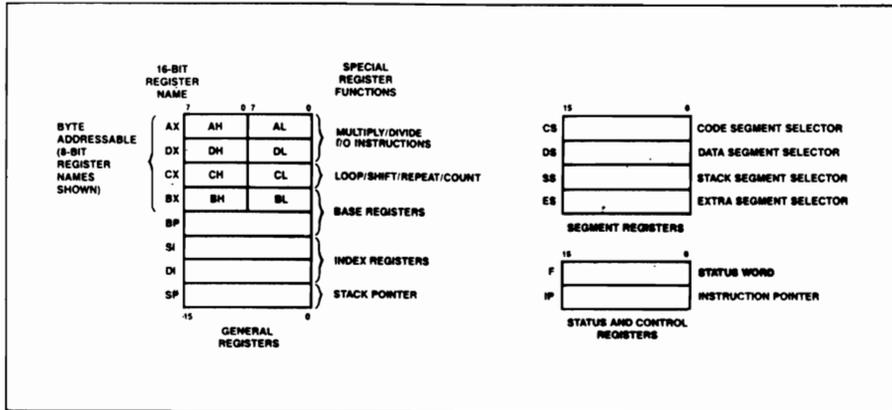


Figure 3a. 80186 General Purpose Register Set

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# iAPX 286/10
## HIGH PERFORMANCE MICROPROCESSOR
## WITH MEMORY MANAGEMENT AND PROTECTION
### (80286-8, 80286-6, 80286-4)

- **High Performance Processor (Up to six times iAPX 86)**
- **Large Address Space:**
  - **—16 Megabytes Physical**
  - **—1 Gigabyte Virtual per Task**
- **Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems**
- **Two iAPX 86 Upward Compatible Operating Modes:**
  - **—iAPX 86 Real Address Mode**
  - **—Protected Virtual Address Mode**
- **Range of clock rates**
  - **—8 MHz for 80286-8**
  - **—6 MHz for 80286-6**
  - **—4 MHz for 80286-4**

- **Optional Processor Extension:**
  - **—iAPX 286/20 High Performance 80-bit Numeric Data Processor**

- **Complete System Development Support:**
  - **—Development Software: Assembler, PL/M, Pascal, FORTRAN, and System Utilities**
  - **—In-Circuit-Emulator (ICE™-286)**

- **High Bandwidth Bus Interface (8 Megabyte/Sec)**

- **Available in EXPRESS:**
  - **—Standard Temperature Range**

The iAPX 286/10 (80286 part number) is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. An 8 MHz iAPX 286/10 provides up to six times greater throughout than the standard 5 MHz iAPX 86/10. The 80286 includes memory management capabilities that map up to $2^{30}$ (one gigabyte) of virtual address space per task into $2^{24}$ bytes (16 megabytes) of physical memory.

The iAPX 286 is upward compatible with iAPX 86 and 88 software. Using iAPX 86 real address mode, the 80286 is object code compatible with existing iAPX 86, 88 software. In protected virtual address mode, the 80286 is source code compatible with iAPX 86, 88 software and may require upgrading to use virtual addresses supported by the 80286's integrated memory management and protection mechanism. Both modes operate at full 80286 performance and execute a superset of the iAPX 86 and 88's instructions.

The 80286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.



**Figure 1. 80286 Internal Block Diagram**

**Component Pad View**—As viewed from underside of component when mounted on the board.

**P.C. Board View**—As viewed from the component side of the P.C. board.

**NOTE:** N.C. pads must not be connected.

**Figure 2. 80286 Pin Configuration**

**Table 1. Pin Description**

*The following pin function descriptions are for the 80286 microprocessor:*

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| CLK | I | **System Clock** provides the fundamental timing for iAPX 286 systems. It is divided by two inside the 80286 to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input. |
| $D_{15}$-$D_0$ | I/O | **Data Bus** inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF during bus hold acknowledge. |
| $A_{23}$-$A_0$ | O | **Address Bus** outputs physical memory and I/O port addresses. A0 is LOW when data is to be transferred on pins $D_{7-0}$. $A_{23}$-$A_{16}$ are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF during bus hold acknowledge. |
| BHE | O | **Bus High Enable** indicates transfer of data on the upper byte of the data bus, $D_{15-8}$. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE to condition chip select functions. BHE is active LOW and floats to 3-state OFF during bus hold acknowledge. |

| BHE and A0 Encodings | | |
|---|---|---|
| BHE Value | A0 Value | Function |
| 0 | 0 | Word transfer |
| 0 | 1 | Byte transfer on upper half of data bus ($D_{15-8}$) |
| 1 | 0 | Byte transfer on lower half of data bus ($D_{7-0}$) |
| 1 | 1 | Reserved |

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## Table 1. Pin Description (Cont.)

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| $\overline{S1}$, $\overline{S0}$ | O | **Bus Cycle Status** indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is in a $T_S$ state whenever one or both are LOW. $\overline{S1}$ and $\overline{S0}$ are active LOW and float to 3-state OFF during bus hold acknowledge. |

| 80286 Bus Cycle Status Definition | | | | |
|---|---|---|---|---|
| COD/$\overline{INTA}$ | M/$\overline{IO}$ | $\overline{S1}$ | $\overline{S0}$ | Bus cycle initiated |
| 0 (LOW) | 0 | 0 | 0 | Interrupt acknowledge |
| 0 | 0 | 0 | 1 | Reserved |
| 0 | 0 | 1 | 0 | Reserved |
| 0 | 0 | 1 | 1 | None, not a status cycle |
| 0 | 1 | 0 | 0 | IF A1 = 1 then halt; else shutdown |
| 0 | 1 | 0 | 1 | Memory data read |
| 0 | 1 | 1 | 0 | Memory data write |
| 0 | 1 | 1 | 1 | None, not a status cycle |
| 1 (HIGH) | 0 | 0 | 0 | Reserved |
| 1 | 0 | 0 | 1 | I/O read |
| 1 | 0 | 1 | 0 | I/O write |
| 1 | 0 | 1 | 1 | None, not a status cycle |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Memory instruction read |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | None: not a status cycle |

| Symbol | Type | Name and Function |
|--------|------|-------------------|
| M/$\overline{IO}$ | O | **Memory/IO Select** distinguishes memory access from I/O access. If HIGH during $T_S$, a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/$\overline{IO}$ floats to 3-state OFF during bus hold acknowledge. |
| COD/$\overline{INTA}$ | O | **Code/Interrupt Acknowledge** distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{INTA}$ floats to 3-state OFF during bus hold acknowledge. Its timing is the same as M/$\overline{IO}$. |
| $\overline{LOCK}$ | O | **Bus Lock** indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{LOCK}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{LOCK}$ is active LOW and floats to 3-state OFF during bus hold acknowledge. |
| $\overline{READY}$ | I | **Bus Ready** terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ LOW. $\overline{READY}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{READY}$ is ignored during bus hold acknowledge. |
| HOLD<br>HLDA | I<br>O | **Bus Hold Request and Hold Acknowledge** control ownership of the 80286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the 80286 will float its bus drivers to 3-state OFF and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the 80286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH. |
| INTR | I | **Interrupt Request** requests the 80286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock. |
| NMI | I | **Non-maskable Interrupt Request** interrupts the 80286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the 80286 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles. |

## Table 1. Pin Description (Cont.)

| Symbol | Type | Name and Function |
|---|---|---|
| PEREQ<br>PEACK | I<br>O | **Processor Extension Operand Request and Acknowledge** extend the memory management and protection capabilities of the 80286 to processor extensions. The PEREQ input requests the 80286 to perform a data operand transfer for a processor extension. The PEACK output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH and floats to 3-state OFF during bus hold acknowledge. PEACK may be asynchronous to the system clock. PEACK is active LOW. |
| BUSY<br>ERROR | I<br>I | **Processor Extension Busy and Error** indicate the operating condition of a processor extension to the 80286. An active BUSY input stops 80286 program execution on WAIT and some ESC instructions until BUSY becomes inactive (HIGH). The 80286 may be interrupted while waiting for BUSY to become inactive. An active ERROR input causes the 80286 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock. |
| RESET | I | **System Reset** clears the internal logic of the 80286 and is active HIGH. The 80286 may be re-initialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the 80286 enter the state shown below:<br><br>**80286 Pin State During Reset**<br><br>| Pin Value | Pin Names |<br>| --- | --- |<br>| 1 (HIGH) | S0, S1, PEACK, A23-A0, BHE, LOCK |<br>| 0 (LOW) | M/IO, COD/INTA, HLDA |<br>| 3-state OFF | D15–D0 |<br><br>Operation of the 80286 begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the 80286 for internal initializations before the first bus cycle to fetch code from the power-on execution address is performed.<br><br>A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock. |
| VSS | I | **System Ground:** 0 Volts. |
| VCC | I | **System Power:** +5 Volt Power Supply. |
| CAP | I | **Substrate Filter Capacitor:** a 0.047μf ± 20% 12V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum DC leakage current of 1 μa is allowed through the capacitor.<br><br>For correct operation of the 80286, the substrate bias generator must charge this capacitor to its operating voltage. The capacitor chargeup time is 5 milliseconds (max.) after VCC and CLK reach their specified AC and DC parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the 80286 processor clock can be phase synchronized to another clock by pulsing RESET LOW synchronous to the system clock. |

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# 80386
# HIGH PERFORMANCE 32-BIT CHMOS MICROPROCESSOR
# WITH INTEGRATED MEMORY MANAGEMENT

- **Flexible 32-Bit Microprocessor**
  - — 8, 16, 32-Bit Data Types
  - — 8 General Purpose 32-Bit Registers

- **Very Large Address Space**
  - — 4 Gigabyte Physical
  - — 64 Terabyte Virtual
  - — 4 Gigabyte Maximum Segment Size

- **Integrated Memory Management Unit**
  - — Virtual Memory Support
  - — Optional On-Chip Paging
  - — 4 Levels of Protection
  - — Fully Compatible with 80286

- **Object Code Compatible with All 8086 Family Microprocessors**

- **Virtual 8086 Mode Allows Running of 8086 Software in a Protected and Paged System**

- **Hardware Debugging Support**

- **Optimized for System Performance**
  - — Pipelined Instruction Execution
  - — On-Chip Address Translation Caches
  - — 16 and 20 MHz Clock
  - — 32 and 40 Megabytes/Sec Bus Bandwidth

- **High Speed Numerics Support via 80387 Coprocessor**

- **Complete System Development Support**
  - — Software: C, PL/M, Assembler System Generation Tools
  - — Debuggers: PSCOPE, ICE™-386

- **High Speed CHMOS III Technology**

- **132 Pin Grid Array Package**
  (See Packaging Specification, Order #231369)

The 80386 is an advanced 32-bit microprocessor designed for applications needing very high performance and optimized for multitasking operating systems. The 32-bit registers and data paths support 32-bit addresses and data types. The processor addresses up to four gigabytes of physical memory and 64 terabytes (2\*\*46) of virtual memory. The integrated memory management and protection architecture includes address translation registers, advanced multitasking hardware and a protection mechanism to support operating systems. In addition, the 80386 allows the simultaneous running of multiple operating systems. Instruction pipelining, on-chip address translation, and high bus bandwidth ensure short average instruction execution times and high system throughput.

The 80386 offers new testability and debugging features. Testability features include a self-test and direct access to the page translation cache. Four new breakpoint registers provide breakpoint traps on code execution or data accesses, for powerful debugging of even ROM-based systems.

Object-code compatibility with all 8086 family members (8086, 8088, 80186, 80188, 80286) means the 80386 offers immediate access to the world's largest microprocessor software base.
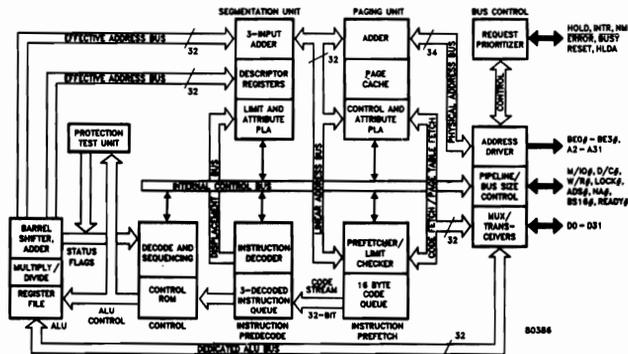


**Figure 1-1. 80386 Pipelined 32-Bit Microarchitecture**

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## 2. BASE ARCHITECTURE

### 2.1 INTRODUCTION

The 80386 consists of a central processing unit, a memory management unit and a bus interface.

The central processing unit consists of the execution unit and instruction unit. The execution unit contains the eight 32-bit general purpose registers which are used for both address calculation, data operations and a 64-bit barrel shifter used to speed shift, rotate, multiply, and divide operations. The multiply and divide logic uses a 1-bit per cycle algorithm. The multiply algorithm stops the iteration when the most significant bits of the multiplier are all zero. This allows typical 32-bit multiplies to be executed in under one microsecond. The instruction unit decodes the instruction opcodes and stores them in the decoded instruction queue for immediate use by the execution unit.

The memory management unit (MMU) consists of a segmentation unit and a paging unit. Segmentation allows the managing of the logical address space by providing an extra addressing component, one that allows easy code and data relocatability, and efficient sharing. The paging mechanism operates beneath and is transparent to the segmentation process, to allow management of the physical address space. Each segment is divided into one or more 4K byte pages. To implement a virtual memory system, the 80386 supports full restartability for all page and segment faults.

Memory is organized into one or more variable length segments, each up to four gigabytes in size. A given region of the linear address space, a segment, can have attributes associated with it. These attributes include its location, size, type (i.e. stack, code or data), and protection characteristics. Each task on an 80386 can have a maximum of 16,381 segments of up to four gigabytes each, thus providing 64 terabytes (trillion bytes) of virtual memory to each task.

The segmentation unit provides four-levels of protection for isolating and protecting applications and the operating system from each other. The hardware enforced protection allows the design of systems with a high degree of integrity.

The 80386 has two modes of operation: Real Address Mode (Real Mode), and Protected Virtual Address Mode (Protected Mode). In Real Mode the 80386 operates as a very fast 8086, but with 32-bit extensions if desired. Real Mode is required primarily to setup the processor for Protected Mode operation. Protected Mode provides access to the sophisticated memory management, paging and privilege capabilities of the processor.

Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each such task behaves with 8086 semantics, thus allowing 8086 software (an application program, or an entire operating system) to execute. The Virtual 8086 tasks can be isolated and protected from one another and the host 80386 operating system, by the use of paging, and the I/O Permission Bitmap.

Finally, to facilitate high performance system hardware designs, the 80386 bus interface offers address pipelining, dynamic data bus sizing, and direct Byte Enable signals for each byte of the data bus. These hardware features are described fully beginning in Section 5.

### 2.2 REGISTER OVERVIEW

The 80386 has 32 register resources in the following categories:

- General Purpose Registers
- Segment Registers
- Instruction Pointer and Flags
- Control Registers
- System Address Registers
- Debug Registers
- Test Registers.

The registers are a superset of the 8086, 80186 and 80286 registers, so all 16-bit 8086, 80186 and 80286 registers are contained within the 32-bit 80386.

Figure 2-1 shows all of 80386 base architecture registers, which include the general address and data registers, the instruction pointer, and the flags register. The contents of these registers are task-specific, so these registers are automatically loaded with a new context upon a task switch operation.

The base architecture also includes six directly accessible segments, each up to 4 Gbytes in size. The segments are indicated by the selector values placed in 80386 segment registers of Figure 2-1. Various selector values can be loaded as a program executes, if desired.

GENERAL DATA AND ADDRESS REGISTERS
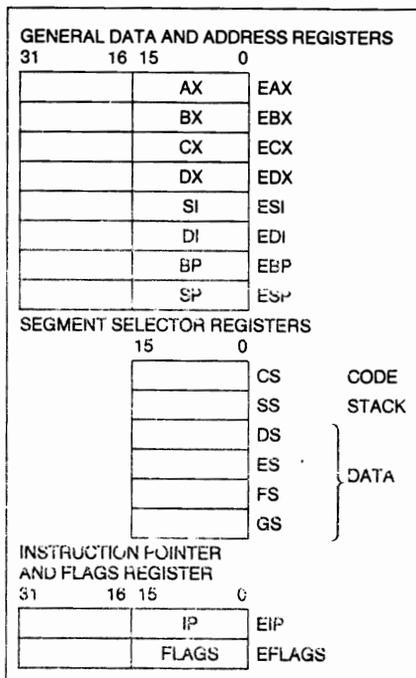
Figure 2-1. 80386 Base Architecture Registers

The selectors are also task-specific, so the segment registers are automatically loaded with new context upon a task switch operation.

The other types of registers, Control, System Address, Debug, and Test, are primarily used by system software.

## 2.3 REGISTER DESCRIPTIONS

### 2.3.1 General Purpose Registers

**General Purpose Registers:** The eight general purpose registers of 32 bits hold data or address quantities. The general registers, Figure 2-2, support data operands of 1, 8, 16, 32 and 64 bits, and bit fields of 1 to 32 bits. They support address operands of 16 and 32 bits. The 32-bit registers are named EAX, EBX, ECX, EDX, ESI, EDI, EBP, and ESP.

The least significant 16 bits of the registers can be accessed separately. This is done by using the 16-bit names of the registers AX, BX, CX, DX, SI, DI, BP, and SP. When accessed as a 16-bit operand, the upper 16 bits of the register are neither used nor changed.

Finally 8-bit operations can individually access the lowest byte (bits 0–7) and the higher byte (bits 8–15) of general purpose registers AX, BX, CX and DX. The lowest bytes are named AL, BL, CL and DL, respectively. The higher bytes are named AH, BH, CH and DH, respectively. The individual byte accessibility offers additional flexibility for data operations, but is not used for effective address calculation.
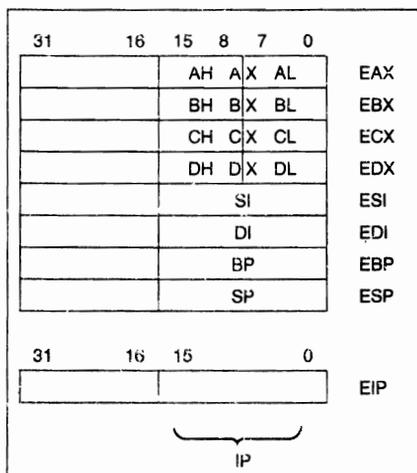
Figure 2-2. General Registers and Instruction Pointer

### 2.3.2 Instruction Pointer

The instruction pointer, Figure 2-2, is a 32-bit register named EIP. EIP holds the offset of the next instruction to be executed. The offset is always relative to the base of the code segment (CS). The lower 16 bits (bits 0–15) of EIP contain the 16-bit instruction pointer named IP, which is used by 16-bit addressing.

### 2.3.3 Flags Register

The Flags Register is a 32-bit register named EFLAGS. The defined bits and bit fields within EFLAGS, shown in Figure 2-3, control certain operations and indicate status of the 80386. The lower 16 bits (bit 0–15) of EFLAGS contain the 16-bit flag register named FLAGS, which is most useful when executing 8086 and 80286 code.

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**NOTE:**
Ω indicates Intel reserved: do not define; see section 2.3.10.

**Figure 2-3. Flags Register**

VM (Virtual 8086 Mode, bit 17)

The VM bit provides Virtual 8086 Mode within Protected Mode. If set while the 80386 is in Protected Mode, the 80386 will switch to Virtual 8086 operation, handling segment loads as the 8086 does, but generating exception 13 faults on privileged opcodes. The VM bit can be set only in Protected Mode, by the IRET instruction (if current privilege level = 0) and by task switches at any privilege level. The VM bit is unaffected by POPF. PUSHF always pushes a 0 in this bit, even if executing in virtual 8086 Mode. The EFLAGS image pushed during interrupt processing or saved during task switches will contain a 1 in this bit if the interrupted code was executing as a Virtual 8086 Task.

RF (Resume Flag, bit 16)

The RF flag is used in conjunction with the debug register breakpoints. It is checked at instruction boundaries before breakpoint processing. When RF is set, it causes any debug fault to be ignored on the next instruction. RF is then automatically reset at the successful completion of every instruction (no faults are signalled) except the IRET instruction, the POPF instruction, (and JMP, CALL, and INT instructions causing a task switch). These instructions set RF to the value specified by the memory image. For example, at the end of the breakpoint service routine, the IRET instruction can pop an EFLAG image having the RF bit set and resume the program's execution at the breakpoint address without generating another breakpoint fault on the same location.

NT (Nested Task, bit 14)

This flag applies to Protected Mode. NT is set to indicate that the execution of this task is nested within another task. If set, it indicates that the current nested task's Task State Segment (TSS) has a valid back link to the previous task's TSS. This bit is set or reset by control transfers to other tasks. The value of NT in EFLAGS is tested by the IRET instruction to determine whether to do an inter-task return or an intra-task return. A POPF or an IRET instruction will affect the setting of this bit according to the image popped, at any privilege level.

IOPL (Input/Output Privilege Level, bits 12-13)

This two-bit field applies to Protected Mode. IOPL indicates the numerically maximum CPL (current privilege level) value permitted to execute I/O instructions without generating an exception 13 fault or consulting the I/O Permission Bitmap. It also indicates the maximum CPL value allowing alteration of the IF (INTR Enable Flag) bit when new values are popped into the EFLAG register. POPF and IRET instruction can alter the IOPL field when executed at CPL = 0. Task switches can always alter the IOPL field, when the new flag image is loaded from the incoming task's TSS.

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OF (Overflow Flag, bit 11)

OF is set if the operation resulted in a signed overflow. Signed overflow occurs when the operation resulted in carry/borrow **into** the sign bit (high-order bit) of the result but did not result in a carry/borrow **out of** the high-order bit, or vice-versa. For 8/16/32 bit operations, OF is set according to overflow at bit 7/15/31, respectively.

DF (Direction Flag, bit 10)

DF defines whether ESI and/or EDI registers postdecrement or postincrement during the string instructions. Postincrement occurs if DF is reset. Postdecrement occurs if DF is set.

IF (INTR Enable Flag, bit 9)

The IF flag, when set, allows recognition of external interrupts signalled on the INTR pin. When IF is reset, external interrupts signalled on the INTR are not recognized. IOPL indicates the maximum CPL value allowing alteration of the IF bit when new values are popped into EFLAGS or FLAGS.

TF (Trap Enable Flag, bit 8)

TF controls the generation of exception 1 trap when single-stepping through code. When TF is set, the 80386 generates an exception 1 trap after the next instruction is executed. When TF is reset, exception 1 traps occur only as a function of the breakpoint addresses loaded into debug registers DR0–DR3.

SF (Sign Flag, bit 7)

SF is set if the high-order bit of the result is set, it is reset otherwise. For 8-, 16-, 32-bit operations, SF reflects the state of bit 7, 15, 31 respectively.

ZF (Zero Flag, bit 6)

ZF is set if all bits of the result are 0. Otherwise it is reset.

AF (Auxiliary Carry Flag, bit 4)

The Auxiliary Flag is used to simplify the addition and subtraction of packed BCD quantities. AF is set if the operation resulted in a carry out of bit 3 (addition) or a borrow into bit 3 (subtraction). Otherwise AF is reset. AF is affected by carry out of, or borrow into bit 3 only, regardless of overall operand length: 8, 16 or 32 bits.

PF (Parity Flags, bit 2)

PF is set if the low-order eight bits of the operation contains an even number of "1's" (even parity). PF is reset if the low-order eight bits have odd parity. PF is a function of only the low-order eight bits, regardless of operand size.

CF (Carry Flag, bit 0)

CF is set if the operation resulted in a carry out of (addition), or a borrow into (subtraction) the high-order bit. Otherwise CF is reset. For 8-, 16- or 32-bit operations, CF is set according to carry/borrow at bit 7, 15 or 31, respectively.

Note in these descriptions, "set" means "set to 1," and "reset" means "reset to 0."

### 2.3.4 Segment Registers

Six 16-bit segment registers hold segment selector values identifying the currently addressable memory segments. Segment registers are shown in Figure 2-4. In Protected Mode, each segment may range in size from one byte up to the entire linear and physi-
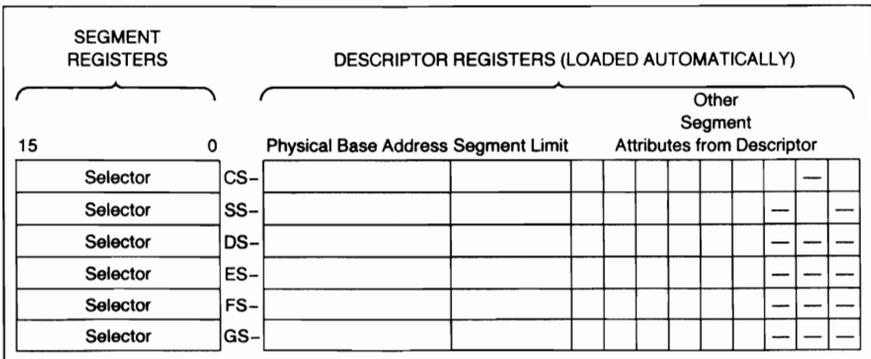


Figure 2-4. 80386 Segment Registers, and Associated Descriptor Registers

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cal space of the machine, 4 Gbytes ($2^{32}$ bytes). In Real Address Mode, the maximum segment size is fixed at 64 Kbytes ($2^{16}$ bytes).

The six segments addressable at any given moment are defined by the segment registers CS, SS, DS, ES, FS and GS. The selector in CS indicates the current code segment; the selector in SS indicates the current stack segment; the selectors in DS, ES, FS and GS indicate the current data segments.

## 2.3.5 Segment Descriptor Registers

The segment descriptor registers are not programmer visible, yet it is very useful to understand their content. Inside the 80386, a descriptor register (programmer invisible) is associated with each programmer-visible segment register, as shown by Figure 2-4. Each descriptor register holds a 32-bit segment base address, a 32-bit segment limit, and the other necessary segment attributes.

When a selector value is loaded into a segment register, the associated descriptor register is automatically updated with the correct information. In Real Address Mode, only the base address is updated directly (by shifting the selector value four bits to the left), since the segment maximum limit and attributes are fixed in Real Mode. In Protected Mode, the base address, the limit, and the attributes are all updated per the contents of the segment descriptor indexed by the selector.

Whenever a memory reference occurs, the segment descriptor register associated with the segment being used is automatically involved with the memory reference. The 32-bit segment base address becomes a component of the linear address calculation, the 32-bit limit is used for the limit-check operation, and the attributes are checked against the type of memory reference requested.

## 2.3.6 Control Registers

The 80386 has three control registers of 32 bits, CR0, CR2 and CR3, to hold machine state of a global nature (not specific to an individual task). These registers, along with System Address Registers described in the next section, hold machine state that affects all tasks in the system. To access the Control Registers, load and store instructions are defined.

### CR0: Machine Control Register (includes 80286 Machine Status Word)

CR0, shown in Figure 2-5, contains 6 defined bits for control and status purposes. The low-order 16 bits of CR0 are also known as the Machine Status Word, MSW, for compatibility with 80286 Protected Mode. LMSW and SMSW instructions are taken as special aliases of the load and store CR0 operations, where only the low-order 16 bits of CR0 are involved. For compatibility with 80286 operating systems the 80386's LMSW instructions work in an identical fashion to the LMSW instruction on the 80286. (i.e. It only operates on the low-order 16-bits of CR0 and it ignores the new bits in CR0.) New 80386 operating systems should use the MOV CR0, Reg instruction.

The defined CR0 bits are described below.

PG  (Paging Enable, bit 31)

the PG bit is set to enable the on-chip paging unit. It is reset to disable the on-chip paging unit.

ET  (Processor Extension Type, bit 4)

ET indicates the processor extension type (either 80287 or 80387) as detected by the level of the ERROR≠ input following 80386 reset. The ET bit may also be set or reset by loading CR0 under program control if desired. If ET is set, the 80387-compatible 32-bit protocol is used. If ET is reset, 80287-compatible 16-bit protocol is used.

Note that for strict 80286 compatibility, ET is not affected by the LMSW instruction. When the MSW or CR0 is stored, bit 4 accurately reflects the current state of the ET bit.



| 31 | 24 | 23 | 16 | 15 | 8 | 7 | | | | 0 | |
|----|----|----|----|----|---|---|---|---|---|---|---|
| P G | | | | | | | E T | T S | E M | M P | P E | CR0 |

MSW

NOTE: ▓▓ indicates Intel reserved: Do not define; SEE SECTION 2.3.10
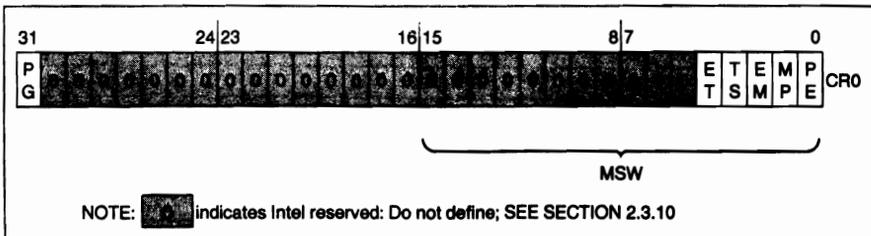
**Figure 2-5. Control Register 0**

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**TS**  (Task Switched, bit 3)

TS is automatically set whenever a task switch operation is performed. If TS is set, a coprocessor ESCape opcode will cause a Coprocessor Not Available trap (exception 7). The trap handler typically saves the 80287/80387 context belonging to a previous task, loads the 80287/80387 state belonging to the current task, and clears the TS bit before returning to the faulting coprocessor opcode.

**EM**  (Emulate Coprocessor, bit 2)

The EMulate coprocessor bit is set to cause all coprocessor opcodes to generate a Coprocessor Not Available fault (exception 7). It is reset to allow coprocessor opcodes to be executed on an actual 80287 or 80387 coprocessor (this the default case after reset). Note that the WAIT opcode is not affected by the EM bit setting.

**MP**  (Monitor Coprocessor, bit 1)

The MP bit is used in conjunction with the TS bit to determine if the WAIT opcode will generate a Coprocessor Not Available fault (exception 7) when TS = 1. When both MP = 1 and TS = 1, the WAIT opcode generates a trap. Otherwise, the WAIT opcode does not generate a trap. Note that TS is automatically set whenever a task switch operation is performed.

**PE**  (Protection Enable, bit 0)

The PE bit is set to enable the Protected Mode. If PE is reset, the processor operates again in Real Mode. PE may be set by loading MSW or CR0. PE can be reset only by a load into CR0. Resetting the PE bit is typically part of a longer instruction sequence needed for proper transition from Protected Mode to Real Mode. Note that for strict 80286 compatibility, PE cannot be reset by the LMSW instruction.

**CR1: reserved**

CR1 is reserved for use in future Intel processors.

**CR2: Page Fault Linear Address**

CR2, shown in Figure 2-6, holds the 32-bit linear address that caused the last page fault detected. The error code pushed onto the page fault handler's stack when it is invoked provides additional status information on this page fault.

**CR3: Page Directory Base Address**

CR3, shown in Figure 2-6, contains the physical base address of the page directory table. The 80386 page directory table is always page-aligned (4 Kbyte-aligned). Therefore the lowest twelve bits of CR3 are ignored when written and they store as undefined.

A task switch through a TSS which **changes** the value in CR3, or an explicit load into CR3 with any value, will invalidate all cached page table entries in the paging unit cache. Note that if the value in CR3 does not change during the task switch, the cached page table entries are not flushed.

## 2.3.7  System Address Registers

Four special registers are defined to reference the tables or segments supported by the 80286/80386 protection model. These tables or segments are:

GDT (Global Descriptor Table),

IDT (Interrupt Descriptor Table),

LDT (Local Descriptor Table),

TSS (Task State Segment).

The addresses of these tables and segments are stored in special registers, the System Address and System Segment Registers illustrated in Figure 2-7. These registers are named GDTR, IDTR, LDTR and TR, respectively. Section 4 **Protected Mode Architecture** describes the use of these registers.

**GDTR and IDTR**

These registers hold the 32-bit linear base address and 16-bit limit of the GDT and IDT, respectively.

The GDT and IDT segments, since they are global to all tasks in the system, are defined by 32-bit linear addresses (subject to page translation if paging is enabled) and 16-bit limit values.

| 31 | 24 | 23 | 16 | 15 | 8 | 7 | 0 | |
|----|----|----|----|----|---|---|---|---|
| PAGE FAULT LINEAR ADDRESS REGISTER | | | | | | | | CR2 |
| PAGE DIRECTORY BASE REGISTER | | | | 0 0 0 0 0 0 0 0 0 0 0 0 | | | | CR3 |

NOTE: ▓0▓ indicates Intel reserved: Do not define; SEE SECTION 2.3.10
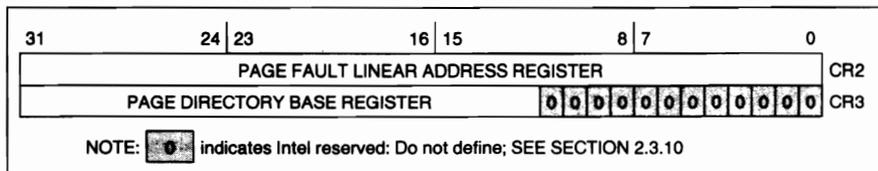
**Figure 2-6. Control Registers 2 and 3**

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SYSTEM ADDRESS REGISTERS
47 32-BIT LINEAR BASE ADDRESS 16 15     LIMIT     0

GDTR
IDTR

SYSTEM SEGMENT
REGISTERS                    DESCRIPTOR REGISTERS (AUTOMATICALLY LOADED)

15          0        32-BIT LINEAR BASE ADDRESS    32-BIT SEGMENT LIMIT    ATTRIBUTES

TR    SELECTOR
LDTR    SELECTOR
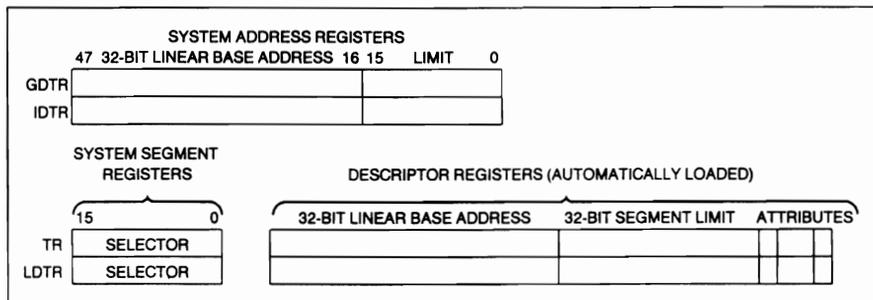
**Figure 2-7. System Address and System Segment Registers**

### LDTR and TR

These registers hold the 16-bit selector for the LDT descriptor and the TSS descriptor, respectively.

The LDT and TSS segments, since they are task-specific segments, are defined by selector values stored in the system segment registers. Note that a segment descriptor register (programmer-invisible) is associated with each system segment register.

### 2.3.8 Debug and Test Registers

**Debug Registers:** The six programmer accessible debug registers provide on-chip support for debugging. Debug Registers DR0–3 specify the four linear breakpoints. The Debug Control Register DR7 is used to set the breakpoints and the Debug Status Register DR6, displays the current state of the breakpoints. The use of the debug registers is described in section 2.12 **Debugging support.**

DEBUG REGISTERS
31                    0

| LINEAR BREAKPOINT ADDRESS 0 | DR0 |
| LINEAR BREAKPOINT ADDRESS 1 | DR1 |
| LINEAR BREAKPOINT ADDRESS 2 | DR2 |
| LINEAR BREAKPOINT ADDRESS 3 | DR3 |
| Intel reserved. Do not define. | DR4 |
| Intel reserved. Do not define. | DR5 |
| BREAKPOINT STATUS | DR6 |
| BREAKPOINT CONTROL | DR7 |

TEST REGISTERS (FOR PAGE CACHE)
31                    0

| TEST CONTROL | TR6 |
| TEST STATUS | TR7 |
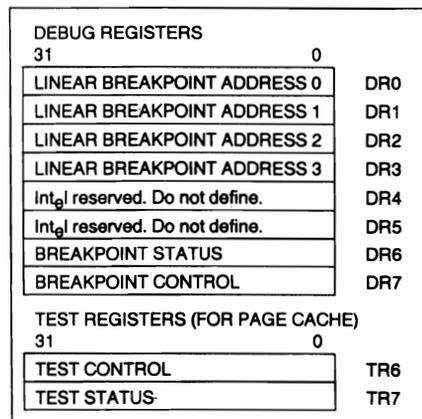
**Figure 2-8. Debug and Test Registers**

**Test Registers:** Two registers are used to control the testing of the RAM/CAM (Content Addressable Memories) in the Translation Lookaside Buffer portion of the 80386. TR6 is the command test register, and TR7 is the data register which contains the data of the Translation Lookaside buffer test. Their use is discussed in section 2.11 **Testability.**

Figure 2-8 shows the Debug and Test registers.

### 2.3.9 Register Accessibility

There are a few differences regarding the accessibility of the registers in Real and Protected Mode. Table 2-1 summarizes these differences. See Section 4 **Protected Mode Architecture** for further details.

### 2.3.10 Compatibility

**VERY IMPORTANT NOTE:**
**COMPATIBILITY WITH FUTURE PROCESSORS**

In the preceding register descriptions, note certain 80386 register bits are Intel reserved. When reserved bits are called out, treat them as fully undefined. This is essential for your software compatibility with future processors! Follow the guidelines below:

1) Do not depend on the states of any undefined bits when testing the values of defined register bits. Mask them out when testing.

2) Do not depend on the states of any undefined bits when storing them to memory or another register.

3) Do not depend on the ability to retain information written into any undefined bits.

4) When loading registers always load the undefined bits as zeros.

**Table 2-1. Register Usage**

| Register | Use in Real Mode | | Use in Protected Mode | | Use in Virtual 8086 Mode | |
|---|---|---|---|---|---|---|
| | Load | Store | Load | Store | Load | Store |
| General Registers | Yes | Yes | Yes | Yes | Yes | Yes |
| Segment Registers | Yes | Yes | Yes | Yes | Yes | Yes |
| Flag Register | Yes | Yes | Yes | Yes | IOPL | IOPL* |
| Control Registers | Yes | Yes | PL = 0 | PL = 0 | No | Yes |
| GDTR | Yes | Yes | PL = 0 | Yes | No | Yes |
| IDTR | Yes | Yes | PL = 0 | Yes | No | Yes |
| LDTR | No | No | PL = 0 | Yes | No | No |
| TR | No | No | PL = 0 | Yes | No | No |
| Debug Control | Yes | Yes | PL = 0 | PL = 0 | No | No |
| Test Registers | Yes | Yes | PL = 0 | PL = 0 | No | No |

**NOTES:**
PL = 0: The registers can be accessed only when the current privilege level is zero.
*IOPL: The PUSHF and POPF instructions are made I/O Privilege Level sensitive in Virtual 8086 Mode.

5) However, registers which have been previously stored may be reloaded without masking.

Depending upon the values of undefined register bits will make your software dependent upon the unspecified 80386 handling of these bits. Depending on undefined values risks making your software incompatible with future processors that define usages for the 80386-undefined bits. AVOID ANY SOFTWARE DEPENDENCE UPON THE STATE OF UNDEFINED 80386 REGISTER BITS.

## 2.4 INSTRUCTION SET

### 2.4.1 Instruction Set Overview

The instruction set is divided into nine categories of operations:

Data Transfer
Arithmetic
Shift/Rotate
String Manipulation
Bit Manipulation
Control Transfer
High Level Language Support
Operating System Support
Processor Control

These 80386 instructions are listed in Table 2-2.

All 80386 instructions operate on either 0, 1, 2, or 3 operands; where an operand resides in a register, in the instruction itself, or in memory. Most zero operand instructions (e.g. CLI, STI) take only one byte. One operand instructions generally are two bytes long. The average instruction is 3.2 bytes long. Since the 80386 has a 16-byte instruction queue, an average of 5 instructions will be prefetched. The use of two operands permits the following types of common instructions:

Register to Register
Memory to Register
Immediate to Register
Register to Memory
Immediate to Memory.

The operands can be either 8, 16, or 32 bits long. As a general rule, when executing code written for the 80386 (32-bit code), operands are 8 or 32 bits; when executing existing 80286 or 8086 code (16-bit code), operands are 8 or 16 bits. Prefixes can be added to all instructions which override the default length of the operands, (i.e. use 32-bit operands for 16-bit code, or 16-bit operands for 32-bit code).

## 2.4.2 80386 Instructions

### Table 2-2a. Data Transfer

#### GENERAL PURPOSE

| | |
|---|---|
| MOV | Move operand |
| PUSH | Push operand onto stack |
| POP | Pop operand off stack |
| PUSHA | Push all registers on stack |
| POPA | Pop all registers off stack |
| XCHG | Exchange Operand, Register |
| XLAT | Translate |

#### CONVERSION

| | |
|---|---|
| MOVZX | Move byte or Word, Dword, with zero extension |
| MOVSX | Move byte or Word, Dword, sign extended |
| CBW | Convert byte to Word, or Word to Dword |
| CWD | Convert Word to DWORD |
| CWDE | Convert Word to DWORD extended |
| CDQ | Convert DWORD to QWORD |

#### INPUT/OUTPUT

| | |
|---|---|
| IN | Input operand from I/O space |
| OUT | Output operand to I/O space |

#### ADDRESS OBJECT

| | |
|---|---|
| LEA | Load effective address |
| LDS | Load pointer into D segment register |
| LES | Load pointer into E segment register |
| LFS | Load pointer into F segment register |
| LGS | Load pointer into G segment register |
| LSS | Load pointer into S (Stack) segment register |

#### FLAG MANIPULATION

| | |
|---|---|
| LAHF | Load A register from Flags |
| SAHF | Store A register in Flags |
| PUSHF | Push flags onto stack |
| POPF | Pop flags off stack |
| PUSHFD | Push EFlags onto stack |
| POPFD | Pop EFlags off stack |
| CLC | Clear Carry Flag |
| CLD | Clear Direction Flag |
| CMC | Complement Carry Flag |
| STC | Set Carry Flag |
| STD | Set Direction Flag |

### Table 2-2b. Arithmetic Instructions

#### ADDITION

| | |
|---|---|
| ADD | Add operands |
| ADC | Add with carry |
| INC | Increment operand by 1 |
| AAA | ASCII adjust for addition |
| DAA | Decimal adjust for addition |

#### SUBTRACTION

| | |
|---|---|
| SUB | Subtract operands |
| SBB | Subtract with borrow |
| DEC | Decrement operand by 1 |
| NEG | Negate operand |
| CMP | Compare operands |
| DAS | Decimal adjust for subtraction |
| AAS | ASCII Adjust for subtraction |

#### MULTIPLICATION

| | |
|---|---|
| MUL | Multiply Double/Single Precision |
| IMUL | Integer multiply |
| AAM | ASCII adjust after multiply |

#### DIVISION

| | |
|---|---|
| DIV | Divide unsigned |
| IDIV | Integer Divide |
| AAD | ASCII adjust before division |

### Table 2-2c. String Instructions

| | |
|---|---|
| MOVS | Move byte or Word, Dword string |
| INS | Input string from I/O space |
| OUTS | Output string to I/O space |
| CMPS | Compare byte or Word, Dword string |
| SCAS | Scan Byte or Word, Dword string |
| LODS | Load byte or Word, Dword string |
| STOS | Store byte or Word, Dword string |
| REP | Repeat |
| REPE/ REPZ | Repeat while equal/zero |
| RENE/ REPNZ | Repeat while not equal/not zero |

### Table 2-2d. Logical Instructions

#### LOGICALS

| | |
|---|---|
| NOT | "NOT" operands |
| AND | "AND" operands |
| OR | "Inclusive OR" operands |
| XOR | "Exclusive OR" operands |
| TEST | "Test" operands |

### Table 2-2d. Logical Instructions (Continued)

| SHIFTS | |
|---|---|
| SHL/SHR | Shift logical left or right |
| SAL/SAR | Shift arithmetic left or right |
| SHLD/ SHRD | Double shift left or right |
| ROTATES | |
| ROL/ROR | Rotate left/right |
| RCL/RCR | Rotate through carry left/right |

### Table 2-2e. Bit Manipulation Instructions

| SINGLE BIT INSTRUCTIONS | |
|---|---|
| BT | Bit Test |
| BTS | Bit Test and Set |
| BTR | Bit Test and Reset |
| BTC | Bit Test and Complement |
| BSF | Bit Scan Forward |
| BSR | Bit Scan Reverse |

### Table 2-2f. Program Control Instructions

| CONDITIONAL TRANSFERS | |
|---|---|
| SETCC | Set byte equal to condition code |
| JA/JNBE | Jump if above/not below nor equal |
| JAE/JNB | Jump if above or equal/not below |
| JB/JNAE | Jump if below/not above nor equal |
| JBE/JNA | Jump if below or equal/not above |
| JC | Jump if carry |
| JE/JZ | Jump if equal/zero |
| JG/JNLE | Jump if greater/not less nor equal |
| JGE/JNL | Jump if greater or equal/not less |
| JL/JNGE | Jump if less/not greater nor equal |
| JLE/JNG | Jump if less or equal/not greater |
| JNC | Jump if not carry |
| JNE/JNZ | Jump if not equal/not zero |
| JNO | Jump if not overflow |
| JNP/JPO | Jump if not parity/parity odd |
| JNS | Jump if not sign |
| JO | Jump if overflow |
| JP/JPE | Jump if parity/parity even |
| JS | Jump if Sign |

### Table 2-2f. Program Control Instructions (Continued)

| UNCONDITIONAL TRANSFERS | |
|---|---|
| CALL | Call procedure/task |
| RET | Return from procedure |
| JMP | Jump |
| ITERATION CONTROLS | |
| LOOP | Loop |
| LOOPE/ LOOPZ | Loop if equal/zero |
| LOOPNE/ LOOPNZ | Loop if not equal/not zero |
| JCXZ | JUMP if register CX = 0 |
| INTERRUPTS | |
| INT | Interrupt |
| INTO | Interrupt if overflow |
| IRET | Return from Interrupt/Task |
| CLI | Clear interrupt Enable |
| STI | Set Interrupt Enable |

### Table 2-2g. High Level Language Instructions

| BOUND | Check Array Bounds |
|---|---|
| ENTER | Setup Parameter Block for Entering Procedure |
| LEAVE | Leave Procedure |

### Table 2-2h. Protection Model

| SGDT | Store Global Descriptor Table |
|---|---|
| SIDT | Store Interrupt Descriptor Table |
| STR | Store Task Register |
| SLDT | Store Local Descriptor Table |
| LGDT | Load Global Descriptor Table |
| LIDT | Load Interrupt Descriptor Table |
| LTR | Load Task Register |
| LLDT | Load Local Descriptor Table |
| ARPL | Adjust Requested Privilege Level |
| LAR | Load Access Rights |
| LSL | Load Segment Limit |
| VERR/ VERW | Verify Segment for Reading or Writing |
| LMSW | Load Machine Status Word (lower 16 bits of CR0) |
| SMSW | Store Machine Status Word |

### Table 2-2i. Processor Control Instructions

| HLT | Halt |
|---|---|
| WAIT | Wait until BUSY # negated |
| ESC | Escape |
| LOCK | Lock Bus |

## 2.5 ADDRESSING MODES

### 2.5.1 Addressing Modes Overview

The 80386 provides a total of 11 addressing modes for instructions to specify operands. The addressing modes are optimized to allow the efficient execution of high level languages such as C and FORTRAN, and they cover the vast majority of data references needed by high-level languages.

### 2.5.2 Register and Immediate Modes

Two of the addressing modes provide for instructions that operate on register or immediate operands:

**Register Operand Mode:** The operand is located in one of the 8-, 16- or 32-bit general registers.

**Immediate Operand Mode:** The operand is included in the instruction as part of the opcode.

### 2.5.3 32-Bit Memory Addressing Modes

The remaining 9 modes provide a mechanism for specifying the effective address of an operand. The linear address consists of two components: the segment base address and an effective address. The effective address is calculated by using combinations of the following four address elements:

**DISPLACEMENT:** An 8-, or 32-bit immediate value, following the instruction.

**BASE:** The contents of any general purpose register. The base registers are generally used by compilers to point to the start of the local variable area.

**INDEX:** The contents of any general purpose register except for ESP. The index registers are used to access the elements of an array, or a string of characters.

**SCALE:** The index register's value can be multiplied by a scale factor, either 1, 2, 4 or 8. Scaled index mode is especially useful for accessing arrays or structures.

Combinations of these 4 components make up the 9 additional addressing modes. There is no performance penalty for using any of these addressing combinations, since the effective address calculation is pipelined with the execution of other instructions.

The one exception is the simultaneous use of Base and Index components which requires one additional clock.

As shown in Figure 2-9, the effective address (EA) of an operand is calculated according to the following formula.

$$EA = Base\ Reg + (Index\ Reg\ *\ Scaling) + Displacement$$

Direct Mode: The operand's offset is contained as part of the instruction as an 8-, 16- or 32-bit displacement.
**EXAMPLE: INC Word PTR [500]**

Register Indirect Mode: A BASE register contains the address of the operand.
**EXAMPLE: MOV [ECX], EDX**

Based Mode: A BASE register's contents is added to a DISPLACEMENT to form the operands offset.
**EXAMPLE: MOV ECX, [EAX + 24]**

Index Mode: An INDEX register's contents is added to a DISPLACEMENT to form the operands offset.
**EXAMPLE: ADD EAX, TABLE[ESI]**

Scaled Index Mode: An INDEX register's contents is multiplied by a scaling factor which is added to a DISPLACEMENT to form the operands offset.
**EXAMPLE: IMUL EBX, TABLE[ESI*4],7**

Based Index Mode: The contents of a BASE register is added to the contents of an INDEX register to form the effective address of an operand.
**EXAMPLE: MOV EAX, [ESI] [EBX]**

Based Scaled Index Mode: The contents of an INDEX register is multiplied by a SCALING factor and the result is added to the contents of a BASE register to obtain the operands offset.
**EXAMPLE: MOV ECX, [EDX*8] [EAX]**

Based Index Mode with Displacement: The contents of an INDEX Register and a BASE register's contents and a DISPLACEMENT are all summed together to form the operand offset.
**EXAMPLE: ADD EDX, [ESI] [EBP + 00FFFFF0H]**

Based Scaled Index Mode with Displacement: The contents of an INDEX register are multiplied by a SCALING factor, the result is added to the contents of a BASE register and a DISPLACEMENT to form the operand's offset.
**EXAMPLE: MOV EAX, LOCALTABLE[EDI*4] [EBP + 80]**

## 6. MECHANICAL DATA

### 6.1 INTRODUCTION

In this section, the physical packaging and its connections are described in detail.

### 6.2 PIN ASSIGNMENT

The 80386 pinout as viewed from the top side of the component is shown by Figure 6-1. Its pinout as viewed from the Pin side of the component is Figure 6-2.

$V_{CC}$ and GND connections must be made to multiple $V_{CC}$ and $V_{SS}$ (GND) pins. Each $V_{CC}$ and $V_{SS}$ must be connected to the appropriate voltage level. The circuit board should include $V_{CC}$ and GND planes for power distribution and all $V_{CC}$ and $V_{SS}$ pins must be connected to the appropriate plane.

**NOTE:**
Pins identified as "N.C." should remain completely unconnected.
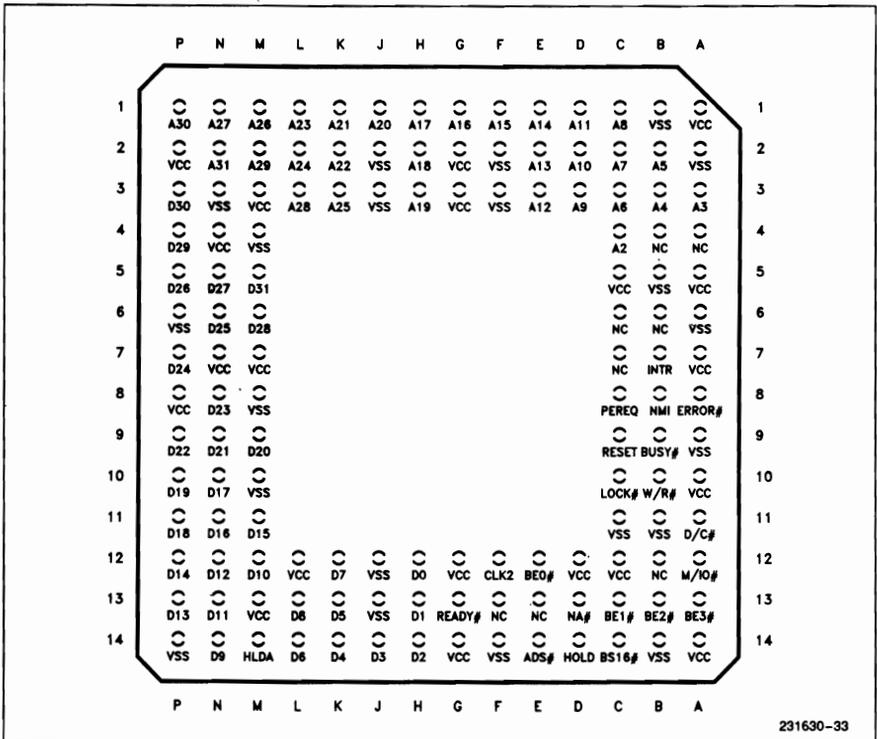


Figure 6-1. 80386 PGA Pinout—View from Top Side

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**Table 6-1. 80386 PGA Pinout—Functional Grouping**

| Pin / Signal | | Pin / Signal | | Pin / Signal | | Pin / Signal | |
|---|---|---|---|---|---|---|---|
| N2 | A31 | M5 | D31 | A1 | $V_{CC}$ | A2 | $V_{SS}$ |
| P1 | A30 | P3 | D30 | A5 | $V_{CC}$ | A6 | $V_{SS}$ |
| M2 | A29 | P4 | D29 | A7 | $V_{CC}$ | A9 | $V_{SS}$ |
| L3 | A28 | M6 | D28 | A10 | $V_{CC}$ | B1 | $V_{SS}$ |
| N1 | A27 | N5 | D27 | A14 | $V_{CC}$ | B5 | $V_{SS}$ |
| M1 | A26 | P5 | D26 | C5 | $V_{CC}$ | B11 | $V_{SS}$ |
| K3 | A25 | N6 | D25 | C12 | $V_{CC}$ | B14 | $V_{SS}$ |
| L2 | A24 | P7 | D24 | D12 | $V_{CC}$ | C11 | $V_{SS}$ |
| L1 | A23 | N8 | D23 | G2 | $V_{CC}$ | F2 | $V_{SS}$ |
| K2 | A22 | P9 | D22 | G3 | $V_{CC}$ | F3 | $V_{SS}$ |
| K1 | A21 | N9 | D21 | G12 | $V_{CC}$ | F14 | $V_{SS}$ |
| J1 | A20 | M9 | D20 | G14 | $V_{CC}$ | J2 | $V_{SS}$ |
| H3 | A19 | P10 | D19 | L12 | $V_{CC}$ | J3 | $V_{SS}$ |
| H2 | A18 | P11 | D18 | M3 | $V_{CC}$ | J12 | $V_{SS}$ |
| H1 | A17 | N10 | D17 | M7 | $V_{CC}$ | J13 | $V_{SS}$ |
| G1 | A16 | N11 | D16 | M13 | $V_{CC}$ | M4 | $V_{SS}$ |
| F1 | A15 | M11 | D15 | N4 | $V_{CC}$ | M8 | $V_{SS}$ |
| E1 | A14 | P12 | D14 | N7 | $V_{CC}$ | M10 | $V_{SS}$ |
| E2 | A13 | P13 | D13 | P2 | $V_{CC}$ | N3 | $V_{SS}$ |
| E3 | A12 | N12 | D12 | P8 | $V_{CC}$ | P6 | $V_{SS}$ |
| D1 | A11 | N13 | D11 | | | P14 | $V_{SS}$ |
| D2 | A10 | M12 | D10 | | | | |
| D3 | A9 | N14 | D9 | F12 | CLK2 | A4 | N.C. |
| C1 | A8 | L13 | D8 | | | B4 | N.C. |
| C2 | A7 | K12 | D7 | E14 | ADS# | B6 | N.C. |
| C3 | A6 | L14 | D6 | | | B12 | N.C. |
| B2 | A5 | K13 | D5 | B10 | W/R# | C6 | N.C. |
| B3 | A4 | K14 | D4 | A11 | D/C# | C7 | N.C. |
| A3 | A3 | J14 | D3 | A12 | M/IO# | E13 | N.C. |
| C4 | A2 | H14 | D2 | C10 | LOCK# | F13 | N.C. |
| A13 | BE3# | H13 | D1 | | | | |
| B13 | BE2# | H12 | D0 | D13 | NA# | C8 | PEREQ |
| C13 | BE1# | | | C14 | BS16# | B9 | BUSY# |
| E12 | BE0# | | | G13 | READY# | A8 | ERROR# |
| | | D14 | HOLD | | | | |
| C9 | RESET | M14 | HLDA | B7 | INTR | B8 | NMI |

## Table 8-1. 80386 Instruction Set Clock Count Summary

| INSTRUCTION | FORMAT | | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|---|
| | | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **GENERAL DATA TRANSFER** | | | | | | |
| **MOV = Move:** | | | | | | |
| Register to Register/Memory | `1000100w` `mod reg r/m` | | 2/2 | 2/2 | b | h |
| Register/Memory to Register | `1000101w` `mod reg r/m` | | 2/4 | 2/4 | b | h |
| Immediate to Register/Memory | `1100011w` `mod 000 r/m` immediate data | | 2/2 | 2/2 | b | h |
| Immediate to Register (short form) | `1011 w reg` immediate data | | 2 | 2 | | |
| Memory to Accumulator (short form) | `1010000w` full displacement | | 4 | 4 | b | h |
| Accumulator to Memory (short form) | `1010001w` full displacement | | 2 | 2 | b | h |
| Register Memory to Segment Register | `10001110` `mod sreg3 r/m` | | 2/5 | 18/19 | b | h, i, j |
| Segment Register to Register/Memory | `10001100` `mod sreg3 r/m` | | 2/2 | 2/2 | b | h |
| **MOVSX = Move With Sign Extension** | | | | | | |
| Register From Register/Memory | `00001111` `1011111w` `mod reg r/m` | | 3/6 | 3/6 | b | h |
| **MOVZX = Move With Zero Extension** | | | | | | |
| Register From Register/Memory | `00001111` `1011011w` `mod reg r/m` | | 3/6 | 3/6 | b | h |
| **PUSH = Push:** | | | | | | |
| Register/Memory | `11111111` `mod 110 r/m` | | 5 | 5 | b | h |
| Register (short form) | `01010 reg` | | 2 | 2 | b | h |
| Segment Register (ES, CS, SS or DS) | `000 sreg2 110` | | 2 | 2 | b | h |
| Segment Register (FS or GS) | `00001111` `10 sreg3 000` | | 2 | 2 | b | h |
| Immediate | `011010s0` immediate data | | 2 | 2 | b | h |
| **PUSHA = Push All** | `01100000` | | 18 | 18 | b | h |
| **POP = Pop** | | | | | | |
| Register/Memory | `10001111` `mod 000 r/m` | | 5 | 5 | b | h |
| Register (short form) | `01011 reg` | | 4 | 4 | b | h |
| Segment Register (ES, SS or DS) | `000 sreg 2 111` | | 7 | 21 | b | h, i, j |
| Segment Register (FS or GS) | `00001111` `10 sreg 3 001` | | 7 | 21 | b | h, i, j |
| **POPA = Pop All** | `01100001` | | 24 | 24 | b | h |
| **XCHG = Exchange** | | | | | | |
| Register/Memory With Register | `1000011w` `mod reg r/m` | | 3/5 | 3/5 | b, f | f, h |
| Register With Accumulator (short form) | `10010 reg` | **Clk Count Virtual 8086 Mode** | 3 | 3 | | |
| **IN = Input from:** | | | | | | |
| Fixed Port | `1110010w` `port number` | †26 | 12 | 6*/26** | | m |
| Variable Port | `1110110w` | †27 | 13 | 7*/27** | | m |
| **OUT = Output to:** | | | | | | |
| Fixed Port | `1110011w` `port number` | †24 | 10 | 4*/24** | | m |
| Variable Port | `1110111w` | †25 | 11 | 5*/25** | | m |
| **LEA = Load EA to Register** | `10001101` `mod reg r/m` | | 2 | 2 | | |

* If CPL ≤ IOPL   ** If CPL > IOPL

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | | | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|---|---|
| | | | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **SEGMENT CONTROL** | | | | | | | |
| LDS = Load Pointer to DS | 11000101 | mod reg | r/m | 7 | 22 | b | h, i, j |
| LES = Load Pointer to ES | 11000100 | mod reg | r/m | 7 | 22 | b | h, i, j |
| LFS = Load Pointer to FS | 00001111 | 10110100 | mod reg r/m | 7 | 25 | b | h, i, j |
| LGS = Load Pointer to GS | 00001111 | 10110101 | mod reg r/m | 7 | 25 | b | h, i, j |
| LSS = Load Pointer to SS | 00001111 | 10110010 | mod reg r/m | 7 | 22 | b | h, i, j |
| **FLAG CONTROL** | | | | | | | |
| CLC = Clear Carry Flag | 11111000 | | | 2 | 2 | | |
| CLD = Clear Direction Flag | 11111100 | | | 2 | 2 | | |
| CLI = Clear Interrupt Enable Flag | 11111010 | | | 8 | 8 | | m |
| CLTS = Clear Task Switched Flag | 00001111 | 00000110 | | 5 | 5 | c | l |
| CMC = Complement Carry Flag | 11110101 | | | 2 | 2 | | |
| LAHF = Load AH into Flag | 10011111 | | | 2 | 2 | | |
| POPF = Pop Flags | 10011101 | | | 5 | 5 | b | h, n |
| PUSHF = Push Flags | 10011100 | | | 4 | 4 | b | h |
| SAHF = Store AH into Flags | 10011110 | | | 3 | 3 | | |
| STC = Set Carry Flag | 11111001 | | | 2 | 2 | | |
| STD = Set Direction Flag | 11111001 | | | 2 | 2 | | |
| STI = Set Interrupt Enable Flag | 11111011 | | | 8 | 8 | | m |
| **ARITHMETIC** **ADD = Add** | | | | | | | |
| Register to Register | 000000dw | mod reg | r/m | 2 | 2 | | |
| Register to Memory | 0000000w | mod reg | r/m | 7 | 7 | b | h |
| Memory to Register | 0000001w | mod reg | r/m | 6 | 6 | b | h |
| Immediate to Register/Memory | 100000sw | mod000 r/m | immediate data | 2/7 | 2/7 | b | h |
| Immediate to Accumulator (short form) | 0000010w | immediate data | | 2 | 2 | | |
| **ADC = Add With Carry** | | | | | | | |
| Register to Register | 000100dw | mod reg | r/m | 2 | 2 | | |
| Register to Memory | 0001000w | mod reg | r/m | 7 | 7 | b | h |
| Memory to Register | 0001001w | mod reg | r/m | 6 | 6 | b | h |
| Immediate to Register/Memory | 100000sw | mod010 r/m | immediate data | 2/7 | 2/7 | b | h |
| Immediate to Accumulator (short form) | 0001010w | immediate data | | 2 | 2 | | |
| **INC = Increment** Register/Memory | 1111111w | mod000 r/m | | 2/6 | 2/6 | b | h |
| Register (short form) | 01000 reg | | | 2 | 2 | | |
| **SUB = Subtract** Register from Register | 001010dw | mod reg | r/m | 2 | 2 | | |

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|
| | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **ARITHMETIC** (Continued) | | | | | |
| Register from Memory | `0010100w` `mod reg` `r/m` | 7 | 7 | b | h |
| Memory from Register | `0010101w` `mod reg` `r/m` | 6 | 6 | b | h |
| Immediate from Register/Memory | `100000sw` `mod 101` `r/m` `immediate data` | 2/7 | 2/7 | b | h |
| Immediate from Accumulator (short form) | `0010110w` `immediate data` | 2 | 2 | | |
| **SBB = Subtract with Borrow** | | | | | |
| Register from Register | `000110dw` `mod reg` `r/m` | 2 | 2 | | |
| Register from Memory | `0001100w` `mod reg` `r/m` | 7 | 7 | b | h |
| Memory from Register | `0001101w` `mod reg` `r/m` | 6 | 6 | b | h |
| Immediate from Register/Memory | `100000sw` `mod 011` `r/m` `immediate data` | 2/7 | 2/7 | b | h |
| Immediate from Accumulator (short form) | `0001110w` `immediate data` | 2 | 2 | | |
| **DEC = Decrement** | | | | | |
| Register/Memory | `1111111w` `reg 001` `r/m` | 2/6 | 2/6 | b | h |
| Register (short form) | `01001` `reg` | 2 | 2 | | |
| **CMP = Compare** | | | | | |
| Register with Register | `001110dw` `mod reg` `r/m` | 2 | 2 | | |
| Memory with Register | `0011100w` `mod reg` `r/m` | 5 | 5 | b | h |
| Register with Memory | `0011101w` `mod reg` `r/m` | 6 | 6 | b | h⁻ |
| Immediate with Register/Memory | `100000sw` `mod 111` `r/m` `immediate data` | 2/5 | 2/5 | b | h |
| Immediate with Accumulator (short form) | `0011110w` `immediate data` | 2 | 2 | | |
| **NEG = Change Sign** | `1111011w` `mod 011` `r/m` | 2/6 | 2/6 | b | h |
| **AAA = ASCII Adjust for Add** | `00110111` | 4 | 4 | | |
| **AAS = ASCII Adjust for Subtract** | `00111111` | 4 | 4 | | |
| **DAA = Decimal Adjust for Add** | `00100111` | 4 | 4 | | |
| **DAS = Decimal Adjust for Subtract** | `00101111` | 4 | 4 | | |
| **MUL = Multiply (unsigned)** | | | | | |
| Accumulator with Register/Memory | `1111011w` `mod 100` `r/m` | | | | |
| Multiplier-Byte | | 12–17/15–20 | 12–17/15–20 | b, d | d, h |
| -Word | | 12–25/15–28 | 12–25/15–28 | b, d | d, h |
| -Doubleword | | 12–41/15–44 | 12–41/15–44 | b, d | d, h |
| **IMUL = Integer Multiply (signed)** | | | | | |
| Accumulator with Register/Memory | `1111011w` `mod 101` `r/m` | | | | |
| Multiplier-Byte | | 12–17/15–20 | 12–17/15–20 | b, d | d, h |
| -Word | | 12–25/15–28 | 12–25/15–28 | b, d | d, h |
| -Doubleword | | 12–41/15–44 | 12–41/15–44 | b, d | d, h |
| Register with Register/Memory | `00001111` `10101111` `mod reg` `r/m` | | | | |
| Multiplier-Byte | | 12–17/15–20 | 12–17/15–20 | b, d | d, h |
| -Word | | 12–25/15–28 | 12–25/15–28 | b, d | d, h |
| -Doubleword | | 12–41/15–44 | 12–41/15–44 | b, d | d, h |
| Register/Memory with Immediate to Register | `011010s1` `mod reg` `r/m` `immediate data` | | | | |
| -Word | | 13–26/14–27 | 13–26/14–27 | b, d | d, h |
| -Doubleword | | 13–42/14–43 | 13–42/14–43 | b, d | d, h |

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## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|
| | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **ARITHMETIC** (Continued) | | | | | |
| **DIV = Divide (Unsigned)** | | | | | |
| Accumulator by Register/Memory | `1111011w` `mod 110 r/m` | | | | |
| Divisor—Byte | | 14/17 | 14/17 | b,e | e,h |
| —Word | | 22/25 | 22/25 | b,e | e,h |
| —Doubleword | | 38/41 | 38/41 | b,e | e,h |
| **IDIV = Integer Divide (Signed)** | | | | | |
| Accumulator By Register/Memory | `1111011w` `mod 111 r/m` | | | | |
| Divisor—Byte | | 19/22 | 19/22 | b,e | e,h |
| —Word | | 27/30 | 27/30 | b,e | e,h |
| —Doubleword | | 43/46 | 43/46 | b,e | e,h |
| **AAD = ASCII Adjust for Divide** | `11010101` `00001010` | 19 | 19 | | |
| **AAM = ASCII Adjust for Multiply** | `11010100` `00001010` | 17 | 17 | | |
| **CBW = Convert Byte to Word** | `10011000` | 3 | 3 | | |
| **CWD = Convert Word to Double Word** | `10011001` | 2 | 2 | | |
| **LOGIC** | | | | | |
| Shift Rotate Instructions | | | | | |
| Not Through Carry (ROL, ROR, SAL, SAR, SHL, and SHR) | | | | | |
| Register/Memory by 1 | `1101000w` `mod TTT r/m` | 3/7 | 3/7 | b | h |
| Register/Memory by CL | `1101001w` `mod TTT r/m` | 3/7 | 3/7 | b | h |
| Register/Memory by Immediate Count | `1100000w` `mod TTT r/m` immed 8-bit data | 3/7 | 3/7 | b | h |
| Through Carry (RCL and RCR) | | | | | |
| Register/Memory by 1 | `1101000w` `mod TTT r/m` | 9/10 | 9/10 | b | h |
| Register/Memory by CL | `1101001w` `mod TTT r/m` | 9/10 | 9/10 | b | h |
| Register/Memory by Immediate Count | `1100000w` `mod TTT r/m` immed 8-bit data | 9/10 | 9/10 | b | h |

TTT Instruction
000 ROL
001 ROR
010 RCL
011 RCR
100 SHL/SAL
101 SHR
111 SAR

| INSTRUCTION | FORMAT | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|
| **SHLD = Shift Left Double** | | | | | |
| Register/Memory by Immediate | `00001111` `10100100` `mod reg r/m` immed 8-bit data | 3/7 | 3/7 | | |
| Register/Memory by CL | `00001111` `10100101` `mod reg r/m` | 3/7 | 3/7 | | |
| **SHRD = Shift Right Double** | | | | | |
| Register/Memory by Immediate | `00001111` `10101100` `mod reg r/m` immed 8-bit data | 3/7 | 3/7 | | |
| Register/Memory by CL | `00001111` `10101101` `mod reg r/m` | 3/7 | 3/7 | | |
| **AND = And** | | | | | |
| Register to Register | `001000dw` `mod reg r/m` | 2 | 2 | | |

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|---|
| | | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| LOGIC (Continued) | | | | | | |
| Register to Memory | `0 0 1 0 0 0 0 w` `mod reg` `r/m` | | 7 | 7 | b | h |
| Memory to Register | `0 0 1 0 0 0 1 w` `mod reg` `r/m` | | 6 | 6 | b | h |
| Immediate to Register/Memory | `1 0 0 0 0 0 0 w` `mod 1 0 0` `r/m` immediate data | | 2/7 | 2/7 | b | h |
| Immediate to Accumulator (Short Form) | `0 0 1 0 0 1 0 w` immediate data | | 2 | 2 | | |
| TEST = And Function to Flags, No Result | | | | | | |
| Register/Memory and Register | `1 0 0 0 0 1 0 w` `mod reg` `r/m` | | 2/5 | 2/5 | b | h |
| Immediate Data and Register/Memory | `1 1 1 1 0 1 1 w` `mod 0 0 0` `r/m` immediate data | | 2/5 | 2/5 | b | h |
| Immediate Data and Accumulator (Short Form) | `1 0 1 0 1 0 0 w` immediate data | | 2 | 2 | | |
| OR = Or | | | | | | |
| Register to Register | `0 0 0 0 1 0 d w` `mod reg` `r/m` | | 2 | 2 | | |
| Register to Memory | `0 0 0 0 1 0 0 w` `mod reg` `r/m` | | 7 | 7 | b | h |
| Memory to Register | `0 0 0 0 1 0 1 w` `mod reg` `r/m` | | 6 | 6 | b | h |
| Immediate to Register/Memory | `1 0 0 0 0 0 0 w` `mod 0 0 1` `r/m` immediate data | | 2/7 | 2/7 | b | h |
| Immediate to Accumulator (Short Form) | `0 0 0 0 1 1 0 w` immediate data | | 2 | 2 | | |
| XOR = Exclusive Or | | | | | | |
| Register to Register | `0 0 1 1 0 0 d w` `mod reg` `r/m` | | 2 | 2 | | |
| Register to Memory | `0 0 1 1 0 0 0 w` `mod reg` `r/m` | | 7 | 7 | b | h |
| Memory to Register | `0 0 1 1 0 0 1 w` `mod reg` `r/m` | | 6 | 6 | b | h |
| Immediate to Register/Memory | `1 0 0 0 0 0 0 w` `mod 1 1 0` `r/m` immediate data | | 2/7 | 2/7 | b | h |
| Immediate to Accumulator (Short Form) | `0 0 1 1 0 1 0 w` immediate data | | 2 | 2 | | |
| NOT = Invert Register/Memory | `1 1 1 1 0 1 1 w` `mod 0 1 0` `r/m` | | 2/6 | 2/6 | b | h |
| STRING MANIPULATION | | Clk Count Virtual 8086 Mode | | | | |
| CMPS = Compare Byte Word | `1 0 1 0 0 1 1 w` | | 10 | 10 | b | h |
| INS = Input Byte/Word from DX Port | `0 1 1 0 1 1 0 w` | †29 | 15 | 9*/29** | b | h, m |
| LODS = Load Byte/Word to AL/AX/EAX | `1 0 1 0 1 1 0 w` | | 5 | 5 | b | h |
| MOVS = Move Byte Word | `1 0 1 0 0 1 0 w` | | 7 | 7 | b | h |
| OUTS = Output Byte/Word to DX Port | `0 1 1 0 1 1 1 w` | †28 | 14 | 8*/28** | b | h, m |
| SCAS = Scan Byte Word | `1 0 1 0 1 1 1 w` | | 7 | 7 | b | h |
| STOS = Store Byte/Word from AL/AX/EX | `1 0 1 0 1 0 1 w` | | 4 | 4 | b | h |
| XLAT = Translate String | `1 1 0 1 0 1 1 1` | | 5 | 5 | | h |
| REPEATED STRING MANIPULATION Repeated by Count in CX or ECX | | | | | | |
| REPE CMPS = Compare String (Find Non-Match) | `1 1 1 1 0 0 1 1` `1 0 1 0 0 1 1 w` | | 5+9n | 5+9n | b | h |

* If CPL ≤ IOPL    ** If CPL > IOPL

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
|---|---|---|---|---|---|---|---|
| | | | | CLOCK COUNT | | NOTES | |
| **REPEATED STRING MANIPULATION** (Continued) | | | | | | | |
| **REPNE CMPS = Compare String** | | | | Clk Count Virtual 8086 Mode | | | |
| (Find Match) | `11110010` | `1010011w` | | 5+9n | 5+9n | b | h |
| **REP INS = Input String** | `11110010` | `0110110w` | | †27+6n | 13+6n | 7+6n*/27+6n** | b | h, m |
| **REP LODS = Load String** | `11110010` | `1010110w` | | 5+6n | 5+6n | b | h |
| **REP MOVS = Move String** | `11110010` | `1010010w` | | 7+4n | 7+4n | b | h |
| **REP OUTS = Output String** | `11110010` | `0110111w` | | †26+5n | 12+5n | 6+5n*/26+5n** | b | h, m |
| **REPE SCAS = Scan String** | | | | | | | |
| (Find Non-AL/AX/EAX) | `11110011` | `1010111w` | | 5+8n | 5+8n | b | h |
| **REPNE SCAS = Scan String** | | | | | | | |
| (Find AL/AX/EAX) | `11110010` | `1010111w` | | 5+8n | 5+8n | b | h |
| **REP STOS = Store String** | `11110010` | `1010101w` | | 5+5n | 5+5n | b | h |
| **BIT MANIPULATION** | | | | | | | |
| **BSF = Scan Bit Forward** | `00001111` | `10111100` | mod reg r/m | 10+3n | 10+3n | b | h |
| **BSR = Scan Bit Reverse** | `00001111` | `10111101` | mod reg r/m | 10+3n | 10+3n | b | h |
| **BT = Test Bit** | | | | | | | |
| Register/Memory, Immediate | `00001111` | `10111010` | mod 1 0 0 r/m immed 8-bit data | 3/6 | 3/6 | b | h |
| Register/Memory, Register | `00001111` | `10100011` | mod reg r/m | 3/12 | 3/12 | b | h |
| **BTC = Test Bit and Complement** | | | | | | | |
| Register/Memory, Immediate | `00001111` | `10111010` | mod 1 1 1 r/m immed 8-bit data | 6/8 | 6/8 | b | h |
| Register/Memory, Register | `00001111` | `10111011` | mod reg r/m | 6/13 | 6/13 | b | h |
| **BTR = Test Bit and Reset** | | | | | | | |
| Register/Memory, Immediate | `00001111` | `10111010` | mod 1 1 0 r/m immed 8-bit data | 6/8 | 6/8 | b | h |
| Register/Memory Register | `00001111` | `10110011` | mod reg r/m | 6/13 | 6/13 | b | h |
| **BTS = Test Bit and Set** | | | | | | | |
| Register/Memory, Immediate | `00001111` | `10111010` | mod 1 0 1 r/m immed 8-bit data | 6/8 | 6/8 | b | h |
| Register/Memory, Register | `00001111` | `10101011` | mod reg r/m | 6/13 | 6/13 | b | h |
| **CONTROL TRANSFER** | | | | | | | |
| **CALL = Call** | | | | | | | |
| Direct Within Segment | `11101000` | full displacement | | 7+m | 7+m | b | r |
| Register/Memory | | | | | | | |
| Indirect Within Segment | `11111111` | mod 0 1 0 r/m | | 7+m/10+m | 7+m/10+m | b | h, r |
| Direct Intersegment | `10011010` | unsigned full offset, selector | | 17+m | 34+m | b | j,k,r |

**Notes:**
† Clock count shown applies if I/O permission allows I/O to the port in virtual 8086 mode. If I/O bit map denies permission exception 13 fault occurs; refer to clock counts for INT 3 instruction.
\* If CPL ≤ IOPL        \*\* If CPL > IOPL

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|
| | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **CONTROL TRANSFER** (Continued) | | | | | |
| Protected Mode Only (Direct Intersegment) | | | | | |
| Via Call Gate to Same Privilege Level | | | 52 + m | | h,j,k,r |
| Via Call Gate to Different Privilege Level, (No Parameters) | | | 86 + m | | h,j,k,r |
| Via Call Gate to Different Privilege Level, (x Parameters) | | | 94 + 4x + m | | h,j,k,r |
| From 286 Task to 286 TSS | | | 273 | | h,j,k,r |
| From 286 Task to 386 TSS | | | 298 | | h,j,k,r |
| From 286 Task to Virtual 8086 Task (386 TSS) | | | 217 | | h,j,k,r |
| From 386 Task to 286 TSS | | | 273 | | h,j,k,r |
| From 386 Task to 386 TSS | | | 300 | | h,j,k,r |
| From 386 Task to Virtual 8086 Task (386 TSS) | | | 217 | | h,j,k,r |
| Indirect Intersegment | 1 1 1 1 1 1 1 1 \| mod 0 1 1 \| r/m | 22 + m | 38 + m | b | h,j,k,r |
| Protected Mode Only (Indirect Intersegment) | | | | | |
| Via Call Gate to Same Privilege Level | | | 56 + m | | h,j,k,r |
| Via Call Gate to Different Privilege Level, (No Parameters) | | | 90 + m | | h,j,k,r |
| Via Call Gate to Different Privilege Level, (x Parameters) | | | 98 + 4x + m | | h,j,k,r |
| From 286 Task to 286 TSS | | | 278 | | h,j,k,r |
| From 286 Task to 386 TSS | | | 303 | | h,j,k,r |
| From 286 Task to Virtual 8086 Task (386 TSS) | | | 221 | | h,j,k,r |
| From 386 Task to 286 TSS | | | 278 | | h,j,k,r |
| From 386 Task to 386 TSS | | | 305 | | h,j,k,r |
| From 386 Task to Virtual 8086 Task (386 TSS) | | | 221 | | h,j,k,r |
| **JMP = Unconditional Jump** | | | | | |
| Short | 1 1 1 0 1 0 0 1 \| 8-bit displacement | 7 + m | 7 + m | | r |
| Direct within Segment | 1 1 1 0 1 0 0 1 \| full displacement | 7 + m | 7 + m | | r |
| Register/Memory Indirect within Segment | 1 1 1 1 1 1 1 1 \| mod 1 0 0 \| r/m | 7 + m/ 10 + m | 7 + m/ 10 + m | b | h,r |
| Direct Intersegment | 1 1 1 0 1 0 1 0 \| unsigned full offset, selector | 12 + m | 27 + m | | j,k,r |
| Protected Mode Only (Direct Intersegment) | | | | | |
| Via Call Gate to Same Privilege Level | | | 45 + m | | h,j,k,r |
| From 286 Task to 286 TSS | | | 274 | | h,j,k,r |
| From 286 Task to 386 TSS | | | 301 | | h,j,k,r |
| From 286 Task to Virtual 8086 Task (386 TSS) | | | 218 | | h,j,k,r |
| From 386 Task to 286 TSS | | | 270 | | h,j,k,r |
| From 386 Task to 386 TSS | | | 303 | | h,j,k,r |
| From 386 Task to Virtual 8086 Task (386 TSS) | | | 220 | | h,j,k,r |
| Indirect Intersegment | 1 1 1 1 1 1 1 1 \| mod 1 0 1 \| r/m | 17 + m | 31 + m | b | h,j,k,r |
| Protected Mode Only (Indirect Intersegment) | | | | | |
| Via Call Gate to Same Privilege Level | | | 49 + m | | h,j,k,r |
| From 286 Task to 286 TSS | | | 279 | | h,j,k,r |
| From 286 Task to 386 TSS | | | 306 | | h,j,k,r |
| From 286 Task to Virtual 8086 Task (386 TSS) | | | 222 | | h,j,k,r |
| From 386 Task to 286 TSS | | | 275 | | h,j,k,r |
| From 386 Task to 386 TSS | | | 308 | | h,j,k,r |
| From 386 Task to Virtual 8086 Task (386 TSS) | | | 224 | | h,j,k,r |

### Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | | CLOCK COUNT Real Address Mode or Virtual 8086 Mode | CLOCK COUNT Protected Virtual Address Mode | NOTES Real Address Mode or Virtual 8086 Mode | NOTES Protected Virtual Address Mode |
|---|---|---|---|---|---|---|
| **CONTROL TRANSFER** (Continued) | | | | | | |
| **RET = Return from CALL:** | | | | | | |
| Within Segment | `1 1 0 0 0 0 1 1` | | 10 + m | 10 + m | b | g, h, r |
| Within Segment Adding Immediate to SP | `1 1 0 0 0 0 1 0` | 16-bit displ | 10 + m | 10 + m | b | g, h, r |
| Intersegment | `1 1 0 0 1 0 1 1` | | 18 + m | 32 + m | b | g, h, j, k, r |
| Intersegment Adding Immediate to SP | `1 1 0 0 1 0 1 0` | 16-bit displ | 18 + m | 32 + m | b | g, h, j, k, r |
| Protected Mode Only (RET): | | | | | | |
| to Different Privilege Level | | | | | | |
| Intersegment | | | | 68 | | h, j, k, r |
| Intersegment Adding Immediate to SP | | | | 68 | | h, j, k, r |
| **CONDITIONAL JUMPS** | | | | | | |
| NOTE: Times Are Jump "Taken or Not Taken" | | | | | | |
| **JO = Jump on Overflow** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 0 0 0 0` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 0 0 0 0` | full displacement | 7 + m or 3 | 7 + m or 3 | r |
| **JNO = Jump on Not Overflow** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 0 0 0 1` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 0 0 0 1` | full displacement | 7 + m or 3 | 7 + m or 3 | r |
| **JB/JNAE = Jump on Below/Not Above or Equal** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 0 0 1 0` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 0 0 1 0` | full displacement | 7 + m or 3 | 7 + m or 3 | r |
| **JNB/JAE = Jump on Not Below/Above or Equal** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 0 0 1 1` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 0 0 1 1` | full displacement | 7 + m or 3 | 7 + m or 3 | r |
| **JE/JZ = Jump on Equal/Zero** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 0 1 0 0` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 0 1 0 0` | full displacement | 7 + m or 3 | 7 + m or 3 | r |
| **JNE/JNZ = Jump on Not Equal/Not Zero** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 0 1 0 1` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 0 1 0 1` | full displacement | 7 + m or 3 | 7 + m or 3 | r |
| **JBE/JNA = Jump on Below or Equal/Not Above** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 0 1 1 0` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 0 1 1 0` | full displacement | 7 + m or 3 | 7 + m or 3 | r |
| **JNBE/JA = Jump on Not Below or Equal/Above** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 0 1 1 1` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 0 1 1 1` | full displacement | 7 + m or 3 | 7 + m or 3 | r |
| **JS = Jump on Sign** | | | | | | |
| 8-Bit Displacement | `0 1 1 1 1 0 0 0` | 8-bit displ | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | `0 0 0 0 1 1 1 1` | `1 0 0 0 1 0 0 0` | full displacement | 7 + m or 3 | 7 + m or 3 | r |

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | | | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|---|---|
| | | | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **CONDITIONAL JUMPS** (Continued) | | | | | | | |
| **JNS = Jump on Not Sign** | | | | | | | |
| 8-Bit Displacement | 01111001 | 8-bit displ | | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | 00001111 | 10001001 | full displacement | 7 + m or 3 | 7 + m or 3 | | r |
| **JP/JPE = Jump on Parity/Parity Even** | | | | | | | |
| 8-Bit Displacement | 01111010 | 8-bit displ | | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | 00001111 | 10001010 | full displacement | 7 + m or 3 | 7 + m or 3 | | r |
| **JNP/JPO = Jump on Not Parity/Parity Odd** | | | | | | | |
| 8-Bit Displacement | 01111011 | 8-bit displ | | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | 00001111 | 10001011 | full displacement | 7 + m or 3 | 7 + m or 3 | | r |
| **JL/JNGE = Jump on Less/Not Greater or Equal** | | | | | | | |
| 8-Bit Displacement | 01111100 | 8-bit displ | | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | 00001111 | 10001100 | full displacement | 7 + m or 3 | 7 + m or 3 | | r |
| **JNL/JGE = Jump on Not Less/Greater or Equal** | | | | | | | |
| 8-Bit Displacement | 01111101 | 8-bit displ | | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | 00001111 | 10001101 | full displacement | 7 + m or 3 | 7 + m or 3 | | r |
| **JLE/JNG = Jump on Less or Equal/Not Greater** | | | | | | | |
| 8-Bit Displacement | 01111110 | 8-bit displ | | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | 00001111 | 10001110 | full displacement | 7 + m or 3 | 7 + m or 3 | | r |
| **JNLE/JG = Jump on Not Less or Equal/Greater** | | | | | | | |
| 8-Bit Displacement | 01111111 | 8-bit displ | | 7 + m or 3 | 7 + m or 3 | | r |
| Full Displacement | 00001111 | 10001111 | full displacement | 7 + m or 3 | 7 + m or 3 | | r |
| **JCXZ = Jump on CX Zero** | 11100011 | 8-bit displ | | 9 + m or 5 | 9 + m or 5 | | r |
| **JECXZ = Jump on ECX Zero** | 11100011 | 8-bit displ | | 9 + m or 5 | 9 + m or 5 | | r |
| (Address Size Prefix Differentiates JCXZ from JECXZ) | | | | | | | |
| **LOOP = Loop CX Times** | 11100010 | 8-bit displ | | 11 + m | 11 + m | | r |
| **LOOPZ/LOOPE = Loop with Zero/Equal** | 11100001 | 8-bit displ | | 11 + m | 11 + m | | r |
| **LOOPNZ/LOOPNE = Loop While Not Zero** | 11100000 | 8-bit displ | | 11 + m | 11 + m | | r |
| **CONDITIONAL BYTE SET** | | | | | | | |
| NOTE: Times Are Register/Memory | | | | | | | |
| **SETO = Set Byte on Overflow** | | | | | | | |
| To Register/Memory | 00001111 | 10010000 | mod 000 r/m | 4/5 | 4/5 | | h |
| **SETNO = Set Byte on Not Overflow** | | | | | | | |
| To Register/Memory | 00001111 | 10010001 | mod 000 r/m | 4/5 | 4/5 | | h |
| **SETB/SETNAE = Set Byte on Below/Not Above or Equal** | | | | | | | |
| To Register/Memory | 00001111 | 10010010 | mod 000 r/m | 4/5 | 4/5 | | h |

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | | | | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|---|---|---|
| | | | | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| CONDITIONAL BYTE SET (Continued) | | | | | | | | . |
| SETNB = Set Byte on Not Below/Above or Equal | | | | | | | | |
| To Register/Memory | 00001111 | 10010011 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETE/SETZ = Set Byte on Equal/Zero | | | | | | | | |
| To Register/Memory | 00001111 | 10010100 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETNE/SETNZ = Set Byte on Not Equal/Not Zero | | | | | | | | |
| To Register/Memory | 00001111 | 10010101 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETBE/SETNA = Set Byte on Below or Equal/Not Above | | | | | | | | |
| To Register/Memory | 00001111 | 10010110 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETNBE/SETA = Set Byte on Not Below or Equal/Above | | | | | | | | |
| To Register/Memory | 00001111 | 10010111 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETS = Set Byte on Sign | | | | | | | | |
| To Register/Memory | 00001111 | 10011000 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETNS = Set Byte on Not Sign | | | | | | | | |
| To Register/Memory | 00001111 | 10011001 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETP/SETPE = Set Byte on Parity/Parity Even | | | | | | | | |
| To Register/Memory | 00001111 | 10011010 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETNP/SETPO = Set Byte on Not Parity/Parity Odd | | | | | | | | |
| To Register/Memory | 00001111 | 10011011 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETL/SETNGE = Set Byte on Less/Not Greater or Equal | | | | | | | | |
| To Register/Memory | 00001111 | 10011100 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETNL/SETGE = Set Byte on Not Less/Greater or Equal | | | | | | | | |
| To Register/Memory | 00001111 | 01111101 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETLE/SETNG = Set Byte on Less or Equal/Not Greater | | | | | | | | |
| To Register/Memory | 00001111 | 10011110 | mod 000 | r/m | 4/5 | 4/5 | | h |
| SETNLE/SETG = Set Byte on Not Less or Equal/Greater | | | | | | | | |
| To Register/Memory | 00001111 | 10011111 | mod 000 | r/m | 4/5 | 4/5 | | h |
| ENTER = Enter Procedure | 11001000 | 16-bit displacement, 8-bit level | | | | | | |
| L = 0 | | | | | 10 | 10 | b | h |
| L = 1 | | | | | 12 | 12 | b | h |
| L > 1 | | | | | 15 + 4(n − 1) | 15 + 4(n − 1) | b | h |
| LEAVE = Leave Procedure | 11001001 | | | | 4 | 4 | b | h |

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## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| | | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|
| INSTRUCTION | FORMAT | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **INTERRUPT INSTRUCTIONS** | | | | | |
| INT = Interrupt: | | | | | |
| Type Specified | `11001101` `type` | 37 | | b | |
| Type 3 | `11001100` | 33 | . | b | |
| INTO = Interrupt 4 if Overflow Flag Set | `11001110` | | | | |
| If OF = 1 | | 35 | | b, e | |
| If OF = 0 | | 3 | 3 | b, e | |
| Bound = Interrupt 5 if Detect Value Out of Range | `01100010` `mod reg  r/m` | | | | |
| If Out of Range | | 44 | | b, e | e, g, h, j, k, r |
| If In Range | | 10 | 10 | b, e | e, g, h, j, k, r |
| **Protected Mode Only (INT)** | | | | | |
| INT: Type Specified | | | | | |
| Via Interrupt or Trap Gate | | | . | | |
| to Same Privilege Level | · | | 59 | | g, j, k, r |
| Via Interrupt or Trap Gate | | | | | |
| to Different Privilege Level | | | 99 | | g, j, k, r  , |
| From 286 Task to 286 TSS via Task Gate | | | 282 | | g, j, k, r |
| From 286 Task to 386 TSS via Task Gate | | | 309 | | g, j, k, r |
| From 286 Task to virt 8086 md via Task Gate | | | 226 | | g, j, k, r |
| From 386 Task to 286 TSS via Task Gate | | | 284 | | g, j, k, r |
| From 386 Task to 386 TSS via Task Gate | | | 311 | | g, j, k, r |
| From 386 Task to virt 8086 md via Task Gate | | | 228 | | g, j, k, r |
| From virt 8086 md to 286 TSS via Task Gate | | | 289 | | g, j, k, r |
| From virt 8086 md to 386 TSS via Task Gate | | | 316 | | g, j, k, r |
| From virt 8086 md to priv level 0 via Trap Gate or Interrupt Gate | | | 119 | | |
| **INT: TYPE 3** | | | | | |
| Via Interrupt or Trap Gate | | | | | |
| to Same Privilege Level | | | 59 | | g, j, k, r |
| Via Interrupt or Trap Gate | | | | | |
| to Different Privilege Level | | | 99 | | g, j, k, r |
| From 286 Task to 286 TSS via Task Gate | | | 278 | | g, j, k, r |
| From 286 Task to 386 TSS via Task Gate | | | 305 | | g, j, k, r |
| From 286 Task to Virt 8086 md via Task Gate | | | 222 | | g, j, k, r |
| From 386 Task to 286 TSS via Task Gate | | | 280 | | g, j, k, r |
| From 386 Task to 386 TSS via Task Gate | | | 307 | | g, j, k, r |
| From 386 Task to Virt 8086 md via Task Gate | | | 224 | | g, j, k, r |
| From virt 8086 md to 286 TSS via Task Gate | | | 285 | | g, j, k, r |
| From virt 8086 md to 386 TSS via Task Gate | | | 312 | | g, j, k, r |
| From virt 8086 md to priv level 0 via Trap Gate or Interrupt Gate | | | 119 | | |
| **INTO:** | | | | | |
| Via Interrupt or Trap Grate | | | | | |
| to Same Privilege Level | | | 59 | | g, j, k, r |
| Via Interrupt or Trap Gate | | | | | |
| to Different Privilege Level | | | 99 | | g, j, k, r |
| From 286 Task to 286 TSS via Task Gate | | | 280 | | g, j, k, r |
| From 286 Task to 386 TSS via Task Gate | | | 307 | | g, j, k, r |
| From 286 Task to virt 8086 md via Task Gate | | | 224 | | g, j, k, r |
| From 386 Task to 286 TSS via Task Gate | | | 282 | | g, j, k, r |
| From 386 Task to 386 TSS via Task Gate | | | 309 | | g, j, k, r |
| From 386 Task to virt 8086 md via Task Gate | | * 225 | | g, j, k, r | |
| From virt 8086 md to 286 TSS via Task Gate | | | 287 | | g, j, k, r |
| From virt 8086 md to 386 TSS via Task Gate | | | 314 | | g, j, k, r |
| From virt 8086 md to priv level 0 via Trap Gate or Interrupt Gate | | | 119 | | |

### Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | | | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|---|---|
| | | | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **INTERRUPT INSTRUCTIONS** (Continued) | | | | | | | |
| **BOUND:** | | | | | | | |
| Via Interrupt or Trap Gate to Same Privilege Level | | | | | 59 | | g, j, k, r |
| Via Interrupt or Trap Gate to Different Privilege Level | | | | | 99 | | g, j, k, r |
| From 286 Task to 286 TSS via Task Gate | | | | | 254 | | g, j, k, r |
| From 286 Task to 386 TSS via Task Gate | | | | | 284 | | g, j, k, r |
| From 268 Task to virt 8086 Mode via Task Gate | | | | | 231 | | g, j, k, r |
| From 386 Task to 286 TSS via Task Gate | | | | | 264 | | g, j, k, r |
| From 386 Task to 386 TSS via Task Gate | | | | | 294 | | g, j, k, r |
| From 368 Task to virt 8086 Mode via Task Gate | | | | | 243 | | g, j, k, r, |
| From virt 8086 Mode to 286 TSS via Task Gate | | | | | 264 | | g, j, k, r |
| From virt 8086 Mode to 386 TSS via Task Gate | | | | | 294 | | g, j, k, r |
| From virt 8086 md to priv level 0 via Trap Gate or Interrupt Gate | | | | | 119 | | |
| **INTERRUPT RETURN** | | | | | | | |
| IRET = Interrupt Return | 11001111 | | | 22 | | g, h, j, k, r | |
| Protected Mode Only (IRET) | | | | | | | |
| To the Same Privilege Level (within task) | | | | | 38 | | g, h, j, k, r |
| To Different Privilege Level (within task) | | | | | 82 | | g, h, j, k, r |
| From 286 Task to 286 TSS | | | | | 232 | | h, j, k, r |
| From 286 Task to 386 TSS | | | | | 265 | | h, j, k, r |
| From 286 Task to Virtual 8086 Task | | | | | 214 | | h, j, k, r |
| From 286 Task to Virtual 8086 Mode (within task) | | | | | 60 | | |
| From 386 Task to 286 TSS | | | | | 271 | | h, j, k, r |
| From 386 Task to 386 TSS | | | | | 275 | | h, j, k, r |
| From 386 Task to Virtual 8086 Task | | | | | 224 | | h, j, k, r |
| From 386 Task to Virtual 8086 Mode (within task) | | | | | 60 | | |
| **PROCESSOR CONTROL** | | | | | | | |
| HLT = HALT | 11110100 | | | 5 | 5 | | l |
| MOV = Move to and From Control/Debug/Test Registers | | | | | | | |
| CR0/CR2/CR3 from register | 00001111 | 00100010 | 11 eee reg | 10/4/5 | 10/4/5 | | l |
| Register From CR0-3 | 00001111 | 00100000 | 11 eee reg | 6 | 6 | | l |
| DR0-3 From Register | 00001111 | 00100011 | 11 eee reg | 22 | 22 | | l |
| DR6-7 From Register | 00001111 | 00100011 | 11 eee reg | 16 | 16 | | l |
| Register from DR6-7 | 00001111 | 00100001 | 11 eee reg | 14 | 14 | | l |
| Register from DR0-3 | 00001111 | 00100001 | 11 eee reg | 22 | 22 | | l |
| TR6-7 from Register | 00001111 | 00100110 | 11 eee reg | 12 | 12 | | l |
| Register from TR6-7 | 00001111 | 00100100 | 11 eee reg | 12 | 12 | | l |
| NOP = No Operation | 10010000 | | | 3 | 3 | | |
| WAIT = Wait until BUSY # pin is negated | 10011011 | | | 6 | 6 | | |

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|
| | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **PROCESSOR EXTENSION INSTRUCTIONS** | | | | | |
| Processor Extension Escape | `11011TTT` `mod LLL r/m` TTT and LLL bits are opcode information for coprocessor. | See 80287/80387 data sheets for clock counts | | | h |
| **PREFIX BYTES** | | | | | |
| Address Size Prefix | `01100111` | 0 | 0 | | |
| LOCK = Bus Lock Prefix | `11110000` | 0 | 0 | | m |
| Operand Size Prefix | `01100110` | 0 | 0 | | |
| **Segment Override Prefix** | | | | | |
| CS: | `00101110` | 0 | 0 | | |
| DS: | `00111110` | 0 | 0 | | |
| ES: | `00100110` | 0 | 0 | | |
| FS: | `01100100` | 0 | 0 | | |
| GS: | `01100101` | 0 | 0 | | |
| SS: | `00110110` | 0 | 0 | | |
| **PROTECTION CONTROL** | | | | | |
| ARPL = Adjust Requested Privilege Level | | | | | |
| From Register/Memory | `01100011` `mod reg r/m` | N/A | 20/21 | a | h |
| LAR = Load Access Rights | | | | | |
| From Register/Memory | `00001111` `00000010` `mod reg r/m` | N/A | 15/16 | a | g, h, j, p |
| LGDT = Load Global Descriptor | | | | | |
| Table Register | `00001111` `00000001` `mod 010 r/m` | 11 | 11 | b, c | h, l |
| LIDT = Load Interrupt Descriptor | | | | | |
| Table Register | `00001111` `00000001` `mod 011 r/m` | 11 | 11 | b, c | h, l |
| LLDT = Load Local Descriptor | | | | | |
| Table Register to Register/Memory | `00001111` `00000000` `mod 010 r/m` | N/A | 20/24 | a | g, h, j, l |
| LMSW = Load Machine Status Word | | | | | |
| From Register/Memory | `00001111` `00000001` `mod 110 r/m` | 10/13 | 10/13 | b, c | h, l |
| LSL = Load Segment Limit | | | | | |
| From Register/Memory | `00001111` `00000011` `mod reg r/m` | | | | |
| Byte-Granular Limit | | N/A | 20/21 | a | g, h, j, p |
| Page-Granular Limit | | N/A | 25/26 | a | g, h, j, p |
| LTR = Load Task Register | | | | | |
| From Register/Memory | `00001111` `00000000` `mod 001 r/m` | N/A | 23/27 | a | g, h, j, l |
| SGDT = Store Global Descriptor | | | | | |
| Table Register | `00001111` `00000001` `mod 000 r/m` | 9 | 9 | b, c | h |
| SIDT = Store Interrupt Descriptor | | | | | |
| Table Register | `00001111` `00000001` `mod 001 r/m` | 9 | 9 | b, c | h |
| SLDT = Store Local Descriptor Table Register | | | | | |
| To Register/Memory | `00001111` `00000000` `mod 000 r/m` | N/A | 2/2 | a | h |

## Table 8-1. 80386 Instruction Set Clock Count Summary (Continued)

| INSTRUCTION | FORMAT | | | CLOCK COUNT | | NOTES | |
|---|---|---|---|---|---|---|---|
| | | | | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode | Real Address Mode or Virtual 8086 Mode | Protected Virtual Address Mode |
| **SMSW** = Store Machine Status Word | `00001111` | `00000001` | `mod 1 0 0  r/m` | 2/2 | 2/2 | b, c | h, l |
| **STR** = Store Task Register To Register/Memory | `00001111` | `00000000` | `mod 0 0 1  r/m` | N/A | 2/2 | a | h |
| **VERR** = Verify Read Access Register/Memory | `00001111` | `00000000` | `mod 1 0 0  r/m` | N/A | 10/11 | a | g, h, j, p |
| **VERW** = Verify Write Access | `00001111` | `00000000` | `mod 1 0 1  r/m` | N/A | 15/16 | a | g, h, j, p |

### INSTRUCTION NOTES FOR TABLE 8-1

**Notes a through c apply to 80386 Real Address Mode only:**
a. This is a Protected Mode instruction. Attempted execution in Real Mode will result in exception 6 (invalid opcode).
b. Exception 13 fault (general protection) will occur in Real Mode if an operand reference is made that partially or fully extends beyond the maximum CS, DS, ES, FS or GS limit, FFFFH. Exception 12 fault (stack segment limit violation or not present) will occur in Real Mode if an operand reference is made that partially or fully extends beyond the maximum SS limit.
c. This instruction may be executed in Real Mode. In Real Mode, its purpose is primarily to initialize the CPU for Protected Mode.

**Notes d through g apply to 80386 Real Address Mode and 80386 Protected Virtual Address Mode:**
d. The 80386 uses an early-out multiply algorithm. The actual number of clocks depends on the position of the most significant bit in the operand (multiplier).
  Clock counts given are minimum to maximum. To calculate actual clocks use the following formula:
  Actual Clock = if m < > 0 then max ($[\log_2 |m|]$, 3) + b clocks:
     if m = 0 then 3 + b clocks
  In this formula, m is the multiplier, and
  b = 9 for register to register,
  b = 12 for memory to register,
  b = 10 for register with immediate to register,
  b = 11 for memory with immediate to register.
e. An exception may occur, depending on the value of the operand.
f. LOCK# is automatically asserted, regardless of the presence or absence of the LOCK# prefix.
g. LOCK# is asserted during descriptor table accesses.

**Notes h through r apply to 80386 Protected Virtual Address Mode only:**
h. Exception 13 fault (general protection violation) will occur if the memory operand in CS, DS, ES, FS or GS cannot be used due to either a segment limit violation or access rights violation. If a stack limit is violated, an exception 12 (stack segment limit violation or not present) occurs.
i. For segment load operations, the CPL, RPL, and DPL must agree with the privilege rules to avoid an exception 13 fault (general protection violation). The segment's descriptor must indicate "present" or exception 11 (CS, DS, ES, FS, GS not present). If the SS register is loaded and a stack segment not present is detected, an exception 12 (stack segment limit violation or not present) occurs.
j. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert LOCK# to maintain descriptor integrity in multiprocessor systems.
k. JMP, CALL, INT, RET and IRET instructions referring to another code segment will cause an exception 13 (general protection violation) if an applicable privilege rule is violated.
l. An exception 13 fault occurs if CPL is greater than 0 (0 is the most privileged level).
m. An exception 13 fault occurs if CPL is greater than IOPL.
n. The IF bit of the flag register is not updated if CPL is greater than IOPL. The IOPL and VM fields of the flag register are updated only if CPL = 0.
o. The PE bit of the MSW (CR0) cannot be reset by this instruction. Use MOV into CR0 if desiring to reset the PE bit.
p. Any violation of privilege rules as applied to the selector operand does not cause a protection exception; rather, the zero flag is cleared.
q. If the coprocessor's memory operand violates a segment limit or segment access rights, an exception 13 fault (general protection exception) will occur before the ESC instruction is executed. An exception 12 fault (stack segment limit violation or not present) will occur if the stack limit is violated by the operand's starting address.
r. The destination of a JMP, CALL, INT, RET or IRET must be in the defined limit of a code segment or an exception 13 fault (general protection violation) will occur.

# 80387
## 80-BIT CHMOS III
## NUMERIC PROCESSOR EXTENSION

- **High Performance 80-Bit Internal Architecture**
- **Implements ANSI/IEEE Standard 754-1985 for Binary Floating-Point Arithmetic**
- **Five to Seven Times 8087/80287 Performance**
- **Upward Object-Code Compatible from 8087 and 80287**
- **Expands 80386 Data Types to Include 32-, 64-, 80-Bit Floating Point, 32-, 64-Bit Integers and 18-Digit BCD Operands**
- **Directly Extends 80386 Instruction Set to Include Trigonometric, Logarithmic, Exponential and Arithmetic Instructions for All Data Types**

- **Full-Range Transcendental Operations for SINE, COSINE, TANGENT, ARCTANGENT and LOGARITHM**
- **Built-In Exception Handling**
- **Operates Independently of Real, Protected and Virtual-8086 Modes of the 80386**
- **Eight 80-Bit Numeric Registers, Usable as Individually Addressable General Registers or as a Register Stack**
- **Available in 68-Pin PGA Package**
(See Packaging Spec: Order #231369)

The Intel 80387 is a high-performance numerics processor extension that extends the 80386 architecture with floating point, extended integer and BCD data types. The 80386/80387 computing system fully conforms to the ANSI/IEEE floating-point standard. Using a numerics oriented architecture, the 80387 adds over seventy mnemonics to the 80386/80387 instruction set, making the 80386/80387 a complete solution for high-performance numerics processing. The 80387 is implemented with 1.5 micron, high-speed CHMOS III technology and packaged in a 68-pin ceramic pin grid array (PGA) package. The 80386/80387 is upward object-code compatible from the 80386/80287, 80286/80287 and 8086/8087 computing systems.



**Figure 0.1. 80387 Block Diagram**

231920–1

## Figure 1.1. 80386/80387 Register Set



## 1.0 FUNCTIONAL DESCRIPTION

The 80387 Numeric Processor Extension (NPX) provides arithmetic instructions for a variety of numeric data types in 80386/80387 systems. It also executes numerous built-in transcendental functions (e.g. tangent, sine, cosine, and log functions). The 80387 effectively extends the register and instruction set of an 80386 system for existing data types and adds several new data types as well. Figure 1.1 shows the model of registers visible to 80386/80387 programs. Essentially, the 80387 can be treated as an additional resource or an extension to the 80386. The 80386 together with an 80387 can be used as a single unified system, the 80386/80387.

The 80387 works the same whether the 80386 is executing in real-address mode, protected mode, or virtual-8086 mode. All memory access is handled by the 80386; the 80387 merely operates on instructions and values passed to it by the 80386. Therefore, the 80387 is not sensitive to the processing mode of the 80386.

In real-address mode and virtual-8086 mode, the 80386/80387 is completely upward compatible with software for 8086/8087, 80286/80287 real-address mode, and 80386/80287 real-address mode systems.

In protected mode, the 80386/80387 is completely upward compatible with software for 80286/80287 protected mode, and 80386/80287 protected mode systems.

The only differences of operation that may appear when 8086/8087 programs are ported to a protected-mode 80386/80387 system (*not* using virtual-8086 mode), is in the format of operands for the administrative instructions FLDENV, FSTENV, FRSTOR and FSAVE. These instructions are normally used only by exception handlers and operating systems, not by applications programs.

The 80387 contains three functional units that can operate in parallel to increase system performance. The 80386 can be transferring commands and data to the 80387 *bus control logic* for the next instruction while the 80387 *floating-point unit* is performing the current numeric instruction.

# 82380
# HIGH PERFORMANCE 32-BIT DMA CONTROLLER WITH INTEGRATED SYSTEM SUPPORT PERIPHERALS

- **High Performance 32-Bit DMA Controller**
  - **40 MBytes/sec Maximum Data Transfer Rate at 20 MHz**
  - **8 Independently Programmable Channels**
- **20-Source Interrupt Controller**
  - **Individually Programmable Interrupt Vectors**
  - **15 External, 5 Internal Interrupts**
  - **82C59A Superset**
- **Four 16-Bit Programmable Interval Timers**
  - **82C54 Compatible**

- **Programmable Wait State Generator**
  - **0 to 15 Wait States**
- **DRAM Refresh Controller**
- **80386 Shutdown Detect and Reset Control**
  - **Software/Hardware Reset**
- **IBM PC Compatible\***
- **High Speed CHMOS III Technology**
- **132-Pin PGA Package**
- **Optimized for use with the 80386 Microprocessor**
  - **Resides on Local Bus for Maximum Bus Bandwidth**

The 82380 is a multi-function support peripheral that integrates system functions necessary in an 80386 environment. It has eight channels of high performance 32-bit DMA with the most efficient transfer rates possible on the 80386 bus. System support peripherals integrated into the 82380 provide Interrupt Control, Timers, Wait State generation, DRAM Refresh Control, and System Reset logic.

The 82380's DMA Controller can transfer data between devices of different data path widths using a single channel. Each DMA channel operates independently in any of several modes. Each channel has a temporary data storage register for handling non-aligned data without the need for external alignment logic.

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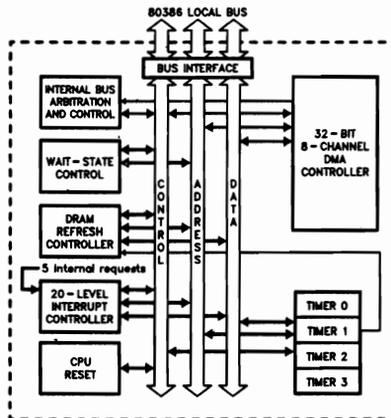


**82380 Internal Block Diagram**

290128-1

## 12.2 Pin Assignment

The 82380 pinout as viewed from the top side of the component is shown in Figure 12.1. Its pinout as viewed from the pin side of the component is shown in Figure 12.2.

$V_{CC}$ and GND connections must be made to multiple $V_{CC}$ and $V_{SS}$ (GND) pins. Each $V_{CC}$ and $V_{SS}$ MUST be connected to the appropriate voltage level. The circuit board should include $V_{CC}$ and GND planes for power distribution and all $V_{CC}$ pins must be connected to the appropriate plane.

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 01 | $V_{SS}$ | $V_{CC}$ | $V_{SS}$ | $V_{CC}$ | A12 | A9 | A8 | A5 | A3 | BE1# | BE0# | EDACK1 | $V_{SS}$ | $V_{CC}$ | 01 |
| 02 | $V_{CC}$ | A19 | A17 | A15 | A13 | A10 | A7 | A4 | BE3# | ADS# | EDACK2 | INT | $V_{SS}$ | $V_{CC}$ | 02 |
| 03 | $V_{SS}$ | A21 | A18 | A16 | A14 | A11 | A6 | A2 | BE2# | EOP# | EDACK0 | HLDA | DREQ7 | DREQ5 | 03 |
| 04 | $V_{CC}$ | A22 | A20 | | | | | | | | | DREQ6 | NA# | DREQ3 | 04 |
| 05 | A25 | A24 | A23 | | | METAL LID | | | | | | DREQ4/IRQ9# | DREQ2 | DREQ1 | 05 |
| 06 | A28 | A27 | A26 | | | | | | | | | DREQ0 | IRQ22# | IRQ23# | 06 |
| 07 | A31 | A29 | A30 | | | | | | | | | IRQ21# | IRQ20# | IRQ19# | 07 |
| 08 | D31 | D23 | D15 | | | | | | | | | IRQ17# | IRQ16# | IRQ18# | 08 |
| 09 | D7 | D30 | D22 | | | | | | | | | IRQ13# | IRQ14# | IRQ15# | 09 |
| 10 | D14 | D6 | D13 | | | | | | | | | WSC1 | IRQ12# | IRQ11# | 10 |
| 11 | D29 | D21 | D28 | | | | | | | | | READY# | CLKIN | WSC0 | 11 |
| 12 | $V_{CC}$ | D5 | D12 | D27 | D3 | D10 | D17 | READYO# | HOLD | W/R# | D/C# | CPURST | RESET | $V_{CC}$ | 12 |
| 13 | $V_{SS}$ | D20 | D4 | D19 | D26 | D2 | D9 | D16 | D24 | TOUT1/REF# | M/IO# | TOUT3# | TOUT2#/IRQ3# | $V_{SS}$ | 13 |
| 14 | $V_{CC}$ | $V_{SS}$ | $V_{CC}$ | D11 | D18 | D25 | CLK2 | D1 | D0 | D8 | $V_{SS}$ | $V_{CC}$ | $V_{SS}$ | $V_{CC}$ | 14 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | |

290128-95

**Figure 12.2. 82380 PGA Pinout—View from PIN side**

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### Table 12-1. 82380 PGA Pinout—Functional Grouping

| Pin/Signal | | Pin/Signal | | Pin/Signal | | Pin/Signal | |
|---|---|---|---|---|---|---|---|
| A7 | A31 | A8 | D31 | P12 | Vcc | L14 | Vss |
| C7 | A30 | B9 | D30 | M14 | Vcc | A1 | Vss |
| B7 | A29 | A11 | D29 | P1 | Vcc | P13 | Vss |
| A6 | A28 | C11 | D28 | P2 | Vcc | N1 | Vss |
| B6 | A27 | D12 | D27 | P14 | Vcc | N2 | Vss |
| C6 | A26 | E13 | D26 | D1 | Vcc | C1 | Vss |
| A5 | A25 | F14 | D25 | C14 | Vcc | A3 | Vss |
| B5 | A24 | J13 | D24 | B1 | Vcc | B14 | Vss |
| C5 | A23 | B8 | D23 | A2 | Vcc | A13 | Vss |
| B4 | A22 | C9 | D22 | A4 | Vcc | N14 | Vss |
| B3 | A21 | B11 | D21 | A12 | Vcc | | |
| C4 | A20 | B13 | D20 | A14 | Vcc | P6 | IRQ23# |
| B2 | A19 | D13 | D19 | | | N6 | IRQ22# |
| C3 | A18 | E14 | D18 | G14 | CLK2 | M7 | IRQ21# |
| C2 | A17 | G12 | D17 | L12 | D/C# | N7 | IRQ20# |
| D3 | A16 | H13 | D16 | K12 | W/R# | P7 | IRQ19# |
| D2 | A15 | C8 | D15 | L13 | M/IO# | P8 | IRQ18# |
| E3 | A14 | A10 | D14 | K2 | ADS# | M8 | IRQ17# |
| E2 | A13 | C10 | D13 | N4 | NA# | N8 | IRQ16# |
| E1 | A12 | A12 | D12 | J12 | HOLD | P9 | IRQ15# |
| F3 | A11 | D14 | D11 | M3 | HLDA | N9 | IRQ14# |
| F2 | A10 | F12 | D10 | M6 | DREQ0 | M9 | IRQ13# |
| F1 | A9 | G13 | D9 | P5 | DREQ1 | N10 | IRQ12# |
| G1 | A8 | K14 | D8 | N5 | DREQ2 | P10 | IRQ11# |
| G2 | A7 | A9 | D7 | P4 | DREQ3 | M2 | INT |
| G3 | A6 | B10 | D6 | M5 | DREQ4/IRQ9# | | |
| H1 | A5 | B12 | D5 | P3 | DREQ5 | N11 | CLKIN |
| H2 | A4 | C13 | D4 | M4 | DREQ6 | K13 | TOUT1/REF# |
| J1 | A3 | E12 | D3 | N3 | DREQ7 | N13 | TOUT2#/IRQ3# |
| H3 | A2 | F13 | D2 | | | M13 | TOUT3# |
| J2 | BE3# | H14 | D1 | K3 | EOP# | M11 | READY# |
| J3 | BE2# | J14 | D0 | L3 | EDACK0 | H12 | READYO# |
| K1 | BE1# | | | M1 | EDACK1 | P11 | WSC0 |
| L1 | BE0# | N12 | RESET | L2 | EDACK2 | M10 | WSC1 |
| | | M12 | CPURST | | | | |

# 82385
# HIGH PERFORMANCE
# 32-BIT CACHE CONTROLLER

- **Improves 80386 System Performance**
  - **Reduces Average CPU Wait States to Nearly Zero**
  - **Zero Wait State Read Hit**
  - **Zero Wait State Posted Writes**
  - **Allows Other Masters to Access the System Bus More Readily**

- **Hit Rates up to 99%**

- **Optimized as 80386 Companion**
  - **Simple 80386 Interface**
  - **Part of 386-Based Compute Engine Including 80387 Numerics Coprocessor and 82380 Integrated System Peripheral**
  - **16 MHz and 20 MHz Operation**

- **Software Transparent**

- **Synchronous Dual Bus Architecture**
  - **Bus Watching Maintains Cache Coherency**

- **Maps Full 80386 Address Space (4 Gigabytes)**

- **Flexible Cache Mapping Policies**
  - **Direct Mapped or 2-Way Set Associative Cache Organization**
  - **Supports Non-Cacheable Memory Space**
  - **Unified Cache for Code and Data**

- **Integrates Cache Directory and Cache Management Logic**

- **High Speed CHMOS III Technology**

- **132-Pin PGA Package**

The 82385 Cache Controller is a high performance 32-bit peripheral for Intel's 80386 Microprocessor. It stores a copy of frequently accessed code and data from main memory in a zero wait state local cache memory. The 82385 enables the 80386 to run at its full potential by reducing the average number of CPU wait states to nearly zero. The dual bus architecture of the 82385 allows other masters to access system resources while the 80386 operates locally out of its cache. In this situation, the 82385's "bus watching" mechanism preserves cache coherency by monitoring the system bus address lines at no cost to system or local throughput.

The 82385 is completely software transparent, protecting the integrity of system software. High performance and board savings are achieved because the 82385 integrates a cache directory and all cache management logic on one chip.
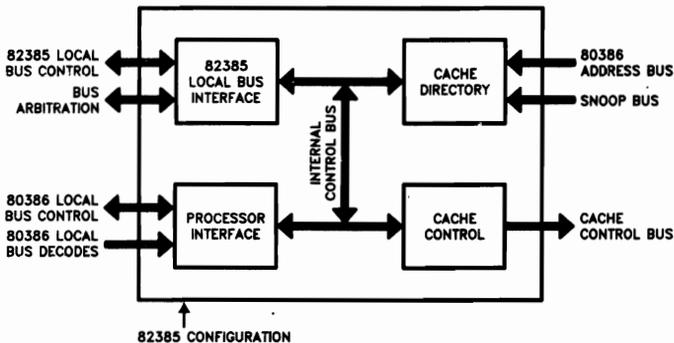


290143-1

**82385 Internal Block Diagram**

# 1.0 82385 FUNCTIONAL OVERVIEW

The 82385 Cache Controller is a high performance 32-bit peripheral for Intel's 80386 microprocessor. This chapter provides an overview of the 82385, and of the basic architecture and operation of an 80386/82385 system.

## 1.1 82385 OVERVIEW

The main function of a cache memory system is to provide fast local storage for frequently accessed code and data. The cache system intercepts 80386 memory references to see if the required data resides in the cache. If the data resides in the cache (a hit), it is returned to the 80386 without incurring wait states. If the data is not cached (a miss), the reference is forwarded to the system and the data retrieved from main memory. An efficient cache will yield a high "hit rate" (the ratio of cache hits to total 80386 accesses), such that the majority of accesses are serviced with zero wait states. The net effect is that the wait states incurred in a relatively infrequent miss are averaged over a large number of accesses, resulting in an average of nearly zero wait states per access. Since cache hits are serviced locally, a processor operating out of its local cache has a much lower "bus utilization" which reduces system bus bandwidth requirements, making more bandwidth available to other bus masters.

The 82385 Cache Controller integrates a cache directory and all cache management logic required to support an external 32 Kbyte cache. The cache directory structure is such that the entire physical address range of the 80386 (4 Gigabytes) is mapped into the cache. Provision is made to allow areas of memory to be set aside a non-cacheable. The user has two cache organization options: direct mapped and 2-way set associative. Both provide the high hit rates necessary to make a large, relatively slow main memory array look like a fast, zero wait state memory to the 80386.

A good hit rate is an essential ingredient of a successful cache implementation. Hit rate is the measure of how efficient a cache is in maintaining a copy of the most frequently requested code and data. However, efficiency is not the only factor for performance consideration. Just as essential are sound cache management policies. These policies refer to the handling of 80386 writes, preservation of cache coherency, and ease of system design. The 82385's "posted write" capability allows the majority of 80386 writes, including non-cacheable and I/O writes, to run with zero wait states, and the 82385's "bus watching" mechanism preserves cache coherency with no impact on system performance. Physically, the 82385 ties directly to the 80386 with virtually no external logic.

## 1.2 SYSTEM OVERVIEW I: BUS STRUCTURE

A good grasp of the bus structure of an 80386/82385 system is essential in understanding both the 82385 and its role in an 80386 system. The following is a description of this structure.



**Figure 1-1. 80386 System Bus Structure**

## 1.2.1 80386 Local Bus/82385 Local Bus/System Bus

Figure 1-1 depicts the bus structure of a typical 80386 system. The "80386 Local Bus" consists of the physical 80386 address, data, and control busses. The local address and data busses are buffered and/or latched to become the "system" address and data busses. The local control bus is decoded by bus control logic to generate the various system bus read and write commands.

The addition of an 82385 Cache Controller causes a separation of the 80386 bus into two distinct busses: the actual 80386 local bus and the "82385 Local Bus" (Figure 1-2). The 82385 local bus is designed to look like the front end of an 80386 by providing 82385 local bus equivalents to all appropriate 80386 signals. The system ties to this "80386-like" front end just as it would to an actual 80386. The 80386 simply sees a fast system bus, and the system sees an 80386 front end with low bus bandwidth requirements. The cache subsystem is transparent to both. Note that the 82385 local bus is not simply a buffered version of the 80386 bus, but rather is distinct from, and able to operate in parallel with the 80386 bus. Other masters residing on either the 82385 local bus or system bus are free to manage system resources while the 80386 operates out of its cache.

## 1.2.2 Bus Arbitration

The 82385 presents the "80386-like" interface which is called the 82385 local bus. Whereas the 80386 provides a Hold Request/Hold Acknowledge bus arbitration mechanism via its HOLD and HLDA pins, the 82385 provides an equivalent mechanism via its BHOLD and BHLDA pins. (These signals are described in section 3.7.) When another master requests the 82385 local bus, it issues the request to the 82385 via BHOLD. Typically, at the end of the current 82385 local bus cycle, the 82385 will release the 82385 local bus and acknowledge the request via BHLDA. The 80386 is of course free to continue operating on the 80386 local bus while another master owns the 82385 local bus.

## 1.2.3 Master/Slave Operation

The above 82385 local bus arbitration discussion is strictly true only when the 82385 is programmed for "Master" mode operation. The user can, however, configure the 82385 for "Slave" mode operation. (Programming is done via a hardware strap option.) The roles of BHOLD and BHLDA are reversed for an 82385 in slave mode; BHOLD is now an output indicating a request to control the bus, and BHLDA is an input indicating that a request has been granted. An 82385 programmed in slave mode drives the 82385 local bus only when it has requested and subsequently been granted bus control. This allows multiple 80386/82385 subsystems to reside on the same 82385 local bus (Figure 1-3).



**Figure 1-2. 80386/82385 System Bus Structure**

**Figure 1-3. Multi-Master/Multi-Cache Environment**

## 1.2.4 Cache Coherency

Ideally, a cache contains a copy of the most heavily used portions of main memory. To maintain cache "coherency" is to make sure that this local copy is identical to main memory. In a system where multiple masters can access the same memory, there is always a risk that one master will alter the contents of a memory location that is duplicated in the local cache of another master. (The cache is said to contain "stale" data.) One rather restrictive solution is to not allow cache subsystems to cache shared memory. Another simple solution is to flush the cache anytime another master writes to system memory. However, this can seriously degrade system performance as excessive cache flushing will reduce the hit rate of what may otherwise be a highly efficient cache.

The 82385 preserves cache coherency via "bus watching" (also called snooping), a technique that neither impacts performance nor restricts memory mapping. An 82385 that is not currently bus master monitors system bus cycles, and when a write cycle by another master is detected (a snoop), the system address is sampled and used to see if the referenced location is duplicated in the cache. If so (a snoop hit), the corresponding cache entry is invalidated, which will force the 80386 to fetch the up-to-date data from main memory the next time it accesses this modified location. Figure 1-4 depicts the general form of bus watching.
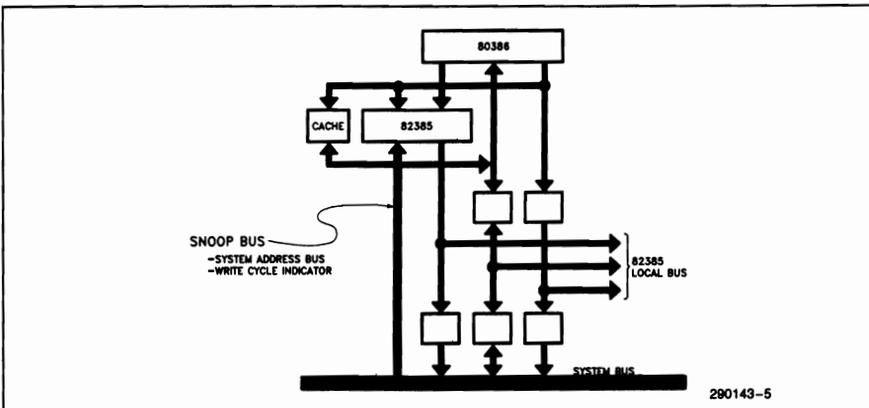


**Figure 1-4. 82385 Bus Watching—Monitor System Bus Write Cycles**

| | P | N | M | L | K | J | H | G | F | E | D | C | B | A |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VCC | VSS | VCC | A27 | A24 | A22 | A19 | A18 | A15 | A12 | A9 | VCC | VSS | A6 |
| 2 | VSS | VSS | A31 | A29 | A25 | A23 | A21 | A17 | A14 | A11 | A8 | A7 | A3 | SA2 |
| 3 | VCC | NA# | READYO# | A30 | A28 | A26 | A20 | A16 | A13 | A10 | A5 | A4 | A2 | SA3 |
| 4 | VSS | CALEN | LDSTB | | | | | | | | | SA4 | SA5 | SA7 |
| 5 | CS3# | CT/R# | CSO# | | | | | | | | | SA6 | SA10 | SA9 |
| 6 | CWEB# | CS2# | CS1# | | | | | | | | | SA8 | SA11 | SA13 |
| 7 | COEA# | CWEA# | COEB# | | | | | | | | | SA12 | SA15 | SA14 |
| 8 | BRDYEN# | MISS# | WBS | | | | | | | | | SA18 | SA16 | SA17 |
| 9 | BLOCK# | BADS# | BAOE# | | | | | | | | | SA22 | SA19 | SA20 |
| 10 | BACP | BT/R# | DOE# | | | | | | | | | SA25 | SA24 | SA21 |
| 11 | VCC | BHOLD | BHLDA | | | | | | | | | SA27 | SA26 | SA23 |
| 12 | VSS | BBE1# | BBEO# | BBE2# | BRESET | SEN | BE2# | NCA# | D/C# | FLUSH | 2W/D# | SA31 | SA29 | SA28 |
| 13 | VCC | VCC | BBE3# | BCLK2 | BREADY# | SSTB# | BE1# | X16# | LOCK# | ADS# | RESET | CLK2 | M/S# | SA30 |
| 14 | VSS | VSS | VSS | RESERVED | BNA# | BE3# | LBA# | BEO# | W/R# | M/IO# | READY1# | VCC | VSS | RESERVED |

290143–42

Figure 8-1. 82385 PGA Pinout—View from TOP Side

# 82062
# WINCHESTER DISK CONTROLLER

- ■ Controls SA1000/ST506 Interface Winchester Drives

- ■ 5 MBit/Sec Transfer Rate

- ■ 128, 256, 512, and 1024 Byte Sector Lengths

- ■ Six High-Level Commands: Restore, Seek, Read Sector, Write Sector, Scan ID, and Write Format

- ■ Multiple Sector Transfer Capability

- ■ Implied Seek With Read/Write Commands

- ■ 7 Byte Sector Length Extension For External Error Correction Code

- ■ Single +5 Volt Power Supply

The 82062 Winchester Disk Controller chip interfaces microprocessor systems to Winchester disks that use the Shugart Associates SA1000 or Seagate Technology ST506 interface. Examples include Seagate ST506 and ST512, Shugart SA1000, SA1100, and SA600, Tandon 600, Texas Instruments 506, RMS 500, and Quantum Q2000. The device translates parallel data from the microprocessor to a 5 mbit/sec, MFM-encoded serial bit stream. It provides all the drive control logic and, in addition, control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The 82062 is designed to interface to the host controller through an external sector buffer.
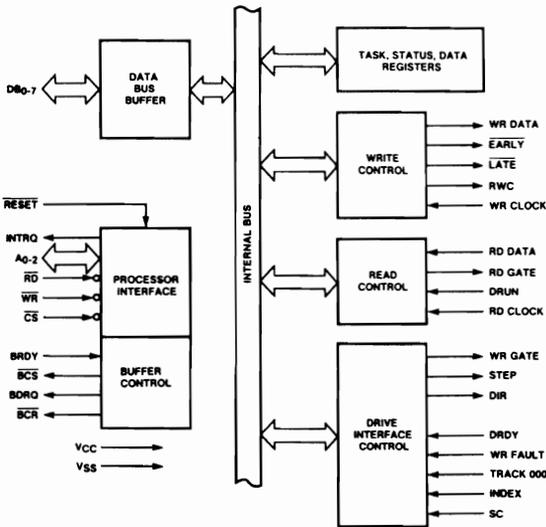


Figure 1.   82062 Internal Block Diagram
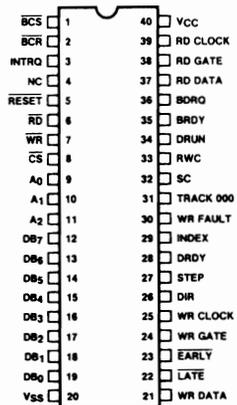
Figure 2.   Pin Configuration

## FUNCTIONAL DESCRIPTION

The 82062 Winchester Disk Controller integrates much of the logic needed to implement Winchester disk controller subsystems. It provides MFM-encoded data and all the control lines required by hard disks using the Seagate Technology ST506 or Shugart Associates SA1000 interface standard. Currently, most 5-1/4 inch and many 8 inch Winchester drives use this interface.

Due to the higher data rates required by these drives—1 byte every 1.6 usec—the 82062 is designed to interface with the host CPU or I/O controller through an external buffer RAM. The 82062 WDC has four pins that minimize the logic required to design a buffer interface.

Figure 3 shows a block diagram of an 82062 subsystem. The WDC is controlled by the host CPU through six commands:

Restore
Seek
Read Sector
Write Sector
Scan ID
Write Format

These commands use information stored by six task registers. Command execution starts immediately after the command register is loaded—therefore commands require only one byte from the CPU after the WDC has been initialized.

The 82062 adds all the required track formatting to the data field, including two bytes of CRC. Optionally, these two bytes can be replaced by seven bytes of ECC information for external error correction

## PROCESSOR INTERFACE

Figure 4 shows one possible hardware interface between the WDC and the host CPU or I/O controller. For initializing the 82062, the host uses the standard peripheral interface lines: $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, and $A_{0-2}$. For read and write cycles, the host and the WDC exchange data through an external RAM buffer. The WDC has four pins, $\overline{BCR}$, $\overline{BCS}$, BRDY, and BDRQ, that facilitate the design of the buffer interface.

The processor starts disk operations by initializing the WDC. It first writes the appropriate parameters into the task register file. The task information includes the drive number, cylinder, head, and sector numbers, sector size, number of sectors to be transferred, and the track number for write precompensation to start. After the task information, the command is written to the command register. See the 82062 Register-CPU Interface section for more details.
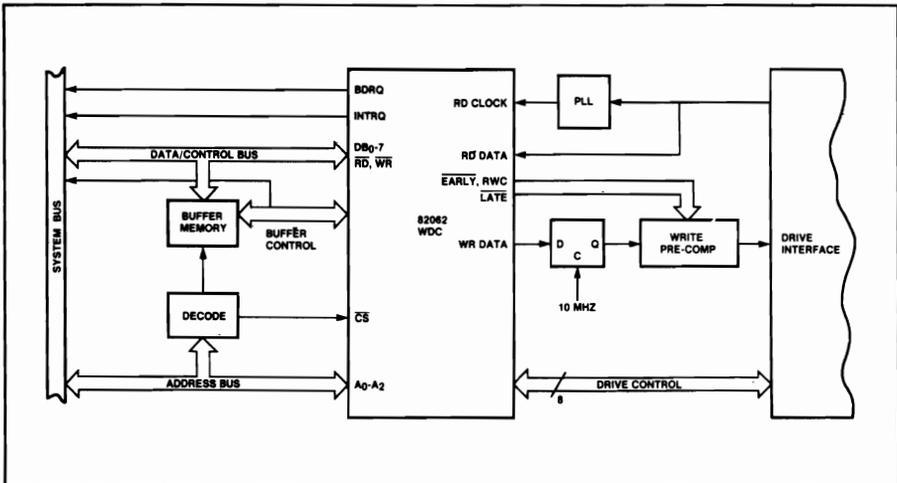


**Figure 3.  System Block Diagram**

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# 82064
# CHMOS WINCHESTER DISK CONTROLLER
# WITH ON-CHIP ERROR DETECTION AND CORRECTION

- Controls ST506/ST412 Interface Winchester Disk Drives
- 5 Mbit/sec Data Transfer Rate
- Compatible with All Intel and Most Other Microprocessors
- High Speed Operation
  — "Zero Wait State" Operation with 8 MHz 80286 and 10 MHz 80186/188
  — "One Wait State" Operation with 10 MHz 80286
- Eight High-Level Commands: Restore, Seek, Read Sector, Write Sector, Scan ID, Write Format, Compute Correction, Set Parameter

- Low Power CHMOS III
- On-Chip ECC Unit Automatically Corrects Errors
- 5 or 11-Bit Correction—Span Software Selectable
- Implied Seeks with Read/Write Commands
- Multiple Sector Transfer Capability
- 128, 256, 512 and 1024 Byte Sector Lengths
- Available in 40-Lead Ceramic Dual In-Line, 40-Lead Plastic Dual In-Line, and 44-Lead Plastic Chip Carrier Packages
  (See Packaging Spec., Order #231369)

The 82064 Winchester Disk Controller (WDC) with on-chip error detection and correction circuitry interfaces microprocessor systems to 5¼" Winchester disk drives. The 82064 is a CHMOS version of the Western Digital WD2010. It is an upgrade to the Western Digital WD1010A-05 Winchester Disk Controller, and includes on-chip ECC, support for drives with up to 2k tracks, and has an additional control signal which eliminates an external decoder.

The 82064 is fabricated on Intel's advanced CHMOS III technology and is available in 40-lead CERDIP, plastic DIP, and 44-lead plastic leaded chip carrier packages.
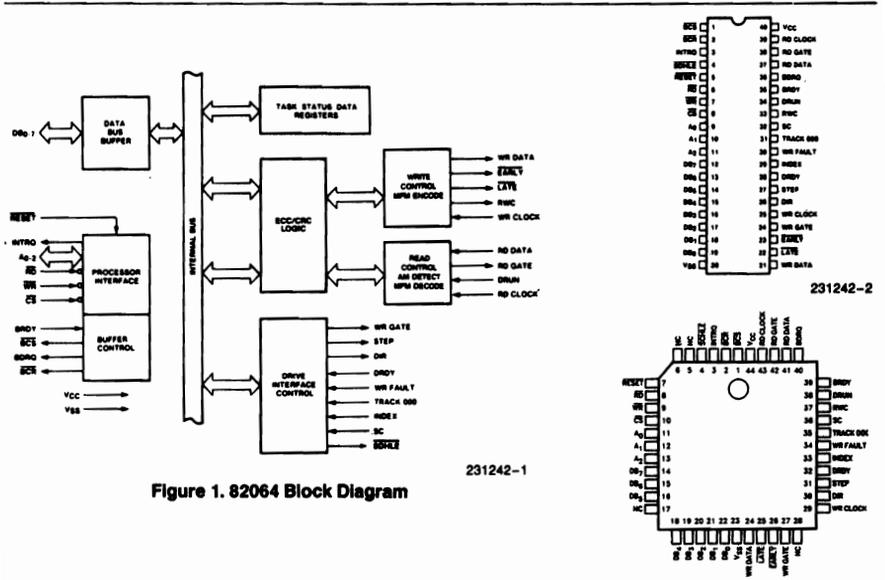


Figure 1. 82064 Block Diagram

231242-1

231242-2

231242-29

Figure 2. 82064 Pinouts

**Table 1. Pin Description**

| Symbol | Pin No. | | Type | Name and Function |
|--------|---------|------|------|-------------------|
| | DIP | PLCC | | |
| $\overline{\text{BCS}}$ | 1 | 1 | O | **BUFFER CHIP SELECT:** Output used to enable reading or writing of the external sector buffer by the 82064. When low, the host should not be able to drive the 82064 data bus, $\overline{\text{RD}}$, or $\overline{\text{WR}}$ lines. |
| $\overline{\text{BCR}}$ | 2 | 2 | O | **BUFFER COUNTER RESET:** Output that is asserted by the 82064 prior to read/write operation. This pin is asserted whenever $\overline{\text{BCS}}$ changes state. Used to reset the address counter of the buffer memory. |
| INTRQ | 3 | 3 | O | **INTERRUPT REQUEST:** Interrupt generated by the 82064 upon command termination. It is reset when the STATUS register is read, or a new command is written to the COMMAND register. Optionally signifies when a data transfer is required on Read Sector commands. |
| $\overline{\text{SDHLE}}$ | 4 | 4 | O | $\overline{\text{SDHLE}}$ is asserted when the SDH register is written by the host. |
| $\overline{\text{RESET}}$ | 5 | 7 | I | **RESET:** Initializes the controller and clears all status flags. Does not clear the Task Register File. |
| $\overline{\text{RD}}$ | 6 | 8 | I/O | **READ:** Tri-state, bi-directional signal. As an input, $\overline{\text{RD}}$ controls the transfer of information from the 82064 registers to the host. $\overline{\text{RD}}$ is an output when the 82064 is reading data from the sector buffer ($\overline{\text{BCS}}$ low). |
| $\overline{\text{WR}}$ | 7 | 9 | I/O | **WRITE:** Tri-state, bi-directional signal. As an input, $\overline{\text{WR}}$ controls the transfer of command or task information into the 82064 registers. $\overline{\text{WR}}$ is an output when the 82064 is writing data to the sector buffer ($\overline{\text{BCS}}$ low). |
| $\overline{\text{CS}}$ | 8 | 10 | I | **CHIP SELECT:** Enables $\overline{\text{RD}}$ and $\overline{\text{WR}}$ as inputs for access to the Task Registers. It has no effect once a disk command starts. |
| $A_{0-2}$ | 9–11 | 11–13 | I | **ADDRESS:** Used to select a register from the task register file. |
| $DB_{0-7}$ | 12–19 | 14–16 18–22 | I/O | **DATA BUS:** Tri-state, bi-directional 8-bit Data Bus with control determined by BCS. When BCS is high the microprocessor has full control of the data bus for reading and writing the Task Register File. When BCS is low the 82064 controls the data bus to transfer to or from the buffer. |
| $V_{ss}$ | 20 | 23 | | Ground |
| WR DATA | 21 | 24 | O | **WRITE DATA:** Output that shifts out MFM data at a rate determined by Write Clock. Requires an external D flip-flop clocked at 10 MHz. The output has an active pullup and pulldown that can sink 4.8 mA. |
| $\overline{\text{LATE}}$ | 22 | 25 | O | **LATE:** Output used to derive a delay value for write precompensation. Valid when WR GATE is high. Active on all cylinders. |
| $\overline{\text{EARLY}}$ | 23 | 26 | O | **EARLY:** Output used to derive a delay value for write precompensation. Valid when WR GATE is high. Active on all cylinders. |

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# 82716/VSDD
# VIDEO STORAGE AND DISPLAY DEVICE

- Low Cost Graphics and Text Capability
- Minimum Chip Count Display Controller
- Displays Up to 16 Bit Map and Character Objects of Any Size
- On-Chip 16/4096 Color Palette
- On-Chip DRAM Controller
- On-Chip D/A Converters
- Arbitration of Processor RAM Requests
- NAPLPS and CEPT Compatible

- Objects Allow Windowing or Animation
- Resolution Up to 640 x 512 Pixels
- Up to 512K Bytes of Display Memory
- Compatible with 8 and 16 Bit Processors/Micro Controllers
- Twin Mode Operation for Higher Throughput
- Powerful External Sync and Overlay Capabilities

82716/VSDD is a low cost, highly integrated video controller. It displays graphics and textual information using a minimum of chips. It allows the management of up to 16 display objects on the screen at any one time. These objects may be formatted as bit map or character arrays and can be used for windowing or animation.

An on-chip color palette allows the selection of up to 16 colors, from a range of 4096. The palette can be programmed to drive a set of on-chip D/A converters. The VSDD also provides DRAM controller functions.
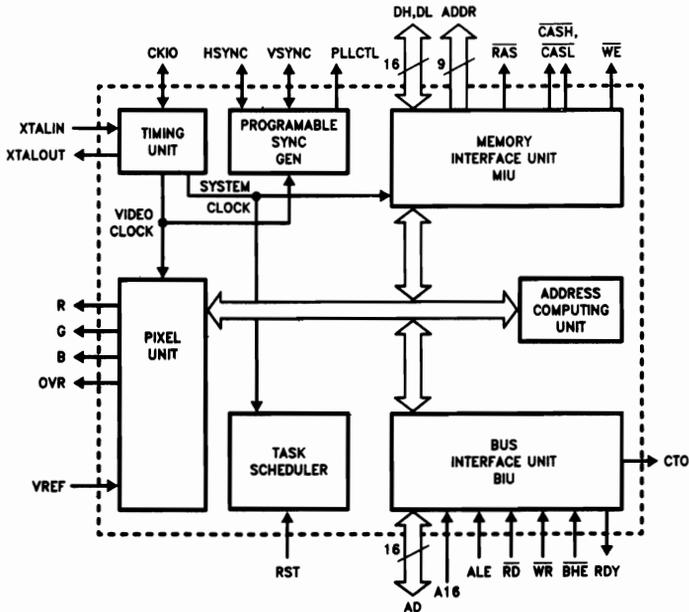


Figure 1. VSDD Block Diagram

231680-1

## GENERAL DESCRIPTION

The 82716/VSDD is a low cost, highly integrated VLSI CRT controller offering advanced display capabilities for Videotex and color graphics displays. Its internal architecture allows it to be connected to any Intel compatible processor. The screen image is constructed from various user-specified objects residing in the VSDD memory (mapped into the processor's address space). Pixels are taken directly from the memory for display on the screen. Characters are constructed employing user-defined RAM-based character generators. The VSDD takes the object data from its memory, buffers it, and runs it through a color palette and D/A converters to produce a video signal. The VSDD also supports overlapped objects and transparent pixels.

In conjunction with appropriate software, the VSDD can be compatible with such video standards as NAPLPS, CEPT or custom configurations. Its multi-window features and resolution make the VSDD ideal for:

• Home Information Systems, TV's, VCR's, Games and Home Computers

• Alphanumeric Color/Monochrome Terminals

• Real-Time Process Control Monitoring Equipment

• Videotex Terminals of the Alphageometric, Alphanumeric and Alphaphotographic Type

• Automotive Displays

• Medical Electronics

Figure 1 shows the block diagram of the VSDD.

## FUNCTIONAL DESCRIPTION

**Bus Interface Unit (BIU):** BIU is the interface between the CPU and the VSDD. CPU accesses the DRAM through the BIU.

**Memory Interface Unit (MIU):** It is the interface between the VSDD and the DRAM. MIU generates the control signals and the row and column addresses for DRAM.

**Timing Unit:** It consists of oscillator and clock generators. The Video and internal clocks are generated by timing unit.

**Sync Generator:** The sync generator controls the horizontal and vertical timings for raster generation (HSYNC and VSYNC).

**Pixel Unit:** The pixel unit contains pixel formatting unit as well as scan line buffers in which display information is placed for each scan line. It also contains the color lookup table (color palette) and D/A converters (DACs). DACs convert the digital color specifications to analog RGB signals for the monitor.

**Task Scheduler:** This unit is the control circuit of the VSDD. It provides the control signals for internal logic.

**Address Computing Unit:** It computes the DRAM addresses.



**Figure 2. Simple System Configuration**

# 82720
# GRAPHICS DISPLAY CONTROLLER

- **High-Performance Graphics for Siggraph Core-, N.A.P.L.P.S.- and ANSI VDI-Compatible or Custom Systems**
- **Displays Low-to-High Resolution Images**
- **Draws Characters, Points, Lines, Arcs and Rectangles**
- **Supports Monochrome, Greyscale or Color Displays**
- **Zooms, Pans and Windows Through a 1/2-Mbyte Display Memory**

- **Extremely Flexible Programmable Screen Display, Blanking and Sync Formats**
- **Compatible with Intel's MCS®-51 and iAPX 88/86/186 Microprocessor Families**
- **High-Level Commands Off Load the Master Processor from Bit Map Loading and Screen Refresh Tasks**
- **Supports Graphics, Character, and Mixed Display Modes**

## FUNCTIONAL DESCRIPTION

The 82720 Graphics Display Controller (GDC) is an intelligent microprocessor peripheral designed to drive high-performance raster-scan computer graphics and character CRT displays. Positioned between the video display memory and an Intel microprocessor bus, the GDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the GDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the GDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed while partitioned screen areas can be independently scrolled and panned. With its light pen input and multiple controller capability, the GDC is ideal for most computer graphics applications. Systems implemented with the GDC can be designed to be compatible with standards such as Siggraph Core, N.A.P.L.P.S., and ANSI VDI or custom implementations.
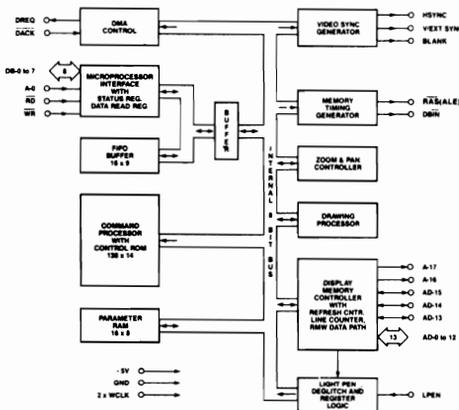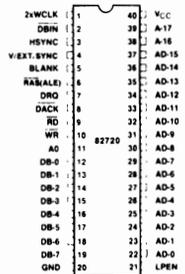


**Figure 1. Block Diagram**          **Figure 2. Pin Configuration**

# 82786 CHMOS GRAPHICS COPROCESSOR

- High Performance Graphics
- Fast Polygon and Line Drawing
- High Speed Character Drawing
- Advanced DRAM/VRAM Controller for Graphics Memory up to 4 Mbytes
- Supports up to 200 MHz CRTs
  — up to 640 by 480 by 8 Bits (DRAMs) or 1400 by 1400 by 1 Bit (DRAMs) or 2048 by 2048 by 8 Bits (VRAMs)
- Up to 256 Simultaneous Colors
- Integral DRAM/VRAM Controller, Shift Registers and DMA Channel
- International Character Support
- Interface Designed for Device-Independent Standards

- Hardware Windows
- Fast Bit-Block Copies Between System and Bitmap Memories
- Third-Party Software Support
- Multi-tasking Support
- Provides Support for Rapid Filling with Patterns
- Programmable Video Timing
- Advanced CHMOS Technology
- Supports Dual Port Video DRAMs & Sequential Access DRAMs
- 88 Pin Grid Array and Leadless Chip Carrier

(See Intel Packaging; Order Number: 231369)

The 82786 is a powerful, yet simple component designed for microcomputer graphics applications including personal computers, engineering workstations, terminals, and laser printers. Its advanced software interface makes applications and systems level programming efficient and straight-forward. Its performance and high-integration make it a cost-effective component while improving the performance of nearly any design. Hardware windows provide instantaneous changes of display contents and support multiple graphics applications from multiple graphics bitmaps. Applications programs written for the IBM Personal Computer can be run within one or more windows of the display when used with Intel CPUs.

The 82786 works with all Intel microprocessors, and is a high-performance replacement for sub-systems and boards which have traditionally used discrete components and/or software for graphics functions. The 82786 requires minimal support circuitry for most system configurations, and thus reduces the cost and board space requirements of many applications. The 82786 is based on Intel's advanced CHMOS III process.



231676–27

**Figure 1. 82786 Pinout—Bottom View**

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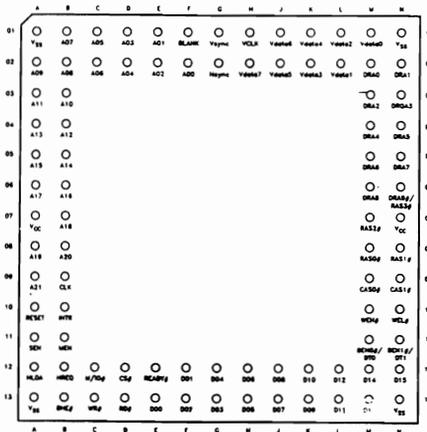
# i486™ MICROPROCESSOR

- **Binary Compatible with Large Software Base**
  - MS-DOS*, OS/2**, Windows
  - UNIX*** System V/386
  - IRMX®, IRMK™ Kernels
- **High Integration Enables On-Chip**
  - 8 Kbyte Code and Data Cache
  - Floating Point Unit
  - Paged, Virtual Memory Management
- **Easy To Use**
  - Built-In Self Test
  - Hardware Debugging Support
  - Intel Software Support
  - Extensive Third Party Software Support

- **High Performance Design**
  - Frequent Instructions Execute in One Clock
  - 25 MHz and 33 MHz Clock Frequencies
  - 106 Mbyte/Sec Burst Bus
  - CHMOS IV Process Technology
- **Complete 32-Bit Architecture**
  - Address and Data Busses
  - Registers
- **Multiprocessor Support**
  - Multiprocessor Instructions
  - Cache Consistency Protocols
  - Support for Second Level Cache

The i486™ CPU offers the highest performance for DOS, OS/2, Windows and UNIX System V/386 applications. It is 100% binary compatible with the 386™ CPU. One million transistors integrate cache memory, floating point hardware and memory management on-chip while retaining binary compatibility with previous members of the 86 architectural family. Frequently used instructions execute in one cycle resulting in RISC performance levels. An 8 Kbyte unified code and data cache combined with a 106 Mbyte/Sec burst bus at 33.3 MHz ensure high system throughput even with inexpensive DRAMs.

New features enhance multiprocessing systems. New instructions speed manipulation of memory based semaphores. On-chip hardware ensures cache consistency and provides hooks for multilevel caches.

The built in self test extensively tests on-chip logic, cache memory and the on-chip paging translation cache. Debug features include breakpoint traps on code execution and data accesses.

## i486™ Microprocessor Pipelined 32-Bit Microarchitecture



240440-1

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*MS-DOS® is a registered trademark of Microsoft Corporation
**OS/2™ is a trademark of Microsoft Corporation.
***UNIX™ is a trademark of AT&T.

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|
| S | A27 | A26 | A23 | NC | A14 | VSS | A12 | VSS | VSS | VSS | VSS | VSS | A10 | VSS | A6 | A4 | ADS# |
| R | A28 | A25 | VCC | VSS | A18 | VCC | A15 | VCC | VCC | VCC | VCC | A11 | A8 | VCC | A3 | BLAST# | NC |
| Q | A31 | VSS | A17 | A19 | A21 | A24 | A22 | A20 | A16 | A13 | A9 | A5 | A7 | A2 | BREQ | PLOCK# | PCHK# |
| P | D0 | A29 | A30 | | | | | | | | | | | | HLDA | VCC | VSS |
| N | D2 | D1 | DP0 | | | | | | | | | | | | LOCK# | M/IO# | W/R# |
| M | VSS | VCC | D4 | | | | | | | | | | | | D/C# | VCC | VSS |
| L | VSS | D6 | D7 | | | | | | | | | | | | PWT | VCC | VSS |
| K | VSS | VCC | D14 | | | | | | | | | | | | BE0# | VCC | VSS |
| J | VCC | D5 | D16 | | | | | | | | | | | | BE2# | BE1# | PCD |
| H | VSS | D3 | DP2 | | | | | | | | | | | | BRDY# | VCC | VSS |
| G | VSS | VCC | D12 | | | | | | | | | | | | NC | VCC | VSS |
| F | DP1 | D8 | D15 | | | | | | | | | | | | KEN# | RDY# | BE3# |
| E | VSS | VCC | D10 | | | | | | | | | | | | HOLD | VCC | VSS |
| D | D9 | D13 | D17 | | | | | | | | | | | | A20M# | BS8# | BOFF# |
| C | D11 | D18 | CLK | VCC | VCC | D27 | D26 | D28 | D30 | NC | NC | NC | NC | FERR# | FLUSH# | RESET | BS16# |
| B | D19 | D21 | VSS | VSS | VSS | D25 | VCC | D31 | VCC | NC | VCC | NC | NC | NC | NMI | NC | EADS# |
| A | D20 | D22 | NC | D23 | DP3 | D24 | VSS | D29 | VSS | NC | VSS | NC | NC | NC | IGNNE# | INTR | AHOLD |

486™ Microprocessor PIN SIDE VIEW

240440-2

**Figure 1.1**

•
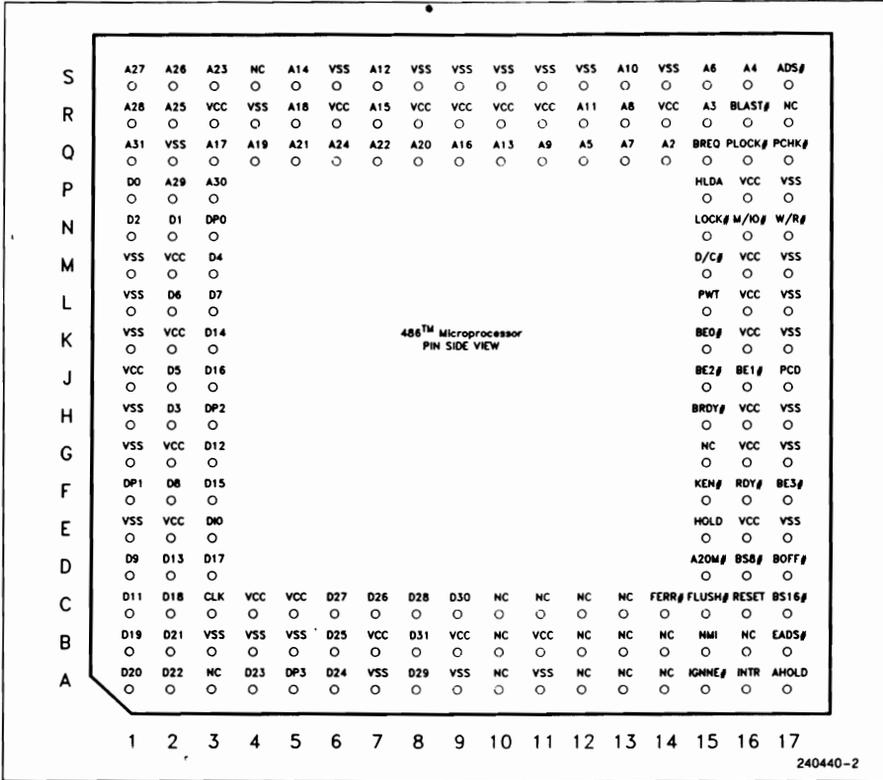
## QUICK PIN REFERENCE

What follows is a brief pin description. For detailed signal descriptions refer to Section 6.

| Symbol | Type | Name and Function |
|---|---|---|
| CLK | I | *Clock* provides the fundamental timing and the internal operating frequency for the 486 microprocessor. All external timing parameters are specified with respect to the rising edge of CLK. |
| **ADDRESS BUS** | | |
| A31–A4<br>A2–A3 | I/O<br>O | A31–A2 are the *address lines* of the microprocessor. A31–A2 together with the byte enables, BE0#–BE3#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the microprocessor to perform cache line invalidations. Input signals must meet setup and hold times $t_{22}$ and $t_{23}$. A31–A2 are active HIGH and are not driven during bus or address hold. |
| BE3#<br>BE2#<br>BE1#<br>BE0# | O<br>O<br>O<br>O | The *byte enable* signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3# applies to D24–D31, BE2# applies to D16–D23, BE1# applies to D8–D15 and BE0# applies to D0–D7. BE0#–BE3# are active LOW and are not driven during bus hold. |
| **DATA BUS** | | |
| D31–D0 | I/O | These are the *data lines* for the 486 microprocessor. Lines D0–D7 define the least significant byte of the data bus while lines D24–D31 define the most significant byte of the data bus. These signals must meet setup and hold times $t_{22}$ and $t_{23}$ for proper operation on reads. These pins are active HIGH and are driven during the second and subsequent clocks of write cycles. |
| **DATA PARITY** | | |
| DP0–DP3 | I/O | There is one *data parity* pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the 486 microprocessor. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information to insure that the correct parity check status is indicated by the 486 microprocessor. The signals read on these pins do not affect program execution.<br>Input signals must meet setup and hold times $t_{22}$ and $t_{23}$. DP0–DP3 should be connected to $V_{CC}$ through a pullup resistor in systems which do not use parity. DP0–DP3 are active HIGH and are driven during the second and subsequent clocks of write cycles. |
| PCHK# | O | *Parity Status* is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. PCHK# is valid only in the clock immediately after read data is returned to the microprocessor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated. |
| **BUS CYCLE DEFINITION** | | |
| M/IO#<br>D/C#<br>W/R# | O<br>O<br>O | The *memory/input-output, data/control* and *write/read* lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted.<table><tr><td>M/IO#</td><td>D/C#</td><td>W/R#</td><td>Bus Cycle Initiated</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Halt/Special Cycle</td></tr><tr><td>0</td><td>1</td><td>0</td><td>I/O Read</td></tr><tr><td>0</td><td>1</td><td>1</td><td>I/O Write</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Code Read</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Memory Read</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Memory Write</td></tr></table>The bus definition signals are not driven during bus hold and follow the timing of the address bus. Refer to Section 7.2.11 for a description of the special bus cycles. |

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## QUICK PIN REFERENCE (Continued)

| Symbol | Type | Name and Function |
|---|---|---|
| **BUS CYCLE DEFINITION** (Continued) | | |
| LOCK # | O | The *bus lock* pin indicates that the current bus cycle is locked. The 486 microprocessor will not allow a bus hold when LOCK # is asserted (but address holds are allowed). LOCK # goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when ready is returned. LOCK # is active LOW and is not driven during bus hold. Locked read cycles will not be transformed into cache fill cycles if KEN is returned active. |
| PLOCK # | O | The *pseudo-lock* pin indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are floating point long reads and writes (64 bits), segment table descriptor reads (64 bits), in addition to cache line fills (128 bits). The 486 microprocessor will drive PLOCK # active until the addresses for the last bus cycle of the transaction have been driven regardless of whether RDY # or BRDY # have been returned. |
| | | Normally PLOCK # and BLAST # are inverse of each other. However during the first bus cycle of a 64-bit floating point write, both PLOCK # and BLAST # will be asserted. PLOCK # is a function of the BS8 #, BS16 # and KEN # inputs. PLOCK # should be sampled only in the clock ready is returned. PLOCK # is active LOW and is not driven during bus hold. |
| **BUS CONTROL** | | |
| ADS # | O | The *address status* output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS # is driven active in the same clock as the addresses are driven. ADS # is active LOW and is not driven during bus hold. |
| RDY # | I | The *non-burst ready* input indicates that the current bus cycle is complete. RDY # indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the 486 microprocessor in response to a write. RDY # is ignored when the bus is idle and at the end of the first clock of the bus cycle. |
| | | RDY # is active during address hold. Data can be returned to the processor while AHOLD is active. |
| | | RDY # is active LOW, and is not provided with an internal pullup resistor. RDY # must satisfy setup and hold times $t_{16}$ and $t_{17}$ for proper chip operation. |
| **BURST CONTROL** | | |
| BRDY # | I | The *burst ready input* performs the same function during a burst cycle that RDY # performs during a non-burst cycle. BRDY # indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. BRDY # is ignored when the bus is idle and at the end of the first clock in a bus cycle. |
| | | BRDY # is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus will be strobed into the microprocessor when BRDY # is sampled active. If RDY # is returned simultaneously with BRDY #, BRDY # is ignored and the burst cycle is prematurely aborted. |
| | | BRDY # is active LOW and is provided with a small pullup resistor. BRDY # must satisfy the setup and hold times $t_{16}$ and $t_{17}$. |
| BLAST # | O | The *burst last* signal indicates that the next time BRDY # is returned the burst bus cycle is complete. BLAST # is active for both burst and non-burst bus cycles. BLAST # is active LOW and is not driven during bus hold. |

## QUICK PIN REFERENCE (Continued)

| Symbol | Type | Name and Function |
|---|---|---|
| **INTERRUPTS** | | |
| RESET | I | The *reset* input forces the 486 microprocessor to begin execution at a known state. The microprocessor cannot begin execution of instructions until at least 1 ms after $V_{CC}$ and CLK have reached their proper DC and AC specifications. The RESET pin should remain active during this time to insure proper microprocessor operation. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times $t_{20}$ and $t_{21}$ for recognition in any specific clock. |
| INTR | I | The *maskable interrupt* indicates that an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing will be initiated. The 486 microprocessor will generate two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to assure that the interrupt is recognized. INTR is active HIGH and is not provided with an internal pulldown resistor. INTR is asynchronous, but must meet setup and hold times $t_{20}$ and $t_{21}$ for recognition in any specific clock. |
| NMI | I | The *non-maskable interrupt* request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held LOW for at least four CLK periods before this rising edge. NMI is not provided with an internal pulldown resistor. NMI is asynchronous, but must meet setup and hold times $t_{20}$ and $t_{21}$ for recognition in any specific clock. |
| **BUS ARBITRATION** | | |
| BREQ | O | The *internal cycle pending* signal indicates that the 486 microprocessor has internally generated a bus request. BREQ is generated whether or not the 486 microprocessor is driving the bus. BREQ is active HIGH and is never floated. |
| HOLD | I | The *bus hold request* allows another bus master complete control of the 486 microprocessor bus. In response to HOLD going active the 486 microprocessor will float most of its output and input/output pins. HLDA will be asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The 486 microprocessor will remain in this state until HOLD is deasserted. HOLD is active high and is not provided with an internal pulldown resistor. HOLD must satisfy setup and hold times $t_{18}$ and $t_{19}$ for proper operation. |
| HLDA | O | *Hold acknowledge* goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the 486 microprocessor has given the bus to another local bus master. HLDA is driven active in the same clock that the 486 microprocessor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold. |
| BOFF# | I | The *backoff* input forces the 486 microprocessor to float its bus in the next clock. The microprocessor will float all pins normally floated during bus hold but HLDA will not be asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The microprocessor remains in bus hold until BOFF# is negated. If a bus cycle was in progress when BOFF# was asserted the cycle will be restarted. BOFF# is active LOW and must meet setup and hold times $t_{18}$ and $t_{19}$ for proper operation. |
| **CACHE INVALIDATION** | | |
| AHOLD | I | The *address hold* request allows another bus master access to the 486 microprocessor's address bus for a cache invalidation cycle. The 486 microprocessor will stop driving its address bus in the clock following AHOLD going active. Only the address bus will be floated during address hold, the remainder of the bus will remain active. AHOLD is active HIGH and is provided with a small internal pulldown resistor. For proper operation AHOLD must meet setup and hold times $t_{18}$ and $t_{19}$. |

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## QUICK PIN REFERENCE (Continued)

| Symbol | Type | Name and Function |
|---|---|---|
| **CACHE INVALIDATION** (Continued) | | |
| EADS | I | This signal indicates that a *valid external address* has been driven onto the 486 microprocessor address pins. This address will be used to perform an internal cache invalidation cycle. EADS # is active LOW and is provided with an internal pullup resistor. EADS # must satisfy setup and hold times $t_{12}$ and $t_{13}$ for proper operation. |
| **CACHE CONTROL** | | |
| KEN # | I | The *cache enable* pin is used to determine whether the current cycle is cacheable. When the 486 microprocessor generates a cycle that can be cached and KEN # is active, the cycle will become a cache line fill cycle. Returning KEN # active one clock before ready during the last read in the cache line fill will cause the line to be placed in the on-chip cache. KEN # is active LOW and is provided with a small internal pullup resistor. KEN # must satisfy setup and hold times $t_{14}$ and $t_{15}$ for proper operation. |
| FLUSH # | I | The *cache flush* input forces the 486 microprocessor to flush its entire internal cache. FLUSH # is active low and need only be asserted for one clock. FLUSH # is asynchronous but setup and hold times $t_{20}$ and $t_{21}$ must be met for recognition in any specific clock. |
| **PAGE CACHEABILITY** | | |
| PWT<br>PCD | O<br>O | The *page write-through* and *page cache disable* pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry or page directory entry. If paging is disabled or for cycles that are not paged, PWT and PCD reflect the state of the PWT and PCD bits in control register 3. PWT and PCD have the same timing as the cycle definition pins (M/IO #, D/C # and W/R #). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache enable bit (CE) in Control Register 0. |
| **NUMERIC ERROR REPORTING** | | |
| FERR # | O | The *floating point error* pin is driven active when a floating point error occurs. FERR # is similar to the ERROR # pin on the 387™ math coprocessor. FERR # is included for compatibility with systems using DOS type floating point error reporting. FERR # is active LOW, and is not floated during bus hold. |
| IGNNE # | I | When the *ignore numeric error* pin is asserted the 486 microprocessor will ignore a numeric error and continue executing non-control floating point instructions. When IGNNE # is deasserted the 486 microprocessor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE # has no effect when the NE bit in control register 0 is set. IGNNE # is active LOW and is provided with a small internal pullup resistor. IGNNE # is asynchronous but setup and hold times $t_{20}$ and $t_{21}$ must be met to insure recognition on any specific clock. |
| **BUS SIZE CONTROL** | | |
| BS16 #<br>BS8 # | I<br>I | The *bus size 16* and *bus size 8* pins (bus sizing pins) cause the 486 microprocessor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before ready is used by the 486 microprocessor to determine the bus size. These signals are active LOW and are provided with internal pullup resistors. These inputs must satisfy setup and hold times $t_{14}$ and $t_{15}$ for proper operation. |
| **ADDRESS MASK** | | |
| A20M # | I | When the *address bit 20 mask* pin is asserted, the 486 microprocessor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M # emulates the address wraparound at one Mbyte which occurs on the 8086. A20M # is active LOW and should be asserted only when the processor is in real mode. This pin is asynchronous but should meet setup and hold times $t_{20}$ and $t_{21}$ for recognition in any specific clock. |

## Table 1.1. Output Pins

| Name | Active Level | When Floated |
|------|--------------|--------------|
| BREQ | HIGH | |
| HLDA | HIGH | |
| BE0#–BE3# | LOW | Bus Hold |
| PWT, PCD | HIGH | Bus Hold |
| W/R#, D/C#, M/IO# | HIGH | Bus Hold |
| LOCK# | LOW | Bus Hold |
| PLOCK# | LOW | Bus Hold |
| ADS# | LOW | Bus Hold |
| BLAST# | LOW | Bus Hold |
| PCHK# | LOW | |
| FERR# | LOW | |
| A2–A3 | HIGH | Bus, Address Hold |

## Table 1.2. Input Pins

| Name | Active Level | Synchronous/ Asynchronous |
|------|--------------|---------------------------|
| CLK | | |
| RESET | HIGH | Asynchronous |
| HOLD | HIGH | Synchronous |
| AHOLD | HIGH | Synchronous |
| EADS# | LOW | Synchronous |
| BOFF# | LOW | Synchronous |
| FLUSH# | LOW | Asynchronous |
| A20M# | LOW | Asynchronous |
| BS16#, BS8# | LOW | Synchronous |
| KEN# | LOW | Synchronous |
| RDY# | LOW | Synchronous |
| BRDY# | LOW | Synchronous |
| INTR | HIGH | Asynchronous |
| NMI | HIGH | Asynchronous |
| IGNNE# | LOW | Asynchronous |

## Table 1.3. Input/Output Pins

| Name | Active Level | When Floated |
|------|--------------|--------------|
| D0–D31 | HIGH | Bus Hold |
| DP0–DP3 | HIGH | Bus Hold |
| A4–A31 | HIGH | Bus, Address Hold |

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## 2.0 ARCHITECTURAL OVERVIEW

The 486 microprocessor is a 32-bit architecture with on-chip memory management, floating point and cache memory units.

The 486 microprocessor contains all the features of the 386™ microprocessor with enhancements to increase performance. The instruction set includes the complete 386 microprocessor instruction set along with extensions to serve new applications. The on-chip memory management unit (MMU) is completely compatible with the 386 microprocessor MMU. The 486 microprocessor brings the 387™ math coprocessor on-chip. All software written for the 386 microprocessor, 387 math coprocessor and previous members of the 86/87 architectural family will run on the 486 microprocessor without any modifications.

Several enhancements have been added to the 486 microprocessor to increase performance. On-chip cache memory allows frequently used data and code to be stored on-chip reducing accesses to the external bus. RISC design techniques have been used to reduce instruction cycle times. A burst bus feature enables fast cache fills. All of these features combined, lead to performance greater than twice that of a 386 microprocessor.

The memory management unit (MMU) consists of a segmentation unit and a paging unit. Segmentation allows management of the logical address space by providing easy data and code relocatibility and efficient sharing of global resources. The paging mechanism operates beneath segmentation and is transparent to the segmentation process. Paging is optional and can be disabled by system software. Each segment can be divided into one or more 4 Kbyte segments. To implement a virtual memory system, the 486 microprocessor supports full restartability for all page and segment faults.

Memory is organized into one or more variable length segments, each up to four gigabytes ($2^{32}$ bytes) in size. A segment can have attributes associated with it which include its location, size, type (i.e., stack, code or data), and protection characteristics. Each task on a 486 microprocessor can have a maximum of 16,381 segments each up to four gigabytes in size. Thus each task has a maximum of 64 terabytes (trillion bytes) of virtual memory.

The segmentation unit provides four-levels of protection for isolating and protecting applications and the operating system from each other. The hardware enforced protection allows the design of systems with a high degree of integrity.

The 486 microprocessor has two modes of operation: Real Address Mode (Real Mode) and Protected Mode Virtual Address Mode (Protected Mode). In Real Mode the 486 microprocessor operates as a very fast 8086. Real Mode is required primarily to setup the processor for Protected Mode operation. Protected Mode provides access to the sophisticated memory management paging and privilege capabilities of the processor.

Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each virtual 8086 task behaves with 8086 semantics, allowing 8086 software (an application program or an entire operating system) to execute.

The on-chip floating point unit operates in parallel with the arithmetic and logic unit and provides arithmetic instructions for a variety of numeric data types. It executes numerous built-in transcendental functions (e.g., tangent, sine, cosine, and log functions). The floating point unit fully conforms to the ANSI/IEEE standard 754-1985 for floating point arithmetic.

The on-chip cache is 8 Kbytes in size. It is 4-way set associative and follows a write-through policy. The on-chip cache includes features to provide flexibility in external memory system design. Individual pages can be designated as cacheable or non-cacheable by software or hardware. The cache can also be enabled and disabled by software or hardware.

Finally the 486 microprocessor has features to facilitate high performance hardware designs. The 1X clock eases high frequency board level designs. The burst bus feature enables fast cache fills. These features are described beginning in Section 6.

## 2.1 Register Set

The 486 microprocessor register set includes all the registers contained in the 386 microprocessor and the 387 math coprocessor. The register set can be split into the following categories:

Base Architecture Registers
General Purpose Registers
Instruction Pointer
Flags Register
Segment Registers

Systems Level Registers
Control Registers
System Address Registers

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Floating Point Registers

Data Registers

Tag Word

Status Word

Instruction and Data Pointers

Control Word

Debug and Test Registers

The base architecture and floating point registers are accessible by the applications program. The system level registers are only accessible at privilege level 0 and are used by the systems level program. The debug and test registers are also only accessible at privilege level 0.

## 2.1.1 BASE ARCHITECTURE REGISTERS

Figure 2.1 shows the 486 microprocessor base architecture registers. The contents of these registers are task-specific and are automatically loaded with a new context upon a task switch operation.
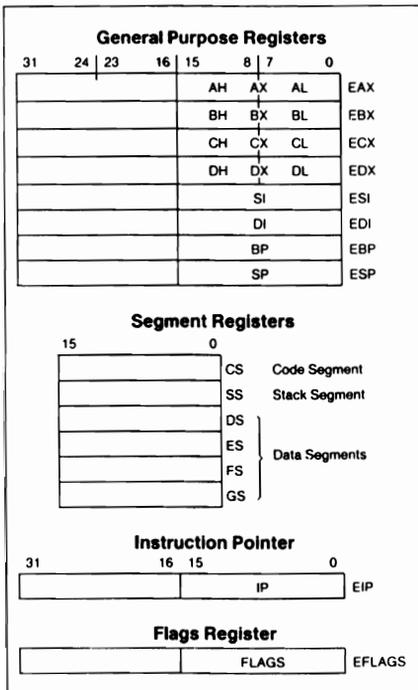


**Figure 2.1. Base Architecture Registers**

The base architecture includes six directly accessible descriptors, each specifying a segment up to 4 Gbytes in size. The descriptors are indicated by the selector values placed in the 486 microprocessor segment registers. Various selector values can be loaded as a program executes.

The selectors are also task-specific, so the segment registers are automatically loaded with new context upon a task switch operation.

### 2.1.1.1 General Purpose Registers

The eight 32-bit general purpose registers are shown in Figure 2.1. These registers hold data or address quantities. The general purpose registers can support data operands of 1, 8, 16 and 32 bits, and bit fields of 1 to 32 bits. Address operands of 16 and 32 bits are supported. The 32-bit registers are named EAX, EBX, ECX, EDX, ESI, EDI, EBP and ESP

The least significant 16 bits of the general purpose registers can be accessed separately by using the 16-bit names of the registers AX, BX, CX, DX, SI, DI, BP and SP. The upper 16 bits of the register are not changed when the lower 16 bits are accessed separately

Finally 8-bit operations can individually access the lowest byte (bits 0–7) and the higher byte (bits 8–15) of the general purpose registers AX, BX, CX and DX. The lowest bytes are named AL, BL, CL and DL respectively. The higher bytes are named AH, BH, CH and DH respectively. The individual byte accessibility offers additional flexibility for data operations but is not used for effective address calculation.

### 2.1.1.2 Instruction Pointer

The instruction pointer, shown in Figure 2.1, is a 32-bit register named EIP. EIP holds the offset of the next instruction to be executed. The offset is always relative to the base of the code segment (CS). The lower 16 bits (bits 0–15) of the EIP contain the 16-bit instruction pointer named IP, which is used for 16-bit addressing.

### 2.1.1.3 Flags Register

The flags register is a 32-bit register named EFLAGS. The defined bits and bit fields within EFLAGS control certain operations and indicate status of the 486 microprocessor. The lower 16 bits (bit 0–15) of EFLAGS contain the 16-bit register named FLAGS, which is most useful when executing 8086 and 80286 code. EFLAGS is shown in Figure 2.2.

**Figure 2.2. Flags Register**

EFLAGS bits 1, 3, 5, 15 and 19–31 are "undefined". When these bits are stored during interrupt processing or with a PUSHF instruction (push flags onto stack), a one is stored in bit 1 and zeros in bits 3, 5, 15 and 19–31.

The EFLAGS register in the 486 microprocessor contains a new bit not available in the 386 microprocessor. The new bit, AC, is defined in the upper 16 bits of the register and it enables faults on accesses to misaligned data.

AC    (Alignment Check, bit 18)

The AC bit enables the generation of faults if a memory reference is to a misaligned address. Alignment faults are enabled when AC is set to 1. A mis-aligned address is a word access

to an odd address, a dword access to an address that is not on a dword boundary, or an 8-byte reference to an address that is not on a 64-bit word boundary. See Section 7.1.6 for more information on operand alignment.

Alignment faults are only generated by programs running at privilege level 3. The AC bit setting is ignored at privilege levels 0, 1 and 2. Note that references to the descriptor tables (for selector loads), or the task state segment (TSS), are implicitly level 0 references even if the instructions causing the references are executed at level 3. Alignment faults are reported through interrupt 17, with an error code of 0. Table 2.1 gives the alignment required for the 486 microprocessor data types.

**Table 2.1. Data Type Alignment Requirements**

| Memory Access | Alignment (Byte Boundary) |
|---|---|
| Word | 2 |
| Dword | 4 |
| Single Precision Real | 4 |
| Double Precision Real | 8 |
| Extended Precision Real | 8 |
| Selector | 2 |
| 48-Bit Segmented Pointer | 4 |
| 32-Bit Flat Pointer | 4 |
| 32-Bit Segmented Pointer | 2 |
| 48-Bit "Pseudo-Descriptor" | 4 |
| FSTENV/FLDENV Save Area | 4/2 (On Operand Size) |
| FSAVE/FRSTOR Save Area | 4/2 (On Operand Size) |
| Bit String | 4 |

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# MC68000L4
### (4 MHz)
# MC68000L6
### (6 MHz)
# MC68000L
### (8 MHz)

## Advance Information

### 16-BIT MICROPROCESSING UNIT

Advances in semiconductor technology have provided the capability to place on a single silicon chip a microprocessor at least an order of magnitude higher in performance and circuit complexity than has been previously available. The MC68000 is the first of a family of such VLSI microprocessors from Motorola. It combines state-of-the-art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

The resources available to the MC68000 user consist of the following

- 32-Bit Data and Address Registers
- 16 Megabyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory Mapped I/O
- 14 Addressing Modes

As shown in the programming model, the MC68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

## HMOS

(High Density N-Channel, Silicon-Gate Depletion Load)

### 16-BIT MICROPROCESSOR

**L SUFFIX**
CERAMIC PACKAGE
CASE 746-1

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| D4 | 1 ● | 64 | D5 |
| D3 | 2 | 63 | D6 |
| D2 | 3 | 62 | D7 |
| D1 | 4 | 61 | D8 |
| D0 | 5 | 60 | D9 |
| A̅S̅ | 6 | 59 | D10 |
| U̅D̅S̅ | 7 | 58 | D11 |
| L̅D̅S̅ | 8 | 57 | D12 |
| R/W̅ | 9 | 56 | D13 |
| D̅T̅A̅C̅K̅ | 10 | 55 | D14 |
| B̅G̅ | 11 | 54 | D15 |
| B̅G̅A̅C̅K̅ | 12 | 53 | GND |
| B̅R̅ | 13 | 52 | A23 |
| V_CC | 14 | 51 | A22 |
| CLK | 15 | 50 | A21 |
| GND | 16 | 49 | V_CC |
| H̅A̅L̅T̅ | 17 | 48 | A20 |
| R̅E̅S̅E̅T̅ | 18 | 47 | A19 |
| V̅M̅A̅ | 19 | 46 | A18 |
| E | 20 | 45 | A17 |
| V̅P̅A̅ | 21 | 44 | A16 |
| B̅E̅R̅R̅ | 22 | 43 | A15 |
| I̅P̅L̅2 | 23 | 42 | A14 |
| I̅P̅L̅1 | 24 | 41 | A13 |
| I̅P̅L̅0 | 25 | 40 | A12 |
| FC2 | 26 | 39 | A11 |
| FC1 | 27 | 38 | A10 |
| FC0 | 28 | 37 | A9 |
| A1 | 29 | 36 | A8 |
| A2 | 30 | 35 | A7 |
| A3 | 31 | 34 | A6 |
| A4 | 32 | 33 | A5 |

### PROGRAMMING MODEL

| 31 | 16 15 | 8 7 | 0 | |
|---|---|---|---|---|
| | | | D0 | |
| | | | D1 | |
| | | | D2 | |
| | | | D3 | Eight |
| | | | D4 | Data |
| | | | D5 | Registers |
| | | | D6 | |
| | | | D7 | |

| 31 | 16 15 | | 0 | |
|---|---|---|---|---|
| | | | A0 | |
| | | | A1 | |
| | | | A2 | Seven |
| | | | A3 | Address |
| | | | A4 | Registers |
| | | | A5 | |
| | | | A6 | |

User Stack Pointer — A7 — Two Stack
Supervisor Stack Pointer — Pointers

| 31 | | 0 | |
|---|---|---|---|
| | | | Program Counter |

| 15 | 8 7 | 0 | |
|---|---|---|---|
| System Byte | User Byte | | Status Register |

This is advance information and specifications are subject to change without notice.

A 23-bit address bus provides a memory addressing range of greater than 16 megabytes. This large range of addressing capability, coupled with a memory management unit, allows large, modular programs to be developed and operated without resorting to cumbersome and time consuming software bookkeeping and paging techniques.

The status register contains the interrupt mask (eight levels available) as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and/or in a supervisor (S) state.
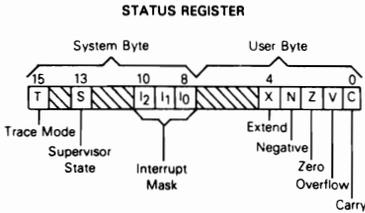
Five basic data types are supported. These data types are:
- Bits
- BCD Digits (4-bits)
- Bytes (8-bits)
- Word (16-bits)
- Long Words (32-bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided for in the instruction set.

The 14 addressing modes, shown in Table 1, include six basic types:
- Register Direct
- Register Indirect
- Absolute
- Immediate
- Program Counter Relative
- Implied

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting and indexing. Program counter relative mode can also be modified via indexing and offsetting

### STATUS REGISTER



### TABLE 1 — DATA ADDRESSING MODES

| Mode | Generation |
|------|-----------|
| **Register Direct Addressing** | |
| Data Register Direct | $EA = Dn$ |
| Address Register Direct | $EA = An$ |
| **Absolute Data Addressing** | |
| Absolute Short | $EA = $ (Next Word) |
| Absolute Long | $EA = $ (Next Two Words) |
| **Program Counter Relative Addressing** | |
| Relative with Offset | $EA = (PC) + d_{16}$ |
| Relative with Index and Offset | $EA = (PC) + (Xn) + d_8$ |
| **Register Indirect Addressing** | |
| Register Indirect | $EA = (An)$ |
| Postincrement Register Indirect | $EA = (An), An \leftarrow An + N$ |
| Predecrement Register Indirect | $An \leftarrow An - N, EA = (An)$ |
| Register Indirect with Offset | $EA = (An) + d_{16}$ |
| Indexed Register Indirect with Offset | $EA = (An) + (Xn) + d_8$ |
| **Immediate Data Addressing** | |
| Immediate | DATA = Next Word(s) |
| Quick Immediate | Inherent Data |
| **Implied Addressing** | |
| Implied Register | $EA = $ SR, USP, SP, PC |

NOTES:
EA = Effective Address
An = Address Register
Dn = Data Register
Xn = Address or Data Register used as Index Register
SR = Status Register
PC = Program Counter
( ) = Contents of

$d_8$ = Eight-bit Offset (displacement)
$d_{16}$ = Sixteen-bit Offset (displacement)
N = 1 for Byte, 2 for Words and 4 for Long Words
$\leftarrow$ = Replaces

The MC68000 instruction set is shown in Table 2. Some additional instructions are variations, or subsets, of these and they appear in Table 3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations, BCD arithmetic and expanded operations (through traps).

**TABLE 2 — INSTRUCTION SET**

| Mnemonic | Description | Mnemonic | Description | Mnemonic | Description |
|----------|-------------|----------|-------------|----------|-------------|
| ABCD | Add Decimal with Extend | EOR | Exclusive Or | PEA | Push Effective Address |
| ADD | Add | EXG | Exchange Registers | RESET | Reset External Devices |
| AND | Logical And | EXT | Sign Extend | ROL | Rotate Left without Extend |
| ASL | Arithmetic Shift Left | JMP | Jump | ROR | Rotate Right without Extend |
| ASR | Arithmetic Shift Right | JSR | Jump to Subroutine | ROXL | Rotate Left with Extend |
| $B_{CC}$ | Branch Conditionally | LEA | Load Effective Address | ROXR | Rotate Right with Extend |
| BCHG | Bit Test and Change | LINK | Link Stack | RTE | Return from Exception |
| BCLR | Bit Test and Clear | LSL | Logical Shift Left | RTR | Return and Restore |
| BRA | Branch Always | LSR | Logical Shift Right | RTS | Return from Subroutine |
| BSET | Bit Test and Set | MOVE | Move | SBCD | Subtract Decimal with Extend |
| BSR | Branch to Subroutine | MOVEM | Move Multiple Registers | $S_{CC}$ | Set Conditional |
| BTST | Bit Test | MOVEP | Move Peripheral Data | STOP | Stop |
| CHK | Check Register Against Bounds | MULS | Signed Multiply | SUB | Subtract |
| CLR | Clear Operand | MULU | Unsigned Multiply | SWAP | Swap Data Register Halves |
| CMP | Compare | NBCD | Negate Decimal with Extend | TAS | Test and Set Operand |
| $DB_{CC}$ | Test Condition, Decrement and Branch | NEG | Negate | TRAP | Trap |
| | | NOP | No Operation | TRAPV | Trap on Overflow |
| DIVS | Signed Divide | NOT | One's Complement | TST | Test |
| DIVU | Unsigned Divide | OR | Logical Or | UNLK | Unlink |

**TABLE 3 — VARIATIONS OF INSTRUCTION TYPES**

| Instruction Type | Variation | Description | Instruction Type | Variation | Description |
|------------------|-----------|-------------|------------------|-----------|-------------|
| ADD | ADD | Add | MOVE | MOVE | Move |
| | ADDA | Add Address | | MOVEA | Move Address |
| | ADDQ | Add Quick | | MOVEQ | Move Quick |
| | ADDI | Add Immediate | | MOVE from SR | Move from Status Register |
| | ADDX | Add with Extend | | MOVE to SR | Move to Status Register |
| AND | AND | Logical And | | MOVE to CCR | Move to Condition Codes |
| | ANDI | And Immediate | | MOVE USP | Move User Stack Pointer |
| CMP | CMP | Compare | NEG | NEG | Negate |
| | CMPA | Compare Address | | NEGX | Negate with Extend |
| | CMPM | Compare Memory | OR | OR | Logical Or |
| | CMPI | Compare Immediate | | ORI | Or Immediate |
| EOR | EOR | Exclusive Or | SUB | SUB | Subtract |
| | EORI | Exclusive Or Immediate | | SUBA | Subtract Address |
| | | | | SUBI | Subtract Immediate |
| | | | | SUBQ | Subtract Quick |
| | | | | SUBX | Subtract with Extend |

## DATA ORGANIZATION AND ADDRESSING CAPABILITIES

The following paragraphs describe the data organization and addressing capabilities of the MC68000.

### OPERAND SIZE

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. All explicit instructions support byte, word or long word operands. Implicit instructions support some subset of all three sizes.

### DATA ORGANIZATION IN REGISTERS

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers together with the active stack pointer support address operands of 32 bits.

**DATA REGISTERS.** Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31.

When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high-order portion is neither used nor changed.

**ADDRESS REGISTERS.** Each address register and the stack pointer is 32 bits wide and holds a full 32 bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

### DATA ORGANIZATION IN MEMORY

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in Figure 1. The low order byte has an odd address that is one count higher than the word address. Instructions and multibyte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address n + 2.

The data types supported by the MC68000 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in Figure 2.

### ADDRESSING

Instructions for the MC68000 contain two kinds of information: the type of function to be performed, and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

  Register Specification — the number of the register is given in the register field of the instruction.

  Effective Address — use of the different effective address modes

  Implicit Reference — the definition of certain instructions implies the use of specific registers.

FIGURE 1 — WORD ORGANIZATION IN MEMORY
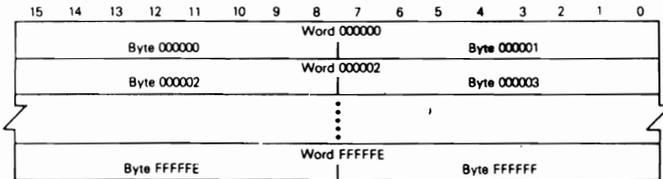
## FIGURE 2 — DATA·ORGANIZATION IN MEMORY

**Bit Data**
1 Byte = 8 Bits

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
|   |   |   |   |   |   |   |   |
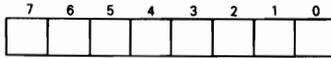
**Integer Data**
1 Byte = 8 Bits

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| MSB | | Byte 0 | | | | | LSB | | | Byte 1 | | | | | |
| | | Byte 2 | | | | | | | | Byte 3 | | | | | |

**1 Word = 16 Bits**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | Word 0 | | | | | | | | LSB |
| | | | | | | | Word 1 | | | | | | | | |
| | | | | | | | Word 2 | | | | | | | | |

**1 Long Word = 32 Bits**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | High Order | | | | | | | | |
| — Long Word 0 — | | | | | | | Low Order | | | | | | | | LSB |
| — Long Word 1 — | | | | | | | | | | | | | | | |
| — Long Word 2 — | | | | | | | | | | | | | | | |
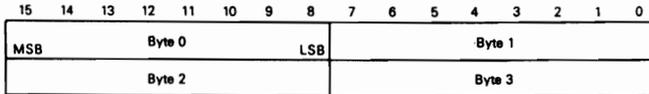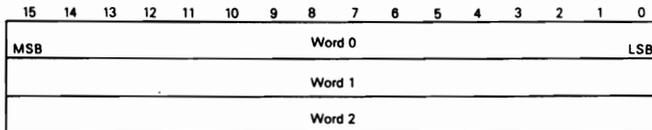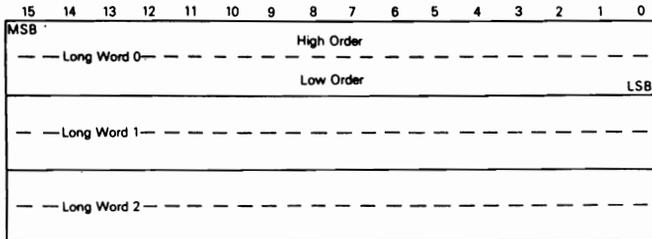
**Addresses**
1 Address = 32 Bits

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | High Order | | | | | | | | |
| — Address 0 — | | | | | | | Low Order | | | | | | | | LSB |
| — Address 1 — | | | | | | | | | | | | | | | |
| — Address 2 — | | | | | | | | | | | | | | | |
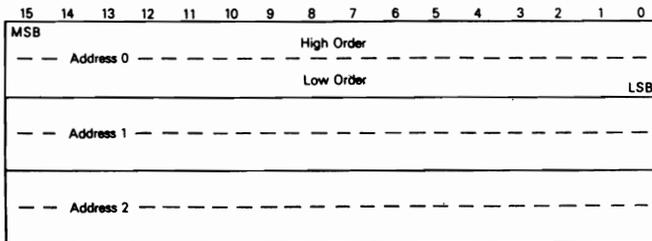
MSB = Most Significant Bit
LSB = Least Significant Bit

**Decimal Data**
2 Binary Coded Decimal Digits = 1 Byte

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| MSD | | BCD 0 | | | BCD 1 | | LSD | | BCD 2 | | | | BCD 3 | | |
| | | BCD 4 | | | BCD 5 | | | | BCD 6 | | | | BCD 7 | | |
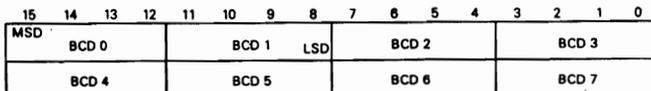
MSD = Most Significant Digit
LSD = Least Significant Digit

## INSTRUCTION FORMAT

Instructions are from one to five words in length, as shown in Figure 3. The length of the instruction and the operation to be performed is specified by the first word of the instruction which is called the operation word. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

## PROGRAM/DATA REFERENCES

The MC68000 separates memory references into two classes: program references, and data references. Program references, as the name implies, are references to that section of memory that contains the program being executed. Data references refer to that section of memory that contains data. Generally, operand reads are from the data space. All operand writes are to the data space.

## REGISTER SPECIFICATION

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

## EFFECTIVE ADDRESS

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 4 shows the general format of the single effective address instruction operation word. The effective address is composed of two 3-bit fields: the mode field, and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 3. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

**REGISTER DIRECT MODES.** These effective addressing modes specify that the operand is in one of the 16 multifunction registers.

**Data Register Direct.** The operand is in the data register specified by the effective address register field.

**Address Register Direct.** The operand is in the address register specified by the effective address register field.

**MEMORY ADDRESS MODES.** These effective addressing modes specify that the operand is in memory and provide the specific address of the operand.

**Address Register Indirect.** The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

**Address Register Indirect With Postincrement.** The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two, or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

**Address Register Indirect With Predecrement.** The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

**Address Register Indirect With Displacement.** This address mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

**Address Register Indirect With Index.** This address mode requires one word of extension. The address of the operand

### FIGURE 3 — INSTRUCTION FORMAT

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Operation Word (First Word Specifies Operation and Modes) | | | | | | | | | | | | | | | |
| Immediate Operand (If Any, One or Two Words) | | | | | | | | | | | | | | | |
| Source Effective Address Extension (If Any, One or Two Words) | | | | | | | | | | | | | | | |
| Destination Effective Address Extension (If Any, One or Two Words) | | | | | | | | | | | | | | | |
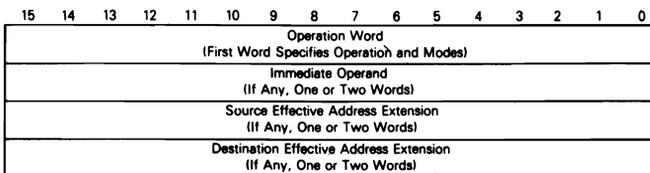
### FIGURE 4 — SINGLE-EFFECTIVE-ADDRESS INSTRUCTION OPERATION WORD GENERAL FORMAT

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X | X | X | Effective Address | | | | | |
| | | | | | | | | | | Mode | | | Register | | |
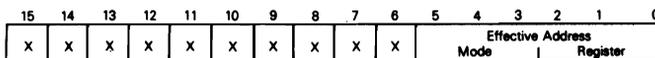
is the sum of the address in the address register, the sign-extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

**SPECIAL ADDRESS MODES.** The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

**Absolute Short Address.** This address mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

**Absolute Long Address.** This address mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the address is the second extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

**Program Counter With Displacement.** This address mode requires one word of extension. The address of the operand is the sum of the address in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference is classified as a program reference.

**Program Counter With Index.** This address mode requires one word of extension. The address is the sum of the address in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference is classified as a program reference.

**Immediate Data.** This address mode requires either one or two words of extension depending on the size of the operation.

    Byte operation — operand is low order byte of extension word

    Word operation — operand is extension word

    Long word operation — operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

**Condition Codes or Status Register.** A selected set of instructions may reference the status register by means of the effective address field. These are:

    ANDI to CCR
    ANDI to SR
    EORI to CCR
    EORI to SR
    ORI to CCR
    ORI to SR

**EFFECTIVE ADDRESS ENCODING SUMMARY**

Table 4 is a summary of the effective addressing modes discussed in the previous paragraphs.

**IMPLICIT REFERENCE**

Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR). Table 5 provides a list of these instructions and the registers implied.

**SYSTEM STACK.** The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state, SSP is the active system stack pointer, and the USP cannot be referenced as an address register. If the S-bit indicates user state, the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

**TABLE 4 — EFFECTIVE ADDRESS ENCODING SUMMARY**

| Addressing Mode | Mode | Register |
|---|---|---|
| Data Register Direct | 000 | register number |
| Address Register Direct | 001 | register number |
| Address Register Indirect | 010 | register number |
| Address Register Indirect with Postincrement | 011 | register number |
| Address Register Indirect with Predecrement | 100 | register number |
| Address Register Indirect with Displacement | 101 | register number |
| Address Register Indirect with Index | 110 | register number |
| Absolute Short | 111 | 000 |
| Absolute Long | 111 | 001 |
| Program Counter with Displacement | 111 | 010 |
| Program Counter with Index | 111 | 011 |
| Immediate or Status Register | 111 | 100 |

**TABLE 5 — IMPLICIT INSTRUCTION REFERENCE SUMMARY**

| Instruction | Implied Register(s) |
|---|---|
| Branch Conditional (B$_{CC}$), Branch Always (BRA) | PC |
| Branch to Subroutine (BSR) | PC, SP |
| Check Register against Bounds (CHK) | SSP, SR |
| Test Condition, Decrement and Branch (DB$_{CC}$) | PC |
| Signed Divide (DIVS) | SSP, SR |
| Unsigned Divide (DIVU) | SSP, SR |
| Jump (JMP) | PC |
| Jump to Subroutine (JSR) | PC, SP |
| Link and Allocate (LINK) | SP |
| Move Condition Codes (MOVE CCR) | SR |
| Move Status Register (MOVE SR) | SR |
| Move User Stack Pointer (MOVE USP) | USP |
| Push Effective Address (PEA) | SP |
| Return from Exception (RTE) | PC, SP, SR |
| Return and Restore Condition Codes (RTR) | PC, SP, SR |
| Return from Subroutine (RTS) | PC, SP |
| Trap (TRAP) | SSP, SR |
| Trap on Overflow (TRAPV) | SSP, SR |
| Unlink (UNLK) | SP |

# INSTRUCTION SET SUMMARY

The following paragraphs contain an overview of the form and structure of the MC68000 instruction set. The instructions form a set of tools that include all the machine functions to perform the following operations:

Data Movement
Integer Arithmetic
Logical
Shift and Rotate
Bit Manipulation
Binary Coded Decimal
Program Control
System Control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

## DATA MOVEMENT OPERATIONS

The basic method of data acquisition (transfer and storage) is provided by the move (MOVE) instruction. The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 6 is a summary of the data movement operations

### TABLE 6 — DATA MOVEMENT OPERATIONS

| Instruction | Operand Size | Operation |
|---|---|---|
| EXG | 32 | Rx ↔ Ry |
| LEA | 32 | EA → An |
| LINK | — | An → SP@ − <br> SP → An <br> SP + d → SP |
| MOVE | 8, 16, 32 | (EA)s → EAd |
| MOVEM | 16, 32 | (EA) → An, Dn <br> An, Dn → EA |
| MOVEP | 16, 32 | (EA) → Dn <br> Dn → EA |
| MOVEQ | 8 | #xxx → Dn |
| PEA | 32 | EA → SP@ − |
| SWAP | 32 | Dn[31:16] ↔ Dn[15:0] |
| UNLK | — | An → Sp <br> SP@ + → An |

NOTES:
s = source
d = destination
[ ] = bit numbers
@ − = indirect with predecrement
@ + = indirect with postdecrement

## INTEGER ARITHMETIC OPERATIONS

The arithmetic operations include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, with data operations accepting all operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be used on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long word product, and a long word dividend with word divisor to produce a word quotient with a word remainder.

Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A test operand (TST) instruction that will set the condition codes as a result of a compare of the operand with zero is also available. Test and set (TAS) is a synchronization instruction useful in multiprocessor systems. Table 7 is a summary of the integer arithmetic operations

### TABLE 7 — INTEGER ARITHMETIC OPERATIONS

| Instruction | Operand Size | Operation |
|---|---|---|
| ADD | 8, 16, 32 <br><br> 16, 32 | Dn + (EA) → Dn <br> (EA) + Dn → EA <br> (EA) + #xxx → EA <br> An + (EA) → An |
| ADDX | 8, 16, 32 <br> 16, 32 | Dx + Dy + X → Dx <br> Ax@ − Ay@ − + X → Ax@ |
| CLR | 8, 16, 32 | 0 → EA |
| CMP | 8, 16, 32 <br><br><br> 16, 32 | Dn − (EA) <br> (EA) − #xxx <br> Ax@ + − Ay@ + <br> An − (EA) |
| DIVS | 32 ÷ 16 | Dn/(EA) → Dn |
| DIVU | 32 ÷ 16 | Dn/(EA) → Dn |
| EXT | 8 → 16 <br> 16 → 32 | (Dn)8 → Dn16 <br> (Dn)16 → Dn32 |
| MULS | 16*16 → 32 | Dn*(EA) → Dn |
| MULU | 16*16 → 32 | Dn*(EA) → Dn |
| NEG | 8, 16, 32 | 0 − (EA) → EA |
| NEGX | 8, 16, 32 | 0 − (EA) − X → EA |
| SUB | 8, 16, 32 <br><br><br> 16, 32 | Dn − (EA) → Dn <br> (EA) − Dn → EA <br> (EA) − #xxx → EA <br> An − (EA) → An |
| SUBX | 8, 16, 32 | Dx − Dy − X → Dx <br> Ax@ − Ay@ − − X → Ax@ |
| TAS | 8 | (EA) − 0, 1 → EA[7] |
| TST | 8, 16, 32 | (EA) − 0 |

NOTE: [ ] = bit number

## LOGICAL OPERATIONS

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provide these logical operations with all sizes of immediate data. Table 8 is a summary of the logical operations.

**TABLE 8 — LOGICAL OPERATIONS**

| Instruction | Operand Size | Operation |
|---|---|---|
| AND | 8, 16, 32 | Dn∧(EA) → Dn<br>(EA)∧Dn → EA<br>(EA)∧#xxx → EA |
| OR | 8, 16, 32 | Dn v (EA) → Dn<br>(EA) v Dn → EA<br>(EA) v #xxx → EA |
| EOR | 8, 16, 32 | (EA) ● Dy → EA<br>(EA) ● #xxx → EA |
| NOT | 8, 16, 32 | ~ (EA) → EA |

NOTE: ~ = invert

## SHIFT AND ROTATE OPERATIONS

Shift operations in both directions are provided by the arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in the instruction of one to eight bits, or 0 to 63 specified in a data register.

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 9 is a summary of the shift and rotate operations.

**TABLE 9 — SHIFT AND ROTATE OPERATIONS**



## BIT MANIPULATION OPERATIONS

Bit manipulation operations are accomplished using the following instructions: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 10 is a summary of the bit manipulation operations. (Bit 2 of the status register is Z.)

**TABLE 10 — BIT MANIPULATION OPERATIONS**

| Instruction | Operand Size | Operation |
|---|---|---|
| BTST | 8, 32 | ~ bit of (EA) → Z |
| BSET | 8, 32 | ~ bit of (EA) → Z<br>1 → bit of EA |
| BCLR | 8, 32 | ~ bit of (EA) → Z<br>0 → bit of EA |
| BCHG | 8, 32 | ~ bit of (EA) → Z<br>~ bit of (EA) → bit of EA |

## BINARY CODED DECIMAL OPERATIONS

Multiprecision arithmetic operations on binary coded decimal numbers are accomplished using the following instructions: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 11 is a summary of the binary coded decimal operations.

**TABLE 11 — BINARY CODED DECIMAL OPERATIONS**

| Instruction | Operand Size | Operation |
|---|---|---|
| ABCD | 8 | $Dx_{10} + Dy_{10} + X$ → Dx<br>$Ax@ - 10 + Ay@ - 10 + X$ → Ax@ |
| SBCD | 8 | $Dx_{10} - Dy_{10} - X$ → Dx<br>$Ax@ - 10 - Ay@ - 10 - X$ → Ax@ |
| NBCD | 8 | $0 - (EA)_{10} - X$ → EA |

## PROGRAM CONTROL OPERATIONS

Program control operations are accomplished using a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 12.

The conditional instructions provide setting and branching for the following conditions:

| | | | |
|---|---|---|---|
| CC | – carry clear | LS | – low or same |
| CS | – carry set | LT | – less than |
| EQ | – equal | MI | – minus |
| F | – never true | NE | – not equal |
| GE | – greater or equal | PL | – plus |
| GT | – greater than | T | – always true |
| HI | – high | VC | – no overflow |
| LE | – less or equal | VS | – overflow |

## TABLE 12 — PROGRAM CONTROL OPERATIONS

| Instruction | Operation |
|---|---|
| **Conditional** | |
| B$_{CC}$ | Branch conditionally (14 conditions) 8- and 16-bit displacement |
| DB$_{CC}$ | Test condition, decrement, and branch 16-bit displacement |
| S$_{CC}$ | Set byte conditionally (16 conditions) |
| **Unconditional** | |
| BRA | Branch always 3- and 16-bit displacement |
| BSR | Branch to subroutine 8- and 16-bit displacement |
| JMP | Jump |
| JSR | Jump to subroutine |
| **Returns** | |
| RTR | Return and restore condition codes |
| RTS | Return from subroutine |

## TABLE 13 — SYSTEM CONTROL OPERATIONS

| Instruction | Operation |
|---|---|
| **Privileged** | |
| RESET | Reset external devices |
| RTE | Return from exception |
| STOP | Stop program execution |
| ORI to SR | Logical OR to status register |
| MOVE USP | Move user stack pointer |
| ANDI to SR | Logical AND to status register |
| EORI to SR | Logical EOR to status register |
| MOVE EA to SR | Load new status register |
| **Trap Generating** | |
| TRAP | Trap |
| TRAPV | Trap on overflow |
| CHK | Check register against bounds |
| **Status Register** | |
| ANDI to CCR | Logical AND to condition codes |
| EORI to CCR | Logical EOR to condition codes |
| MOVE EA to CCR | Load new condition codes |
| ORI to CCR | Logical OR to condition codes |
| MOVE SR to EA | Store status register |

## SYSTEM CONTROL OPERATIONS

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 13.

## SIGNAL AND BUS OPERATION DESCRIPTION

The following paragraphs contain a brief description of the input and output signals. A discussion of bus operation during the various machine cycles and operations is also given.

### SIGNAL DESCRIPTION

The input and output signals can be functionally organized into the groups shown in Figure 5. The following paragraphs provide a brief description of the signals and also a reference (if applicable) to other paragraphs that contain more detail about the function being performed.

**ADDRESS BUS (A1 THROUGH A23).** This 23-bit, unidirectional, three-state bus is capable of addressing 8 megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are all set to a logic high.

**DATA BUS (D0 THROUGH D15).** This 16-bit, bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-D7.

**ASYNCHRONOUS BUS CONTROL.** Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

### FIGURE 5 — INPUT AND OUTPUT SIGNALS
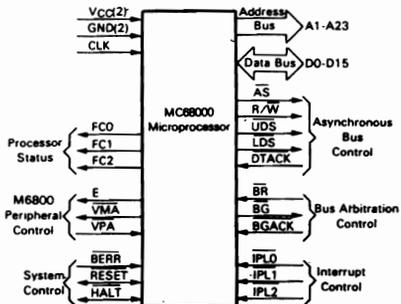


**Address Strobe ($\overline{AS}$).** This signal indicates that there is a valid address on the address bus.

**Read/Write (R/$\overline{W}$).** This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

**Upper And Lower Data Strobes ($\overline{UDS}$, $\overline{LDS}$).** These signals control the data on the data bus, as shown in Table 14. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/$\overline{W}$ line is low, the processor will write to the data bus as shown.

TABLE 14 — DATA STROBE CONTROL OF DATA BUS

| $\overline{UDS}$ | $\overline{LDS}$ | R/$\overline{W}$ | D8-D15 | D0-D7 |
|------|------|------|--------|-------|
| High | High | — | No valid data | No valid data |
| Low | Low | High | Valid data bits 8-15 | Valid data bits 0-7 |
| High | Low | High | No valid data | Valid data bits 0-7 |
| Low | High | High | Valid data bits 8-15 | No valid data |
| Low | Low | Low | Valid data bits 8-15 | Valid data bits 0-7 |
| High | Low | Low | Valid data bits 0-7* | Valid data bits 0-7 |
| Low | High | Low | Valid data bits 8-15 | Valid data bits 8-15* |

*These conditions are a result of current implementation and may not appear on future devices.

**Data Transfer Acknowledge ($\overline{DTACK}$).** This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

**BUS ARBITRATION CONTROL.** These three signals form a bus arbitration circuit to determine which device will be the bus master device.

**Bus Request ($\overline{BR}$).** This input is wire ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master

**Bus Grant ($\overline{BG}$).** This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

**Bus Grant Acknowledge ($\overline{BGACK}$).** This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

1. a bus grant has been received
2. address strobe is inactive which indicates that the microprocessor is not using the bus

3. data transfer acknowledge is inactive which indicates that either memory or the peripherals are not using the bus
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership.

**INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$).** These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is given in $\overline{IPL0}$ and the most significant bit is contained in $\overline{IPL2}$.

**SYSTEM CONTROL.** The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

**Bus Error ($\overline{BERR}$).** This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices
2. interrupt vector number acquisition failure
3. illegal access request as determined by a memory management unit
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retried.

Refer to **BUS ERROR AND HALT OPERATION** paragraph for additional information about the interaction of the bus error and halt signals.

**Reset ($\overline{RESET}$).** This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of a RESET instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external halt and reset signals applied at the same time. Refer to **RESET OPERATION** paragraph for additional information about reset operation.

**Halt ($\overline{HALT}$).** When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state. Refer to **BUS ERROR AND HALT OPERATION** paragraph for additional information about the interaction between the halt and bus error signals.

When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

**M6800 PERIPHERAL CONTROL.** These control signals are used to allow the interfacing of synchronous M6800 peripheral devices with the asynchronous MC68000 These signals are explained in the following paragraphs

**Enable (E).** This signal is the standard enable signal common to all M6800 type peripheral devices. The period for this output is ten MC68000 clock periods (six clocks low, four clocks high).

**Valid Peripheral Address ($\overline{VPA}$).** This input indicates that the device or region addressed is a M6800 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt Refer to **INTERFACE WITH M6800 PERIPHERALS**.

**Valid Memory Address ($\overline{VMA}$).** This output is used to indicate to M6800 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address ($\overline{VPA}$) input which indicates that the peripheral is a M6800 family device.

**PROCESSOR STATUS (FC0, FC1, FC2).** These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 15. The information indicated by the function code outputs is valid whenever address strobe ($\overline{AS}$) is active.

**TABLE 15 — FUNCTION CODE OUTPUTS**

| FC2 | FC1 | FC0 | Cycle Type |
|-----|-----|-----|------------|
| Low | Low | Low | (Undefined, Reserved) |
| Low | Low | High | User Data |
| Low | High | Low | User Program |
| Low | High | High | (Undefined, Reserved) |
| High | Low | Low | (Undefined, Reserved) |
| High | Low | High | Supervisor Data |
| High | High | Low | Supervisor Program |
| High | High | High | Interrupt Acknowledge |

**CLOCK (CLK).** The clock input is a TTL compatible signal that is internally buffered for development of the internal clocks needed by the processor The clock input shall be a constant frequency.

**SIGNAL SUMMARY.** Table 16 is a summary of all the signals discussed in the previous paragraphs.

**TABLE 16 — SIGNAL SUMMARY**

| Signal Name | Mnemonic | Input/Output | Active State | Three State |
|-------------|----------|--------------|--------------|-------------|
| Address Bus | A1-A23 | output | high | yes |
| Data Bus | D0-D15 | input/output | high | yes |
| Address Strobe | $\overline{AS}$ | output | low | yes |
| Read/Write | R/$\overline{W}$ | output | read-high write-low | yes |
| Upper and Lower Data Strobes | $\overline{UDS}$, $\overline{LDS}$ | output | low | yes |
| Data Transfer Acknowledge | $\overline{DTACK}$ | input | low | no |
| Bus Request | $\overline{BR}$ | input | low | no |
| Bus Grant | $\overline{BG}$ | output | low | no |
| Bus Grant Acknowledge | $\overline{BGACK}$ | input | low | no |
| Interrupt Priority Level | $\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$ | input | low | no |
| Bus Error | $\overline{BERR}$ | input | low | no |
| Reset | $\overline{RESET}$ | input/output | low | no* |
| Halt | $\overline{HALT}$ | input/output | low | no* |
| Enable | E | output | high | no |
| Valid Memory Address | $\overline{VMA}$ | output | low | yes |
| Valid Peripheral Address | $\overline{VPA}$ | input | low | no |
| Function Code Output | FC0, FC1, FC2 | output | high | yes |
| Clock | CLK | input | high | no |
| Power Input | $V_{CC}$ | input | – | – |
| Ground | GND | input | – | – |

*open drain

## BUS OPERATION

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

**DATA TRANSFER OPERATIONS.** Transfer of data between devices involves the following leads:

- Address Bus A1 through A23
- Data Bus D0 through D15
- Control Signals

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the MC68000 for interlocked multiprocessor communications.

### NOTE

The terms **assertion** and **negation** will be used extensively. This is done to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The term assert or assertion is used to indicate that a signal is active or true independent of whether that voltage is low or high. The term negate or negation is used to indicate that a signal is inactive or false.

**Read Cycle.** During a read cycle, the processor receives data from memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both bytes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions it internally.

A word read cycle flow chart is given in Figure 6. A byte read cycle flow chart is given in Figure 7. Read cycle timing is given in Figure 8 and Figure 9 details word and byte read cycle operation.

### FIGURE 6 — WORD READ CYCLE FLOW CHART

| BUS MASTER | SLAVE |
|---|---|

**Address Device**
1) Set R/$\overline{W}$ to Read
2) Place Address on A1-A23
3) Place Function Code on FC0-FC2
4) Assert Address Strobe ($\overline{AS}$)
5) Assert Upper Data Strobe ($\overline{UDS}$) and Lower Data Strobe ($\overline{LDS}$)

**Input Data**
1) Decode Address
2) Place Data on D0-D15
3) Assert Data Transfer Acknowledge ($\overline{DTACK}$)

**Acquire Data**
1) Latch Data
2) Negate $\overline{UDS}$ and $\overline{LDS}$
3) Negate $\overline{AS}$

**Terminate Cycle**
1) Remove Data from D0-D15
2) Negate $\overline{DTACK}$

**Start Next Cycle**

### FIGURE 7 — BYTE READ CYCLE FLOW CHART

| BUS MASTER | SLAVE |
|---|---|

**Address Device**
1) Set R/$\overline{W}$ to Read
2) Place Address on A1-A23
3) Place Function Code on FC0-FC2
4) Assert Address Strobe ($\overline{AS}$)
5) Assert Upper Data Strobe ($\overline{UDS}$) or Lower Data Strobe ($\overline{LDS}$) (based on A0)

**Input Data**
1) Decode Address
2) Place Data on D0-D7 or D8-D15 (based on $\overline{UDS}$ or $\overline{LDS}$)
3) Assert Data Transfer Acknowledge ($\overline{DTACK}$)

**Acquire Data**
1) Latch Data
2) Negate $\overline{UDS}$ or $\overline{LDS}$
3) Negate $\overline{AS}$

**Terminate Cycle**
1) Remove Data from D0-D7 or D8-D15
2) Negate $\overline{DTACK}$

**Start Next Cycle**

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FIGURE 8 — READ AND WRITE CYCLE TIMING DIAGRAM

CLK

A4-A23

A1-A3

addr. stobe $\overline{AS}$

upper/lower data strobe $\overline{UDS}$

$\overline{LDS}$

R/$\overline{W}$

$\overline{DTACK}$

DB-D15

D0-D7

FCO-2

|← — — -Read— — →|← — — —Write- — — →|← — — — -Slow Read— — —→|
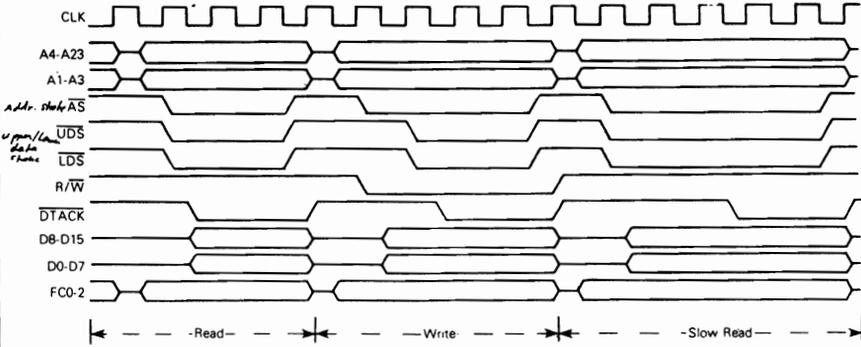
FIGURE 9 — WORD AND BYTE READ CYCLE TIMING DIAGRAM

CLK

A4-A23

A1-A3

A0*

$\overline{AS}$

$\overline{UDS}$

$\overline{LDS}$

R/$\overline{W}$

$\overline{DTACK}$

D8-D15

D0-D7

FCO-2

*Internal Signal Only

|← — -Word Read- — →|← — Odd Byte Read— →|← —Even Byte Read — →|
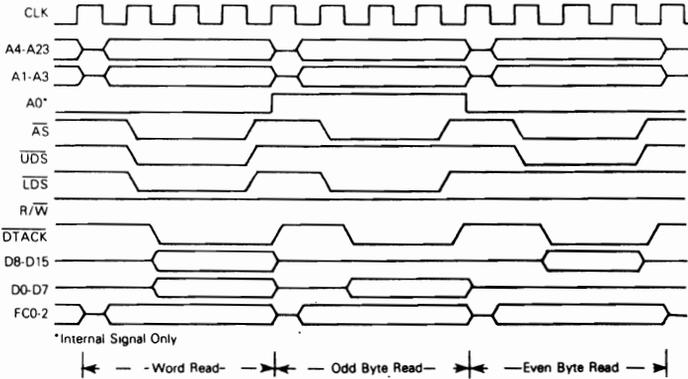
**Write Cycle.** During a write cycle, the processor sends data to memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte For byte opera-

tions, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. A word write cycle flow chart is given in Figure 10. A byte write cycle flow chart is given in Figure 11. Write cycle timing is given in Figure 8 and Figure 12 details word and byte write cycle operation.

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### FIGURE 10 — WORD WRITE CYCLE FLOW CHART

| BUS MASTER | SLAVE |
|---|---|

**Address Device**

1) Place Address on A1-A23
2) Place Function Code on FC0-FC2
3) Assert Address Strobe (AS)
4) Set R/W to Write
5) Place Data on D0-D15
6) Assert Upper Data Strobe (UDS) and Lower Data Strobe (LDS)

**Input Data**

1) Decode Address
2) Store Data on D0-D15
3) Assert Data Transfer Acknowledge (DTACK)

**Terminate Output Transfer**

1) Negate UDS and LDS
2) Negate AS
3) Remove Data from D0-D15
4) Set R/W to Read

**Terminate Cycle**

1) Negate DTACK

**Start Next Cycle**

### FIGURE 11 — BYTE WRITE CYCLE FLOW CHART

| BUS MASTER | SLAVE |
|---|---|

**Address Device**

1) Place Address on A1-A23
2) Place Function Code on FC0-FC2
3) Assert Address Strobe (AS)
4) Set R/W to Write
5) Place Data on D0-D7 or D8-D15 (according to A0)
6) Assert Upper Data Strobe (UDS) or Lower Data Strobe (LDS) (based on A0)

**Input Data**

1) Decode Address
2) Store Data on D0-D7 if LDS is asserted
   Store Data on D8-D15 if UDS is asserted
3) Assert Data Transfer Acknowledge (DTACK)

**Terminate Output Transfer**

1) Negate UDS and LDS
2) Negate AS
3) Remove Data from D0-D7 or D8-D15
4) Set R/W to Read

**Terminate Cycle**

1) Negate DTACK

**Start Next Cycle**

### FIGURE 12 — WORD AND BYTE WRITE CYCLE TIMING DIAGRAM

CLK

A4-A23

A1-A3

A0*

AS

UDS

LDS

R/W

DTACK

D8-D15

D0-D7

FC0-2

*Internal Signal Only

|← — —Word Write— — →|← — ·Odd Byte Write — →|← — Even Byte Write— — →|

**Read-Modify-Write Cycle.** The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the MC68000 this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write cycles are byte operations. A read-modify-write cycle flow chart is given in Figure 13 and a timing diagram is given in Figure 14.

**FIGURE 13 — READ-MODIFY-WRITE CYCLE FLOW CHART**

BUS MASTER                                                                    SLAVE

Address Device
1) Place Address on A1-A23
2) Set R/$\overline{W}$ to Read
3) Assert Address Strobe ($\overline{AS}$)
4) Assert Upper Data Strobe ($\overline{UDS}$) or Lower Data Strobe ($\overline{LDS}$)

                                                                    Input Data
                                                        1) Decode Address
                                                        2) Place Data on D0-D7 or D8-D15
                                                        3) Assert Data Transfer Acknowledge
                                                           ($\overline{DTACK}$)

Acquire Data
1) Latch Data
2) Negate $\overline{UDS}$ or $\overline{LDS}$
3) Start Data Modification

                                                                    Terminate Cycle
                                                        1) Remove Data from D0-D7 or D8-D15
                                                        2) Negate DTACK

Start Output Transfer
1) Set R/$\overline{W}$ to Write
2) Place Data on D0-D7 or D8-D15
3) Assert Upper Data Strobe ($\overline{UDS}$) or Lower Data Strobe ($\overline{LDS}$)

                                                                    Input Data
                                                        1) Store Data on D0-D7 or D8-D15
                                                        2) Assert Data Transfer Acknowledge
                                                           ($\overline{DTACK}$)

Terminate Output Transfer
1) Negate $\overline{UDS}$ or $\overline{LDS}$
2) Negate $\overline{AS}$
3) Remove Data from D0-D7 or D8-D15
4) Set R/$\overline{W}$ to Read

                                                                    Terminate Cycle
                                                        1) Negate $\overline{DTACK}$

Start Next Cycle

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**FIGURE 14 — READ-MODIFY-WRITE CYCLE TIMING DIAGRAM**
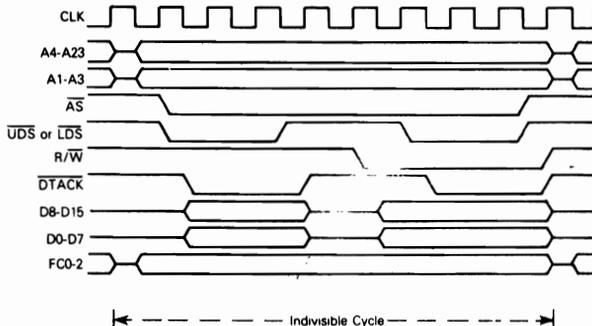


**BUS ARBITRATION.** Bus arbitration is a technique used by master-type devices to request, be granted, and acknowledge bus mastership. In its simplest form, it consists of:

1. Asserting a bus mastership request.
2. Receiving a grant that the bus is available at the end of the current cycle.
3. Acknowledging that mastership has been assumed.

Figure 15 is a flow chart showing the detail involved in a request from a single device. Figure 16 is a timing diagram for the same operations. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated at the time that an acknowledge is asserted. This type of operation would be true for a system consisting of the processor and one device capable of bus mastership. In systems having a number of devices capable of bus mastership, the bus request line from each device is wire ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signal is negated a few clock cycles after the transition of the acknowledge ($\overline{BGACK}$) signal.

However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after it was negated. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

**FIGURE 15 — BUS ARBITRATION CYCLE FLOW-CHART**
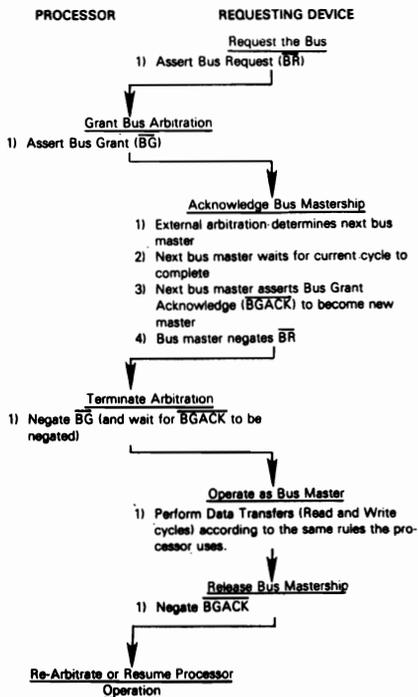
**FIGURE 16 — BUS ARBITRATION CYCLE TIMING DIAGRAM**
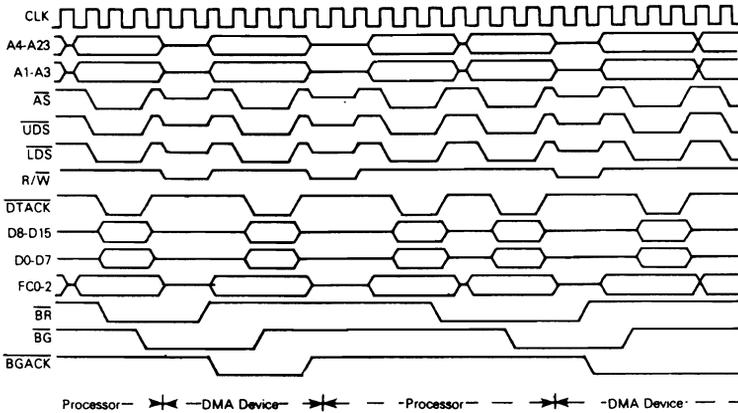


**Requesting the Bus.** External devices capable of becoming bus masters request the bus by asserting the bus request (BR) signal. This is a wire ORed signal (although it need not be constructed from open collector devices) that indicates to the processor that some external device requires control of the external bus. The processor is effectively at a lower bus priority level than the external device and will relinquish the bus after it has completed the last bus cycle it has started.

When no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry responded to noise inadvertently.

**Receiving the Bus Grant.** The processor asserts bus grant (BG) as soon as possible. Normally this is immediately after internal synchronization. The only exception to this occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe (AS) signal. In this case, bus grant will not be asserted until one clock after address strobe is asserted to indicate to external devices that a bus cycle is being executed.

The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

**Acknowledgement of Mastership.** Upon receiving a bus grant, the requesting device waits until address strobe, data transfer acknowledge, and bus grant acknowledge are negated before issuing its own BGACK. The negation of the address strobe indicates that the previous master has com-

pleted its cycle, the negation of bus grant acknowledge indicates that the previous master has released the bus. (While address strobe is asserted no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. Note that in some applications data transfer acknowledge might not enter into this function. General purpose devices would then be connected such that they were only dependent on address strobe. When bus grant acknowledge is issued the device is bus master until it negates bus grant acknowledge. Bus grant acknowledge should not be negated until after the bus cycle(s) is (are) completed. Bus mastership is terminated at the negation of bus grant acknowledge.

The bus request from the granted device should be dropped when bus grant acknowledge is asserted. If bus request is still asserted after bus grant acknowledge is negated, the processor performs another arbitration sequence and issues another bus grant. Note that the processor does not perform any external bus cycles before it re-asserts bus grant.

**BUS ERROR AND HALT OPERATION.** In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided. External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

**Exception Sequence.** The bus error exception sequence is entered when the processor receives a bus error signal and the halt pin is inactive. Figure 17 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. Stacking the program counter and status register
2. Stacking the error information
3. Reading the bus error vector table entry
4. Executing the bus error handler routine

The stacking of the program counter and the status register is the same as if an interrupt had occurred. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address $000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to **EXCEPTION PROCESSING** for additional information.

**Re-Running the Bus Cycle.** When the processor receives a bus error signal and the halt pin is being driven by an external device, the processor enters the re-run sequence. Figure 18 is a timing diagram for re-running the bus cycle.

The processor completes the bus cycle, then puts the address, data and function code output lines in the high impedance state. The processor remains "halted," and will not run another bus cycle until the halt signal is removed by external logic. Then the processor will re-run the previous bus cycle using the same address, the same function codes, the same data (for a write operation), and the same controls. The bus error signal should be removed before the halt signal is removed.

FIGURE 17 — BUS ERROR TIMING DIAGRAM
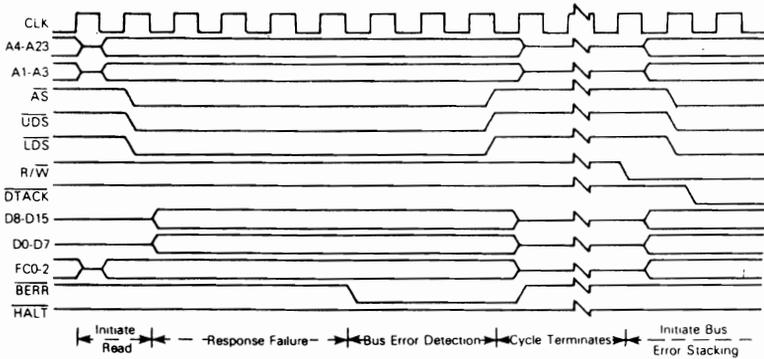


FIGURE 18 — RE-RUN BUS CYCLE TIMING INFORMATION
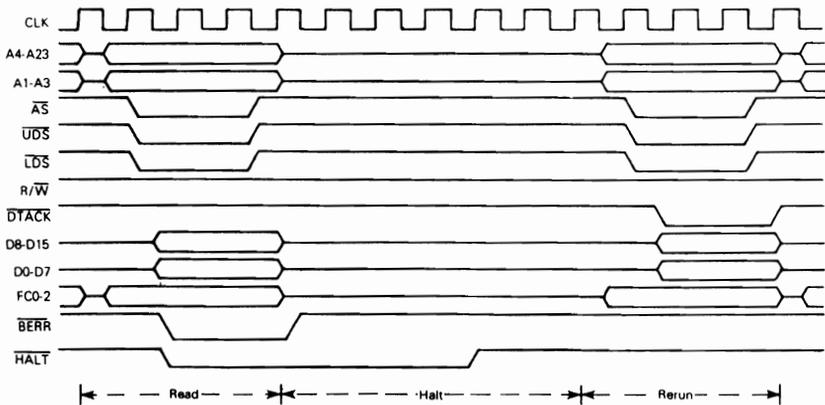
## NOTE

The processor will not re-run a read-modify-write cycle This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a Test-and-Set operation is performed without ever releasing $\overline{AS}$

**Halt Operation with No Bus Error.** The halt input signal to the MC68000 performs a Halt/Run/Single-Step function in a similar fashion to the M6800 halt function The halt and run modes are somewhat self explanatory in that when the halt signal is constantly active the processor "halts" (does nothing) and when the halt signal is constantly inactive the processor "runs" (does something)

The single-step mode is derived from correctly timed transitions on the halt signal input It forces the processor to execute a single bus cycle by entering the "run" mode until the processor starts a bus cycle then changing to the "halt" mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

Figure 19 details the timing required for correct single-step operations Some care must be exercised to avoid harmful interactions between the bus error signal and the halt pin when using the single cycle mode as a debugging tool. This is also true of interactions between the halt and reset lines since these can reset the machine

When the processor completes a bus cycle after recognizing that the halt signal is active, most three-state signals are put in the high-impedance state These include·

1. address lines
2. data lines
3. function code lines

This is required for correct performance of the re-run bus cycle operation

Note that when the processor honors a request to halt, the function codes are put in the high-impedance state (their buffer characteristics are the same as the address buffers) While the processor is honoring the halt request, bus arbitration performs as usual. That is, halting has no effect on bus arbitration It is the bus arbitration function that removes the control signals from the bus

The halt function and the hardware trace capability allow the hardware debugger to trace single bus cycles or single instructions at a time. These processor capabilities, along with a software debugging package, give total debugging flexibility.

**Double Bus Faults.** When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row. This is commonly referred to as a double bus fault. When a double bus fault occurs, the processor will halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

Note that a bus cycle which is re-run does not constitute a bus error exception, and does not contribute to a double bus fault. Note also that this means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor

FIGURE 19 — HALT SIGNAL TIMING CHARACTERISTICS
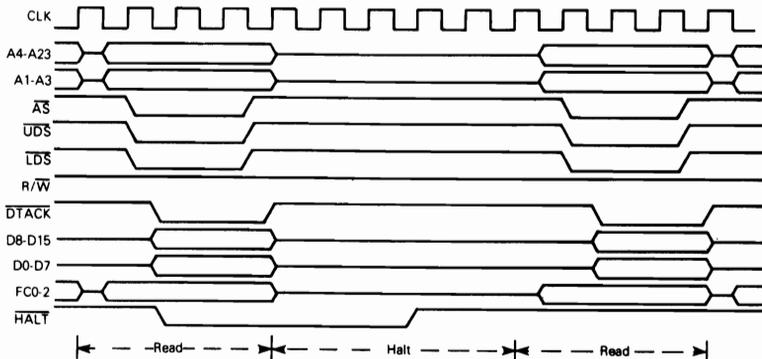
RESET OPERATION. The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system  Figure 20 is a timing diagram for reset operations. Both the halt and the reset lines must be applied to ensure total reset of the processor

When the reset and halt lines are driven by an external device, it is recognized as an entire system reset, including the processor  The processor responds by reading the reset vector table entry (vector number zero, address $0000000) and loads it into the supervisor stack pointer (SSP)  Vector. table entry number one at address $000004 is read next and loaded into the program counter  The processor initializes

the status register to an interrupt level of seven  No other registers are affected by the reset sequence

When a RESET sequence is executed, the processor drives the reset pin for 124 clock pulses  In this case, the processor is trying to reset the rest of the system  Therefore, there is no effect on the internal state of the processor  All of the processor's internal registers and the status register are unaffected by the execution of a RESET instruction  All external devices connected to the reset line should be reset at the completion of the RESET instruction

When $V_{CC}$ is initially applied to the processor, an external reset must be applied to the reset pin for 100 milliseconds

FIGURE 20 — RESET OPERATION TIMING DIAGRAM



NOTES
1) Internal start-up time
2) SSP High read in here
3) SSP Low read in here
4) PC High read in here
5) PC Low read in here
6) First instruction fetched here

Bus State Unknown

All Control Signals Inactive
Data Bus In Read Mode
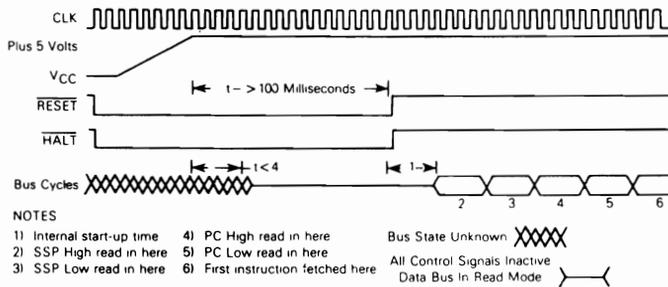
## EXCEPTION PROCESSING

The following paragraphs describe the actions of the MC68000 which are outside the normal processing associated with the execution of instructions. The functions of the bits in the supervisor portion of the status register are covered the supervisor/user bit, the trace enable bit, and the processor interrupt priority mask. Finally, the sequence of memory references and actions taken by the processor on exception conditions is detailed

The halted processing state is an indication of catastrophic hardware failure  For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts  Only an external reset can restart a halted processor  Note that a processor in the stopped state is not in the halted state, nor vice versa

### PROCESSING STATES

The MC68000 is always one of three processing states normal, exception, or halted  The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results  A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further memory references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

### PRIVILEGE STATES

The processor operates in one of two states of privilege the "user" state or the "supervisor" state  The privilege state determines which operations are legal, is used by the external memory management device to control and translate accesses, and is used to choose between the supervisor stack pointer and the user stack pointer in instruction references

The privilege state is a mechanism for providing security in a computer system  Programs should access only their own code and data areas, and ought to be restricted from accessing information which they do not need and must not modify.

The privilege mechanism provides security by allowing most programs to execute in user state  In this state, the accesses are controlled, and the effects on other parts of the system are limited  The operating system executes in the supervisor state, has access to all resources, and performs the overhead tasks for the user state programs.

SUPERVISOR STATE. The supervisor state is the higher state of privilege For instruction execution, the supervisor state is determined by the S-bit of the status register; if the S-bit is asserted (high), the processor is in the supervisor state All instructions can be executed in the supervisor state The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicitly or address register seven explicitly access the supervisor stack pointer

All exception processing is done in the supervisor state, regardless of the setting of the S-bit The bus cycles generated during exception processing are classified as supervisor references All stacking operations during exception processing use the supervisor stack pointer

USER STATE. The user state is the lower state of privilege For instruction execution, the user state is determined by the S-bit of the status register, if the S-bit is negated (low), the processor is executing instructions in the user state.

Most instructions execute the same in user state as in supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole status register are privileged. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in the user privilege state, those instructions which use either the system stack pointer implicitly, or address register seven explicitly, access the user stack pointer

PRIVILEGE STATE CHANGES. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception

processing, the current setting of the S-bit of the status register is saved and the S-bit is asserted, putting the processing in the supervisor state. Therefore, when instruction execution resumes at the address specified to process the exception, the processor is in the supervisor privilege state.

REFERENCE CLASSIFICATION. When the processor makes a reference, it classifies the kind of reference being made, using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 17 lists the classification of references.

TABLE 17 — REFERENCE CLASSIFICATION

| Function Code Output | | | Reference Class |
|---|---|---|---|
| FC2 | FC1 | FC0 | |
| 0 | 0 | 0 | (Unassigned) |
| 0 | 0 | 1 | User Data |
| 0 | 1 | 0 | User Program |
| 0 | 1 | 1 | (Unassigned) |
| 1 | 0 | 0 | (Unassigned) |
| 1 | 0 | 1 | Supervisor Data |
| 1 | 1 | 0 | Supervisor Program |
| 1 | 1 | 1 | Interrupt Acknowledge |

EXCEPTION PROCESSING

Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made, and the status register is set for exception processing. In the second step the exception vector is determined, and the third step is the saving of the current processor context. In the fourth step a new context is obtained, and the processor switches to instruction processing.

EXCEPTION VECTORS. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 21), except for the reset

FIGURE 21 — EXCEPTION VECTOR FORMAT

| Word 0 | New Program Counter (High) | A0 = 0, A1 = 0 |
|---|---|---|
| Word 1 | New Program Counter (Low) | A0 = 0, A1 = 1 |
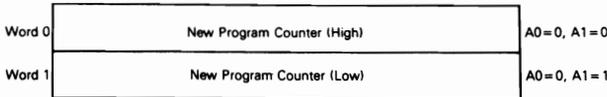
FIGURE 22 — PERIPHERAL VECTOR NUMBER FORMAT

| D.15 | | D8 D7 | | | | | | | D0 |
|---|---|---|---|---|---|---|---|---|---|
| Ignored | | v7 | v6 | v5 | v4 | v3 | v2 | v1 | v0 |
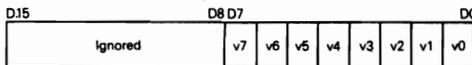
Where:
v7 is the MSB of the Vector Number
v0 is the LSB of the Vector Number

vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an eight-bit number which, when multiplied by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number (Figure 22) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24-bit address, as shown in Figure 23. The memory layout for exception vectors is given in Table 18.

As shown in Table 18, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through address 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, there are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

KINDS OF EXCEPTIONS. Exceptions can be generated by either internal or external causes. The externally generated exceptions are the interrupts and the bus error and reset requests. The interrupts are requests from peripheral devices for processor action while the bus error and reset inputs are used for access control and processor restart. The internally generated exceptions come from instructions, or from ad-

FIGURE 23 — ADDRESS TRANSLATED FROM 8-BIT
VECTOR NUMBER

| A23 | | | | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|-----|---|---|---|-----|----|----|----|----|----|----|----|----|----|----|
| All Zeroes | | | | | v7 | v6 | v5 | v4 | v3 | v2 | v1 | v0 | 0 | 0 |
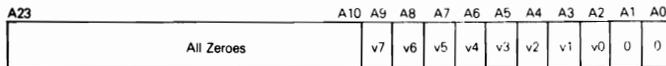
TABLE 18 — EXCEPTION VECTOR ASSIGNMENT

| Vector | Address | | | Assignment |
|--------|---------|---|---|------------|
| Number(s) | Dec | Hex | Space | |
| 0 | 0 | 000 | SP | Reset: Initial SSP |
| — | 4 | 004 | SP | Reset: Initial PC |
| 2 | 8 | 008 | SD | Bus Error |
| 3 | 12 | 00C | SD | Address Error |
| 4 | 16 | 010 | SD | Illegal Instruction |
| 5 | 20 | 014 | SD | Zero Divide |
| 6 | 24 | 018 | SD | CHK Instruction |
| 7 | 28 | 01C | SD | TRAPV Instruction |
| 8 | 32 | 020 | SD | Privilege Violation |
| 9 | 36 | 024 | SD | Trace |
| 10 | 40 | 028 | SD | Line 1010 Emulator |
| 11 | 44 | 02C | SD | Line 1111 Emulator |
| 12* | 48 | 030 | SD | (Unassigned, reserved) |
| 13* | 52 | 034 | SD | (Unassigned, reserved) |
| 14* | 56 | 038 | SD | (Unassigned, reserved) |
| 15 | 60 | 03C | SD | Unitialized Interrupt Vector |
| 16-23* | 64 | 04C | SD | (Unassigned, reserved) |
| | 95 | 05F | | |
| 24 | 96 | 060 | SD | Spurious Interrupt |
| 25 | 100 | 064 | SD | Level 1 Interrupt Autovector |
| 26 | 104 | 068 | SD | Level 2 Interrupt Autovector |
| 27 | 108 | 06C | SD | Level 3 Interrupt Autovector |
| 28 | 112 | 070 | SD | Level 4 Interrupt Autovector |
| 29 | 116 | 074 | SD | Level 5 Interrupt Autovector |
| 30 | 120 | 078 | SD | Level 6 Interrupt Autovector |
| 31 | 124 | 07C | SD | Level 7 Interrupt Autovector |
| 32-47 | 128 | 080 | SD | TRAP Instruction Vectors |
| | 191 | 0BF | | — |
| 48-63* | 192 | 0C0 | SD | (Unassigned, reserved) |
| | 255 | 0FF | | — |
| 64-255 | 256 | 100 | SD | User Interrupt Vectors |
| | 1023 | 3FF | | — |

*Vector numbers 12, 13, 14, 16 through 23 and 48 through 63 are reserved for future enhancements by Motorola. No user peripheral devices should be assigned these numbers.

dress errors or tracing. The trap (TRAP), trap on overflow (TRAPV), check register against bounds (CHK) and divide (DIV) instructions all can generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses and privilege violations cause exceptions. Tracing behaves like a very high priority, internally generated interrupt after each instruction execution.

**EXCEPTION PROCESSING SEQUENCE.** Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S-bit is asserted, putting the processor into the supervisor privilege state. Also, the T-bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch, classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status, except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer. The program counter value stacked usually points to the next unexecuted instruction, however for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

**MULTIPLE EXCEPTIONS.** These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted, and the exception processing to commence at the next minor cycle of the processor. The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by bus error and then address error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and

privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

The priority relation between two exceptions determines which is taken, or taken first, if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T-bit is asserted, the trace exception has priority, and is processed first. Before instruction processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. A summary of exception grouping and priority is given in Table 19.

TABLE 19 — EXCEPTION GROUPING AND PRIORITY

| Group | Exception | Processing |
|---|---|---|
| 0 | Reset<br>Bus Error<br>Address Error | Exception processing begins at the next minor cycle |
| 1 | Trace<br>Interrupt<br>Illegal<br>Privilege | Exception processing begins before the next instruction |
| 2 | TRAP, TRAPV,<br>CHK,<br>Zero Divide | Exception processing is started by normal instruction execution |

**EXCEPTION PROCESSING DETAILED DISCUSSION**

Exceptions have a number of sources, and each exception has processing which is peculiar to it. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

**RESET.** The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state, and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The power-up/restart code should be pointed to by the initial program counter.

The RESET instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

**INTERRUPTS.** Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt priority levels

are numbered from one to seven, level seven being the highest priority. The status register contains a three-bit mask which indicates the current processor priority, and interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not force immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in a following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. First a copy of the status register is saved, and the privilege state is set to supervisor, tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flow chart for the interrupt acknowledge sequence is given in Figure 24; a timing diagram is given in Figure 25.

**FIGURE 24 — INTERRUPT ACKNOWLEDGE SEQUENCE FLOW CHART**

PROCESSOR     INTERRUPTING DEVICE

Request Interrupt

Grant Interrupt
1) Compare interrupt level in status register and wait for current instruction to complete
2) Place interrupt level on A1, A2, A3
3) Set R/$\overline{W}$ to read
4) Set function code to interrupt acknowledge
5) Assert address strobe ($\overline{AS}$)
6) Assert lower data strobe ($\overline{LDS}$)

Provide Vector Number
1) Place vector number of D0-D7
2) Assert data transfer acknowledge ($\overline{DTACK}$)

Acquire Vector Number
1) Latch vector number
2) Negate $\overline{LDS}$
3) Negate $\overline{AS}$

Release
1) Negate $\overline{DTACK}$

Start Interrupt Processing

**FIGURE 25 — INTERRUPT ACKNOWLEDGE SEQUENCE TIMING DIAGRAM**



CLK
A4-A23
A1-A3
$\overline{AS}$
$\overline{UDS}$
$\overline{LDS}$
R/$\overline{W}$
$\overline{DTACK}$
D8-D15
D0-D7
FC0-2
IPL0-2

|← —— Read Cycle —— →|←— ——Vector Number Acquisition— ——→|

538
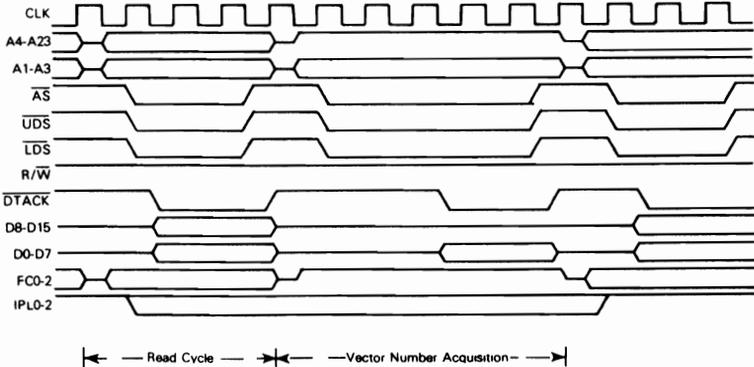
Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a "non-maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction

**INSTRUCTION TRAPS.** Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception, and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds

The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

**ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS.** Illegal instruction is the term used to refer to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and separate exception vectors are given to these patterns to permit efficient emulation This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

**PRIVILEGE VIOLATIONS.** In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

| | |
|---|---|
| STOP | AND (word) Immediate to SR |
| RESET | EOR (word) Immediate to SR |
| RTE | OR (word) Immediate to SR |
| MOVE to SR | MOVE USP |

**TRACING.** To aid in program development, the MC68000 includes a facility to allow instruction by instruction tracing. In the trace state, after each instruction is executed an exception is forced, allowing a debugging program to monitor the execution of the program under test.

The trace facility uses the T-bit in the supervisor portion of the status register. If the T-bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T-bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception If, during the execution of the instruction, an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

**BUS ERROR.** Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, two to ten bytes beyond the ad-

**FIGURE 26 — SUPERVISOR STACK ORDER**
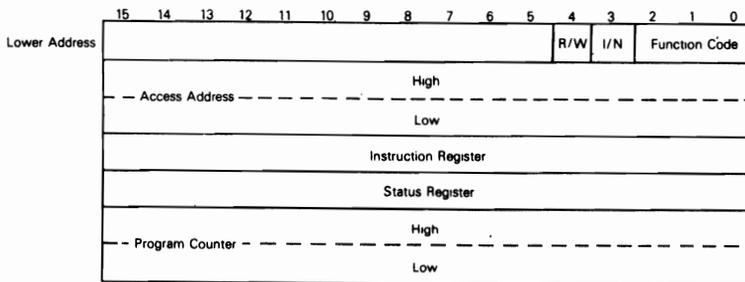


R/W (read/write) write = 0, read = 1. I/N (instruction/not): instruction = 0, not = 1

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dress of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed, and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved: whether it was a read or a write, whether the processor was processing an instruction or not, and the classification displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if it is in the normal state or processing a Group 2 exception; the processor is not processing an instruction if it is processing a Group 0 or a Group 1 exception. Figure 26 illustrates how this information is organized on the supervisor stack. Although this information is not sufficient in general to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in the vector. It is

the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted, and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes itself from the system rather than destroy all memory contents. Only the RESET pin can restart a halted processor

**ADDRESS ERROR.** Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor ceases whatever processing it is currently doing and begins exception processing. After exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted.

## INTERFACE WITH M6800 PERIPHERALS

Motorola's extensive line of M6800 peripherals are directly compatible with the MC68000. Some of these devices that are particularly useful are:

MC6821 Peripheral Interface Adapter

MC6840 Programmable Timer Module

MC6843 Floppy Disk Controller

MC6845 CRT Controller

MC6850 Asynchronous Communication Interface Adapter

MC6852 Synchronous Serial Data Adapter

MC6854 Advanced Data Link Controller

MC68488 General Purpose Interface Adapter

To interface the synchronous M6800 peripherals with the asynchronous MC68000, the processor modifies its bus cycle to meet the M6800 cycle requirements whenever an M6800 device address is detected. This is possible since both processors use memory mapped I/O. Figure 27 is a flow chart of the interface operation between the processor and M6800 devices.

### DATA TRANSFER OPERATION

Three signals on the processor provide the M6800 interface. They are: enable (E), valid memory address ($\overline{VMA}$), and valid peripheral address ($\overline{VPA}$). Enable corresponds to the E or $\phi2$ signal in existing M6800 systems. It is the bus clock used by the frequency clock that is one tenth of the incoming MC68000 clock frequency. The timing of E allows 1 MHz peripherals to be used with an 8 MHz MC68000. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

M6800 cycle timing is given in Figure 28. At state zero (S0) in the cycle, the address bus and function codes are in the high-impedance state. One half clock later, in state 1, the address bus and function code outputs are released from the high-impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/$\overline{W}$) signal is switched to low (write)

### FIGURE 27 — M6800 INTERFACING FLOW CHART

**PROCESSOR**                    **SLAVE**

<u>Initiate Cycle</u>

1) The processor starts a normal Read or Write cycle

<u>Define M6800 Cycle</u>

1) External hardware asserts Valid Peripheral Address ($\overline{VPA}$)

<u>Synchronize With Enable</u>

1) The processor monitors Enable (E) until it is low (Phase 1)
2) The processor asserts Valid Memory Address ($\overline{VMA}$)

<u>Transfer Data</u>

1) The peripheral waits until E is active and then transfers the data

<u>Terminate Cycle</u>

1) The processor waits until E goes low. (On a Read cycle the data is latched as E goes low internally)
2) The processor negates $\overline{VMA}$
3) The processor negates $\overline{AS}$, $\overline{UDS}$, and $\overline{LDS}$

<u>Start Next Cycle</u>

during state 2. One half clock later, in state 3, the write data is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus.

The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$. The $\overline{VPA}$ input signals the processor that the address on the bus is the address of an M6800 device (or an area reserved for M6800 devices) and that the bus should conform to the φ2 transfer characteristics of the M6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by address strobe.

After the recognition of $\overline{VPA}$, the processor assures that the Enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the M6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal.

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one half clock cycle later in state 7, and the Enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle, the data bus is put in the high-impedance state and the read/write signal is switched high at this time. The peripheral logic must remove $\overline{VPA}$ within one clock after address strobe is negated.

Figure 29 shows the timing required by M6800 peripherals, the timing specified for the M6800, and the corresponding timing for the MC68000. For further details on peripheral timing, consult the current data sheet for the peripheral of interest. Notice that the MC68000 $\overline{VMA}$ is active low, contrasted with the active high M6800 VMA. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting peripherals.

FIGURE 28 — M6800 CYCLE OPERATION



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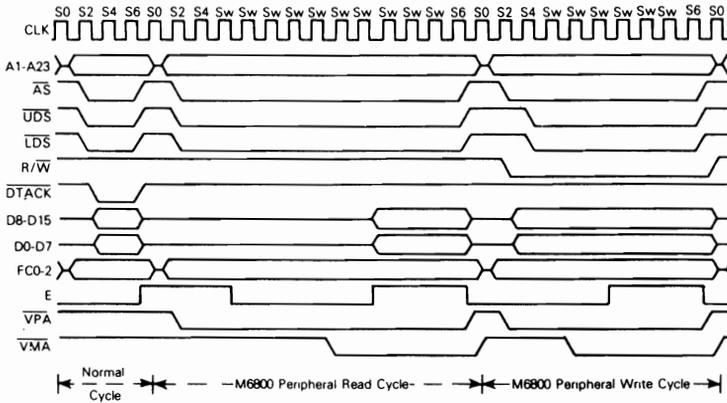
FIGURE 29 — MC68000 TO MC6800 PERIPHERAL TIMING DIAGRAM
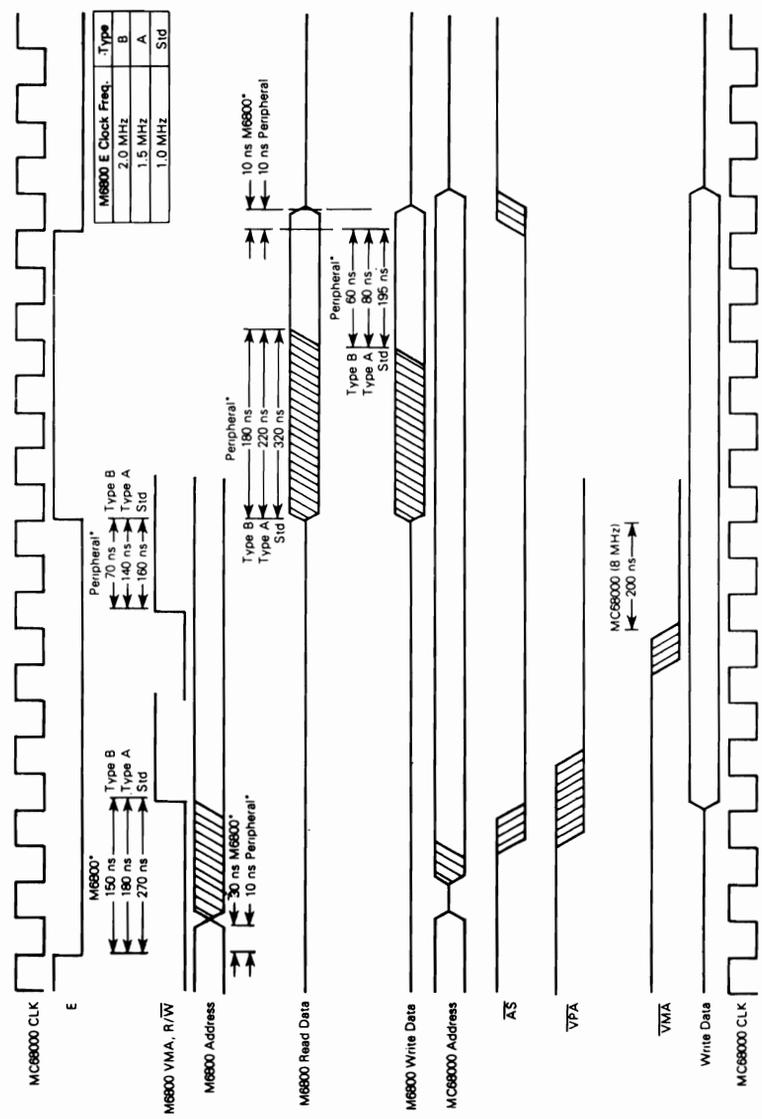
*Times are expressed for different device clock frequencies

| M6800 E Clock Freq. | Type |
|---|---|
| 2.0 MHz | B |
| 1.5 MHz | A |
| 1.0 MHz | Std |

## INTERRUPT INTERFACE OPERATION

During an interrupt acknowledge cycle while the processor is fetching the vector, if $\overline{VPA}$ is asserted, the MC68000 will assert $\overline{VMA}$ and complete a normal M6800 read cycle as shown in Figure 30. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is known as autovectoring. The seven autovectors are vector numbers 25 through 31 (decimal).

This operates in the same fashion (but is not restricted to) the M6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the M6800 and the MC68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since $\overline{VMA}$ is asserted during autovectoring, the M6800 peripheral address decoding should prevent unintended accesses.

**FIGURE 30 — AUTOVECTOR OPERATION TIMING DIAGRAM**
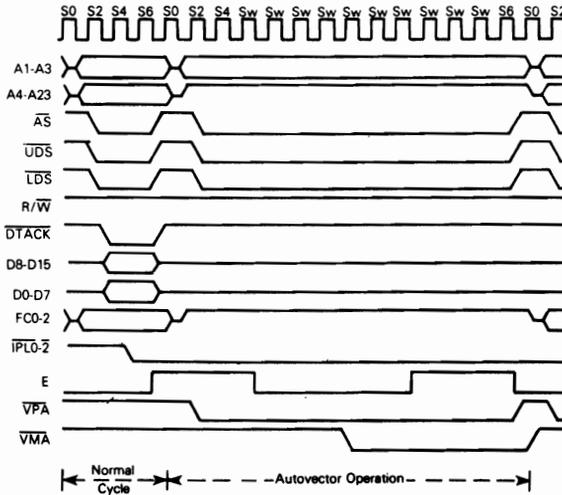
# INSTRUCTION SET

The following paragraphs provide information about the addressing categories and instruction set of the MC68000.

## ADDRESSING CATEGORIES

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instruction definitions.

Data — If an effective address mode may be used to refer to data·operands, it is considered a data addressing effective address mode.

Memory — If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.

Alterable — If an effective address mode may be used to refer to alterable (writeable) operands, it is considered an alterable addressing effective address mode.

Control — If an effective address mode may be used to refer to memory operands without an associated size, it is considered a control addressing effective address mode.

Table 20 shows the various categories to which each of the effective address modes belong. Table 21 is the instruction set summary.

The status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

#### TABLE 20 — EFFECTIVE ADDRESSING MODE CATEGORIES

| Effective Address Modes | Mode | Register | Addressing Categories | | | |
|---|---|---|---|---|---|---|
| | | | Data | Memory | Control | Alterable |
| Dn | 000 | register number | X | — | — | X |
| An | 001 | register number | — | — | — | X |
| An@ | 010 | register number | X | X | X | X |
| An@ + | 011 | register number | X | X | — | X |
| An@ − | 100 | register number | X | X | — | X |
| An@(d) | 101 | register number | X | X | X | X |
| An@(d, ix) | 110 | register number | X | X | X | X |
| xxx.W | 111 | 000 | X | X | X | X |
| xxx.L | 111 | 001 | X | X | X | X |
| PC@(d) | 111 | 010 | X | X | X | — |
| PC@(d, ix) | 111 | 011 | X | X | X | — |
| #xxx | 111 | 100 | X | X | — | — |

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**TABLE 21 — INSTRUCTION SET**

| Mnemonic | Description | Operation | Condition Codes | | | | |
|---|---|---|---|---|---|---|---|
| | | | X | N | Z | V | C |
| ABCD | Add Decimal with Extend | $(Destination)_{10} + (Source)_{10} \rightarrow$ Destination | * | U | * | U | * |
| ADD | Add Binary | (Destination) + (Source) → Destination | * | * | * | * | * |
| ADDA | Add Address | (Destination) + (Source) → Destination | – | – | – | – | – |
| ADDI | Add Immediate | (Destination) + Immediate Data → Destination | * | * | * | * | * |
| ADDQ | Add Quick | (Destination) + Immediate Data → Destination | * | * | * | * | * |
| ADDX | Add Extended | (Destination) + (Source) + X → Destination | * | * | * | * | * |
| AND | AND Logical | (Destination) ∧ (Source) → Destination | – | * | * | 0 | 0 |
| ANDI | AND Immediate | (Destination) ∧ Immediate Data → Destination | – | * | * | 0 | 0 |
| ASL, ASR | Arithmetic Shift | (Destination) Shifted by <count> → Destination | * | * | * | * | * |
| B$_{CC}$ | Branch Conditionally | If CC then PC + d → PC | – | – | – | – | – |
| BCHG | Test a Bit and Change | ~(<bit number>) OF Destination → Z <br> ~(<bit number>) OF Destination → <br> <bit number> OF Destination | – | – | * | – | – |
| BCLR | Test a Bit and Clear | ~(<bit number>) OF Destination → Z <br> 0 → <bit number> → OF Destination | – | – | * | – | – |
| BRA | Branch Always | PC + d → PC | – | – | – | – | – |
| BSET | Test a Bit and Set | ~(<bit number>) OF Destination → Z <br> 1 → <bit number> OF Destination | – | – | * | – | – |
| BSR | Branch to Subroutine | PC → SP@ – ; PC + d → PC | – | – | – | – | – |
| BTST | Test a Bit | ~(<bit number>) OF Destination → Z | – | – | * | – | – |
| CHK | Check Register against Bounds | If Dn <0 or Dn> (<ea>) then TRAP | – | * | U | U | U |
| CLR | Clear an Operand | 0 → Destination | – | 0 | 1 | 0 | 0 |
| CMP | Compare | (Destination) – (Source) | – | * | * | * | * |
| CMPA | Compare Address | (Destination) – (Source) | – | * | * | * | * |
| CMPI | Compare Immediate | (Destination) – Immediate Data | – | * | * | * | * |
| CMPM | Compare Memory | (Destination) – (Source) | – | * | * | * | * |
| DB$_{CC}$ | Test Condition, Decrement and Branch | If ~ CC then Dn – 1 → Dn; if Dn ≠ – 1 then PC + d → PC | – | – | – | – | – |
| DIVS | Signed Divide | (Destination)/(Source) → Destination | – | * | * | * | 0 |
| DIVU | Unsigned Divide | (Destination)/(Source) → Destination | – | * | * | * | 0 |
| EOR | Exclusive OR Logical | (Destination) ⊕ (Source) → Destination | – | * | * | 0 | 0 |
| EORI | Exclusive OR Immediate | (Destination) ⊕ Immediate Data → Destination | – | * | * | 0 | 0 |
| EXG | Exchange Register | Rx ↔ Ry | – | – | – | – | – |
| EXT | Sign Extend | (Destination) Sign-extended → Destination | – | * | * | 0 | 0 |
| JMP | Jump | Destination → PC | – | – | – | – | – |
| JSR | Jump to Subroutine | PC → SP@ – ; Destination → PC | – | – | – | – | – |
| LEA | Load Effective Address | Destination → An | – | – | – | – | – |
| LINK | Link and Allocate | An → SP@ – ; SP → An; SP + d → SP | – | – | – | – | – |
| LSL, LSR | Logical Shift | (Destination) Shifted by <count> → Destination | * | * | * | 0 | * |
| MOVE | Move Data from Source to Destination | (Source) → Destination | – | * | * | 0 | 0 |
| MOVE to CCR | Move to Condition Code | (Source) → CCR | * | * | * | * | * |
| MOVE to SR | Move to the Status Register | (Source) → SR | * | * | * | * | * |

\* affected    0 cleared    U defined <br>
– unaffected    1 set

**TABLE 21 — INSTRUCTION SET (CONTINUED)**

| Mnemonic | Description | Operation | Condition Codes | | | | |
|---|---|---|---|---|---|---|---|
| | | | X | N | Z | V | C |
| MOVE from SR | Move from the Status Register | SR → Destination | — | — | — | — | — |
| MOVE USP | Move User Stack Pointer | USP → An; An → USP | — | — | — | — | — |
| MOVEA | Move Address | (Source) → Destination | — | — | — | — | — |
| MOVEM | Move Multiple Registers | Registers → Destination (Source) → Registers | — | — | — | — | — |
| MOVEP | Move Peripheral Data | (Source) → Destination | — | — | — | — | — |
| MOVEQ | Move Quick | Immediate Data → Destination | — | • | • | 0 | 0 |
| MULS | Signed Multiply | (Destination)*(Source) → Destination | — | • | • | 0 | 0 |
| MULU | Unsigned Multiply | (Destination)*(Source) → Destination | — | • | • | 0 | 0 |
| NBCD | Negate Decimal with Extend | $0 - (\text{Destination})_{10} - X \rightarrow$ Destination | • | U | • | U | • |
| NEG | Negate | 0 − (Destination) → Destination | • | • | • | • | • |
| NEGX | Negate with Extend | 0 − (Destination) − X → Destination | • | • | • | • | • |
| NOP | No Operation | — | — | — | — | — | — |
| NOT | Logical Complement | ~ (Destination) → Destination | — | • | • | 0 | 0 |
| OR | Inclusive OR Logical | (Destination) v (Source) → Destination | — | • | • | 0 | 0 |
| ORI | Inclusive OR Immediate | (Destination) v Immediate Data → Destination | — | • | • | 0 | 0 |
| PEA | Push Effective Address | Destination → SP@ − | — | — | — | — | — |
| RESET | Reset External Devices | — | — | — | — | — | — |
| ROL, ROR | Rotate (Without Extend) | (Destination) Rotated by < count > → Destination | — | • | • | 0 | • |
| ROXL, ROXR | Rotate with Extend | (Destination) Rotated by < count > → Destination | • | • | • | 0 | • |
| RTE | Return from Exception | SP@ − → SR; SP@ + → PC | • | • | • | • | • |
| RTR | Return and Restore Condition Codes | SP@ + → CC; SP@ + → PC | • | • | • | • | • |
| RTS | Return from Subroutine | SP@ + → PC | — | — | — | — | — |
| SBCD | Subtract Decimal with Extend | $(\text{Destination})_{10} - (\text{Source})_{10} - X \rightarrow$ Destination | • | U | • | U | • |
| S$_{CC}$ | Set According to Condition | If CC then 1's → Destination else 0's → Destination | — | — | — | — | — |
| STOP | Load Status Register and Stop | Immediate Data → SR; STOP | • | • | • | • | • |
| SUB | Subtract Binary | (Destination) − (Source) → Destination | • | • | • | • | • |
| SUBA | Subtract Address | (Destination) − (Source) → Destination | — | — | — | — | — |
| SUBI | Subtract Immediate | (Destination) − Immediate Data → Destination | • | • | • | • | • |
| SUBQ | Subtract Quick | (Destination) − Immediate Data → Destination | • | • | • | • | • |
| SUBX | Subtract with Extend | (Destination) − (Source) − X → Destination | • | • | • | • | • |
| SWAP | Swap Register Halves | Register [31:16] ↔ Register [15:0] | — | • | • | 0 | 0 |
| TAS | Test and Set an Operand | (Destination) Tested → CC; 1 → [7] OF Destination | — | • | • | 0 | 0 |
| TRAP | Trap | PC → SSP@ −; SR → SSP@ −; (Vector) → PC | — | — | — | — | — |
| TRAPV | Trap on Overflow | If V then TRAP | — | — | — | — | — |
| TST | Test an Operand | (Destination) Tested → CC | — | • | • | 0 | 0 |
| UNLK | Unlink | An → SP; SP@ + → An | — | — | — | — | — |

[  ] = bit number

## INSTRUCTION EXECUTION TIMES

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that the memory cycle time is no greater than four periods of the external processor clock input, which prevents the insertion of wait states in the bus cycle. The number of bus read and write cycles for each instruction is also included with the timing data. This data is enclosed in parenthesis following the execution periods and is shown as (r/w) where r is the number of read cycles and w is the number of write cycles.

### NOTE
The number of periods includes instruction fetch and all applicable operand fetches and stores.

### EFFECTIVE ADDRESS OPERAND CALCULATION TIMING

Table 22 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parenthesis as (r/w). Note there are no write cycles involved in processing the effective address.

### MOVE INSTRUCTION CLOCK PERIODS

Tables 23 and 24 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parenthesis as: (r/w)

### STANDARD INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 25 indicates the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 25, the headings have the following meanings. An = address register operand, Dn = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

### IMMEDIATE INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 26 includes the time to fetch immediate operands, perform the operations, store the results, and read the next operation. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 26, the headings have the following meanings. $I$ = immediate operand, Dn = data register operand, M = memory operand, and SR = status register.

### SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 27 indicates the number of clock periods for the single operand instructions. The number of bus read and write cycles is shown in parenthesis as (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated

### TABLE 22 — EFFECTIVE ADDRESS CALCULATION TIMING

| Addressing Mode | | Byte, Word | Long |
|---|---|---|---|
| **Register** | | | |
| Dn | Data Register Direct | 0(0/0) | 0(0/0) |
| An | Address Register Direct | 0(0/0) | 0(0/0) |
| **Memory** | | | |
| An@ | Address Register Indirect | 4(1/0) | 8(2/0) |
| An@ + | Address Register Indirect with Postincrement | 4(1/0) | 8(2/0) |
| An@ − | Address Register Indirect with Predecrement | 6(1/0) | 10(2/0) |
| An@(d) | Address Register Indirect with Displacement | 8(2/0) | 12(3/0) |
| An@(d, ix)* | Address Register Indirect with Index | 10(2/0) | 14(3/0) |
| xxx.W | Absolute Short | 8(2/0) | 12(3/0) |
| xxx.L | Absolute Long | 12(3/0) | 16(4/0) |
| PC@(d) | Program Counter with Displacement | 8(2/0) | 12(3/0) |
| PC@(d, ix)* | Program Counter with Index | 10(2/0) | 14(3/0) |
| $I$xxx | Immediate | 4(1/0) | 8(2/0) |

*The size of the index register (ix) does not affect execution time.

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### TABLE 23 — MOVE BYTE AND WORD INSTRUCTION CLOCK PERIODS

| Source | Destination | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Dn | An | An@ | An@ + | An@ | An@(d) | An@(d, ix)* | xxx.W | xxx.L |
| Dn | 4(1/0) | 4(1/0) | 9(1/1) | 9(1/1) | 9(1/1) | 13(2/1) | 15(2/1) | 13(2/1) | 17(3/1) |
| An | 4(1/0) | 4(1/0) | 9(1/1) | 9(1/1) | 9(1/1) | 13(2/1) | 15(2/1) | 13(2/1) | 17(3/1) |
| An@ | 8(2/0) | 8(2/0) | 13(2/1) | 13(2/1) | 13(2/1) | 17(3/1) | 19(3/1) | 17(3/1) | 21(4/1) |
| An@ + | 8(2/0) | 8(2/0) | 13(2/1) | 13(2/1) | 13(2/1) | 17(3/1) | 19(3/1) | 17(3/1) | 21(4/1) |
| An@ − | 10(2/0) | 10(2/0) | 15(2/1) | 15(2/1) | 15(3/1) | 19(3/1) | 21(3/1) | 19(3/1) | 23(4/1) |
| An@(d) | 12(3/0) | 12(3/0) | 17(3/1) | 17(3/1) | 17(3/1) | 21(4/1) | 23(4/1) | 21(4/1) | 25(5/1) |
| An@(d, ix)* | 14(3/0) | 14(3/0) | 19(3/1) | 19(3/1) | 19(3/1) | 23(4/1) | 25(4/1) | 23(4/1) | 27(5/1) |
| xxx.W | 12(3/0) | 12(3/0) | 17(3/1) | 17(3/1) | 17(3/1) | 21(4/1) | 23(4/1) | 21(4/1) | 25(5/1) |
| xxx.L | 16(4/0) | 16(4/0) | 21(4/1) | 21(4/1) | 21(4/1) | 25(5/1) | 27(5/1) | 25(5/1) | 29(6/1) |
| PC@(d) | 12(3/1) | 12(3/0) | 17(3/1) | 17(3/1) | 17(3/1) | 21(4/1) | 23(4/1) | 21(4/1) | 25(5/1) |
| PC@(d, ix)* | 14(3/0) | 14(3/0) | 19(3/1) | 19(3/1) | 19(3/1) | 23(4/1) | 25(4/1) | 23(4/1) | 27(5/1) |
| *xxx* | 8(2/0) | 8(2/0) | 13(2/1) | 13(2/1) | 13(2/1) | 17(3/1) | 19(3/1) | 17(3/1) | 21(4/1) |

*The size of the index register (ix) does not affect execution time

### TABLE 24 — MOVE LONG INSTRUCTION CLOCK PERIODS

| Source | Destination | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Dn | An | An@ | An@ + | An@ − | An@(d) | An@(d, ix)* | xxx.W | xxx.L |
| Dn | 4(1/0) | 4(1/0) | 14(1/2) | 14(1/2) | 16(1/2) | 18(2/2) | 20(2/2) | 18(2/2) | 22(3/2) |
| An | 4(1/0) | 4(1/0) | 14(1/2) | 14(1/2) | 16(1/2) | 18(2/2) | 20(2/2) | 18(2/2) | 22(3/2) |
| An@ | 12(3/0) | 12(3/0) | 22(3/2) | 22(3/2) | 22(3/2) | 26(4/2) | 28(4/2) | 26(4/2) | 30(5/2) |
| An@ + | 12(3/0) | 12(3/0) | 22(3/2) | 22(3/2) | 22(3/2) | 26(4/6) | 28(4/2) | 26(4/2) | 30(5/2) |
| An@ − | 14(3/0) | 14(3/0) | 24(3/2) | 24(3/2) | 24(3/2) | 28(4/2) | 30(4/2) | 28(4/2) | 32(5/2) |
| An@(d) | 16(4/0) | 16(4/0) | 26(4/2) | 26(4/2) | 26(4/2) | 30(5/2) | 32(5/2) | 30(5/2) | 34(6/2) |
| An@(d, ix)* | 18(4/0) | 18(4/0) | 28(4/2) | 28(4/2) | 28(4/2) | 32(5/2) | 34(5/2) | 32(5/2) | 36(6/2) |
| xxx.W | 16(4/0) | 16(4/0) | 26(4/2) | 26(4/2) | 26(4/2) | 30(5/2) | 32(5/2) | 30(5/2) | 34(6/2) |
| xxx.L | 20(5/0) | 20(5/0) | 30(5/2) | 30(5/2) | 30(5/2) | 34(6/2) | 36(6/2) | 34(6/2) | 38(7/2) |
| PC@(d) | 16(4/0) | 16(4/0) | 26(4/2) | 26(4/2) | 26(4/2) | 30(5/2) | 32(5/2) | 30(5/2) | 34(6/2) |
| PC@(d, ix)* | 18(4/0) | 18(4/0) | 28(4/2) | 28(4/2) | 28(4/2) | 32(5/2) | 34(5/2) | 32(5/2) | 36(6/2) |
| *xxx* | 12(3/0) | 12(3/0) | 22(3/2) | 22(3/2) | 22(3/2) | 26(4/2) | 28(4/2) | 26(4/2) | 30(5/2) |

*The size of the index register (ix) does not affect execution time

### TABLE 25 — STANDARD INSTRUCTION CLOCK PERIODS

| Instruction | Size | op <ea>, An | op <ea>, Dn | op Dn, <M> |
|---|---|---|---|---|
| ADD | Byte, Word | 8(1/0) + | 4(1/0) + | 9(1/1) + |
| | Long | 6(1/0) + ** | 6(1/0) + ** | 14(1/2) + |
| AND | Byte, Word | — | 4(1/0) + | 9(1/1) + |
| | Long | — | 6(1/0) + ** | 14(1/2) + |
| CMP | Byte, Word | 6(1/0) + | 4(1/0) + | — |
| | Long | 6(1/0) + | 6(1/0) + | — |
| DIVS | — | — | 158(1/0) + * | — |
| DIVU | — | — | 140(1/0) + * | — |
| EOR | Byte, Word | — | 4(1/0)*** | 9(1/1) + |
| | Long | — | 8(1/0)*** | 14(1/2) + |
| MULS | — | — | 70(1/0) + * | — |
| MULU | — | — | 70(1/0) + * | — |
| OR | Byte, Word | — | 4(1/0) + | 9(1/1) + |
| | Long | — | 6(1/0) + ** | 14(1/2) + |
| SUB | Byte, Word | 8(1/0) + | 4(1/0) + | 9(1/1) + |
| | Long | 6(1/0) + ** | 6(1/0) + ** | 14(1/2) + |

+ add effective address calculation time   ** total of 8 clock periods for instruction if the effective address is register direct
* indicates maximum value   *** only available effective address mode is data register direct

## TABLE 26 — IMMEDIATE INSTRUCTION CLOCK PERIODS

| Instruction | Size | op #, Dn | op #, M | op #, SR |
|---|---|---|---|---|
| ADDI | Byte, Word | 8(2/0) | 13(2/1) + | — |
| | Long | 16(3/0) | 22(3/2) + | — |
| ADDQ | Byte, Word | 4(1/0) | 9(1/1) + | — |
| | Long | 8(1/0) | 14(1/2) + | — |
| ANDI | Byte, Word | 8(2/0) | 13(2/1) + | 20(3/0) |
| | Long | 16(3/0) | 22(3/2) + | — |
| CMPI | Byte, Word | 8(2/0) | 8(2/0) + | — |
| | Long | 14(3/0) | 12(3/0) + | — |
| EORI | Byte, Word | 8(2/0) | 13(2/1) + | 20(3/0) |
| | Long | 16(3/0) | 22(3/2) + | — |
| MOVEQ | Long | 4(1/0) | — | — |
| ORI | Byte, Word | 8(2/0) | 13(2/1) + | 20(3/0) |
| | Long | 16(3/0) | 22(3/2) + | — |
| SUBI | Byte, Word | 8(2/0) | 13(2/1) + | — |
| | Long | 16(3/0) | 22(3/2) + | — |
| SUBQ | Byte, Word | 4(1/0) | 9(1/1) + | — |
| | Long | 8(1/0) | 14(1/2) + | — |

+ add effective address calculation time

## TABLE 27 — SINGLE OPERAND INSTRUCTION CLOCK PERIODS

| Instruction | Size | Register | Memory |
|---|---|---|---|
| CLR | Byte, Word | 4(1/0) | 9(1/1) + |
| | Long | 6(1/0) | 14(1/2) + |
| NBCD | Byte | 6(1/0) | 9(1/1) + |
| NEG | Byte, Word | 4(1/0) | 9(1/1) + |
| | Long | 6(1/0) | 14(1/2) + |
| NEGX | Byte, Word | 4(1/0) | 9(1/1) + |
| | Long | 6(1/0) | 14(1/2) + |
| NOT | Byte, Word | 4(1/0) | 9(1/1) + |
| | Long | 6(1/0) | 14(1/2) + |
| Scc | Byte, False | 4(1/0) | 9(1/1) + |
| | Byte, True | 6(1/0) | 9(1/1) + |
| TAS | Byte | 4(1/0) | 11(1/1) + |
| TST | Byte, Word | 4(1/0) | 4(1/0) |
| | Long | 4(1/0) | 4(1/0) + |

+ add effective address calculation time

### SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 28 indicates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

### BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 29 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

### CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 30 indicates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

### JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Table 31 indicates the number of clock periods required for the jump, jump to subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w).

TABLE 28 — SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

| Instruction | Size | Register | Memory |
|---|---|---|---|
| ASR, ASL | Byte, Word | 6 + 2n(1/0) | 9(1/1) + |
| | Long | 8 + 2n(1/0) | — |
| LSR, LSL | Byte, Word | 6 + 2n(1/0) | 9(1/1) + |
| | Long | 8 + 2n(1/0) | — |
| ROR, ROL | Byte, Word | 6 + 2n(1/0) | 9(1/1) + |
| | Long | 8 + 2n(1/0) | — |
| ROXR, ROXL | Byte, Word | 6 + 2n(1/0) | 9(1/1) + |
| | Long | 8 + 2n(1/0) | — |

TABLE 29 — BIT MANIPULATION INSTRUCTION CLOCK PERIODS

| Instruction | Size | Dynamic | | Static | |
|---|---|---|---|---|---|
| | | Register | Memory | Register | Memory |
| BCHG | Byte | — | 9(1/1) + | — | 13(2/1) + |
| | Long | 8(1/0)* | — | 12(2/0)* | — |
| BCLR | Byte | — | 9(1/1) + | — | 13(2/1) + |
| | Long | 10(1/0)* | — | 14(2/0)* | — |
| BSET | Byte | — | 9(1/1) + | — | 13(2/1) + |
| | Long | 8(1/0)* | — | 12(2/0)* | — |
| BTST | Byte | — | 4(1/0) + | — | 8(2/0) + |
| | Long | 6(1/0) | — | 10(2/0) | — |

+ add effective address calculation time
* indicates maximum value

TABLE 30 — CONDITIONAL INSTRUCTION CLOCK PERIODS

| Instruction | Displacement | Trap or Branch Taken | Trap or Branch Not Taken |
|---|---|---|---|
| B_CC | Byte | 10(1/0) | 8(1/0) |
| | Word | 10(1/0) | 12(2/0) |
| BRA | Byte | 10(1/0) | — |
| | Word | 10(1/0) | — |
| BSR | Byte | 20(2/2) | — |
| | Word | 20(2/2) | — |
| DB_CC | CC true | — | 12(2/0) |
| | CC false | 10(2/0) | 14(3/0) |
| CHK | — | 43(5/3) + * | 8(1/0) + |
| TRAP | — | 37(4/3) | |
| TRAPV | — | 37(5/3) | 4(1/0) |

+ add effective address calculation time
* indicates maximum value

TABLE 31 — JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

| Instr | Size | An@ | An@+ | An@- | An@(d) | An@(d, ix)* | xxx.W | xxx.L | PC@(d) | PC@(d, ix)* |
|---|---|---|---|---|---|---|---|---|---|---|
| JMP | - | 8(2/0) | - | - | 10(2/0) | 14(3/0) | 10(2/0) | 12(3/0) | 10(2/0) | 14(3/0) |
| JSR | - | 18(2/2) | - | - | 20(2/2) | 24(2/2) | 20(2/0) | 22(3/2) | 20(2/2) | 24(2/2) |
| LEA | - | 4(1/0) | - | - | 8(2/0) | 12(2/0) | 8(2/0) | 12(3/0) | 8(2/0) | 12(2/0) |
| PEA | - | 14(1/2) | - | - | 18(2/2) | 22(2/2) | 18(2/2) | 22(3/2) | 18(2/2) | 22(2/2) |
| MOVEM M→R | Word | 12+4n (3+n/0) | 12+4n (3+n/0) | - | 16+4n (4+n/0) | 18+4n (4+n/0) | 16+4n (4+n/0) | 20+4n (5+n/0) | 16+4n (4+n/0) | 18+4n (4+n/0) |
| M→R | Long | 12+8n (3+2n/0) | 12+8n (3+2n/0) | - | 16+8n (4+2n/0) | 18+8n (4+2n/0) | 16+8n (4+2n/0) | 20+8n (5+2n/0) | 16+8n (4+2n/0) | 18+8n (4+2n/0) |
| MOVEM R→M | Word | 8+5n (2/n) | - | 8+5n (2/n) | 12+5n (3/n) | 14+5n (3/n) | 12+5n (3/n) | 16+5n (4/n) | - | - |
| R→M | Long | 8+10n (2/2n) | - | 8+10n (2/2n) | 12+10n (3/2n) | 14+10n (3/2n) | 12+10n (3/2n) | 16+10n (4/2n) | - | - |

n is the number of registers to move

* is the size of the index register (ix) does not affect the instruction's execution time

TABLE 32 — MULTI-PRECISION INSTRUCTION CLOCK PERIODS

| Instruction | Size | op Dn, Dn | op M, M |
|---|---|---|---|
| ADDX | Byte, Word | 4(1/0) | 19(3/1) |
| | Long | 8(1/0) | 32(5/2) |
| CMPM | Byte, Word | — | 12(3/0) |
| | Long | — | 20(5/0) |
| SUBX | Byte, Word | 4(1/0) | 19(3/1) |
| | Long | 8(1/0) | 32(5/2) |
| ABCD | Byte | 6(1/0) | 19(3/1) |
| SBCD | Byte | 6(1/0) | 19(3/1) |

## MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 32 indicates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parenthesis as: (r/w).

In Table 32, the headings have the following meanings: Dn = data register operand and M = memory operand.

## MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 33 indicates the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

## EXCEPTION PROCESSING CLOCK PERIODS

Table 34 indicates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking, the vector fetch, and the fetch of the first instruction of the handler routine. The number of bus read and write cycles is shown in parenthesis as: (r/w).

#### TABLE 33 — MISCELLANEOUS INSTRUCTION CLOCK PERIODS

| Instruction | Size | Register | Memory | Register ← Memory | Memory ← Register |
|---|---|---|---|---|---|
| MOVE from SR | — | 6(1/0) | 9(1/1) + | — | — |
| MOVE to CCR | — | 12(2/0) | 12(2/0) + | — | — |
| MOVE to SR | — | 12(2/0) | 12(2/0) + | — | — |
| MOVEP | Word | — | — | 18(2/2) | 16(4/0) |
| | Long | — | — | 28(2/4) | 24(6/0) |
| EXG | — | 6(1/0) | — | — | — |
| EXT | Word | 4(1/0) | — | — | — |
| | Long | 4(1/0) | — | — | — |
| LINK | — | 18(2/2) | — | — | — |
| MOVE from USP | — | 4(1/0) | — | — | — |
| MOVE to USP | — | 4(1/0) | — | — | — |
| NOP | — | 4(1/0) | — | — | — |
| RESET | — | 132(1/0) | — | — | — |
| RTE | — | 20(5/0) | — | — | — |
| RTR | — | 20(5/0) | — | — | — |
| RTS | — | 16(4/0) | — | — | — |
| STOP | — | 4(0/0) | — | — | — |
| SWAP | — | 4(1/0) | — | — | — |
| UNLK | — | 12(3/0) | — | — | — |

+ add effective address calculation time

#### TABLE 34 — EXCEPTION PROCESSING CLOCK PERIODS

| Exception | Periods |
|---|---|
| Address Error | 57(4/7) |
| Bus Error | 57(4/7) |
| Interrupt | 47(5/3)* |
| Illegal Instruction | 37(4/3) |
| Privileged Instruction | 37(4/3) |
| Trace | 37(4/3) |

*The interrupt acknowledge bus cycle is assumed to take four external clock periods

**FIGURE 31 — AC ELECTRICAL WAVEFORMS**

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.
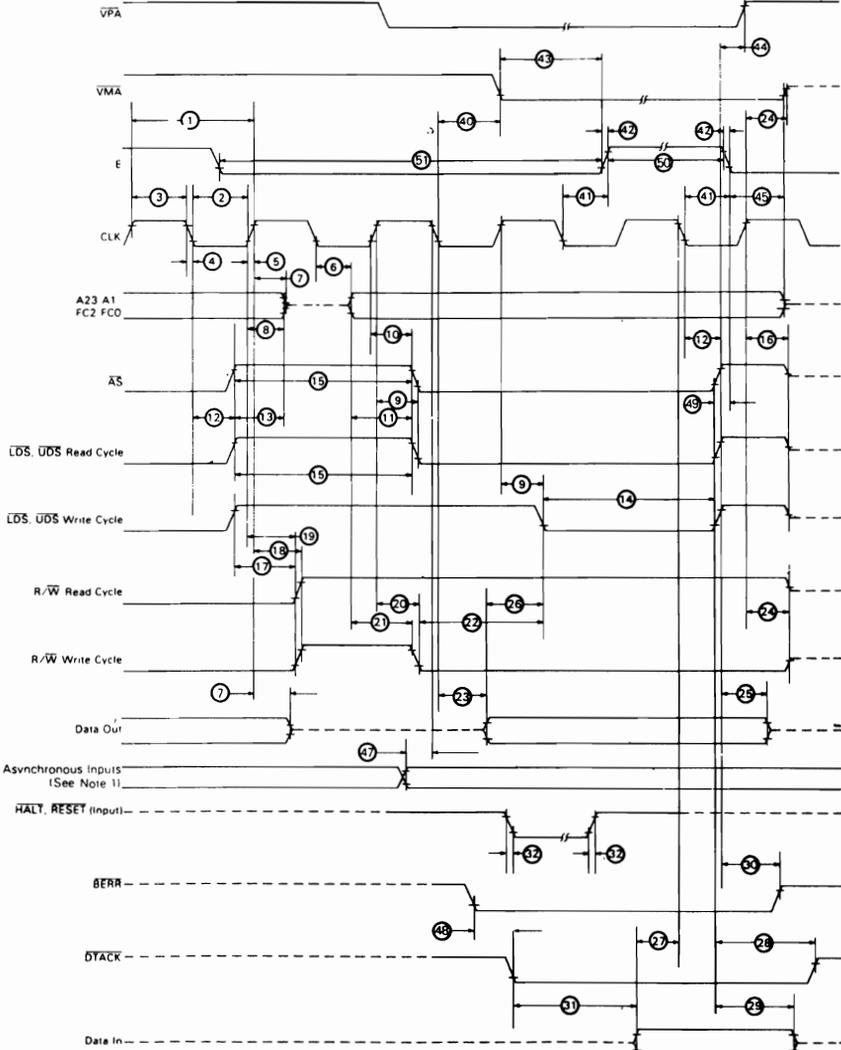


NOTE 1. Setup time for the asynchronous inputs BERR, BGACK, BR, DTACK, IPL0-IPL2, and VPA guarantees their recognition at the next falling edge of the clock.

NOTE 2: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 volts, logic low = 0.8 volts.

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## 32-BIT VIRTUAL MEMORY MICROPROCESSOR

This document contains both a summary of the MC68020 as well as a detailed set of parametrics. The purpose is twofold – to provide an introduction to the MC68020 and support for the sophisticated user. For detailed information on the MC68020 refer to the *MC68020 User's Manual*.

The MC68020 is the first full 32-bit implementation of the M68000 Family of microprocessors from Motorola. Using VLSI technology, the MC68020 is implemented with 32-bit registers and data paths, 32-bit addresses, a rich basic instruction set, and versatile addressing modes. The resources available to the MC68020 user consist of the following

- Virtual Memory/Machine Support
- Sixteen 32-Bit General Purpose Data and Address Registers
- Two 32-Bit Supervisor Stack Pointers
- Five Special Purpose Control Registers
- 4 Gigabyte Direct Addressing Range
- 18 Addressing Modes
- Memory Mapped I/O
- Coprocessor Interface
- High Performance On-Chip Instruction Cache
- Operations on Seven Data Types
- Complete Floating Point Support via MC68881 Coprocessor

### FIGURE 1 – FUNCTIONAL SIGNAL GROUPS
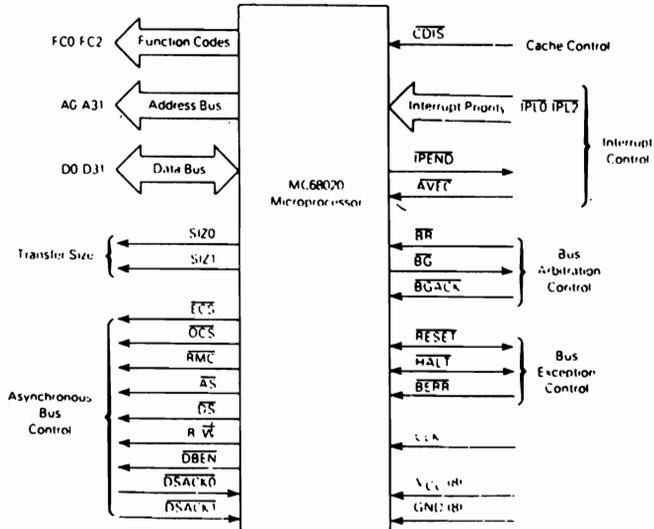
# MC68120
# MC68121

## Advance Information

The MC68120/MC68121 Intelligent Peripheral Controller (IPC) is a general purpose, mask programmable peripheral controller. The IPC provides the interface between an M68000 or M6800 Family microprocessor and the final peripheral devices through a system bus and control lines. System bus data is transferred to and from the IPC via dual-port RAM while the software utilizes the semaphore registers to control RAM tasking or any other shared resource. Multiple operating modes range from a single chip mode with 21 I/O lines and 2 control lines to an expanded mode supporting an address space of 64K bytes. The MC68120 has 2K bytes of on-chip ROM to make full use of all operating modes. The MC68121 utilizes only the expanded address modes, due to the absence of on-chip ROM.

A serial communications interface, 16-bit timer, dual-ported RAM and semaphore registers are available for use by the IPC in all operating modes.

- System Bus Compatible with the Asynchronous M68000 Family
- System Bus Compatible with the MC6809 and Other M6800 Family Processors Peripherals
- Local Bus Allows Interface with all M6800 Peripherals
- MC6801 Source and Object Code Compatible
- Upward Compatible with MC6800 Source and Object Code
- 2048 Bytes of ROM (MC68120 Only)
- 128 Bytes of Dual-Ported RAM
- Multiple Operation Modes Ranging from Single Chip to Expanded, with 64K Byte Address Space
- Six Shared Semaphore Registers
- 21 Parallel I/O Lines and 2 Handshake Lines (5 I/O Lines on MC68121)
- Serial Communications Interface (SCI)
- 16-Bit Three-Function Timer
- 8-Bit CPU and Internal Bus
- Halt/Bus Available Capability Control
- 8 × 8 Multiply Instruction
- TTL Compatible Inputs and Outputs
- External and Internal Interrupts

### HMOS
(HIGH-DENSITY N-CHANNEL SILICON-GATE)

### INTELLIGENT PERIPHERAL CONTROLLER



L SUFFIX
CERAMIC PACKAGE
CASE 740

### PIN ASSIGNMENT
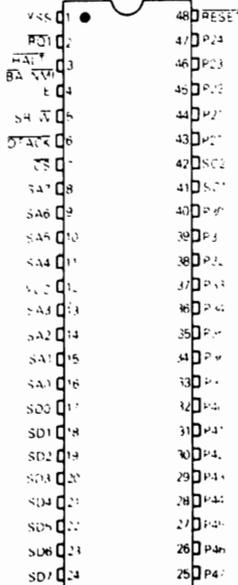


### GENERIC INFORMATION
($T_A = 0°C$ to 70°C)

| Package Type | Frequency (MHz) | Generic Number |
|---|---|---|
| Ceramic | 1 0 | MC68120L1 (Unicorn ROM) |
| L Suffix | 1 0 | MC68121L |
| | 1 25 | MC68120L1 1 (Unicorn ROM) |
| | 1 25 | MC68121L 1 |

# MC68120, MC68121

MC68120/MC68121 INTELLIGENT PERIPHERAL CONTROLLER – BLOCK DIAGRAM
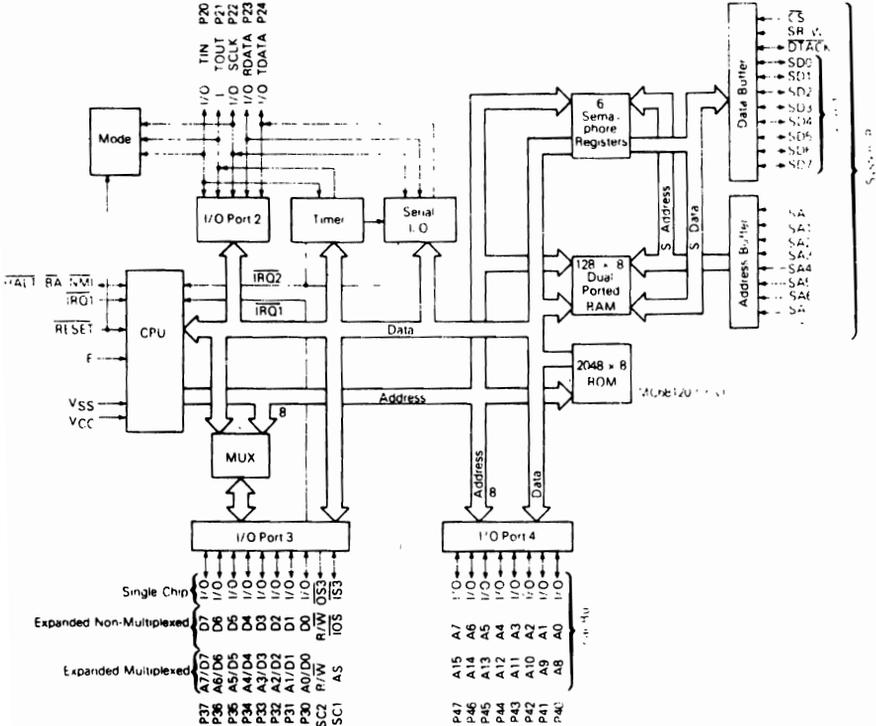


## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | V |
| Input Voltage | $V_{in}$ | -0.3 to +7.0 | V |
| Operating Temperature Range | $T_A$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{stg}$ | -55 to +150 | °C |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Rating |
|---|---|---|---|
| Thermal Resistance Ceramic Package | $\theta_{JA}$ | 50 | C/W |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. either $V_{SS}$ or $V_{CC}$).

# MC68701

## Advance Information

### MC68701 MICROCOMPUTER UNIT (MCU)

The MC68701 is an 8-bit single chip microcomputer unit (MCU) which signif ... y enhances the capabilities of the M6800 family of parts. It can be used in production systems to allow for easy firmware changes with minimum delay or it can be used to emulate the MC6801/03 for software development. It includes an upgraded M6800 microprocessor unit (MPU) with upward source and object code compatibility. Execution times of key instructions have been improved and several new instructions have been added including an unsigned multiply. The MCU can function as a monolithic microcomputer or can be expanded to a 64K byte address space. It is TTL compatible and requires one + 5 volt power supply for nonprogramming operation. An additional Vpp power supply is needed for EPROM programming. On-chip resources include 2048 bytes of EPROM, 128 bytes of RAM, Serial Communications Interface (SCI), parallel I/O, and a three function Programmable Timer. A summary of MCU features includes:

- Enhanced MC6800 Instruction Set
- 8 × 8 Multiply Instruction
- Serial Communications Interface (SCI)
- Upward Source and Object Code Compatibility with the MC6800
- 16-Bit Three-Function Programmable Timer
- Single-Chip or Expanded Operation to 64K Byte Address Space
- Bus Compatibility with the M6800 Family
- 2048 Bytes of UV Erasable, User Programmable ROM (EPROM)
- 128 Bytes of RAM (64 Bytes Retainable on Powerdown)
- 29 Parallel I/O and Two Handshake Control Lines
- Internal Clock Generator with Divide-by-Four Output
- 40 to 85°C Temperature Range

L SUFFIX
CERAMIC PACKAGE
CASE 715

### PIN ASSIGNMENT

| | | |
|---|---|---|
| VSS | 1 | 40 E |
| XTAL1 | 2 | 39 SC1 |
| EXTAL 2 | 3 | 38 SC2 |
| NMI | 4 | 37 P30 |
| IRQ1 | 5 | 36 P31 |
| RESET/Vpp | 6 | 35 P32 |
| Vcc | 7 | 34 P33 |
| P20 | 8 | 33 P34 |
| P21 | 9 | 32 P35 |
| P22 | 10 | 31 P36 |
| P23 | 11 | 30 P37 |
| P24 | 12 | 29 P40 |
| P10 | 13 | 28 P41 |
| P11 | 14 | 27 P42 |
| P12 | 15 | 26 P43 |
| P13 | 16 | 25 P44 |
| P14 | 17 | 24 P45 |
| P15 | 18 | 23 P46 |
| P16 | 19 | 22 P47 |
| P17 | 20 | 21 Vcc Standby |

#### GENERIC INFORMATION

| Package Type | Frequency (MHz) | Temperature | Generic Number |
|---|---|---|---|
| Ceramic L Suffix | 1 0 | 0°C to 70°C | MC68701L |
| | 1 0 | 40°C to 85°C | MC68701CL |
| | 1 25 | 0°C to 70°C | MC68701L 1 |
| | 1 25 | 40°C to 85°C | MC68701CL 1 |
| | 1 5 | 0°C to 70°C | MC68A701L |
| | 2 0 | 0°C to 70°C | MC68B701L |

# MC68701

MC68701 MICROCOMPUTER BLOCK DIAGRAM



## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | V |
| Input Voltage | $V_{in}$ | -0.3 to +7.0 | V |
| Operating Temperature Range<br>MC68701<br>MC68701C | $T_A$ | $T_L$ to $T_H$<br>0 to 70<br>-40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | 0 to 85 | °C |

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Rating |
|---|---|---|---|
| Thermal Resistance<br>Ceramic Package | $\theta_{JA}$ | 50 | °C/W |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g. either $V_{SS}$ or $V_{CC}$).

## POWER CONSIDERATIONS

The average chip-junction temperature, $T_J$, in °C can be obtained from

$$T_J = T_A + (P_D \cdot \theta_{JA}) \tag{1}$$

Where

$T_A$ = Ambient Temperature, °C

$\theta_{JA}$ = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT}$ = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \blacktriangleleft P_{INT}$ and can be neglected. $P_{PORT}$ may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between $P_D$ and $T_J$ (if $P_{PORT}$ is neglected) is

$$P_D = K - (T_J + 273°C) \tag{2}$$

Solving equations 1 and 2 for K gives

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \tag{3}$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

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## THE MC68881 FLOATING-POINT CO-PROCESSOR

The MC68881 is a high-performance HMOS floating-point processor designed to interface with the advanced MC68020 microprocessor. It can also be used as a peripheral in systems with other processors. The MC68881 is a comprehensive floating-point co-processor that provides a wide range of floating point capabilities seldom found even in a large main frame computer. System performance with the MC68020 is the overriding design goal of the MC68881

### ARCHITECTURE

The architecture of the MC68881 was defined as an extension to the architecture of the M68000 Family. It is a register-oriented processor. The programmer's model for the MC68881 is shown in Figure 1

FIGURE 1 — PROGRAMMER'S MODEL



```
79                                                                          0
┌──────────────────────────────────────────────────────────────────────────┐
│                      Floating-Point Data Register 0                        │
│                      Floating-Point Data Register 1                        │
│                      Floating-Point Data Register 2                        │
│                      Floating-Point Data Register 3                        │
│                      Floating-Point Data Register 4                        │
│                      Floating-Point Data Register 5                        │
│                      Floating-Point Data Register 6                        │
│                      Floating-Point Data Register 7                        │
└──────────────────────────────────────────────────────────────────────────┘
```

```
15                  0
┌───────────────────┐
│     Control       │
│    Exception      │
│ Accrued Exception │
└───────────────────┘
   Condition Codes →  └──┴──┘
```

```
31                          1  0
┌──────────────────────────────┐
│      Instruction Address      │
└──────────────────────────────┘
```
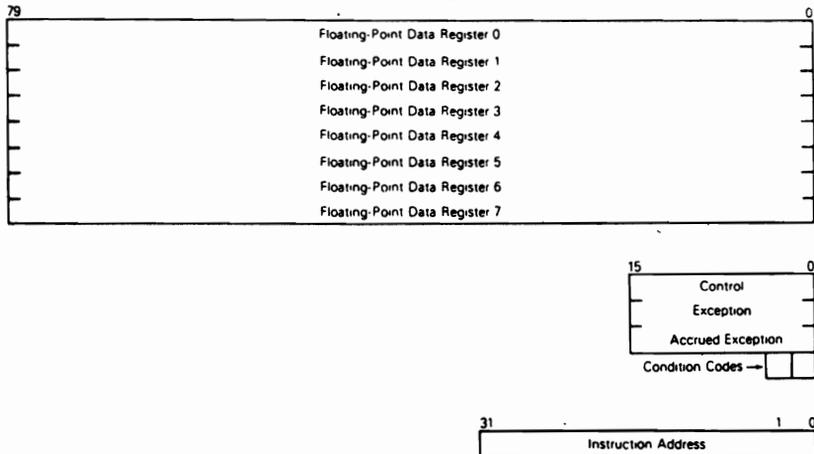
There are eight 80-bit floating-point data registers. These registers always hold full extended precision numbers. The control word contains the user selectable modes. The accrued exception word contains the logical inclusive OR of the exceptions for all operations since the last clear of the accrued exception register. The exception word contains the exception(s) of the last operation only. The condition code register holds the result of the last compare instruction

The instruction address register contains the address in main processor memory of the last instruction executed by the co-processor. This address can be used during an error trap to determine the address of the faulty instruction.

### ARCHITECTURAL DETAILS

#### Data Types

The MC68881 incorporates four new data types. They are:

Single Precision Real (S)
Double Precision Real (D)
Double-Extended Precision Real (X)
Packed Real BCD String (P)

In the assembly language syntax these new data types are handled in the same manner as the existing byte, word, and long word data types. The suffixes S, D, X, and P are appended to the opcode

## Operation Types

The operations on the MC68881 can be broken into five major types. They are

Dyadic Operations (2 operands)
Monadic Operations (1 operand)
Moves and Conversions
Conditional Tests
Control Operations

**Dyadic Operations** — All dyadic operations have as their source argument a MC68020 memory location, a MC68020 data register, or a floating-point data register. The source is converted to double-extended precision, if not already such. The destination argument is always a floating-point data register. The result is returned to the floating-point data register defined as the destination argument

**Monadic Operations** — The monadic instructions only have one argument. It is either in MC68020 memory, an MC68020 data register, or in a floating-point register. It is always converted to double-extended precision format, if it is not already. The destination is always a floating-point register

**Moves and Conversions** — Conversion to double-extended precision format is implicit in the move-in portion of the dyadic or monadic operation. Similarly, data contained in floating-point registers may be converted to other formats as operands are moved out of the MC68881

**Conditional Test** — The conditional instructions are the FBcc and FScc which are identical to the M68000 Family instructions Bcc and Scc except they use the MC68881's condition codes for determining the truth of the condition

**Control Operations** — The control instructions are used to set modes in the control register and to read the exception, accrued exception, and instruction address registers

### Co-Processor Interface

The co-processor interface designed by Motorola is an integral part of the design of both the MC68020 and the MC68881 design. The interface is clean and simple with the MC68020 and MC68881 sharing the tasks of the interface. The MC68020 provides services for the MC68881 at the co-processor's request. The services provided by the MC68020 are the ones done more efficiently by the main processor

On the other hand, the MC68881 does not depend on the MC68020 for all services as do some co-processor schemes. Once the MC68020 has provided the services requested by the MC68881 (which may be none) it is free to continue processing. Thus the choice of concurrency or non-currency is determined on an instruction-by-instruction basis and is determined by the co-processor. The great majority of MC68881 instructions are in fact overlapped in execution with MC68020 instructions

Since the co-processor interface is simple and flexible, it opens up the possibility of user-created co-processors. For this and other reasons the co-processor interface allows multiple co-processors in a system. Furthermore, the same handshaking that occurs between the main CPU and the co-processor can be simulated in software on CPUs that do not have the co-processor interface, by treating the MC68881 as a peripheral

Lastly, the co-processor interface was designed with the ever growing M68000 Family in mind. The MC68881 is fully compatible with all future and existing M68000 parts including the M68450 DMA Controller, the M68451 Memory Management Unit, and the MC68020's cache memory. It also supports true virtual memory

### Implementation

The MC68881 is a microcoded processor whose complexity is on the order of the MC68020 itself. It will be built using Motorola's advanced HMOS III process

The hardware consists of a high-speed 67-bit ALU for manipulating mantissa bits. The hardware also includes a barrel shifter that can shift from 1 bit to 67 bits in one machine cycle. The barrel shifter not only speeds up standard arithmetic functions, but is also a fundamental part of transcendental function implementation. Since argument reduction for transcendental functions will be performed by the microcode, the number of functions provided will be dependent on the available microcode space

### THE IEEE FLOATING POINT STANDARD

The MC68881 is a conforming implementation of the proposed standard. In fact it not only supports all the *required* features and functions of the proposed standard, but also implements most of the *suggested* features as well. Further, the MC68881 conforms without the need for any software external to the processor. All operations take place in high-speed hardware

## Data Format Conformance

The MC68881 supports three data sizes defined by the proposed standard. They are single, double, and double-extended. (The single-extended type is redundant when these three are included; all references in this document which refer to "extended" imply "double-extended".) The format for all three data types has the basic organization of

| s | e | m |
|---|---|---|

where
s = sign
e = exponent
m = mantissa

The sizes of each field for the three floating-point formats are

| | Size in Bits | | |
|---|---|---|---|
| | Single | Double | Extended |
| Sign | 1 | 1 | 1 |
| Exponent | 8 | 11 | 15 |
| Mantissa | 23 | 52 | 64 |
| Total | 32 | 64 | 80 |

The three formats described above are the formats which are assumed by floating-point numbers in user's memory. Each time one of these numbers is transferred to the MC68881 it is converted into an extended real number. Thereafter, all operations in the co-processor take place with full extended precision. Even integers and BCD strings are converted into 80-bit numbers when they are loaded into an MC68881 data register. This means that the MC68881 supports mixed mode arithmetic

## Data Type Conformance

The proposed standard requires that not only must normalized numbers be recognized, but that special data types must also be recognized. The largest and smallest exponents are reserved for these special data types

Positive True Zero
Negative True Zero
Plus Infinity
Minus Infinity
Denormalized Numbers
Not-a-Number (NaN's)

## Operation Conformance

All operations specified by the proposed standard are supplied in full precision by the MC68881. The arithmetic operations provided are

Add
Subtract
Multiply
Divide
Remainder
Compare
Square Root
Integer Part

## MODE CONFORMANCE

**Rounding Modes** — The MC68881 supports all four rounding modes specified in the standard:

Round to Nearest
Round Towards Plus Infinity
Round Towards Minus Infinity
Round Towards Zero

**Rounding Precisions** — Even though the MC68881 does all arithmetic to full 80-bit precision, sometimes it is desirable to round the 80-bit result to the precision of a single or double result. The three choices are:

Round to Extended (Default)
Round to Double
Round to Single

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**Infinity Closures** -- Two types of infinity closures are also defined by the standard and supported in the MC68881 *Affine* closure defines a number system where both plus and minus infinity exist and are at opposite ends of the number line

In *projective* closure, infinity is unsigned and the number system can be thought of as a circle which includes all numbers

### Error Handling Conformance

The proposed standard provides for the hardware to trap if an error occurs. On the MC68020/MC68881 if an error occurs on an enabled trap, the MC68881 will signal the MC68020 to take a trap and will supply a vector number. In other words, floating point exception traps are handled just like any other MC68020 traps. No external glue parts are required and there is no possibility of dead-lock

### BEYOND THE IEEE PROPOSAL

The MC68881 offers many features and functions beyond those required or suggested by the IEEE

### Additional Instructions

Some of the additional instructions provided in the MC68881 are

Absolute Value
Negate
Scale Exponent
Set Byte determined by Floating-Point Condition
Branch on Floating-Point Condition
Get Index Based on Floating-Point Type
Move Constant to Floating-Point Register
Get Fraction of Floating-Point Number
Get Exponent of Floating-Point Number
Modulo

### Transcendentals

The MC68881 includes on-chip hardware for evaluation of transcendental functions. The functions planned are.

Sine x
Cosine x
Arc Tangent x
Log Base 2
$e^x$
Log Base e

The following functions will also be provided if there is adequate space in the microcode after the above functions are included:

Tangent x
Hyperbolic Arc Tangent
Hyperbolic Sine
Hyperbolic Cosine
Hyperbolic Tangent
Log Base 10
Log Base 2
$10^x$
$y^x$

Each of these functions is calculated to double-extended precision

### SUMMARY

The MC68881 is the most comprehensive floating-point processor. It provides all the required functions and features of the proposed IEEE standard in hardware. In addition many other functions are provided to round out the support necessary in most numeric programs. The architecture is a logical extension to the M68000 Family architecture and is clean and easy to use. Furthermore, it lends itself to being moved onto the main processor in the future. The co-processor interface was designed with a great deal of thought; not only to allow it to work well with the MC68881, but also to allow for future co-processors, multiple co-processors, and user defined co-processors. Lastly, the MC68881 is being designed with state-of-the-art hardware and all-out performance as the primary design goal

# MC68851

## Product Preview

### THE MC68851 HCMOS PAGED MEMORY MANAGEMENT UNIT (PMMU)

The MC68851 is a high-performance HCMOS paged memory management unit (PMMU) designed to efficiently support a demand paged virtual memory environment as a coprocessor with the MC68020 advanced microprocessor The MC68851 can also be used as a peripheral with other processors, especially the MC68010 The MC68851 provides an efficient means of paging and access control The implementation of a comprehensive paged memory management system is facilitated by utilizing the following MC68851 features:

- Very Fast Logical-to-Physical Address Translation
- Logical Address Consists of a 4-Bit Function Code and a 32-Bit Address
- Full 32-Bit Physical Address
- Eight Available Page Sizes from 256 to 32K Bytes
- Fully Associative 64 Entry On-Chip Translation Cache
- Translation Cache Can Hold Descriptors for Multiple Processes
- Internal Hardware Maintains Translation Tables and On-Board Cache
- MC68020 Instruction Set Extension and Instruction Oriented Interface Using M68000 Family Coprocessor Interface
- Supports Linear Address Space of 4 Gigabytes or a Hierarchical Protection Mechanism with Eight Levels of Privilege/Protection
- Supports Multiple Logical and/or Physical Bus Masters
- Supports Logical and/or Physical Data Cache
- Supports Instruction Breakpoints for Software Debugging and Program Control

The primary system functions of the MC68851 are to provide logical-to-physical address translation, to monitor and enforce the protection/privilege mechanism, and to support the breakpoint operations. The MC68851 also supports the M68000 Family coprocessor interface in order to simplify processor/coprocessor communication

### ADDRESS TRANSLATION

Logical-to-physical address translation is the most frequently executed operation of the MC68851 and, as such, this task has been optimized and requires minimal processor intervention The logical address operated on by the MC68851 consists of the 32-bit incoming logical address and a 4-bit function code

The MC68851 initiates an address translation by searching for the page descriptor corresponding to the logical-to-

physical mapping in the on-chip translation-lookaside module (TLM) The TLM is a very fast 64-entry fully-associative cache memory which stores recently used page descriptors If the descriptor does not reside in the TLM, then the bus cycle of the logical bus master is aborted and the MC68851 executes bus cycles to search the translation table in physical memory The translation table is a hierarchical structure in main memory that, at its lowest level, contains the page descriptors controlling the logical-to-physical address translations The 64-bit primary root pointer registers in the MC68851 (see Figure 1) point to the head of these translation tables The page descriptor is loaded into the TLM and the logical bus master is allowed to retry its bus cycle, which should now be correctly translated

### PROTECTION MECHANISM

The MC68851 hierarchical protection mechanism provides cycle-by-cycle examination and enforcement of the access rights of the currently executing process There are eight distinct levels in the privilege hierarchy and these levels are encoded in the upper three bits of the incoming logical address LA (31-29). The MC68851 compares these bits against the value in the current access level register (CAL in Figure 1) If the priority level of the incoming address is less than the current access level, then the bus cycle is requesting a higher privilege than allowed and the MC68851 will terminate this access as a fault. The MC68851 will not assert a physical address strobe during a bus cycle resulting in a privilege violation

The MC68851 completely supports the MC68020 module call and return functions (CALLM/RTM), which include a mechanism to change privilege levels during module operation

### BREAKPOINTS

The MC68851 provides a breakpoint acknowledge facility to support the MC68020 and other processors with on-chip cache memory. When the MC68020 encounters a breakpoint instruction it executes a breakpoint acknowledge cycle by reading a particular address in CPU address space The PMMU decodes this address and responds by either providing a replacement opcode for the breakpoint opcode and asserting the data size and acknowledge outputs or by asserting bus error to initiate illegal instruction processing The PMMU can be programmed to signal the illegal instruction exception or to provide the replacement opcode n times $(1 \leq n \geq 255)$ before signaling the exception

```
63                              32
        CPU Root
         Pointer
31                               0

        DMA Root
         Pointer

      Supervisor Root
         Pointer

      Translation Control
15                    0
      Cache Status

        Status
7           0
   CAL        VAL         SCC

      Access Control

BAD0            BAC0
BAD1            BAC1
BAD2            BAC2
BAD3            BAC3
BAD4            BAC4
BAD5            BAC5
BAD6            BAC6
BAD7            BAC7
```

Translation Control
Registers

Protection Control
Registers

Breakpoint Acknowledge
Data and Control
Registers
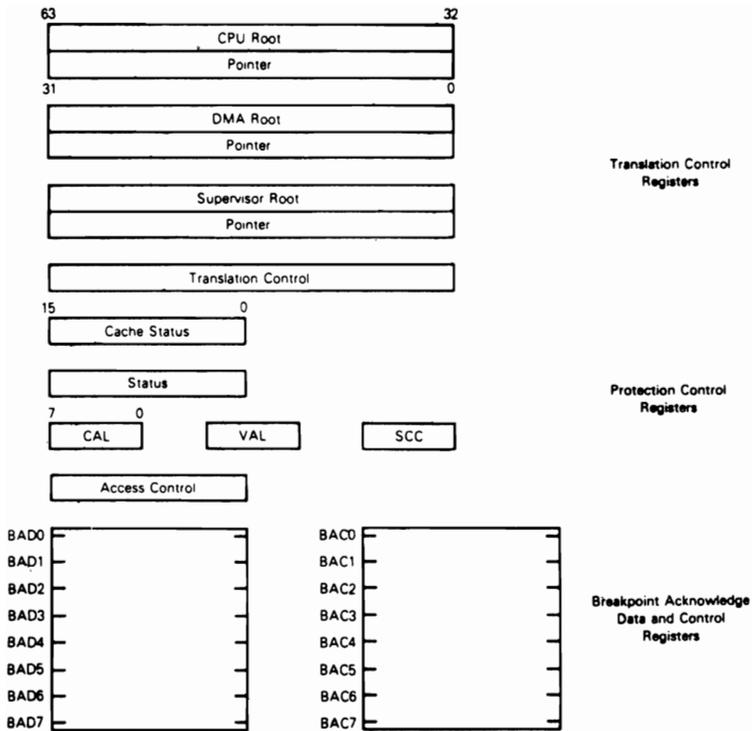
## COPROCESSOR INTERFACE

The M68000 Family coprocessor interface is an integral part of the design of the MC68020 advanced microprocessor, the MC68881 floating-point processor, and the MC68851 paged memory management unit. The coprocessor interface allows the execution of special purpose instructions which are not executable by the processor. Each coprocessor (e g., MC68851 or MC68881) has an instruction set that reflects its special function. These instructions may be executed merely by placing the instruction opcode and parameters in the MC68020 instruction stream. The MC68020 decodes the coprocessor instruction and performs bus communication with the coprocessor registers specifying the nature of the action to be taken. Both the MC68020 and the coprocessor will execute parts of the instruction depending on which is best suited to handle a particular task.

The interchange of information and the division of responsibility between the processor and the coprocessor are controlled by the coprocessor interface and this process is transparent to the user. The addition of a coprocessing unit to an MC68020 system simply complements the instruction set executable by the processor.

The coprocessor interface was designed to be flexible, functional, and expandable. The interface is intended to support the M68000 Family of devices and future extensions to the Motorola coprocessor family, as well as user defined coprocessors in single or multiple coprocessor systems.

## M68000 FAMILY INSTRUCTION SET EXTENSION

The MC68851 implements an extension of the current M68000 Family instruction set using the M68000 Family coprocessor interface. These instructions provide control functions for

1 loading and storing of MMU registers,
2 testing access rights and conditionals based on the result of these tests, and
3 MMU control functions

The instruction set extension is as follows

**PMOVE** — Moves data to/from MC68851 register

**PVALID** — Compares access rights requested by logical address and traps if it is less than the current access level.

**PTEST** — Searches the translation tables to determine the access rights to an effective address. Sets the MC68851 status register according to the results.

**PFLUSH** — Flush translation cache entries by root pointer, by root pointer and effective address, or by root pointer, effective address, and function code

**PSAVE** — Saves the internal state of the MC68851 coprocessor interface in order to support the MC68020 virtual memory capabilities.

**PRESTORE** — Restores the state of the coprocessor interface stored by the PSAVE instruction.

**PBcc** — Branches conditionally on MC68851 condition

**PDBcc** — Tests MC68851 condition, decrements, and branches.

**PScc** — Tests operand according to MC68851 condition

**PTRAPcc** — Traps on MC68851 condition

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MC68881 connected in a MC68020 system
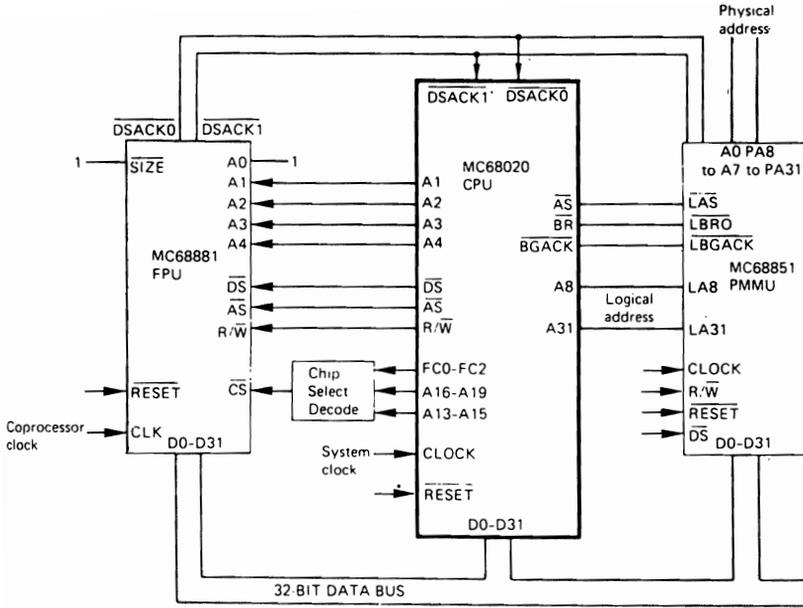
## Number of bits in each field for three types of floating-point data size

|  | Single | Double | Double Extended |
|---|---|---|---|
| Sign | 1 | 1 | 1 |
| Exponent | 8 | 11 | 15 |
| Mantissa | 23 | 52 | 64 |
| Total | 32 | 64 | 80 |
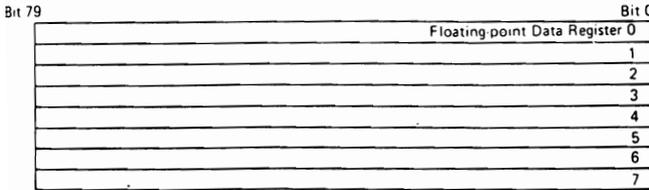


Internal registers of the MC68881

565
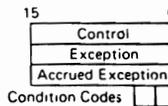
# Z8001/2 Z8000® CPU
# Central Processing Unit

# Product
# Specification

## FEATURES

- Regular, easy-to-use architecture

- Instruction set more powerful than many mirficomputers

- Directly addresses 8 Mbytes

- Eight user-selectable addressing modes

- Seven data types that range from bits to 32-bit long words and byte and word strings

- System and Normal operating modes

- Separate code, data, and stack spaces

- Sophisticated interrupt structure

- Resource-shaping capabilities for multiprocessing systems

- Multi-programming support

- Compiler support

- Memory management and protection provided by Z8010 Memory Management Unit

- 32-bit operations, including signed multiply and divide

- Z-BUS compatible

- 4, 6, and 10 MHz clock rate

## GENERAL DESCRIPTION

The Z8000 is an advanced high-end 16-bit microprocessor that spans a wide variety of applications ranging from simple stand-alone computers to complex parallel-processing systems. Essentially a monolithic minicomputer central processing unit, the Z8000 CPU is characterized by an instruction set more powerful than many minicomputers; abundant resources in registers, data types, addressing modes and addressing range, and a regular architecture that enhances throughput by avoiding critical bottlenecks such as implied cr dedicated registers.

CPU resources include sixteen 16-bit general-purpose registers, seven data types that range from bits to 32-bit long words and byte and word strings, and eight user-selectable addressing modes. The 110 distinct instruction types can be combined with the various data types and addressing modes to form a powerful set of 414 instructions. Moreover, the instruction set is regular; most instructions can use any of the five main addressing modes and can operate on byte, word, and long-word data types.

The CPU can operate in either the system or normal mode. The distinction between these two modes permits privileged operations, thereby improving operating system organization and implementation. Multiprogramming is supported by the "atomic" Test and Set instruction; multiprocessing by a combination of instruction and
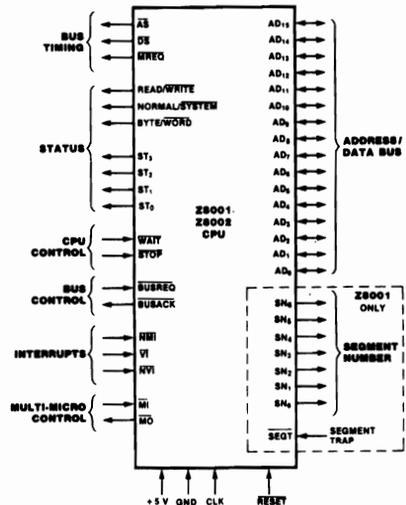


Figure 1. Z8000 CPU Pin Functions

hardware features; and compilers by multiple stacks, special instructions, and addressing modes.

The Z8000 CPU is offered in two versions: the Z8001 48-pin segmented CPU and the Z8002 40-pin nonsegmented CPU (Figure 1). The main difference between the two is in addressing range. The Z8001 can directly address 8 megabytes of memory; the Z8002 directly addresses 64 kilobytes. The two operating modes—system and normal—and the distinction between code, data, and stack spaces within each mode allows memory extension up to 48 megabytes for the Z8001 and 384 kilobytes for the Z8002.

To meet the requirements of complex, memory-intensive applications, a companion memory-management device is offered for the Z8001 The Z8010 Memory Management Unit manages the large address space by providing features such as segment relocation and memory protection. The Z8001 can be used with or without the Z8010. If used by itself, the Z8001 still provides an 8 megabyte direct addressing range, extendable to 48 megabytes.

The Z8001, Z8002, and Z8010 are fabricated with high-density, high-performance scaled n-channel silicon-gate depletion-load technology, and are housed in dual-in-line packages (DIPs) and leadless chip carriers (LCC).

## REGISTER ORGANIZATION

The Z8000 CPU is a register-oriented machine that offers sixteen 16-bit general-purpose registers and a set of special system registers. All general-purpose registers can be used as accumulators and all but one as index registers or memory pointers

Register flexibility is created by grouping and overlapping multiple registers (Figures 2 and 3). For byte operations, the first eight 16-bit registers (R0... R7) are treated as sixteen 8-bit registers (RL0, RH0..., RL7, RH7). The sixteen 16-bit registers are grouped in pairs (RR0... RR14) to form 32-bit long-word registers. Similarly, the register set is grouped in quadruples (RQ0... RQ12) to form 64-bit registers.
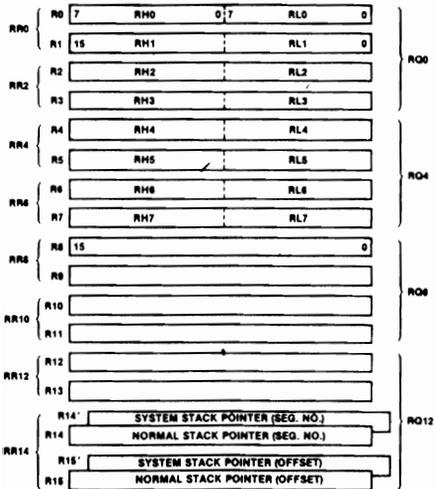


Figure 2. Z8001 General-Purpose Registers
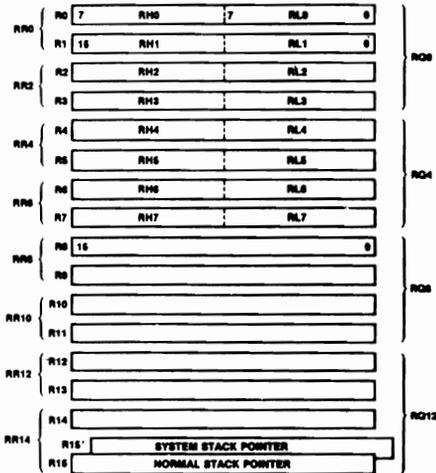


Figure 3. Z8002 General-Purpose Registers

## STACKS

The Z8001 and Z8002 can use stacks located anywhere in memory. Call and Return instructions as well as interrupts and traps use implied stacks. The distinction between normal and system stacks separates system information from the application program information. Two stack pointers are available: the system stack pointer and the normal stack pointer. Because they are part of the general-purpose register group, the user can manipulate the stack pointers with any instruction available for register operations.

In the Z8001, register pair RR14 is the implied stack pointer. Register R14 contains the 7-bit segment number and R15 contains the 16-bit offset. In the Z8002, register R15 is the implied 16-bit stack pointer.

## REFRESH

The Z8000 CPU contains a counter that can be used to automatically refresh dynamic memory. The refresh counter register consists of a 9-bit row counter, a 6-bit rate counter, and an enable bit (Figure 4). The 9-bit row counter can address up to 256 rows and is incremented by two each time the rate counter reaches end-of-count. The rate counter determines the time between successive refreshes. It consists of a programmable 6-bit modulo-n prescaler (n = 1 to 64), driven at one-fourth the CPU clock rate. The refresh period can be programmed by 1 to 64 μs with a 4 MHz clock. Refresh can be disabled by programming the refresh enable/disable bit.



**Figure 4. Refresh Counter**

## PROGRAM STATUS INFORMATION

This group of status registers contains the program counter, flags, and control bits. When an interrupt or trap occurs, the entire group is saved and a new program status group is loaded.

Figure 5 illustrates how the program status groups of the Z8001 and Z8002 differ. In the nonsegmented Z8002, the program status group consists of two words: the program counter (PC), and the flag and control word (FCW). In the segmented Z8001, the program status group consists of four words: a two-word program counter, the flag and control word, and an unused word reserved for future use. Seven bits of the first PC word designate one of the 128 memory segments. The second word supplies the 16-bit offset that designates a memory location within the segment.

With the exception of the segment enable bit in the Z8001 program status group, the flags and control bits are the same for both CPUs.
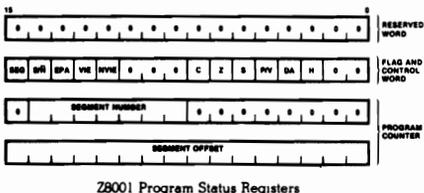


Z8001 Program Status Registers
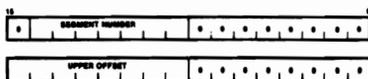
Z8001 Program Status Area Pointer
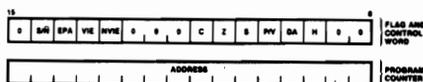
Z8002 Program Status Registers
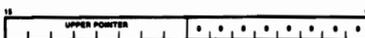
Z8002 Program Status Area Pointer

**Figure 5. Z8000 CPU Special Registers**

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## INTERRUPT AND TRAP STRUCTURE

The Z8000 provides a very flexible and powerful interrupt and trap structure. Interrupts are external asynchronous events requiring CPU attention, and are generally triggered by peripherals needing service. Traps are synchronous events resulting from the execution of certain instructions. Both are processed in a similar manner by the CPU.

The CPU supports three types of interrupts (non-maskable, vectored, and non-vectored) and four traps [system call, Extended Process Architecture (EPA) instruction, privileged instructions, and segmentation trap]. The vectored and non-vectored interrupts are maskable. Of the four traps, the only external one is the segmentation trap, which is generated by the Z8010.

The remaining traps occur when instructions limited to the system mode are used in the normal mode, or as a result of the System Call instruction, or for an EPA instruction. The descending order of priority for traps and interrupts is: internal traps, nonmaskable interrupt, segmentation trap, vectored interrupt, and non-vectored interrupt.

When an interrupt or trap occurs, the current program status is automatically pushed on the system stack. The program status consists of the processor status (PC and FCW) plus a 16-bit identifier. The identifier contains the reason or source of the trap or interrupt. For internal traps, the identifier is the first word of the trapped instruction. For external traps or interrupts, the identifier is the vector on the data bus read by the CPU during the interrupt-acknowledge or trap-acknowledge cycle.

After saving the current program status, the new program status is automatically loaded from the program status area in system memory. This area is designated by the program status area pointer (PSAP).

## DATA TYPES

Z8000 instructions can operate on bits, BCD digits (4 bits), bytes (8 bits), words (16 bits), long words (32 bits), and byte strings and word strings (up to 64 kilobytes long). Bits can be set, reset, and tested; digits are used in BCD arithmetic operations; bytes are used for characters or small integer values; words are used for integer values, instructions and nonsegmented addresses; long words are used for long integer values and segmented addresses. All data elements except strings can reside either in registers or memory. Strings are stored in memory only.

The basic data element is the byte. The number of bytes used when manipulating a data element is either implied by the operation or—for strings and multiple register operations—explicitly specified in the instruction.

## SEGMENTATION AND MEMORY MANAGEMENT

High-level languages, sophisticated operating systems, large programs and data bases, and decreasing memory prices are all accelerating the trend toward larger memory requirements in microcomputer systems. The Z8001 meets this requirement with an eight megabyte addressing space. This large address space is directly accessed by the CPU using a segmented addressing scheme and can be managed by the Z8010 Memory Management Unit.

### Segmented Addressing

A segmented addressing space—compared with linear addressing—is closer to the way a programmer uses memory because each procedure and data space resides in its own segment. The 8 megabytes of Z8001 addressing space is divided into 128 relocatable segments up to 64 kilobytes each. A 23-bit segmented address uses a 7-bit segment address to point to the segment, and a 16-bit offset to address any location relative to the beginning of the segment. The two parts of the segmented address may be manipulated separately. The segmented Z8001 can run any code written for the nonsegmented Z8002 in any one of its 128 segments, provided it is set to the nonsegmented mode.
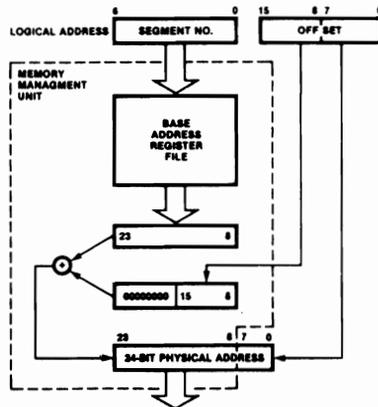


Figure 6. Logical-to-Physical Address Translation

In .hardware, segmented addresses are contained in a register pair or long-word memory location. The segment number and offset can be manipulated separately or together by all the available word and long-word operations.

When contained in an instruction, a segmented address has two different representations: long offset and short offset. The long offset occupies two words, whereas the short offset requires only one and combines in one word the 7-bit segment number with an 8-bit offset (range 0-256). The short offset mode allows very dense encoding of addresses and minimizes the need for long addresses required by direct accessing of this large address space.

**Memory Management**

The addresses manipulated by the programmer, used by instructions and output by the Z8001, are called *logical* addresses. The Memory Management Unit takes the logical addresses and transforms them into the *physical* addresses required for accessing the memory (Figure 6). This address transformation process is called relocation. Segment relocation makes user software addresses independent of the physical memory so the user is freed from specifying

where information is actually located in the physical memory.

The relocation process is transparent to user software. A translation table in the Memory Management Unit associates the 7-bit segment number with the base address of the physical memory segment. The 16-bit offset is added to the physical base address to obtain the actual physical address. The system may dynamically reload translation tables as tasks are created, suspended, or changed.

In addition to supporting dynamic segment relocation, the Memory Management Unit also provides segment protection and other segment management features. The protection features prevent illegal uses of segments, such as writing into a write-protected zone.

Each Memory Management Unit stores 64 segment entries that consist of the segment base address, its attributes, size, and status. Segments are variable in size from 256 bytes to 64 kilobytes in increments of 256 bytes. Pairs of Management Units support the 128 segment numbers available for each of the six CPU address spaces. Within an address space, several Management Units can be used to create multiple translation tables.

# EXTENDED PROCESSING ARCHITECTURE

The Zilog Extended Processing Architecture (EPA) provides an extremely flexible and modular approach to expanding both the hardware and software capabilities of the Z8000 CPU. Features of the EPA include:

- Specialized instructions for external processors or software traps may be added to CPU instruction set.

- Increases throughput of the system by using up to four specialized external processors in parallel with the CPU.

- Permits modular design of Z8000-based systems.

- Provides easy management of multiple microprocessor configurations via "single instruction stream" communication.

- Simple interconnection between extended processing units and Z8000 CPU requires no additional external supporting logic.

- Supports debugging of suspect hardware against proven software.

- Standard features on all Zilog Z8000 CPUs.

Specific benefits include:

- EPUs can be added as the system grows and as EPUs with specialized functions are developed.

- Control of EPUs is accomplished via a "single instruction stream" in the Z8000 CPU, eliminating many significant system software and bus contention management obstacles that occur in other multiprocessor (e.g., master-slave) organization schemes.

The processing power of the Zilog Z8000 16-bit microprocessor can be boosted beyond its intrinsic capability by Extended Processing Architecture. Simply stated, EPA allows the Z8000 CPU to accommodate up to four Extended Processing Units (EPUs), which perform specialized functions in parallel with the CPU's main instruction execution stream (Figure 7).

The use of extended processors to boost the main CPU's performance capability has been proven with large mainframe computers and minicomputers. In these systems, specialized functions such as array processing, special input/output processing, and data communications processing are typically assigned to extended processor hardware. These extended processors are complex computers in their own right.

The Zilog Extended Processing Architecture combines the best concepts of these proven performance boosters with the latest in high-density MOS integrated-circuit design. The result is an elegant expansion of design capability—a powerful microprocessor architecture capable of connecting single-chip EPUs that permits very effective parallel processing and makes for a smoothly integrated instruction stream from the Z8000 programmer's point of view. A typical addition to the current Z8000 instruction set is a set of Floating Point Instructions.

The Extended Processing Units connect directly to the Z8000 Bus (Z-BUS) and continuously monitor the CPU instruction stream. When an extended instruction is detected, the appropriate EPU responds, obtaining or

placing data or status information on the Z-BUS using the Z8000-generated control signals and performing its function as directed

The Z8000 CPU is responsible for instructing the EPU and delivering operands and data to it. The EPU recognizes instructions intended for it and executes them, using data supplied with the instruction and/or data within its internal registers. There are four classes of EPU instructions:

■ Data transfers between main memory and EPU registers

■ Data transfers between CPU registers and EPU registers

■ EPU internal operations

■ Status transfers between the EPUs and the Z8000 CPU Flag and Control Word register (FCW)

Four Z8000 addressing modes may be utilized with transfers between EPU registers and the CPU and main memory.

■ Register

■ Indirect Register

■ Direct Address

■ Index

In addition to the hardware-implemented capabilities of the Extended Processing Architecture, there is an extended instruction trap mechanism to permit software simulation of EPU functions A control bit in the Z8000 FCW register indicates whether actual EPUs are present or not. If not, when an extended instruction is detected, the Z8000 traps on the instruction, so that a software "trap handler" can emulate the desired EPU function—a very useful development tool. The EPA software trap routine supports the debugging of suspect hardware against proven software. This feature will increase in significance as designers become familiar with the EPA capability of the Z8000 CPU.

This software trap mechanism facilitates the design of systems for later addition of EPUs initially, the extended function is executed as a trap subroutine, when the EPU is finally attached, the trap subroutine is eliminated and the EPA control bit is set Application software is unaware of the change

Extended Processing Architecture also offers protection against extended instruction overlapping Each EPU connects to the Z8000 CPU via the STOP line so that if an EPU is requested to perform a second extended instruction function before it has completed the previous one, it can put the CPU into the Stop/Refresh state until execution of the previous extended instruction is complete

EPA and CPU instruction execution are shown in Figure 8 The CPU begins operation by fetching an instruction and determining whether it is a CPU or an EPU command The EPU meanwhile monitors the Z-BUS for its own instructions If the CPU encounters an EPU command, it checks to see whether an EPU is present, if not, the EPU may be simulated by an EPU instruction trap software routine, if an EPU is present, the necessary data and/or address is placed on the Z-BUS. If the EPU is free when the instruction and data for it appear, the extended instruction is executed If the EPU is still processing a previous instruction, it activates the CPU's STOP line to lock the CPU off at the Z-BUS until execution is complete After the instruction is finished, the EPU deactivates the STOP line and CPU transactions continue
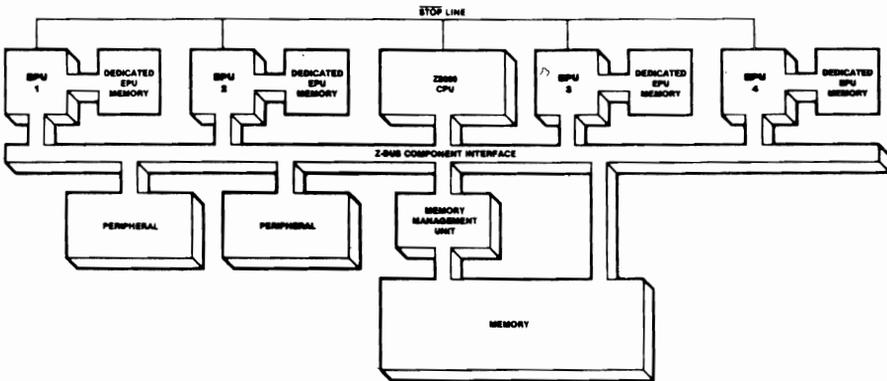


Figure 7. Typical Extended Processor Configuration
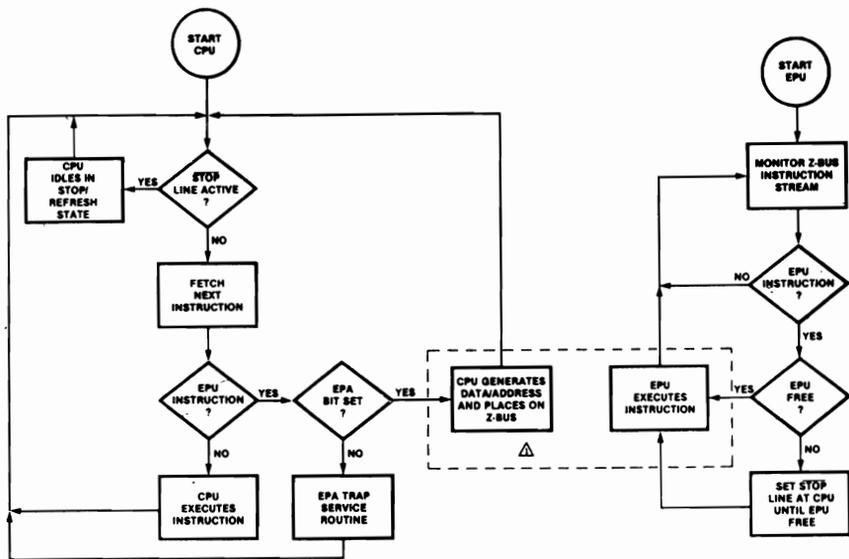
$\triangle$ DATA OR ADDRESSES ARE PLACED ON THE BUS AND USED BY THE EPU IN THE EXECUTION OF AN INSTRUCTION.

**Figure 8. EPA and Z8000 CPU Instruction Execution**

## INPUT/OUTPUT

A set of I/O instructions performs 8-bit or 16-bit transfers between the CPU and I/O devices. I/O devices are addressed with a 16-bit I/O port address. The I/O port address is similar to a memory address; however, I/O address space need not be part of the memory address space. I/O port and memory addresses coexist on the same bus lines and they are distinguished by the status outputs.

Two types of I/O instructions are available: standard and special. Each has its own address space. The I/O instructions include a comprehensive set of In, Out, and Block I/O instructions for both bytes and words. Special I/O instructions are used for loading and unloading the Memory Management Unit. The status information distinguishes between standard and special I/O references.

## MULTI-MICROPROCESSOR SUPPORT

Multi-microprocessor systems are supported in hardware and software. A pair of CPU pins is used in conjunction with certain instructions to coordinate multiple microprocessors. The Multi-Micro Out pin issues a request for the resource, while the Multi-Micro In pin is used to recognize the state of the resource. Thus, any CPU in a multiple microprocessor system can exclude all other asynchronous CPUs from a critical shared resource.

Multi-microprocessor systems are supported in software by the instructions Multi-Micro Request, Test Multi-Micro In, Set Multi-Micro Out, and Reset Multi-Micro Out. In addition, the eight megabyte CPU address space is beneficial in multiple microprocessor systems that have large memory requirements.

## ADDRESSING MODES

The information included in Z8000 instructions consists of the function to be performed, the type and size of data elements to be manipulated, and the location of the data elements. Locations are designated by register addresses, memory addresses, or I/O addresses. The addressing mode of a given instruction defines the address space it references and the method used to compute the address itself. Addressing modes are explicitly specified or implied by the instruction.

Figure 9 illustrates the eight addressing modes: Register (R), Immediate (IM), Indirect Register (IR), Direct Address (DA), Index (X), Relative Address (RA), Base Address (BA), and Base Index (BX). In general, an addressing mode explicitly specifies either register address space or memory address space. Program memory address space and I/O address space are usually implied by the instruction.

| Addressing Mode | Operand Addressing | | | Operand Value |
|---|---|---|---|---|
| | In the Instruction | In a Register | In Memory | |
| **R** Register | REGISTER ADDRESS → OPERAND | | | The content of the register |
| **IM** Immediate | OPERAND | | | In the instruction |
| **·IR** Indirect Register | REGISTER ADDRESS → ADDRESS | | → OPERAND | The content of the location whose address is in the register |
| **DA** Direct Address | ADDRESS | | → OPERAND | The content of the location whose address is in the instruction |
| **·X** Index | REGISTER ADDRESS → INDEX / BASE ADDRESS | | → OPERAND | The content of the location whose address is the address in the instruction plus the content of the working register. |
| **RA** Relative Address | DISPLACEMENT / PC VALUE | | → OPERAND | The content of the location whose address is the content of the program counter, offset by the displacement in the instruction |
| **·BA** Base Address | REGISTER ADDRESS → BASE ADDRESS / DISPLACEMENT | | → OPERAND | The content of the location whose address is the address in the register, offset by the displacement in the instruction |
| **·BX** Base Index | REGISTER ADDRESS → BASE ADDRESS / REGISTER ADDRESS → INDEX | | → OPERAND | The content of the location whose address is the address in a register plus the index value in another register. |

*Do not use R0 or RR0 as indirect, index, or base registers.

**Figure 9. Addressing Modes**

## PIN DESCRIPTION

**AD$_0$-AD$_{15}$.** *Address/Data* (inputs/outputs, active High, 3-state). These multiplexed address and data lines are used for I/O and to address memory.

**$\overline{\text{AS}}$.** *Address Strobe* (output, active Low, 3-state). The rising edge of $\overline{\text{AS}}$ indicates addresses are valid.

**$\overline{\text{BUSACK}}$.** *Bus Acknowledge* (output active Low). A Low on this line indicates the CPU has relinquished control of the bus.

**$\overline{\text{BUSREQ}}$.** *Bus Request* (input, active Low). This line must be driven Low to request the bus from the CPU.

**B/$\overline{\text{W}}$.** *Byte/Word* (output, Low = Word, 3-state). This signal defines the type of memory reference on the 16-bit address/data bus.

**CLK.** *System Clock* (input). CLK is a 5V single-phase time-base input.

**$\overline{\text{DS}}$.** *Data Strobe* (output, active Low, 3-state). This line times the data in and out of the CPU.

**$\overline{\text{MREQ}}$.** *Memory Request* (output, active Low, 3-state). A Low on this line indicates that the address/data bus holds a memory address.

**$\overline{\text{MI}}$, $\overline{\text{MO}}$.** *Multi-Micro In, Multi-Micro Out* (input and output, active Low). These two lines form a resource-request daisy chain that allows one CPU in a multi-microprocessor system to access a shared resource.

**$\overline{\text{NMI}}$.** *Non-Maskable Interrupt* (edge triggered, input, active Low). A high-to-low transition on $\overline{\text{NMI}}$ requests a

non-maskable interrupt. The $\overline{\text{NMI}}$ interrupt has the highest priority of the three types of interrupts.

**N/$\overline{\text{S}}$.** *Normal/System Mode* (output, Low = System Mode, 3-state). N/$\overline{\text{S}}$ indicates the CPU is in the normal or system mode.

**$\overline{\text{NMI}}$.** *Non-Vectored Interrupt* (input, active Low). A Low on this line requests a non-vectored interrupt.

**$\overline{\text{RESET}}$.** *Reset* (input, active Low). A Low on this line resets the CPU.

**R/$\overline{\text{W}}$.** *Read/Write* (output, Low = Write, 3-state). R/$\overline{\text{W}}$ indicates that the CPU is reading from or writing to memory or I/O.

**$\overline{\text{SEGT}}$.** *Segment Trap* (input, active Low). The Memory Management Unit interrupts the CPU with a Low on this line when the MMU detects a segmentation trap. Input on Z8001 only.

**SN$_0$-SN$_6$.** *Segment Number* (outputs, active High, 3-state). These lines provide the 7-bit segment number used to address one of 128 segments by the Z8010 memory Management Unit. Output by the Z8001 only.

**ST$_0$-ST$_3$.** *Status* (outputs, active High, 3-state). These lines specify the CPU status (see Status Code Lines).

**$\overline{\text{STOP}}$.** *Stop* (input, active Low). This input can be used to single-step instruction execution.

**$\overline{\text{VI}}$.** *Vectored Interrupt* (input, active Low). A Low on this line requests a vectored interrupt.

**$\overline{\text{WAIT}}$.** *Wait* (input, active Low). This line indicates to the CPU that the memory or I/O device is not ready for data transfer.

Z8001/2 CPU
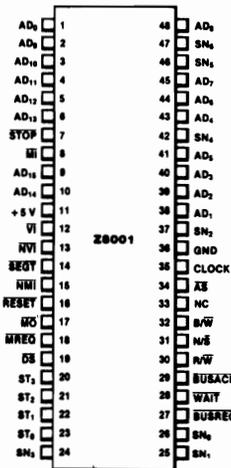


**Figure 10a. 48-pin Dual-In-Line Package (DIP), Pin Assignments**
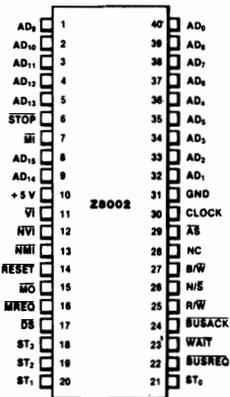


**Figure 11a. 40-pin Dual-In-Line Package (DIP), Pin Assignments**
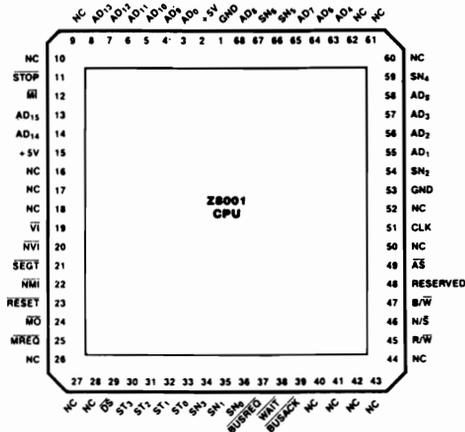
**Figure 10b. 68-pin Chip Carrier, Pin Assignments**
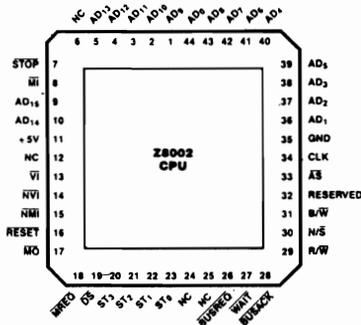


**Figure 11b. 44-pin Chip Carrier, Pin Assignments**

## Z8000 CPU TIMING

The Z8000 CPU executes instructions by stepping through sequences of basic machine cycles, such as memory read or write, I/O device read or write, interrupt acknowledge, and internal execution. Each of these basic cycles requires three to ten clock cycles to execute. Instructions that require more clock cycles to execute are broken up into several machine cycles. Thus no machine cycle is longer than ten clock cycles and fast response to a Bus Request is guaranteed.

The instruction opcode is fetched by a normal memory read operation. A memory refresh cycle can be inserted just after the completion of any first instruction fetch (IF₁) cycle and can also be inserted while the following instructions are being executed: MULT, MULTL, DIV, DIVL, HALT, all Shift instructions, all Block Move instructions, and the Multi-Micro

Request instruction (MREQ).

The following timing diagrams show the relative timing relationships of all CPU signals during each of the basic operations. When a machine cycle requires additional clock cycles for CPU internal operation, one to five clock cycles are added. Memory and I/O read and write, as well as interrupt acknowledge cycles, can be extended by activating the $\overline{\text{WAIT}}$ input. For exact timing information, refer to the composite timing diagram.

Note that the $\overline{\text{WAIT}}$ input is not synchronized in the Z8000 and that the setup and hold times for $\overline{\text{WAIT}}$, relative to the clock, must be met. If asynchronous $\overline{\text{WAIT}}$ signals are generated, they must be synchronized with the CPU clock before entering the Z8000.

# Z80,000™ CPU

# Preliminary Product Specification

## FEATURES

- Full 32-bit architecture and implementation
- 4G (billion) bytes of directly addressable memory
- Linear or segmented address space
- Virtual memory management integrated with CPU
- On-chip cache memory
- General-purpose register file with sixteen 32-bit registers
- Nine general addressing modes
- Numerous data types include bit, bit field, logical value, signed integer, and string
- Extended Processing Architecture supports floating-point operations

- Regular use of operations, addressing modes, and data types in instruction set
- System and normal modes of operation with separate stacks
- Sophisticated interrupt and trap handling
- Software is a binary-compatible extension of Z8000™ software
- Hardware is compatible with other Z-BUS™ components
- Mainframe performance

## GENERAL DESCRIPTION

The Z80,000 CPU is an advanced, high-end 32-bit microprocessor that integrates the architecture of a mainframe computer into a single chip. While maintaining full compatibility with Z8000 family software and hardware, the Z80,000 CPU offers greater power and flexibility in both its architecture and interface capability. Operating systems and compilers are easily developed in the Z80,000 CPU's high-quality environment, and the hardware interface provides for connection to a wide variety of system configurations.

Addresses in the Z80,000 CPU are 32 bits. This allows direct addressing of 4G bytes in each of four address spaces: system-mode data, system-mode instruction, normal-mode data, and normal-mode instruction. The CPU supports three modes of address representation. The 16-bit compact addresses are compatible with Z8000 nonsegmented mode. The 32-bit segmented addresses include both 16-bit offset, which is compatible with Z8000 segmented mode, and 24-bit offset. In addition a full 32-bit linear address space is provided.

The CPU features a general-purpose register file with sixteen 32-bit registers and nine operand addressing modes. The various addressing modes allow encoding choices for compact representation or for full 32-bit addressing. The instruction set can operate on bit, bit field, logical value, signed integer, unsigned integer, address, string, stack, and packed decimal byte data types. Logical and arithmetic instructions operate on bytes (8 bits), words (16 bits) and longwords (32 bits). The Extended Processing Architecture (EPA) supports floating-point operations. In addition, the instruction set is highly regular in combining operations, data types, and addressing modes. High-level language compilation is supported with instructions for procedure linkage, array index calculation, and bounds checking. Other instructions provide operating system functions such as system call and control of memory management.

There are two main operating modes, system and normal, supported by separate stacks. User programs operate in normal mode, while sensitive operating

system functions are performed in system mode. This protects critical parts of the operating system from user access. In addition, some instructions are privileged, and execute only in system mode. Memory management functions protect both system memory from user programs, and user memory from other users. Vectored, nonvectored, and nonmaskable interrupts support real-time operating systems.

Memory management is fully integrated with the CPU; no external support circuitry is necessary. A paging address translation mechanism is implemented Registers in the CPU point to address translation tables located in memory; the most recently used table entries are kept in a Translation Lookaside Buffer (TLB) in the CPU. The CPU performs logical to physical address translation and access protection for each memory reference. When a logical memory reference causes a translation or protection violation, the state of the CPU is automatically restored to restart the instruction. I/O ports can be referenced either by dedicated instructions or by the memory management mechanism mapping logical memory addresses to I/O port addresses.

Extensive trapping facilities, such as integer overflow, subrange out of bounds, and subscript out of bounds, catch common run-time errors. Software debuggers can use trace and breakpoint traps. Privileged instruction traps and memory protection violation traps secure the operating system from user programming errors or mischief. The overflow stack allows recovery from otherwise fatal errors.

The CPU has full 32-bit internal address and data paths. Externally, 32 pins time-multiplex the address and data. The interface is compatible with the complete line of Z-BUS peripherals. The hardware interface features 16-bit or 32-bit memory data path and programmable wait states. Burst transfers and an on-chip cache for instructions and data help develop high-performance systems. The interface supports multiprocessing configurations with interlocked memory references and two types of bus request protocols. The system designer can tailor the Z80,000-based system to cost and performance needs.

In summary, the Z80,000 CPU meets and surpasses the requirements of medium and high-end microprocessor systems for the 1980s. Software program development is easily accomplished with the CPU's sophisticated architecture. The highly pipelined design, on-chip cache, and external interface support systems ranging from dedicated controllers to mainframe computers. While Zilog continues to develop support for the Z80,000 CPU, Z8000 peripherals and development software are fully compatible with this latest in Zilog's line of high-performance microprocessors.

## REGISTERS

The Z80,000 CPU is a register-oriented processor offering sixteen 32-bit general-purpose registers, a 32-bit Program Counter (PC), a 16-bit Flag and Control Word (FCW), and nine other special-purpose registers.

The general-purpose register file (Figure 1) contains 64 bytes of storage. The first 16 bytes (RL0,RH0,...,RL7,RH7) can be used as accumulators for byte data. The first 16 words (R0,R1,...,R15) can be used as accumulators for word data, as index registers (except R0), or for memory addresses in compact mode (except R0). Any longword register (RR0,RR2,...,RR30) can be used as an accumulator for longword data, an index register in linear or segmented mode (except RR0), or for memory addresses in linear or segmented mode (except RR0). Quadword registers (RQ0,RQ4,...,RQ28) can be used as accumulators for Multiply, Divide, and Extend Sign instructions. This unique register organization allows bytes and words of data to be manipulated conveniently while leaving most of the register file free to hold addresses, counters, and any other data.

**Two registers are dedicated to the Stack Pointer (SP) and Frame Pointer (FP) used by Call, Enter, Exit, and Return** instructions. In compact mode, R15 is the Stack Pointer and R14 the Frame Pointer. In linear or segmented mode, RR14 is the Stack Pointer and RR12 is the Frame Pointer



**Figure 1. General-Purpose Register File**

The PC and FCW form the Program Status (Figure 2), which is automatically saved for traps and interrupts. The bits in FCW indicate operating modes, masks for traps and interrupts, and flags set according to the result of instructions. The remaining special registers are used for memory management, system configuration, and other CPU control (Figure 3)
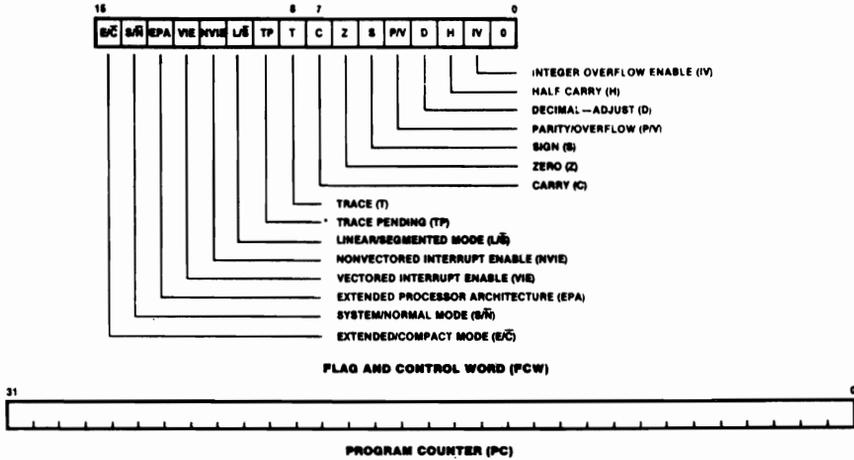


**Figure 2. Program Status Registers**

## ADDRESS SPACES

As shown in Figure 4, the CPU has three modes of address representation: compact, segmented, and linear The mode is selected by two control bits in the Flag and Control Word register (Table 1). The Extended/Compact (E/C̄) bit selects whether compact addresses (16 bits) or extended addresses (32 bits) are used. For extended addresses the Linear/Segmented (L/S̄) bit selects whether linear or segmented addresses are used.

The Load Address instruction can be used to manipulate addresses in any mode of representation.

In compact mode, addresses are 16 bits. Address calculations using compact addresses involve all 16 bits. Compact mode is more efficient and less program-consuming for applications requiring less than 64K bytes of program and less than 64K bytes of data. This efficiency is due to shorter instructions in compact mode, and the fact that addresses in the register file use word rather than longword registers. Applications requiring more than 64K bytes of either program or data should use segmented or linear modes.

**Table 1. Address Representation**

| Control Bits in FCW | | Representation |
|---|---|---|
| E/C̄ | L/S̄ | |
| 0 | 0 | Compact |
| 0 | 1 | Reserved |
| 1 | 0 | Segmented |
| 1 | 1 | Linear |

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PROGRAM STATUS AREA POINTER (PSAP)

NORMAL STACK POINTER (NSP)

TRANSLATION TABLE DESCRIPTOR REGISTERS

OVERFLOW STACK POINTER (OSP)

HARDWARE INTERFACE CONTROL REGISTER (HICR)
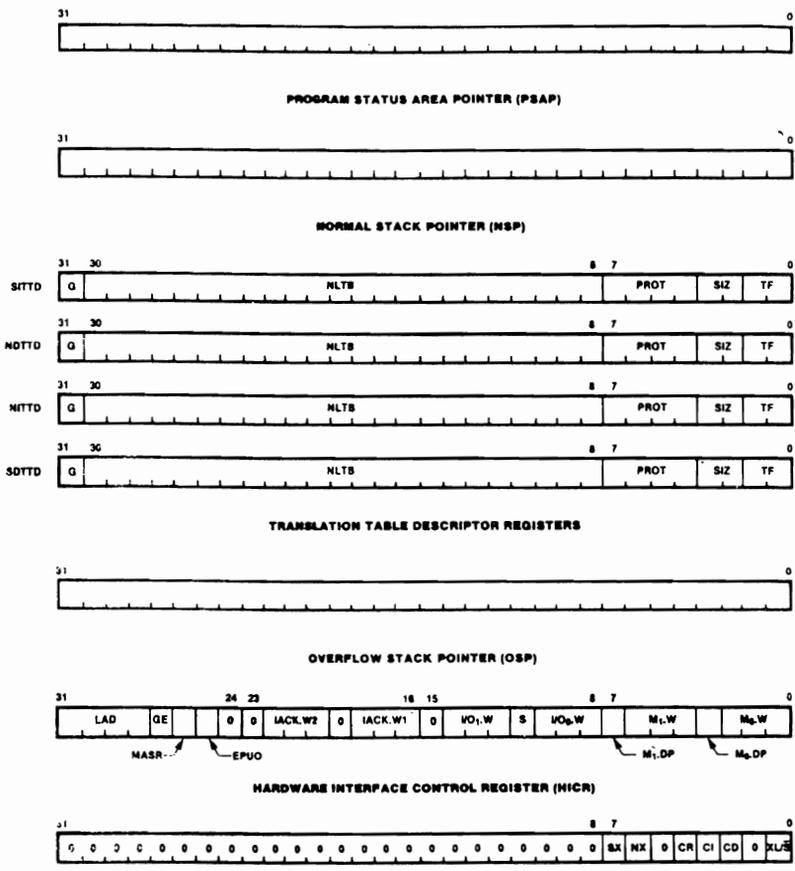
SYSTEM CONFIGURATION CONTROL LONGWORD (SCCL)

Figure 3. Special-Purpose Control Registers

**(A) COMPACT ADDRESS**

**(I) 64K BYTE SEGMENT SIZE**

**(II) 16M BYTE SEGMENT SIZE**

**(B) SEGMENTED ADDRESSES**

**(C) LINEAR ADDRESSES**
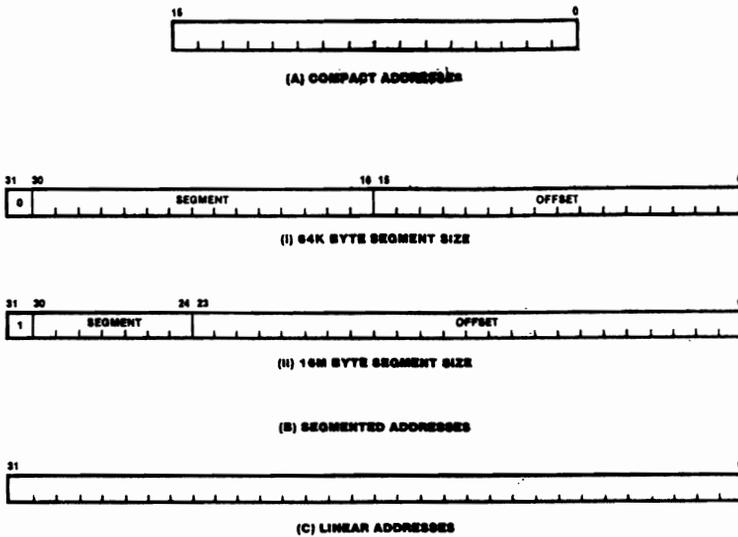
**Figure 4. Address Representations**

In segmented mode, addresses are 32 bits. Segmented addresses are composed of either a 15-bit segment number and a 16-bit segment offset or a 7-bit segment number and a 24-bit segment offset. Bit 31 of the address selects either of the two types of segmented addresses. Address calculations using segmented addresses involve only the segment offset; the segment number is unaffected. In segmented mode, the address space allows up to 32,768 segments of 64K-byte maximum size and up to 128 segments of 16M-byte maximum size. Many applications benefit from the logical structure of segmentation by allocating individual objects, such as a program module, stack, or large data structure, to separate segments.

In linear mode, addresses are 32 bits. Address calculations using linear addresses involve all 32 bits. In linear mode, the address space of 4G bytes is uniform and unstructured. Many applications benefit from the flexibility of linear addressing by allocating objects at arbitrary positions in the address space.

Memory is byte addressable by the CPU. The address used for multiple-byte data is the address of the most-significant byte. Multiple-byte data can be located at any byte address with no alignment restrictions.

I/O ports can be addressed by either dedicated instructions or by the memory management mechanism mapping logical memory addresses to I/O ports. I/O ports can be byte, word, or longword in size.

## NORMAL AND SYSTEM MODES

The CPU has two modes of operation, normal and system, selected by the S/N̄ bit in the Flag and Control Word register. These modes impact on CPU operation in three areas: privileged instructions, stack pointers, and memory management.

Since the most sensitive portions of the operating system usually execute in system mode, separate stack pointers are used to isolate the two operating modes.

Some instructions, such as those performing I/O operations or accessing control registers, can only be executed in system mode; in addition, the memory management mechanism allows access to some memory locations in system mode only. Programs executing in normal mode can request services from the operating system using the System Call instruction and trap.

# THEORY OF OPERATION

Figure 5 shows a block diagram of the Z80,000 CPU's internal organization, including the following major functional units and data paths:

- The external interface logic controls transactions on the bus. Addresses and data from the internal memory bus are transmitted through the interface to the Z-BUS. The Z-BUS is a time-multiplexed, address/data bus that connects the components of a microprocessor system.

- The cache stores copies of instruction and data memory locations. Instructions are read from the cache on the instruction bus. Data is read from or written to the cache on the memory bus. The cache also includes a copy of the physical Program Counter, so that the logical addresses of instructions are translated only for branches and when incrementing the Program Counter across a page boundary.

- The Translation Lookaside Buffer (TLB) translates logical addresses calculated by the address arithmetic unit to physical addresses used to access the cache.

- The address arithmetic unit performs all address calculations. This unit has a path to the register file for reading base and index registers and another path to the instruction bus for reading displacements and direct addresses. The result of the address calculation is transmitted to the TLB.

- The register file contains the sixteen general-purpose longword registers, Program Status registers, special-purpose control registers, and several registers used to store values temporarily during instruction execution. The register file has one path to the address arithmetic unit and two paths to the execution arithmetic and logic unit.

- The execution arithmetic and logic unit calculates the results of instruction execution, such as add, exclusive-OR, and simple load. This unit has two paths to the register file on which two operands can be read simultaneously or one can be written. One of the paths to the register file is multiplexed with a path from the memory bus.

- The instruction decoding and control unit decodes instructions and controls the operation of the other functional units. This unit has a path from the instruction bus and two programmable logic arrays for separate microcoded control of the two arithmetic units. This unit also controls exception handling and TLB loading.

All of the functional units and data paths listed above are 32 bits wide.

The operation of the CPU is highly pipelined so that several instructions are simultaneously in different stages of execution. Thus, the functional units effectively operate in parallel with one instruction being fetched while an address is calculated for another instruction and results are stored for a third instruction

Figure 6 shows the six-stage, synchronous pipeline. Instructions flow through each stage of the pipeline in sequence. The various pipeline stages can be working simultaneously on separate instructions or on separate portions of a single complex instruction. Each pipeline stage operates in one processor cycle, which is composed of two clock cycles, called $\phi$1 and $\phi$2. Thus, a processor cycle is 200 ns with a 10 MHz clock or 80 ns with a 25 MHz clock.

The instruction-fetch stage increments the Program Counter and initiates instructions fetched from the cache. The instruction-decoding stage receives and decodes instructions to set up control of the address-calculation stage.

The address-calculation stage can generally calculate a memory address in one processor cycle, except for Base Index, Relative, and Relative Index addressing modes, which require multiple cycles. After the logical effective address has been calculated, the corresponding physical address is provided by the TLB. The operand-fetch stage fetches the data from the cache and latches it into a holding register.

The execution stage performs data manipulations. Byte, word, and longword results are generally calculated in one processor cycle, but certain instructions, such as multiply and block-move operations, require multiple cycles. During the execution stage, results are stored to registers. Results are stored to the cache and external memory during the operand-store stage. The flags are also set during the operand-store stage.

The cache can handle two references during a processor cycle. Instruction fetches use the $\phi$2 clock cycle for tag comparison and $\phi$1 for data access. Either an operand fetch or store can use $\phi$1 for tag comparison and $\phi$2 for data access

The pipeline allows single instructions, like register-to-register load and memory-to-register add, to execute at a rate of one per processor cycle. Thus, the peak performance of the CPU is 12.5 million instructions per second (MIPS) with a 25 MHz clock. In practice, the actual performance is reduced to approximately one-third of the peak because of delays due to the execution of multiple-cycle instructions, interference between instructions in the pipeline, and main memory accesses for cache and TLB misses
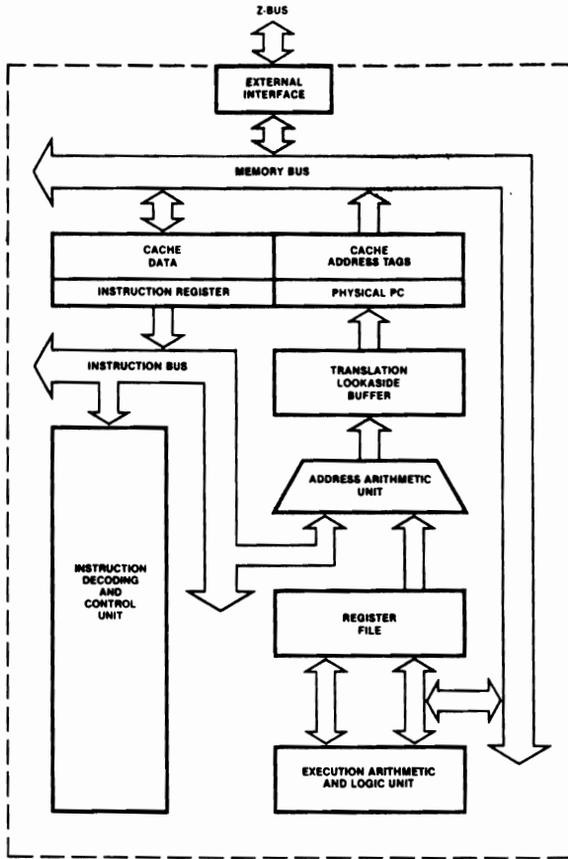
**Figure 5. Z80,000 CPU Functional Block Diagram**
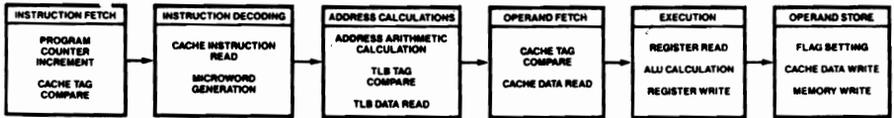


**Figure 6. Instruction Pipeline**

582

# 2114
# 1024 X 4 BIT STATIC RAM

|  | 2114-2 | 2114-3 | 2114 | 2114L2 | 2114L3 | 2114L |
|---|---|---|---|---|---|---|
| Max. Access Time (ns) | 200 | 300 | 450 | 200 | 300 | 450 |
| Max. Power Dissipation (mw) | 525 | 525 | 525 | 370 | 370 | 370 |

- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**

- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Pin-Out Compatible with 3605 and 3625 Bipolar PROMs**

The Intel® 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The 2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The 2114 is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

The 2114 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

**PIN CONFIGURATION**   **LOGIC SYMBOL**   **BLOCK DIAGRAM**
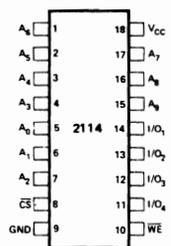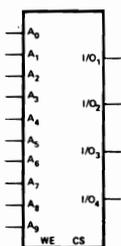


**PIN NAMES**

| $A_0$–$A_9$ | ADDRESS INPUTS | $V_{CC}$ | POWER (+5V) |
|---|---|---|---|
| $\overline{WE}$ | WRITE ENABLE | GND | GROUND |
| $\overline{CS}$ | CHIP SELECT |  |  |
| $I/O_1$–$I/O_4$ | DATA INPUT/OUTPUT |  |  |

583
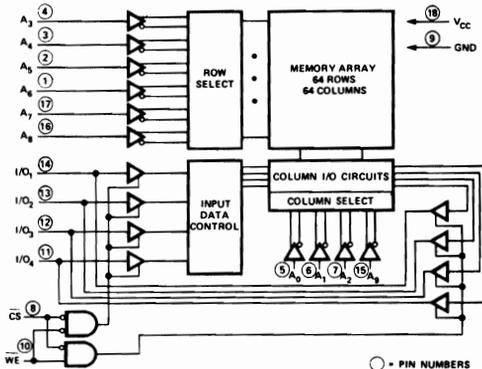
# 2048-word×8-bit High Speed Static CMOS RAM

## ■FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time    120ns/150ns/200ns (max.)
- Low Power Standby and    Standby:    100μW (typ.)
  Low Power Operation    Operation:    180mW (typ.)
- Completely Static RAM:    No clock or Timing Strobe Required
- Directly TTL Compatible:    All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

## ■FUNCTIONAL BLOCK DIAGRAM





HM6116-2, HM6116-3, HM6116-4

(DG-24)

HM6116P-2, HM6116P-3, HM6116P-4

(DP-24)

## ■PIN ARRANGEMENT



( Top View )
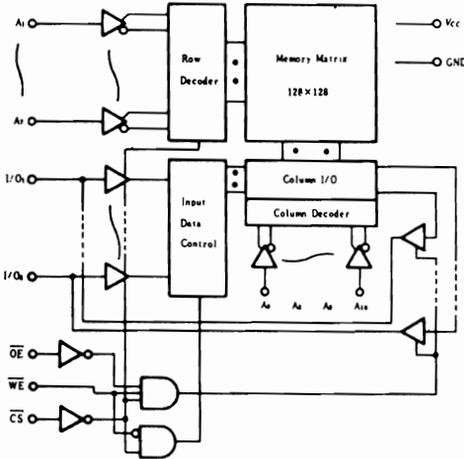
## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to GND | $V_T$ | −0.5* to +7.0 | V |
| Operating Temperature | $T_{opr}$ | 0 to +70 | ℃ |
| Storage Temperature (Plastic) | $T_{stg}$ | −55 to +125 | ℃ |
| Storage Temperature (Ceramic) | $T_{stg}$ | −65 to +150 | ℃ |
| Temperature Under Bias | $T_{bias}$ | −10 to +85 | ℃ |
| Power Dissipation | $P_T$ | 1.0 | W |

* Pulse Width 50ns : −1.5 V

## ■TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | $V_{cc}$ Current | I/O Pin | Ref. Cycle |
|---|---|---|---|---|---|---|
| H | × | × | Not Selected | $I_{SB}$, $I_{SB1}$ | High Z | |
| L | L | H | Read | $I_{CC}$ | Dout | Read Cycle (1)~(3) |
| L | H | L | Write | $I_{CC}$ | Din | Write Cycle (1) |
| L | L | L | Write | $I_{CC}$ | Din | Write Cycle (2) |

584
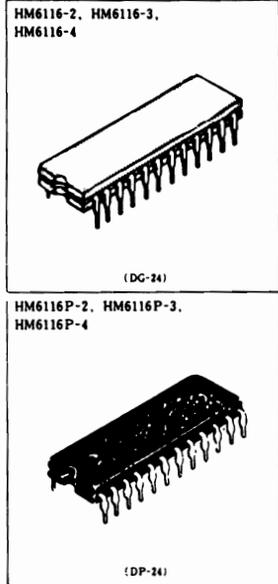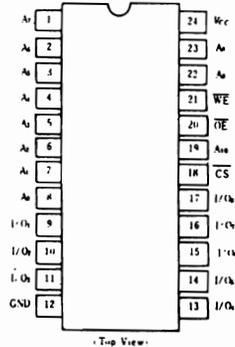
# MCM65116

## Advance Information

### 16K BIT STATIC RANDOM ACCESS MEMORY

The MCM65116 is a 16,384-bit Static Random Access Memory organized as 2048 words by 8-bits, fabricated using Motorola's High-performance silicon-gate CMOS (HCMOS) technology It uses a design approach which provides the simple timing features associated with fully static memories, and the reduced power associated with CMOS memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access time.

Chip Enable (E) controls the power-down feature It is not a clock but rather a chip control that affects power consumption In less than a cycle time after chip enable (E) goes high, the part automatically reduces its power requirements and remains in this low-power standby as long as the chip enable (E) remains high. The automatic power-down feature causes no performance degradation

The MCM65116 is in a 24-pin dual-in-line package with the industry standard JEDEC approved pinout and is pinout compatible with the industry standard 16K EPROM/ROM

- Single + 5 V Supply
- 2048 Words by 8-Bit Organization
- HCMOS Technology
- Fully Static. No Clock or Timing Strobe Required
- Maximum Access Time: MCM65116-12 — 120 ns
  MCM65116-15 — 150 ns
  MCM65116-20 — 200 ns
- Power Dissipation: 55 mA Maximum (Active)
  10 mA Maximum (Standby-TTL Levels)
  2 mA Maximum (Standby)
  100 μA Maximum (Standby-MCM65LT16)
- Low Voltage Data Retention (MCM65L116 only) 100 μW Maximum
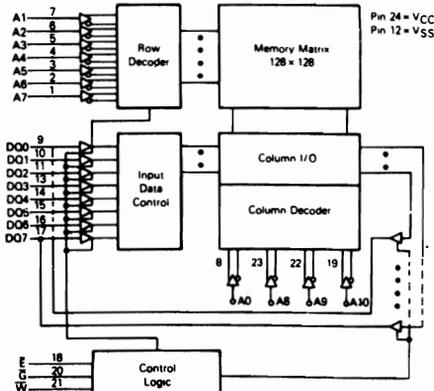
## HCMOS
(COMPLEMENTARY MOS)

### 2,048 × 8 BIT STATIC RANDOM ACCESS MEMORY

P SUFFIX
PLASTIC PACKAGE
CASE 709

C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 623

### PIN ASSIGNMENTS

| | | | |
|---|---|---|---|
| A7 | 1 | 24 | VCC |
| A6 | 2 | 23 | A8 |
| A5 | 3 | 22 | A9 |
| A4 | 4 | 21 | W |
| A3 | 5 | 20 | G |
| A2 | 6 | 19 | A10 |
| A1 | 7 | 18 | E |
| A0 | 8 | 17 | DQ7 |
| DQ0 | 9 | 16 | DQ6 |
| DQ1 | 10 | 15 | DQ5 |
| DQ2 | 11 | 14 | DQ4 |
| VSS | 12 | 13 | DQ3 |
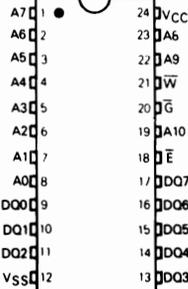
### PIN NAMES

| | |
|---|---|
| A0-A10 | Address Input |
| DQ0-DQ7 | Data Input/Output |
| W | Write Enable |
| G | Output Enable |
| E | Chip Enable |
| VCC | Power ( + 5 V) |
| VSS | Ground |

## BLOCK DIAGRAM

Pin 24 = VCC
Pin 12 = VSS

ADI-911/5-82

# HM6264P-10, HM6264P-12, HM6264P-15

### 8192-word x 8-bit High Speed Static CMOS RAM

**FEATURES**

- Fast access Time                 100ns/120ns/150ns (max.)
- Low Power Standby             Standby:      0.1mW (typ.)
  Low Power Operation        Operating:   200mW (typ.)
- Single +5V Supply
- Completely Static Memory . . . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible:  All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

(DP-28)

**BLOCK DIAGRAM**



**PIN ARRANGEMENT**



(Top View)
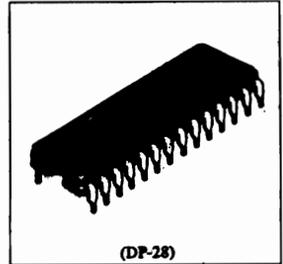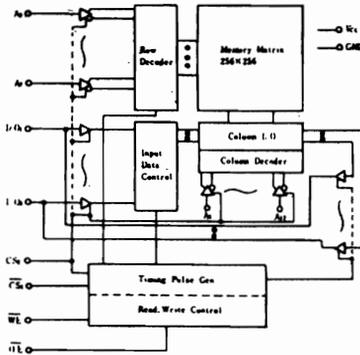
**ABSOLUTE MAXIMUM RATINGS**

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Terminal Voltage * | $V_T$ | −0.5 ** to +7.0 | V |
| Power Dissipation | $P_T$ | 1.0 | W |
| Operating Temperature | $T_{opr}$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +125 | °C |
| Storage Temperature (Under Bias) | $T_{bias}$ | −10 to +85 | °C |

* With respect to GND.    ** Pulse width 50ns: −3.0V
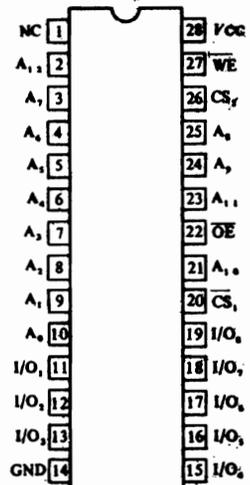
**TRUTH TABLE**

| $\overline{WE}$ | $\overline{CS_1}$ | $CS_2$ | $\overline{OE}$ | Mode | I/O Pin | $V_{CC}$ Current | Note |
|---|---|---|---|---|---|---|---|
| X | H | X | X | Not Selected | High Z | $I_{SB}, I_{SB1}$ | |
| X | X | L | X | (Power Down) | High Z | $I_{SB}, I_{SB2}$ | |
| H | L | H | H | Output Disabled | High Z | $I_{CC}, I_{CC1}$ | |
| H | L | H | L | Read | Dout | $I_{CC}, I_{CC1}$ | |
| L | L | H | H | Write | Din | $I_{CC}, I_{CC1}$ | Write Cycle (1) |
| L | L | H | L | Write | Din | $I_{CC}, I_{CC1}$ | Write Cycle (2) |

x : Don't care.

586

# MCM63256

## Product Preview

### 256K BIT READ ONLY MEMORY

The MCM63256 is a MOS mask programmable byte-organized Read Only Memory (ROM). The MCM63256 is organized as 32,768 bytes of 8 bits and is fabricated using Motorola's high performance N-channel silicon gate technology (HMOS). This device is designed to provide maximum circuit density and reliability with highest possible performance while maintaining low power dissipation and wide operating margins and remaining fully compatible with TTL inputs and outputs.

The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Single ± 10% + 5 Volt Power Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Automatic Power Down
- Power Dissipation
  100 mA Active (Maximum) (Unloaded)
  15 mA Standby (Maximum)
- Current Surge Suppression When Powering Up Device
- Program Layer Late in Process for Quick Turnaround Time
- 150 ns Maximum Access from Address and Chip Enable
- 28-Pin JEDEC Standard Package and Pinout

**ADDITIONAL FEATURE**

- Address (A14) is User Selectable for Either Pin 27 or Pin 1



**P SUFFIX**
PLASTIC PACKAGE
CASE 710

### BLOCK DIAGRAM



VCC = Pin 28
VSS = Pin 14

*Active level defined by the user.

### PIN ASSIGNMENT



| PIN NAMES | |
|---|---|
| A0-A14 | Address |
| E | Chip Enable |
| G | Output Enable |
| Q0-Q7 | Data Output |
| VCC | + 5 V Power Supply |
| VSS | Ground |

NP-350/5-82
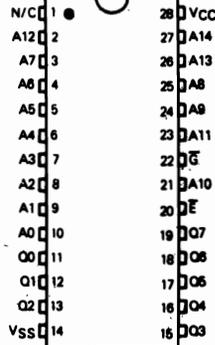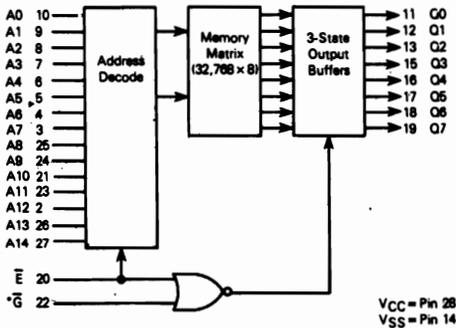
## 256K-BIT (32,768 x 8) CMOS STATIC RANDOM ACCESS MEMORY WITH DATA RETENTION AND LOW POWER

The Fujitsu MB 84256 is a 32,768-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronouse circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volts power supply is required.

The MB 84256 is ideally suited for use in microprocesser systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

- Organization:    32,768 x 8 bits
- Fast access time: 100 ns max. (MB 84256-10/10L/10LL)
  120 ns max. (MB 84256-12/12L/12LL)
  150 ns max. (MB 84256-15/15L/15LL)
- Completely static operation:  No clock required
- TTL compatible inputs/outputs
- Three-state outputs
- Single +5V power supply, ±10% tolerance
- Low power standby:
  CMOS level:   5.5   mW max.  (MB 84256-10/12/15)
  0.55 mW max.  (MB 84256-10L/10LL/12L/12LL/
  15L/15LL)
  TTL level:    16.5 mW max.  (MB 84256-10/10L/10LL/12/12L/12LL/
  15/15L/15LL)
- Data retention:  2.0V
- Standard 28-pin DIP (600 mil) (Suffix: -P)
- Standard 28-pin Bend-type Plastic Flat Package (450 mil) (Suffix: -PF)
- Standard 32-pad LCC (Suffix: -CV)

### ABSOLUTE MAXIMUM RATINGS (see NOTE)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | −0.5 to +7.0 | V |
| Input Voltage | | $V_{IN}$ | −0.5 to $V_{CC}$+0.5 | V |
| Output Voltage | | $V_{OUT}$ | −0.5 to $V_{CC}$+0.5 | V |
| Temperature Under Bias | | $T_{BIAS}$ | −10 to +85 | °C |
| Storage Temperature Range | CERAMIC | $T_{STG}$ | −65 to +150 | °C |
| | PLASTIC | | −40 to +125 | |



PLASTIC PACKAGE DIP-28P-M02    PLASTIC PACKAGE FPT-28P-M02

CERAMIC PACKAGE LCC-32C-A02

### PIN ASSIGNMENT
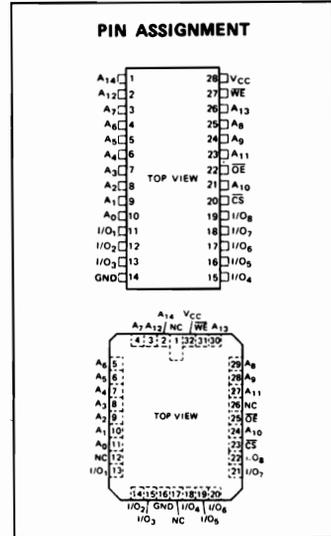
Toshiba is the world leader in CMOS and NMOS Static RAMs and was one of the first suppliers of the 256K CMOS SRAM.

| 32,768 WORDS × 8 BIT CMOS STATIC RAM SILICON GATE CMOS | TC55257APL-85/AFL-85/APL-85L/AFL-85L TC55257APL-10/AFL-10/APL-10L/AFL-10L TC55257APL-12/AFL-12/APL-12L/AFL-12L |
|---|---|

The TC55257APL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.) and minimum cycle time of 85ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is typical 2μA. The TC55257APL has two control inputs: Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257APL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

- Low Power Dissipation
  27.5 mW/MHz (Max.) Operating
- Standby Current
  100μA(Max.): TC55257APL-85/AFL-85
  APL-10/AFL-10
  APL-12/AFL-12
  2μA(Max.): TC55257APL-85L/AFL-85L
  ($T_a$ = 25°C)　APL-10L/AFL-10L
  APL-12L/AFL-12L
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$

- Data Retention Supply Voltage: 2.0~5.5V
- Access Time

| | TC55257APL-85 /AFL-85/APL-85L /AFL-85L | TC55257APL-10 /AFL-10/APL-10L /AFL-10L | TC55257APL-12 /AFL-12/APL-12L /AFL-12L |
|---|---|---|---|
| Access Time (MAX.) | 85ns | 100ns | 120ns |
| $\overline{CE}$ Access Time (MAX.) | 85ns | 100ns | 120ns |
| Output Enable Time (MAX.) | 45ns | 50ns | 60ns |

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic FP Package

## PIN CONNECTION    (TOP VIEW)

| | | | |
|---|---|---|---|
| A14 | 1 | 28 | $V_{DD}$ |
| A12 | 2 | 27 | R/W |
| A7 | 3 | 26 | A13 |
| A6 | 4 | 25 | A8 |
| A5 | 5 | 24 | A9 |
| A4 | 6 | 23 | A11 |
| A3 | 7 | 22 | $\overline{OE}$ |
| A2 | 8 | 21 | A10 |
| A1 | 9 | 20 | $\overline{CE}$ |
| A0 | 10 | 19 | I/O8 |
| I/O1 | 11 | 18 | I/O7 |
| I/O2 | 12 | 17 | I/O6 |
| I/O3 | 13 | 16 | I/O5 |
| GND | 14 | 15 | I/O4 |

## PIN NAMES

| $A_0 \sim A_{14}$ | Address Inputs |
|---|---|
| R/W | Read/Write Control Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{CE}$ | Chip Enable Input |
| $I/O_1 \sim I/O_8$ | Data Input/Output |
| $V_{DD}$ | Power ( + 5V) |
| GND | Ground |

## BLOCK DIAGRAM
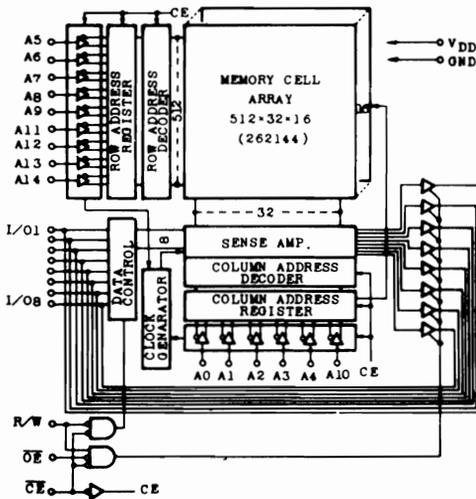
# MN4164, N MOS 65K Bit Dynamic Ram

## Description

System oriented features include: operation from a single +5V ±10% tolerance power supply, direct TTL interfacing capability, on-chip addresses and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system.

The RAM module also incorporates several flexible operating modes: "Read," "Write," "Read-Modify-Write" cycles, "Page-Mode" operation and "RAS-Only" refresh. Proper control of the clock inputs (RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (for operating in page mode).

## Features

- 65,536 x 1 RAM, 16-pin package
- Row access time:
  - 150 ns Max. (MN4164-15/MN4164P-15)
  - 200 ns Max. (MN4164-20/MN4164P-20)
  - 250 ns Max. (MN4164-25/MN4164P-25)
- Cycle time:
  - 270 ns Max. (MN4164-15/MN4164P-15)
  - 330 ns Max. (MN4164-20/MN4164P-20)
  - 410 ns Max. (MN4164-25/MN4164P-25)
- Low power dissipation:
  - 275 mW Max. (active)
  - 27.5 mW Max. (standby)
- Single 5V supply, ±10% tolerance
- 128 refresh cycles/2ms

## MN4164 Block Diagram



MN4164-15
MN4164-20
MN4164-25
Unit: mm (inch)
(16 PIN CERAMIC DIL)

MN4164P-15
MN4164P-20
MN4164P-25
Unit: mm
(16 PIN PLASTIC DIL)
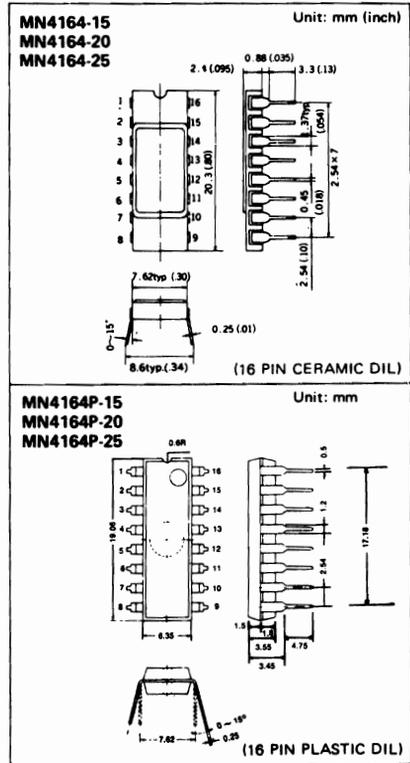
## Pin Assignment (Top View)
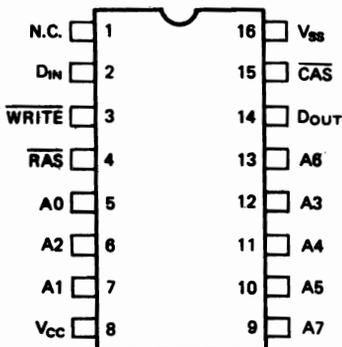


| Pin | | Pin | |
|---|---|---|---|
| N.C. | 1 | 16 | V$_{SS}$ |
| D$_{IN}$ | 2 | 15 | CAS |
| WRITE | 3 | 14 | D$_{OUT}$ |
| RAS | 4 | 13 | A6 |
| A0 | 5 | 12 | A3 |
| A2 | 6 | 11 | A4 |
| A1 | 7 | 10 | A5 |
| V$_{CC}$ | 8 | 9 | A7 |

| Pin Names | Function |
|---|---|
| A$_0$ ~ A$_7$ | Address Inputs |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| WRITE | Write Enable |
| D$_{IN}$ | Data Input |
| D$_{OUT}$ | Data Output |
| V$_{CC}$ | Power (+5V) |
| V$_{SS}$ | Ground (0V) |

# MN4164, N MOS 65K Bit Dynamic Ram
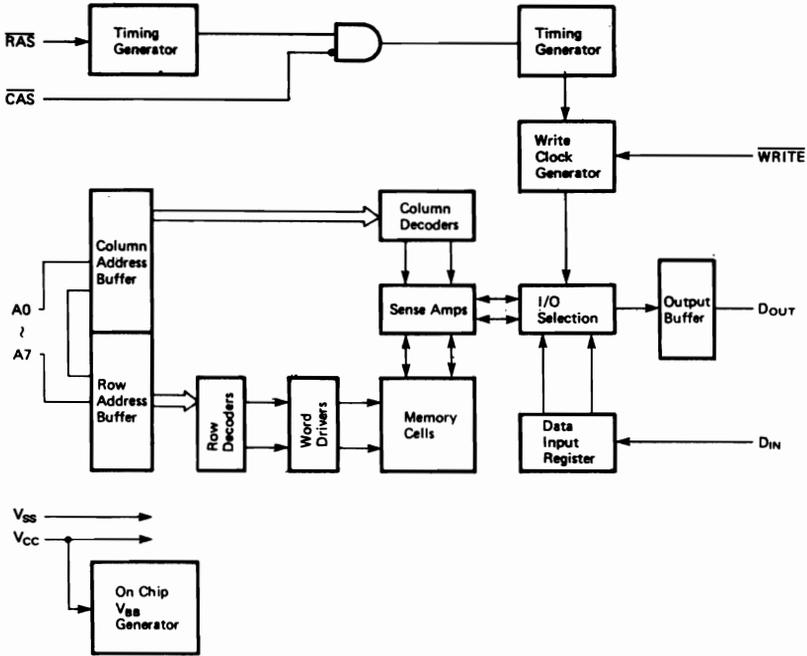


## Absolute Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any Pin relative tb $V_{SS}$ | $V_{IN}, V_{OUT}$ | −1.0 to +7.0 | V |
| Voltage on $V_{CC}$ Supply relative to $V_{SS}$ | $V_{CC}$ | −1.0 to +7.0 | V |
| Operating Temperature | $T_{OP}$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +150 | °C |
| Power Dissipation | $P_D$ | 1 | W |
| Short Ci.cuit Current | $I_{OS}$ | 50 | mA |

Note: Exceeding Absolute Maximum Ratings may cause permanent device damage. Functional operating of the device is not implied outside the operating conditions. Exposure to absolute maximum ratings for extended periods of time may impact device reliability.

## Recommended Operating Conditions (Referenced to $V_{SS}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Temperature |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 0°C to +70°C |
| | $V_{SS}$ | 0 | 0 | 0 | V | |
| Input High Voltage, all inputs | $V_{IH}$ | 2.2 | — | $V_{CC}$ +1.0V | V | |
| Input Low Voltage, all inputs | $V_{IL}$ | −1.0 | — | 0.8 | V | |

## Capacitance (Ta = 25°C, f = 1 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | — | — | 10 | pF |
| Output Capacitance | $C_{OUT}$ | — | — | 12 | pF |

## Description

The M41256xxM15B integrated circuit is a high-speed, low-power 262,144 words by 1-bit dynamic random access memory (DRAM) device. The device is manufactured according to the general requirements of MIL-STD-883, is screened according to Method 5004 for a class B device, and meets the qualification and quality conformance requirements of Method 5005.

## Features

- Military temperature range, Tc = −55°C to +110°C
- Complies with MIL-STD-883
- 262,144 words × 1-bit organization
- 150 ns access time from $\overline{RE}$
- 75 ns access time from CE
- 360/330 mW active power, Page Mode at minimum cycle time
- 55 mW standby power
- Multiplexed address inputs
- ±10% power supply tolerance
- Read-Modify-Write capabilities
- $\overline{RE}$ Only refresh/Hidden Refresh
- Latched or high-impedance output during refresh
- 256 refresh cycles
- Page Mode operation
- Available in a hermetic ceramic DIP

Figure 1. Page Mode Block Diagram
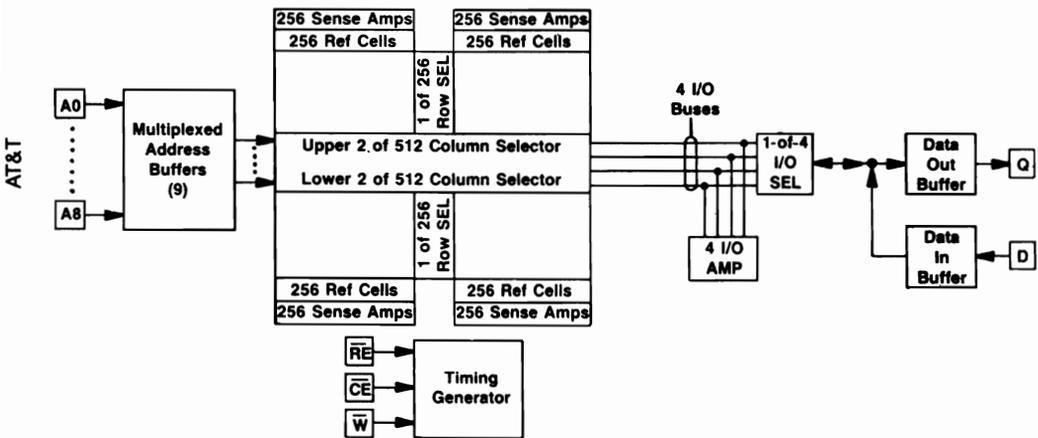


## Pin Descriptions

Figure 2. Pin Function Diagram
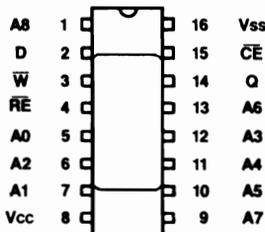


Pin Description Key

| Symbol | Name |
|--------|------|
| Vcc | +5 V Supply |
| D | Data In |
| Q | Data Out |
| A(0-8) | Address Input(0-8) |
| $\overline{W}$ | Write Enable |
| $\overline{RE}$ | Row Enable |
| $\overline{CE}$ | Column Enable |
| Vss | Ground |
| NC | No Connect |

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# MCM6256

## Product Preview

### 256K-BIT DYNAMIC RAM

The MCM6256 is a 262,144 bit, high-speed, dynamic Random Access Memory. Organized as 262,144 one-bit words and fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. The MCM6256 has the capability of using laser fuse redundancy and is manufactured using advanced direct-step on wafer photolithographic equipment.

By multiplexing row and column address inputs, the MCM6256 requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6256 incorporates a one transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of the MCM6256 is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. Nibble mode address is controlled by the addresses on pin 1 (A8 row and A8 column).

- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (± 10%)
- Maximum Access Time:
  MCM6256-10 = 100 ns
  MCM6256-12 = 120 ns
  MCM6256-15 = 150 ns
- Low Power Dissipation:
  70 mA maximum (Active) MCM6256-10
  4 mA maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- Automatic ($\overline{CAS}$ before $\overline{RAS}$) Refresh Mode
- Fast Nibble Mode on Read and Write Cycles
  20 ns Access Time
  40 ns Cycle Time



L SUFFIX
CERAMIC PACKAGE
CASE 690

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| A8 | 1 | 16 | $V_{SS}$ |
| D | 2 | 15 | $\overline{CAS}$ |
| $\overline{W}$ | 3 | 14 | Q |
| $\overline{RAS}$ | 4 | 13 | A6 |
| A0 | 5 | 12 | A3 |
| A2 | 6 | 11 | A4 |
| A1 | 7 | 10 | A5 |
| $V_{CC}$ | 8 | 9 | A7 |
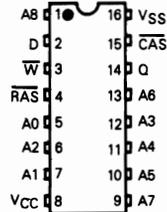
### PIN NAMES

| | |
|---|---|
| A0-A8 | Address Input |
| D | Data In |
| Q | Data Out |
| $\overline{W}$ | Read/Write Input |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $V_{CC}$ | Power (+5 V) |
| $V_{SS}$ | Ground |
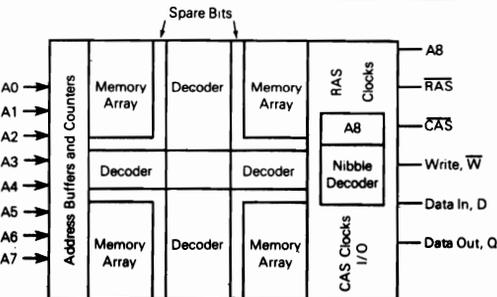
This document contains information on a product under development.

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**Toshiba was the first to introduce the 1MB DRAM and is now the world's leading supplier.** We offer fast page, nibble or static column operating modes in CMOS. Production quantities of these devices are available in DIP, SOJ and ZIP packages.

| 1,048,576 WORDS × 1 BIT DYNAMIC RAM | TC511000P/J/Z-85 |
| SILICON GATE CMOS | TC511000P/J/Z-10 |
| *This is advanced information and specifications are subject to change without notice. | TC511000P/J/Z-12 |

The TC511000P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000P/J/Z utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000P/J/Z to be packaged in a standard 18 pin plastic DIP, 20 pin plastic SOJ and 20 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

| | | TC511000P/J/Z-85 | TC511000P/J/Z-10 | TC511000P/J/Z-12 |
|---|---|---|---|---|
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 85ns | 100ns | 120ns |
| $t_{AA}$ | Column Address Access Time | 45ns | 50ns | 60ns |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 25ns | 25ns | 30ns |
| $t_{RC}$ | Cycle Time | 165ns | 190ns | 220ns |
| $t_{PC}$ | Fast Page Mode Cycle Time | 50ns | 55ns | 70ns |

- Single power supply of 5V ± 10% with a built-in $V_{BB}$ generator
- Low Power
  - 330mW MAX. Operating (TC511000P/J/Z-10)
  - 275mW MAX. Operating (TC511000P/J/Z-12)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Fast Page Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package  Plastic DIP: TC511000P
  - Plastic SOJ: TC511000J
  - Plastic ZIP: TC511000Z

## PIN CONNECTION (TOP VIEW)

- Plastic DIP
- Plastic SOJ
- Plastic ZIP
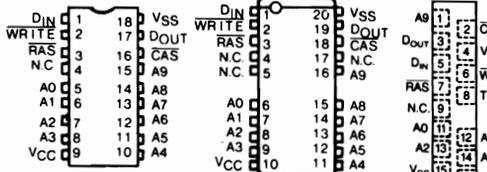


## PIN NAMES

| A0~A9 | Address Inputs |
|---|---|
| $\overline{RAS}$ | Row Address Strobe |
| $D_{IN}$ | Data In |
| $D_{OUT}$ | Data Out |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WRITE}$ | Read/Write Input |
| $V_{CC}$ | Power ( + 5V) |
| $V_{SS}$ | Ground |
| N.C. | No Connection |

## BLOCK DIAGRAM



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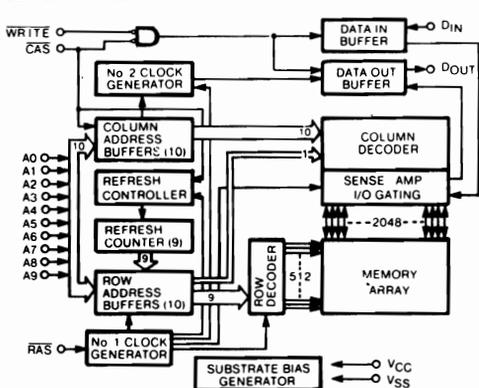
# 2316 STATIC READ ONLY MEMORY (2048x8)

## DESCRIPTION

The 2316 high performance read only memory is organized 2048 words by 8 bits with access times of less than 350 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations.

The 2316 operates totally asynchronously. No clock input is required. The three programmable chip select inputs allow eight 16K ROMS to be OR-tied without external decoding.

Designed to replace two 2708 8K EPROMS, the 2316 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

- 400mV Noise Immunity on Inputs
- 2048 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450 ns, 350 ns
- Totally Static Operation
- TTL Compatible

- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- Pin Compatible with 2716 EPROM
- Replacement for two 2708s
- 2708/2716 EPROMS Accepted as Program Data Inputs

## ORDERING INFORMATION

MXS 2316 _____

FREQUENCY RANGE
NO SUFFIX = 450ns
A = 350ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

## PIN CONFIGURATION

2316

| | | |
|---|---|---|
| $A_7$ | 1 | 24 $V_{CC}$ |
| $A_6$ | 2 | 23 $A_8$ |
| $A_5$ | 3 | 22 $A_9$ |
| $A_4$ | 4 | 21 $CS_3/\overline{CS}_3$ |
| $A_3$ | 5 | 20 $CS_1/\overline{CS}_1$ |
| $A_2$ | 6 | 19 $A_{10}$ |
| $A_1$ | 7 | 18 $CS_2/\overline{CS}_2$ |
| $A_0$ | 8 | 17 $O_8$ |
| $O_1$ | 9 | 16 $O_7$ |
| $O_2$ | 10 | 15 $O_6$ |
| $O_3$ | 11 | 14 $O_5$ |
| GND | 12 | 13 $O_4$ |
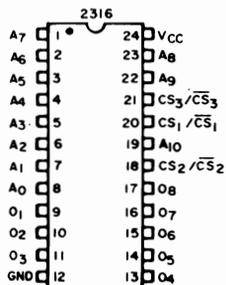
# 2332 STATIC READ ONLY MEMORY (4096x8)

## DESCRIPTION

The 2332 high performance read only memory is organized 4096 words by 8 bits with access times of less than 350 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels.

The 2332 operates totally asynchronously. No clock input is required. The two programmable chip select inputs allow four 32K ROMS to be OR-tied without external decoding.

Designed to replace two 2716 16K EPROMS, the 2332 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 2332    450 ns
                 2332A  350 ns
- Completely TTL Compatible
- Totally Static Operation

- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- Pin Compatible with 2716 & 2732 EPROM
- Replacement for Two 2716s
- 2708/2716 EPROMS Accepted as Program Data Inputs
- 400mV Noise Immunity on Inputs

## ORDERING INFORMATION

MXS 2332 ____

FREQUENCY RANGE
NO SUFFIX = 450ns
A = 350ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

## PIN CONFIGURATION

```
              2332
    A7  ⌷ 1 •     24 ⌷ VCC
    A6  ⌷ 2       23 ⌷ A8
    A5  ⌷ 3       22 ⌷ A9
    A4  ⌷ 4       21 ⌷ CS2/CS̄2
    A3  ⌷ 5       20 ⌷ CS1/CS̄1
    A2  ⌷ 6       19 ⌷ A10
    A1  ⌷ 7       18 ⌷ A11
    A0  ⌷ 8       17 ⌷ O8
    O1  ⌷ 9       16 ⌷ O7
    O2  ⌷ 10      15 ⌷ O6
    O3  ⌷ 11      14 ⌷ O5
   GND  ⌷ 12      13 ⌷ O4
```

596
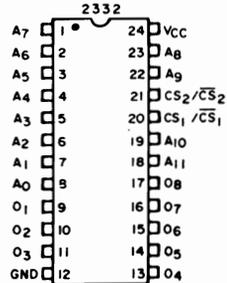
# 2364 STATIC READ ONLY MEMORY (8192x8)

## DESCRIPTION

The 2364 high performance read only memory is organized 8192 words by 8 bits with access times of less than 350 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels.

The 2364 operates totally asynchronously. No clock input is required. The programmable chip select input allows two 64K ROMS to be OR-tied without external decoding.

Designed to replace two 2732 32K EPROMS, the 2364 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450 ns, 350 ns
- Completely TTL Compatible
- Totally Static Operation
- Three-State Outputs for Wire-OR Expansion

- One Programmable Chip Select
- Pin Compatible with 2716 & 2732 EPROM
- Replacement for Two 2732s
- 2716/2732 EPROMS Accepted as Program Data Inputs
- 400mV Noise Immunity on Inputs

## ORDERING INFORMATION

MXS 2364

FREQUENCY RANGE
NO SUFFIX = 450ns
A = 350ns

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

## PIN CONFIGURATION

2364

| | | |
|---|---|---|
| $A_7$ | 1 | 24 $V_{CC}$ |
| $A_6$ | 2 | 23 $A_8$ |
| $A_5$ | 3 | 22 $A_9$ |
| $A_4$ | 4 | 21 $A_{12}$ |
| $A_3$ | 5 | 20 $CS_1 / \overline{CS}_1$ |
| $A_2$ | 6 | 19 $A_{10}$ |
| $A_1$ | 7 | 18 $A_{11}$ |
| $A_0$ | 8 | 17 $O_8$ |
| $O_1$ | 9 | 16 $O_7$ |
| $O_2$ | 10 | 15 $O_6$ |
| $O_3$ | 11 | 14 $O_5$ |
| GND | 12 | 13 $O_4$ |
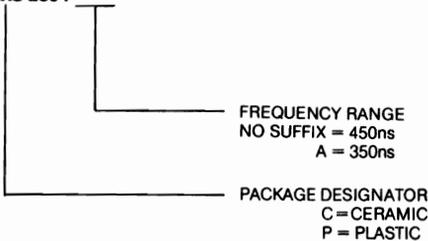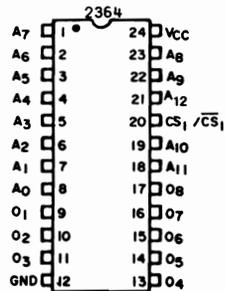
# MCM65256

## Product Preview

### 256K BIT READ ONLY MEMORY

The MCM65256 is a complementary MOS mask programmable byte-organized Read Only Memory (ROM). The MCM65256 is organized as 32,768 bytes of 8 bits and is fabricated using Motorola's high performance silicon gate CMOS technology (HCMOS). This device is designed to provide maximum circuit density and reliability with highest possible performance while maintaining low power dissipation and wide operating margins. The MCM65256 offers low-power operation from a single +5 Volt supply and is fully TTL compatible on all inputs and outputs.

The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Single ± 10% +5 Volt Power Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- 250 ns Maximum Access from Address and Chip Enable
- Automatic Power Down
- Active Current 50 mA Maximum (Unloaded at a 250 ns Cycle Time) — Decreases with Increasing Cycle Time
- D.C. Active Current 10 mA Maximum
- Standby Current 50 μA Maximum (Full Rail Inputs)
- Standby Current 3.0 mA Maximum (TTL Inputs)
- Mask Programmable Chip Enable and Output Enable
- Program Layer Late in Process for Quick Turnaround Time
- 28-Pin JEDEC Standard Package and Pinout
- Address (A14) is User Selectable for Either Pin 27 or Pin 1

### HCMOS
(COMPLEMENTARY MOS)

### 32,768 × 8 BIT
### READ ONLY MEMORY

P SUFFIX
PLASTIC PACKAGE
CASE 710

### PIN ASSIGNMENT
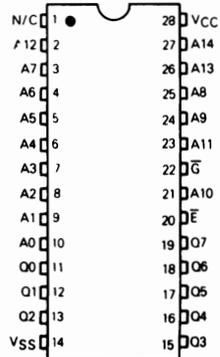
```
N/C  [ 1  ●      28 ]  VCC
A12  [ 2         27 ]  A14
A7   [ 3         26 ]  A13
A6   [ 4         25 ]  A8
A5   [ 5         24 ]  A9
A4   [ 6         23 ]  A11
A3   [ 7         22 ]  G̅
A2   [ 8         21 ]  A10
A1   [ 9         20 ]  E̅
A0   [ 10        19 ]  Q7
Q0   [ 11        18 ]  Q6
Q1   [ 12        17 ]  Q5
Q2   [ 13        16 ]  Q4
VSS  [ 14        15 ]  Q3
```

### PIN NAMES

| | |
|---|---|
| A0-A14 | Address |
| E̅ | Chip Enable |
| G̅ | Output Enable |
| Q0-Q7 | Data Output |
| VCC | +5 V Power Supply |
| VSS | Ground |

### BLOCK DIAGRAM

```
A0  10 ─┐
A1   9  │
A2   8  │    ┌─────────┐    ┌──────────┐   ┌──────────┐   ──11  Q0
A3   7  ├───▶│         │───▶│ Memory   │──▶│ 3-State  │──▶──12  Q1
A4   6  │    │ Address │    │ Matrix   │   │ Output   │   ──13  Q2
A5   5  │    │ Decode  │    │(32,768×8)│   │ Buffers  │──▶──15  Q3
A6   4  │    │         │    └──────────┘   │          │   ──16  Q4
A7   3  │    │         │                   │          │──▶──17  Q5
A8  25  │    │         │                   │          │   ──18  Q6
A9  24  │    │         │                   │          │──▶──19  Q7
A10 21  │    │         │                   └──────────┘
A11 23  │    │         │
A12  2  │    │         │
A13 26  │    └─────────┘
A14 27 ─┘
```

E̅  20
*G̅  22

VCC = Pin 28
VSS = Pin 14
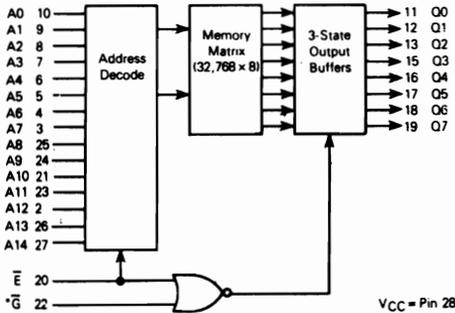
*Active level defined by the user.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

# 65,536 × 8 STATIC READ ONLY MEMORY

## FEATURES

- 65,536 × 8 bit organization
- Access time – 150 ns max
- Current — Operating: 100 mA max
  Standby: 20 mA max
- Total static operation
- Static 5 V supply
- Automatic powerdown ($\overline{CE}$)
- Complete TTL compatibility
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC approved pinout
- EPROMs accepted as program data input

## DESCRIPTION

The VT23512 high performance Read Only Memory is organized 65,536 words by eight bits with an access time of 150 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

The VT23512 offers automatic powerdown with powerdown controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically powerdown and remain in a low-power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system level power savings of as much as 80%. The VT23512 also has an Output Enable ($\overline{OE}$) function to eliminate bus contention in multiple-bus microprocessor systems.

## PIN DIAGRAM
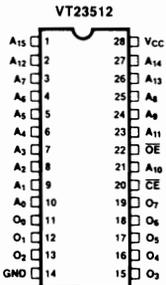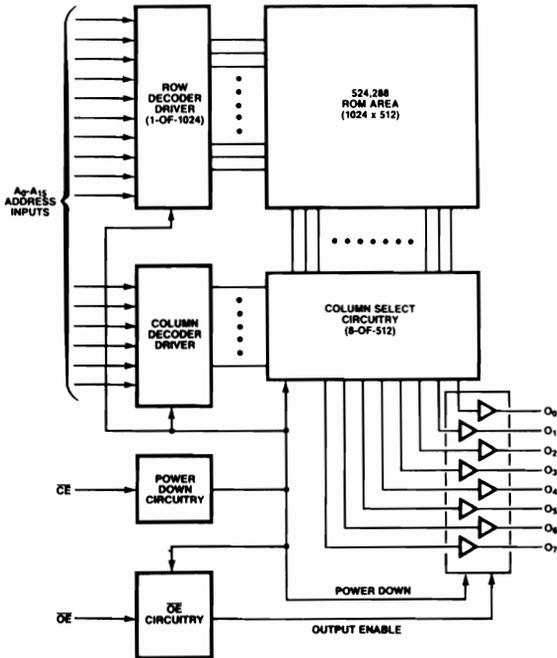
VT23512

| | | | |
|---|---|---|---|
| A$_{15}$ | 1 | 28 | V$_{CC}$ |
| A$_{12}$ | 2 | 27 | A$_{14}$ |
| A$_7$ | 3 | 26 | A$_{13}$ |
| A$_6$ | 4 | 25 | A$_8$ |
| A$_5$ | 5 | 24 | A$_9$ |
| A$_4$ | 6 | 23 | A$_{11}$ |
| A$_3$ | 7 | 22 | $\overline{OE}$ |
| A$_2$ | 8 | 21 | A$_{10}$ |
| A$_1$ | 9 | 20 | $\overline{CE}$ |
| A$_0$ | 10 | 19 | O$_7$ |
| O$_0$ | 11 | 18 | O$_6$ |
| O$_1$ | 12 | 17 | O$_5$ |
| O$_2$ | 13 | 16 | O$_4$ |
| GND | 14 | 15 | O$_3$ |

## BLOCK DIAGRAM

## 1MB (128K WORD × 8 BIT) CMOS MASK ROM
### SILICON GATE CMOS

**TC531000AP**

The TC531000AP is a 1,048,576 bit read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in microprocessor program memory and especially character generation. The TC531000AP, using CMOS technology, is most suitable for low power applications where battery operations are required.

The TC531000AP has one chip enable input $\overline{CE}$/CE, programmable for device selection.

The TC531000AP is molded in a 28 pin standard plastic package and is 0.6 inch in width.

### PIN CONNECTION – 28 PIN (TOP VIEW)
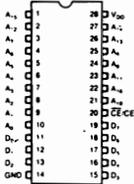
### PIN NAMES

| $A_0 \sim A_{16}$ | Address Inputs |
|---|---|
| $D_0 \sim D_7$ | Data Outputs |
| $\overline{CE}$/CE | Chip Enable Input |
| $V_{DD}$ | Power Supply |
| GND | Ground |

- Single 5V Power Supply
- Access Time: 150ns (Max.)
- Power Dissipation
  Operating Current: 40mA (Max.)
  Standby Current: 20μA (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 28 pin 600 mil width DIP Plastic Package
- Fully Static Operation
- Programmable Chip Enable

## 2MB (256K WORD × 8 BIT) CMOS MASK ROM
### SILICON GATE CMOS

**TC532000P**

The TC532000P is a 2,097,152 bit read only memory organized as 262,144 words by 8 bits with a low bit cost, thus being suitable for use in microprocessor program memory, data memory, and especially character generation. The TC532000P, using CMOS technology, is most suitable for low power applications where battery operations are required.

- Single 5V Power Supply
- Access Time: 200 ns (Max.)
- Power Dissipation
  Operating Current: 30mA (Max.)
  Standby Current: 20μA (Max.)

The TC532000P has one programmable chip enable input $\overline{CE}$/CE for device selection.

The TC532000P is molded in a 32 pin standard plastic package and is 0.6 inch in width.

- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 32 pin 600 mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

### PIN CONNECTION – 32 PIN (TOP VIEW)

| N.C. | 1 | 32 | $V_{DD}$ |
|---|---|---|---|
| A16 | 2 | 31 | N.C. |
| A15 | 3 | 30 | A17 |
| A12 | 4 | 29 | A14 |
| A7 | 5 | 28 | A13 |
| A6 | 6 | 27 | A8 |
| A5 | 7 | 26 | A9 |
| A4 | 8 | 25 | A11 |
| A3 | 9 | 24 | $\overline{OE}$ |
| A2 | 10 | 23 | A10 |
| A1 | 11 | 22 | CE/$\overline{CE}$ |
| A0 | 12 | 21 | D7 |
| D0 | 13 | 20 | D6 |
| D1 | 14 | 19 | D5 |
| D2 | 15 | 18 | D4 |
| GND | 16 | 17 | D3 |
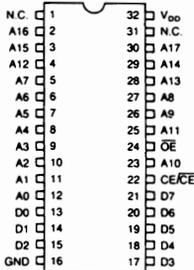
### PIN NAMES

| $A_0 \sim A_{17}$ | Address Inputs |
|---|---|
| $D_0 \sim D_7$ | Data Outputs |
| $\overline{OE}$ | Output Enable Input |
| CE/$\overline{CE}$ | Chip Enable Input |
| $V_{DD}$ | Power Supply |
| GND | Ground |
| N.C. | No connection |

### BLOCK DIAGRAM (2MB)

600
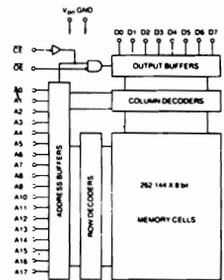
# 2708
# 8K (1K × 8) UV ERASABLE PROM

|        | Max. Power | Max. Access |
|--------|------------|-------------|
| 2708   | 800 mW     | 450 ns      |
| 2708L  | 425 mW     | 450 ns      |
| 2708-1 | 800 mW     | 350 ns      |
| 2708-6 | 800 mW     | 550 ns      |

- **Low Power Dissipation — 425 mW Max. (2708L)**
- **Fast Access Time — 350 ns Max. (2708-1)**
- **Static — No Clocks Required**
- **Data Inputs and Outputs TTL Compatible during both Read and Program Modes**
- **Three-State Outputs — OR-Tie Capability**

The Intel® 2708 is an 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM, ideally suited where fast turnaround and pattern experimentation are important requirements. All data inputs and outputs are TTL compatible during both the read and program modes. The outputs are three-state, allowing direct interface with common system bus structures.

The 2708L at 425 mW is available for systems requiring lower power dissipation than from the 2708. A power dissipation savings of over 50% without any sacrifice in speed is obtained with the 2708L. The 2708L has high input noise immunity and is specified at 10% power supply tolerance. A high-speed 2708-1 is also available at 350 ns for microprocessors requiring fast access times.

The 2708 family is fabricated with the N-channel silicon gate FAMOS technology and is available in a 24-pin dual in-line package.

## PIN CONFIGURATION
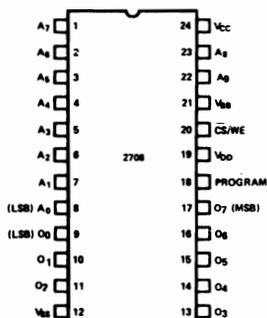


## BLOCK DIAGRAM
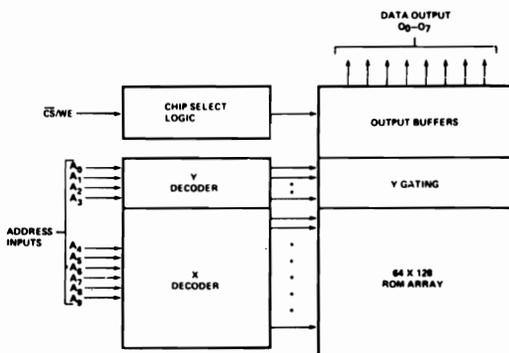


## PIN NAMES

| $A_0$-$A_9$ | ADDRESS INPUTS |
|------|------|
| $O_1$-$O_8$ | DATA OUTPUTS/INPUTS |
| CS/WE | CHIP SELECT/WRITE ENABLE INPUT |

## PIN CONNECTION DURING READ OR PROGRAM

| | | PIN NUMBER | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | DATA I/O 9-11, | ADDRESS INPUTS 1-8, | $V_{SS}$ | PROGRAM | $V_{DD}$ | CS/WE | $V_{BB}$ | $V_{CC}$ |
| MODE | 13-17 | 22, 23 | 12 | 18 | 19 | 20 | 21 | 24 |
| READ | $D_{OUT}$ | $A_{IN}$ | GND | GND | +12 | $V_{IL}$ | -5 | +5 |
| DESELECT | HIGH IMPEDANCE | DON'T CARE | GND | GND | +12 | $V_{IH}$ | -5 | +5 |
| PROGRAM | $D_{IN}$ | $A_{IN}$ | GND | PULSED 26V | +12 | $V_{IHW}$ | -5 | +5 |

# 2716
# 16K (2K × 8) UV ERASABLE PROM

- **Fast Access Time**
  - 350 ns Max. 2716-1
  - 390 ns Max. 2716-2
  - 450 ns Max. 2716
  - 490 ns Max. 2716-5
  - 650 ns Max. 2716-6

- **Single +5V Power Supply**

- **Low Power Dissipation**
  - 525 mW Max. Active Power
  - 132 mW Max. Standby Power

- **Pin Compatible to Intel® 2732 EPROM**

- **Simple Programming Requirements**
  - Single Location Programming
  - Programs with One 50 ms Pulse

- **Inputs and Outputs TTL Compatible during Read and Program**

- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. A selected 2716-5 and 2716-6 is available for slower speed applications. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

## PIN CONFIGURATION

### 2716

```
A7  [ 1      24 ] VCC
A6  [ 2      23 ] A8
A5  [ 3      22 ] A9
A4  [ 4      21 ] VPP
A3  [ 5  16K 20 ] OE
A2  [ 6      19 ] A10
A1  [ 7      18 ] CE
A0  [ 8      17 ] O7
O0  [ 9      16 ] O6
O1  [ 10     15 ] O5
O2  [ 11     14 ] O4
GND [ 12     13 ] O3
```

### 2732 †

```
A7  [ 1      24 ] VCC
A6  [ 2      23 ] A8
A5  [ 3      22 ] A9
A4  [ 4      21 ] A11
A3  [ 5  32K 20 ] OE/VPP
A2  [ 6      19 ] A10
A1  [ 7      18 ] CE
A0  [ 8      17 ] O7
O0  [ 9      16 ] O6
O1  [ 10     15 ] O5
O2  [ 11     14 ] O4
GND [ 12     13 ] O3
```
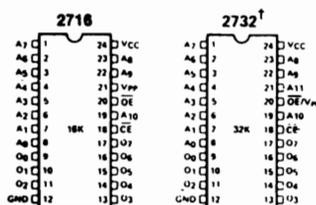
†Refer to 2732 data sheet for specifications

## PIN NAMES

| | |
|---|---|
| A0-A10 | ADDRESSES |
| CE/PGM | CHIP ENABLE/PROGRAM |
| OE | OUTPUT ENABLE |
| O0-O7 | OUTPUTS |

## MODE SELECTION

| PINS MODE | CE/PGM (18) | OE (20) | VPP (21) | VCC (24) | OUTPUTS (9-11, 13-17) |
|---|---|---|---|---|---|
| Read | VIL | VIL | +5 | +5 | DOUT |
| Standby | VIH | Don't Care | +5 | +5 | High Z |
| Program | Pulsed VIL to VIH | VIH | +25 | +5 | DIN |
| Program Verify | VIL | VIL | +25 | +5 | DOUT |
| Program Inhibit | VIL | VIH | +25 | +5 | High Z |

## BLOCK DIAGRAM
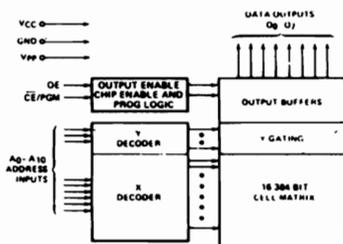
## ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instruction Section) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu$W/cm$^2$ power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

## DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V $V_{CC}$ and a $V_{PP}$. The $V_{PP}$ power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

### TABLE I. MODE SELECTION

| PINS<br>MODE | CE/PGM<br>(18) | OE<br>(20) | Vpp<br>(21) | Vcc<br>(24) | OUTPUTS<br>(9-11, 13-17) |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | +5 | +5 | $D_{OUT}$ |
| Standby | $V_{IH}$ | Don't Care | +5 | +5 | High Z |
| Program | Pulsed $V_{IL}$ to $V_{IH}$ | $V_{IH}$ | +25 | +5 | $D_{IN}$ |
| Program Verify | $V_{IL}$ | $V_{IL}$ | +25 | +5 | $D_{OUT}$ |
| Program Inhibit | $V_{IL}$ | $V_{IH}$ | +25 | +5 | High Z |

### READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from CE to output ($t_{CE}$). Data is available at the outputs 120 ns ($t_{OE}$) after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

### STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the CE input. When in standby mode, the outputs are in a high impedence state, independent of the OE input.

## OUTPUT OR-TIEING

Because 2716's are usually used in larger memory arrays, Intel has provided a 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE (pin 18) be decoded and used as the primary device selecting function, while OE (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

## PROGRAMMING

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the $V_{PP}$ power supply is at 25V and OE is at $V_{IH}$. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the CE/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the CE/PGM input programs the paralleled 2716s.

## PROGRAM INHIBIT

Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for CE/PGM, all like inputs (including OE) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's CE/PGM input with $V_{PP}$ at 25V will program that 2716. A low level CE/PGM input inhibits the other 2716 from being programmed.

## PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with $V_{PP}$ at 25V. Except during programming and program verify, $V_{PP}$ must be at 5V.

# 2732
# 32K (4K x 8) UV ERASABLE PROM

- **Fast Access Time:**
  - **— 450 ns Max. 2732**
  - **— 550 ns Max. 2732-6**

- **Single +5V ± 5% Power Supply**

- **Output Enable for MCS-85™ and MCS-86™ Compatibility**

- **Low Power Dissipation: 150mA Max. Active Current 30mA Max. Standby Current**

- **Pin Compatible to Intel® 2716 EPROM**

- **Completely Static**

- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50ms Pulse**

- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM) The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The total programming time for all bits is three and a half minutes. All these features make designing with the 2732 in microcomputer systems faster, easier, and more economical.

An important 2732 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The OE control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's 2716 and 2732 EPROMs. AP-72 is available from Intel's Literature Department.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

## PIN CONFIGURATION

```
A7  [ 1      24 ]  Vcc
A6  [ 2      23 ]  A8
A5  [ 3      22 ]  A9
A4  [ 4      21 ]  A11
A3  [ 5      20 ]  OE/Vpp
A2  [ 6      19 ]  A10
A1  [ 7      18 ]  CE
A0  [ 8      17 ]  O7
O0  [ 9      16 ]  O6
O1  [ 10     15 ]  O5
O2  [ 11     14 ]  O4
GND [ 12     13 ]  O3
```
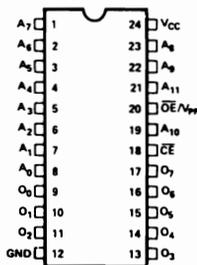
## PIN NAMES

| | |
|---|---|
| $A_0$-$A_{11}$ | ADDRESSES |
| $\overline{CE}$ | CHIP ENABLE |
| $\overline{OE}$ | OUTPUT ENABLE |
| $O_0$-$O_7$ | OUTPUTS |

## MODE SELECTION

| MODE \ PINS | $\overline{CE}$ (18) | $\overline{OE}/V_{PP}$ (20) | $V_{CC}$ (24) | OUTPUTS (9-11,13-17) |
|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | +5 | $D_{OUT}$ |
| Standby | $V_{IH}$ | Don't Care | +5 | High Z |
| Program | $V_{IL}$ | $V_{PP}$ | +5 | $D_{IN}$ |
| Program Verify | $V_{IL}$ | $V_{IL}$ | +5 | $D_{OUT}$ |
| Program Inhibit | $V_{IH}$ | $V_{PP}$ | +5 | High Z |

## BLOCK DIAGRAM



604
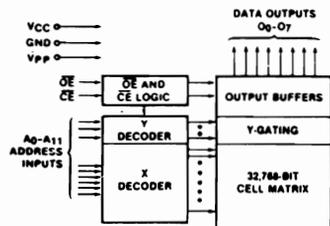
# 2764
# (8K × 8) UV ERASABLE PROM

- **200 ns (2764-2) Maximum Access Time . . . HMOS\*-E Technology**

- **Compatible to high speed 8mHz 8086-2 MPU . . . Zero WAIT State**

- **Two Line Control**

- **Pin Compatible to 2732A EPROM**

- **Industry Standard Pinout . . . JEDEC Approved**

- **Low Standby Current . . . 35mA Max.**

The Intel® 2764 is a 5V only 65,536 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 2764 access time is 250ns with speed selection available at 200ns. The access time is compatible to high performance microprocessors, such as Intel's 8mHz 8086-2. In these systems, the 2764 allows the microprocessor to operate without the addition of WAIT states.

An important 2764 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 2764 has a standby mode which reduces the power dissipation without increasing access time. The active current is 150mA, while the standby current is only 35mA, a 75% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The 2764 is fabricated with HMOS\*-E technology, Intel's high-speed N-channel MOS Silicon Gate    chnology.



## 2732A PIN CONFIGURATION

## 2764 PIN CONFIGURATION
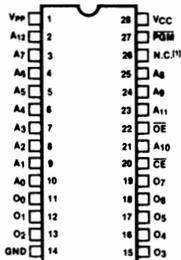
[1]For total compatibility from 2732A provide a trace to pin 26

## BLOCK DIAGRAM

### PIN NAMES

| | |
|---|---|
| A₀-A₁₂ | ADDRESSES |
| $\overline{CE}$ | CHIP ENABLE |
| $\overline{OE}$ | OUTPUT ENABLE |
| O₀-O₇ | OUTPUTS |
| $\overline{PGM}$ | PROGRAM |
| N.C.[1] | NO CONNECT |
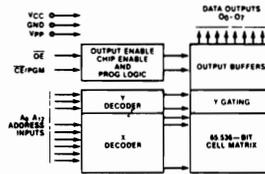
## MODE SELECTION

| PINS<br>MODE | $\overline{CE}$<br>(20) | $\overline{OE}$<br>(22) | $\overline{PGM}$<br>(27) | Vpp<br>(1) | Vcc<br>(28) | Outputs<br>(11-13, 15-19) |
|---|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | D_OUT |
| Standby | $V_{IH}$ | x | x | $V_{CC}$ | $V_{CC}$ | High Z |
| Program | $V_{IL}$ | x | $V_{IL}$ | $V_{PP}$ | $V_{CC}$ | D_IN |
| Program Verify | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{PP}$ | $V_{CC}$ | D_OUT |
| Program Inhibit | $V_{IH}$ | x | x | $V_{PP}$ | $V_{CC}$ | High Z |

x can be either $V_{IL}$ or $V_{IH}$

\*HMOS is a patented process of Intel Corporation.

605

# 2816
# 16K (2K x 8) ELECTRICALLY ERASABLE PROM

- ■ HMOS-E *FLOTOX Cell Design
- ■ Reliable Floating Gate Technology
- ■ Very Fast Access Time
  - — 250 ns Max. — 2816
  - — 350 ns Max. — 2816-3
- ■ Single Byte Erase/Write Capability
- ■ 10 ms Byte Erase/Write Time
- ■ Chip Erase Time of 10 ms

- ■ Conforms to JEDEC Byte-Wide Family Standard
- ■ Microprocessor Compatible Architecture
- ■ Low Power Dissipation
  - —495 mW Max. Active Power
  - —132 mW Max. Standby Power
- ■ Erase/Write Specifications Guaranteed 0-70°C

The Intel® 2816 is a 16,384 bit electrically erasable programmable read-only memory (E²PROM). The 2816 can be easily erased and reprogrammed on a byte basis. A chip erase function is also provided. The device operates from a 5-volt power supply in the read mode; writing and erasing are accomplished by providing a single 21-volt pulse.

The 2816, with its very fast read access speed, is compatible with high performance microprocessors such as the 8086-2. Using the fast access speed allows zero wait operation in large system configurations.

The electrical erase/write capability of the 2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write. Never before has in-system alterability been possible with this combination of density, performance and flexibility. Any byte can be erased or written in 10 ms without affecting the data in any other byte. Alternatively, the entire memory can be erased in 10 ms allowing the total time to rewrite all 2K bytes to be cut by 50%. The 2816 provides a significant increase in flexibility allowing new applications (dynamic reconfiguration, continuous calibration) never before possible.

The 2816 E²PROM possesses Intel's 2-line control architecture to eliminate bus contention in a system environment. A power down mode is also featured; In the standby mode power consumption is reduced by over 73% without increasing access time. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

Byte erase and write are controlled entirely by TTL signal levels, yet require no control signals beyond $\overline{CE}$ and $\overline{OE}$. For byte write a selected chip ($\overline{CE}$ = TTL low) senses the 21V $V_{PP}$ pulse and automatically goes into write mode. Byte erase mode is identical to byte write except that data-in must be all logic ones (TTL-high). Never before has an in-system alteration of non-volatile information been implemented with such simple control.

*HMOS-E is a patented process of Intel Corporation.
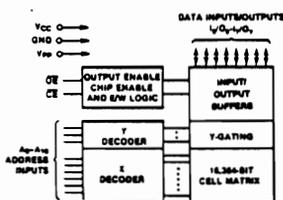


Figure 1. 2816 Functional Block Diagram      Figure 2. Pin Diagrams
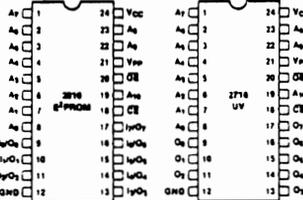
| PIN NAMES | |
|---|---|
| A₀-A₁₀ | ADDRESSES |
| $\overline{CE}$ | CHIP ENABLE |
| $\overline{OE}$ | OUTPUT ENABLE |
| O₀-O₇ | DATA OUTPUTS |
| I₀-I₇ | DATA INPUTS |
| V_PP | PROGRAM VOLTAGE |

# 27128A
# ADVANCED 128K (16K x 8) PRODUCTION AND UV ERASABLE PROMs

- ■ Fast 200 nsec Access Time
  — HMOS* II-E Technology
- ■ Low Power
  — 100 mA Maximum Active
  — 40 mA Maximum Standby
- ■ Int<sub>e</sub>ligent Identifier™ Mode
  — Automated Programming Operations
- ■ Compatible with 2764A, 27128, 27256

- ■ New Quick-Pulse Programming™ Algorithm
  — Used on Plastic DIP
  — Int<sub>e</sub>ligent Programming™ Algorithm Compatible
- ■ ±10% V<sub>CC</sub> Tolerance Available
- ■ Available in 28-Pin Cerdip and Plastic Packages
  (See Packaging Spec, Order #231369)

The Intel 27128A is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 27128A is an advanced high speed version of the 27128 and is fabricated with Intel's HMOSII-E technology which significantly reduces die size and greatly improves the device's performance, reliability and manufacturability.

The 27128A is currently available in two different package types. CERDIP packages provide flexibility in prototyping and R&D environments where reprogrammability is required. Plastic DIP EPROMs provide optimum cost effectiveness in production environments.

Intel's new Quick-Pulse Programming Algorithm enables these Plastic EPROMs to be programmed within two seconds. Programming equipment that takes advantage of this innovation will electronically identify the EPROM with the help of the int<sub>e</sub>ligent Identifier and rapidly program it using a superior programming method. The int<sub>e</sub>ligent Programming Algorithm may be utilized in the absence of such equipment and is used to program CERDIP devices.

The 27128A is available in fast access times including 200 ns (27128A-2). This ensures compatibility with high-performance microprocessors, such as Intel's 8 MHz 80186 allowing full speed operation without the addition of WAIT states. The 27128A is also directly compatible with the 12 MHz 8051 family. For access times down to 110 ns, refer to the 27128B data sheet.

*HMOS is a patented process of Intel Corporation.
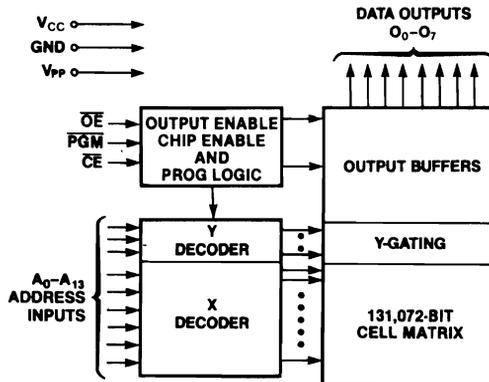


**Figure 1. Block Diagram**

230849-1

# 27256
# 256K (32K x 8) PRODUCTION AND UV ERASABLE PROMS

- **New Quick-Pulse Programming™ Algorithm for Plastic P27256**
  - **4 Second Programming**
  - **int₂ligent Programming™ Algorithm Compatible**
- **Fast Access Time**
  - **170 ns D27256-1**
  - **200 ns P27256-2**
- **int₂ligent Identifier™ Mode**

- **Plastic Production P27256 is Compatible with Auto-Insertion Equipment**
- **Moisture Resistant**
- **Industry Standard Pinout ... JEDEC Approved ... 28 Lead Cerdip and Plastic Package**
  (See Packaging Spec, Order #231369)

The Intel 27256 is a 5V only, 262,144-bit Ultraviolet Erasable (Cerdip)/plastic production (P27256) electrically programmable read-only memory (EPROM). Organized as 32K words by 8 bits, individual bytes can be accessed in less than 170 ns (27256-1). This is compatible with high performance microprocessors, such as the Intel iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The Plastic P27256 is ideal for high volume production environments where code flexibility is crucial. Plastic packaging is also well-suited to auto-insertion equipment in cost-effective automated assembly lines. Intel's new Quick-Pulse Programming Algorithm enables the P27256 to be programmed within four seconds (plus programmer overhead). Programming equipment which takes advantage of this innovation will electronically identify the EPROM with the help of the int₂ligent Identifier and rapidly program it using a superior programming method. The int₂ligent Programming Algorithm may be utilized in the absence of such equipment.

The 27256 enables implementation of new, advanced systems with firmware-intensive architectures. The combination of the 27256's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The 27256's large storage capability of 32 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS*II-E technology.

*HMOS is a patented process of Intel Corporation.
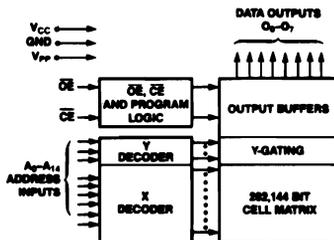


290097-1

**Figure 1. Block Diagram**

## Pin Names

| | |
|---|---|
| $A_0$–$A_{14}$ | Addresses |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $O_0$–$O_7$ | Outputs |
| D.U. | Don't Use |
| $\overline{WE}$ | Write Enable |

### 27256 / P27256

| 27916 | 27513 | 27512 | 27128A | 2764A 27C64 | 2732A | 2716 |
|---|---|---|---|---|---|---|
| $V_{PP}$ | D.U. | $A_{15}$ | $V_{PP}$ | $V_{PP}$ | | |
| $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_{12}$ | $A_7$ | $A_7$ |
| $A_7$ | $A_7$ | $A_7$ | $A_7$ | $A_7$ | $A_6$ | $A_6$ |
| $A_6$ | $A_6$ | $A_6$ | $A_6$ | $A_6$ | $A_5$ | $A_5$ |
| $A_5$ | $A_5$ | $A_5$ | $A_5$ | $A_5$ | $A_4$ | $A_4$ |
| $A_4$ | $A_4$ | $A_4$ | $A_4$ | $A_4$ | $A_3$ | $A_3$ |
| $A_3$ | $A_3$ | $A_3$ | $A_3$ | $A_3$ | $A_2$ | $A_2$ |
| $A_2$ | $A_2$ | $A_2$ | $A_2$ | $A_2$ | $A_1$ | $A_1$ |
| $A_1$ | $A_1$ | $A_1$ | $A_1$ | $A_1$ | $A_0$ | $A_0$ |
| $A_0$ | $A_0$ | $A_0$ | $A_0$ | $A_0$ | $O_0$ | $O_0$ |
| $O_0$ | $D_0/O_0$ | $O_0$ | $O_0$ | $O_0$ | $O_1$ | $O_1$ |
| $O_1$ | $D_1/O_1$ | $O_1$ | $O_1$ | $O_1$ | $O_2$ | $O_2$ |
| $O_2$ | $O_2$ | $O_2$ | $O_2$ | $O_2$ | Gnd | Gnd |
| Gnd | Gnd | Gnd | Gnd | Gnd | Gnd | Gnd |

P27256 DIP pin assignments:
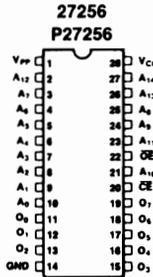
| Pin | | Pin | |
|---|---|---|---|
| 1 | $V_{PP}$ | 28 | $V_{CC}$ |
| 2 | $A_{12}$ | 27 | $A_{14}$ |
| 3 | $A_7$ | 26 | $A_{13}$ |
| 4 | $A_6$ | 25 | $A_8$ |
| 5 | $A_5$ | 24 | $A_9$ |
| 6 | $A_4$ | 23 | $A_{11}$ |
| 7 | $A_3$ | 22 | $\overline{OE}$ |
| 8 | $A_2$ | 21 | $A_{10}$ |
| 9 | $A_1$ | 20 | $\overline{CE}$ |
| 10 | $A_0$ | 19 | $O_7$ |
| 11 | $O_0$ | 18 | $O_6$ |
| 12 | $O_1$ | 17 | $O_5$ |
| 13 | $O_2$ | 16 | $O_4$ |
| 14 | GND | 15 | $O_3$ |

| 2716 | 2732A | 2764A 27C64 | 27128A | 27512 | 27513 | 27916 |
|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ | $V_{CC}$ PGM | $V_{CC}$ PGM | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ |
| | | N.C. | $A_{14}$ | $A_{14}$ | $\overline{WE}$ | PGM/$\overline{WE}$ |
| $V_{CC}$ | $V_{CC}$ | $A_{13}$ | $A_{13}$ | $A_{13}$ | $A_{13}$ | $A_{13}$ |
| $A_8$ | $A_8$ | $A_8$ | $A_8$ | $A_8$ | $A_8$ | $A_8$ |
| $A_9$ | $A_9$ | $A_9$ | $A_9$ | $A_9$ | $A_9$ | $A_9$ |
| $V_{PP}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ | $A_{11}$ |
| $\overline{OE}$ | $\overline{OE}$/$V_{PP}$ | $\overline{OE}$ | $\overline{OE}$ | $\overline{OE}$/$V_{PP}$ | $\overline{OE}$/$V_{PP}$ | $\overline{OE}$ |
| $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ | $A_{10}$ |
| $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ | $\overline{CE}$ |
| $O_7$ | $O_7$ | $O_7$ | $O_7$ | $O_7$ | $O_7$ | $O_7$ |
| $O_6$ | $O_6$ | $O_6$ | $O_6$ | $O_6$ | $O_6$ | $O_6$ |
| $O_5$ | $O_5$ | $O_5$ | $O_5$ | $O_5$ | $O_5$ | $O_5$ |
| $O_4$ | $O_4$ | $O_4$ | $O_4$ | $O_4$ | $O_4$ | $O_4$ |
| $O_3$ | $O_3$ | $O_3$ | $O_3$ | $O_3$ | $O_3$ | $O_3$ |

290097-2

**NOTE:**
Intel"Universal Site"-Compatible EPROM pin configurations are shown in the blocks adjacent to the P27256 pins.

**Figure 2. Cerdip/Plastic DIP Pin Configuration**

# 27512
# 512K (64K x 8) PRODUCTION AND
# UV ERASABLE PROM

- Software Carrier Capability
- 170 ns Maximum Access Time
- Two-Line Control
- Int$_e$lligent Identifier™ Mode
  — Automated Programming Operations
- TTL Compatible

- Low Power
  — 125 mA max. Active
  — 40 mA max. Standby
- Int$_e$lligent Programming™ Algorithm
- Available in 28-Pin Cerdip
  (See packaging spec order #231369)

The Intel 27512 is a 5V-only, 524,288-bit ultraviolet Erasable and Electrically Programmable Read Only Me﹐ .i3-ry (EPROM) organized as 64K words by 8 bits. This ensures compatibility with high-performance microprocessors, such as the Intel 8 MHz iAPX 286, allowing full speed operation without the addition of performance-degrading WAIT states. The 27512 is also directly compatible with Intel's 8051 family of microcontrollers.

The 27512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the 27512's high-density, cost-effective EPROM storage, and new advanced microprocessors having megabyte addressing capability provides designers with opportunities to engineer user-friendly, high-reliability, high-performance systems.

The 27512's large storage capability of 64 K-bytes enables it to function as a high-density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27512 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time-consuming disk accesses and downloads.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27512 is manufactured using Intel's advanced HMOS *II-E technology.

*HMOS is a patented process of Intel Corporation.



231088-1
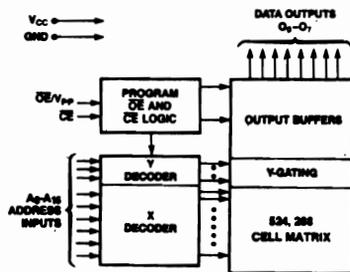
Figure 1. Block Diagram

## Pin Names

| | |
|---|---|
| A0–A15 | Addresses |
| CE | Chip Enable |
| OE/Vpp | Outputs Enable/Vpp |
| O0–O7 | Outputs |
| D.U. | Don't Use |

| 27513 | 27256 27C256 87C256 | 27128 27128A | 2764 2764A 27C64 87C64 |
|---|---|---|---|
| D.U. | Vpp | Vpp | Vpp |
| A12 | A12 | A12 | A12 |
| A7 | A7 | A7 | A7 |
| A6 | A6 | A6 | A6 |
| A5 | A5 | A5 | A5 |
| A4 | A4 | A4 | A4 |
| A3 | A3 | A3 | A3 |
| A2 | A2 | A2 | A2 |
| A1 | A1 | A1 | A1 |
| A0 | A0 | A0 | A0 |
| D0/O0 | O0 | O0 | O0 |
| D1/O1 | O1 | O1 | O1 |
| O2 | O2 | O2 | O2 |
| Gnd | Gnd | Gnd | Gnd |

**27512**
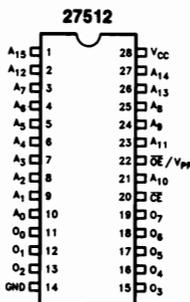
| Pin | | Pin |
|---|---|---|
| A15 | 1 | 28 Vcc |
| A12 | 2 | 27 A14 |
| A7 | 3 | 26 A13 |
| A6 | 4 | 25 A8 |
| A5 | 5 | 24 A9 |
| A4 | 6 | 23 A11 |
| A3 | 7 | 22 OE/Vpp |
| A2 | 8 | 21 A10 |
| A1 | 9 | 20 CE |
| A0 | 10 | 19 O7 |
| O0 | 11 | 18 O6 |
| O1 | 12 | 17 O5 |
| O2 | 13 | 16 O4 |
| GND | 14 | 15 O3 |

| 2764 2764A 27C64 87C64 | 27128 27128A | 27256 27C256 | 27513 |
|---|---|---|---|
| Vcc | Vcc | Vcc | Vcc |
| PGM | PGM | A14 | WE |
| N.C. | A13 | A13 | A13 |
| A8 | A8 | A8 | A8 |
| A9 | A9 | A9 | A9 |
| A11 | A11 | A11 | A11 |
| OE | OE | OE | OE/Vpp |
| A10 | A10 | A10 | A10 |
| CE ALE/CE | CE | CE ALE/CE | CE |
| O7 | O7 | O7 | O7 |
| O6 | O6 | O6 | O6 |
| O5 | O5 | O5 | O5 |
| O4 | O4 | O4 | O4 |
| O3 | O3 | O3 | O3 |

231088–2

**Figure 2. Pin Configurations**

## EXTENDED TEMPERATURE (EXPRESS) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. EXPRESS EPROM products are available with 168 ±8 hours, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

## EXPRESS EPROM PRODUCT FAMILY

### PRODUCT DEFINITIONS

| Type | Operating Temperature | Burn-in 125°C (hr) |
|---|---|---|
| Q | 0°C to +70°C | 168 ±8 |
| T | −40°C to +85°C | None |
| L | −40°C to +85°C | 168 ±8 |

## EXPRESS OPTIONS

### 27512 VERSIONS

| Packaging Options | |
|---|---|
| Speed Versions | Cerdip |
| -170V05 | Q |
| -200V05, -200V10 | Q, L |
| -STD, -25, -250V10 | Q, T, L |
| -3, -30 | Q, T, L |

# 27F64
# 64K (8K x 8) CHMOS FLASH MEMORY

- ■ **Quick-Erase™ Algorithm**
  - — **Two Second Typical Array Electrical Erasure**
- ■ **High Performance Speeds**
  - — **150 ns Maximum Access Time**
- ■ **Low Power Consumption**
  - — **100 μA Maximum Standby Current for Power-Down Savings**
- ■ **Quick-Pulse Programming™ Algorithm**
  - — **One Second Typical Chip Program**

- ■ **On-Board Program/Erase**
  - — **New Modes Simplify In-Module Firmware Upgrades**
- ■ **2764A and 27C64 JEDEC Pinout**
  - — **28 Pin Cerdip Package**
  - (See Packaging Spec., Order # 231369)
- ■ **EPROM Based ETOX™ Process**
  - — **3 Year CHMOS* EPROM Manufacturing Base**
  - — **± 10% $V_{CC}$ Tolerance**
  - — **Improved Latch-Up Immunity through EPI Processing**

The Intel 27F64 (EPROM tunnel oxide) ETOX™ flash memory is a 64K bit non-volatile memory organized as 8192 bytes of 8 bits. The 27F64 electrically erases all bits in parallel, making it ideal for EPROM applications where U.V. erasure is impractical or time consuming. Electrical erasure allows manufacturers to efficiently implement code changes for testing and end-of-line final configuration.

To decrease the cost of servicing and updating program code, the 27F64 offers new programming and erase modes called On-Board modes. These modes simplify in-circuit programming and erasure by maintaining $V_{CC}$ at 5V, and $\overline{CE}$ and $\overline{OE}$ at standard logic levels. Devices socketed or soldered to circuit boards can be erased and programmed via an edge connector to a PROM programmer, or via the board tester already available. The Quick-Erase™ algorithm and On-Board features give system designers innovative capabilities. Compared to byte-alterable E2PROM, these features address industry's need for a cost-effective code update solution.

Intel's new ETOX** flash memory process combines the programming mechanism of EPROM with the erase mechanism of E2PROM to produce dense electrically erasable memories with the reliability and manufacturability of today's EPROM technology.

Intel's unique Epitaxial (EPI) processing provides excellent latch-up immunity. Prevention of latch-up is specified for stress up to 100 mA from −1V to $V_{CC}$ + 1V on address and data pins. All high voltage pins are protected from overshoot up to 14V.
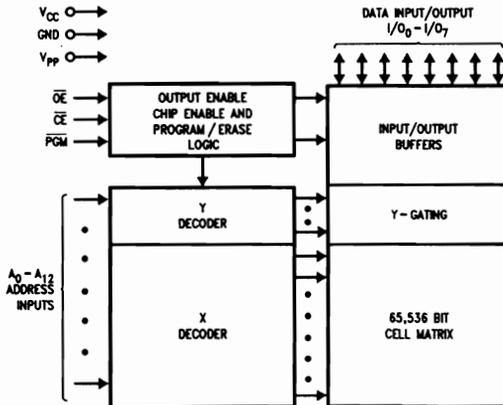


**Figure 1. 27F64 Internal Block Diagram**

290153–1

*CHMOS is a patented process of Intel Corporation.

**Intel's ETOX™ flash process has patents pending.

## 27F64



290153-2
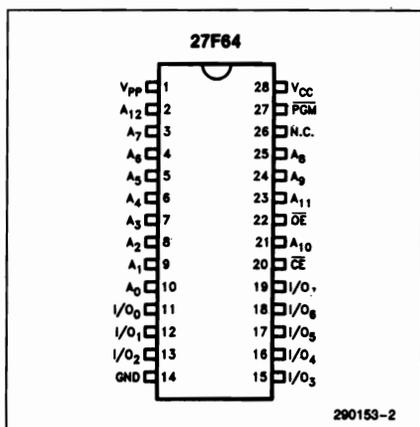
**Figure 2. Cerdip (D) Pin Configuration**

### Pin Names

| | |
|---|---|
| $A_0-A_{12}$ | Addresses |
| $I/O_0-I/O_7$ | Data Input/Output |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $\overline{PGM}$ | Program |
| $V_{PP}$ | Program/Erase Power |
| $V_{CC}$ | Device Power |
| GND | Ground |
| N.C. | No Internal Connection |

### Table 1. Pin Description

| Symbol | Type | Name and Function |
|---|---|---|
| $A_0-A_{12}$ | I | **ADDRESS BUS** inputs the memory addresses, and selects the 8 bits in the 256 row by 256 column array. |
| $I/O_0-I/O_7$ | I/O | **DATA BUS** inputs data during memory program cycles; outputs data during memory read cycles. The data bus is active high and floats to tri-state OFF when the chip is deselected or the outputs disabled. |
| $\overline{CE}$ | I | **CHIP ENABLE** activates the device's control logic, input buffers, decoders, and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels. |
| $\overline{OE}$ | I | **OUTPUT ENABLE** when active low gates the device's output through the data buffers during a read cycle. $\overline{OE}$ driven to a third logic level $V_H$ 11.5V–13.0V, selects the conventional chip erase mode. |
| $\overline{PGM}$ | I | **PROGRAM** controls the program and erase pulse-width in the conventional modes by being driven low. $\overline{PGM}$ driven to a third logic level $V_H$ (11.5V–13.0V) gates entry into the On-Board program verify, erase, and erase verify modes*. In the On-Board erase mode, $\overline{CE}$ controls the erase pulse width. |
| $V_{PP}$ | | **PROGRAM/ERASE POWER SUPPLY** (12.75V ±0.25V) for programming and erasing the device. $V_{PP}$ also supplies the Flash memory cell margin voltage during the On-Board program verify and erase verify modes. In these modes, $V_{PP}$ must switch to 6.25V ±0.25V and 3.25V ±0.25V, respectively. |
| $V_{CC}$ | | **DEVICE POWER** for most operations (5V ±5% or ±10%). $V_{CC}$ also supplies the memory cell's margin voltage during the conventional program verify and erase verify modes. In these modes, $V_{CC}$ must switch to 6.25V ±0.25V and 3.25V ±0.25V, respectively. |
| GND | | **GROUND:** Reference for the device's circuitry. |
| N.C. | | **NO INTERNAL CONNECTION** to this device. Pin may be driven or left floating. |

**NOTE:**
*For complete discussion and explanation of the On-Board modes, refer to the On-Board device operation section.

# 28F256
# 256K (32K x 8) CMOS FLASH MEMORY

- ■ Flash Electrical Chip-Erase
  - — 1 Second Typical Chip-Erase
- ■ Quick-Pulse Programming™
  - — 100 μs Typical Byte-Program
  - — 4 Second Chip-Program
- ■ 12.0V or 12.75V V_PP Versions
  - — 12.0V V_PP
  - — 12.75V V_PP for Faster Typical Erase/Program Performance
- ■ 100 Erase/Program Cycles
- ■ High-Performance Speeds
  - — 170 ns Maximum Access Time
- ■ Low Power Consumption
  - — 100 μA Maximum Standby Current

- ■ Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- ■ Noise Immunity Features
  - — ±10% V_CC Tolerance
  - — Maximum Latch-Up Immunity through EPI Processing
- ■ ETOX™ Flash-Memory Technology
  - — EPROM-Compatible Process Base
  - — High-Volume Manufacturing Experience
- ■ Compatible with JEDEC-Standard Byte-Wide EPROM Pinouts
  - — 32-Pin Cerdip
  - — 32-Lead PLCC
  - (See Packaging Spec., Order #231369)

Intel's 28F256 CMOS flash-memory offers the most cost-effective and reliable alternative for updatable non-volatile memory. The 28F256 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be erased and reprogrammed: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F256 increases memory flexibility, while contributing to time- and cost-savings. The 28F256 is targeted for alterable code- or data-storage applications where traditional E2PROM functionality (byte-erasure) is either not required or not cost-effective. The 28F256 can also be applied where EPROM ultraviolet erasure is impractical or time-consuming.

The 28F256 is a 256-Kilobit non-volatile memory organized as 32768 bytes of 8 bits. Intel's 28F256 is offered in 32-pin Cerdip or 32-lead PLCC packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

The 28F256 is also available in 12.0V V_PP or 12.75V V_PP versions. The 12.0V version accommodates standard 12V power supplies, while the 12.75V version yields typical erase/program performance two times faster than the 12.0V version.

Intel's 28F256 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 170 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 mA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from −1V to V_CC + 1V.

With Intel's ETOX™ (EPROM tunnel oxide) process base, the 28F256 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.
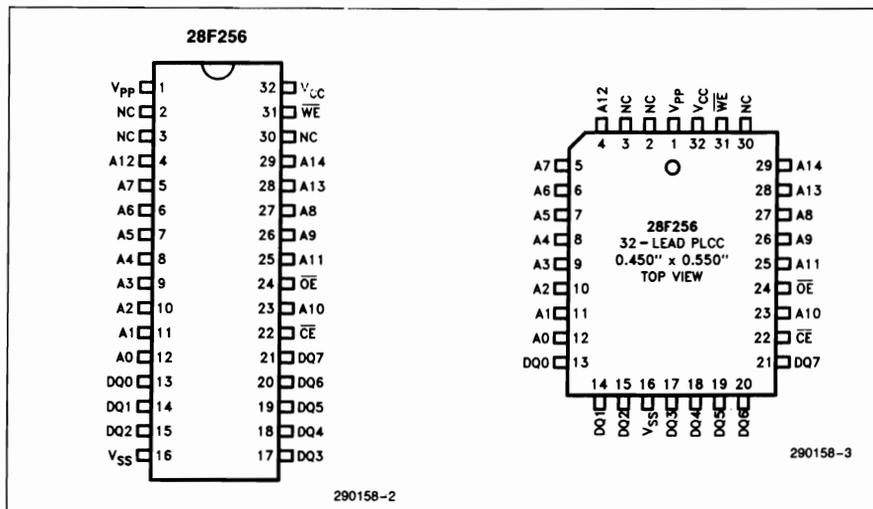
Figure 2. 28F256 Pin Configurations

Table 1. Pin Description

| Symbol | Type | Name and Function |
|---|---|---|
| $A_0$–$A_{14}$ | INPUT | **ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle. |
| $DQ_0$–$DQ_7$ | INPUT/OUTPUT | **DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle. |
| $\overline{CE}$ | INPUT | **CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels. |
| $\overline{OE}$ | INPUT | **OUTPUT ENABLE:** Gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low. |
| $\overline{WE}$ | INPUT | **WRITE ENABLE:** Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} = V_{PPL}$, memory contents cannot be altered. |
| $V_{PP}$ | | **ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array. |
| $V_{CC}$ | | **DEVICE POWER SUPPLY** (5V ±10%) |
| $V_{SS}$ | | **GROUND** |
| NC | | **NO INTERNAL CONNECTION** to device. Pin may be driven or left floating. |

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| 131,072 WORD x 8 BIT FLASH ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY SILICON STACKED GATE MOS | TC58F1000P/F/J-15 TC58F1000P/F/J-20 |
|---|---|

The TC58F1000P/F/J is a 1,048,576 bits, Flash Electrically Erasable and Programmable Read Only Memory (FEEPROM) organized as 131,072 words by 8 bits. The TC58F1000P/F/J is fabricated using Toshiba's advanced CMOS technology which provides the high speed and low power features, with access times of 150ns/200ns, an operating current of 30mA at 6.7 MHz and a standby current of 100μA.

The TC58F1000P/F/J features a command control mode and an EPROM compatible mode for programming and erasing. The command control mode is used for in-system programming controlled by the MPU tim-

ing. A specific software sequence must be executed to enable the program, program-verify, chip-erase, block-erase, erase-verify, signature read and mode reset operations. The EPROM compatible mode is used for programming and erasing with a conventional EPROM programmer. The programming time is 14-seconds and the erasing time is only 1-second. The TC58F1000P/F/J is also provided with a block-erase feature. The pro gramming time of 1 block (4K byte) is only 0.5-second.

The TC58F1000P/F/J has a JEDEC standard pinout configuration and is packaged in either a 32-pin plastic DIP, 32-pin flat package (SOP) or 32-pin SOJ.

- Access Time: 150ns/200ns
- Power dissipation
  Operating: 30mA
  Standby: 100μA
- Erase/Write endurance
  100 cycles
  10,000 cycles (Option)
- High-speed programming
  14 second/chip
  0.5 second/block

- Electrical erasing mode:
  Chip erase   1 second
  Block erase  1 second
  (Block size: 4K Byte x 32 blocks)
- Package options
  Suffix "P": 32-pin Plastic DIP
  Suffix "F": 32-pin Plastic flat package (SOP)
  Suffix "J": 32-pin Plastic SOJ
- Program Erase mode
  Command control mode
  EPROM Compatible mode

## PIN CONNECTION   (TOP VIEW)

```
        Vpp 1        32 Vcc
        A16 2        31 WE
        A15 3        30 N C
        A12 4        29 A14
         A7 5        28 A13
         A6 6        27 A8
         A5 7        26 A9
         A4 8        25 A11
         A3 9        24 OE
         A2 10       23 A10
         A1 11       22 CE
         A0 12       21 D7
         D0 13       20 D6
         D1 14       19 D5
         D2 15       18 D4
        GND 16       17 D3
```
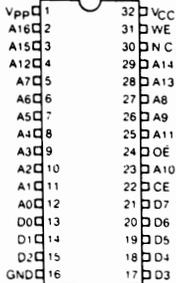
## PIN NAMES

| A0 ~ 16 | Address input |
|---|---|
| D0 ~ 7 | Data input/output |
| CE | Chip enable |
| OE | Output enable |
| WE | Write enable/EPROM mode switch |
| N C | No connection |
| Vpp | Program and erase power Supply |
| Vcc | Power Supply |
| GND | Ground |

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# ADC0800 8-Bit A/D Converter

## General Description

The ADC0800 is an 8-bit monolithic A/D converter using P-channel ion-implanted MOS technology. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown analog voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital outputs contain an 8-bit complementary binary word corresponding to the unknown. The binary output is TRI-STATE® to permit bussing on common data lines.

The ADC0800PD is specified over −55°C to +125°C and the ADC0800PCD is specified over 0°C to 70°C.

## Features

- Low cost
- ±5V, 10V input ranges
- No missing codes
- Ratiometric conversion
- TRI-STATE outputs
- Fast                                           $T_C = 50 \mu s$
- Contains output latches
- TTL compatible
- Supply voltages                    5 $V_{DC}$ and −12 $V_{DC}$
- Resolution                                           8 bits
- Linearity                                              ±1 LSB
- Conversion speed                        40 clock periods
- Clock range                                  50 to 800 kHz

## Block Diagram
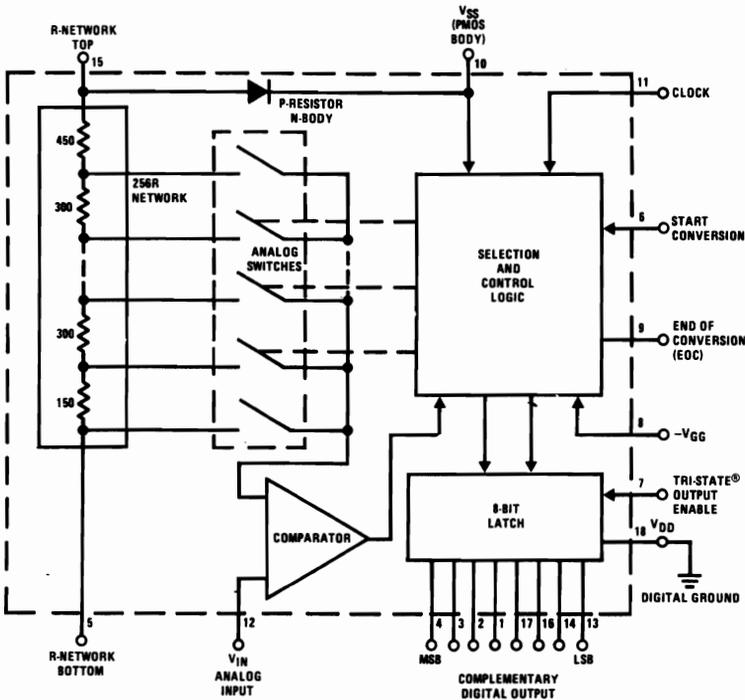


(00000000 = + full-scale)

TL/H/5670-1

# ADC0808, ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Multiplexer

## General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

## Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 $V_{DC}$ or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package

## Key Specifications

| | |
|---|---|
| ■ Resolution | 8 Bits |
| ■ Total Unadjusted Error | ± ½ LSB and ±1 LSB |
| ■ Single Supply | 5 $V_{DC}$ |
| ■ Low Power | 15 mW |
| ■ Conversion Time | 100 μs |

## Block Diagram
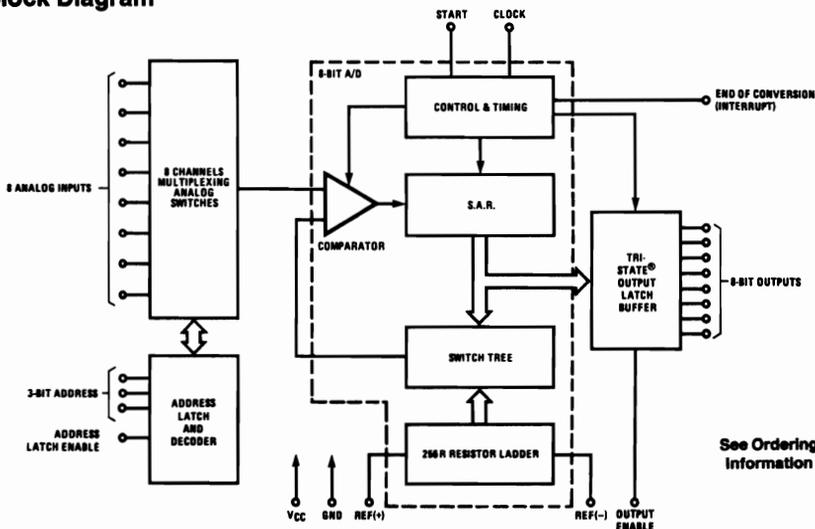


See Ordering Information

TL/H/5672-1

# ADC1210, ADC1211 12-Bit CMOS A/D Converters

## General Description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 $\mu$s typ, and can be connected to convert 10 bits in 30 $\mu$s.

Both devices are available in military and industrial temperature ranges.

## Features

- 12-bit resolution
- $\pm \frac{3}{4}$ LSB or $\pm 2$ LSB nonlinearity
- Single $+5$V to $\pm 15$V supply range
- 100 $\mu$s 12-bit, 30 $\mu$s 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 k$\Omega$ analog input impedance

## Block Diagram
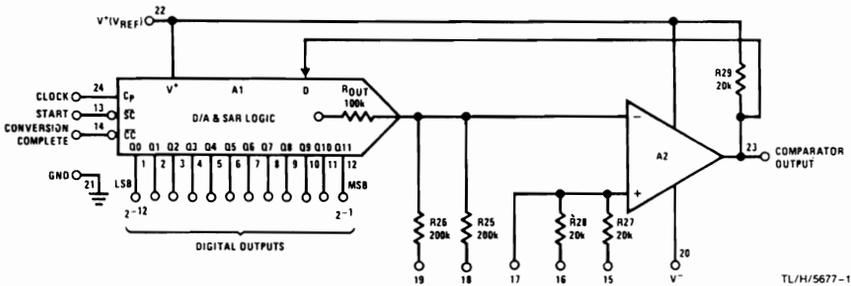


TL/H/5677-1

## Connection Diagram

**Dual-In-Line Package**
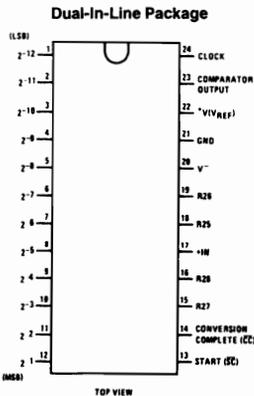


TOP VIEW          TL/H/5677-2

Order Number ADC1210HD,
ADC1210HCD, ADC1211HD,
ADC1211HCD
See NS Package D24D

# DAC0800/DAC0801/DAC0802 8-Bit Digital-to-Analog Converters

## General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ± 1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ± 0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, $V_{LC}$, grounded. Changing the $V_{LC}$ potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ± 4.5V to ± 18V power supply range; power dissipation is only 33 mW with ± 5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C are DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively.

## Features

- Fast settling output current ............ 100 ns
- Full scale error ............ ± 1 LSB
- Nonlinearity over temperature ............ ± 0.1%
- Full scale current drift ............ ± 10 ppm/°C
- High output compliance ............ −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range ............ ± 4.5V to ± 18V
- Low power consumption ............ 33 mW at ± 5V
- Low cost

## Typical Applications
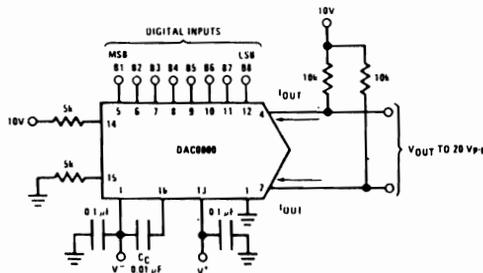


TL/H/5686–1

FIGURE 1. ± 20 $V_{p-p}$ Output Digital-to-Analog Converter (Note 4)

## Ordering Information

| Non-Linearity | Temperature Range | Order Numbers | | | | | |
|---|---|---|---|---|---|---|---|
| | | J Package (J16A)* | | N Package (N16A)* | | SO Package (M16A) | |
| ± 0.1% FS | 55°C ≤ $T_A$ ≤ +125°C | DAC0802LJ | DAC-08AQ | | | | |
| ± 0.1% FS | 0°C ≤ $T_A$ ≤ +70°C | DAC0802LCJ | DAC-08HQ | DAC0802LCN | DAC-08HP | DAC0802LCM | |
| ± 0.19% FS | 55°C ≤ $T_A$ ≤ +125°C | DAC0800LJ | DAC-08Q | | | | |
| ± 0.19% FS | 0°C ≤ $T_A$ ≤ +70°C | DAC0800LCJ | DAC-08EQ | DAC0800LCN | DAC-08EP | DAC0800LCM | |
| ± 0.39% FS | 0°C ≤ $T_A$ ≤ +70°C | DAC0801LCJ | DAC-08CQ | DAC0801LCN | DAC-08CP | DAC0801LCM | |

*Devices may be ordered by using either order number.

# DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

## General Description

The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current ($I_{REF}$) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}$/ 256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

## Features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

## Block and Connection Diagrams
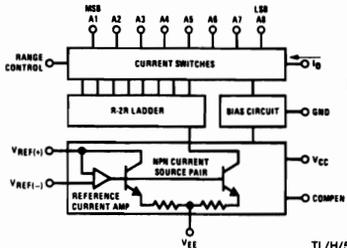


TL/H/5687–1

Order Number
DAC0808, DAC0807,
or DAC0806
See NS Package
Number J16A,
M16A or N16A

**Dual-In-Line Package**
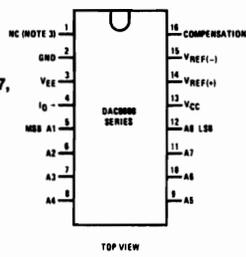


TOP VIEW                    TL/H/5687–2

**Small-Outline Package**
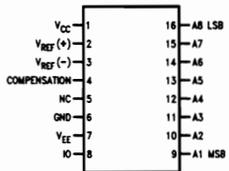


TL/H/5687–13

**Top View**

## Ordering Information

| ACCURACY | OPERATING TEMPERATURE RANGE | ORDER NUMBERS | | | |
|---|---|---|---|---|---|
| | | J PACKAGE (J16A)* | | N PACKAGE (N16A)* | SO PACKAGE (M16A) |
| 8-bit | −55°C ≤ $T_A$ ≤ +125°C | DAC0808LJ | MC1508L8 | | | |
| 8-bit | 0°C ≤ $T_A$ ≤ +75°C | DAC0808LCJ | MC1408L8 | DAC0808LCN | MC1408P8 | DAC0808LCM |
| 7-bit | 0°C ≤ $T_A$ ≤ +75°C | DAC0807LCJ | MC1408L7 | DAC0807LCN | MC1408P7 | DAC0807LCM |
| 6-bit | 0°C ≤ $T_A$ ≤ +75°C | DAC0806LCJ | MC1408L6 | DAC0806LCN | MC1408P6 | DAC0806LCM |

*Note. Devices may be ordered by using either order number.

# MICRO-DAC™ DAC1208, DAC1209, DAC1210, DAC1230, DAC1231, DAC1232 12-Bit, μP Compatible, Double-Buffered D to A Converters

## General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between $I_{OUT1}$ and $I_{OUT2}$ maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

The DAC1208 series and DAC1230 series are the 12-bit members of a family of microprocessor compatible DACs (MICRO-DACs™). For applications requiring other resolutions, the DAC1000 series for 10-bit and DAC0830 series for 8-bit are available alternatives.

## Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without μP) if desired
- All parts guaranteed 12-bit monotonic
- DAC1230 series is pin compatible with the DAC0830 series 8-bit MICRO-DACs

## Key Specifications

- Current Settling Time      1 μs
- Resolution      12 Bits
- Linearity (Guaranteed over temperature)      10, 11, or 12 Bits of FS
- Gain Tempco      1.3 ppm/°C
- Low Power Dissipation      20 mW
- Single Power Supply      5 $V_{DC}$ to 15 $V_{DC}$

## Typical Application
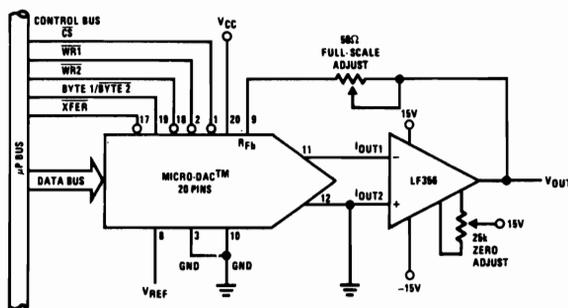


TL/H/5690–1

# 12-Bit Ultrahigh-Speed Monolithic D/A Converter

## AD568

## FEATURES
**Ultrahigh Speed: Current Settling to 1LSB in 35ns**
**High Stability Buried Zener Reference on Chip**
**Monotonicity Guaranteed over Temperature**
**10.24mA Full-Scale Output Suitable for Video
  Applications**
**Integral and Differential Linearity Guaranteed Over
  Temperature**
**0.3" "Skinny DIP" Packaging**
**Variable Threshold Allows TTL and CMOS
  Interface**

## PRODUCT DESCRIPTION
The AD568 is an ultrahigh-speed, 12-bit digital-to-analog converter (DAC) settling to 0.025% in 35ns. The monolithic device is fabricated using Analog Devices' Complementary Bipolar (CB) Process. This is a proprietary process featuring high-speed NPN and PNP devices on the same chip without the use of dielectric isolation or multichip hybrid techniques. The high speed of the AD568 is maintained by keeping impedance levels low enough to minimize the effects of parasitic circuit capacitances.

The DAC consists of 16 current sources configured to deliver a 10.24mA full-scale current. Multiple matched current sources and thin-film ladder techniques are combined to produce bit weighting. The DAC's output is a 10.24mA full scale (FS) for current output applications or a 1.024V FS unbuffered voltage output. Additionally, a 10.24V FS buffered output may be generated using an onboard 1kΩ span resistor with an external op amp. Bipolar ranges are accomplished by pin strapping.

Laser wafer trimming insures full 12-bit linearity. All grades of the AD568 are guaranteed monotonic over their full operating temperature range. Furthermore, the output resistance of the DAC is trimmed to 100Ω ±1.0%. The gain temperature coefficient of the voltage output is 30ppm/°C max (K).

The AD568 is available in three performance grades. The AD568JQ and KQ are available in 24-pin cerdip (0.3") packages and are specified for operation from 0 to +70°C. The AD568SQ features operation from −55°C to +125°C and is also packaged in the hermetic 0.3" cerdip.
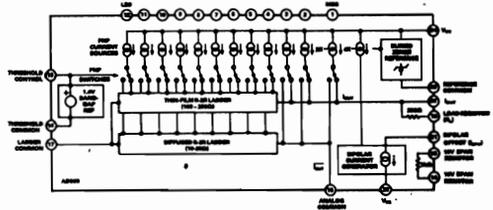
## PRODUCT HIGHLIGHTS
1. The ultrafast settling time of the AD568 allows leading edge performance in waveform generation, graphics display and high-speed A/D conversion applications.
2. Pin strapping provides a variety of voltage and current output ranges for application versatility. Tight control of the absolute output current reduces trim requirements in externally-scaled applications.
3. Matched on-chip resistors can be used for precision scaling in high-speed A/D conversion circuits.
4. The digital inputs are compatible with TTL and +5V CMOS logic families.
5. Skinny DIP (0.3") packaging minimizes board space requirements and eases layout considerations.

Analog Devices

623

# Monolithic
# 12-Bit Quad DAC
# AD664

## FEATURES
**Four Complete Voltage Output DACs**
**Data Register Readback Feature**
**"Reset to Zero" Override**
**Multiplying Operation**
**Double-Buffered Latches**
**PLCC, LCC and DIP Packages**

## APPLICATIONS
**Automatic Test Equipment**
**Robotics**
**Process Control**
**Disk Drives**
**Instrumentation**

## PRODUCT DESCRIPTION

The AD664 is four complete 12 bit, voltage-output DACs on one monolithic IC chip. Each DAC has a double buffered input latch structure and a latch data readback function. All DAC read and write operations occur through a single microprocessor-compatible I/O port.

The I/O port accomodates 4-, 8- and 12-bit parallel words allowing simple interfacing with a wide variety of microprocessors. A reset to zero control pin is provided to allow a user to simultaneously reset all DAC outputs to zero, regardless of the contents of the input latch. Any one or all of the DACs may be placed in a transparent mode allowing immediate response of the outputs to the input data.

The analog portion of the AD664 consists of four DAC cells, four output amplifiers, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the on-board application resistors and output amplifier. The output range of each DAC cell is programmed through the digital I/O port and may be set to unipolar or bipolar range, 0 to 10 volts or −10 to +10 volts respectively. All DACs are operated from a single external reference.

The functional completeness of the AD664 results from the combination of Analog Devices' BIMOS II process, laser-trimmed thin-film resistors and double-level metal interconnects.

## PRODUCT HIGHLIGHTS

1. The AD664 provides four voltage-output DACs on one chip offering the highest density 12-bit D/A function available.

2. The output range of each DAC is fully and independently programmable.

3. Readback capability allows verification of contents of internal data registers.

4. The asynchronous RESET control returns all D/A outputs to zero volts.

## AD664 FUNCTIONAL BLOCK DIAGRAMS
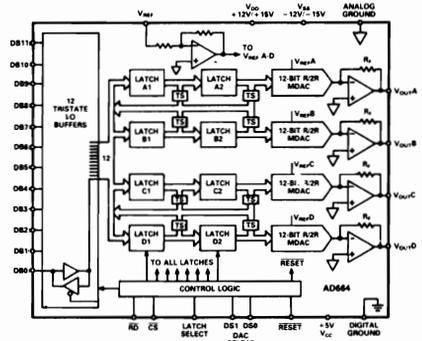


*28-Pin Block Diagram*
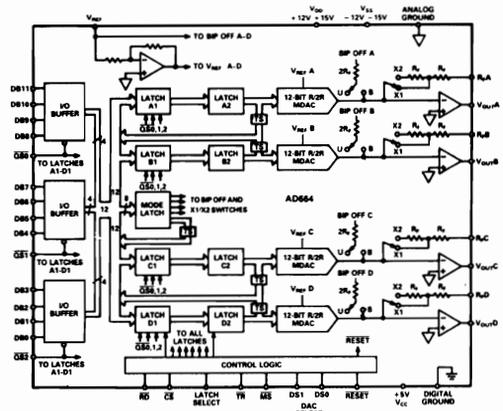


*44-Pin Block Diagram*

5. DAC-to-DAC matching performance is specified and tested.

6. Linearity error is specified to be 1/2LSB at room temperature and 1LSB maximum.

7. DAC performance is guaranteed to be monotonic over the full operating temperature range.

8. Readback outputs have tristate outputs.

9. Multiplying-mode operation allows use with fixed or variable external references.

# Complete
# 12-Bit A/D Converter

## AD674A*

### FEATURES
Complete 12-Bit A/D Converter with Reference
and Clock
Faster Version of AD574A
8- and 16-Bit Bus Interface
No Missing Codes Over Temperature
15μs max Conversion Time
±12V and ±15V Operation
Unipolar and Bipolar Inputs
DIP Package

### AD674A FUNCTIONAL BLOCK DIAGRAM
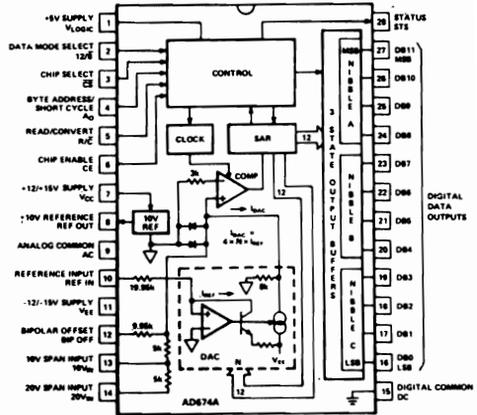


### PRODUCT DESCRIPTION
The AD674A is a complete 12-bit successive-approximation
analog-to-digital converter with three-state output buffer circuitry
for direct interface to an 8- and 16-bit microprocessor bus. A
high-precision voltage reference and clock are included on-chip,
and the circuit requires only power supplies and control signals
for operation.

The AD674A is pin compatible with the industry-standard
AD574A but offers faster conversion time and bus-access speed.

The AD674A design is implemented with two LSI chips each
containing both analog and digital circuitry, resulting in the
maximum performance and flexibility at the lowest cost. The
chips are laser trimmed at the wafer stage to obtain full rated
performance without external trims.

The AD674A is available in six different grades. The AD674AJ,
K, and L grades are specified for operation over the 0 to +70°C
temperature range. The AD674AS, T, and U are specified for
the −55°C to +125°C range. All grades are available in a 28-pin
hermetically sealed ceramic DIP.

The S, T, and U grades are also available with optional processing
to MIL-STD-883C Class B in 28-pin DIP. The Analog Devices
Military Products Databook should be consulted for details on
/883B testing of the AD674A.

*Protected by U.S. Patent Nos. 3,803,590; 4,213,806; 4,511,413;
RE 28,633.

### PRODUCT HIGHLIGHTS
1. The AD674A interfaces to most 8- or 16-bit microprocessors.
   Multiple-mode three-state output buffers connect directly to
   the data bus while the read and convert commands are taken
   from the control bus. The 12 bits of output data can be read
   either as one 12-bit word or as two 8-bit bytes (one with 8
   data bits, the other with 4 data bits and 4 trailing zeros).

2. The precision, laser-trimmed scaling and bipolar offset resistors
   provide four calibrated ranges: 0 to +10 and 0 to +20 volts
   unipolar, −5 to +5 and −10 to +10 volts bipolar. Typical
   bipolar offset and full-scale calibration errors of ±0.1% can
   be trimmed to zero with one external component each.

3. The internal buried zener reference is trimmed to 10.00 volts
   with 1% maximum error and 15ppm/°C typical T.C. The
   reference is available externally and can drive up to 2.0mA
   beyond the requirements of the reference and bipolar offset
   resistors.

# Complete High-Speed
# 16-Bit A/D Converter

## AD1376

### FEATURES
Complete 16-Bit Converter With Reference
  and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits Over Temperature
Fast Conversion – 14μs (14 Bit)
Short Cycle Capability
Parallel and Serial Outputs
Low Power: 645mW Typical
Industry Standard Pin Out

**AD1376 FUNCTIONAL BLOCK DIAGRAM**
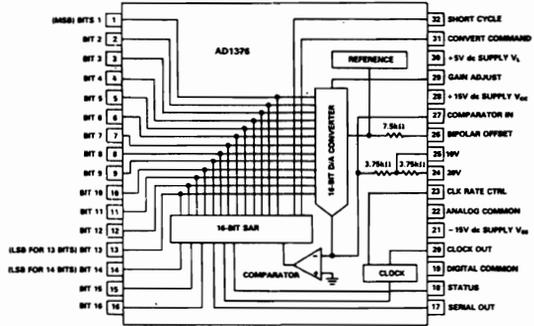


### PRODUCT DESCRIPTION
The AD1376 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin, pin-stake DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR, and maximum 14-bit conversion time of 15μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD1376 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

### APPLICATIONS
The AD1376 is excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

### PRODUCT HIGHLIGHTS
1. The AD1376 provides 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J grade) at 25°C.

2. Conversion time is 14μs typical to 14 bits with short cycle capability, and 16μs to 16 bits.

3. Two binary codes are available on the AD1376 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary twos complement (CTC) coding may be obtained by inverting Pin 1 (MSB).

4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

5. The AD1376 includes an internal reference and clock, with external clock adjust pin, and a serial output.

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# Monolithic 8-Bit
# Video A/D Converter

# AD9048

## FEATURES
**8-Bits; 20MSPS Minimum Word Rates**
**420mW Power Dissipation**
**No T/H Required**
**17pF Input Capacitance**
**Industry Standard Pinouts**

## PRODUCT DESCRIPTION
The AD9048 is an 8-bit, 20MSPS flash converter which is pin-for-pin compatible with the TDC1048 unit but offers enhancements over its predecessor. Significantly improved output driver stages and reduced power make the AD9048 attractive for system designs.

Full power bandwidth is 7MHz minimum, making it an ideal choice for doing real-time conversion of video signals, where analog frequency information of interest is seldom higher than 4MHz-5MHz.

Clocked latching comparators, encoding logic, and an output buffer register operating at minimum rates of 20MSPS make it unnecessary to incorporate a sample-and-hold (S/H) or track-and-hold (T/H) into designs using the AD9048. All digital control inputs and outputs are TTL compatible.

Devices which operate over two case temperature ranges and with two grades of linearity are available. Linearities of 0.5LSB or 0.75LSB can be ordered for a commercial range of 0 to +70°C, or extended temperatures of −55°C to +125°C . Units are packaged in 28-pin ceramic DIPs and are also available as LCC packages.

## AD9048 FUNCTIONAL BLOCK DIAGRAM
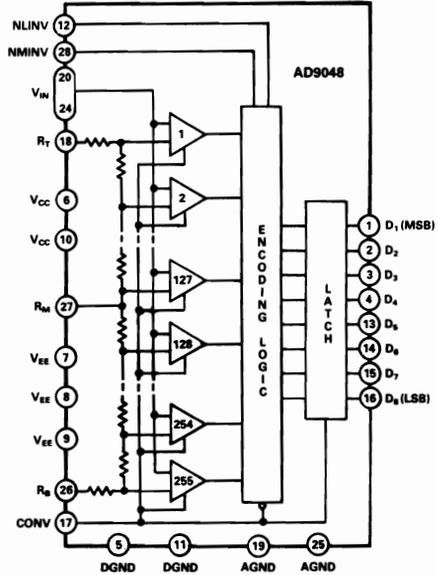


## OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

### 28-Pin Cerdip Package
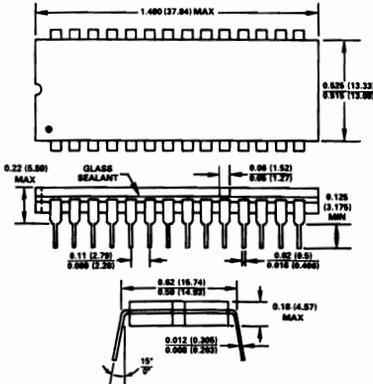


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

### 28-Pin Ceramic Leadless Chip Carrier (LCC)
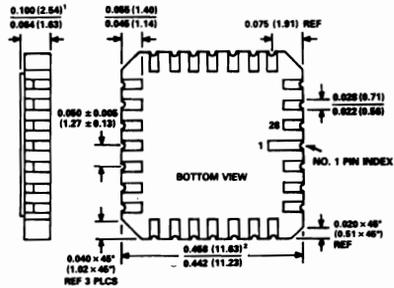


NOTES
[1] THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
[2] APPLIES TO ALL FOUR SIDES.
ALL TERMINALS ARE GOLD PLATED.

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# Interface Circuits

## LM311 voltage comparator

### general description

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

### features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C.

## schematic diagram and auxiliary circuits
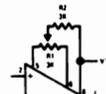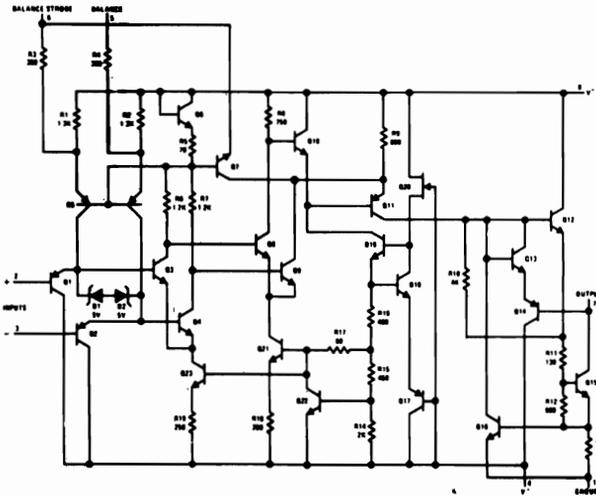


Offset Balancing
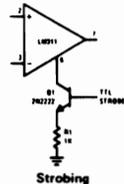
Strobing
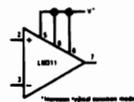
Increasing Input Stage Current*

## connection diagrams *



Metal Can

Flat Package

Dual-In-Line Package

Dual-In-Line Package

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

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8-35

BI-FET II™ Technology
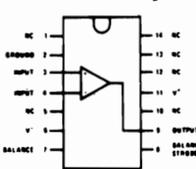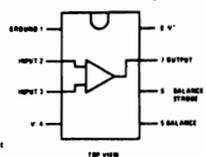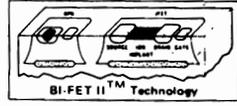
# LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

## General Description

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

## Features

- Internally trimmed offset voltage                        10 mV
- Low input bias current                                    50pA
- Low input noise voltage                            $16 \text{ nV}/\sqrt{\text{Hz}}$
- Low input noise current                          $0.01 \text{ pA}/\sqrt{\text{Hz}}$
- Wide gain bandwidth                                       4 MHz
- High slew rate                                        $13 \text{ V}/\mu\text{s}$
- Low supply current                                       3.6 mA
- High input impedance                                  $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$,              $<0.02\%$
  $RL = 10k, V_O = 20Vp-p, BW = 20 \text{ Hz-20 kHz}$
- Low 1/f noise corner                                      50 Hz
- Fast settling time to 0.01%                            $2 \mu\text{s}$

## Typical Connection



## Simplified Schematic



1/2 Dual
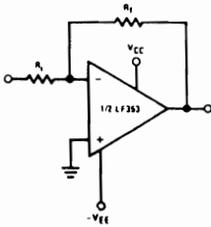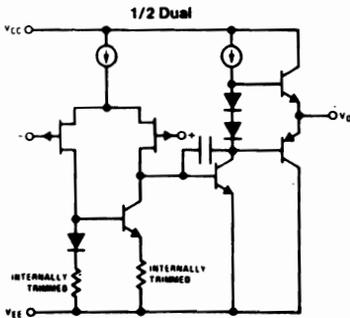
## Connection Diagrams

**Metal Can Package** (Top View)
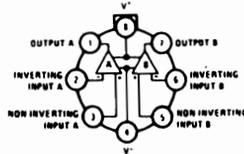


Order Number LF353H
See NS Package Number H08C

**Dual-In-Line Package** (Top View)
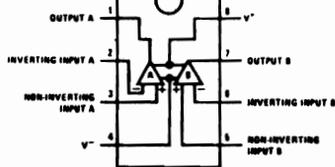


Order Number LF353J, LF353M or LF353N
See NS Package Number J08A, M08A or N08E

TL/H/5649-1

# LM363 Precision Instrumentation Amplifier

## General Description

The LM363 is a monolithic true instrumentation amplifier. It requires no external parts for fixed gains of 10, 100 and 1000. High precision is attained by on-chip trimming of offset voltage and gain. A super-beta biopolar input stage gives very low input bias current and voltage noise, extremely low offset voltage drift, and high common-mode rejection ratio. A new two-stage amplifier design yields an open loop gain of 10,000,000 and a gain bandwidth product of 30 MHz, yet remains stable for all closed loop gains. The LM363 operates with supply voltages from ±5V to ±18V with only 1.5 mA current drain.

The LM363's low voltage noise, low offset voltage and offset voltage drift make it ideal for amplifying low-level, low-impedance transducers. At the same time, its low bias current and high input impedance (both common-mode and differential) provide excellent performance at high impedance levels. These features, along with its ultra-high common-mode rejection, allow the LM363 to be used in the most demanding instrumentation amplifier applications, replacing expensive hybrid, module or multi-chip designs. Because the LM363 is internally trimmed, precision external resistors and their associated errors are eliminated.

The 16-pin dual-in-line package provides pin-strappable gains of 10, 100 or 1000. Its twin differential shield drivers eliminate bandwidth loss due to cable capacitance. Compensation pins allow overcompensation to reduce bandwidth and output noise, or to provide greater stability with capacitive loads. Separate output force, sense and reference pins permit gains between 10 and 10,000 to be programmed using external resistors.

On the 8-pin TO-5 package, gain is internally set at 10, 100 or 500 but may be increased with external resistors. The shield driver and offset adjust pins are omitted on the 8-pin versions.

The LM363 is rated for 0°C to 70°C.

## Features

- Offset and gain pretrimmed
- 12 nV/$\sqrt{Hz}$ input noise (G = 500/1000)
- 130 dB CMRR typical (G = 500/1000)
- 2 nA bias current typical
- No external parts required
- Dual shield drivers
- Available at 0.5 $\mu$V/°C maximum drift
- Can be used as a high performance op amp
- Low supply current (1.5 mA typ)

## Typical Connections

### 8-Pin Package



TL/H/5609-1

### 16-Pin Package

G = 10   2, 3, 4, open
G = 100  3–4 shorted
G = 1000 2–4 shorted
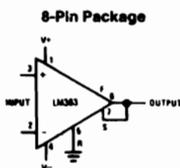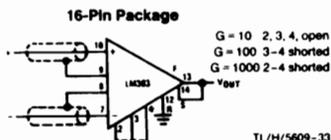


TL/H/5609-33

## Connection Diagrams

### Metal Can Package



TOP VIEW
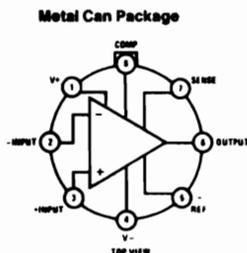
Order Number LM363H-10,
LM363H-100 or LM363H-500
See NS Package Number H08C

### 16-Pin Dual-In-Line Package



TOP VIEW
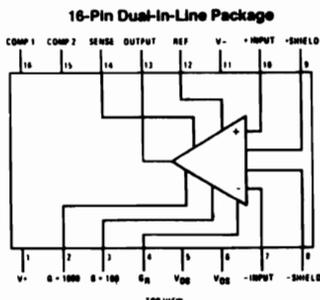
TL/H/5609-2

Order Number 363D
See NS Package Number D16C

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# LM565/LM565C Phase Locked Loop

## General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10 1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication

The LM565H is specified for operation over the −55°C to +125°C military temperature range The LM565CH and LM565CN are specified for operation over the 0°C to +70°C temperature range

## Features

- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output

- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ·1°₀ to ·60°₀

## Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

## Connection Diagrams

**Metal Can Package**
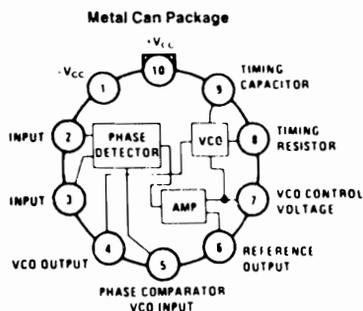


TL/H/7853-2

**Order Number LM565H or LM565CH
See NS Package Number H10C**

**Dual-In-Line Package**
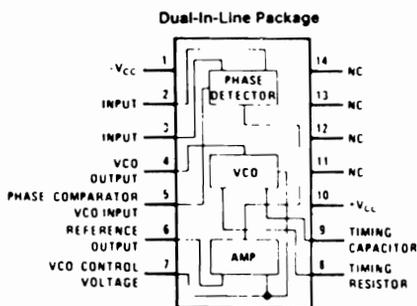


TL/H/7853-3

**Order Number LM565CN
See NS Package Number N14A**

# Interface Circuits

## LM710 voltage comparator

### general description

The LM710 is a high-speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in

saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710 is useful as a pulse height discriminator, a voltage comparator in high-speed A/D converters or a go, no-go detector in automatic test equipment. It also has applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the unit suggests it for applications replacing relatively simple discrete component circuitry

## schematic* and connection diagrams
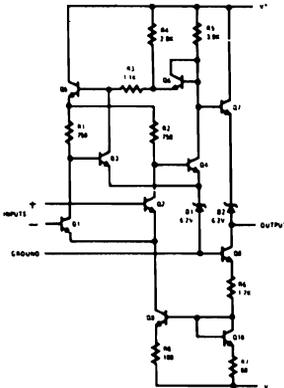


Metal Can Package
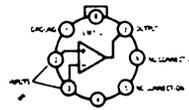
## typical applications*

Schmidt Trigger
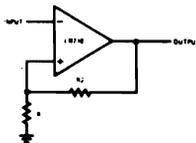


Pulse Width Modulator
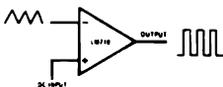


Line Receiver With
Increased Output
Sink Current
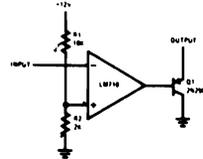


Level Detector With
Lamp Driver
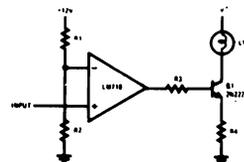


*Pin connections shown are for metal can.

# Interface Circuits

## LM711 dual comparator

### general description

The LM711 contains two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. Similar to the LM710, the device features low offset and thermal drift, a large input voltage range, low power consumption, fast recovery from large overloads and compatibility with most integrated logic circuits.

With the addition of an external resistor network, the LM711 can be used as a sense amplifier for core memories. The input thresholding, combined with the high gain of the comparator, eliminates many of the inaccuracies encountered with con

ventional sense amplifier designs. Further, it has the speed and accuracy needed for reliably detecting the outputs of cores as small as 20 mils.

The LM711 is also useful in other applications where a dual comparator with OR'ed outputs is required, such as a double-ended limit detector. By using common circuitry for both halves, the device can provide high speed with lower power dissipation than two single comparators. The LM711 is available in either an 10-lead low profile TO-5 header or a 1.4" by 1.4" metal flat package.

## schematic and connection diagrams
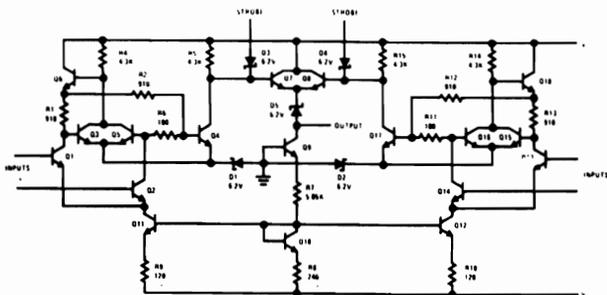


Metal Can Package
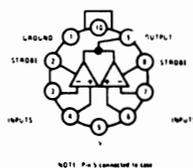
## typical applications

Sense Amplifier With Supply Strobing
for Reduced Power Consumption*



*Standby dissipation is about 40 mW.
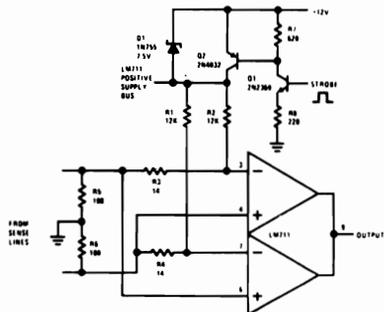
Double-Ended Limit Detector
With Lamp Driver
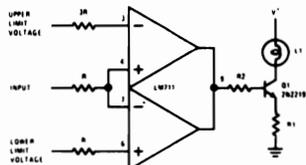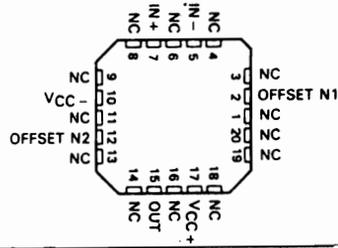
**GENERAL DESCRIPTION** — The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Supply Voltage | |
| Military (741) | ±22 V |
| Commercial (741C) | ±18 V |
| Internal Power Dissipation (Note 1) | |
| Metal Can | 500 mW |
| DIP | 670 mW |
| Mini DIP | 310 mW |
| Flatpak | 570 mW |
| Differential Input Voltage | ±30 V |
| Input Voltage (Note 2) | ±15 V |
| Storage Temperature Range | |
| Metal Can, DIP, and Flatpak | −65°C to +150°C |
| Mini DIP | −55°C to +125°C |
| Operating Temperature Range | |
| Military (741) | −55°C to +125°C |
| Commercial (741C) | 0°C to +70°C |
| Lead Temperature (Soldering) | |
| Metal Can, DIP, and Flatpak (60 seconds) | 300°C |
| Mini DIP (10 seconds) | 260°C |
| Output Short Circuit Duration (Note 3) | Indefinite |

**CONNECTION DIAGRAMS**

**8-LEAD METAL CAN**
(TOP VIEW)
PACKAGE OUTLINE 5B
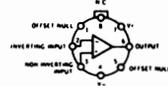
Note: Pin 4 connected to case

ORDER INFORMATION

| TYPE | PART NO. |
|---|---|
| 741 | 741HM |
| 741C | 741HC |

**14-LEAD DIP**
(TOP VIEW)
PACKAGE OUTLINE 6A
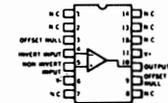
ORDER INFORMATION

| TYPE | PART NO. |
|---|---|
| 741 | 741DM |
| 741C | 741DC |

**10-LEAD FLATPAK**
(TOP VIEW)
PACKAGE OUTLINE 3F
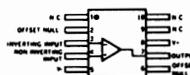
ORDER INFORMATION

| TYPE | PART NO. |
|---|---|
| 741 | 741FM |

**8-LEAD MINIDIP**
(TOP VIEW)
PACKAGE OUTLINE 9T

ORDER INFORMATION

| TYPE | PART NO. |
|---|---|
| 741C | 741TC |

**EQUIVALENT CIRCUIT**



Notes on following pages.

**FIGURE 9.47** Manufacturer's specification sheets for the Fairchild μA741 (Courtesy of Fairchild Semiconductor)

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# µA747
# DUAL FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER
## FAIRCHILD LINEAR INTEGRATED CIRCUITS

**GENERAL DESCRIPTION** — The µA747 is a pair of high performance monolithic Operational Amplifiers constructed using the Fairchild Planer* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the µA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The µA747 is short-circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see µA741 data sheet.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

## ABSOLUTE MAXIMUM RATINGS
Supply Voltage
| | |
|---|---|
| Military (747) | ±22 V |
| Commercial (747C) | ±18 V |

Internal Power Dissipation (Note 1)
| | |
|---|---|
| Metal Can | 500 mW |
| DIP | 670 mW |
| Differential Input Voltage | ±30 V |
| Input Voltage (Note 2) | ±15 V |
| Voltage between Offset Null and V_ | ±0.5 V |
| Storage Temperature Range | −65°C to +150°C |

Operating Temperature Range
| | |
|---|---|
| Military (747) | −55° C to +125°C |
| Commercial (747C) | 0°C to 70°C |
| Lead Temperature (Soldering, 60 seconds) | 300°C |
| Output Short-Circuit Duration (Note 3) | Indefinite |

### EQUIVALENT CIRCUIT (Each Side)

### CONNECTION DIAGRAMS
**14-LEAD DIP (TOP VIEW)**
PACKAGE OUTLINE 7A
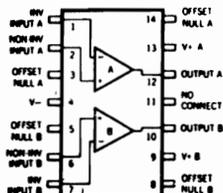


### ORDER INFORMATION
| TYPE | PART NO. |
|---|---|
| 747 | 747DM |
| 747C | 747DC |

### 10-LEAD METAL CAN (TOP VIEW)
PACKAGE OUTLINE 5F
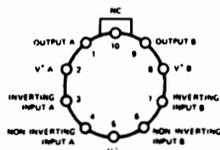


### ORDER INFORMATION
| TYPE | PART NO. |
|---|---|
| 747 | 747HM |
| 747C | 747HC |

Mini-DIP
CA3130E
CA3130AE

H-1817

All Types
8-LEAD TO-5
with Dual-In-Line
Formed Leads
(S suffix)
H-1787

All Types
8-LEAD TO-5
(T suffix)
H-1526
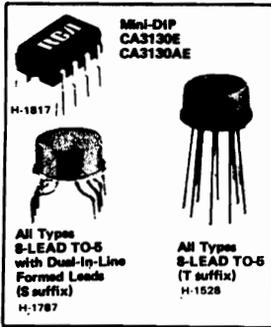
# BiMOS
# Operational Amplifiers

## With MOS/FET Input/ COS/MOS Output

**FEATURES:**
- *MOS/FET input stage provides:*
  *very high $Z_I$ = 1.5 $T\Omega$ (1.5 × $10^{12}\Omega$) typ.*
  *very low $I_I$ = 5 pA typ. at 15-V operation*
  *2 pA typ. at 5-V operation*
- *Common-mode input-voltage range includes*
  *negative supply rail; input terminals can*     *Ideal for*
  *be swung 0.5 V below negative supply rail*     *single-supply*
- *COS/MOS output stage permits signal swing*     *applications*
  *to either (or both) supply rails*

RCA-CA3130T, CA3130E, CA3130S, CA-3130AT, CA 3130AS, CA3130AE, CA3130BT, and CA3130BS are integrated-circuit operational amplifiers that combine the advantages of both COS/MOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3130 is available in chip form (H suffix). The CA3130 and CA3130A are also available in the Mini-DIP 8-lead dual-in-line plastic

- *Low $V_{IO}$: 2 mV max. (CA3130B)*
- *Wide BW: 15 MHz typ. (unity-gain crossover)*
- *High SR: 10 V/μs typ. (unity-gain follower)*
- *High output current ($I_O$): 20 mA typ.*
- *High $A_{OL}$: 320,000 (110 dB) typ.*
- *Compensation with single external capacitor*

**APPLICATIONS:**
- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *High-input-impedance comparators*
  *(Ideal interface with digital COS/MOS)*
- *High-input-impedance wideband amplifiers*
- *Voltage followers*
  *(e.g., follower for single-supply D/A*
  *converter)*
- *Voltage regulators*
  *(permits control of output voltage*
  *down to zero volts)*
- *Peak detectors*
- *Single-supply full-wave precision rectifiers*
- *Photo-diode sensor amplifiers*

package (E suffix). All types operate over the full military-temperature range of -55°C to +125°C. The CA3130B is intended for applications requiring premium-grade specifications. The CA3130A offers superior input characteristics over those of the CA3130.



PHASE COMPENSATION   TAB   STROBE
OFFSET NULL   V+
INV INPUT   OUTPUT
NON-INV INPUT   OFFSET NULL
V- AND CASE

TOP VIEW
**S and T Suffixes**

OFFSET NULL   STROBE
INV INPUT   V+
NON-INV INPUT   OUTPUT
V-   OFFSET NULL

TOP VIEW
**E Suffix**
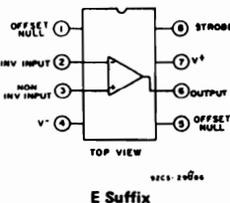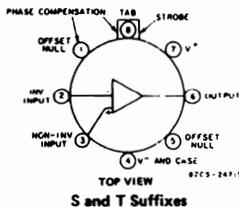
*Fig.1 — Functional diagrams for the CA3130 series.*

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### CA3140, CA3140A, CA3140B Types

# BiMOS Operational Amplifiers

Mini-DIP
CA3140E
CA3140AE

H-1817

All Types
8-Lead TO-5
With Dual-In-Line
Formed Leads
"DIL-CAN"
(S Suffix)

H-1787

All Types
8-Lead TO-5
(T Suffix)

H-1528

With MOS/FET Input/Bipolar Output

## FEATURES:

■ MOS/FET Input Stage
  (a) *Very high input impedance ($Z_{IN}$) — 1.5 TΩ typ.*
  (b) *Very low input current ($I_I$) — 10 pA typ. at ± 15 V*
  (c) *Low input-offset voltage ($V_{IO}$) — to 2 mV max.*
  (d) *Wide common-mode input-voltage range ($V_{ICR}$)—*
      *can be swung 0.5 volt below negative supply-voltage*
      *rail*
  (e) *Output swing complements input common-mode range*
  (f) *Rugged input stage — bipolar diode protected*

The CA3140B, CA3140A, and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 COS/MOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

The CA3140, CA3140A, and CA3140 BiMOS operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140B operates at supply voltages from 4 to 44 volts; the CA3140A and CA3140 from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower mode and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead dual-in-line

■ Directly replaces industry type 741 in most applications
■ Includes numerous industry operational
  amplifier categories such as general-pur-
  pose, FET input, wideband (high slew rate)
■ Operation from 4-to-44 volts
  Single or Dual supplies
■ Internally compensated
■ Characterized for ± 15-volt operation
  and for TTL supply systems with
  operation down to 4 volts
■ Wide bandwidth — 4.5 MHz unity
  gain at ± 15 V or 30 V; 3.7 MHz at 5 V
■ High voltage-follower slew rate — 9 V/μs
■ Fast setting time — 1.4 μs typ.
  to 10 mV with a 10-$V_{p-p}$ signal
■ Output swings to within 0.2 volt
  of negative supply
■ Strobable output stage

## APPLICATIONS:

■ Ground-referenced single-supply amplifiers
  in automobile and portable instrumentation
■ Sample and hold amplifiers
■ Long-duration timers/multivibrators
  (microseconds—minutes—hours)
■ Photocurrent instrumentation
■ Peak detectors        ■ Active filters
■ Comparators
■ Interface in 5 V TTL systems & other
  low-supply voltage systems
■ All standard operational amplifier applications
■ Function generators    ■ Tone controls
■ Power supplies        ■ Portable instruments
■ Intrusion alarm systems

TOP VIEW
S and T Suffixes
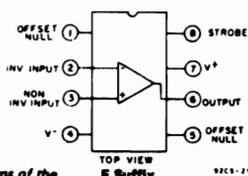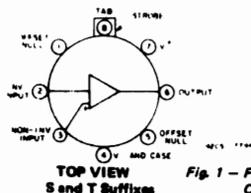
Fig. 1 — Functional diagrams of the
CA3140 series.

TOP VIEW
E Suffix

## MM5387AA, MM53108 digital alarm clocks

### general description

The MM5387AA, MM53108 digital alarm clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. They provide all the logic required to build several types of clocks and timers with up to four display modes (time, seconds, alarm and sleep) to maximize circuit utility, but are specifically intended for clock-radio applications. Both devices will directly-drive 7-segment LED displays in either a 12 hour format (3½ digits) with lead-zero blanking, AM/PM indication and flashing colon, or 24 hour format (4 digits) through hard-wire pin selection; the timekeeping function operates from either a 50 or 60 Hz input, also through pin selection. Outputs consist of display drivers, sleep (e.g., timed radio turn-off), and alarm enable. A power fail indication mode is provided to inform the user of incorrect time display by flashing all "ON" digits at a 1 Hz rate, and is cancelled by simply resetting time. The device operates over a supply range of 24–26V which does not require regulation.

The MM53108 is electrically identical to the MM5387AA, but with mirror-image pin-out to facilitate PC board layout when designing a "module" where the LED display and MOS chip are mounted on the same side; the MM5387AA is more suited for "L" shaped module designs (vertical LED display, horizontal component board). Both devices are supplied in a 40-lead dual-in-line package.

### features

- 50 or 60 Hz operation
- Single power supply
- 12 or 24 hour display format
- AM/PM outputs } 12 hour format
- Leading-zero blanking }
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Elimination of illegal time display at turn "ON"
- Direct interface to LED displays
- 9-minute snooze alarm
- Presettable 59-minute sleep timer
- Available in standard (MM5387AA) or mirror image (MM53108) pin-out

### applications

- Alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

### block diagram
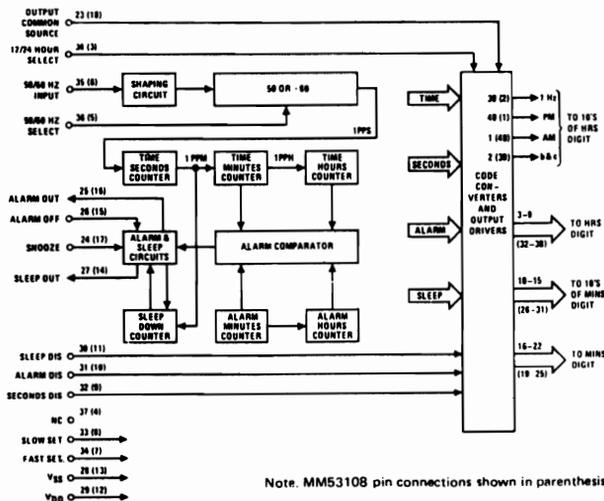


Note. MM53108 pin connections shown in parenthesis

FIGURE 1

## functional description

A block diagram of the MM5387AA, MM53108 digital clock radio circuit is shown in *Figure 1*. The various display setting modes are listed in Table I, and Table II shows the setting control functions. The following description is based on *Figure 1* and refers to both devices as they are electrically identical.

**50 or 60 Hz Input:** A shaping circuit *(Figure 3)* is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 6V o hysteresis. A simple RC filter such as shown in *Figure 7* should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

**50 or 60 Hz Select Input:** A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz time base. This counter is programmed to divide by 60 simply by leaving 50/60 Hz select unconnected; pull-down to $V_{DD}$ is provided by an internal depletion load. Operation at 50 Hz is programmed by connecting 50/60 Hz select to $V_{SS}$

**Display Mode Select Inputs:** In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal depletion pull-down devices allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table I. Alternate display modes are selected by applying $V_{SS}$ to the appropriate pin. As shown in *Figure 1* the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

**Time Setting Inputs:** Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal depletion pull-down devices are provided; application of $V_{SS}$ to these pins affects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, by selecting seconds display and actuating both slow and fast set inputs.

**Output Common Source Connection:** All display output drivers are open-drain devices with all sources common *(Figure 4a)*. The common source pin should be connected to $V_{SS}$.

**12 or 24 Hour Select Input:** By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal depletion pull-down device is again provided. Connecting this pin to $V_{SS}$ programs the 24-hour display format. Segment connections for 10's of Hours in 24-hour mode are shown in *Figure 6*.

**Power Fail Indication:** If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of clock, all "ON" segments will flash at 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal.

## connection diagrams

**Dual-In-Line Package**

| | | |
|---|---|---|
| AM OUTPUT | 1 | 40 PM OUTPUT |
| 10 HRS – b & c | 2 | 39 COLON (1 Hz) |
| HRS – f | 4 | 38 12/24 HR SELECT |
| HRS – g | 3 | 37 NC |
| HRS – a | 5 | 36 50/60 Hz SELECT |
| HRS – b | 6 | 35 50/60 Hz INPUT |
| HRS – c | 7 | 34 FAST SET INPUT |
| HRS – c | 8 | 33 SLOW SET INPUT |
| HRS – e | 9 | 32 SECOND DISPLAY INPUT |
| 10 MINS – f | 10 | 31 ALARM DISPLAY INPUT |
| 10 MINS – g | 11 | 30 SLEEP DISPLAY INPUT |
| 10 MINS – a & d | 12 | 29 $V_{DD}$ |
| 10 MINS – b | 13 | 28 $V_{SS}$ |
| 10 MINS – e | 14 | 27 SLEEP OUTPUT |
| 10 MINS – c | 15 | 26 ALARM "OFF" INPUT |
| MINS – f | 16 | 25 ALARM OUTPUT |
| MINS – g | 17 | 24 SNOOZE INPUT |
| MINS – a | 18 | 23 OUTPUT COMMON SOURCE |
| MINS – b | 19 | 22 MINS – c |
| MINS – e | 20 | 21 MINS – d |

TOP VIEW

**Order Number MM5387AAN**
**See Package 24**

**FIGURE 2(a). MM5387AA**

**Dual-In-Line Package**

| | | |
|---|---|---|
| PM OUTPUT | 1 | 40 AM OUTPUT |
| COLON (1 Hz) | 2 | 39 10 HRS – b & c |
| 12/24 HR SELECT | 3 | 38 HRS – f |
| NC | 4 | 37 HRS – g |
| 50/60 Hz SELECT | 5 | 36 HRS–1 |
| 50/60 Hz INPUT | 6 | 35 HRS – b |
| FAST SET INPUT | 7 | 34 HRS – d |
| SLOW SET INPUT | 8 | 33 HRS – c |
| SECOND DISPLAY INPUT | 9 | 32 HRS – e |
| ALARM DISPLAY INPUT | 10 | 31 10 MINS – f |
| SLEEP DISPLAY INPUT | 11 | 30 10 MINS – g |
| $V_{DD}$ | 12 | 29 10 MINS – a & d |
| $V_{SS}$ | 13 | 28 10 MINS – b |
| SLEEP OUTPUT | 14 | 27 10 MINS – e |
| ALARM "OFF" INPUT | 15 | 26 10 MINS – c |
| ALARM OUTPUT | 16 | 25 MINS – f |
| SNOOZE INPUT | 17 | 24 MINS – g |
| OUTPUT COMMON SOURCE | 18 | 23 MINS – a |
| MINS – c | 19 | 22 MINS – b |
| MINS – d | 20 | 21 MINS – e |

TOP VIEW

**Order Number MM53108N**
**See Package 24**

**FIGURE 2(b). MM53108 (Mirror Image Pin-Out)**

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## functional description (Continued)

**Alarm Operation and Output:** The alarm comparator *(Figure 1)* senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver *(Figure 4b)* which is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input or reset by the alarm "OFF" input.

**Snooze Alarm Input:** Momentarily connecting snooze to V$_{SS}$ inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to V$_{DD}$ by an internal depletion device. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

**Alarm "OFF" Input:** Momentarily connecting alarm "OFF" to V$_{SS}$ resets the alarm latch and thereby silences the alarm. This input is also returned to V$_{DD}$ by an internal depletion device. The momentary alarm "OFF" input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm "OFF" input should remain at V$_{SS}$.

**Sleep Timer and Output:** The sleep output can be used to turn "OFF" a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode, (Table I) and setting the desired time interval (Table II). This automatically results in a current-source output which can be used to turn "ON" a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning "OFF" the radio. This turn "OFF" may also be manually controlled (at any time in the countdown) by a momentary V$_{SS}$ connection to the Snooze input. The output circuitry is the same as the other outputs *(Figure 4b)*.
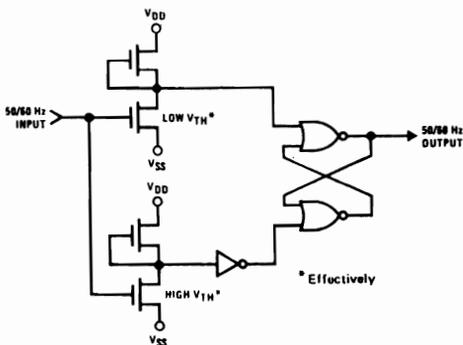


FIGURE 3. 50/60 Hz Input Shaping Circuit
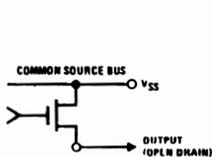


FIGURE 4(a). Segment Outputs
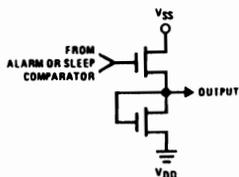


FIGURE 4(b). Alarm and Sleep Outputs

## functional description (Continued)

TABLE I. MM5387AA, MM53108 Display Modes

| *SELECTED DISPLAY MODE | DIGIT NO. 1 | DIGIT NO. 2 | DIGIT NO. 3 | DIGIT NO. 4 |
|---|---|---|---|---|
| Time Display | 10's of Hours & AM/PM | Hours | 10's of Minutes | Minutes |
| Seconds Display | Blanked | Minutes | 10's of Seconds | Seconds |
| Alarm Display | 10's of Hours & AM/PM | Hours | 10's of Minutes | Minutes |
| Sleep Display | Blanked | Blanked | 10's of Minutes | Minutes |

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected)

TABLE II. MM5387AA, MM53108 Setting Control Functions

| SELECTED DISPLAY MODE | CONTROL INPUT | CONTROL FUNCTION |
|---|---|---|
| *Time | Slow | Minutes Advance at 2 Hz Rate |
| | Fast | Minutes Advance at 60 Hz Rate |
| | Both | Minutes Advance at 60 Hz Rate |
| Alarm | Slow | Alarm Minutes Advance at 2 Hz Rate |
| | Fast | Alarm Minutes Advance at 60 Hz Rate |
| | Both | Alarm Resets to 12:00 AM (Midnight) (12-Hour Format) |
| | Both | Alarm Resets to 00:00 (24-Hour Format) |
| Seconds | Slow | Input to Entire Time Counter is Inhibited (Hold) |
| | Fast | Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes |
| | Both | Time Resets to 12:00:00 AM (Midnight) (12 Hour Format) |
| | Both | Time Resets to 00:00:00 (24 Hour Format) |
| Sleep | Slow | Subtracts Count at 2 Hz |
| | Fast | Subtracts Count at 60 Hz |
| | Both | Subtracts Count at 60 Hz |

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).
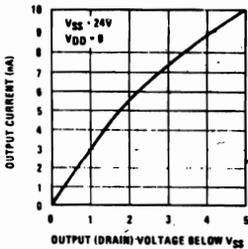


FIGURE 5. Typical Output Current Characteristics of MM5387AA, MM53108
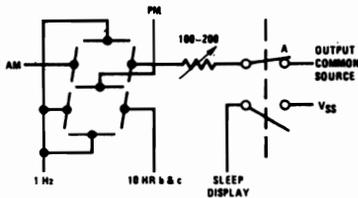


Switch A must be ganged with Sleep display as shown.

FIGURE 6. 24-Hour Operation: 10's of Hours Digit Connections

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# typical applications

*Figure* is a schematic diagram of a general purpose alarm clock circuit (12-hour mode) using the MM5387AA or MM53108 and a 3 1/2-digit LED display.
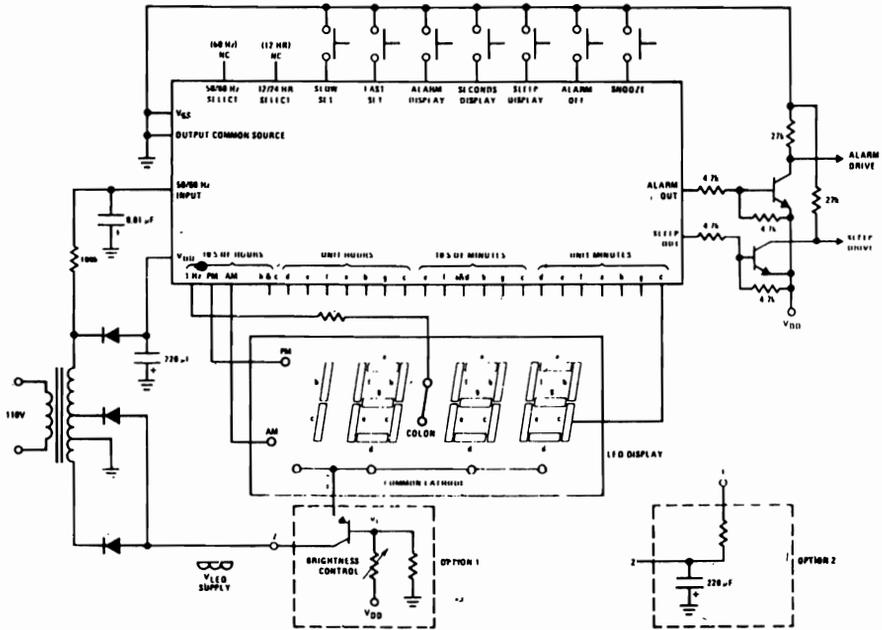


FIGURE 7

## MM5734 8-function accumulating memory calculator

### general description

The single-chip MM5734 calculator was developed using a metal gate P channel enhancement and depletion mode MOS/LSI technology with a primary object of low end product cost. A complete calculator as shown in *Figure 1* requires only the MM5734 calculator chip, an X-Y matrix keyboard, an NSA1198 or NSA1298 LED display and a 9V battery.

Keyboard decoding and key debounce circuitry, all clocks and timing generators, power on clear, and 7 segment output display decoding are included on chip, and require no external components. Segments and digits can usually be driven directly from the MM5734, as the segments typically source 8 mA of peak current and the digit drivers sink 20 mA min.

Leading zero suppression and a floating negative sign allow convenient reading of the display and conserve power. The MM5734 is capable of sensing a low battery voltage and indicates this by displaying a decimal point in digit eight. Up to 8-digits for positive numbers and 7 for negative numbers can be displayed, with the negative sign displayed in the 8th position. Typical current drain of a complete calculator displaying five "5's" is 25 mA.

The MM5734 is capable of decoding a keyboard matrix as shown in *Figure 1*. Three possible models are shown in *Figure 2*. *Figure 2(c)* illustrates a keyboard scheme which includes all 8 functions with only 23 keys by using a function key (F).

### features

- 8 digit, (7-negative), capacity
- 8 functions (+, -, X, , X², √X, 1/X, %)
- Convenient algebraic notation
- Fully protected accumulating memory ( _ M-)
- Automatic constant independent of memory
- Floating input/floating output
- Power-on clear*
- On-chip oscillator*
- Direct 9V battery compatibility
- Low system cost
- Direct digit drive of LED display
- Low cost X Y keyboard matrix

*Requires no external components

### connection diagram

**Dual-In-Line Package**

| Pin | | | Pin |
|---|---|---|---|
| D4 | 1 | 28 | D5 |
| D3 | 2 | 27 | D7 |
| D2 | 3 | 26 | D6 |
| D1 | 4 | 25 | D8 |
| K1 | 5 | 24 | D9 |
| K2 | 6 | 23 | V_DD |
| K3 | 7 | 22 | O |
| K4 | 8 | 21 | S_a |
| OSC | 9 | 20 | S_b |
| S_g | 10 | 19 | NC |
| IN1 | 11 | 18 | S_c |
| S_DP | 12 | 17 | S_d |
| S_f | 13 | 16 | S_e |
| V_SS | 14 | 15 | IN2 |

**TOP VIEW**

**Order Number MM5734N**
**See Package 23**
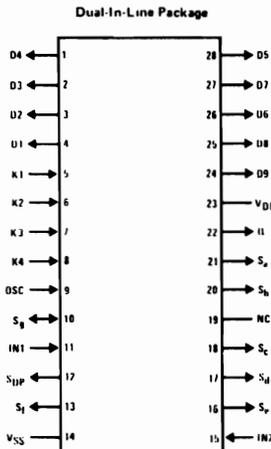
**Pin Description**

| | |
|---|---|
| K1 - K4 | Keyboard Inputs |
| IN1, IN2 | General Purpose Inputs |
| OSC | Programmable as External Oscillator |
| D1- D9 | Digit Outputs |
| S_a–S_g | Segment Outputs |
| SDP | Decimal Point Segment Output |
| O | General Purpose Output |
| V_DD | −9 Volts |
| V_SS | 0 Volts |

### keyboard outline

| | | | |
|---|---|---|---|
| F* | CS* | %* | D9 |
| F* | x²* | EX* | D8 |
| , * | M-* | M-* | ÷* | D7 |
| 1/X* | MH* | MC* | %* | D6 |
| 1/X | , | x² | ÷ | D5 |
| 7 | 8 | 9 | × | D4 |
| 4 | 5 | 6 | − | D3 |
| 1 | 2 | 3 | + | D2 |
| C CF | 0 | . | = | D1 |
| K4 | K3 | K2 | K1 | |

*Double Function Key

## functional description

The MM5734 is a calculator chip which contains five data registers: (1) entry, (2) accumulator, (3) 2 working and (4) memory, each consisting of 8 digits, sign, and decimal point. The entry register is always displayed. It contains digit entries from the keyboard, and results of all functions except M+ and M−. The accumulator is used in all arithmetic functions and stores a copy of the entry register on all results. This allows another number to be entered without losing an intermediate result. Multiply and divide requires three registers to perform the function and save the divisor, or multiplier. The working register is provided to perform these functions in conjunction with the entry and accumulator registers. A second working register is used to store the constant in chain operations while performing $X^2$ or $1/X$. This allows chain operation using $X^2$, $1/X$ and $\sqrt{X}$.

The memory register is used only to store a number to be used later. It is fully protected during all operations, and is only modified by depressing a "MS," "M+," or "M−" key. Power-on clears all of the registers including the memory register.

The MM5734 performs the $+$, $-$, $X$ and $\div$ functions using algebraic notation. This requires the use of a mode register and a terminate flag. The mode register directs the machine to the proper function (add, subtract, multiply or divide) with each new key entry. After the function has been performed, the key entered is used to modify the mode register

The terminate flag is set on "=" and sometimes on "%" and "C." This signifies the end of the problem. The MM5734 allows for full floating entries and intermediate results.

If the terminate flag is set, a "+," "−," "X" or "÷" key signals the beginning of a new problem. The number being displayed is copied into the accumulator register and the mode register assumes the mode of the key entered. The terminate flag is always reset by the "+," "−," "X" and "÷" keys.
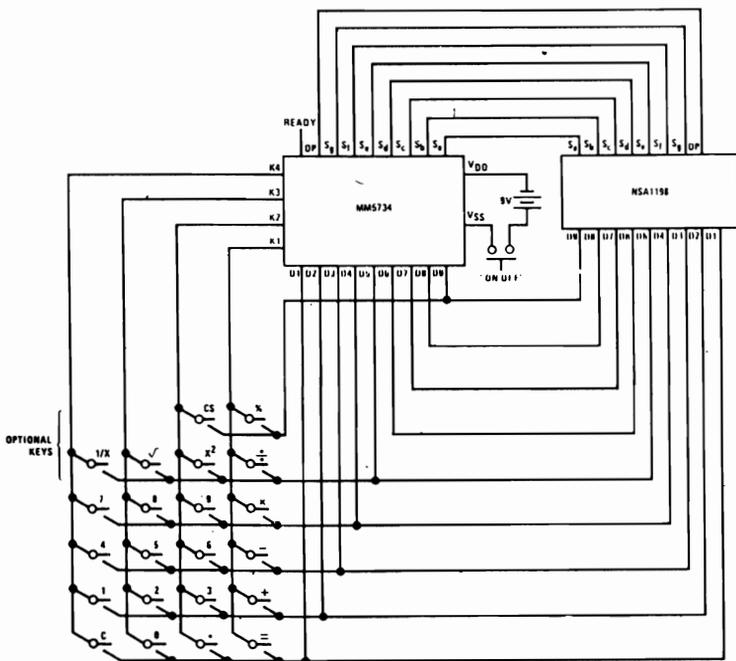


FIGURE 1A. Complete Calculator Schematic
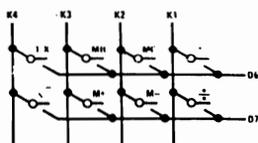


FIGURE 1(b). Optional Keys
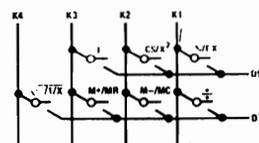


FIGURE 1(c). Optional Keys

## OPERATION IN THE ADD AND SUBTRACT MODE
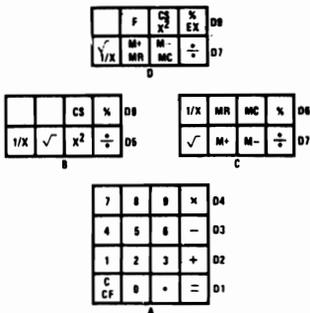


**FIGURE 2**

If the terminate flag is set, an "=" key will result in a constant add/subtract. The number in the accumulator will be added to (or subtracted from) the number being displayed. The result is right-justified and displayed in the entry register. Accumulator and mode registers are not altered, allowing for constant operations.

If the terminate flag is not set and a number has been entered from the keyboard, or memory register, a "+," "−," "X", or "÷" key will result in an addition or subtraction. The entry register will be added to or subtracted from the accumulator and the new running total will be displayed in the entry register and copied into the accumulator register. The mode will be altered according to which key is entered.

If the terminate flag is not set, and a number has not been entered from the keyboard, or memory, a "+," "−," "X," ":" key will only change the mode register to the new key entry.

If the terminate flag is not set, an "=" key will add/subtract the number being displayed to/from the number in the accumulator register. The number being displayed is transferred to the accumulator, and the result of the operation is displayed in the entry register. The terminate flag is set, conditioning the calculator for constant, add/subtract operation. The number being displayed previous to the "=" key is stored in the accumulator as the constant.

Operation of the "%" key in add/subtract mode, with the terminate flag reset, will multiply the accumulator by the last entry, divide the result by 100, and display it in the entry register. The mode register remains as it was in the add/subtract mode. All of the above is required to perform the percent add on or discount problems. Depression of an "=" key after the "%" key will either tax or discount the original number as a function of the mode register and the last entry.

Operation of the "%" key in add/subtract mode, with the terminate flag set, will shift the decimal point of the number being displayed two places to the left and copy it into the accumulator register. The mode is set to multiply and the terminate flag remains set.

### Operation in the Multiply Mode

If the terminate flag is set, an "=" key will result in a constant multiply operation. The number being displayed is multiplied by the constant stored in the accumulator register. The result is displayed in the entry register and the accumulator and mode registers are not altered, allowing for constant operation. Repeated depressions of the "=" key can be used to raise a number to an integer power, i.e., "C," "C," "5.2," "X," "=," "=," "=," computes $5.2^4$.

The constant in multiplication, as well as in addition, subtraction and division is the last number entered. For the sequence: "C," "C," "3," "÷," "4," "X," "2," "=" the constant multiplier for future problems is 2.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the display will be multiplied by the contents of the accumulator, and the results will be displayed in the entry register. The number previously in the entry register is stored in the accumulator register and the terminate flag is set.

If the terminate flag is not set, and a number has been entered from the keyboard or memory register, a "+," "−," "X" or "÷" key will result in a multiplication. The number being displayed will be multiplied by the number residing in the accumulator register. The result will be copied into the accumulator and displayed in the entry register. The mode register is updated as a function of the key depressed.

Operation of the "%" key while in multiply mode looks exactly the same as an "=" key except the decimal point of the display is shifted two positions to the left before the multiplication takes place.

### Operation in the Divide Mode

If the terminate flag is set, an "=" key will result in constant divide operation. The number being displayed is divided by the constant stored in the accumulator register. The accumulator and mode registers are not altered allowing for constant operations. Repeated depressions of the "−" key will result in repeated divisions by the constant. Thus, it is possible to raise a number to a negative power using the sequence "C," "C," "1," "÷," "No.," "=," "=," etc.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the accumulator register will be divided by the number being displayed. The result is transferred to the entry register and displayed. The terminate flag is set and the divisor is stored in the accumulator register.

If the terminate flag is not set, a "+," "−," "X" or "÷" key will result in a division. The number in the accumulator register will be divided by the number being displayed. The results are displayed in the entry register, and a copy of the result is stored in the accumulator. The mode register is modified to reflect the latest key entry.

Operation of the "%" key while in divide mode looks exactly the same as the "=" key except the decimal point of the display is shifted two positions to the left before division takes place.
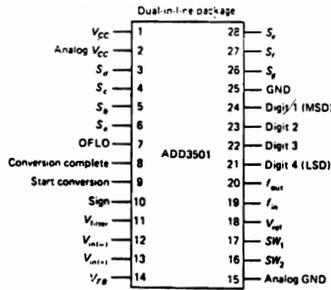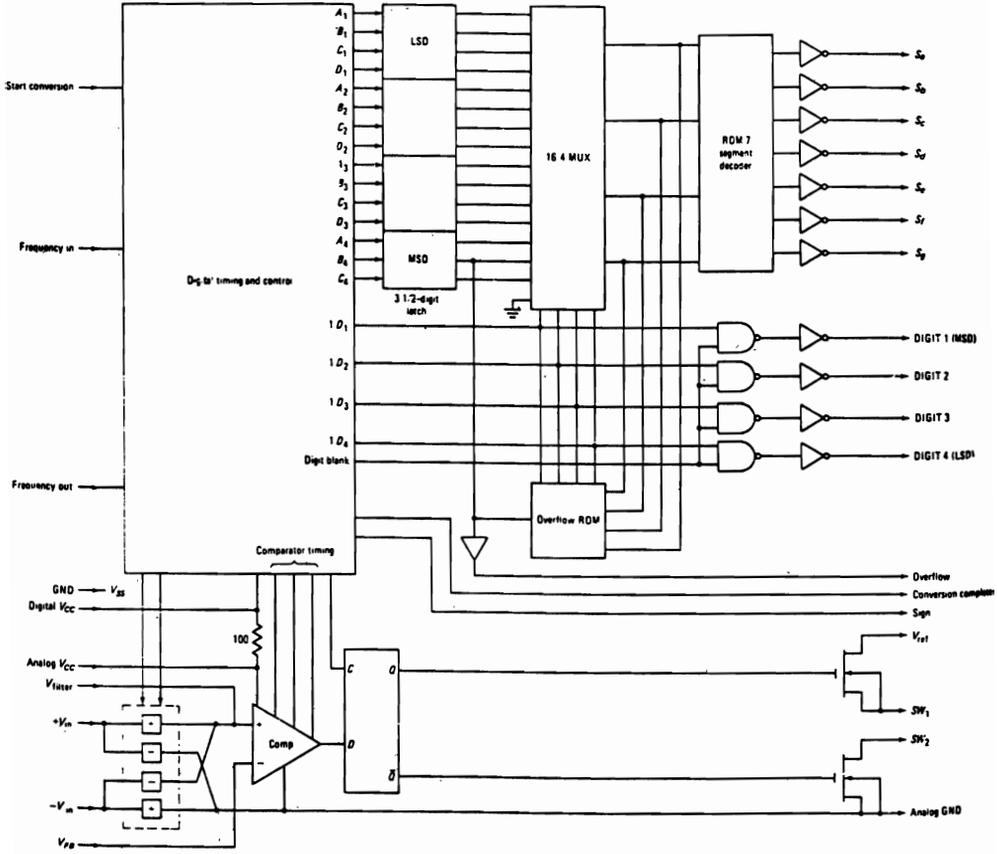
FIG. 14-21  National Semiconductor ADC 3501

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# Electronic Telephone

## The Complete Electronic Telephone Circuit

**MC34010/11A** — $T_A = -20°$ to $+60°C$, Case 711, 777
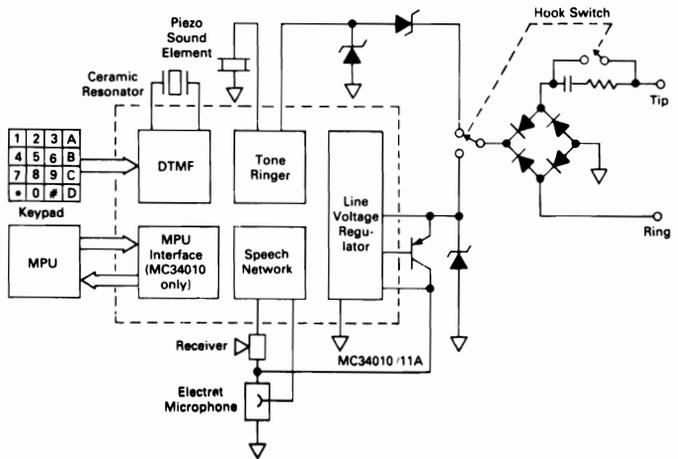


The conventional transformer-driven telephone handset is undergoing major innovations. The bulky transformer is disappearing. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2-to-4 wire conversion, DTMF dialing, tone ringing, and a variety of related activities.

The culmination of these capabilities is the Electronic Telephone Circuit, the MC34010/11A. These IC's place all of the above mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar linear ($I^2L$) technology and provide all the necessary elements of a modern tone-dialing telephone. The MC34010 even incorporates an MPU interface circuit for the inclusion of automatic dialing in the final system.

### Features

- Provides All Basic Telephone Functions, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator

- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique

- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA-470 Requirements

- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter

- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths

- $I^2L$ Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity

- MC34010P Provides Microprocessor Interface Port for Automatic Dialing Features

# Tone Ringers

The MC34012 and MC34017 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are on the line. The MC34012 series and the MC34017 series were designed to meet those requirements.

**MC34012** — $T_A$ = −20° to +60°C, Case 626, 751
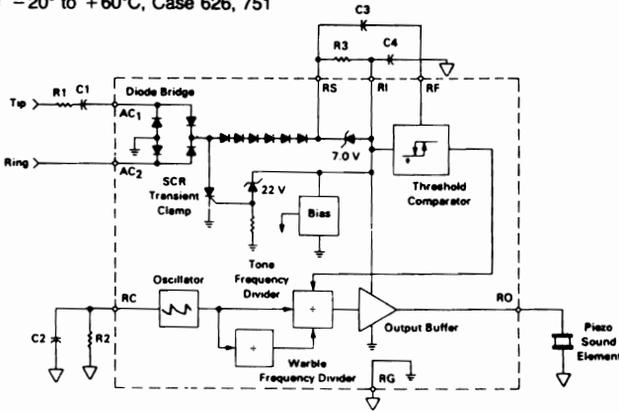


- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options — MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz

- Push Pull Output Stage for Greater Output Power Capability (MC34017)
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

**MC34017** — $T_A$ = −20° to +60°C, Case 626, 751
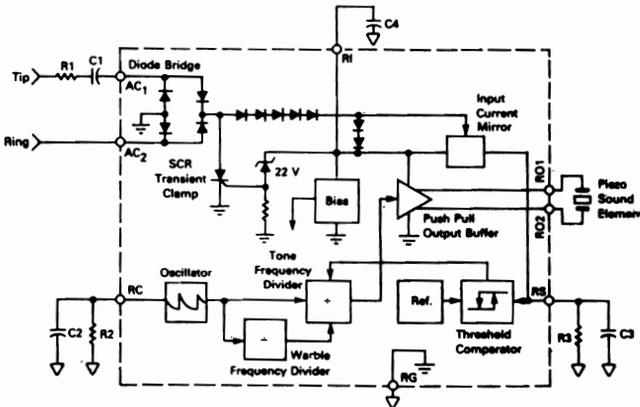
# PCF8200
## CMOS Male/Female Speech Synthesizer

*Objective Specification*

## DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.

## FEATURES

- Male and female speech with good quality
- Speech-band from 0 to 5kHz
- Bit rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to +85°C
- Single 5V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8-bit parallel bus or I²C bus
- Software readable status word (parallel bus or I²C bus)
- BUSY-signal and REQN-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

## APPLICATIONS

- Telecommunications
- Video games
- Aids for the handicapped
- Industrial control equipment
- Automotive
- Irrigation systems

## PIN CONFIGURATION

N Package

| Pin | | Pin | |
|-----|-----|-----|-----|
| V_DD-A | 1 | 24 | V_DD-D |
| V_REF | 2 | 23 | D8 |
| OUT | 3 | 22 | D7 |
| V_SS-A | 4 | 21 | D2 |
| NC | 5 | 20 | D3 |
| TEST | 6 | 19 | D4 |
| OSC1 | 7 | 18 | D5 |
| OSC0 | 8 | 17 | SCL/D6 |
| SERN/PAR | 9 | 16 | SDA/D7 |
| REQN | 10 | 15 | WN |
| BUSY | 11 | 14 | RN/W |
| V_SS-D | 12 | 13 | CEN |

TOP VIEW
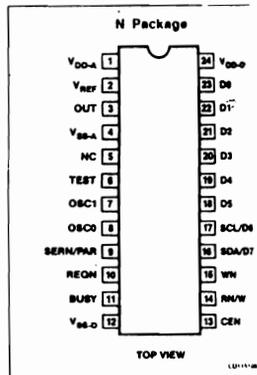
## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|-------------|-------------------|------------|
| 24-Pin Plastic DIP (SOT-101A) | −40°C to +85°C | PCF8200PN |

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## FEATURES

- TIMING FROM MICROSECONDS THROUGH HOURS
- OPERATES IN BOTH ASTABLE AND MONOSTABLE MODES
- ADJUSTABLE DUTY CYCLE
- HIGH CURRENT OUTPUT CAN SOURCE OR SINK 200mA
- OUTPUT CAN DRIVE TTL
- TEMPERATURE STABILITY OF 0.005% PER °C
- NORMALLY ON AND NORMALLY OFF OUTPUT
  -

## APPLICATIONS

PRECISION TIMING
PULSE GENERATION
SEQUENTIAL TIMING
TIME DELAY GENERATION
PULSE WIDTH MODULATION
PULSE POSITION MODULATION
MISSING PULSE DETECTOR

## PIN CONFIGURATION
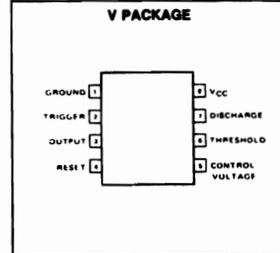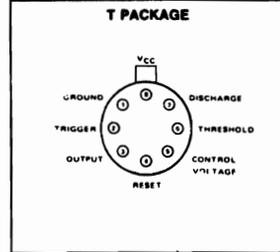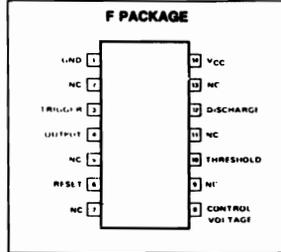
### F PACKAGE



### T PACKAGE



### V PACKAGE



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage
| | |
|---|---|
| SE555 | +18V |
| NE555 | +16V |
| Power Dissipation | 600 mW |

Operating Temperature Range
| | |
|---|---|
| NE555 | 0°C to +70°C |
| SE555 | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 60 seconds) | +300°C |

## EQUIVALENT CIRCUIT
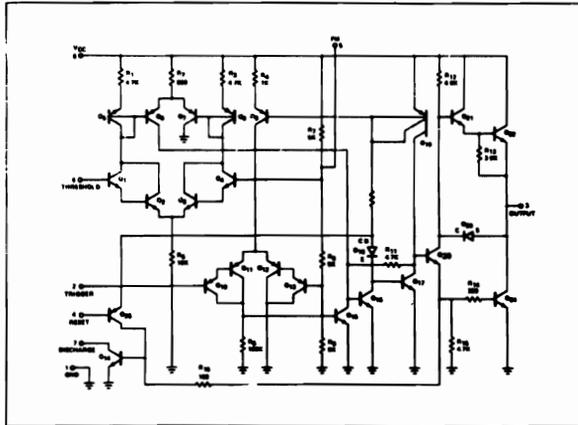


## BLOCK DIAGRAM
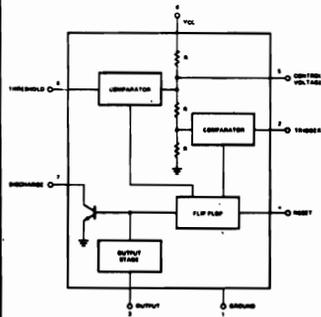
## FEATURES
- TIMING FROM MICROSECONDS TO HOURS
- REPLACES TWO 555 TIMERS
- OPERATES IN BOTH ASTABLE, MONOSTABLE, TIME DELAY MODES
- HIGH OUTPUT CURRENT
- ADJUSTABLE DUTY CYCLE
- TTL COMPATIBLE
- TEMPERATURE STABILITY OF 0.005% PER °C

## ABSOLUTE MAXIMUM RATIONS
Supply Voltage
| | |
|---|---|
| SE556 | +18V |
| NE556 | +16V |
| Power Dissipation | 600mW |

Operating Temperature Range
| | |
|---|---|
| NE556 | 0°C to +70°C |
| SE556 | −55°C to +125°C |
| SE556C | −55°C to +125°C |

Storage Temperature
| | |
|---|---|
| Range | −65°C to +150°C |
| Lead Temperature (Soldering, 60 sec) | +300°C |

## APPLICATIONS
- PRECISION TIMING
- SEQUENTIAL TIMING
- PULSE SHAPING
- PULSE GENERATOR
- MISSING PULSE DETECTOR
- TONE BURST GENERATOR
- PULSE WIDTH MODULATION
- TIME DELAY GENERATOR
- FREQUENCY DIVISION
- INDUSTRIAL CONTROLS
- PULSE POSITION MODULATION
- APPLIANCE TIMING
- TRAFFIC LIGHT CONTROL
- TOUCH TONE ENCODER

## PIN CONFIGURATION
### A PACKAGE

| Pin | | | Pin |
|---|---|---|---|
| Discharge | 1 | 14 | $V_{CC}$ |
| Threshold | 2 | 13 | Discharge |
| Control Voltage | 3 | 12 | Threshold |
| Reset | 4 | 11 | Control Voltage |
| Output | 5 | 10 | Reset |
| Trigger | 6 | 9 | Output |
| Ground | 7 | 8 | Trigger |
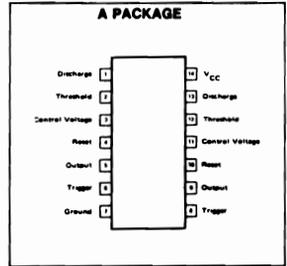
## BLOCK DIAGRAM
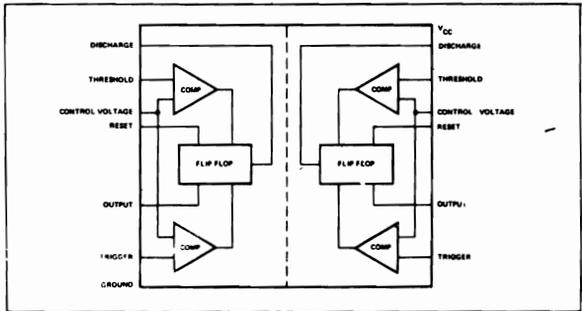
## EQUIVALENT CIRCUIT (SHOWN FOR ONE CIRCUIT ONLY)
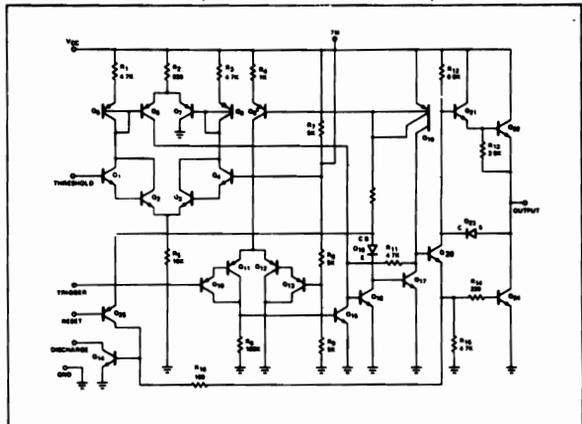
## SG7800A/7800AC/7800/7800C/140/240/340

### DESCRIPTION

The SG7800A/7800/140 series of positive regulators offer self contained, fixed-voltage capability with up to 1.5 amps of load current and input voltages up to 50 volts. (SG7800A series only)

These units feature a unique on-chip trimming system to set the output voltages to within ±1.5% of nominal on the SG7800A series, ±2.0% on the SG140/240 series, and ±4.0% on the SG7800/340 series. The SG7800A versions also offer much improved line and load regulation characteristics.

All protective features of thermal shutdown, current limiting, and safe-area control have been designed into these units and since these regulators require only a small output capacitor for satisfactory performance, ease of application is assured.

Although designed as fixed-voltage regulators, the output voltage can be increased through the use of a simple voltage divider. The low quiescent drain current of the device insures good regulation when this method is used.

Product is available in hermetically sealed TO-3, TO-39 and TO-66 power packages as well as the plastic TO-220 package.
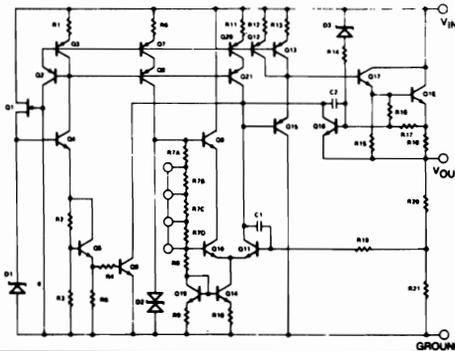
### FEATURES

- Output voltage set internally to ±1.5% on SG7800A
- Input voltage range to 50 volts max. on SG7800A
- Two volt input-output differential
- Excellent line and load regulation
- Foldback current limiting
- Thermal overload protection
- Voltages available — 5V, 6V, 8V, 12V, 15V, 18V, 20V, 24V

### ABSOLUTE MAXIMUM RATINGS

| Device Output Voltage | Input Voltage (operating) | 7800A Series Input Voltage (transient)* | Input Voltage (Output shorted to ground) |
|---|---|---|---|
| 5V | 35V | 50V | 35V |
| 6V | 35V | 50V | 35V |
| 8V | 35V | 50V | 35V |
| 12V | 35V | 50V | 35V |
| 15V | 35V | 50V | 35V |
| 18V | 35V | 50V | 35V |
| 20V | 35V | 50V | 35V |
| 24V | 40V | 50V | 35V |

*see note next page

Operating Junction Temperature Range
SG7800A/7800/140     −55°C to +150°C
SG240     0°C to +150°C
SG7800AC/7800C/340     0°C to +125°C
Storage Temperature Range     −65°C to +150°C

Typical Power/Thermal Characteristics

| Package | K (TO-3) | R(TO-66) | P (TO-220) | T (TO-39) |
|---|---|---|---|---|
| 25°C Case Rated Power | 20W | 15W | 15W | 2W |
| 25°C Ambient Rated Power | 4.3W | 3.0W | 2.0W | 1.0W |
| Design Current | 1.5A | 1.5A | 1.0A | 0.5A |
| Therm. Res. θJC (°C/W) θJA (°C/W) | 3.0 35 | 5.0 40 | 3.0 60 | 15 120 |

### SIMPLIFIED SCHEMATIC



### CONNECTION DIAGRAMS    TOP VIEWS



T-Package TO-39

K-Package TO-3

R-Package TO-66

P-Package TO-220

FRONT VIEW

1 – Input
2 – Output
3 – Ground
Tab – Ground

### CHIP LAYOUT



653
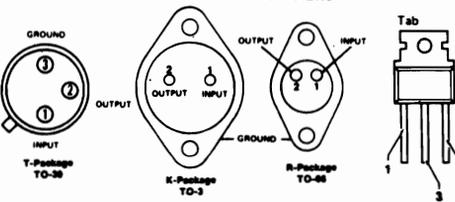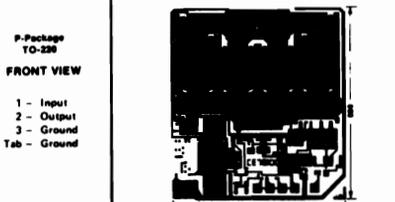
## SG7800A/7800AC/7800/7800C/140/240/340

---

### CHARACTERISTIC CURVES

**PEAK OUTPUT CURRENT vs. INPUT-OUTPUT DIFFERENTIAL**

K, R & P Pkg Only



Output Current - Amps

$V_O = 200$ mV

Input-Output Voltage Differential - Volts
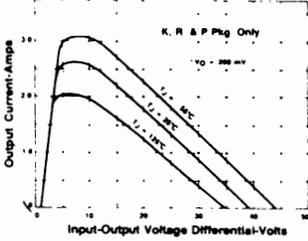
**MINIMUM INPUT-OUTPUT VOLTAGE vs. LOAD CURRENT**



Dropout Voltage - Volts

$T_J = 25°C$
$T_J = 25°C$
$T_J = 125°C$

K, R & P Pkg Only

$\Delta V_O = 200$ mV
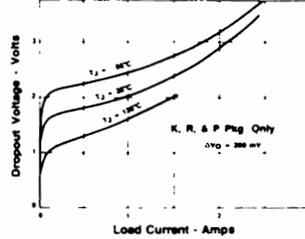
Load Current - Amps

**RIPPLE REJECTION vs. FREQUENCY**



Ripple Rejection - dB

SG7805
SG7815
SG7824

$V_{IN}$ (low) = $V_O$ + 3V
$V_{IN}$ (high) = $V_O$ + 13V
$I_O = 100$ mA
$T_J = 25°C$

Frequency - Hertz
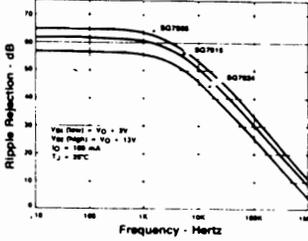
**TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE**



Output Voltage Change - %

$V_{IN} = V_O$ + 5V
$I_O = 10$ mA

Junction Temperature - °C
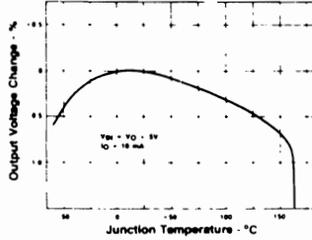
**Note:** Operation at high input voltages is dependent upon load current. When load current is less than 5 mA, output will rise out of regulation as input-output differential increases beyond 30 volts. Note also from curve above, that maximum load current is reduced at high voltages. The 50 volt input rating of the SG7800A series refers to ability to withstand high line or transient conditions without damage. Since the regulator's maximum current capability is reduced, the output may fall out of regulation at high input voltages under nominal loading

---

### APPLICATIONS

**FIXED OUTPUT REGULATOR**



INPUT — SG78XX — OUTPUT
0.33 µF*
0.1 µF*
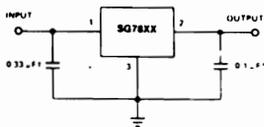
*INCREASING VALUE OF OUTPUT CAPACITOR IMPROVES SYSTEM TRANSIENT RESPONSE
†REQUIRED ONLY IF REGULATOR IS LOCATED AN APPRECIABLE DISTANCE FROM POWER SUPPLY FILTER

**CIRCUIT FOR INCREASING OUTPUT VOLTAGE**



INPUT — SG78XX — OUTPUT
$V_{XX}$
R1
0.33 µF
$I_Q$
R2
0.1 µF

$$V_O = V_{XX}\left(1 + \frac{R2}{R1}\right) + I_Q R2$$
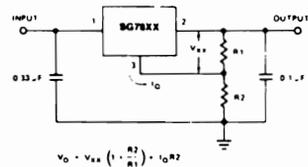
**HIGH OUTPUT CURRENT, SHORT CIRCUIT PROTECTED**



INPUT
$R_{SC}$
2N4398
R1
3Ω
2N6124
SG78XX
OUTPUT
0.33 µF
0.1 µF
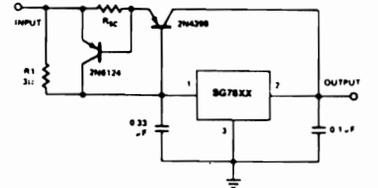
**ADJUSTABLE OUTPUT REGULATOR, 7 to 30 VOLTS**



INPUT — SG7805 — OUTPUT
0.33 µF
SG741
1 kΩ
10K
0.1 µF

---
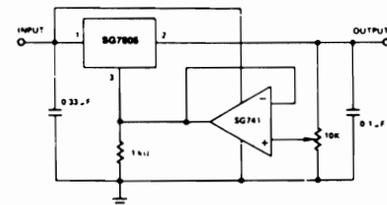
# SG123 / SG223 / SG323

## Description

The SG123 is a three terminal, three amp, five volt regulator similar to the LM123 but with a special low voltage zener instead of the band gap reference. The SG123 has superior load regulation, lower input-output differential minimums, lower quiescent current, and better temperature coefficient. The circuit is specified identically to the LM123 and is pin for pin compatible with that device. The SG123 uses special processing techniques to achieve reliable operation at high temperatures and high current levels for extended periods of time.

The SG123 has been designed for ease of operation as well as performance. It is completely internally phase compensated, and requires no external capacitors unless used with long lead lengths or high speed transients. The device is protected by thermal shutdown, standard current limiting, and an instantaneous power limiting circuit sensitive to high input voltages. In addition, the power transistor is an upgrade of previous three terminal designs and is unusually rugged.

Operation is guaranteed over the junction temperature range of −55°C to +150°C. The SG223 is a similar device guaranteed to operate from −25°C to +150°C. The SG323 is guaranteed over the junction temperature range of 0°C to +125°C.

## Features
- 3A Output Currents
- Full Internal Protection
- 7.0 V Minimum Input Voltage, Typical
- Zener Reference for Top Performance

SCHEMATIC



## CONNECTION DIAGRAM



TOP VIEW
K-Package
TO-3

## CHIP LAYOUT
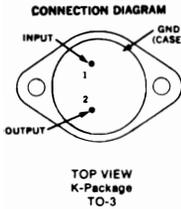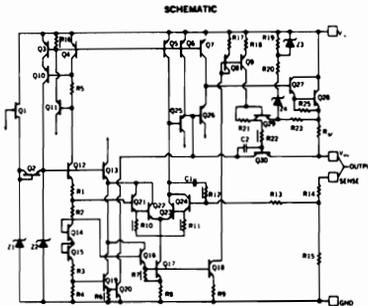


## Absolute Maximum Ratings

| | |
|---|---|
| Input Voltage | 20V |
| Power Dissipation | Internally Limited |
| Operating Junction Temperature Range | |
| SG123 | −55°C to +150°C |
| SG223 | −25°C to +150°C |
| SG323 | 0°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

## Electrical Characteristics (Note 1)

| PARAMETER | CONDITIONS | SG123/SG223 | | | SG323 | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Output Voltage | T = 25°C, V = 7.5V, I = 0 | 4.7 | 5 | 5.3 | 4.8 | 5 | 5.2 | V |
| Output Voltage | 7.5V ≤ V ≤ 15V, 0 ≤ I ≤ 3A, P ≤ 30W | 4.6 | | 5.4 | 4.75 | | 5.25 | V |
| Line Regulation (Note 2) | T = 25°C, 7.5V ≤ V ≤ 15V | | 5 | 25 | | 5 | 25 | mV |
| Load Regulation (Note 2) | T = 25°C, V = 7.5V, 0 ≤ I ≤ 3A | | 25 | 100 | | 25 | 100 | mV |
| Quiescent Current | 7.5V ≤ V ≤ 15V, 0 ≤ I ≤ 3A | | 12 | 20 | | 12 | 20 | mA |
| Short Circuit Current Limit | T = 25°C, V = 15V, V = 7.5V | | 3 | 5.0 | | 3 | 5.0 | A |
| | | | 4 | 5.5 | | 4 | 5.5 | A |
| Long Term Stability | | | | 35 | | | 35 | mV |
| Thermal Resistance Junction to Case (Note 3) | | | 2 | | | 2 | | °C/W |

**Note 1:** Unless otherwise noted, specifications apply for −55°C < T < +150°C for the SG123, −25°C ≤ T ≤ +150°C for the SG223, and 0° < T < +125°C for the SG323. Specifications apply for P < 30W.

**Note 2:** Load and line regulation are specified with high speed tests in order to separate their effects from temperature coefficient. Pulse testing is required with a pulse width < 1 ms and a duty cycle < 5%.

**Note 3:** The junction to ambient thermal resistance of the TO-3 package is about 35°C/W.

# General-Purpose Positive Regulator

## SG723/723C

This regulator is designed for use with either positive or negative supplies as a series, shunt, switching, or floating regulator with currents up to 150mA. Higher current requirements may be accommodated through the use of external NPN or PNP power transistors.

- Positive or negative supply operation
- 0.03% line and load regulation
- Output adjustable from 2 to 37V
- Low standby current drain
- 0.002%/°C average temperature variation

| PARAMETERS | 723[1] | 723C[1] | UNITS |
|---|---|---|---|
| Operating Temperature Range | −55 to +125 | 0 to +70 | °C |
| Package Types | T*, J | T*, J, N | − |
| Input Voltage Range | 9.5 to 50 | 9.5 to 50 | V |
| Output Voltage Range | 2.0 to 37 | 2.0 to 37 | V |
| Input/Output Differential | 3.0 to 38 | 3.0 to 38 | V |
| Load Regulation[2],[3] | 0.15 | 0.2 | % $V_{out}$ |
| Line Regulation $V_{in}$ = 12 to 40V | 0.2 | 0.5 | % $V_{out}$ |
| Ripple Rejection $C_{ref}$ = 5μF; f = 50Hz to 10KHz | 86 (typ) | 86 (typ) | dB |
| Reference Voltage | 6.95 − 7.35 | 6.80 − 7.50 | V |
| Temperature Stability | 0.015 | 0.015 | %/°C |
| Output Noise Voltage $C_{ref}$ = 0; BW = 100Hz to 10KHz | 20 (typ) | 20 (typ) | μV rms |
| Standby Current Drain | 3.5 | 4.0 | mA |
| Minimum Load Current | 0 | 0 | mA |
| Long Term Stability | 0.1 (typ) | 0.1 (typ) | %/khr |

[1] Parameters apply at $T_A$ = +25°C, except temperature stability is over temperature ranges.

[2] Applies for constant junction temperature. Temperature drift* effects must be taken into account separately when the unit is operating under conditions of high dissipation.

[3] $I_L$ = 1 to 50 mA.

* T-package is TO-96 (can height 240" max., 230" min.)



SG723/723C Chip
See T-Package for pad functions)
Note Vz (Pin X) is available only in J or N-Package
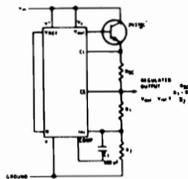


High Current Regulator
External NPN Transistor
$I_L$ = 1A
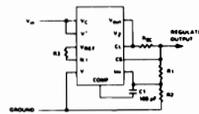


Basic High Voltage Regulator
$V_{out}$ = 7 to 37 volts

## CONNECTION DIAGRAMS
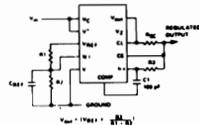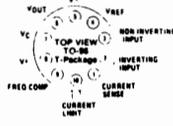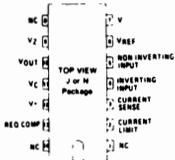






Basic Low Voltage Regulator
$V_{out}$ = 2 to 7 volts

# LM117/LM217/LM317 3-Terminal Adjustable Regulator

## General Description

The LM117/LM217/LM317 are adjustable 3 terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

## Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The LM117K, LM217K and LM317K are packaged in standard TO-3 transistor packages while the LM117H, LM217H and LM317H are packaged in a solid Kovar base TO-39 transistor package. The LM117 is rated for operation from -55°C to +150°C, the LM217 from -25°C to +150°C and the LM317 from 0°C to +125°C. The LM317T and LM317MP, rated for operation over a 0°C to +125°C range, are available in a TO-220 plastic package and a TO-202 package, respectively.

For applications requiring greater output current in excess of 3A and 5A, see LM150 series and LM138 series data sheets, respectively. For the negative complement, see LM137 series data sheet.

**LM117 Series Packages and Power Capability**

| DEVICE | PACKAGE | RATED POWER DISSIPATION | DESIGN LOAD CURRENT |
|---|---|---|---|
| LM117 | TO-3 | 20W | 1.5A |
| LM217 LM317 | TO-39 | 2W | 0.5A |
| LM317T | TO-220 | 15W | 1.5A |
| LM317M | TO-202 | 7.5W | 0.5A |

## Connection Diagrams



(TO-3 STEEL) Metal Can Package

ADJUSTMENT
IN
1
2
CASE IS OUTPUT

BOTTOM VIEW
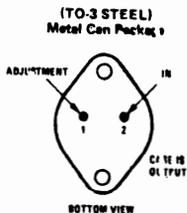
Order Number:
LM117K STEEL
LM217K STEEL
LM317K STEEL
See Package K02A

(TO-39) Metal Can Package

1 INPUT
2 ADJUSTMENT
3 OUTPUT

CASE IS OUTPUT
BOTTOM VIEW
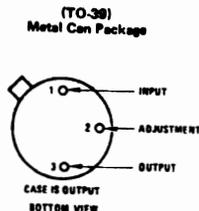
Order Number:
LM117H
LM217H
LM317H
See Package H03A

(TO-220) Plastic Package

VOUT
ADJ
VIN
VOUT
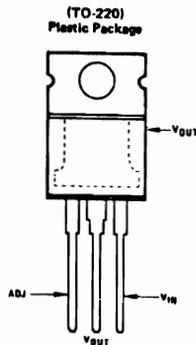
Order Number:
LM317T
See Package T03B

(TO-202) Plastic Package

VOUT
ADJ
VIN
VOUT

FRONT VIEW
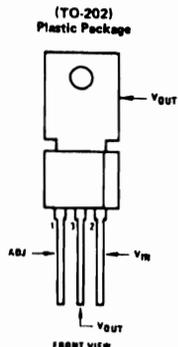
Order Number:
LM317MP
See Package P03A
Tab Formed Devices
LM317MP TB
See Package P03E

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# SG3524
## SMPS Control Circuit

*Product Specification*

## DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer-coupled DC-to-DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

## FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

## PIN CONFIGURATION

### D¹, F, N Packages

| | | | |
|---|---|---|---|
| INVERT INPUT | 1 | 16 | VREF |
| NON INVERT INPUT | 2 | 15 | VIN |
| OSC OUTPUT | 3 | 14 | EMITTER B |
| (-) CA SENSE | 4 | 13 | COLLECTOR B |
| (-) CL SENSE | 5 | 12 | COLLECTOR A |
| RT | 6 | 11 | EMITTER A |
| CT | 7 | 10 | SHUTDOWN |
| GROUND | 8 | 9 | COMPENSATION |

TOP VIEW

NOTE:
1. SOL-Released in large SO package only.
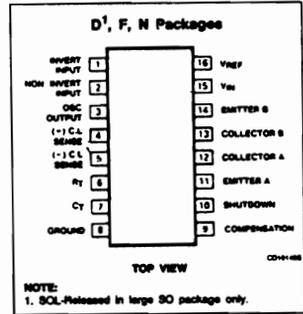
## ORDERING INFORMATION

| DESCRIPTION | TEMPERATURE RANGE | ORDER CODE |
|---|---|---|
| 16-Pin Plastic DIP | 0 to +70°C | SG3524N |
| 16-Pin Cerdip | 0 to +70°C | SG3524F |
| 16-Pin SOL | 0 to +70°C | SG3524D |

## BLOCK DIAGRAM
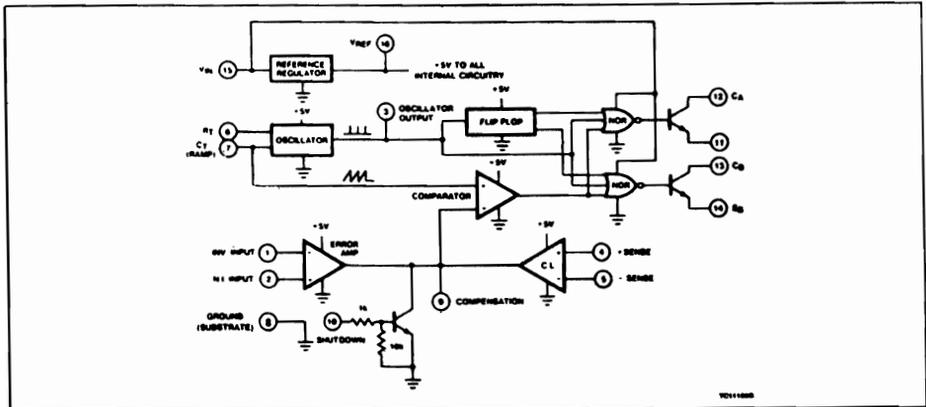
# Standard Digital BUS-Interfaces

Communication between a computer and a peripheral may be

*a*) **Simplex** where information can be transmitted in one direction only, e.g. computer to (non-intelligent) printer, keyboard to computer.
*b*) **Half duplex** where information may be transmitted in both directions but in only one direction at a time, e.g. IEEE 488 bus
*c*) **Full duplex** where information may be transmitted in both directions simultaneously, e.g. VDU.

It is now a universal standard to transmit computer data in bytes comprising a seven-bit ASCII code with the eighth bit as a parity test. The data byte may be transmitted **in parallel**, when all eight bits are transmitted on eight separate transmission lines, or **serially** when the data bits are transmitted separately, in a serial sequence, down a single transmission line
In both cases the data may be transmitted with synchronous clock pulses (**synchronous transmission**). Additional lines for *handshaking* may also be present.

Parallel and serial transmission of the data byte
A6 = 10100110
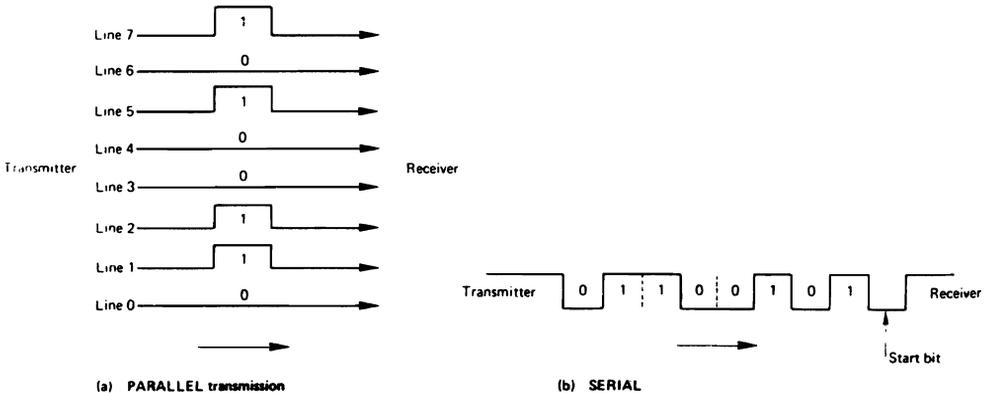


(a) PARALLEL transmission

(b) SERIAL

Parallel transmission has the advantage of speed (about eight times faster than serial transmission). However, it requires eight times as many transmitting and receiving circuits, at increased cost, which are also prone to *cross-talk* and have poor noise immunity. Parallel transmission is usually limited to cases where the transmitter and receiver are situated close to each other, resulting in connecting cable lengths of 20 m or less.

Serial transmission is used for long-range (20 m to many kilometres) communications where the cost of multiple data transmission lines would be high, and where facilities for multiple lines may not even exist (e.g. telephone lines). The use of a single transmission line can allow circuits with good noise immunity properties to be used at an overall economic cost.

To allow different peripherals to be interfaced to different computing systems, with minimal hardware and software effort, standard interfacing systems have been developed. Of these the IEEE 488 (GPIB) bus (parallel transmission) and the RS 232C (serial transmission) are now universally recognised standards.

## IEEE 488 (GPIB) Bus

The standards for this bus were set by the Institute of Electrical and Electronics Engineers (USA) in October 1975 (IEEE document number ANSI MC 1.1, 1975) and accepted as an international standard in 1980. This interface is also known as the HP-IB (Hewlett Packard Interface Bus) and, more recently, as the GPIB (General Purpose Interface Bus).

**Fig. c    IEEE 488 bus structure**

| Connector pin number | Function | Abbreviation | |
|---|---|---|---|
| 6 | Data Valid | DAV | Handshake control lines |
| 7 | Not Ready For Data | NRFD | |
| 8 | Not Data ACcepted | NDAC | |
| 5 | End Or Identify | EOI | Management control lines |
| 9 | InterFace Clear | IFC | |
| 10 | Service ReQuest | SRQ | |
| 11 | ATtentioN | ATN | |
| 17 | Remote ENable | REN | |

IEEE 488 CONTROLLER (Computer)

Device 1 only able to talk (e.g. counter)

Device 2 only able to listen (e.g. signal generator)

Device 3 able to talk and listen (e.g. digital multimeter)

DATA BUS

| | | |
|---|---|---|
| 1 | DIO1 | |
| 2 | DIO2 | |
| 3 | DIO3 | |
| 4 | DIO4 | Data bus |
| 13 | DIO5 | |
| 14 | DIO6 | |
| 15 | DIO7 | |
| 16 | DIO8 | |

Data Input/Output

The **IEEE 488 bus** is primarily designed for connecting instrumentation to a central controller (usually a computer) for purposes of creating fully automated/data-logging measurement systems. At present some 220 different manufacturers produce equipment which is either partially or wholly IEEE 488 bus compatible.

The basic bus structure is shown in fig. c    Devices connected to the bus may be

a) A controller
b) A talker only
c) A listener only
d) A talker and a listener.

The **controller** is responsible for the overall operation of the system by issuing the appropriate commands to other devices on the bus. As might be expected any system may only have one controller, which is usually a minicomputer with data-recording facilities. A **talker only** is a peripheral which can only transmit information (e.g. a frequency counter), whilst a **listener only** can only receive information (e.g. a signal generator). A **talker and listener** can both transmit and receive information (e.g. a digital multimeter). During operation, the controller will dictate whether a given device is a talker, listener or is idle (disconnected from the bus).

Cable connector

View into female end of socket
which is similar to the socket on
an instrument's rear panel

| | | | | | | |
|---|---|---|---|---|---|---|
| Data input output 1 | DIO1 | 1 ☐ 13 | DIO5 | Data input output 5 |
| Data input output 2 | DIO2 | 2 ☐ 14 | DIO6 | Data input output 6 |
| Data input output 3 | DIO3 | 3 ☐ 15 | DIO7 | Data input output 7 |
| Data input output 4 | DIO4 | 4 ☐ 16 | DIO8 | Data input output 8 |
| End or identify | EOI | 5 ☐ 17 | REN | Remote enable |
| Data valid | DAV | 6 ☐ 18 | GND6 | |
| Not ready for data | NRFD | 7 ☐ 19 | GND7 | |
| Not data accepted | NDAC | 8 ☐ 20 | GND8 | Ground returns |
| Interface clear | IFC | 9 ☐ 21 | GND9 | for pins 6-11 |
| Service request | SRQ | 10 ☐ 22 | GND10 | |
| Attention | ATN | 11 ☐ 23 | GND11 | |
| | Shield | 12 ☐ 24 | Logic GND | |

## GPIB Connector Signal Descriptions

| Description |
|---|
| Lines DIO1 through DIO8 are used to transfer addresses, control information and data. The formats for addresses and control bytes are defined by the IEEE 488 standard. Data formats may be ASCII (with or without parity) or binary. DIO1 is the Least Significant Bit (bit 0). |
| *Attention.* This signal is asserted by the Controller to indicate that it is placing an address or control byte on the Data Bus. ATN is de-asserted to allow the assigned Talker to place status or data on the Data Bus. The Controller regains control by reasserting ATN |
| *End or Identify.* This signal has two uses as its name implies. A talker may assert EOI simultaneously with the last byte of data to indicate end of data. The Controller may assert EOI along with ATN to initiate a Parallel Poll |
| *Service Request.* This line is like an interrupt. it may be asserted by any device to request the Controller to take some action. The Controller must determine which device is asserting SRQ by conducting a Serial Poll at its earliest opportunity |
| *Interface Clear.* This signal is asserted only by the System Controller in order to initialize all device interfaces to a known state |
| *Remote Enable.* This signal is asserted only by the System Controller. Its assertion does not place devices into Remote Control mode. REN only *enables* a device to go remote when addressed to listen |
| *Not Ready For Data.* This handshake line is asserted by a listener to indicate it is not yet ready for the next data or control byte |
| *Not Data Accepted.* This handshake line is asserted by a Listener to indicate it has not yet accepted the data or control byte on the DIO lines |
| *Data Valid.* This handshake line is asserted by the Talker to indicate that a data or control byte has been placed on the DIO lines and has had the minimum specified settling time. |

### EIA RS 232C Serial Interface

The Electronics Industry Association (EIA) RS 232C interface standard allows for two full duplex data channels transmitting serial data, either synchronously or asynchronously, with or without handshake. The RS 232C (versions A and B are now obsolete) signal levels are shown in fig. **a b** · from which it should be noted that the binary 0 (also called a Space or ON condition) is more positive than the binary 1 (also called the Mark or OFF condition). This can present problems when interfacing RS 232C to TTL (a common requirement) since not only is there a considerable difference between the two signal voltage levels but the signal logic is inverted as well.

Connection between RS 232C devices is via a standard 25-pin connector (Cinch or Cannon chassis-mount, female-type DB-25S) illustrated in fig. **C** which also lists the pin connections. Unlike the IEEE 488 bus, the RS 232C interface is designed for connection between two devices only—usually a computer and a peripheral. Consequently if a computer wishes to communicate with more than one peripheral, a separate RS 232C interface must be provided for each peripheral. In addition, all RS 232C lines, unlike the IEEE 488 bus, are unidirectional, transfering data in one direction only, a factor which greatly simplifies both the hardware and software control of the interface.

Rarely is the full RS 232C standard implemented, with the majority of systems requiring only a subset of the electrical circuits. This has led to a re-defining of the RS 232C interface in terms of subsets called Level I. Level II and Level III which are defined as:

| | | |
|---|---|---|
| LEVEL I | Pin 2 Transmitted Data<br>Pin 3 Received Data | } Channel 1 |
| | Pin 7 Logical Ground | |
| | Pin 1 Protective Ground | |
| LEVEL II | Level I + | |
| | Pin 6 Data Set Ready | |
| | Pin 8 Data Carrier Detect | |
| | Pin 20 Data Terminal Ready | |
| LEVEL III | Level II + | |
| | Pin 4 Request to Send<br>Pin 5 Clear to Send | } Channel 1 |
| | Pin 22 Ring Indicator | |

Level I is normally used with equipment tied directly to each other, such as a terminal or a printer connected directly to a computer. Level II is normally used where a certain amount of handshaking is required, and is most often encountered in acoustic couplers (for transmission over a normal GPO telephone line, etc). Level III is used where a more precise and detailed control over data flow is required, such as in auto-answer modems. As such, Level III implementation may be considered as reserved for specialist equipment.
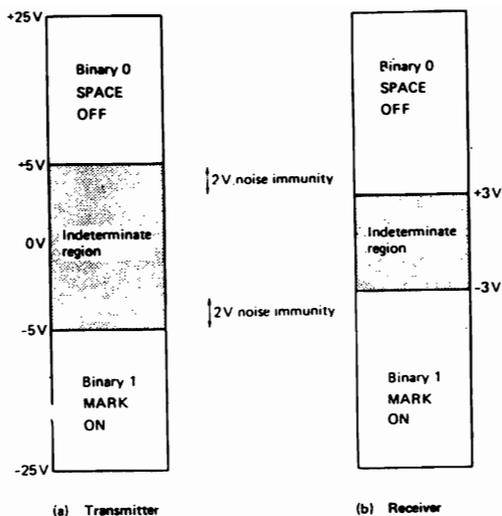
Fig. (c)  EIA RS 232C interface pin assignments

(a) Transmitter    (b) Receiver

| Pin number | Circuit Mnemonic | Description | |
|---|---|---|---|
| 1 | AA | Protective Ground | ⎫ |
| 2 | BA | Transmitted Data | |
| 3 | BB | Received Data | |
| 4 | CA | Request to Send | CHANNEL 1 |
| 5 | CB | Clear to Send | |
| 6 | CC | Data Set Ready | |
| 7 | AB | Logical Ground | ⎭ |
| 8 | CF | Data Carrier Detect | |
| 9 | — | Reserved for testing | |
| 10 | — | | |
| 11 | — | Unassigned | |
| 12 | SCF | Received Line Signal Detector | |
| 13 | SCB | Clear to Send | CHANNEL 2 |
| 14 | SBA | Transmitted Data | |
| 15 | DB | Transmitter Signal Element Timing | |
| 16 | SBB | Received Data      CHANNEL 2 | |
| 17 | DD | Receiver Signal Element Timing | |
| 18 | — | Unassigned | |
| 19 | SCA | Request to Send   CHANNEL 2 | |
| 20 | CD | Data Terminal Ready | |
| 21 | CG | Signal Quality Detector | |
| 22 | CE | Ring Indicator | |
| 23 | CH/CI | Data Signal Rate Select | |
| 24 | DA | Transmit Signal Element Timing | |
| 25 | — | Unassigned | |

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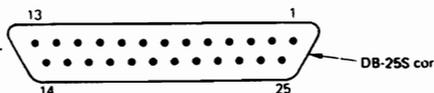
EIA Standard RS-232C is an established specification defining the logic levels and impedances at the modem/terminal interface. This has been a well-accepted standard for low data-rate systems. Maximum data rate is about 20 kilobaud.

Employing a voltage-mode type driver, RS-232C requires dual polarity logic signals and power supplies. The data is unidirectional and not condusive to party-line operation. Hysteresis is generally employed in RS-232C receivers and a single power supply is required at the receiver end. Termination is not required.
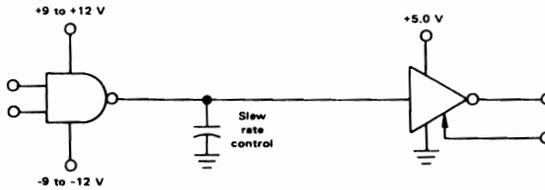


| EIA RS-232C | |
|---|---|
| Driver Output Voltage ($Z_L$ = 3 kΩ to 7 kΩ) | 15 V < $V_{OH}$ < 5.0 V<br>–5.0 V > $V_{OL}$ > –15 V |
| Driver Output Voltage ($Z_L$ = ∞) | $|v_O|$ < 25 V |
| Driver Output Impedance (Power Supplies = 0) | $z_o$ > 300 Ω |
| Driver Short-Circuit Current | $|I_O|$ < 0.5 amp |
| Driver Slew Rate | $\frac{dv}{dt}$ < 30 V/μs |
| Receiver Input Impedance | 7 kΩ > $R_{in}$ > 3 kΩ |
| Receiver Input Voltage | $|v_I|$ < 25 V |
| Receiver Output with Open Input | Mark (high) |
| Receiver Output with 300 Ω to Gnd of Input | Mark (high) |
| Receiver Output with +3.0 V on Input | Space (low) |
| Receiver Output with –3.0 V on Input | Mark (high) |
| Baud Rate | BR < 20 kilobaud |

## MC1488 — Quad RS-232C Driver, Output Current Limiting

The MC1488 is a quad inverting TTL or DTL input line driver for RS-232C. It is designed to operate on ±9 to ±12 V power supplies and at a temperature range of 0 to 70°C.

Features include guaranteed power-off output impedance and output current limiting.

Second sources available.

| $V_{OH}$ ● $V_{CC}/V_{EE}$ = ±9.0 V Volts Min | $V_{OL}$ ● $V_{CC}/V_{EE}$ = ±9.0 V Volts Max | $I_{OS}$ mA | $t_{PHL}$ ● $C_L$ = 15 pF ns Max |
|---|---|---|---|
| 6.0 | -6.0 | ±6.0 to 12 | 175 |
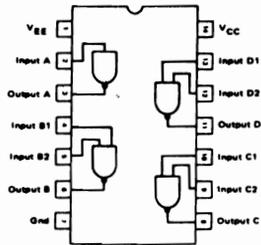
## MC1489 — Quad RS-232C Receiver, 0.25 V Input Hysteresis

The MC1489 quad inverting RS-232C receiver features 250 mV of input hysteresis. The threshold window may be shifted by means of the response control input.

Temperature range is 0 to 70°C and power supply requirement is a single +5 supply.

Second sources available.

## MC1489A — Quad RS-232C Receiver, 1.1 V Input Hysteresis

The MC1489A is an improved version of the MC1489. It features 1.1 volts of input hysteresis for improved performance when slow-slewing input signals are present in noisy environments.

Second sources are available.

| Device Number | Input $V_{IHL}$ Volts | Input $V_{ILH}$ Volts | $t_{PHL}$ ● $R_L$ = 390 Ω ns Max |
|---|---|---|---|
| MC1489 | 1.0 to 1.5 | 0.75 to 1.25 | 50 |
| MC1489A | 1.75 to 2.25 | 0.75 to 1.25 | 50 |

| Bits | 7 | | | | | 0 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1 0 0 | 1 0 1 | 1 1 0 | 1 1 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 4 | 3 | 2 | 1 | Column / Row | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| | 0 | 0 | 0 | 0 | 0 | NUL | DLE | SP | 0 | @ | P | ` | p |
| | 0 | 0 | 0 | 1 | 1 | SOH | DC1 | ! | 1 | A | Q | a | q |
| | 0 | 0 | 1 | 0 | 2 | STX | DC2 | " | 2 | B | R | b | r |
| | 0 | 0 | 1 | 1 | 3 | ETX | DC3 | # | 3 | C | S | c | s |
| | 0 | 1 | 0 | 0 | 4 | EOT | DC4 | $ | 4 | D | T | d | t |
| | 0 | 1 | 0 | 1 | 5 | ENQ | NAK | % | 5 | E | U | e | u |
| | 0 | 1 | 1 | 0 | 6 | ACK | SYN | & | 6 | F | V | f | v |
| | 0 | 1 | 1 | 1 | 7 | BEL | ETB | ' | 7 | G | W | g | w |
| | 1 | 0 | 0 | 0 | 8 | BS- | CAN | ( | 8 | H | X | h | x |
| | 1 | 0 | 0 | 1 | 9 | SKIP HT | EM | ) | 9 | I | Y | i | y |
| | 1 | 0 | 1 | 0 | 10 (a) | LF | SUB | ★ | : | J | Z | j | z |
| | 1 | 0 | 1 | 1 | 11 (b) | VT | ESC | + | ; | K | [ | k | |
| | 1 | 1 | 0 | 0 | 12 (c) | FF | FS | | | L | | l | |
| | 1 | 1 | 0 | 1 | 13 (d) | CR | GS | — | = | M | ] | m | |
| | 1 | 1 | 1 | 0 | 14 (e) | SO | HOME RS | . | | N | | n | ~ |
| | 1 | 1 | 1 | 1 | 15 (f) | SI | NEW LINE US | / | ? | O | | o | DEL RUB |
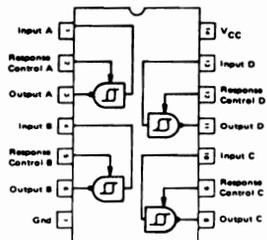
## ASCII Code Table
### Abbreviations For Control Characters

| | | | | | |
|---|---|---|---|---|---|
| NUL | null | FF | form feed | CAN | cancel |
| SOH | start of heading | CR | carriage return | EM | end of medium |
| STX | start of text | SO | shift out | SUB | substitute |
| ETX | end of text | SI | shift in | ESC | escape |
| EOT | end of transmission | DLE | data link escape | FS | file separator |
| ENQ | enquiry | DC1 | device control 1 | GS | group separator |
| ACK | acknowledge | DC2 | device control 2 | RS | record separator |
| BEL | bell | DC3 | device control 3 | US | unit separator |
| BS | backspace | DC4 | device control 4 | SP | space |
| HT | horizontal tabulation | NAK | negative acknowledge | DEL | delete |
| LF | linefeed | SYN | synchronous idle | | |
| VT | vertical tabulation | ETB | end of transmission block | | |

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# NUMBERS CONVERSION TABLE

| DECIMAL 10 | BINARY 2 | OCTAL 8 | HEXADEC 16 | $2^n$ |
|---|---|---|---|---|
| & | % | @ | $ | |
| 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 2 |
| 2 | 10 | 2 | 2 | 4 |
| 3 | 11 | 3 | 3 | 8 |
| 4 | 100 | 4 | 4 | 16 |
| 5 | 101 | 5 | 5 | 32 |
| 6 | 110 | 6 | 6 | 64 |
| 7 | 111 | 7 | 7 | 128 |
| 8 | 1000 | 10 | 8 | 256 |
| 9 | 1001 | 11 | 9 | 512 |
| 10 | 1010 | 12 | A | 1024 |
| 11 | 1011 | 13 | B | 2048 |
| 12 | 1100 | 14 | C | 4096 |
| 13 | 1101 | 15 | D | 8192 |
| 14 | 1110 | 16 | E | 16384 |
| 15 | 1111 | 17 | F | 32768 |
| 16 | 10000 | 20 | 10 | 65536 |
| 17 | 10001 | 21 | 11 | 131072 |
| 18 | 10010 | 22 | 12 | 262144 |
| 19 | 10011 | 23 | 13 | 524288 |
| 20 | 10100 | 24 | 14 | 1048576 |
| 32 | 100000 | 40 | 20 | 4294967296 |
| 50 | 110010 | 62 | 32 | – |
| 60 | 111100 | 74 | 3C | – |
| 64 | 1000000 | 100 | 40 | – |
| 100 | 1100100 | 144 | 64 | – |
| 200 | 11001000 | 310 | C8 | – |
| 255 | 11111111 | 377 | FF | – |

Ex.  & 39 = % 00100111 =   @47  = $27