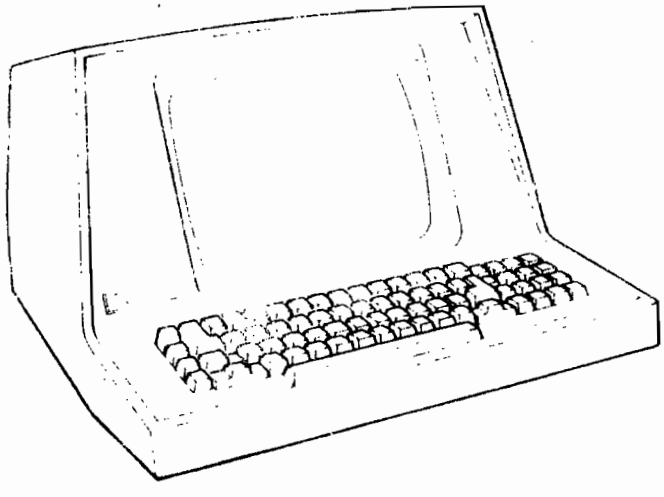
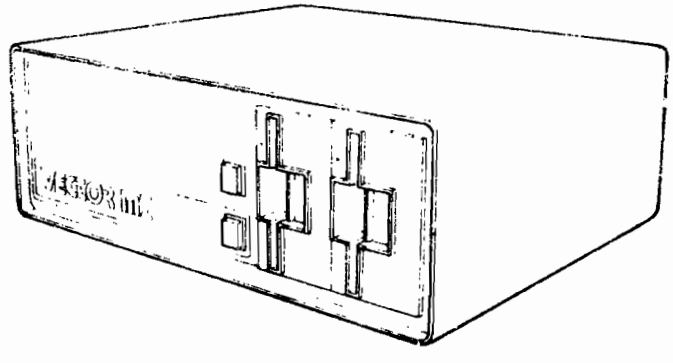
48K
Dynamic Memory Board





VECTOR GRAPHIC INC.

DYNAMIC MEMORY BOARD

Revision 3
February 7, 1979

Revision Numbers

The revision number and date of release of each page herein at the bottom of each page. The revision number and date of on the Title Page corresponds to that of the page most r revised.

Revision 3 - 2/7/78

REPAIR AGREEMENT

The 48K Dynamic RAM Board sold hereunder is sold "as is", with all faults and without any warranty, either expressed or implied, including any implied warranty of fitness for intended use or merchantability. However, the above notwithstanding, VECTOR GRAPHIC, INC., will, for a period of ninety (90) days following delivery to customer, repair or replace any 48K Dynamic RAM Board that is found to contain defects in materials or workmanship, provided:

1. Such defect in material or workmanship existed at the time the 48K Dynamic RAM Board left the VECTOR GRAPHIC, INC., factory;
2. VECTOR GRAPHIC, INC., is given notice of the precise defect claimed within ten (10) days after its discovery;
3. The 48K Dynamic RAM Board is promptly returned to VECTOR GRAPHIC, INC., at customer's expense, for examination by VECTOR GRAPHIC, INC., to confirm the alleged defect, and for subsequent repair or replacement if found to be in order.

Repair, replacement or correction of any defects in material or workmanship which are discovered after expiration of the period set forth above will be performed by VECTOR GRAPHIC, INC., at Buyer's expense, provided the 48K Dynamic RAM Board is returned, also at Buyer's expense, to VECTOR GRAPHIC, INC., for such repair, replacement or correction. In performing any repair, replacement or correction after expiration of the period set forth above, Buyer will be charged in addition to the cost of parts the then-current VECTOR GRAPHIC, INC., repair rate. At the present time the applicable rate is $35.00 for the first hour, and $18.00 per hour for every hour of work required thereafter. Prior to commencing any repair, replacement or correction of defects in material or workmanship discovered after expiration of the period for no-cost-to-Buyer repairs, VECTOR GRAPHIC, INC., will submit to Buyer a written estimate of the expected charges, and VECTOR GRAPHIC, INC., will not commence repair until such time as the written estimate of charges has been returned by Buyer to VECTOR GRAPHIC, INC., signed by duly authorized representative authorizing VECTOR GRAPHIC, INC., to commence with the repair work involved. VECTOR GRAPHIC, INC., shall have no obligation to repair, replace or correct any 48K Dynamic RAM Board until the written estimate has been returned with approval to proceed, and VECTOR GRAPHIC, INC., may at its option also require prepayment of the estimated repair charges prior to commencing work.

Repair Agreement void if the enclosed card is not returned to VECTOR GRAPHIC, INC. within ten (10) days of end consumer purchase.

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I. INTRODUCTION

1.1 Description of the Board

The Vector Graphic 48K Dynamic Memory Board provides 49,152 8-bit bytes of random access memory, using 24 16K dynamic memory chips. It can be used in ANY S-100 bus computer using a Z-80 CPU board. (Minor modifications may be necessary. See Section III, "User's Guide", below.). It occupies the lower 48K of memory, i.e. beginning at 0000H.

The Vector Graphic 48K Dynamic Memory Board is clearly a breakthrough in cost effectiveness. This is accomplished by combining compact inexpensive dynamic memory chips with the use of the refresh provisions of the Z-80 CPU. The most recent static RAM boards cost considerably more, take up more space, and require more power. Other dynamic memory boards use complex support logic on the board, rather than the built in features of the Z-80.

In addition to the above features, the Vector Graphic Dynamic Memory Board has proven to be remarkably reliable. Considerable attention was given during design of the board to the elimination of noise. It features a gridded ground plane designed to reduce noise. Accepted design practice was observed in structuring grounds, power supply, and bypass.

1.2 Description of the Manual

This manual provides a general description of the Vector Graphic Dynamic Memory Board, a more detailed discussion of the theory of operation, and information on how to use and test the board. Since the board is not sold as a kit, assembly information and parts list are not included.

II. THEORY OF OPERATION

2.1 The 48K Board Circuitry

The Vector Graphic 48K Dynamic Memory Board uses the refresh provisions of the Z-80 CPU board, which greatly simplifies the support logic circuitry on the board.

A memory reference cycle begins with the CPU board sending the address over A0-A15. Each of the memory chips contains 16K bits, so 14 address bits must be supplied to the chips. This is done by time multiplexing 7 address inputs. Initially the low order 7 addresses are applied to the chip address inputs by U39. After the address lines have had time to settle, the CPU board issues a memory read signal on SMEMR or a write signal in MWRITE. This signal propagates down a chain of inverters in U13 to initiate a timing sequence which does the following things in order:

1. Generates a low going $\overline{\text{RAS}}$ strobe for the appropriate memory block which is selected by U35 and gates U11 and U23. This strobe latches the address bits internally in the memory chips.

2. Disables U39, a tri state driver.

3. Enables U38, applying the high order 7 address lines to the chips.

4. Generates a low going $\overline{\text{CAS}}$ strobe which latches the addresses in the memory chips and initiates a timing sequence in the chip to enable the output drivers if it is a read cycle, or to write the data into the selected memory location if it is a write cycle.

If the cycle is a read cycle or M1 cycle, the logic associated with U43 enables the bus driver U41 to place the memory data on the DI bus to be read by the CPU. If the cycle is a write cycle, data on the DO bus is buffered by U40 and made available at the data input pin of the chips. The 74LS244 chips have Schmitt trigger inputs to discriminate against noise.

The principal difference between static and dynamic memory is the need to refresh the data stored in a dynamic memory. This is necessary because each bit of data is represented by an electric charge stored on a capacitor in each memory "cell". This charge will gradually leak away due to the finite insulation resistance of the dielectric. In order to restore the amplitude of the charge, it must be periodically read out, amplified, and written back in the same location. This is accomplished, thanks to the ingenuity of the chip designers, by executing a $\overline{\text{RAS}}$ only memory cycle for each of the 128 row addresses within a 2 millisecond interval. In other dynamic

memory boards, this is done using counters, multiplexers and complicated priority resolving circuitry to interleave refresh cycles with CPU access cycles.

2.2 The Refresh Feature of the Z-80 Board

Fortunately, the designers of the Z-80 provided for this requirement by including a 7 bit refresh counter in the chip which is incremented every M1 cycle and by designing the chip to output the count on the address bus during every M1 cycle at a point in time when the address bus is idle. The Vector Graphic Z-80 board outputs a $\overline{\text{RFSH}}$ signal on pin 66 of the bus to indicate that a refresh cycle must be initiated. The timing of this signal is modified by U24 and reclocked by the system clock to satisfy the timing requirements of the memory chips. The output of U23 pin 8 is combined in U11 to generate a RAS strobe which is applied to all chips during the refresh cycle.

There are several conditions under which the normal refresh sequence will be interrupted which could result in loss of memory data.

1. if the CPU is held in a wait state for 2 mS or longer.

2. if a DMA device takes control of the bus for more than 2 mS without generating the necessary refresh signals.

3. if the CPU is held in a reset condition for more than 2 mS.

Condition 1 would not occur in a Vector Graphic computer, but can occur in a system with a front panel where the READY line is used to HALT program execution. There are other ways in which this can occur since the READY line is a popular way of suspending CPU operation. Caution should be exercised with PROM programming boards, which typically hold the CPU in a wait state of 600 micro-seconds during a programming pulse. See Section III, "User's Guide," for information on handling this problem with PROM programmers. Other common uses of the READY line are to synchronize disk transfers and to prevent video display glitching. These last two are usually not a problem due to the relatively short wait period, on the order of a few microseconds.

Condition 2 does not occur in a Vector Graphic computer since none of the boards use DMA. If you are using DMA along with the 48K board, the DMA must not interrupt the CPU for longer than 2 ms without generating the necessary refresh signals.

Condition 3 has been eliminated by providing additional circuitry on the memory board to generate a short reset pulse synchronized with a M1 cycle. This consists of an RC network C8, R12, R11, to condition the $\overline{\text{PRESET}}$ signal connected to the front panel reset switch. Grounding $\overline{\text{PRESET}}$ allows U1 to be set by the next M1 cycle (memory

cycles can not be interrupted without loss of data). U1 triggers U2 generating a 200 micro-second pulse to pull unused bus line 55 low through the open collector inverters in U14. If you purchased the 48K board as a separate board, not as part of a complete Vector Graphic computer, you will have to make certain minor modifications to your Z-80 CPU board so that the Reset circuit responds to the signal coming from the 48K board on pin 55. These modifications are described in the User's Guide (Section III of this manual.) Vector Graphic computers shipped with the 48K board will have the modifications made at the factory.

III. USER'S GUIDE

3.1 Modifications to the 48K Board and Z-80 Board

This section is concerned with making modifications to the jumpers on the 48K board and CPU board in order to use the 48K board in existing systems. If your system is a Vector Graphic computer such as the MZ, MEMORITE, or Vector 3, which was shipped with the 48K board, no changes are required to either board.

1. REFRESH SIGNAL - Jumpers can be installed to provide the proper RFSH signal, making use of the signal presently coming from your CPU. This is to ensure that a refresh cycle is generated during every instruction fetch cycle. Without this signal, operation is not possible.

2. RESET CIRCUITRY - Modifications can be made to the reset circuit of the CPU board so that it responds to the short reset pulse generated by the 48K RAM board on pin 55 rather than the $\overline{\text{PRESET}}$ signal on pin 75. This modification is optional. It is to prevent the CPU from being held in a reset state for longer than 2 milliseconds which would result in loss of memory data, since the memory is not being refreshed while the CPU is in a reset state.

The above two modifications are discussed in detail below:

3.1.1 Refresh Signal

If you are using the 48K board with a non-Vector Graphic CPU board, refer to the manual for your CPU board to determine if the polarity and pin connection of the $\overline{\text{RFSH}}$ signal are correct. This signal is generated by pin 28 of the Z-80 CPU chip and should be buffered onto pin 66 of the bus using a non-inverting buffer of the 8097 or 74367 type. If this is not the case, it is necessary to modify the jumper arrangement on the 48K board. Area C on the board allows for inverting the polarity of the $\overline{\text{RFSH}}$ signal if it is inverted on the CPU board. Cut the trace between pad 2 and pad 1 and connect a jumper between pad 3 and pad 1. If the $\overline{\text{RFSH}}$ signal is brought to pin 98 on the bus instead of pin 66, a pad is provided on the 48K board. Cut the trace in area A to pin 66 and install a jumper to pin 98.

3.1.2 Reset Circuitry

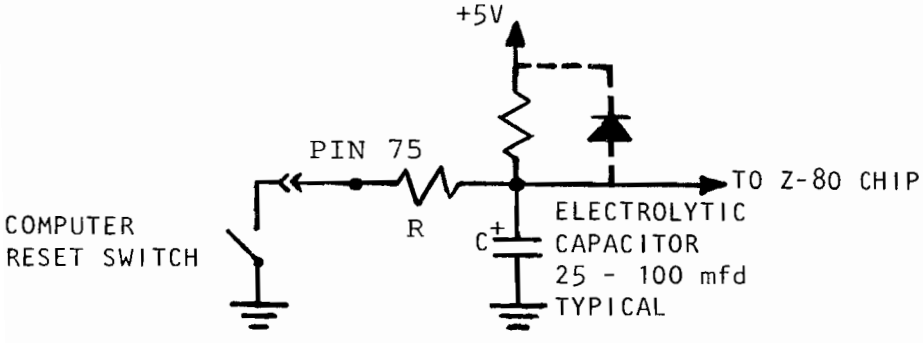
The purpose of this modification is to allow the short (about 200 microseconds) pulse generated by the 48K board on pin 55 (previously unused) to reset the CPU, rather than using the $\overline{\text{PRESET}}$ signal

generated on pin 75 by the Reset switch. The signal on pin 55 is activated by the front panel Reset switch. As described below, there are two different versions of this modification:

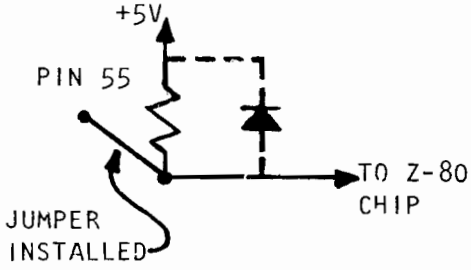
Non-Vector Graphic Z-80 Boards and Vector Graphic Revision 1 Z-80 Boards

The modification described below is applicable to all existing computer systems, including systems using the Vector Graphic Revision 1 Z-80 Board (which includes all existing Vector Graphic computers shipped with static RAM boards.)

A typical Reset circuit on a Z-80 CPU board and the necessary modifications are shown below:



ORIGINAL CIRCUIT



MODIFIED CIRCUIT

Remove the Resistor R and Capacitor C from the board. Then connect a jumper from pin 55 to the pad previously connected to the + end of the capacitor.

Vector Graphic Z-80 Boards

This version of the modification is relevent to any existing computer, including Vector Graphic computers, using a Vector Graphic Z-80 CPU board. Install a jumper between pin 55 and the junction of the 220 ohm and 180 ohm resistor connected to the emitter of the 2N3643 transistor. This junction will be found near the upper right-hand corner of the schematic. Pads are provided on Revision 2 of the Z-80 board, but are not provided on Revision 1. Then, remove the 100 ohm resistor and the capacitor which are connected to pin 75.

3.2 The READY Line

If the CPU is held in a wait state for 2 mS or longer, the normal refresh sequence will be interrupted which could result in the loss of memory data. Since computers with a front panel use the READY line to HALT program operation, if your computer has a front panel, you may NOT use the front panel when the 48K Board is being used. If you do, the system will bomb.

Caution should also be exercised with PROM programming boards, which typically hold the CPU in a wait state of 600 micro-seconds during a programming pulse. After every byte programmed, a software loop should execute 128 instructions to ensure refresh. A typical loop is as follows:

```
        PUSH B
        MVI  B,80H
LOOP    DJNZ LOOP
        POP  B
```

Other common uses of the READY line are to synchronize disk transfers and to prevent video display glitching. These last two are usually not a problem due to the relatively short wait period, on the order of a few microseconds.

3.3 Using DMA

If you are using DMA along with the 48K board, the DMA must not interrupt the CPU for longer than 2 mS without generating the necessary refresh signals.

3.4 Address of the Board

The 48K RAM board is designed to occupy the lower 48K of address space. No provision has been made to change this. For this reason, you will not find any references in this manual to the method of specifying the address of the board.

3.5 Memory test

This section is relevent if you are using a Vector Graphic computer, or at least a Vector Graphic 12K PROM/RAM board in addition to the 48K board.

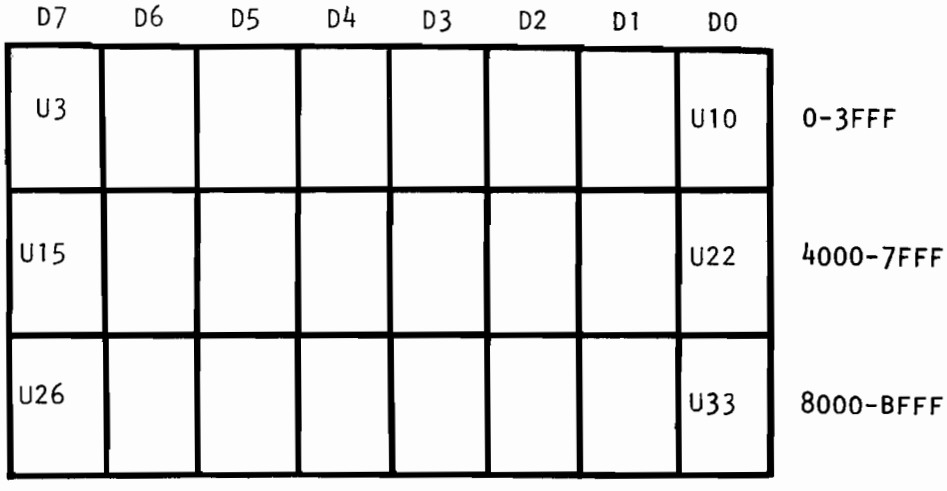
The 48K board can be tested using the Vector Graphic Extended Monitor T command. Install the board in your system and turn the system on. Type T 0000 C000. After a few seconds C000 XX C3 should appear on the terminal indicating that location C000 (the first PROM

location) could not be written to. The test will automatically repeat, and no addresses other than C000 should be printed out. Depress the RESET key on the front panel to terminate the test.

A more thorough test can be made using the MDIAG program supplied on the Vector MZ system diskette. Refer to Appendix J of the MZ User's Manual.

SPECIFICATIONS

Capacity:	49,152 8-bit bytes
Buffering:	Buffered data input and output
Access Time:	Compatible with Z-80 at 4MHZ without wait states
Power Consumption:	0.25A of +8V and 0.20A of +16V, typical
$\overline{\text{Phantom}}$:	Ouput buffer disable compatible with Vector Graphic PROM/RAM (Reset and Go) Board
DMA:	Must not interrupt the CPU for longer than $2X10^{-3}$ seconds without generating the necessary refresh signals
Availability:	Shipped assembled, tested, burned in, and guaranteed 1 year; no kits



48K DYNAMIC MEMORY CHIP LOCATIONS

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

74LS244

TO ALL CHIPS IN PARALLEL

TOP ROW Vcc +5V, -5V

BOTTOM ROW +12V

RIGHT SIDE

LEFT SIDE

U21 MEMORY ARRAY 8 X 3 16K CHIPS MK 4116-3

74LS244 U40

74LS244 U41

74LS00

74LS14

74LS02

74LS74

74LS75 U35

74121 U2

7406 U14

LS00 U34

LS02 U42

LS13 U43

INVERTED NORMAL

RESET CIRCUIT

HEAT SINK 7805 U12 +5V

HEAT SINK 7812 U25 +12V

7905 U37 -5V

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: DECIMALS .XX ± .02 .XXX ± .010 ANGLES ±½°	CONTRACT NO.
MATERIAL	APPROVALS / DATE
FINISH	DRAWN GEO. M. STROUD
NEXT ASSY / USED ON	CHECKED R. HARP 11/30/78
APPLICATION	DO NOT SCALE DRAWING

VECTOR GRAPHIC

48K DYNAMIC MEMORY MODULE

REV - 2

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SCALE | SHEET OF

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A7872