VECTOR MZ5

HARDWARE MANUAL

REFERENCE GUIDE

Revision A

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REPAIR AGREEMENT

The MZ5 sold hereunder is sold "as is", with all faults and without any warranty, either expressed or implied, including any implied warranty of fitness for intended use or merchantability. However, the above notwithstanding, VECTOR GRAPHIC, INC., will, for a period of ninety (90) days following delivery to customer, repair or replace any MZ5 that is found to contain defects in materials or workmanship, provided:

1. Such defect in material or workmanship existed at the time the MZ5 left the VECTOR GRAPHIC, INC., factory;
2. VECTOR GRAPHIC, INC., is given notice of the precise defect claimed within ten (10) days after its discovery;
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Repair, replacement or correction of any defects in material or workmanship which are discovered after expiration of the period set forth above will be performed by VECTOR GRAPHIC, INC., at Buyer's expense, provided the MZ5 is returned, also at Buyer's expense, to VECTOR GRAPHIC, INC., for such repair, replacement or correction. In performing any repair, replacement or correction after expiration of the period set forth above, Buyer will be charged in addition to the cost of parts the then-current VECTOR GRAPHIC, INC., repair rate. At the present time the applicable rate is $35.00 for the first hour, and $18.00 per hour for every hour of work required thereafter. Prior to commencing any repair, replacement or correction of defects in material or workmanship discovered after expiration of the period for no-cost-to-Buyer repairs, VECTOR GRAPHIC, INC., will submit to Buyer a written estimate of the expected charges, and VECTOR GRAPHIC, INC., will not commence repair until such time as the written estimate of charges has been returned by Buyer to VECTOR GRAPHIC, INC., signed by duly authorized representative authorizing VECTOR GRAPHIC, INC., to commence with the repair work involved. VECTOR GRAPHIC, INC., shall have no obligation to repair, replace or correct any MZ5 until the written estimate has been returned with approval to proceed, and VECTOR GRAPHIC, INC., may at its option also require prepayment of the estimated repair charges prior to commencing work.

Repair Agreement void if the enclosed card is not returned to VECTOR GRAPHIC, INC. within ten (10) days of end consumer purchase.

FOREWORD

Audience

This manual is intended for computer distributors, or others with at least a moderate technical knowledge of small computers.

Scope

It will describe what the Vector Graphic MZ5 does in the context of a subsystem of other Vector microcomputer syste It considers the power supply, motherboard and chassi general. It does not cover any of the disk drive subassemblies. The manual describes the hardware and its function and provides procedures for troubleshooting, testing and adjusting the subject components.

Organization

This manual is divided into 4 parts. "Perspective" describes how the MZ5 fits into the Vector product line. "Mainframe" explains the function of the main subassemblies. "Troubleshooting" shows how to test the power supply and motherboard to assure they are providing the correct voltages to the circuit boards. "Appendix" contains a listing of the S-100 bus pins, illustrations of the chassis components and schematics showing the circuitry of the power assembly and disk regulator board.

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SPECIFICATIONS

POWER

For one unit (5005 configuration for three users)

Voltage option	115 VAC ±10%	220 VAC ±10%
Frequency	60 Hz ±.5%	50 Hz ±.5%
Current, Operating	3 Amps	1.5 Amps
Current, Surge	15 Amps	7.5 Amps

DIMENSIONS AND WEIGHT*

	Height inches/cm	Depth inches/cm	Width inches/cm	Weight lbs/kg
Mainframe	7.5/18.0	16.75/42.5	20.5/52	43.2/19.6

* Does not include requirements for cabling (typically 4 in./10.2 cm)

ENVIRONMENT

	Operating	Storage
Temperature	10 to 32° C	-34 to 65° C
Humidity (non-condensing)	20-80%	20-80%

I. PERSPECTIVE

The Vector MZ5 serves as the mainframe for the 3105 and 5005 Vector Graphic computer systems. The advantage of purchasing an MZ5 based system lies in the units expandability. When shipped as part of the 3105 system only 4 of the motherboards 18 connectors are occupied. This allows 14 additional boards to be inserted for future expansion. For example, you could include boards for video based systems or expanded memory systems.

The MZ5 Hardware Manual covers the hardware components contained within the MZ5 chassis with the exception of the disk drive units. This includes the Mainframe, Power Supply, and the Motherboard.

For information on other components see the specific hardware manual. For information on installation, use, and maintenance of a System printer as part of an MZ5 based system, see the NEC 7700Q manual that comes with the printer.

II. MAINFRAME

The Vector MZ5 Mainframe's front panel (see Appendix A.2) contains a POWER keyswitch and a RESET button (connected to pin 75 and ground on S-100), along with a disk drive subsystem. Current configurations include:

1. 3105 : One Seagate 5-1/4" hard disk drive, one Tandon 5-1/4" double-sided floppy disk drive, and one Dualmode Disk Controller, one Flashwriter II, one ZCB, and one 64K Dynamic RAM memory boards.

3. 5005 : Same drives as used in 3105 with one Dualmode Disk Controller, one Flashwriter II, one ZCB, one 64K Dynamic RAM memory and one Bitstreamer II boards. For each additional user another pair of Flashwriter and 64K RAM boards is added (up to five users can be serviced by one MZ5 mainframe).

The boards used in the 5005 system are modified for a multi-user environment. These modifications are discussed in the 5005 SYSTEMS OVERVIEW MANUAL.

On the backpanel of the MZ5 (see Appendix A.3) is found a fuse holder, a plug for AC power and an accessory AC receptacle. The backpanel also has a RS-232C connector and the appropriate number of Mindless Terminal connectors.

Mounted on the inside of the MZ5 backplane is a fan assembly. When replacing the fan assembly, make sure that the flow of air is moving out of the mainframe to the rear, and not being sucked into the mainframe. Also on the inside of the mainframe is the power supply module (see Appendix A.5), disk regulator assembly (see Appendix A.6) and an 18-slot motherboard based on the S-100 bus (see Appendix A.4).

2.1 Power Supply

The Vector MZ5 Power Supply is located on the inside of the mainframe. It consists of two 28,000 uF computer grade capacitors, a 60,000 uF computer grade capacitor, two bridge rectifiers and a 110V/220V switchable transformer. Instructions on how to rewire the transformer for a different source voltage are found on the power supply schematic in the Appendix of this manual. The MZ5 Power Supply provides +8, +16, and -16 VDC unregulated power to the computers Motherboard, the Mindless Terminal, and the Disk Drives Regulator Board. NOTE: In order to attach a printer it is necessary that the printer have an independent power supply.

2.2 Motherboard

All S-100 boards used in Vector Microcomputer Systems send and receive bus signals via the S-100 bus assembly on the Motherboard located in the MZ5 Mainframe (see Appendix A.4).

The Motherboard contains 18 slots and can accomodate all the boards used in various Vec Systems. Since all boards access the same S-100 bus signals from the Motherboard, they can be arranged in any desired sequence, contiguous or noncontiguous. The Motherboard is supplied with bus terminators so full-time termination is provided.

2.3 S-100 Bus Termination

The bus terminators provided on the Motherboard are 220 ohm pull-up (to +5V) and 330 ohm pull-down (to GND). See Appendix A.1.

TABLE 1
LINES TERMINATED

24 - 2	38 - DO4	76 - PSYNC	86 - A14
25 - 1	39 - DO5	77 - PWR	87 - A11
29 - A5	40 - DO6	78 - PDBIN	88 - D02
30 - A4	41 - D12	79 - A0	89 - DO3
31 - A3	42 - D13	80 - A1	90 - D07
32 - A15	43 - D17	81 - A2	91 - D14
33 - A12	47 - SMEMR	82 - A6	92 - D15
34 - A9	49 - CLK	83 - A7	93 - D16
35 - DO1	54 - EXT CLR	84 - A8	94 - D11
36 - DO6	66 - RFSH	85 - A13	95 - D10
37 - A10	68 - MWRITE		

III. TROUBLESHOOTING

3.1 Troubleshooting the Power Supply

This section is provided for reference. The MZ5 mainframe has been completely tested at the factory.

WARNING

This power supply uses 110V AC, which is a potentially lethal voltage level. Extreme caution must be exercised when working with these circuits when power is applied. It is suggested that the user always keep one hand in his pocket while working with the power supply. Never make ohmmeter or continuity measurements while the power is applied.

3.2 Preliminary Checkout (Without Power)

WARNING

Do not apply power during these tests as high voltages are present.

Review Power Supply schematic diagram to ensure that the power supply is wired correctly. Check all connectors for mechanical integrity, such as the screw terminals on the electrolytic capacitors and the motherboard. A loose or unterminated wire can cause serious damage to the computer and present a safety hazard to the user.

Using an ohmmeter, check the continuity between the linecord receptacle ground terminal and the negative terminal of either of the 28,000 uF capacitors. Continuity (0 ohms) should be indicated between these points. Now measure from the capacitor to some bare metal portion of the chassis. Continuity should also be indicated here.

With the ohmmeter on the X1 scale, measure across the 60,000 uF capacitor. If a short indicated, reverse the leads of the ohmmeter and repeat the measurement. The cor

indication of the ohmmeter will be a slowly increasing value of resistance (in the order of minutes) to a final value of infinity. If a short is indicated at both times, then either the capacitor is shorted or there is a wiring error.

Repeat the above test on each of the two 28,000 uF capacitors. The final value of resistance for these tests should be 820 ohms +/-20%. Therefore, adjust the scale of the ohmmeter accordingly. The response time will be much shorter for these capacitors.

3.3 Preliminary Checkout (With Power)

Before applying power to the computer, remove all plug-in circuit boards. Ensure that the fuse is installed and that the power switch is off. Connect the AC linecord and turn on the power switch. Listen for any crackling sounds or very loud buzzing in the transformer. Immediately disconnect power by unplugging the linecord if any unusual sounds are noted or if arcing or smoke is apparent.

Correct operation of the power supply shall be indicated by the fan running and the RESET light lit. Using a voltmeter, check each of the power supply voltages. They should read as follows:

Nominal Voltage	Acceptable Limits
+8 Volts	7.5 to +11 Volts
+16 Volts	+15 to +20 Volts
-16 Volts	-15 to -20 Volts

Any voltage reading out of the acceptable limits indicates a failure in that circuit. The most likely failures, after wiring errors have been eliminated, are defective rectifiers or transformer.

After the voltages have been tested at the power supply, carefully check for these voltages on the motherboard. They can be found on the following pins:

Bus Voltage	Bus Pin
+8 Volts	1, 51
+16 Volts	2
-16 Volts	52
GND	50, 100

Incorrect reading here could damage circuit boards when they are installed. If any wrong voltages are found, carefully check wiring to the motherboard.

APPENDIX A - ILLUSTRATIONS AND SCHEMATICS

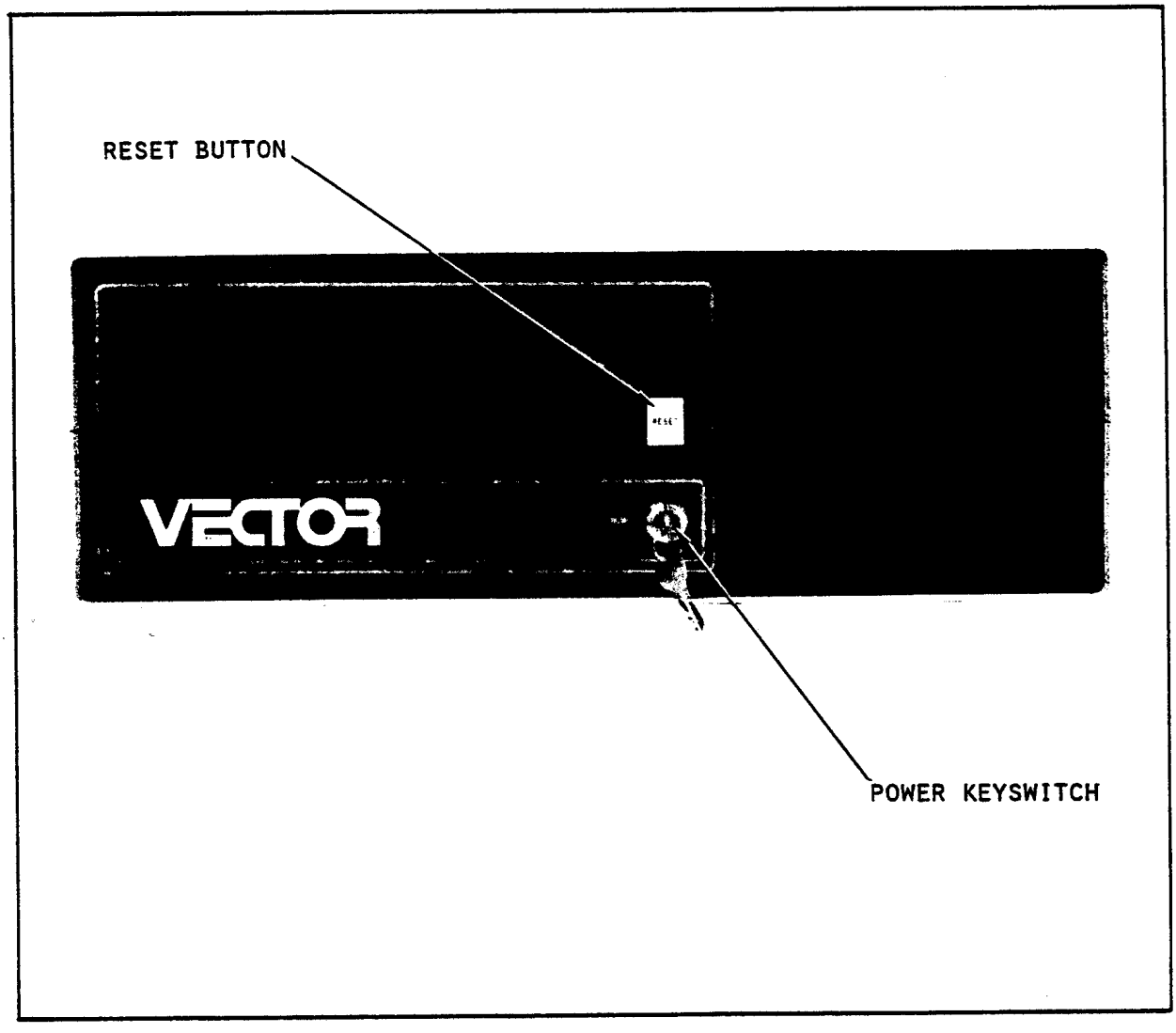
A.1 S-100 Bus Pin List

S-100 Bus Pin List

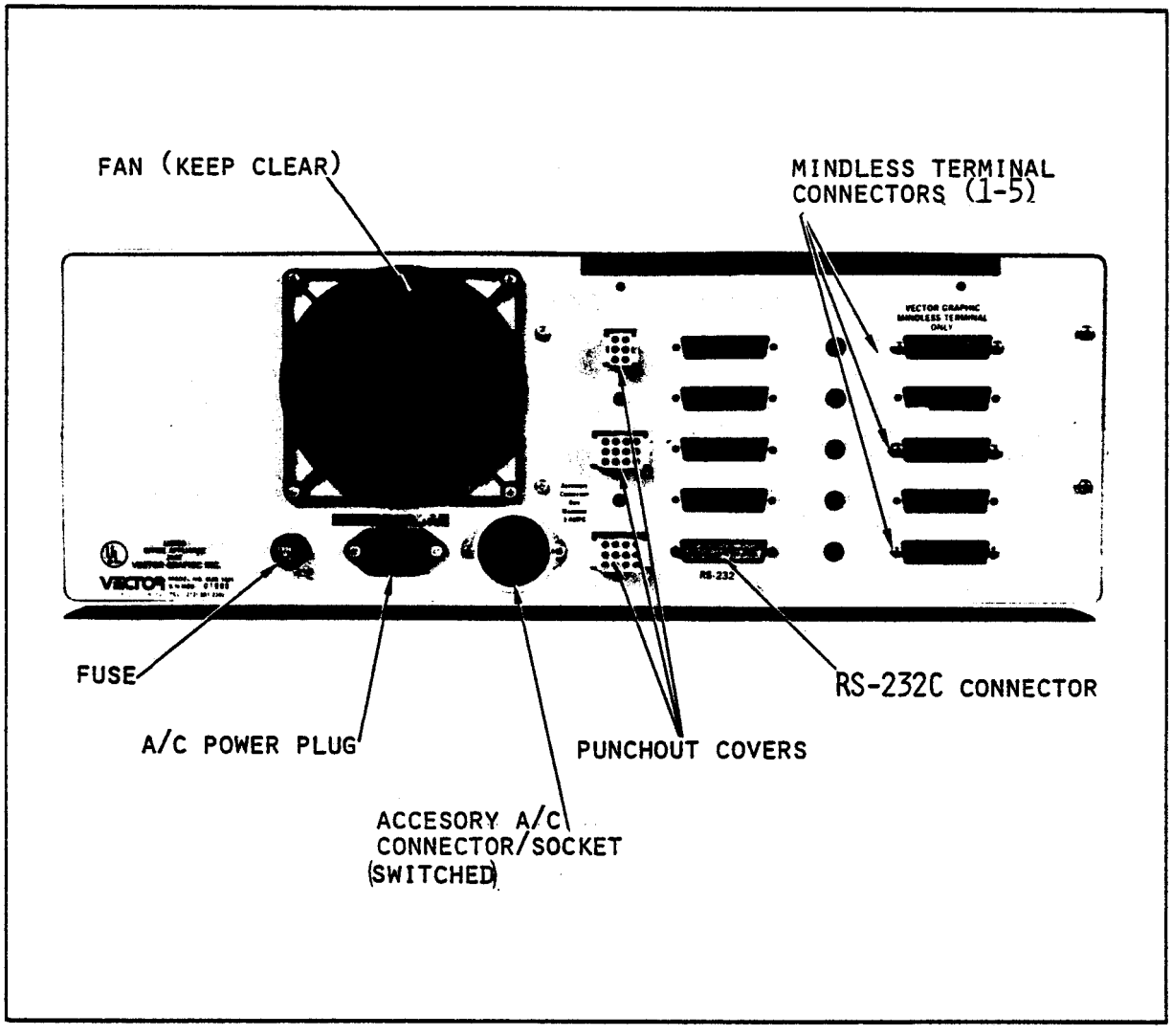
PIN NO.	SIGNAL & TYPE	ACTIVE LEVEL		DESCRIPTION
1	+8 VOLTS (B)			Instantaneous minimum greater than 7 volts, instantaneous maximum less than 25 volts, average maximum less than 11 volts.
2	+16 VOLTS (B)			Instantaneous minimum greater than 14.5 volts, instantaneous maximum less than 35 volts, average maximum less than 21.5 volts.
3	XRDY (S)	H		One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true. See pin 72.
4	VI0*(S)	L	O.C.	Vectored interrupt line 0.
5	VI1*(S)	L	O.C.	Vectored interrupt line 1.
6	VI2*(S)	L	O.C.	Vectored interrupt line 2.
7	VI3*(S)	L	O.C.	Vectored interrupt line 3.
8	VI4*(S)	L	O.C.	Vectored interrupt line 4.
9	VI5*(S)	L	O.C.	Vectored interrupt line 5.
10	VI6*(S)	L	O.C.	Vectored interrupt line 6.
11	VI7*(S)	L	O.C.	Vectored interrupt line 7.
12	NMI*(S)	L	O.C.	Non-maskable interrupt.
13				
14				
15	A18 (M)	H		Extended address bit 18.
16	A16 (M)	H		Extended address bit 16.
17	A17 (M)	H		Extended address bit 17.
18	SDSB* (M)	L	O.C.	The control signal to disable the 8 status signals.
19	CDSB* (M)	L	O.C.	The control signal to disable the 5 control output signals.
20	GND (B)			Common with pin 100.
21	NDEF			Not to be defined. Manufacturer must specify any use in detail.
22	ADSB* (M)	L	O.C.	The control signal to disable the 16 address signals.
23	DODSB* (M)	L	O.C.	The control signal to disable the 8 data output signals.
24	Φ (B)	H		The master timing signal for the bus.
25	pSTVAL*(M)	L		Status valid strobe.
26	pHLDA (M)	H		A control signal used in conjunction with HOLD* to coordinate bus master transfer operations.
27	RFU			Reserved for future use.
28	RFU			Reserved for future use.
29	A5 (M)	H		Address bit 5.
30	A4 (M)	H		Address bit 4.
31	A3 (M)	H		Address bit 3.
32	A15 (M)	H		Address bit 15 (most significant for non-extended addressing.)
33	A12 (M)	H		Address bit 12.
34	A9 (M)	H		Address bit 9.
35	DO1 (M)/DATA1 (M/S)	H		Data out bit 1, bidirectional data bit 1.
36	DO0 (M)/DATA0 (M/S)	H		Data out bit 0, bidirectional data bit 0.
37	A10 (M)	H		Address bit 10.
38	DO4 (M)/DATA4 (M/S)	H		Data out bit 4, bidirectional data bit 4.
39	DO5 (M)/DATA5 (M/S)	H		Data out bit 5, bidirectional data bit 5.
40	DO6 (M)/DATA6 (M/S)	H		Data out bit 6, bidirectional data bit 6.
41	DI2 (S)/DATA10 (M/S)	H		Data in bit 2, bidirectional data bit 10.
42	DI3 (S)/DATA11 (M/S)	H		Data in bit 3, bidirectional data bit 11.
43	DI7 (S)/DATA15 (M/S)	H		Data in bit 7, bidirectional data bit 15.
44	sM1 (M)	H		The status signal which indicates that the current cycle is an op-code fetch.
45	sOUT (M)	H		The status signal identifying the data transfer bus cycle to an output device.
46	sINP (M)	H		The status signal identifying the data transfer bus cycle from an input device.
47	sMEMR (M)	H		The status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycle(s).
48	sHLTA (M)	H		The status signal which acknowledges that a HLT instruction has been executed.
49	CLOCK(B)			2 MHz (0.5%) 40-60% duty cycle. Not required to be synchronous with any other bus signal.
50	GND (B)			Common with pin 100.
51	+8 VOLTS (B)			Common with pin 1.
52	-16 VOLTS (B)			Instantaneous maximum less than -14.5 volts, instantaneous minimum greater than -35 volts, average minimum greater than -21.5 volts.
53	GND (B)			Common with pin 100.
54				
55	FAST RESET			

PIN NO.	SIGNAL & TYPE	ACTIVE LEVEL		DESCRIPTION
56				
57				
58	sXTRQ* (M)	L		The status signal which requests 16-bit slaves to assert SIXTN*.
59	A19 (M)	H		Extended address bit 19.
60	SIXTN* (S)	L	O.C.	The signal generated by 16-bit slaves in response to the 16-bit request signal sXTRQ*.
61	A20 (M)	H		Extended address bit 20.
62	A21 (M)	H		Extended address bit 21.
63	A22 (M)	H		Extended address bit 22.
64	A23 (M)	H		Extended address bit 23.
65	NDEF			Not to be defined signal.
66	NDEF			Not to be defined signal.
67	PHANTOM*(M/S)	L	O.C.	A bus signal which disables normal slave devices and enables phantom slaves—primarily used for bootstrapping systems without hardware front panels.
68	MWRT (B)	H		pWR• — sOUT (logic equation). This signal must follow pWR* by not more than 30 ns. (See note, Section 2.7.5.3)
69	RFU			Reserved for future use.
70	GND (B)			Common with pin 100.
71	RFU			Reserved for future use.
72	RDY (S)	H	O.C.	See comments for pin 3.
73	INT* (S)	L	O.C.	The primary interrupt request bus signal.
74	HOLD* (M)	L	O.C.	The control signal used in conjunction with pHLDA to coordinate bus master transfer operations.
75	RESET*(B)	L	O.C.	The reset signal to reset bus master devices. This signal must be active with POC* and may also be generated by external means.
76	pSYNC (M)	H		
77	pWR* (M)	L		The control signal signifying the presence of valid data on DO bus or data bus.
78	pDBIN (M)	H		The control signal that requests data on the DI bus or data bus from the currently addressed slave.
79	A0 (M)	H		Address bit 0 (least significant).
80	A1 (M)	H		Address bit 1.
81	A2 (M)	H		Address bit 2.
82	A6 (M)	H		Address bit 6.
83	A7 (M)	H		Address bit 7.
84	A8 (M)	H		Address bit 8.
85	A13 (M)	H		Address bit 13.
86	A14 (M)	H		Address bit 14.
87	A11 (M)	H		Address bit 11.
88	DO2 (M)/DATA2 (M/S)	H		Data out bit 2, bidirectional data bit 2.
89	DO3 (M)/DATA3 (M/S)	H		Data out bit 3, bidirectional data bit 3.
90	DO7 (M)/DATA7 (M/S)	H		Data out bit 7, bidirectional data bit 7.
91	DI4 (S)/DATA12 (M/S)	H		Data in bit 4 and bidirectional data bit 12.
92	DI5 (S)/DATA13 (M/S)	H		Data in bit 5 and bidirectional data bit 13.
93	DI6 (S)/DATA14 (M/S)	H		Data in bit 6 and bidirectional data bit 14.
94	DI1 (S)/DATA9 (M/S)	H		Data in bit 1 and bidirectional data bit 9.
95	DI0 (S)/DATA8 (M/S)	H		Data in bit 0 (least significant for 8-bit data) and bidirectional data bit 8.
96	sINTA (M)	H		The status signal identifying the bus inout cycle(s) that may follow an accepted interrupt request presented on INT*.
97	sWO* (M)	L		The status signal identifying a bus cycle which transfers data from a bus master to a slave.
98				
99	POC* (B)	L		The power-on clear signal for all bus devices; when this signal goes low, it must stay low for at least 200 nanoseconds.
100	GND (B)			System ground.

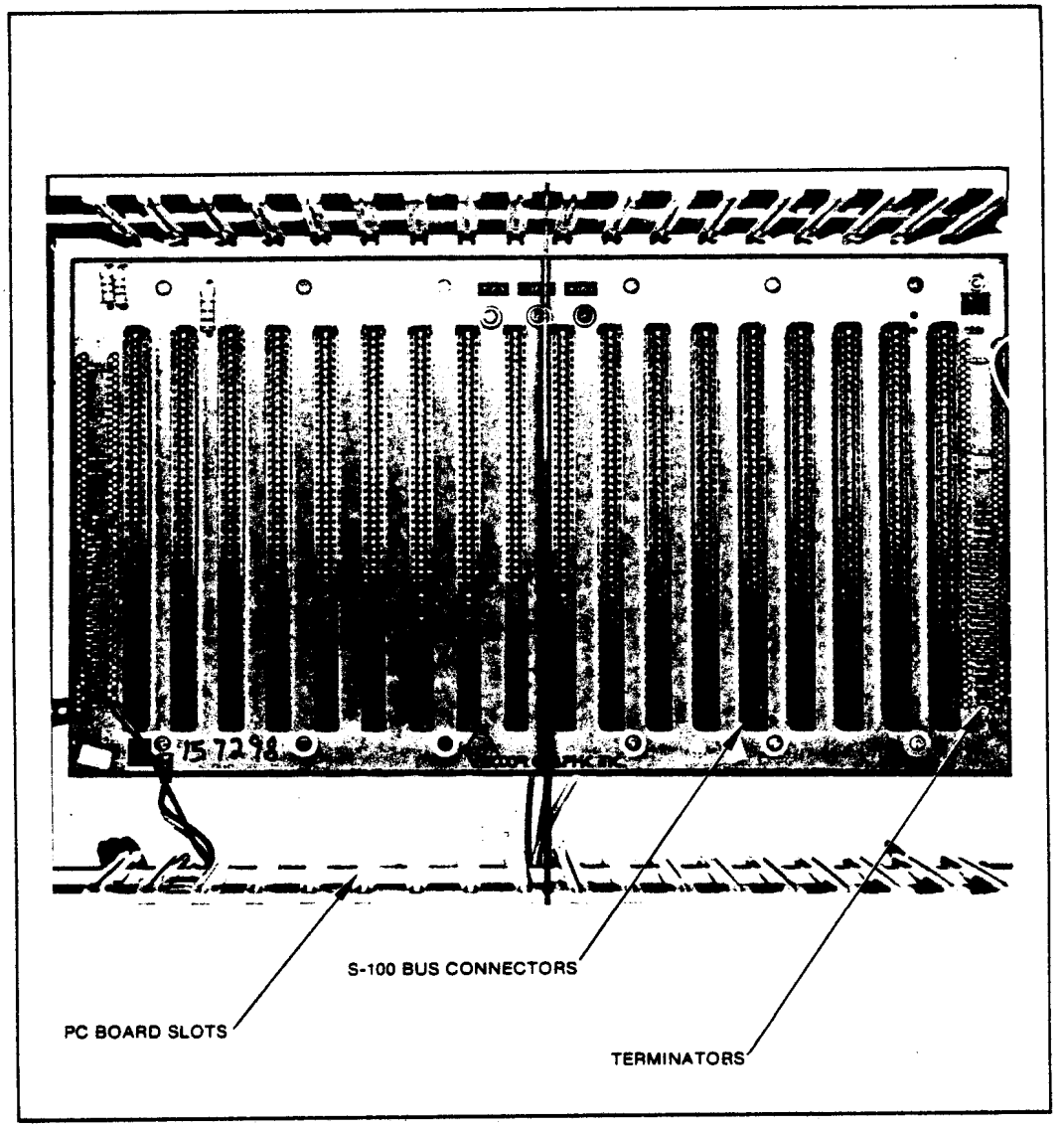
A.2 MZ5 Frontpanel

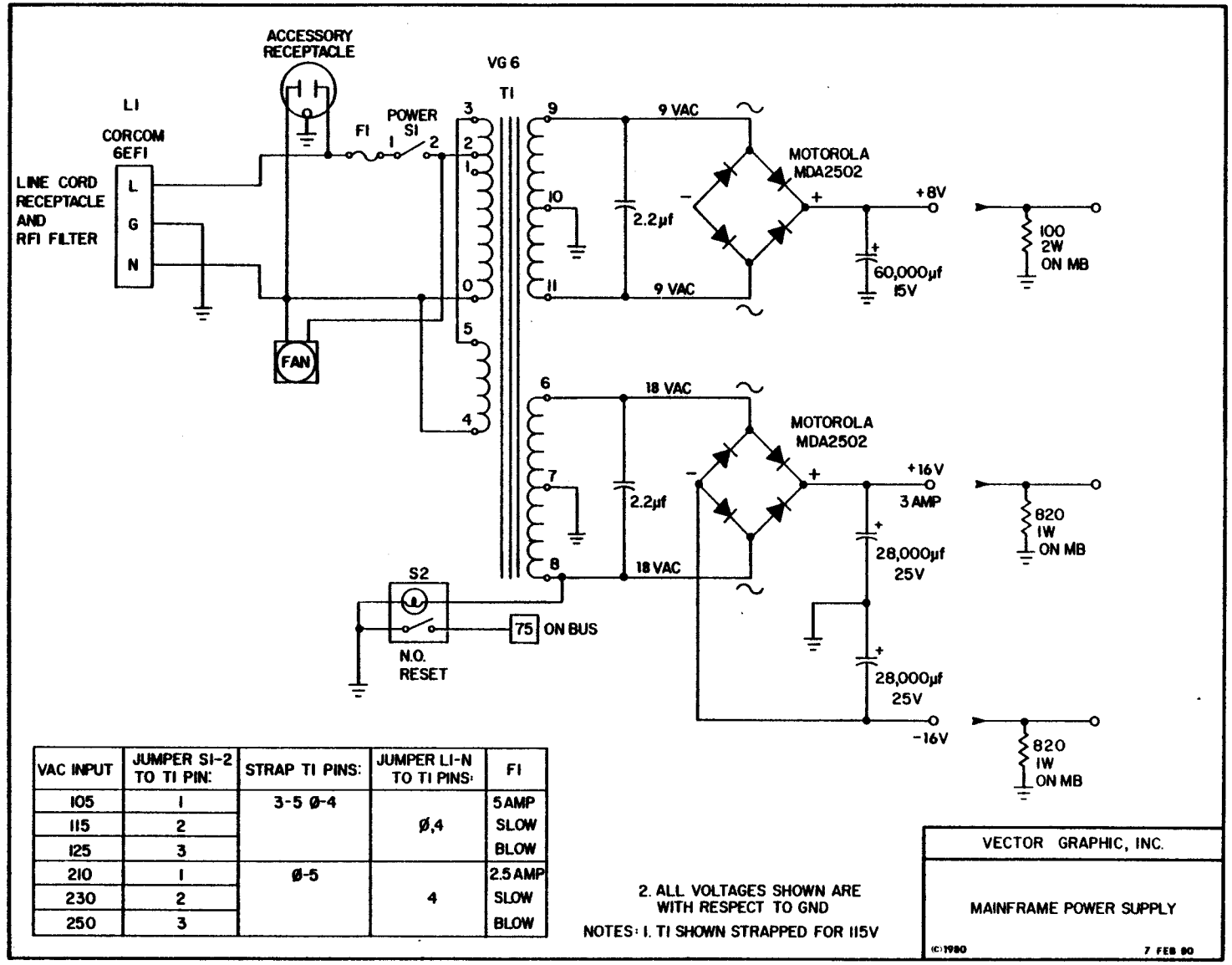


A.3 MZ5 Backpanel



A.4 MZ5 Motherboard





VAC INPUT	JUMPER S1-2 TO T1 PIN:	STRAP T1 PINS:	JUMPER L1-N TO T1 PINS:	F1
105	1	3-5 Ø-4	Ø,4	5 AMP SLOW BLOW
115	2			
125	3			
210	1	Ø-5	4	2.5 AMP SLOW BLOW
230	2			
250	3			

2. ALL VOLTAGES SHOWN ARE WITH RESPECT TO GND

NOTES: 1. T1 SHOWN STRAPPED FOR 115V

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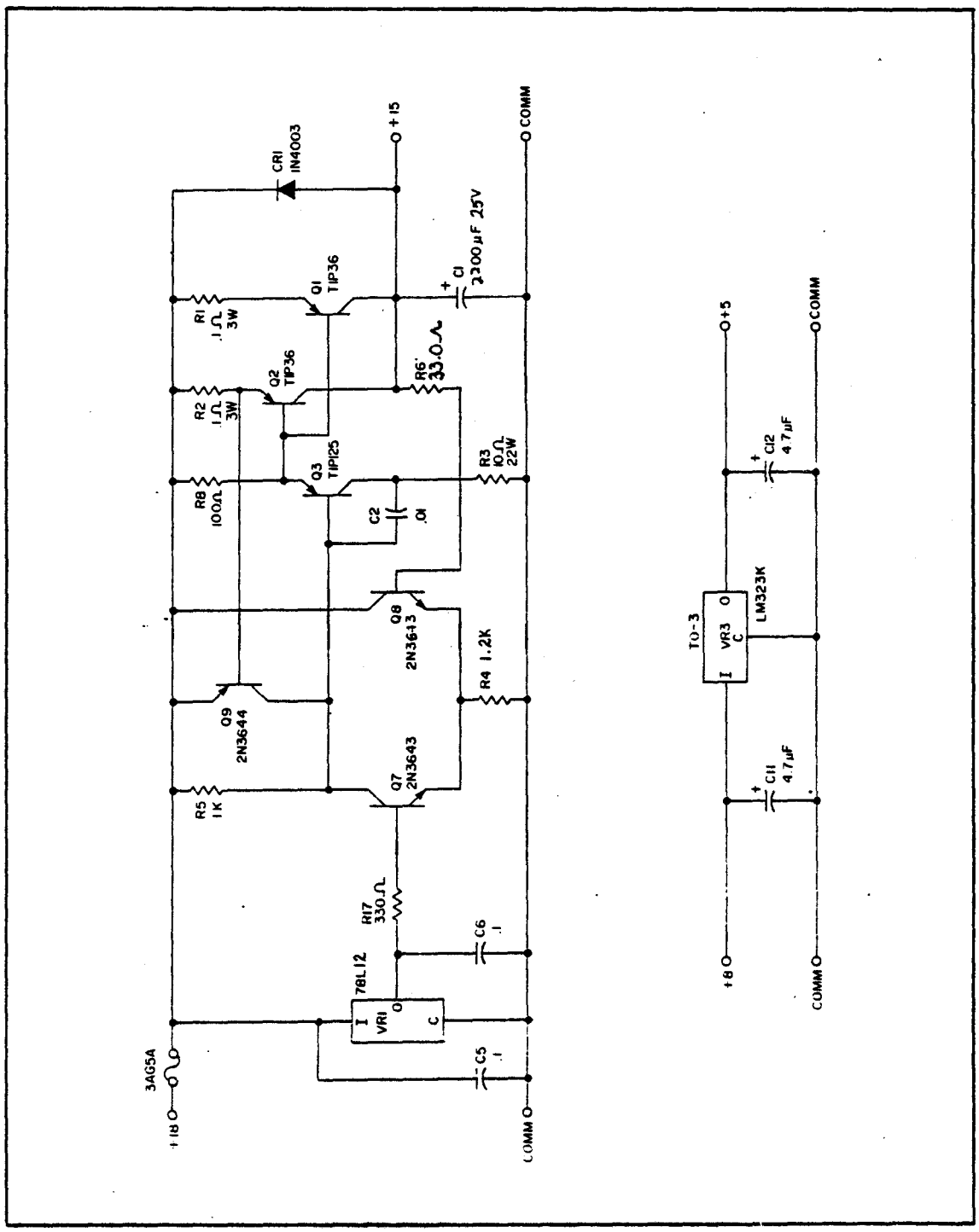
MAINFRAME POWER SUPPLY

 7 FEB 80

A.6 Disk Drive Regulator Board Schematic



MINI-STOR POWER SUPPLY 6-17-81