MP-L2 Parallel Interface

Introduction

The MP-L2 parallel interface is a 5 1/4" wide x 4 3/4" high interface board implemented with the 6821 peripheral interface adaptor integrated circuit. The MP-L2 is used to interface parallel type devices, such as printers, to the computer system. The board is provided with two separate DB-25 connectors with each providing 8 input or output lines, two additional output lines, and two control lines. Input or output selection is done via software programming. Software control of the interrupt lines and handshake polarity is also provided.

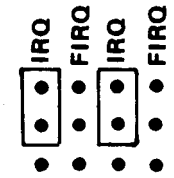
Using the MP-L2

When using the MP-L2 as a printer interface or some other function for which SWTPC supplies the necessary software, a complete understanding of all MP-L2 features is not necessary. Those users should pay particular attention to the section of the system documentation manual concerning the connection of your specific printer and the MP-L2 INTERRUPT JUMPERS section of this instruction set. In other cases, proper use of the MP-L2 requires a thorough knowledge of the programming of a Motorola MC6821 PIA. The PIA PROGRAMMING section of the system documentation manual should be consulted for additional information on PIA programming.

All input/output lines from the PIA are buffered for both protection and drive capability. Before using the MP-L2 the direction of these buffers must be established. Direction selection is implemented by writing a byte of data to a write only latch on the MP-L2 board. This latch also provides four extra output lines for the user.

MP-L2 Interrupt Jumpers

Most SWTPC supplied software requires that the MP-L2 not generate a system interrupt when an input strobe is given to the interface from the outside device. Jumpers are provided on the board to enable either half of the PIA to generate a regular maskable IRQ interrupt or a fast FIRQ interrupt. Placing a jumper in the ON position as shown on the TOP of the circuit board, along with the proper programming of the PIA control register, will enable the appropriate interrupt. For normal system operation the jumpers should be installed as follows:



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Buffer Direction/Output Latch

The MP-L2 contains bi-directional buffers in the PIA input and output lines whose direction must be controlled by software. The desired direction of these buffers is controlled by writing the appropriate bit pattern to a write-only latch on the board. Below is a description of each of the latch configurations. The MP-L2 Address Assignments table should be consulted for the correct latch address.

Latch Functions

Bit #	Function
0	Writing a 0 into this bit position will configure the A side PIA data lines buffer to be an INPUT. Writing a 1 will configure for OUTPUT.
1	Writing a 0 into this bit position will configure the B side PIA data lines buffer to be an INPUT. Writing a 1 will configure for OUTPUT.
2	This bit establishes the direction of A side control line CA2. Writing a 0 will configure for INPUT while a 1 will configure for OUTPUT.
3	This bit establishes the direction of B side control line CB2. Writing a 0 will configure for INPUT while a 1 will configure for OUTPUT.
4	This bit controls the state of the OUT1 line on the A side connector. Writing a 1 gives a 1 output.
5	This bit controls the state of the OUT2 line of the A side connector. Writing a 1 gives a 1 output.
6	This bit controls the state of the OUT1 line on the B side connector. Writing a 1 gives a 1 output.
7	This bit controls the state of the OUT2 line on the B side connector. Writing a 1 gives a 1 output.

Connector Pin Assignments

UPPER CONNECTOR
(A side of PIA)

Pin #	Function		
13	Ground		
14	Data bit 0	(PA0)	(bi-directional)
15	Data bit 1	(PA1)	
16	Data bit 2	(PA2)	
17	Data bit 3	(PA3)	
18	Data bit 4	(PA4)	
19	Data bit 5	(PA5)	
20	Data bit 6	(PA6)	
21	Data bit 7	(PA7)	
22	Control Line CA2		
23	Control Line CA1		(input only)
24	OUT1 (latch bit 4)		(output only)
25	OUT2 (latch bit 5)		(output only)

LOWER CONNECTOR
(B side of PIA)

Pin #	Function		
1-13	Ground		
14	Data bit 0	(PB0)	(bidirectional)
15	Data bit 1	(PB1)	
16	Data bit 2	(PB2)	
17	Data bit 3	(PB3)	
18	Data bit 4	(PB4)	
19	Data bit 5	(PB5)	
20	Data bit 6	(PB6)	
21	Data bit 7	(PB7)	
22	Control line CB2		
23	Control line CB1		(input only)
24	OUT1 (latch bit 6)		(output only)
25	OUT2 (latch bit 7)		(output only)

Drive Capability/Input Requirements

All input/output lines are TTL level compatible. All data lines when used as outputs can source a maximum of 15 mA and can sink 24 mA. Each data line when programmed as an input represents one LS TTL load. Output lines OUT1 and OUT2 can source a maximum of 400 uA and can sink 8 mA. Input lines CA1 and CB1 represent one diode protected MOS load. Control lines CA2 and CB2 can source 2.6 mA and sink 16 mA when used as outputs and represent one LS TTL load when used as inputs.

MP-L2 Address Assignments

The MP-L2 parallel interface should only be used in computer systems which have 16 addresses assigned per I/0 card slot, such as the SWTPC S/09, 69A and 69K systems. Below are the address-register assignments for the MP-L2.

Register Address	Register	
0	A side Data Direction Register of PIA	
1	A side of Control Register of PIA	
2	B side Data Direction Register of PIA	
3	B side Control Register of PIA	
4	--	
5	--	
6	--	
7	--	
g	--	
9	--	
A	--	
B	--	
C	--	
D	--	
E	OUTPUT LATCH	multiply decoded
F	OUTPUT LATCH	multiply decoded

All addresses not indicated are not decoded

For example a MP-L2 board installed in port #2 with I/0 addresses at E000 would have the following assignments:

E020	Aside DDR
E021	Aside control register
E022	B side DDR
E023	B side control register
E02F	LATCH

Port #	Base Address
0	E000
1	E010
2	E020
3	E030
4	E040
5	E050
6	E060
7	E070

Parts List -- MP-L2 Parallel Interface

Integrated Circuits

____	IC1*	74LS02 quad NOR gate
____	IC2*	74LS10 triple 3-input NAND gate
____	IC3*	74LS125 quad buffer
____	IC4*	6820/6821 PIA (MOS)
____	IC5*	74LS245 bi-directional transceiver
____	IC6*	74LS245 bi-directional transceiver
____	IC7*	74LS273 octal latch
____	IC8*	7805 5V regulator

Capacitors

____	C1*	47 mfd 16V electrolytic capacitor
____	C2	0.1 mfd disc capacitor
____	C3	0.1 mfd disc capacitor
____	C4	0.1 mfd disc capacitor
____	C5	0.1 mfd disc capacitor
____	C6	0.1 mfd disc capacitor
____	C7	0.1 mfd disc capacitor
____	C8	0.1 mfd disc capacitor
____	C9	0.1 mfd disc capacitor

Semiconductors

____	D1*	1N4148 silicon diode
____	D2*	1N4148 silicon diode
____	D3*	1N4148 silicon diode
____	D4*	1N4148 silicon diode

All components flagged with a (*) must be oriented as shownin the component layout drawing.