48KRA-1 Dynamic Read/Write Memory Module User's Manual

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CAUTION

Please read Section 2, Handling Precautions and Unpacking, before unpacking or handling your 48KRA-1 any further.

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SECTION 1

INTRODUCTION AND GENERAL INFORMATION

1.1 INTRODUCTION

This manual supplies the information needed to test, use and maintain the 48KRA-1 Dynamic Read/Write Memory Module. In order that you might use your module most effectively and safely, we suggest that you read the entire manual before attempting to use the memory module.

1.2 GENERAL INFORMATION

The 48KRA-1 has a capacity of 49,152 8-bit words (bytes), stored in 24 16K-bit RAMs (Random Access Memories). The 48KRA-1 operates in a dynamic mode. Periodic refreshing is done automatically by the module.

The 48KRA-1 is designed to operate in the Sol S-100 bus and a number of other 8080-based computers which have a 2 MHz PHASE 2 rate without imposing *wait* states. Lines interfacing the S-100 bus are fully buffered.

Address allocation is switch selectable. The 48KRA-1 is organized into three pages of 16,384 bytes each. Each page may be independently assigned to any of 16 starting addresses at 4096-byte intervals, starting with address Ø000 (hexadecimal). If the starting address is DØØØ, EØØØ, or FØØØ, that part of the page which would fall beyond FFFF is assigned to memory space in the range Ø000-2FFF. (Refer to Table 3-1, 48KRA-1 Address Switch Selection.)

A wide variety of extended addressing schemes are available as user options. Modifications for 16-bit data words can also be made by the user.

1.3 SPECIFICATIONS

The 48KRA-1 Memory requires the following ranges of unregulated DC supply:

+7.5 to +10 VDC at 1.20 A max
+15 to +18 VDC at 0.20 A max
-15 to -18 VDC at 0.02 A max

Access time is 460 ns; cycle time is 489 ns min.

Memory IC technology: MOS (Metal Oxide Semiconductor).

SECTION 2

HANDLING PRECAUTIONS AND UNPACKING

2.1 HANDLING PRECAUTIONS

Your memory module and its components are delicate electronic devices. If the following precautions are not observed, they could be damaged during handling, installation, removal, trouble-shooting, or component replacement.

1) Before installing or removing the memory module, turn the computer power OFF. To remove or install it with computer power on can damage the module or the computer.

2) Before installing or removing ICs, turn OFF power to the memory module. To remove or install them with power on can damage the ICs.

3) The memory ICs used on the memory module are MOS devices. MOS (Metal Oxide Semiconductor) devices are constructed with a very thin insulating layer of silicon dioxide (glass) separating the metal gate from the substrate. This layer can be punctured by electric fields, such as static electricity, as small as 100 V carrying only 10 pA. To avoid any possible static electricity discharge damage to the MOS elements, always take care to handle the memory module or its MOS ICs in such a way that no discharge flows through them from your body or from tools.

a. When installing or removing the memory module or its MOS ICs, before touching the module with one hand, always place the other hand on the computer chassis first to discharge static.

b. When grasping the module, grasp it by its edge-connector or the bus traces around its perimeter.

c. Avoid unnecessary handling of the module and the ICs. When handling the MOS ICs, wear cotton clothing (rather than synthetic). Be sure to discharge your body static field before touching the MOS ICs.

All ICs other than the memory ICs and U43 are Schottky TTL and low power Schottky TTL. These do not require precautions against static electricity.

4) *Ground Test Point Connections*

Attach ground clip leads only on the test point (wire loop) installed for this purpose at pin 50 in the lower right corner of the component side of the module. (Refer to Fig 7-4, 48KRA-1 Assembly.) Do not attach clip leads to the ground or power buses around the perimeter of the board. Such connections are liable to short to IC pins.

CAUTION

The heatsink is a poor ground because its finish is nonconducting. Do not attach clip leads to the heatsink.

5) *Manufacturing Options*

A1 is a special configuration module which is varied by the factory according to the memory ICs used in a given production run. Do not interchange or mix the configuration modules of your 48KRA-1 with those of any other memory module which contains a different make and/or type of memory IC.

2.2 UNPACKING INSPECTION

1) Examine the shipping container for signs of possible damage to the contents during transit.

2) READ SECTION 2.1, HANDLING PRECAUTIONS, CAREFULLY.

3) Carefully open the container and withdraw the memory module. Do *not* sink a knife blade deep within the container.

4) Save the shipping materials for possible use in returning the module to your dealer, and in case the dealer needs to ship it to the factory.

5) Visually inspect the module for obvious physical damage. Check that all integrated circuits (ICs) are fully seated in their sockets.

6) If your 48KRA-1 is damaged, please contact the carrier and your dealer immediately, describing the condition of both the shipping container and its contents so that they can take appropriate action.

SECTION 3

SETUP AND INSTALLATION

3.1 MEMORY DISABLE OPTION

The 48KRA-1 comes with the memory disable option ($\overline{\text{PHANTOM}}$) installed in the form of a jumper wire between pads E and F. It is recommended that you retain this option which allows the memory module, at address Ø, to be disabled by the signal $\overline{\text{PHANTOM}}$ which is supplied on S-100 bus pin 67 by the Sol computer and Processor Technology firmware modules such as ALS8 and GPM. $\overline{\text{PHANTOM}}$ is also produced by various other S-100 subsystems available from microcomputer vendors.

If necessary, $\overline{\text{PHANTOM}}$ can be disabled by snipping off the jumper between E and F. E and F are located below the configuration module A1. (Refer to Fig. 7-4, 48KRA-1 Assembly.)

3.2 SETTING STARTING ADDRESSES

3.2.1 Before Setting Switches

Each of the ~~four~~ two pages can be independently allocated with the DIP (Dual Inline Package) switches located near the upper right edge of the module. (Refer to Fig 7-4, 48KRA-1 Assembly.) Page and address assignments for these switches are shown in Figure 3-1, Page and Address Assignments for 48KRA-1 Selection Switches.

You may assign the same starting address to two, or all three pages on *one* module with no ill effect.

In general, you may *not* assign to a module any memory space that is already assigned to another module if they are to share the same bus simultaneously. To do so will cause the bus drivers to contend for possession of the bus resulting improper operation or damage. (One exception to this general rule is if the $\overline{\text{PHANTOM}}$ memory disable option is installed. This option allows the ALS8 to share address zero with a 48KRA-1.) Another exception is bank select or extended addressing. See section 5.6 on extended addressing.

3.2.2 Instructions for Setting Switches

Since the DIP switches are located on the top edge of the memory module, they are accessible after the module is installed in the S-100 backplane; however, to avoid removing the cover of the computer unnecessarily, it is recommended that you set the address switches before installing the module.

1) To select the desired starting address for a page, refer to Table 3-1, 48KRA-1 Address Switch Selection.

1K = 1024 bytes (2^{10})

Table 3-1. 48KRA-1 Address Switch Selection

STARTING ADDRESS		ENDING ADDRESS		DIP SWITCH SETTINGS			
Decimal	Hex	Decimal	Hex	A15	A14	A13	A12
0	0000	16,383	3FFF	0	0	0	0
4,096	1000	20,479	4FFF	0	0	0	1
8,192	2000	24,575	5FFF	0	0	1	0
12,288	3000	28,671	6FFF	0	0	1	1
16,384	4000	32,767	7FFF	0	1	0	0
20,480	5000	36,863	8FFF	0	1	0	1
24,576	6000	40,959	9FFF	0	1	1	0
28,672	7000	45,055	AFFF	0	1	1	1
32,768	8000	49,151	BFFF	1	0	0	0
36,864	9000	53,247	CFFF	1	0	0	1
40,960	A000	57,343	DFFF	1	0	1	0
45,056	B000	61,439	EFFF	1	0	1	1
49,152	C000	65,535	FFFF	1	1	0	0
53,248	D000	4,095	ØFFF	1	1	0	1
57,344	E000	8,191	1FFF	1	1	1	0
61,440	F000	12,287	2FFF	1	1	1	1

0 = Switch open (or OFF - in down position - memory block inactive)

1 = Switch closed (or ON - in up position - memory block active)

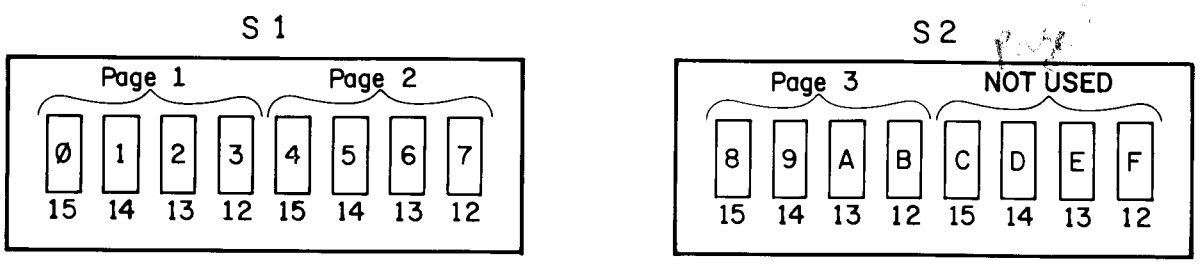


Fig. 3-1. Page & Address Assignments for 48KRA-1 Selection Switches

2) Find the desired starting address for the first page of the memory module in the field titled "STARTING ADDRESS." (Only the indicated starting addresses are available. No intermediate addresses can be used.)

3) On the same horizontal line as the desired starting address, find the corresponding settings for the four switches A15, A14, A13, and A12 in the column titled "DIP SWITCH SETTINGS".

4) On the memory module, find the group of four DIP switches associated with the first page. These are the the first four in Switch 1. Refer to Fig 3-1, Page and Address Assignments for 48KRA-1 Selection Switches. Set the four switches to the selected pattern.

5) In the same manner, set the 4 switches associated with each of the remaining pages.

EXAMPLE 1: Note that each page takes up four 4K blocks. For continuous memory from 0000 to BFFF, the switch settings would be:

	Page 1	*Page 2*	*Page 3*
START. ADDR:	0000	4000	8000
SETTINGS:	0000	0100	1000

EXAMPLE 2: For MEMORY at D000-FFFF and 0000-4FFF.

	Page 1	*Page 2*	*Page 3*
START. ADDR:	D000	F000	1000
SETTINGS:	1101	1111	0001

Note that Page 1 covers both D000-FFFF and 0000-0FFF, and that Page 2 covers both F000-FFFF and 0000-2FFF.

EXAMPLE 3: FOR MEMORY AT 0000-6FFF.

	Page 1	*Page 2*	*Page 3*
START. ADDR:	0000	3000	3000
SETTINGS:	0000	0011	0011

Note that is is permissible for a page to overlap part of another page, or a full page, and that the order of assignment is not important.

You may change address switches with the board installed and power on. But to do this with a program running may crash the program.

3.3 INSTALLATION

(Be sure you have read 2.0, Handling Precautions.)

1) Turn OFF AC power to the host computer.

2) If you are using a Sol computer, make sure it is jumpered for the standard 2.045 MHz clock rate. If you are using another computer, make sure its clock rate is 2.045 MHz or less.

3) Discharge any possible static charge from your body.

4) Be sure the address selection switches are set as desired. (Refer to the previous subsection 3.2, Setting Address Switches.)

5) Orient the memory module to correspond with Fig 7-4, 48KRA-1 Assembly. (The legend should be in the readable position.)

6) Find pin 1 on the computer S-100 bus connector.

7) Orient the memory module edge-connector so that its own pin 1 will mate with pin 1 of the S-100 bus connector. On the component side of the board, edge-connector pin 1 is at the left end of the connector and pin 50 is at the right. Pins 51 through 100 are from left to right on the solder side (backside).

solder side (backside).

CAUTION

If the memory module is installed reversed, the memory module and/or computer could be damaged when power is applied.

8) Slide the memory module into the card guides until its edge-connector just enters the bus connector.

9) Gently push on the module until it is fully seated in the bus connector.

3.4 EXTENDED ADDRESSING AND 16-BIT DATA WORD OPTIONS

Several options for extending addressing beyond 64K are provided for on the memory module. Because of the multiplicity of extended addressing schemes possible and presently used, only general guidelines for its implementation are given. The guidelines, together with the theory, are found in Section 5.6, Extended Addressing. A method for modifying the board to provide 16-bit data words is described in section 5.7.

SECTION 4

MEMORY TEST

4.1 TEST BEFORE OPERATING

Your 48KRA-1 memory module is fully inspected and tested before shipment to ensure that it is operating to specifications. It is packaged for safe transit under normal shipping conditions. Your memory module should, therefore, arrive in your hands ready for use. Nonetheless, we recommend that you test your 48KRA-1 before using it.

This section describes the use of two memory tests: a short test and a "long" test. Actually, the difference in run time between the two tests is not significant. The size of the long test is 15F (hex); the short test is 4C (hex). It is recommended that you use the long version since it is more thorough and more useful for trouble-shooting. Your dealer will allow you to make a tape copy of the long test. If necessary, the short test can be keyed into the computer and used instead. The long test can be entered in an evening's work.

Both these memory tests may also be used as diagnostic tools at any time after their initial use as pre-operating tests.

NOTE

The memory test programs are written for use with Processor Technology SOLOS or CUTER monitor programs. If you are not using either, you will need to modify the test programs to work with your monitor program.

4.2 THE RECOMMENDED PRE-OPERATING MEMORY TEST

(A listing of the long memory test is in the Appendix.)

In addition to testing your memory module, the long memory test prints out a complete map of the memory ICs as they are arranged on the board, marking bad ICs with an X.

4.2.1 Test Procedure (Long Memory Test)

1) Obtain a copy of the test on cassette from your dealer. If you own a 48KRA-1, you may copy the program without violating the copyright. If you cannot obtain a copy, at the next step of this procedure, key in the program from the listing in the Appendix. Once in the computer, the program can be saved on tape for later use.

2) Set the page assignment switches for continuous memory from Ø to 48K, referring to section 3.2, Setting Starting Addresses.

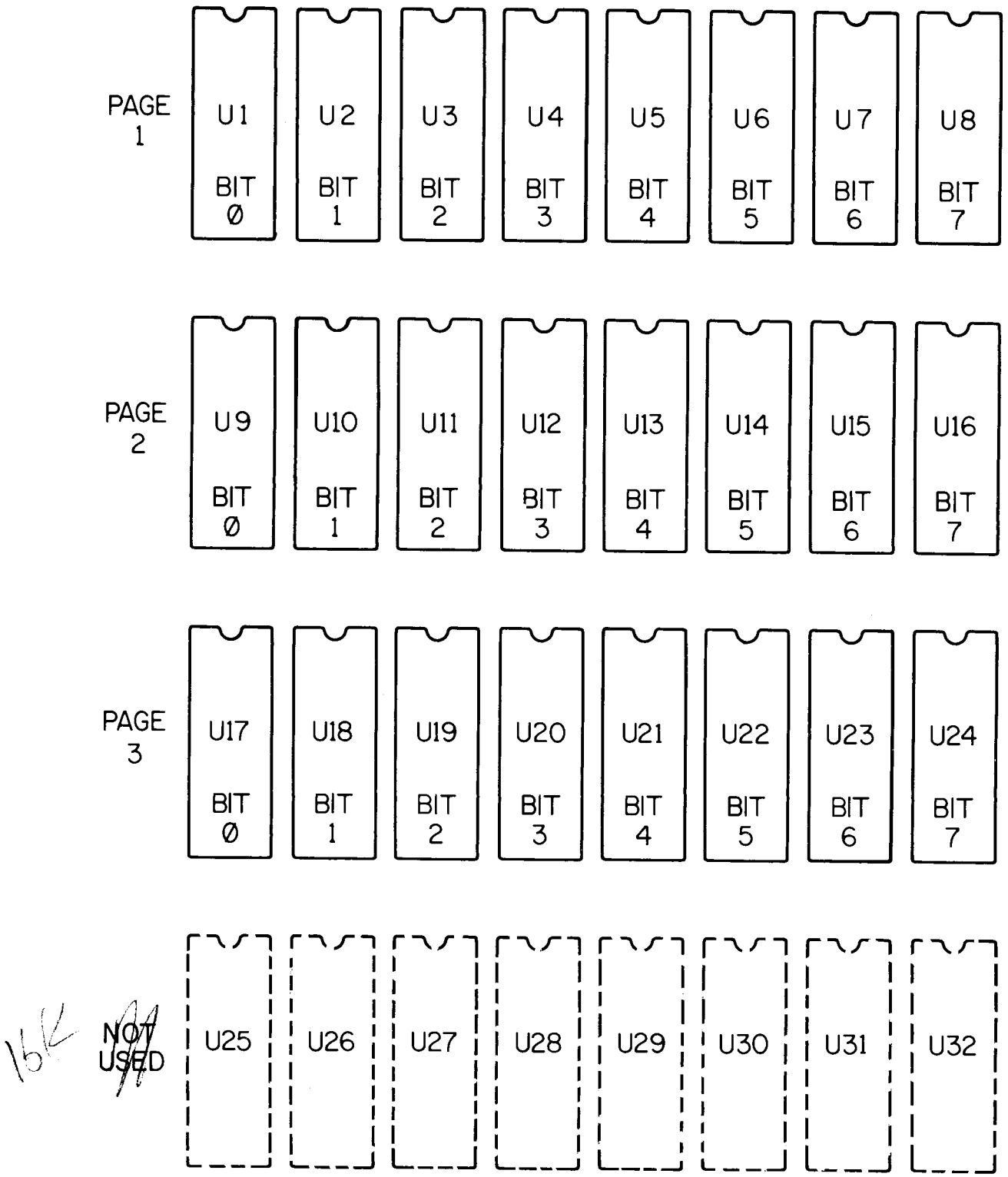


Fig. 4-1. Page & Bit Assignments in 48KRA-1 Memory Array.

3) Load the long memory test into memory at C900 (hex). The Sol computer contains built-in system memory at the necessary locations. The program could be reassembled to run at a different address if necessary.

4) Type: EXEC C900 Press RETURN:

The test displays a copyright notice and displays two options for selection by a key stroke:

Press C The test echoes "C" and repeats the test continuously, accumulating a record of errors. After each pass through the test, this option updates the test results, a map of ICs.

Press any other key The test echoes the key typed and runs one complete test cycle, displays the map of ICs, and returns control to SOLOS/CUTER.

For the pre-operating memory test, select the C option.

EXAMPLE OF ERROR MAP

```
PAGE 1      GG GG GG GG
PAGE 2 ---> XG GG GG GG      G = Good Memory IC
PAGE 3      GG GG GG GG      X = Bad Memory IC
```

Reading left to right, top to bottom, each character in the map represents one of the 24 memory ICs, U1 through U24. The characters are displayed in the same position as the memory ICS on the circuit board, when the board is oriented as in the assembly drawing, Fig 7-4. (For page and bit assignments in the memory array, refer to Fig. 4-1.)

The example map above therefore shows that U9 made one or more errors during the test.

Any memory IC reported as an "X" must be replaced.

5) If the continuous test runs for 30 minutes with no "X" appearing, consider the memory module as having passed.

6) To return control to SOLOS/CUTER at any time, press ESCAPE or UPPER CASE and REPEAT simultaneously.

7) If you have keyed in the program by hand and it runs correctly, save it on cassette for later use, using the SOLOS/CUTER SAVE command. (Refer to *SOLOS/CUTER User's Manual.*)

4.3 SHORT MEMORY TEST

(Refer to the Appendix for the listing.)

Use this short version only if the long version is not available.

1) Set the page select switches for continuous memory from Ø through 48K. (Refer to 3.2, Setting Starting Addresses.)

2) Load the program into memory at C900 (hex). The Sol computer contains built-in system memory at this location. The program could be reassembled to run at a different address if necessary.

3) Type: EXEC C900

If no errors are encountered, the program repeats continuously. If the test runs for 30 minutes without the SOLOS/CUTER prompt appearing, consider the memory module to have passed the test.

4) Return control to SOLOS/CUTER by simultaneously pressing: UPPER CASE and REPEAT.

5) If the SOLOS/CUTER prompt appeared while the test was running, the read data did not match the write data. An error report is stored in four locations of memory, which may be viewed as follows:

a. Enter the command: DU C949 C94C <CR>.

The resulting display shows:

Byte 1 and 2	The memory address where the error occurred. (Most significant byte first.)
Byte 3	Correct Data.
Byte 4	Erroneous Data.

b. If the most significant digit of the error address (in hex) is 1, 2, or 3, the error is in an IC in Page 1.

c. If it is 4, 5, 6, or 7, the error is in Page 2.

d. If it is 8, 9, A, or B, the error is in Page 3.

e. Determine the bad bit by comparing the correct and erroneous data stored in bytes 3 and 4 of the error report.

f. Knowing the bad bit and page, find the bad IC from Figure 4-1 and replace it.

SECTION 5

THEORY OF OPERATION

5.1 OVERVIEW

As you read this section refer to the block diagram, Figure 7-1 and the schematic, Figures 7-2 and 7-3. Note that the schematic is divided into two sheets which may be folded out in both directions, and that signals which go between the two sheets line up at the binding of the manual.

The encircled numbers following the name of a functional block of circuitry described in this section correspond to the key numbers for the referenced block on the system block diagram, Fig. 7-1 and Table 7-1, Key to System Block Diagram.

5.1.1 S-100 Bus Interface

The host computer and the 48KRA-1 communicate with one another over the S-100 Bus. Table 5-2, S-100 Bus Signals, identifies these signals and their sources and defines their functions. Table 5-3 briefly describes internal signals of the memory module.

5.1.2 Memory Array

The memory array (2) consists of 24 16K dynamic memory ICs arranged in three rows of eight. Each dynamic RAM can store 16,384 bits. Each row of eight ICs stores 16,384 *bytes*. Each of the three rows is a page of memory.

5.1.3 Manufacturing Options

The memory module can support a wide variety of memory ICs which are 16-pin DIP ICs requiring +12 V, +5 V, and -5 V. Four pins are used for power supplies. One pin connects data-in and another connects data-out. Seven pins carry address information (14 bits in two samples). $\overline{WE}$ indicates whether to read or write, $\overline{CAS}$ provides timing, and $\overline{RAS}$ provides timing and selection. The memory module is designed to operate using a wide variety of memory ICs having various speeds. Any of a number of types may have been supplied with your module. Circuit variations required for the different memory ICs are provided in a variable 16-pin configuration module (A1) which plugs into a standard IC socket.

5.1.4 Dynamic Memory Refreshing

Since the memory ICs used in the 48KRA-1 are dynamic memories in which the data cells operate by stored electrical charge which gradually dissipates, stored data must be restored periodically. Otherwise, current leakage would eventually change the stored data. The restoring process is called "refreshing" the memory, or simply "refresh." The 48KRA-1 itself provides memory refresh as required without any external intervention. In all cases it is done without introducing any delay to the CPU or DMA device controlling the module.

5.1.5 Addressing

Assignment of the S-100 address lines are as follows:

A0-5	Row addressing.
A7-A11	Column addressing.
A12-A15	Page selection or 4K block selection.
A6, A12 and A13	May be used for row or column, depending upon the type of memory IC.

Address lines A12-A15 are compared to the three sets of four DIP switches to select one or none of three 16K memory arrays called "pages." Each page consists of one row of eight 16K RAM (Random Access Memory) ICs.

Address lines A0 through A5 and A7 through A11 are applied to the Address Multiplexer (5) in two groups. These two groups are selected in succession to the memory address inputs. Row Address Strobe ($\overline{RAS}$) is applied by the $\overline{RAS}$ Drivers (4) to the eight memory ICs of the selected page. The leading edge of $\overline{RAS}$ causes these eight ICs to store A0-A5, the first group of address bits, called the row address, and to start a memory cycle.

Subsequently, Column Address Strobe ($\overline{CAS}$) (generated from the Bus Interface and Control logic (7)) is applied to all of the memory ICs. The leading edge of $\overline{CAS}$ causes those memory ICs selected by $\overline{RAS}$ to store the second group, A7-A11, called the column address.

Note that the column address section of the address multiplexer contains a Type D register which samples the S-100 lines at the same instant that RAS is causing the memory ICs to sample the ROW addresses. These latched address bits are subsequently moved to the memory ICs by CAS.

5.1.6 Write and Read Operations

$\overline{CAS}$ samples Write Enable ($\overline{WE}$) to determine whether the current cycle is to write data into memory or to read data from memory. The contents of the Data-Out Bus (DO0-DO7) are applied to the MEM IN pins of the memory array by the Write Data register (1) . This register is clocked at the rise of RAE with the start of each memory cycle. Each bit from the Data Out bus is applied to three memory ICs, one in each of the three pages. In a memory write operation, $\overline{CAS}$ causes the selected eight memory ICs to store the data found on their Data-In pins in an input latch. This data is subsequently stored at the location described by the row and column addresses.

In a memory read operation, the selected eight memory ICs retrieve data from the memory address indicated by the row and column addresses, send it to their output latches, and enable their output drivers. At the end of $\overline{RAS}$ and $\overline{CAS}$, the read data is latched into the output register (3) , and is sent to the Data In Bus (DI0-DI7) if $\overline{EDO}$ (Enable Data Output) is low.

5.2 PAGE SELECTION

Page selection and board selection depend on the address bits A12-A15 and on three quartets of switches. Each quartet of switches can be set to one of 16 possible starting addresses. Each quartet of switches corresponds to one page of eight memory ICs. The contents of each quartet of switches is compared to address bits A12-A15 by a ROM (Read Only Memory) in the Page Select Array (12) (U39 - U42). If a match is found, the output line from that ROM goes low. There are three such output lines, one per ROM, called $\overline{MATCH}$ lines.

Each $\overline{MATCH}$ line corresponds to a page. A zero (low) on any $\overline{MATCH}$ line causes the $\overline{PSEL}$ (Page Select) lines of higher page number to be held high, thus only one page can be enabled (that with the lowest page number) even though more than one switch set may match A12-A15. This feature allows the memory module to be used in systems where less than its full memory extent is needed.

During memory cycles, the three $\overline{PSEL}$ (Page Select) lines are selected by the Page Multiplexer (6) to drive the three PAGE lines. The PAGE lines select one or none of three $\overline{RAS}$ (Row Address Strobe) Drivers (4) . Each $\overline{RAS}$ selects one of three pages in the memory array (2)

5.3 MEMORY CYCLES

(As defined in terms of the 48KRA-1, a cycle is a timed sequence of events that may perform one memory access.)

5.3.1 Timing Scheme Enables Independent Refresh

48KRA-1 memory cycles correspond to S-100 bus T-cycles. This means that the memory module will not work in systems in which the PHASE 2 clock period is shorter than the minimum cycle period specified for the memory module: 489 ns. This allows a simple control logic design which does its needed refreshing totally independent of the S-100 bus and the CPU. There are no "coincidence" cycles in which the bus and the refresh logic contend for possession of the memory. There are no "wait" states, and the memory module does not use the ready lines.

5.3.2 Timing of Memory Cycles

Located in the Bus Interface and Control Logic (7) , the cycle timing circuitry consists of a latch and delay line driver, a delay line with five taps (U50) and a number of latches to provide the specific signals needed.

When the S-100 bus clock, PHASE 2, goes low, a latch, RAE (U49-9), is set. The delay line input goes low. A negative step moves down the delay line. When it reaches the second tap, it resets the latch at the input end, and the delay line input rises. A positive step moves down the delay line. The fall of the next PHASE 2 starts another cycle.

The delay line determines the specific durations of various features of a cycle. The timing of a typical read cycle is shown in Fig. 5-1.

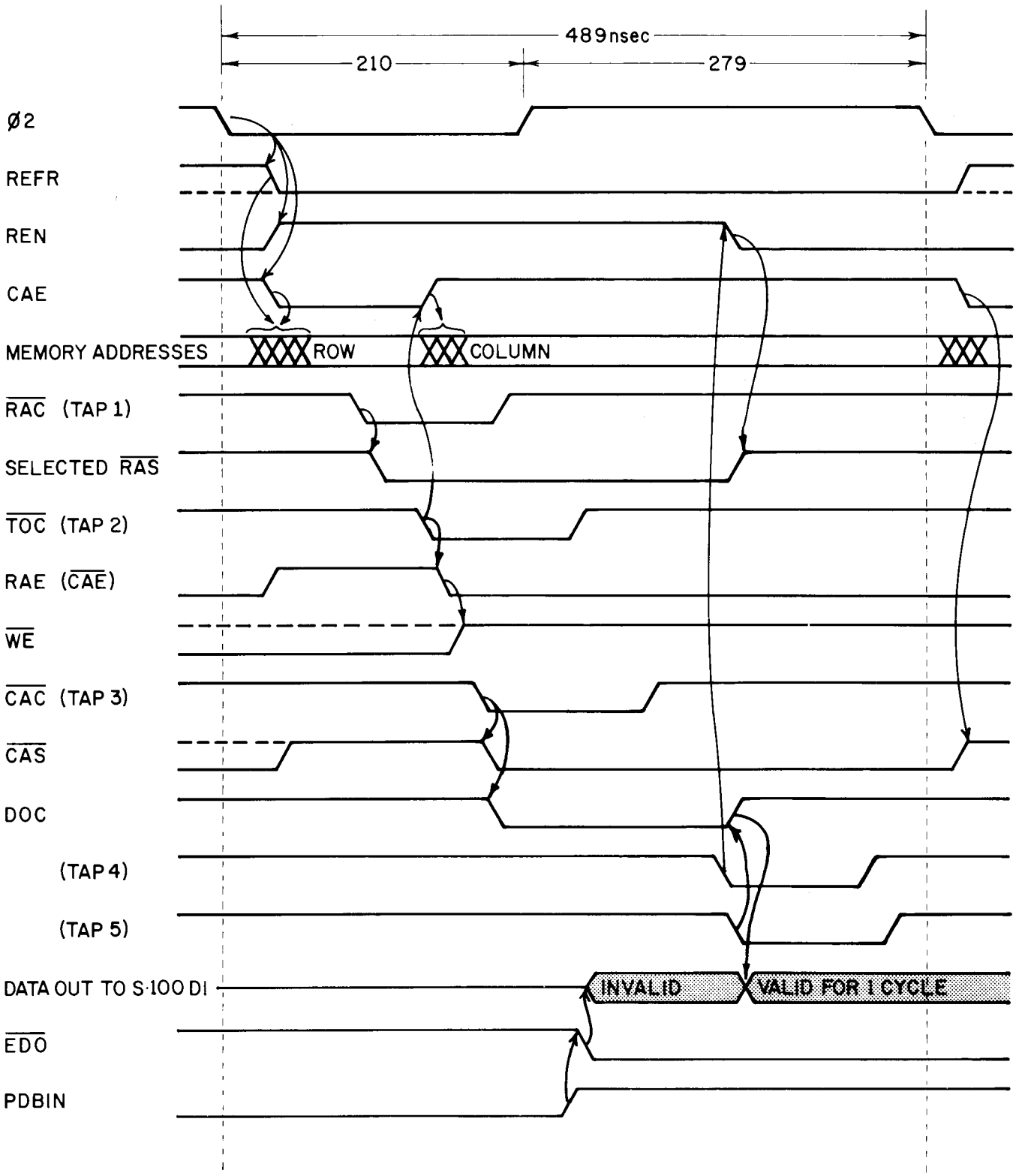


Fig. 5-1 Timing of Typical Read Cycle

5.3.3 Types of Memory Cycles

There are four types of memory module cycles: NULL, READ, WRITE, and REFRESH.

Within the delay line all are identical. At the fall of PHASE 2, the state machine (part of the Bus Interface and Control logic (7)) considers its inputs and sets two outputs to new values. These two outputs, REFR and REN, partially determine the type of cycle. Later, two more outputs, $\overline{WE}$ and PEND, are set, completely determining the type of cycle.

Null Cycle

A Null cycle is distinguished by REN (Row Enable) low. $\overline{RAS}$ and $\overline{CAS}$ do not occur. RAE (Row Address Enable) occurs but has no consequence. None of the memory ICs in the memory array do anything during a Null cycle.

Read Cycle

(Refer to Fig. 5-1, Timing of A Typical Read Cycle.)

A Read cycle is distinguished by REN high, $\overline{WE}$ high, and REFR low. Just after PHASE 2 falls, REN occurs, enabling the three $\overline{RAS}$ drivers (4) , and RAE rises causing the address multiplexers to present the row address to memory. $\overline{RAC}$ occurs, clocking the selected page into the $\overline{RAS}$ drivers. $\overline{RAS}$ occurs at the selected page of memory. ICs in that page of memory store the row address.

CAE rises; the address multiplexers present the column address to the memory ICs. Soon $\overline{CAS}$ occurs. The memory ICs selected by $\overline{RAS}$ now store the column address, and set a bit to indicate that this is a read cycle. Then they get the data from the indicated address, and present it at their output pins. There is some variation among memory types in the details of how and when the outputs are enabled and the data is valid, but the output must be valid and enabled at the rise of DOC (Data Output Clock).

At the end of the read cycle, REN is removed, ending $\overline{RAS}$. The output data is clocked to the output register (3) at the rise of DOC. This data will be enabled to the DI bus if $\overline{BSEL}$, $\overline{ESEL}$ and $\overline{MSEL}$ are all low, and SMEMR and PDBIN are both high. $\overline{CAS}$ rises at the fall of PHASE 2 with the start of the next cycle.

Three ROM outputs (1 from each of three ROMs) in the Page Select Array (12) are connected together to form $\overline{BSEL}$ (Board Select). $\overline{BSEL}$ will be low if any page on the memory module is selected. $\overline{ESEL}$ (Extended Select), produced by the Extended Selection Logic (8) , and $\overline{MSEL}$ produced by the Bus Interface and Control Logic, must also be low during a Read; SMEMR and PDBIN (both from a requesting processor on the S-100 bus) are both high. These are all used by the Bus Interface and Control Logic (7) . The output $\overline{EDO}$ will be low enabling the tri-state outputs of the memory data output latch (3) to drive the DI Bus completing the Read operation when the board is selected.

In the above cycles, memory ICs in the array, but not in the selected page, execute CAS-only cycles. Nothing of consequence happens in the memory module during these CAS-only cycles, but some types of memory ICs require these CAS-only cycles as part of their data output enabling scheme.

Write Cycle

A Write cycle is distinguished by REN high, REFR low and $\overline{WE}$ low. Shortly after PHASE 2 falls, REN occurs enabling the four $\overline{RAS}$ drivers (4) , and RAE rises, causing the address multiplexers to present the row address to memory, and clocking the data to be written into the Write Data Register (1) . Next $\overline{RAC}$ occurs (U50-14), clocking the selected page into the $\overline{RAS}$ drivers. $\overline{RAS}$ occurs at the selected page of memory. ICs in that page of memory store the Row Address. Next, CAE rises, the Address Multiplexers (5) present the column address to the memory ICs. $\overline{WE}$ goes low, indicating a write cycle. Soon $\overline{CAS}$ occurs. The memory ICs selected by $\overline{RAS}$ now store the column address, a bit to indicate that this is a write cycle, and the data to be written from the Data In pins. At the end of the cycle, $\overline{RAS}$ and $\overline{WE}$ are removed. Before the

removal of $\overline{CAS}$, some data, not necessarily that just stored, is set into the output latch (3). This is not valid data and is not read because it does not get enabled onto the DI bus, since PDBIN is low at U36 keeping $\overline{EDO}$ high. $\overline{CAS}$ rises at the fall of PHASE 2 which starts the next cycle.

Refresh Cycle

A Refresh cycle is distinguished by the state machine in the Bus Interface and Control Logic (7) outputs, $\overline{WE}$, REN and $\overline{REFR}$ high. $\overline{REFR}$ causes the Address Multiplexer (5) to present the address supplied by the Refresh Counter (10) to the memory ICs. REN occurs, enabling the four $\overline{RAS}$ drivers. $\overline{RAC}$ occurs, clocking the page number into the $\overline{RAS}$ drivers.

$\overline{RAS}$ occurs at the selected page of memory. ICs in that page of memory store the refresh address as the row address, and in doing what they would normally do with it during a read, they refresh an entire row of memory within the active page.

CAE occurs. This is of no consequence. $\overline{CAS}$ does not occur. At the end of the cycle, REN goes low, removing $\overline{RAS}$. At the fall of PHASE 2 in the next cycle, REFR goes low, causing the refresh Counter (10) to count 1 and returning the Address Multiplexer outputs to the S-100 bus based row address.

5.4 OPERATIONS: The State Machine (7)

An operation is one or more cycles which are designed to achieve a desired result. An operation of the memory module is in response to a request from some other S-100 device. The memory module performs six types of operations: SELECTED READ, SELECTED WRITE, UNSELECTED READ and UNSELECTED WRITE, SELECTED DEPOSIT and UNSELECTED DEPOSIT. Figure 5-2, Sequences of the Operation Request Logic, shows a typical sequence of states for each of the six operation types.

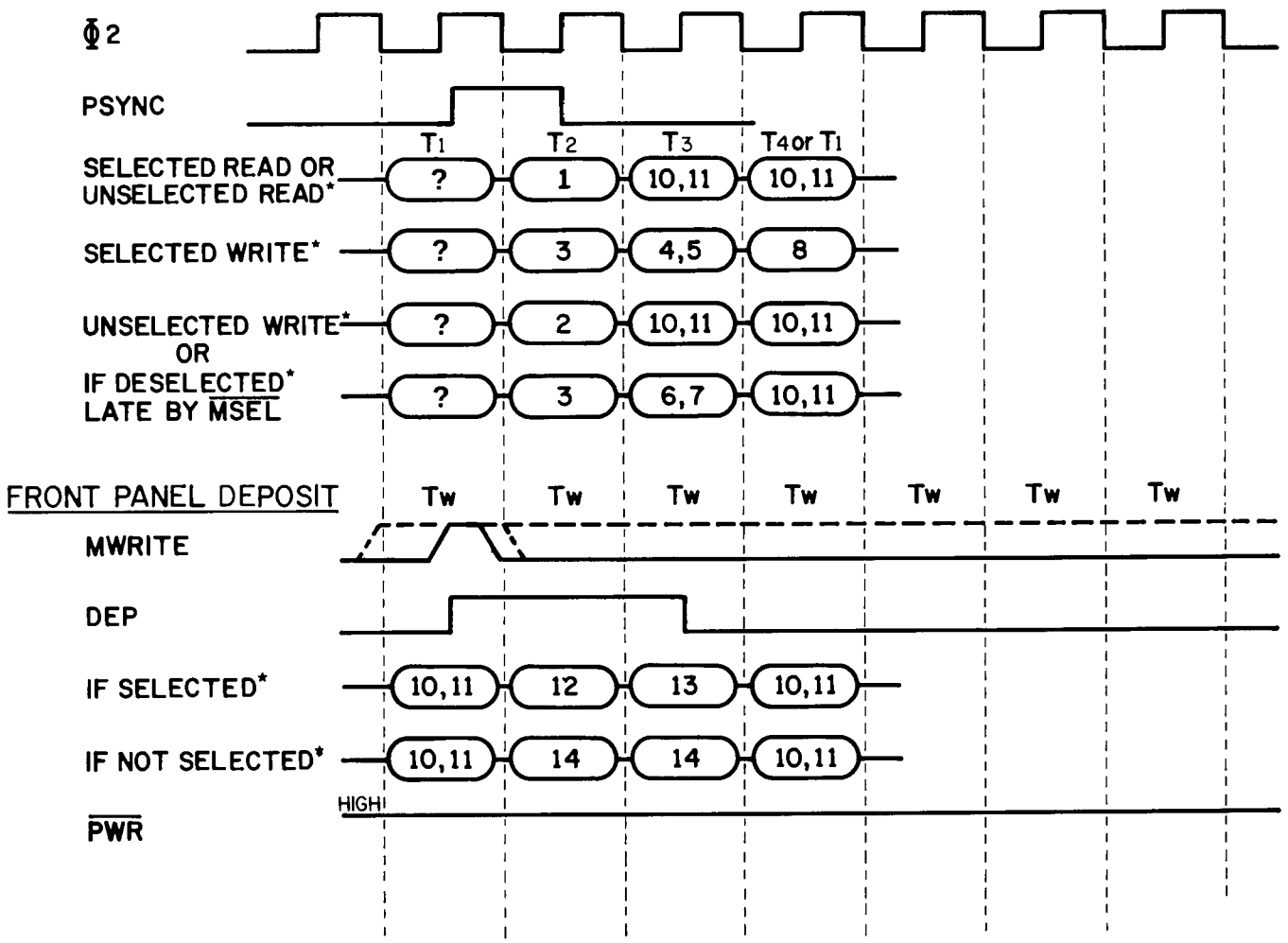
5.4.1 Variations of the Six Operations

Each of these operations has many variations consisting of different sequences of possible states of the state machine. The state machine consists of an 8-input, 4-output ROM (U56) and four clocked latches. These variations are caused by two variables:

1. The presence of T4, T5 and Tw cycles.
2. The need for refresh.

Operation request and sequencing is controlled by a state machine. Table 5-1, Sequences of the Operation of the State Machine, shows the possible states of this state machine expressed in terms of the ROM inputs and outputs. The state machine changes its outputs REFR and REN at the fall of PHASE 2. It changes its output $\overline{WE}$ at the fall of REN. It changes its output PEND at the rise of $\overline{RAC}$.

Each of the 14 possible states are variations of one of the four types of memory cycles: Null, Write, Refresh and Read. (Refer to 5.3.3, Types of Memory Cycles.)



* Operations are marked with an asterisk.

Fig. 5-2. Sequences of the Operation Request Logic

Table 5-1. The States of The State Machine

CYCLE	STATE	CONDITIONS TO ENTER CYCLE								OUTPUT DATA LATCHED DURING CYCLE				HEXA. OUT
		$\overline{BSEL}$	$\overline{MSEL}$	$\overline{SWO}$	$\overline{WRR}$	PEND	PSYNC	DEP	RFRQ	DPEND	DWE	DREN	DREFR	
READ	1 READ	-	-	-	X	X	1	X	X	-	0	1	0	-
	1P	X	-	1	X	X	1	X	X	0	0	1	0	2
READ	2 UWP READ	-	-	-	X	X	1	X	X	-	0	1	0	-
	2P	1	-	0	X	X	1	X	X	0	0	1	0	2
READ	3 SWP READ	-	-	-	X	X	1	X	X	-	0	1	0	-
	3P	0	-	0	X	X	1	X	X	1	0	1	0	A
NULL	4 SWP NULL	0	0	0	1	1	0	0	0	1	0	0	0	8
REFRESH	5 SWP REFR	0	0	0	1	1	0	0	1	1	0	1	1	B
NULL	6 UWP NULL	A	A	0	1	1	0	0	0	0	0	0	0	0
REFRESH	7 UWP REFR	A	A	0	1	1	0	0	1	0	0	1	1	3
WRITE	8 SW WRITE	0	0	0	0	1	0	0	X	0	1	1	0	6
READ	9 UW READ	A	A	0	0	1	0	0	X	0	0	1	0	2
NULL	10 NULL	X	X	X	X	0	0	0	0	0	0	0	0	0
REFRESH	11 REFRESH	X	X	X	X	0	0	0	1	0	0	1	1	3
WRITE	12 DEP WRITE	0	0	X	1	0	0	1	X	1	1	1	0	E
READ	13 DEP READ	0	0	X	1	1	0	1	X	0	0	1	0	2
READ	14 UDEP READ	A	A	X	1	X	0	1	X	0	0	1	0	2
TIME FROM FALL OF PHASE 2 (ns)		170-0	170-126	0-85	350	150	170-300	350	350	150	100	0	0	

1 = SIGNAL HIGH
0 = SIGNAL LOW
A = EITHER/BOTH A's HIGH
X = DON'T CARE
- = NOT READY YET

5.5 REQUESTS FOR MEMORY OPERATIONS

Three requests are possible:

1. *Normal access* — SYNC high, $\overline{\text{MESEL}}$, $\overline{\text{BSEL}}$, $\overline{\text{ESEL}}$, all low.

Normal access has higher priority than Deposit. They will not normally occur at the same time.

2. *Deposit* — DEP high, SYNC low. $\overline{\text{MSEL}}$, $\overline{\text{BSEL}}$, $\overline{\text{ESEL}}$, all low.
3. *Refresh request* — REFR low.

Refresh request has low priority. It will cause a refresh if both the other requests are absent.

5.5.1 Normal Access, Selected

Normal access, selected, and $\overline{\text{SWO}}$ high cause a Read state followed by a Refresh state or a Null state.

Normal access, selected, and $\overline{\text{SWO}}$ low cause a WP READ followed by a Selected Write, followed by a Refresh or a Null state.

Normal access, unselected, and $\overline{\text{SWO}}$ high cause a read state followed by a Refresh state or a Null state.

Normal access, unselected, and $\overline{\text{SWO}}$ low cause a UW (Unselected Write) Read state followed by a Refresh state or a Null state.

5.5.2 Deposit

Description

Deposit results from the use of the front panel Deposit switch while the system is in a continuous train of Tw states usually showing showing a fetch status. The deposit pulse (MWRITE and *not* $\overline{\text{PWR}}$) is several T-cycles long. The first of these results in a Dep Write, the second results in a Dep Read so that the data just written will appear on the DI bus and the front panel data lights. The third will be a Null or a Refresh state. This sequence of three states will happen repeatedly. Eventually MWRITE will go away, causing a return to the normal Default or Refresh condition.

Front Panels Which Use Deposit

The memory module is intended to perform deposits for front panels or similar devices which meet the following description.

S-100 front panels normally have a run-stop switch which stops the processor in an indefinite series of Tw states, showing a fetch status. When switched to stop, PHASE 1 and PHASE 2 clocks continue to be present. All other bus signals are stationary. Lights normally display the 16 address bits and the eight DO bits.

The address may be changed by operating a switch called EXAMINE. This causes the processor to resume operation for three cycles by forcing the DI lines to correspond to the command JUMP; the front panel tricks the processor into believing that the fetch which was being held incomplete by Tw states was really a JUMP. The processor now reads two consecutive bytes which the front panel supplies from its address switches. Next the processor places these two bytes on the address bus and starts another fetch (from that address.) The front panel stops this fetch with another indefinite series of Tw states. The addressed memory location puts the requested data on the DI bus. The front panel displays the new address (which corresponds to its switches) and the new data.

How the Memory Module Produces Deposit

(Refer to Fig. 5-3, States of the Synchronous Counter Producing DEPOSIT.)

To produce front panel deposit, the memory module uses a synchronous counter (U47). If MWRITE is present and $\overline{PWR}$ is absent, the counter produces a signal called DEP. DEP changes at about 350 ns after the trailing edge of PHASE 2. It will be high for two periods and low for one. This pattern will repeat until DEPOSIT is removed.

The first period of DEP (count of E) produces a write cycle (DEP WRITE).

The second period of DEP (count of F) produces a read cycle (DEP READ).

The third period, DEP low (count of Ø), produces a Refresh if one is requested.

Requirements for the Signal DEPOSIT

DEPOSIT must produce MWRITE. DEPOSIT must not produce $\overline{PWR}$. If synchronous, DEPOSIT must be stable at the clock 350 ns after the falling edge of PHASE 2. If asynchronous, DEPOSIT must be longer than one PHASE 2 period.

There is no upper limit to the length of DEPOSIT. DEPOSIT is typically not synchronous to the clocks and is of varying length. The memory module synchronizes Deposit and assures that a long DEPOSIT pulse does not prevent timely refresh. No part of the system may produce MWRITE without $\overline{PWR}$ unless a deposit sequence is an acceptable result. (DMA DEVICES should produce $\overline{PWR}$).

$\overline{WR}$ is the processor's write strobe. $\overline{PWR}$ is $\overline{WR}$ applied to the S-100 bus. A DEPOSIT switch on the front panel produces a pulse which requests the contents of the DO lines (the contents of the front panel data switches) to be written to the memory location indicated by the address lines.

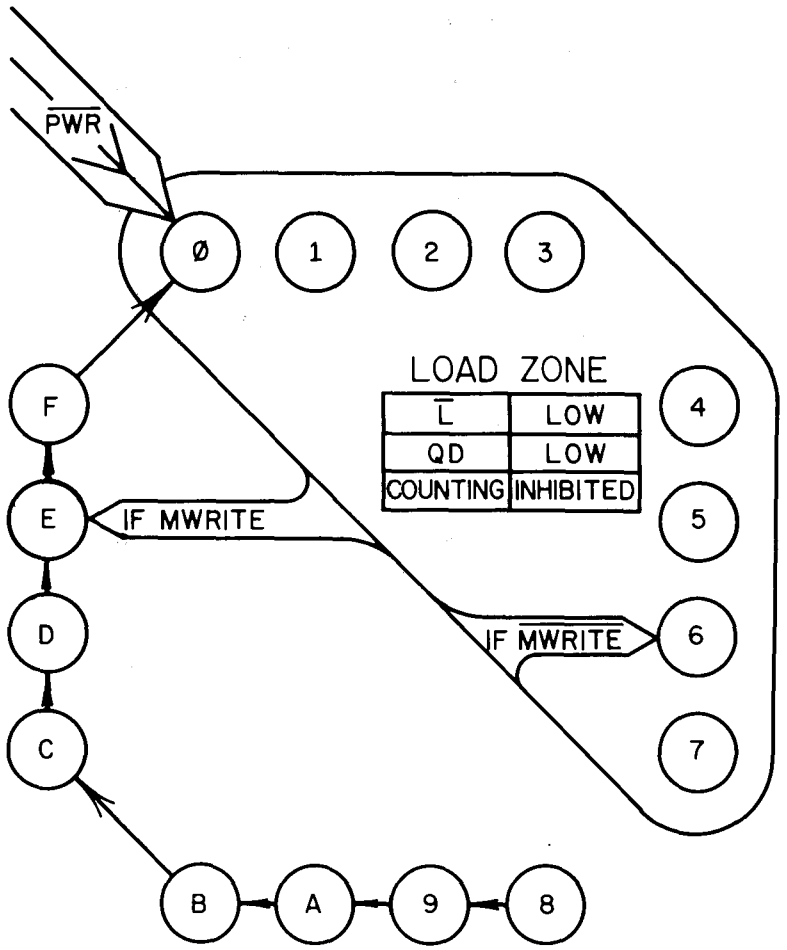
The DEPOSIT pulse is normally ORed with $\overline{PWR}$ to produce MWRITE which is the write strobe used by memory.

The memory module is expected to do the indicated storage in response to MWRITE. It is also expected to place the stored result on the DI bus so that it may appear on the front panel data lights confirming the results to the operator. With most dynamic RAMs this requires a read cycle after the write cycle; thus the memory board must distinguish between MWRITE due to $\overline{PWR}$ (normal processor write) and MWRITE due to Deposit.

5.5.3 Refresh

The refresh request counter (of the Bus Interface and Control Logic (7)) is a 74LS163 (U44). It counts PHASE 2 cycles. The terminal carry is used to produce RFRQ (Refresh Request) which is used by the state machine to request a refresh. REFR goes high when the refresh actually occurs. The clock at the end of terminal carry loads the counter to the complement of the required count. This preset number is established by the manufacturing optional configuration module (9) which varies with the memory ICs used.

A CMOS 4040 provides a 9-bit Refresh Counter (10) (U43) which counts on the trailing edge of Refresh. The low order six outputs, RØ-R5, deliver a refresh row address to the Address Multiplexer. R6 is optionally used for row or column address or page selection. R7 is used for page selection; R8 is used optionally for page selection. Their use depends upon the requirements of the memory ICs used. This selection is established by the optional configuration module (A1).



IF IN LOAD ZONE, STATE ON NEXT CLOCK WILL BE:

	IF $\overline{PWR}$ HIGH	IF $\overline{PWR}$ LOW
IF MWRITE HIGH	E	Ø
IF MWRITE LOW	6	

If E, then F, then Ø. Or, if $\overline{PWR}$, then Ø.

MWRITE • $\overline{\overline{PWR}}$ produces two periods of DEP followed by one period of $\overline{DEP}$.

Fig. 5-3. States of the Synchronous Counter Producing DEPOSIT.

5.6 EXTENDED ADDRESSING

5.6.1 Types of Extended Addressing

The 8080 and most other microprocessors used in S-100 bus systems are able to address a memory space of 2 to the 16th power addresses (about 65 thousand). There are a number of methods in use or proposed which extend the memory addressing capability beyond 2 to the 16th. This is often described as "bank selection."

The 48KRA-1 memory module is equipped with optional circuitry which will accommodate many different extended addressing methods. Once the details of the particular method are known, it is implemented by installing wires, ICs, and component carriers in the empty locations at the lower right corner of the board. This circuitry is referred to as Extended Selection Logic (8) in the block diagram, Fig. 7-1. Extended addressing methods which can be supported by the memory module can be classified by the methods by which the extended address is supplied to the memory board:

1) The extended address is supplied on a group of S-100 lines assigned to this purpose.

   A. The extended address is "encoded," i.e., it consists of a number less than 2^n represented by the 2^n combinations of the n signals.

   B. The extended address is "decoded," i.e., it consists of a number less than or equal to n, represented by an "active" signal on one or none of the n lines.

2) The extended address is supplied to the memory module by an OUT instruction which addresses the selected memory module as an output port. The address arrives at the memory board via the data bus (DO).

   A. Encoded (as in example 1).

   B. Decoded (as in example 1).

3) The extended address is supplied to the memory module on the data bus (DO) during SYNC. It is to be captured and latched by the memory module from the computer's DO lines in the same way that Status is captured and latched by the CPU from the processor's Data lines.

   A. Encoded (as in example 1).

   B. Decoded (as in example 1).

The memory module can be configured to respond to any of these three classes of extended addresses. Whatever the method used, the extended address is examined by the circuit and reduced to a single signal, $\overline{\text{ESEL}}$ which enables the memory module if low, and disables it if high. $\overline{\text{ESEL}}$ is not the same as $\overline{\text{PHANTOM}}$. The two are independent of one another.

5.6.2 Circuit Operation of the Extended Selection Logic

This circuit examines a group of signals in one of a large number of configurations, and condenses the signals into one single yes or no signal, $\overline{\text{ESEL}}$. Because of its convergent nature it is easier to understand if it is examined from output to input, contrary to the usual practice. $\overline{\text{ESEL}}$ is the essential product of this process. If $\overline{\text{ESEL}}$ is low, the memory module will be selected and will respond as expected of a normal memory module. If $\overline{\text{ESEL}}$ is high, the memory module will not respond to either memory read or memory write signal sequences on the S-100 bus. It will, however, continue to refresh itself and maintain its contents. It will be ready for use when selected again.

5.6.3 Modification Guidelines for Extended Selection Logic

(Refer to Fig. 7-4, 48KRA-1 Assembly, for references to Areas A through D and lettered jumper pads.)

How to Produce ESEL

In the standard memory module $\overline{\text{ESEL}}$ is driven by an inverter (U55-6). The input of the inverter (U55-5) is held at +5 V by R9. The output holds $\overline{\text{ESEL}}$ low and the module is always enabled. Several simple two-bank and one of n-bank schemes can be implemented using this inverter and the option pads at its input and output. If the inverter input is to be wired to an S-100 line, R9 should be removed to avoid loading the S-100 line unnecessarily.

For most extended addressing methods you will need to cut the trace between $\overline{\text{ESEL}}$ and U55-6 (Area B, pads 2 and 3) and install a jumper connecting $\overline{\text{ESEL}}$ to U65-9, 10, 11 or 12, (Area C, pads 1, 2, 3 and 4) and install a device in socket U65. (Refer to Areas B and C on the 48KRA-1 Assembly, Fig. 7-4.) For most methods the device installed in U65 will be a programmed PROM. For some simple methods, a component carrier with wire jumpers may suffice. U65 will normally be a 74S287 or 74S387. These are fusible link programmable read only memories. They have eight inputs, two disables, and four outputs. Each output can be programmed (permanently) to produce any function of eight input variables, controlled on an on-or-off basis by two more variables, the disables. Only one output will normally be needed. The other three can be left unprogrammed for later use, or can be programmed with alternate patterns to minimize the number of varieties of ROMs needed. The desired pattern is selected by the output jumper connecting U65, pads 9, 10, 11 or 12 to $\overline{\text{ESEL}}$ (Areas B and C).

The 74S287 has 3-state outputs. The 74S387 has open collector outputs. If a pullup resistor is needed, install a jumper between $\overline{\text{ESEL}}$ and R9 near U55. (Refer to the 48KRA-1 Assembly, Fig. 7-4, Area B, pins 1 to 2.)

Wiring the Address Inputs to U65

The eight inputs of U65 must receive the extended address. These may be connected in one of several ways:

1. From an octal latch (74LS374) installed in U67, via jumpers on a component carrier installed in U66.
2. From the "Extended Address," a set of eight S-100 lines via jumpers on a component carrier installed in U64.
3. Via wire jumpers from any other points which may be appropriate.
4. Any combination of the above.

The octal latch, if used, takes its data from the DO Bus at the rising edge of its clock, XADC (Extended Address Clock). XADC is jumper-optioned to nine sources at the lower right corner of the board. (Refer to the assembly drawing, Fig. 7-4, Area D.) The first option is to the signal $\overline{\text{PSYNC}} \bullet \text{PHASE 2}$. If this option is used, extended address will be captured from the S-100 DO Bus just after the PHASE 2 fall during PSYNC. How the extended address gets put on the DO Bus at this time is a problem which must be solved externally to the memory module.

The remaining eight options are the eight outputs of a 74LS138 which may be installed at U68. If one of these eight is chosen, the extended address will be latched from the DO Bus at the leading (falling) edge of $\overline{\text{PWR}}$ during an OUTPUT operation to the selected port. The port number (eight bits, PØ - P7) is specified as follows:

PORT BIT	FROM S-100 BIT	SPECIFIED BY
PØ	A8	Selection of one of eight options at U65 outputs.
P1	A9	
P2	A10	
P3	A11	Selection of All or All to U68-5 by jumper. (Area B)
P4	A12	Decoded at U40 Pin 10 by program in PROM.
P5	A13	
P6	A14	
P7	A15	

Modifying U40

A PROM is required in U40 to decode the high order four bits of the port address. The memory module may be manufactured containing PROMs at U40 inappropriate to this use. You may, therefore, need to substitute a different PROM at U40-10.

Notice that the octal latch used, a 74LS374, is specified by most suppliers to sink 24 mA. This IC is suitable for use as an S-100 bus driver. Thus, one memory module equipped with the latch may be wired to drive the S-100 "Extended Address" bus of up to eight wires, and serve as the memory controller for other memory boards. It also may be used as an output port for any other purpose if not needed for extended addressing.

Disable Inputs to U65

The PROM which generates $\overline{\text{ESEL}}$, has two DISABLE inputs. One of these is driven by PROM U40-9. The other by U39-9. These two PROMS can be programmed so that response by the memory module can be controlled by any one function of S-100 addresses A12-A15 and switches S2, sections 1, 2, 3, 4 and also by any one function of S-100 addresses A12-A15 and switches S2, sections 5, 6, 7 and 8.

In implementing extended addressing, you may need PROMs for U39 and U40 other than those found on a stock memory module.

These disable controls are provided so that extended address selection can be governed in block sizes down to 4K, selectable by manual switch.

The DISABLE inputs of U65 (Pins 13 and 14) can be jumpered to ØV (enabled) and the lines from U39-11 and U40-11 can be jumpered to the A6 and A7 inputs for a more versatile control with only six extended address bits.

Timing of $\overline{\text{ESEL}}$

The eight inputs and two disables of U65 may be driven by virtually any signals which meet certain timing requirements. $\overline{\text{ESEL}}$ must not change while it is being used by the memory module. The rules describing the $\overline{\text{ESEL}}$ timing constraints are summarized as follows:

1. $\overline{\text{ESEL}}$ may change at the falling edge of PHASE 2 during PSYNC.
2. $\overline{\text{ESEL}}$ may change at the falling edge of $\overline{\text{PWR}}$ when SOUT is high.
3. $\overline{\text{ESEL}}$ may change at any time that the S-100 Address may change.

5.7 MODIFICATION FOR 16-BIT DATA WORDS

(Refer to Fig. 7-4, 48KRA-1 Assembly, for lettered option areas.)

Option Area A provides pads which may be useful in S-100 systems which extend or alter the normal data configuration.

The original S-100 configuration provided a DI bus (DATA IN to the CPU) and a DO bus (DATA OUT from the CPU), both eight bits. These are tied together into a single 8-bit data bus in the Sol. The memory module can be modified to provide bits 8-15 so that two memory modules provide 16-bit wide memory for S-100 bus systems. This can be done by defining an additional set of eight lines to be DATA 8-15, and jumpering the memory module's input and output lines

together to these pins in Area A and cutting the connections to the DO and DI S-100 pins.

Alternately it can be done by re-defining the DO and DI sets as DØ-7 and D8-15 and making the appropriate cuts and jumpers.

For systems which wish to mix 16-bit and 8-bit memory or input/output devices, the signals $\overline{\text{SXTRQ}}$ (Sixteen Request), S-100 pin 59, and $\overline{\text{SXTN}}$ (Sixteen Acknowledge), S-100 pin 61 may be provided by adding jumpers AB and CD. (Refer to Fig. 7-4, 48KRA-1 Assembly.) Note that these pin assignments are in conflict with the DATA 8-15 assignments.

Table 5-2. S-100 Bus Signals of the 48KRA-1 Memory Module

SIGNAL	PIN	SOURCE	FUNCTION
A0-A5	*	Processor	Row address for memory.
A7-A11	*	Processor	Column address for memory.
A6, 12, 13	*	Processor	Row or column address depending on memory IC type.
A12-15	*	Processor	Page and 4K block selection.
A16-23	*	Processor or Extended Address Controller	Extended address lines.
DI0-7	*	Memory	(Data In) Read data lines.
DO0-7	*	Processor	(Data Out) Write data lines.
D8-15	*	Any	Extended read data lines.
MWRITE	68	Computer	(Memory Write) Write-strobe to memory.
PDBIN	78	Processor	(Processor Data Bus In) Indirectly enables DI bus drivers during read.
$\overline{\text{PHANTOM}}$	67	Computer	Disables memory (optional) during power-on initialization program.
PHASE 2	24	Computer	Clocks Bus Interface and Control Logic (7).
PSYNC	76	Processor	(Processor Sync) Controls requests for memory operations.
$\overline{\text{PWR}}$	77	Processor	(Processor Write) High during front panel deposit. Low during processor-controlled write.
SINP	46	Processor	(Status Input) Disables certain operations of the Bus Interface, and Control logic (7).
SMEMR	47	Processor	(Status Memory Read) Indirectly enables DI bus drivers (3).
SOUT	45	Processor	(Status Output) Disables certain operations of the Bus Interface and Control Logic.
$\overline{\text{SWO}}$	97	Processor	(Status Write Out) Controls requests for read or write operations of the Bus Interface and Control Logic.
$\overline{\text{SXTN}}$	61	Memory	(Sixteen Acknowledge) Extended data signal used in systems which mix 8- and 16-bit S-100 cards.
$\overline{\text{SXTRQ}}$	59	Computer	(Sixteen Request) Extended data signal used in systems which mix 8- and 16-bit S-100 cards.

*See Fig. 7-2 and 7-3, 48KRA Schematic, for pin number assignments.

Table 5-3. Internal Signals of the 48KRA-1 Memory Module

$\overline{\text{BSEL}}$	(Board Select) Input to state machine.
$\overline{\text{CAS}}$	(Column Address Strobe) Drives all memory ICs, providing timing.
DOC	Data Output Clock) Clocks data to the output register (3).
$\overline{\text{EDO}}$	(Enable Data Output)
$\overline{\text{ESEL}}$	(Extended Select) Enable from Extended Selection Logic (8).
MEM OUT Ø-7	(Memory Output) lines of the memory array.
$\overline{\text{MSEL}}$	(Memory Selected) Signal of the Bus Interface and Control Logic (7).
AØ-6 MUX	(Multiplexed Address) Outputs of the Address Multiplexer (5).
PEND	(Cycle Pending) Output at the State Machine (7).
$\overline{\text{PSEL}}$	(Page Select)
$\overline{\text{RAC}}$	(Row Address Clock) Clocks the $\overline{\text{RAS}}$ drivers (4), and the column address register (7).
RA DECODER	(Refresh Address Decoder)
RAE	(Row Address Enable) when high, causes the address multiplexers (5) to present the row address. Clocks the write data registerr (1).
$\overline{\text{RAS1}}$ - $\overline{\text{RAS4}}$	The four Row Address Strobe lines to the four pages of memory ICs. One or none of these will be active in any one cycle, providing timing and selection to pages.
REFR	(REFResh) State machine output which specifies refresh (when high).
REN	(Row ENable) State machine output which Enables the $\overline{\text{RAS}}$ drivers.
RFRQ	(Refresh Request) Refresh counter output.
$\overline{\text{WE}}$	(Write Enable) Output of the state machine which specifies a write cycle (when low), a read cycle when high.
$\overline{\text{WRR}}$	(WR Reclocked) Output of the Deposit counter. This signal is produced by reclocking $\overline{\text{PWR}}$, an S-100 bus signal.
XADC	(Extended Address Clock) Signal produced by the Extended Selection Logic (8) governing latching of the extended address from the DO bus.

SECTION 6

MAINTENANCE AND DIAGNOSTICS

6.1 SERVICE

Should you encounter a problem in using the memory module, first consult the manual for a possible solution. If you are still unable to solve the problem or if you have subsequent failures which you cannot service yourself, ask your dealer for help. Service on all Processor Technology equipment, in or out of warranty, is the responsibility of the selling dealer.

6.2 REPLACEMENT PARTS

Order replacement parts by Processor Technology part number, quantity and complete description (e.g., 6.8 ohm, 1/2 watt, 5% resistor). Your dealer may have a limited selection of replacement parts on hand. Certain standard parts may be available from electronic parts suppliers.

6.3 TROUBLESHOOTING AND DIAGNOSTIC TEST PROGRAMS

The "long" memory test used in Section 4, Memory Test, may be used for trouble-shooting the memory modules and for periodic testing to assure system reliability.

6.4 HARDWARE TROUBLESHOOTING

Fig. 7-5, 48KRA-1 PCB traces, can be useful in signal-path tracing. This figure shows the traces on both sides of the PCB as viewed from the component side, but without the components obscuring the traces.

SECTION 7

DRAWINGS

Table 7-1. Key to System Block Diagram

(The encircled key numbers refer to matching numbers on Fig. 7-1, 48KRA-1 System Block Diagram. For ICs represented and other details, refer to Fig. 7-2 and 7-3, 48KRA-1 Schematic.)

KEY #	NAME OF FUNCTIONAL BLOCK	ICs REPRESENTED
(1)	Write Data Register	U61
(2)	Memory Array	U1 through 24
(3)	Output Register/Drivers	U62, 63
(4)	$\overline{RAS}$ Drivers	U35, U41
(5)	Address Multiplexer	U42, U51-U53
(6)	Page Multiplexer	U33
(7)	Bus Interface and Control Logic	U36 (partially) U44, 46-50, 55-59
(8)	Extended Selection Logic	U60, U64-U68
(9)	Configuration Module	A1
(10)	Refresh Counter	U43
(11)	Refresh Page Decoder	U36
(12)	Page Select Array and Switches	U34, U37 through U39; S1, S2
(13)	Refresh Timer	U44

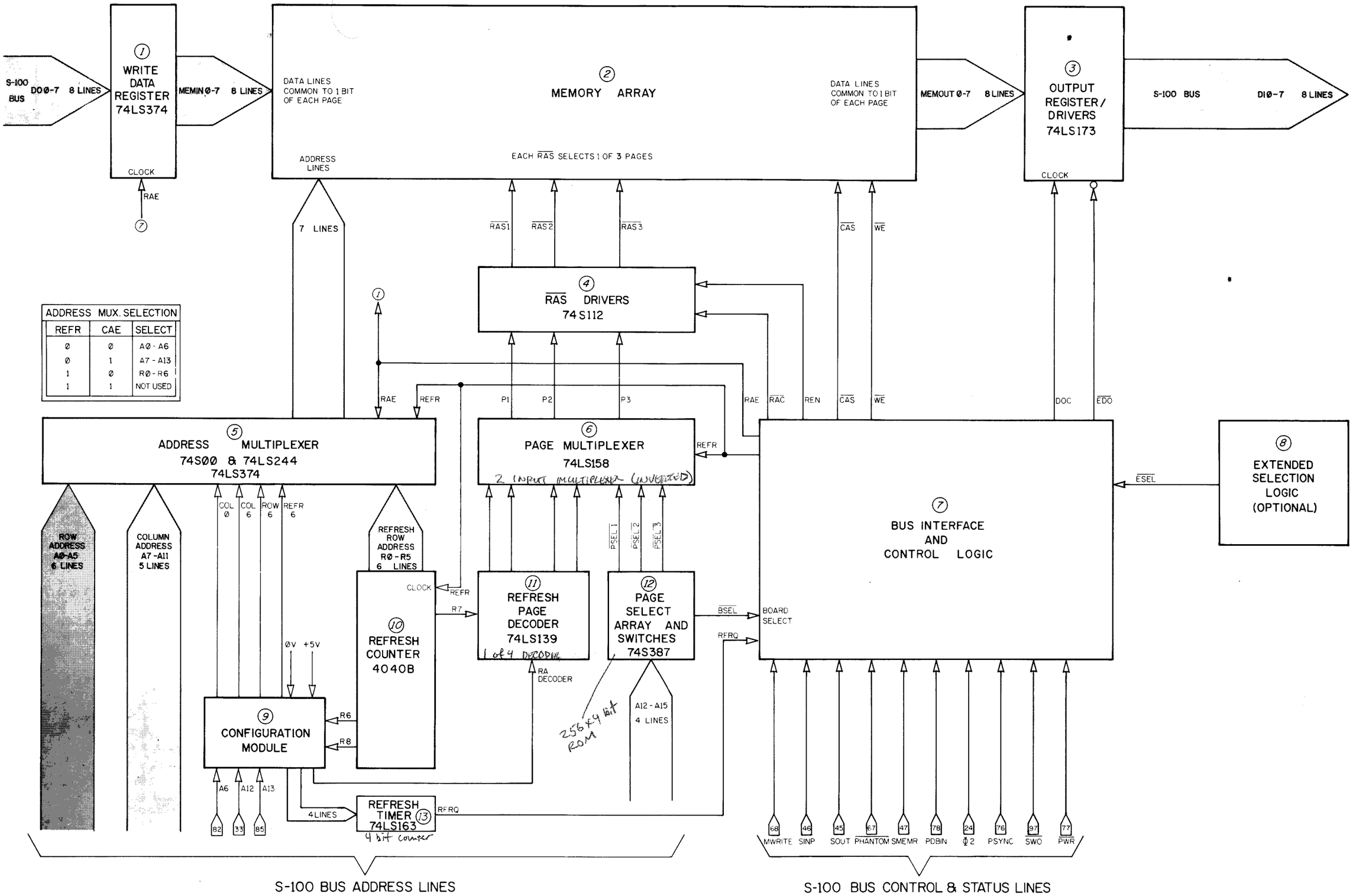


Fig. 7-1. 48KRA-1 System Block Diagram

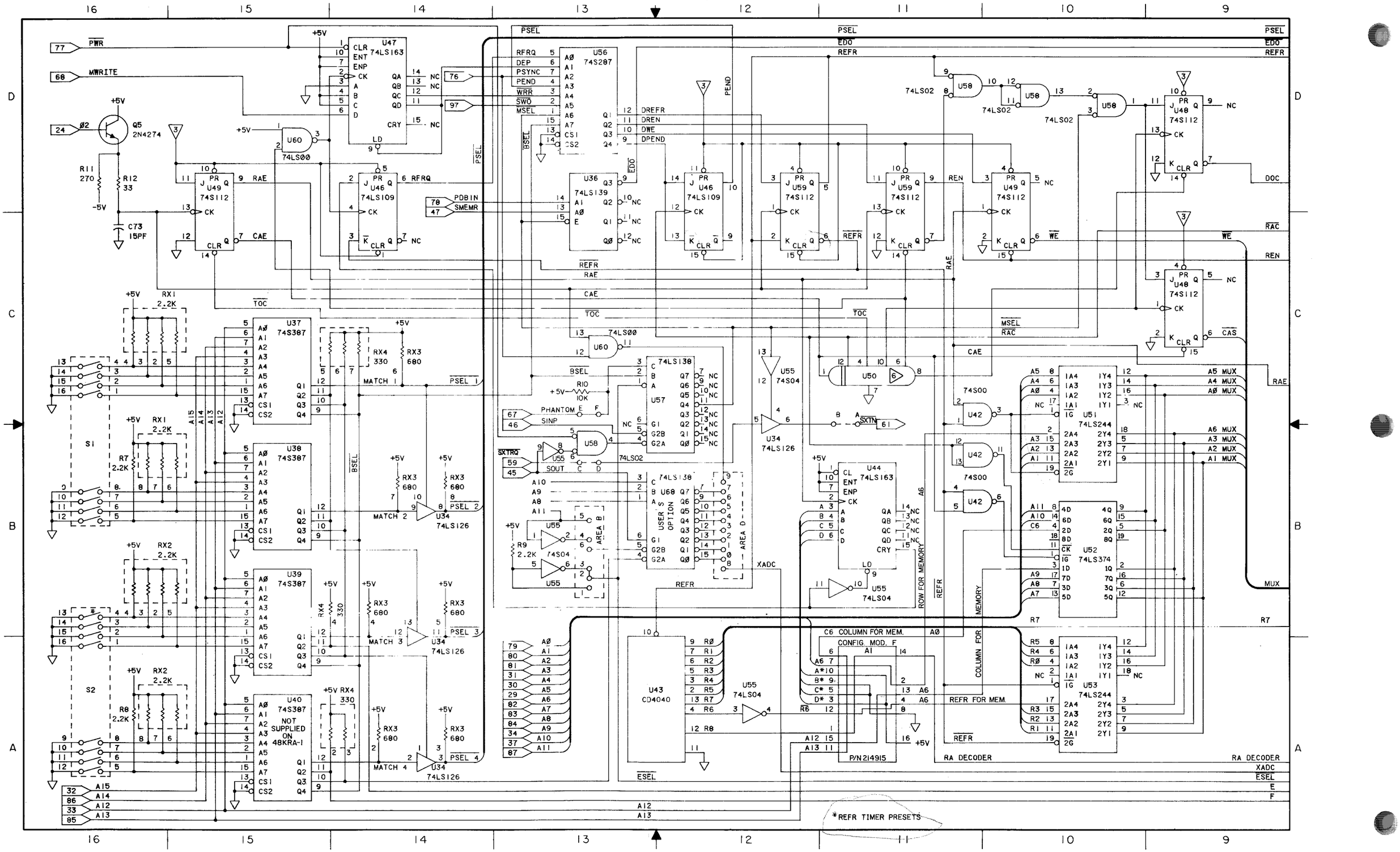
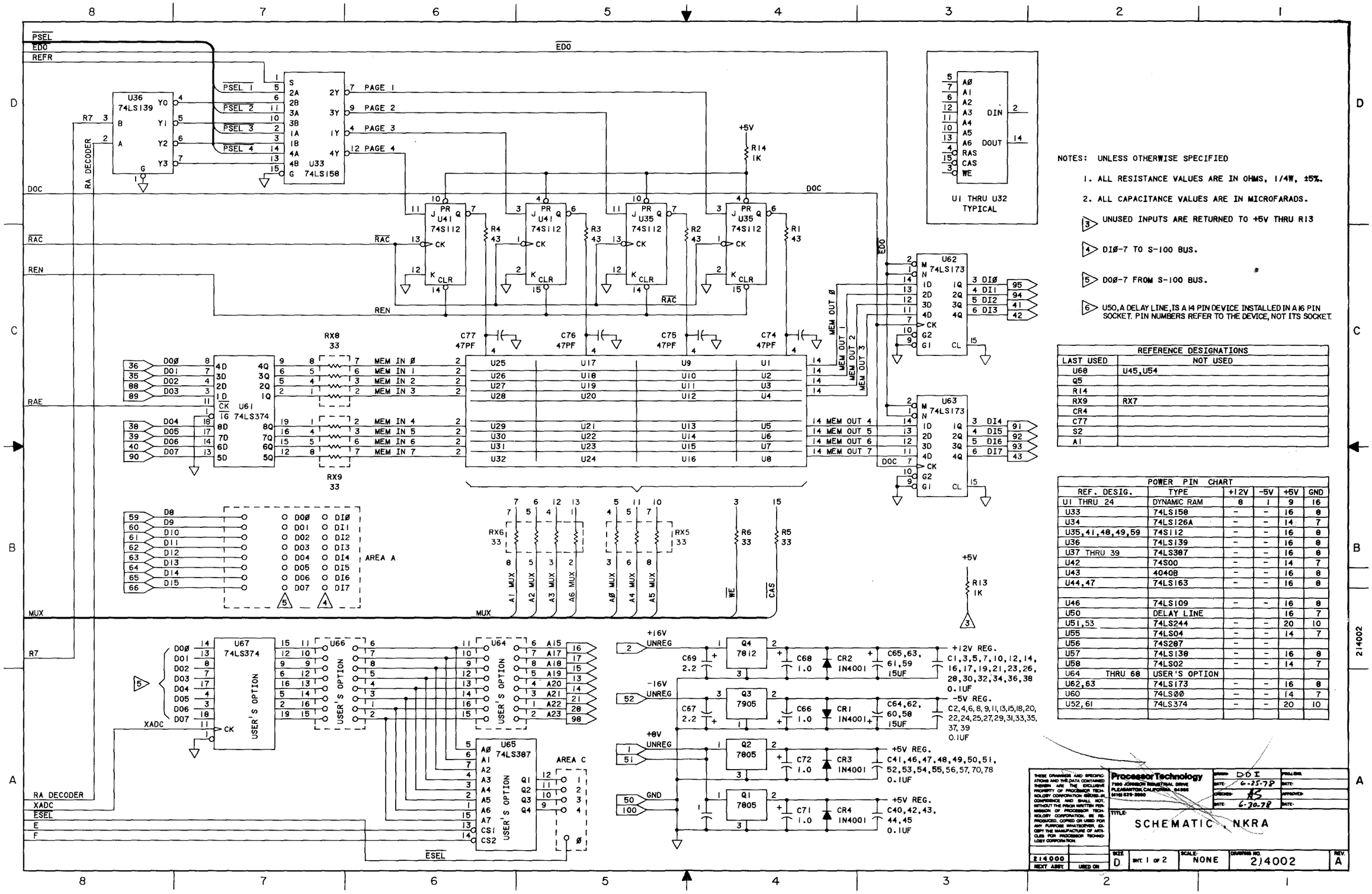


Fig. 7-2. 48KRA-1 Schematic (Sheet 1)



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

(3) UNUSED INPUTS ARE RETURNED TO +5V THRU R13

(4) DIØ-7 TO S-100 BUS.

(5) DOØ-7 FROM S-100 BUS.

(6) U50, A DELAY LINE, IS A 14 PIN DEVICE INSTALLED IN A 16 PIN SOCKET. PIN NUMBERS REFER TO THE DEVICE, NOT ITS SOCKET.

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
U68	U45,U54
Q5	
R14	
RX9	RX7
CR4	
C77	
S2	
A1	

POWER PIN CHART					
REF. DESIG.	TYPE	+12V	-5V	+5V	GND
U1 THRU 24	DYNAMIC RAM	8	1	9	16
U33	74LS158	-	-	16	8
U34	74LS126A	-	-	14	7
U35,41,48,49,59	74S112	-	-	16	8
U36	74LS139	-	-	16	8
U37 THRU 39	74LS387	-	-	16	8
U42	74S00	-	-	14	7
U43	4040B	-	-	16	8
U44,47	74LS163	-	-	16	8
U46	74LS109	-	-	16	8
U50	DELAY LINE			16	7
U51,53	74LS244	-	-	20	10
U55	74LS04	-	-	14	7
U56	74S287	-	-		
U57	74LS138	-	-	16	8
U58	74LS02	-	-	14	7
U64 THRU 68	USER'S OPTION				
U62,63	74LS173	-	-	16	8
U60	74LS00	-	-	14	7
U52,61	74LS374	-	-	20	10

Processor Technology
7100 JOHNSON INDUSTRIAL DRIVE
PLEASANTON, CALIFORNIA 94566
(415) 829-2600

DRAWN: DDI 6-25-78
CHECKED: RS 6-26-78
ENGINEERING:
APPROVED:
DATE:

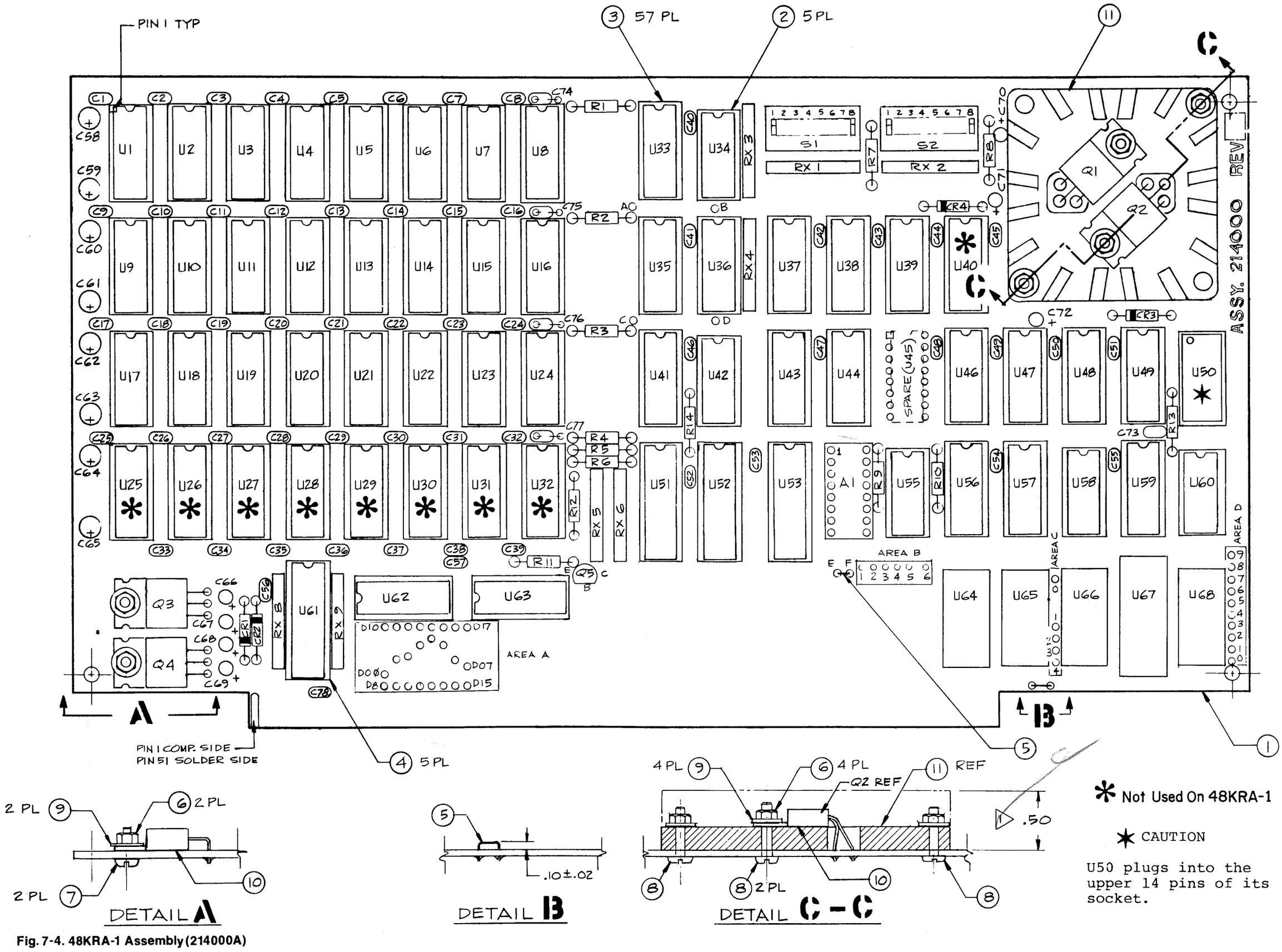
TITLE: SCHEMATIC NKRA

214000 NEXT ASSY. USED ON

SIZE D | SHT. 1 OF 2 | SCALE: NONE | DRAWING NO. 214002 | REV. A

214002

Fig. 7-3. 48KRA-1 Schematic (Sheet 2)

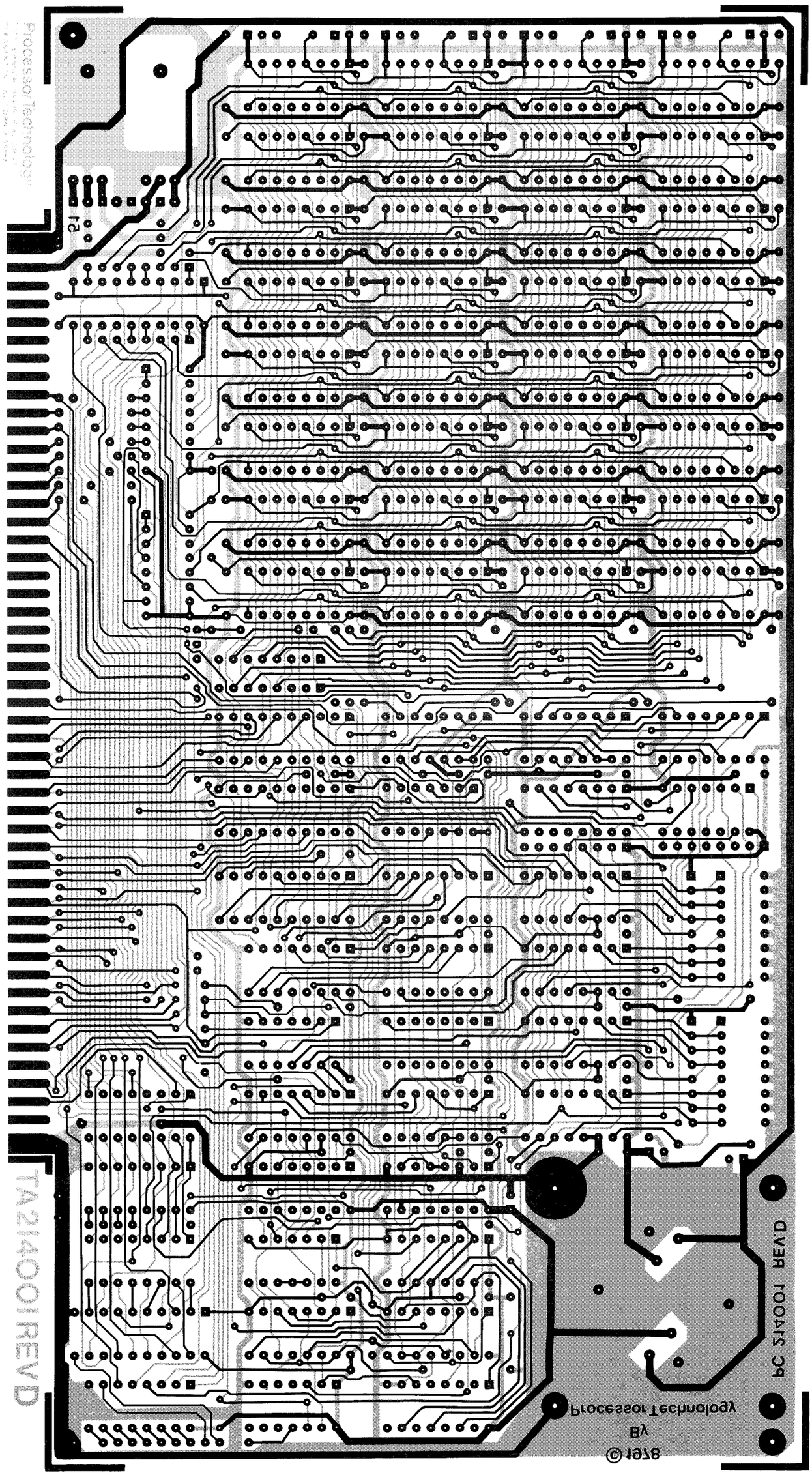


✱ Not Used On 48KRA-1

✱ CAUTION

U50 plugs into the upper 14 pins of its socket.

Fig. 7-4. 48KRA-1 Assembly (214000A)



COMPONENT	WIRING	
+8	+8	1-51
+16	-16	
XRDY	$\overline{\text{SSW DSB}}$	
VI0	$\overline{\text{EXT CLR}}$	
VI1	RTC	5-55
VI2	STSTB	
VI3	DIG1	
VI4	FRDY	
VI5		
VI6		10-60
VI7		
XRDY2		
		15-65
$\overline{\text{STA DSB}}$	MWRT	
$\overline{\text{C/C DSB}}$	$\overline{\text{PS}}$	
UNPROC	PROC	20-70
SS	RUN	
$\overline{\text{ADD DSB}}$	PRDY	
$\overline{\text{DO DSB}}$	$\overline{\text{PINT}}$	
Ø2 CLK	PHOLD	
Ø1 CLK	$\overline{\text{PRESET}}$	25-75
PHLDA	PSYNC	
PWAIT	$\overline{\text{PWR}}$	
PINTE	PDBIN	
A5	A0	
A4	A1	30-80
A3	A2	
A15	A6	
A12	A7	
A9	A8	
DO 1	A13	35-85
DO 0	A14	
A10	A11	
DO 4	DO 2	
DO 5	DO 3	
DO 6	DO 7	40-90
DI 2	DI 4	
DI 3	DI 5	
DI 7	DI 6	
SMI	DI 1	
SOUT	DI 0	45-95
SINP	SINTA	
SMER	SWD	
SHLTA	SSTACK	
$\overline{\text{CLOCK}}$	PDC	
GND	GND	50-100

NOTE:

Both these patterns are viewed from the component side. The component side is the screened pattern. The solid pattern is the trace side.

Fig. 7-5. 48KRA-1 PCB Traces (TA 214001D)

APPENDIX 1

LONG MEMORY TEST PROGRAM (Listing)

```
                        0000 *
C900                    0001        ORG     0C900H
                        0002        XEQ     0C004H
                        0003        LST
                        0004 ***  PROCESSOR TECHNOLOGY 48KRA-1 TEST  ***
                        0005 *
                        0006 *          COPYRIGHT (C) 1978, by
                        0007 *          Processor Technology Corporation
                        0008 *          All rights reserved.
                        0009 *
     C900               0010 BEGIN  EQU     $       **** SETUP I/O ****
C900 2E 04              0011        MVI     L,04H
C902 22 53 CB           0012        SHLD    RTRN1   FOR RETURN TO SOLOS/CUTER
C905 2E 19              0013        MVI     L,19H
C907 22 56 CB           0014        SHLD    SOUT1   FOR SOLOS/CUTER OUTPUT
C90A 2E 1F              0015        MVI     L,1FH
C90C 22 59 CB           0016        SHLD    SINP1   FOR SOLOS/CUTER INPUT
                        0017 *
                        0018 *** ANNOUNCE TEST ***
                        0019 *
C90F 21 7D CA           0020        LXI     H,MSG1  MESSAGE ADDRESS
C912 CD E5 C9           0021        CALL    STRNG   DISPLAY MESSAGE
                        0022 *
                        0023 *** GET CONTINUOUS OR SINGLE PASS MODE
                        0024 *
C915 AF                 0025        XRA     A       SET PASS CONTROL
C916 32 5B CB           0026        STA     CFLAG   FOR 1 PASS
C919 CD F7 C9           0027        CALL    GET     GO WAIT FOR A KEY
C91C FE 43              0028        CPI     'C'     CONTINUOUS MODE ?
C91E C2 28 C9           0029        JNZ     INIT    NOPE.
                        0030 *
C921 F5                 0031        PUSH    PSW     SAVE KEY
C922 3E FF              0032        MVI     A,0FFH  YES
C924 32 5B CB           0033        STA     CFLAG   RAISE FLAG
C927 F1                 0034        POP     PSW     RESTORE KEY
                        0035 *
     C928               0036 INIT   EQU     $       **** INITIALIZATION ****
C928 CD F0 C9           0037        CALL    PUT     ECHO KEY
C92B CD 00 CA           0038        CALL    CRLF
                        0039 *
C92E 21 00 00           0040        LXI     H,0     CLEAR ERROR LOG
C931 22 5E CB           0041        SHLD    ROW1
C934 22 60 CB           0042        SHLD    ROW2
C937 22 5C CB           0043        SHLD    BDADR   TEST BOARD AT ADRS. 0
                        0044 *
```

```
     C93A                0045 CONT   EQU   $       CONTINUOUS MODE LOOPS HERE
C93A 21 37 CB            0046        LXI   H,MSG2  IN PROGRESS MESSAGE
C93D CD E5 C9            0047        CALL  STRNG
C940 97                  0048        SUB   A
C941 32 62 CB            0049        STA   PAGE    PAGE NUMBER = 0
C944 32 63 CB            0050        STA   FILL    STATIC FILLER = 0
                         0051 *
     C947                0052 MAIN   EQU   $       **** MAIN ****
C947 3A 63 CB            0053        LDA   FILL    GET STATIC FILLER
C94A 07                  0054        RLC
C94B CD 39 CA            0055        CALL  WRITE   FILL ONE PAGE
                         0056 *
C94E 97                  0057        SUB   A       MASTER PATTERN = ONE BIT
C94F 37                  0058        STC   .       IN NINE SET TO ONE.
                         0059 *
     C950                0060 LOOP1  EQU   $       **** LOOP 1 ****
C950 F5                  0061        PUSH  PSW     SAVE MASTER PATTERN
C951 CD 0B CA            0062        CALL  NXTPG   GO PAST STATIC TEST PAGE
C954 1E 02               0063        MVI   E,2     TWO PAGES REMAIN
                         0064 *
     C956                0065 TEST1  EQU   $       **** TEST 1 ****
C956 CD 2F CA            0066        CALL  TEST    TEST NEXT PAGE
C959 1D                  0067        DCR   E       REMAINING PAGES TESTED ?
C95A C2 56 C9            0068        JNZ   TEST1   NO, DO NEXT ONE
                         0069 *
C95D 3A 63 CB            0070        LDA   FILL    ELSE  CHECK
C960 07                  0071        RLC   .       STATIC TEST PAGE
C961 CD 52 CA            0072        CALL  READ    FOR DROPPED BITS.
                         0073 *
C964 F1                  0074        POP   PSW     RESTORE MASTER PATTERN
C965 1F                  0075        RAR   .       PERMUTE
C966 D2 50 C9            0076        JNC   LOOP1   REPEAT EIGHT MORE TIMES
                         0077 *
C969 BF                  0078        CMP   A       INVERT BITS OF
C96A 3E FF               0079        MVI   A,0FFH  MASTER PATTERN
                         0080 *
     C96C                0081 LOOP2  EQU   $       **** LOOP 2 ****
C96C F5                  0082        PUSH  PSW     SAVE MASTER PATTERN
C96D CD 0B CA            0083        CALL  NXTPG   SKIP PAST STATIC TEST PAGE
C970 1E 02               0084        MVI   E,2     TWO PAGES REMAIN
                         0085 *
     C972                0086 TEST2  EQU   $
C972 CD 2F CA            0087        CALL  TEST    TEST NEXT PAGE
C975 1D                  0088        DCR   E       REMAINING PAGES TESTED ?
C976 C2 72 C9            0089        JNZ   TEST2   NO, DO NEXT ONE
                         0090 *
C979 3A 63 CB            0091        LDA   FILL    ELSE CHECK STATIC
C97C 07                  0092        RLC   .       TEST PAGE
C97D CD 52 CA            0093        CALL  READ    FOR DROPPED BITS.
                         0094 *
C980 F1                  0095        POP   PSW     RESTORE MASTER PATTERN
C981 1F                  0096        RAR   .       PERMUTE
C982 DA 6C C9            0097        JC    LOOP2   REPEAT EIGHT MORE TIMES
                         0098 *
```

```
C985 CD 0B CA           0099          CALL    NXTPG   REPEAT ENTIRE TEST
C988 3A 62 CB           0100          LDA     PAGE    STARTING WITH
C98B B7                 0101          ORA     A       NEXT PAGE IF WE HAVEN'T
C98C C2 47 C9           0102          JNZ     MAIN    BEEN AROUND 3 TIMES ALREADY.
                        0103 *
C98F 3A 63 CB           0104          LDA     FILL    INVERT FILLER
C992 2F                 0105          CMA     .
C993 32 63 CB           0106          STA     FILL    AND TEST AGAIN
C996 B7                 0107          ORA     A       UNLESS ALREADY DONE.
C997 C2 47 C9           0108          JNZ     MAIN
                        0109 *
C99A CD A7 C9           0110          CALL    MAP     OUTPUT CHIP MAP
                        0111 *
C99D 3A 5B CB           0112          LDA     CFLAG   CONTINUOUS MODE ?
C9A0 B7                 0113          ORA     A
C9A1 CA 52 CB           0114          JZ      RTRN    NO. RETURN TO SOLOS/CUTER
C9A4 C3 3A C9           0115          JMP     CONT    YES. GO AROUND AGAIN
                        0116 *
                        0117 *          *** SUBROUTINES ****
                        0118 *
     C9A7               0119 MAP      EQU     $       **** MAP ****
C9A7 CD 00 CA           0120          CALL    CRLF
C9AA 2A 5E CB           0121          LHLD    ROW1    PAGE 1 & 2 RESULTS
C9AD CD BB C9           0122          CALL    LINE    DISPLAY PAGE 1
C9B0 6C                 0123          MOV     L,H
C9B1 CD BB C9           0124          CALL    LINE    DISPLAY PAGE 2
                        0125 *
C9B4 2A 60 CB           0126          LHLD    ROW2    PAGE 3 RESULTS
C9B7 CD BB C9           0127          CALL    LINE    DISPLAY PAGE 3
C9BA C9                 0128          RET     .       MAP COMPLETE
                        0129 *
     C9BB               0130 LINE     EQU     $       **** LINE ****
C9BB 16 04              0131          MVI     D,4     # OF BIT PAIRS
                        0132 *
C9BD 7D                 0133 PAIR     MOV     A,L     A=RESULTS
C9BE 1F                 0134          RAR     .       CARRY MEANS CHIP HAD ERRORS
C9BF 6F                 0135          MOV     L,A     REMAINING BITS GO BACK
C9C0 CD D9 C9           0136          CALL    CHIP    DISPLAY FIRST BIT OF PAIR
                        0137 *
C9C3 7D                 0138          MOV     A,L     A=RESULTS
C9C4 1F                 0139          RAR     .       TEST BIT,  CARRY IS N.G.
C9C5 6F                 0140          MOV     L,A     RETURN THE REST
C9C6 CD D9 C9           0141          CALL    CHIP    DISPLAY 2ND. BIT OF PAIR
                        0142 *
C9C9 CD D4 C9           0143          CALL    SPAC1   FOR READABILITY
C9CC 15                 0144          DCR     D       LINE DONE?
C9CD C2 BD C9           0145          JNZ     PAIR    NO
                        0146 *
C9D0 CD 00 CA           0147          CALL    CRLF    LINE IS DONE
C9D3 C9                 0148          RET     .       RETURN
                        0149 *
     C9D4               0150 SPAC1    EQU     $       **** SPACE ****
C9D4 3E 20              0151          MVI     A,' '   WRITE A SPACE
C9D6 C3 E0 C9           0152          JMP     MARK1
                        0153 *
```

```
     C9D9              0154 CHIP   EQU    $       **** CHIP ****
C9D9 3E 47             0155        MVI    A,'G'   MARK CHIP 'G'
C9DB D2 E0 C9          0156        JNC    MARK1   IT'S OK, ELSE
C9DE 3E 58             0157        MVI    A,'X'   MARK CHIP 'X'
                       0158 *
C9E0 CD F0 C9          0159 MARK1  CALL   PUT     OUTPUT MARK
C9E3 BF                0160        CMP    A       CLEAR CARRY BIT
C9E4 C9                0161        RET    .       RETURN
                       0162 *
     C9E5              0163 STRNG  EQU    $       **** STRING ****
C9E5 7E                0164        MOV    A,M     GET CHARACTER FROM STRING
C9E6 23                0165        INX    H       BUMP STRING POINTER
C9E7 FE 00             0166        CPI    0       IS IT END MARK ?
C9E9 C8                0167        RZ     .       YES, END OF STRING
C9EA CD F0 C9          0168        CALL   PUT     NO, OUTPUT CHARACTER
C9ED C3 E5 C9          0169        JMP    STRNG   CONTINUE
                       0170 *
     C9F0              0171 PUT    EQU    $       **** OUTPUT ROUTINE ****
C9F0 E5                0172        PUSH   H       SAVE IT
C9F1 47                0173        MOV    B,A     CHAR. TO REG. B
C9F2 CD 55 CB          0174        CALL   SOUT    SOLOS/CUTER OUTPUT
C9F5 E1                0175        POP    H       RESTORE IT
C9F6 C9                0176        RET
                       0177 *
     C9F7              0178 GET    EQU    $       **** INPUT ROUTINE ****
C9F7 CD 58 CB          0179        CALL   SINP    CHECK FOR CHAR.
C9FA CA F7 C9          0180        JZ     GET     NONE YET
C9FD E6 7F             0181        ANI    7FH     NO PARITY !
C9FF C9                0182        RET
                       0183 *
     CA00              0184 CRLF   EQU    $       **** DO CR AND LF ****
CA00 3E 0D             0185        MVI    A,0DH
CA02 CD F0 C9          0186        CALL   PUT     DO CR
CA05 3E 0A             0187        MVI    A,0AH
CA07 CD F0 C9          0188        CALL   PUT     DO LF
CA0A C9                0189        RET
                       0190 *
     CA0B              0191 NXTPG  EQU    $       **** NEXT PAGE ****
CA0B F5                0192        PUSH   PSW     SAVE
CA0C CD 58 CB          0193        CALL   SINP    CHECK FOR 'ESCAPE' KEY
CA0F FE 1B             0194        CPI    1BH
CA11 CA 52 CB          0195        JZ     RTRN    TO SOLOS/CUTER IF FOUND
                       0196 *
CA14 3A 62 CB          0197        LDA    PAGE    GET CURRENT PAGE NUMBER
CA17 C6 40             0198        ADI    40H     ADD 16K
CA19 FE C0             0199        CPI    0C0H    PAST 3RD. PAGE ?
CA1B C2 1F CA          0200        JNZ    NXTP1   NOT YET
                       0201 *
CA1E AF                0202        XRA    A       YES. BACK TO PAGE 0
                       0203 *
CA1F 32 62 CB          0204 NXTP1  STA    PAGE    SAVE
CA22 F1                0205        POP    PSW     RESTORE
CA23 C9                0206        RET    .       AND RETURN
                       0207 *
```

```
     CA24                0208 GETPG  EQU   $       **** GET PAGE ****
CA24 F5                  0209        PUSH  PSW     SAVE
CA25 3A 62 CB            0210        LDA   PAGE    GET PAGE NUMBER
CA28 2A 5C CB            0211        LHLD  BDADR   BOARD ADDRESS
CA2B 84                  0212        ADD   H       ADD PAGE #
CA2C 67                  0213        MOV   H,A     SET PAGE ADDRESS
CA2D F1                  0214        POP   PSW     RESTORE
CA2E C9                  0215        RET   .       RETURN
                         0216 *
     CA2F                0217 TEST   EQU   $       **** TEST ****
CA2F CD 39 CA            0218        CALL  WRITE   WRITE TEST PATTERN
CA32 CD 52 CA            0219        CALL  READ    AND READ IT BACK
CA35 CD 0B CA            0220        CALL  NXTPG   BUMP PAGE POINTER
CA38 C9                  0221        RET   .       THEN RETURN
                         0222 *
     CA39                0223 WRITE  EQU   $       **** WRITE ****
CA39 F5                  0224        PUSH  PSW     SAVE
CA3A CD 24 CA            0225        CALL  GETPG   GET PROPER HL
CA3D 16 40               0226        MVI   D,40H   COUNT 16K
                         0227 *
     CA3F                0228 WRIT1  EQU   $       **** WRITE 1 ****
CA3F F5                  0229        PUSH  PSW     SAVE WORKING PATTERN
CA40 77                  0230        MOV   M,A     TRY TO STORE
CA41 AE                  0231        XRA   M       IS DATA GOOD?
CA42 C4 6A CA            0232        CNZ   BITER   RECORD BIT IF NOT
CA45 F1                  0233        POP   PSW     RESTORE PATTERN
CA46 17                  0234        RAL   .       PERMUTE
CA47 2C                  0235        INR   L       BUMP STORAGE ADDRESS
CA48 C2 3F CA            0236        JNZ   WRIT1
CA4B 24                  0237        INR   H       BUMP BY 256
CA4C 15                  0238        DCR   D       ENOUGH FOR 16K ?
CA4D C2 3F CA            0239        JNZ   WRIT1   NOPE
CA50 F1                  0240        POP   PSW     RESTORE
CA51 C9                  0241        RET   .       AND RETURN
                         0242 *
     CA52                0243 READ   EQU   $       **** READ ****
CA52 F5                  0244        PUSH  PSW     SAVE
CA53 CD 24 CA            0245        CALL  GETPG   GET PROPER HL
CA56 16 40               0246        MVI   D,40H   COUNT 16K
                         0247 *
     CA58                0248 READ1  EQU   $       **** READ 1 ****
CA58 F5                  0249        PUSH  PSW     SAVE WORKING PATTERN
CA59 AE                  0250        XRA   M       IS DATA STILL GOOD ?
CA5A C4 6A CA            0251        CNZ   BITER   ACCUMULATE ERRORS
CA5D F1                  0252        POP   PSW     RESTORE PATTERN
CA5E 17                  0253        RAL   .       PERMUTE
CA5F 2C                  0254        INR   L       BUMP STORAGE ADDRESS
CA60 C2 58 CA            0255        JNZ   READ1
CA63 24                  0256        INR   H       BUMP BY 256
CA64 15                  0257        DCR   D       ENOUGH FOR 16K ?
CA65 C2 58 CA            0258        JNZ   READ1
CA68 F1                  0259        POP   PSW     RESTORE
CA69 C9                  0260        RET   .       AND RETURN
                         0261 *
     CA6A                0262 BITER  EQU   $       **** BIT ERROR ****
CA6A E5                  0263        PUSH  H       SAVE TEST ADDRESS
CA6B 47                  0264        MOV   B,A     ERROR DATA
```

```
                        0265 *
CA6C 3A 62 CB           0266        LDA     PAGE    GET CURRENT PAGE
CA6F 07                 0267        RLC     .       SHIFT TO
CA70 07                 0268        RLC     .       LOW ORDER
CA71 00                 0269        NOP     .       TWO BITS
CA72 00                 0270        NOP     .
                        0271 *
CA73 21 5E CB           0272        LXI     H,BITS  ERROR LOG ADDRESS
CA76 85                 0273        ADD     L       DISPLACE BY PAGE #
CA77 6F                 0274        MOV     L,A
CA78 7E                 0275        MOV     A,M     GET ACCUMULATED ERRORS
CA79 B0                 0276        ORA     B       ADD NEW ONES
CA7A 77                 0277        MOV     M,A     AND PUT IN LOG
                        0278 *
CA7B E1                 0279        POP     H       RESTORE TEST ADDRESS
CA7C C9                 0280        RET     .       AND RETURN TO TEST
                        0281 *
CA7D 0B                 0282 MSG1   DB      0BH     CLEAR SCREEN
CA7E 20 20 20 20        0283        ASC     "        PROCESSOR TECHNOLOGY 48KRA-1 TEST"
     20 20 20 50
     52 4F 43 45
     53 53 4F 52
     20 54 45 43
     48 4E 4F 4C
     4F 47 59 20
     34 38 4B 52
     41 2D 31 20
     54 45 53 54
CAA6 0D 0A              0284        DW      0A0DH
CAA8 43 4F 50 59        0285        ASC     "COPYRIGHT (C) 1978,"
     52 49 47 48
     54 20 28 43
     29 20 31 39
     37 38 2C
CABB 20 50 52 4F        0286        ASC     " PROCESSOR TECHNOLOGY CORP."
     43 45 53 53
     4F 52 20 54
     45 43 48 4E
     4F 4C 4F 47
     59 20 43 4F
     52 50 2E
CAD6 0D 0A              0287        DW      0A0DH
CAD8 0D 0A              0288        DW      0A0DH
CADA 54 59 50 45        0289        ASC     "TYPE 'C' TO RUN CONTINUOUSLY"
     20 27 43 27
     20 54 4F 20
     52 55 4E 20
     43 4F 4E 54
     49 4E 55 4F
     55 53 4C 59
CAF6 20 41 4E 44        0290        ASC     " AND ACCUMULATE ERRORS."
     20 41 43 43
     55 4D 55 4C
     41 54 45 20
     45 52 52 4F
     52 53 2E
CB0D 0D 0A              0291        DW      0A0DH
```

```
CB0F 53 54 52 49      0292        ASC    "STRIKE ANY OTHER KEY TO RUN ONE PASS."
     4B 45 20 41
     4E 59 20 4F
     54 48 45 52
     20 4B 45 59
     20 54 4F 20
     52 55 4E 20
     4F 4E 45 20
     50 41 53 53
     2E
CB34 0D 0A            0293        DW     0A0DH
CB36 00               0294        DB     0
                      0295 *
CB37 34 38 4B 52      0296 MSG2   ASC    "48KRA-1 TEST IN PROGRESS"
     41 2D 31 20
     54 45 53 54
     20 49 4E 20
     50 52 4F 47
     52 45 53 53
CB4F 0D 0A            0297        DW     0A0DH
CB51 00               0298        DB     0
                      0299 *
                      0300 *** VECTORS TO SOLOS/CUTER ***
                      0301 *
CB52 C3               0302 RTRN   DB     0C3H   JMP OP. CODE
CB53                  0303 RTRN1  DS     2      RETURN ADDRESS GOES HERE
CB55 C3               0304 SOUT   DB     0C3H   JMP OP. CODE
CB56                  0305 SOUT1  DS     2      OUTPUT ADDRESS GOES HERE
CB58 C3               0306 SINP   DB     0C3H   JMP OP. CODE
CB59                  0307 SINP1  DS     2      INPUT ADDRESS GOES HERE
                      0308 *
                      0309 *             ****  SCRATCH PAD AREA  ****
                      0310 *
CB5B                  0311 CFLAG  DS     1      IF CONTINUOUS MODE = 0, ELSE 1
CB5C                  0312 BDADR  DS     2      TEST BOARD ADDRESS
     CB5E             0313 BITS   EQU    $      ERROR MAP FOLLOWS
CB5E                  0314 ROW1   DS     2      ERROR LOG FOR TOP ROW
CB60                  0315 ROW2   DS     2      ERROR LOG FOR BOTTOM ROW
CB62                  0316 PAGE   DS     1      CURRENT PAGE
CB63                  0317 FILL   DS     1      STATIC TEST BYTE
                      0318 *
                      0319 *** END OF 48KRA-1 TEST ***
```

APPENDIX 2

SHORT MEMORY TEST PROGRAM (Listing)

```
                        0000 *
C900                    0001        ORG     0C900H
                        0002        XEQ     0C004H
                        0003 *
                        0004 ** 48KRA-1 SHORT MEMORY TEST **
                        0005 *
                        0006 *  Copyright (C) 1978, by
                        0007 *  Processor Technology Corporation
                        0008 *  All rights reserved.
                        0009 *
C900 2E 04              0010        MVI     L,4
C902 22 47 C9           0011        SHLD    RTRN    FOR RETURN TO SOLOS/CUTER
                        0012 *
C905 AF                 0013        XRA     A
C906 37                 0014        STC     .       CREATE MASTER PATTERN
C907 F5                 0015        PUSH    PSW     SAVE IT ON STACK
C908 F5                 0016        PUSH    PSW     AND A COPY TO WORK WITH
                        0017 *
C909 21 00 00           0018 LOOP   LXI     H,0     FILL MEMORY FROM 0 TO BFFF
                        0019 *
C90C F1                 0020 WRITE  POP     PSW     GET WORKING PATTERN
C90D 77                 0021        MOV     M,A     TO MEMORY
                        0022 *
C90E 17                 0023        RAL     .       NEW PATTERN
C90F F5                 0024        PUSH    PSW     BACK TO STACK
                        0025 *
C910 23                 0026        INX     H       NEXT MEMORY ADDRESS
C911 7C                 0027        MOV     A,H
C912 FE C0              0028        CPI     0C0H    PAST BFFF ?
C914 C2 0C C9           0029        JNZ     WRITE   NOT YET
                        0030 *
C917 F1                 0031        POP     PSW     WORKING PATTERN
C918 F1                 0032        POP     PSW     MASTER PATTERN
C919 F5                 0033        PUSH    PSW     BACK TO STACK
C91A F5                 0034        PUSH    PSW     AND A COPY TO WORK WITH
                        0035 *
C91B 21 00 00           0036        LXI     H,0     CHECK FROM 0 TO BFFF
                        0037 *
C91E F1                 0038 READ1  POP     PSW     GET WORKING PATTERN
C91F F5                 0039        PUSH    PSW     THEN SAVE IT
C920 BE                 0040        CMP     M       DOES MEMORY MATCH ?
C921 C2 36 C9           0041        JNZ     ERROR NO. IT'S WRONG !
                        0042 *
C924 F1                 0043        POP     PSW     GET WORKING PATTERN
C925 17                 0044        RAL     .       NEW WORKING PATTERN
C926 F5                 0045        PUSH    PSW     BACK TO STACK
                        0046 *
```

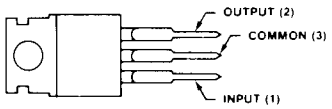
```
C927 23              0047         INX    H       NEXT MEMORY ADDRESS
C928 7C              0048         MOV    A,H
C929 FE C0           0049         CPI    0C0H    PAST BFFF ?
C92B C2 1E C9        0050         JNZ    READ1   NOT YET
                     0051 *
C92E F1              0052         POP    PSW     WORKING PATTERN
C92F F1              0053         POP    PSW     MASTER PATTERN
C930 17              0054         RAL    .       NEW MASTER
C931 F5              0055         PUSH   PSW     BACK TO STACK
C932 F5              0056         PUSH   PSW     AND A COPY TO WORK WITH
C933 C3 09 C9        0057         JMP    LOOP    ON AND ON
                     0058 *
C936 56              0059 ERROR   MOV    D,M     GET INCORRECT DATA
C937 5F              0060         MOV    E,A     AND WHAT IT SHOULD BE
C938 EB              0061         XCHG
C939 22 4B C9        0062         SHLD   SAVE+2   TO REPORT AREA
C93C EB              0063         XCHG   .       GET ADDRESS OF ERROR
C93D 54              0064         MOV    D,H
C93E 65              0065         MOV    H,L     PUT IN CORRECT ORDER
C93F 6A              0066         MOV    L,D
C940 22 49 C9        0067         SHLD   SAVE    TO REPORT AREA
                     0068 *
C943 2A 47 C9        0069         LHLD   RTRN    GET SOLOS/CUTER RETURN ADDRESS
C946 E9              0070         PCHL   .       GO THERE
                     0071 *
C947                 0072 RTRN    DS     2
                     0073 *
                     0074 * REPORT AREA:  BYTES ONE AND TWO ARE THE ADDRESS WHERE THE
                     0075 *                ERROR OCCURED,MOST SIGNIFICANT BYTE FIRST.
                     0076 *
                     0077 *                BYTE THREE IS THE CORRECT DATA.
                     0078 *
                     0079 *                BYTE FOUR IS THE ERRONEOUS DATA.
                     0080 *
     C949            0081 SAVE    EQU    $
                     0082 *
C949                 0083         DS     1       BYTE ONE STORED HERE
C94A                 0084         DS     1       BYTE TWO STORED HERE
C94B                 0085         DS     1       BYTE THREE STORED HERE
C94C                 0086         DS     1       BYTE FOUR STORED HERE
                     0087 *
```

APPENDIX 3

IC PIN CONFIGURATIONS (Top View)

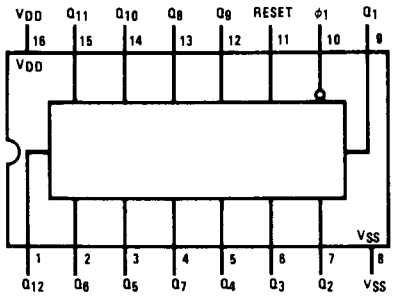
7805, 7812, 7905

U PACKAGE (TO-220)



OUTPUT VOLTAGE	ORDER PART NO.
5V	7805CU/SA7805CU
6V	7806CU/SA7806CU
8V	7808CU/SA7808CU
12V	7812CU/SA7812CU
13 8V	7814CU/SA7814CU
15V	7815CU/SA7815CU
18V	7818CU/SA7818CU
24V	7824CU/SA7824CU

4040B



CD4040BM/CD4040BC

general description

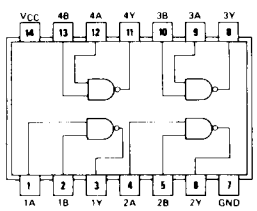
The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

74SØØ

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

00

positive logic:
$Y = \overline{AB}$



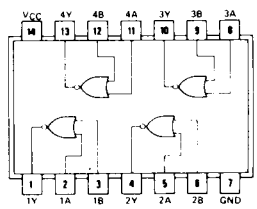
SN5400 (J) SN7400 (J, N)
SN54H00 (J) SN74H00 (J, N)
SN54L00 (J) SN74L00 (J, N)
SN54LS00 (J, W) SN74LS00 (J, N)
SN54S00 (J, W) SN74S00 (J, N)

74LSØ2

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

02

positive logic:
$Y = \overline{A+B}$



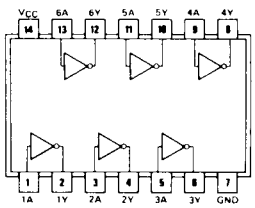
SN5402 (J) SN7402 (J, N)
SN54L02 (J) SN74L02 (J, N)
SN54LS02 (J, W) SN74LS02 (J, N)
SN54S02 (J, W) SN74S02 (J, N)

74LSØ4

HEX INVERTERS

04

positive logic:
$Y = \overline{A}$



SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)

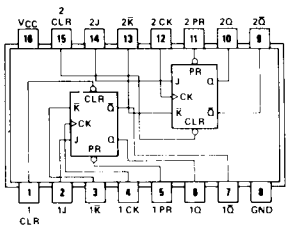
74LS109

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

109

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$



SN54109 (J, W) SN74109 (J, N)
SN54LS109A (J, W) SN74LS109A (J, N)

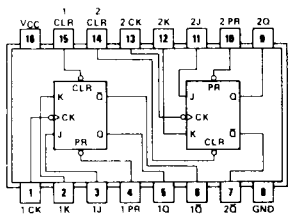
74S112

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

112

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	Q_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	Q_0



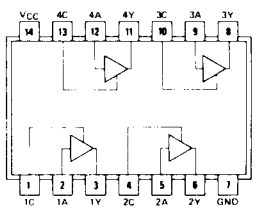
SN54LS112 (J, W) SN74LS112 (J, N)
SN54S112 (J, W) SN74S112 (J, N)

74LS126

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

126

positive logic:
Y = A
Output is off (disabled) when C is low.

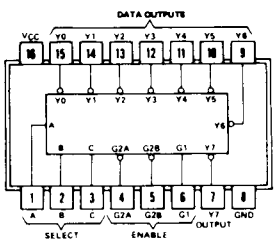


SN54126 (J, W) SN74126 (J, N)
SN54LS126 (J, W) SN74LS126 (J, N)

74LS138

3-TO-8 LINE DECODERS/MULTIPLEXERS

138

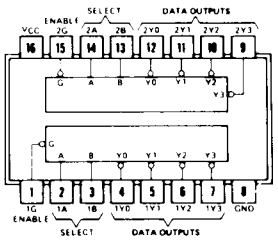


SN54LS138 (J, W) SN74LS138 (J, N)
SN54S138 (J, W) SN74S138 (J, N)

74LS139

DUAL 2-TO-4 LINE DECODERS/MULTIPLEXERS

139



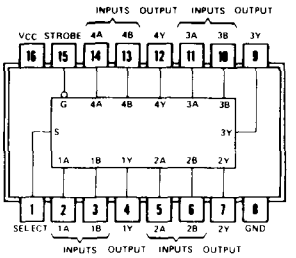
SN54LS139 (J, W) SN74LS139 (J, N)
SN54S 139 (J, W) SN74S139 (J, N)

74LS158

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

157 NONINVERTED DATA OUTPUTS

158 INVERTED DATA OUTPUTS



SN54157 (J, W) SN74157 (J, N)
SN54L157 (J) SN74L157 (J, N)
SN54LS157 (J, W) SN74LS157 (J, N)
SN54S157 (J, W) SN54S157 (J, N)
SN54LS158 (J, W) SN74LS158 (J, N)
SN54S158 (J, W) SN74S158 (J, N)

74LS163

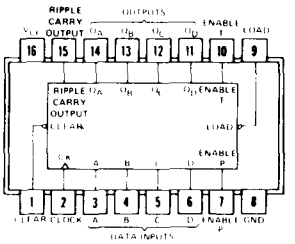
SYNCHRONOUS 4-BIT COUNTERS

160 DECADE, DIRECT CLEAR

161 BINARY, DIRECT CLEAR

162 DECADE, SYNCHRONOUS CLEAR

163 BINARY, SYNCHRONOUS CLEAR

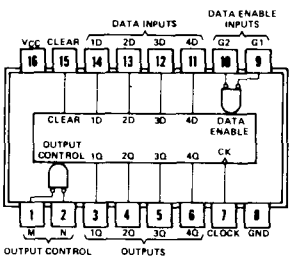


SN54160 (J, W) SN74160 (J, N)
SN54LS160A (J, W) SN74LS160A (J, N)
SN54161 (J, W) SN74161 (J, N)
SN54LS161A (J, W) SN74LS161A (J, N)
SN54162 (J, W) SN74162 (J, N)
SN54LS162A (J, W) SN74LS162A (J, N)
SN54S162 (J, W) SN74S162 (J, N)
SN54163 (J, W) SN74163 (J, N)
SN54LS163A (J, W) SN74LS163A (J, N)
SN54S163 (J, W) SN74S163 (J, N)

74LS173

4-BIT D-TYPE REGISTERS

173 3-STATE OUTPUTS

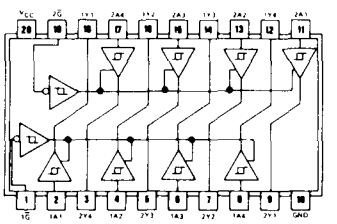


SN54173 (J, W) SN74173 (J, N)
SN54LS173 (J, W) SN74LS173 (J, N)

74LS244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

244 NONINVERTED 3-STATE OUTPUTS

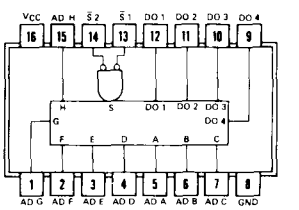


SN54LS244 (J) SN74LS244 (J, N)

74LS287, 74LS387

1024-BIT PROGRAMMABLE READ-ONLY MEMORIES

287 256 4-BIT WORDS
3-STATE OUTPUTS



SN54S287 (J, W) SN74S287 (J, W)