CP/M 2.2 on Sol-20 using Micropolis Mod-I and Mod-II Drives

To create a bootable CP/M disk for the Sol-20 using Micropolis, I started with Lifeboat CP/M 2.2 on a Vector Graphic MZ which uses the Micropolis controller and drives. The Lifeboat CP/M BIOS uses only 8080 code whereas the Vector Graphic version of the BIOS uses Z80 code.

The CONFIG utility for Lifeboat CP/M already has an option for Sol-20 support. This requires that the CONFIG.COM file be present on the target disk for the Sol-20 and that CONFIG.COM be patched to specify the Sol-20 configuration. Here are the steps:

- 1) Run MOVCPM 48 to create a 48K CP/M.
- 2) Run SYSGEN to write the CP/M image to the target floppy.
- 3) Run DDT to patch CONFIG.COM on the target floppy (user entries in **bold**):

```
A>DDT CONFIG.COM
-S120
0120 84 81 (type in 81 here for the Sol-20 and press return)
0121 FF . (type "." and return here to exit memory modify mode)
- (type Ctrl-C to exit to CP/M)
A>SAVE 24 CONFIG.COM
```

The disk is now ready to boot on the Sol-20.

IOBYTE on the Sol-20

CON device (bits 1,0): 00 – TTY, Sol keyboard and display* 01 – CRT on serial port 10 – BAT, not implemented 11 – UC1, user defined	PUN device (bits 5,4): 00 – TTY, Sol display 01 – PTP on serial port* 10 – UP1 on parallel port 11 – UP2, user defined
RDR device (bits 3,2): 00 – TTY, Sol keyboard 01 – PTR on serial port* 10 – UR1 on parallel port 11 – UR2, user defined	LST device (bits 7,6): 00 – TTY, Sol display 01 – CRT on serial port 10 – LPT on parallel port* 11 – UL1, user defined

^{* =} Default IOBYTE

Booting CP/M

Assuming the Micropolis FDC is strapped at the Vector Graphic default of F800, then at the SOLOS monitor prompt type "EX F800" to boot CP/M.

Sol-20 CP/M 2.2 Disk Images for Micropolis

- The disk images CPM22-48K-35T.dsk and CPM22-48K-77T.dsk are bootable CP/M 2.2 disks for the Micropolis Mod-I (35 track) and Mod-II (77 track) drives. CP/M on these disks has a customized USER area (SOLIO.ASM) that makes the DEL key on the Sol-20 keyboard work like a normal backspace. This version also allows fast stepping (3ms vs 30ms) on drives specified as such in the SOLIO source file. Since this version uses a custom USER area that is patched directly into the CP/M image before SYSGEN, the CONFIG program is not required on the disk. The utilities PCGET and PCPUT are included to allow transfer of files between CP/M and a PC using a serial link.
- The disk images SolGames-35T.dsk and SolGames-77T.dsk bootable CP/M 2.2 disks with a number
 of the original Sol-20 games installed. These games have been patched with a CP/M compatible
 loader at the start of the file to allow the program to be launched from the CP/M command line.
 Since most of these games clobber page zero of memory, a computer reset and cold boot of CP/M
 is typically required to re-enter CP/M after playing a game.

CP/M 2.2 above the C000-CFFF "hole" in the Sol-20

The Sol-20 Personality Module (ROM) and video RAM occupy address space from C000-CFFF. This limits the Sol-20 to a 48K CP/M build without modifying the Sol-20 hardware. However, if RAM is installed from D000-F7FF, then CP/M can be placed in the RAM above the Sol-20 hole. This approach requires a few tricks to make all programs operate properly.

The Lifeboat CP/M build is 2200h bytes in length. Performing a "MOVCPM 61" to create a 61K CP/M locates CP/M at D200-F3FF as desired. Initialization code in the BIOS puts the warm boot vector at address zero in RAM and the BDOS entry vector at address five in RAM. Many programs look these addresses to determine the amount of RAM available. However, the values stored there do not account for the hole in RAM starting at C000. To get around this problem, cold start initialization code in the file SOLIO.ASM places a copy of the BIOS jump table at BFCD-BFFF and a jump into the BDOS at BF06. The code then modifies the BIOS to put these addresses into the page zero vectors.

These modifications make the BDOS appear to be at BF06 instead of at A606 (48K build) which makes an additional 6400 bytes of RAM available. The BDOS vector was placed at BF06 instead of BFCA because some programs validate the BDOS vector by making sure the LSB is 06 (e.g., XSUB). In addition to freeing up 6400 bytes of RAM, warm boot doesn't need to reload CP/M because it is never actually overwritten. SOLIO.ASM puts three NOP's in the BIOS where it does the call to reload CP/M in the warm boot routine. Note that CP/M still accesses the disk as part of warm boot to read the directory to detect a change of disk.

When running under the 61K CP/M patch, MOVCPM gives a serial number error (synchronization error). MOVCPM.COM can be patched to disable the serial number check by using DDT MOVCPM.COM to set locations 27A, 27B and 27C to zero (NOP's a jump instruction). Save the patched memory image to disk with SAVE 44 MOVCPM2.COM.