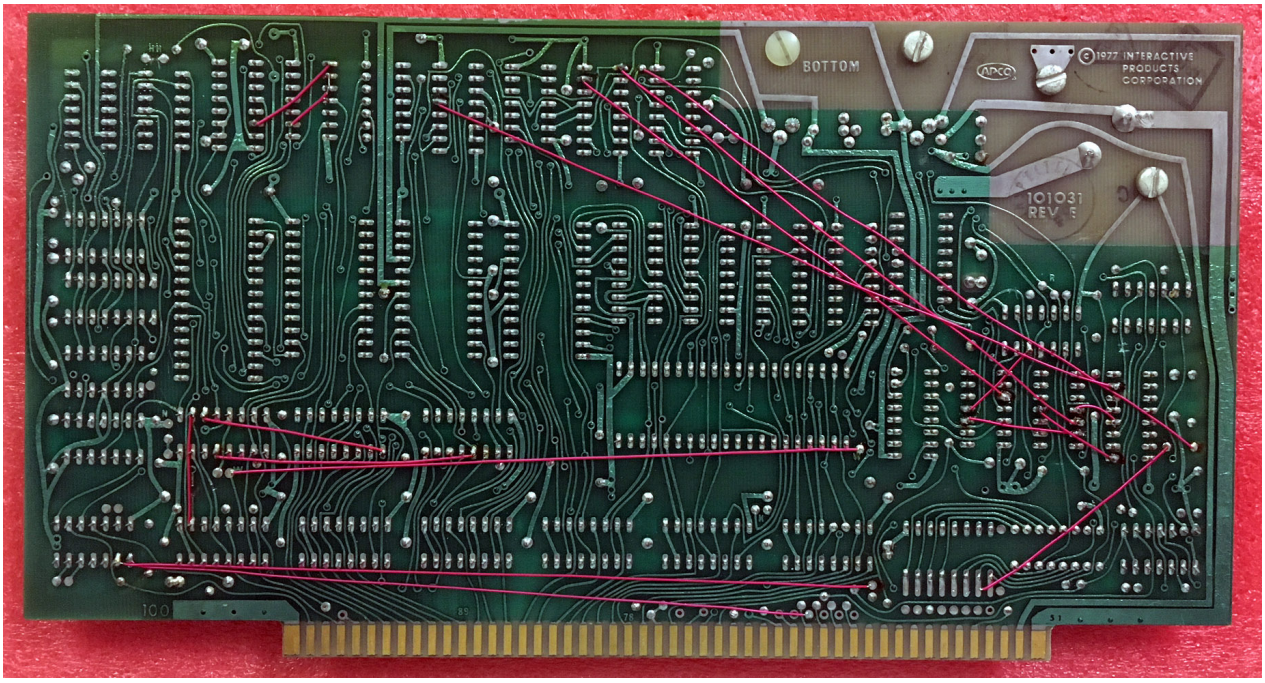
Polymorphic 8813 Mods to Support Polymorphic CP/M

Polymorphic released CP/M for the Poly-8813 in late 1980. Support of CP/M on Polymorphic hardware is difficult because CP/M requires RAM starting at address zero but the Poly CPU board has 3K of PROM starting at address zero. Further, the standard 8813 configuration for System-88 (Exec) places the video board memory and disk controller communication areas between 1000h and 2000h.

In order to run CP/M on the Poly-8813, hardware mods are required to allow run-time swapping of the lower 8K of address space (0000h-1FFFh) between normal 8813 hardware (as listed above) and RAM for CP/M. This is accomplished with modifications to the CPU board, video board, and a memory board. The CPU board is modified to generate a new active low signal on bus pin 16, CPM*. When asserted low, the lower 8K of address is space is RAM. When CPM* is de-asserted (high), the lower 8K of address space is the CPU PROMs, video RAM, etc. The video board is modified to not respond to bus access when CPM* is asserted and a DRAM board is modified to provide 8K of RAM from 0000h-1FFFh that is enabled or disabled under control of the CPM* signal.

CPU Board Modification for CP/M

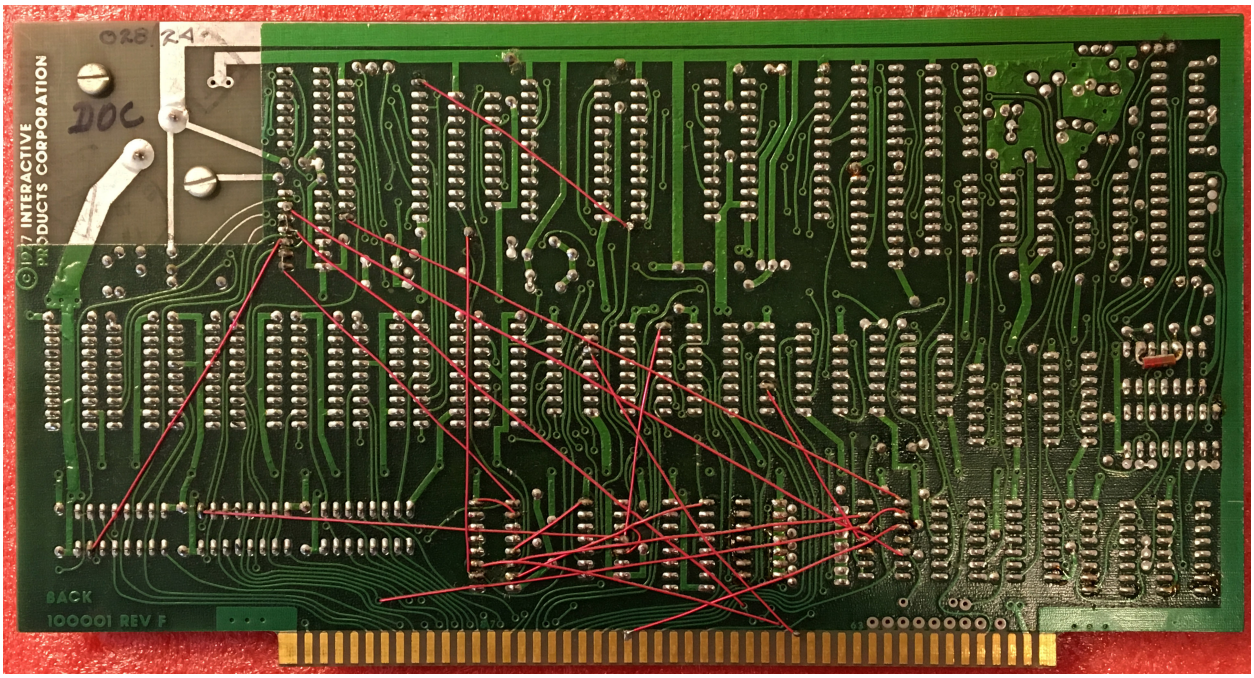
The CPU board mods are detailed in the document “CPU Mods for Poly CP/M.” These mods free up a J-K flip flop in IC10 to use as the CPM* latch. This flip-flop was originally designed to assert bus request (BREQ) in a multi-processor environment but is not used in any standard Polymorphic configurations. An IN from I/O address 0Ch (PS3) asserts CPM* and an IN from I/O address 08h (PS2) de-asserts CPM*. The CPM* signal also disables/enables the CPU’s on-board PROM and RAM when CPM* is asserted/de-asserted. A picture of the CPU board with CP/M mods (along with other typical mods) is shown below.



CPU Board with CP/M (and other) Modifications

Video Board Modifications for CP/M

The only documentation I have found for CP/M mods to the video board assumes a board that has already been modified for the Poly-8813 “Twin System.” The Twin System mod is an extensive mod of over 15 cuts and 15 jumpers that enable one of two video boards at a time based on the state of the Phantom bus line. The additional mod to this board for CP/M is minor and allows the CPM* signal to enable and disable the video board.



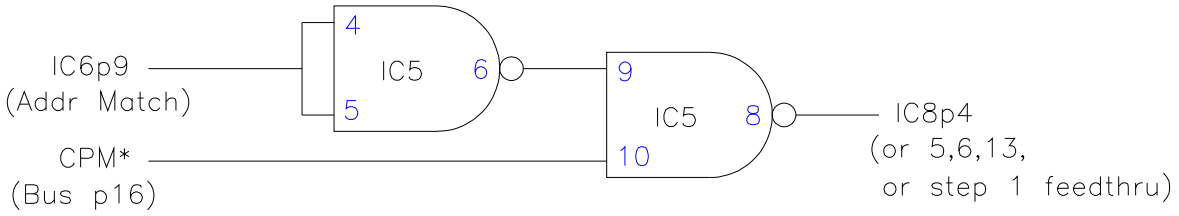
Video Board with Twin System and CP/M Modifications

Starting with a standard video board (not Twin System), much simpler mods to enable/disable the board based on CPM* are possible. The active low output of the address comparator (IC-6) can intercepted, then inverted and NAND’d with the CPM* signal to only pass the address match when CPM* is not asserted.

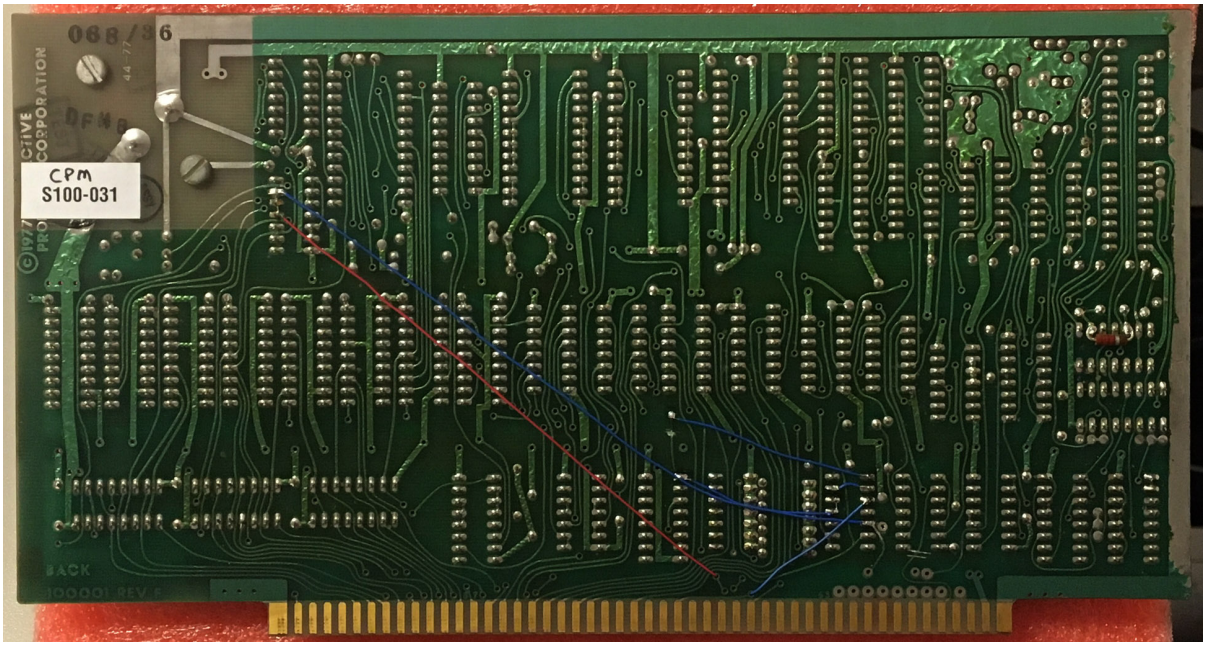
There are three common versions of the video board (1.2, F, and H) and each version typically has a factory installed mod or two based on engineering change orders. Because of this variety, it is hard to create one CP/M mod that works in all cases. The mod shown on the following page is for the version F board and is typical of a mod that can be made to work on any of the boards. The spare NAND gates are typically in IC-42 for version 1.2 and H boards, and in IC-5 for the version F board. Depending on the board version and modifications already present on the board, the output of the final NAND gate connects to IC-8 as shown, or to IC-20p2.

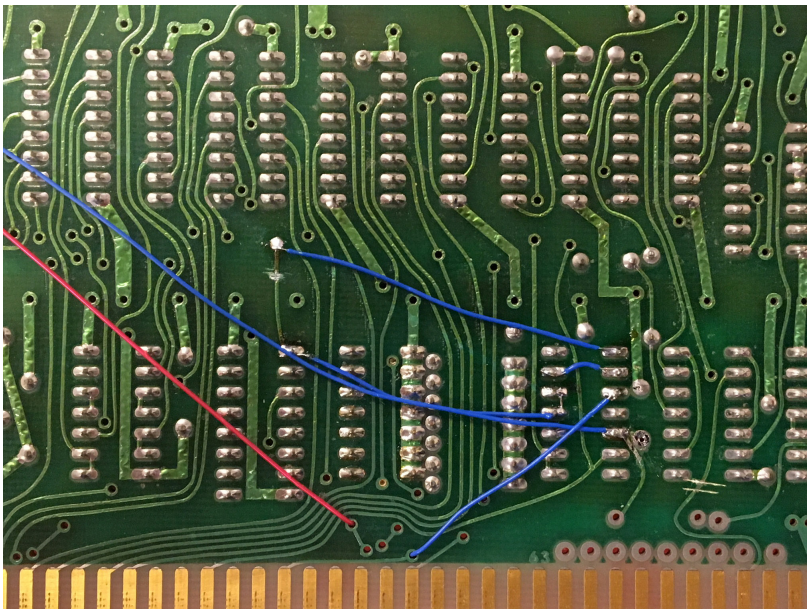
PolyMorphic Version F Video Board
Modification to support CP/M

1) Cut trace on back of PCB from IC6p9 to feedthru.
2) Wire this mod:



The modified video board is shown below. The long red and blue wires are part of a different mod. Only the short blue wires make up the CP/M mod.





RAM Board Modifications for CP/M

A typical 8813 has 48K of RAM that runs from 2000h-DFFFh. This is most often implemented with three of the Poly 16K DRAM boards addressed at 2000h, 6000h, and A000h. The top 8K can optionally be filled with the Poly 8K static RAM board (for example). For Poly CP/M, a few different methods for swapping memory in and out of the 0000h-1FFFh range were implemented.

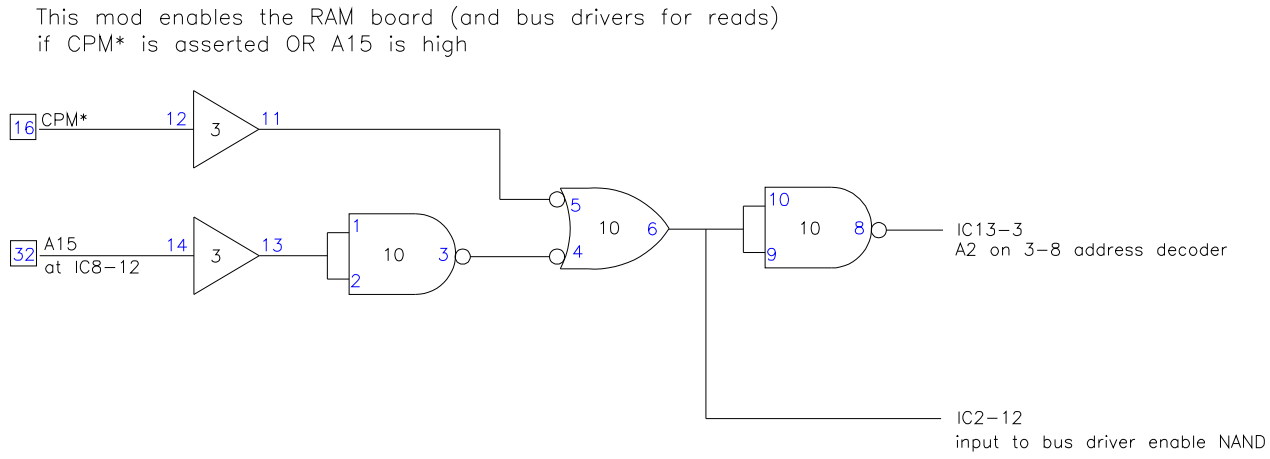
The first solution was an 8K RAM board that appeared at E000h-FFFFh when CPM* was not asserted and at 0000h-1FFFh when CPM* was asserted. I have not seen this board or found documentation for the board.

A second solution was to place the Polymorphic 16K DRAM board at E000h instead of an 8K RAM board. When a Poly 16K DRAM is addressed at E000h, the board wraps around to zero such that the second 8K of the board responds from 0000h-1FFFh. The CP/M mod to this board enables and disables the RAM at 0000h-1FFFh based on the CPM* signal on pin 16. Unlike the 8K board solution, the RAM from E000-FFFFh remains in place independent of the CPM* signal, thus giving a full 64K of RAM to CP/M. Details of this board mod are below.

Finally, a more extensive set of mods to the 16K DRAM board and populating the DRAM sockets with 4116 DRAMs (16K x 1) instead of 4096 DRAMs provided a full 64K of RAM in one board. I'm guessing the CPM* line probably enabled/disabled the bottom 16K of RAM instead of 8K.

16K DRAM Mods to Support Polymorphic CP/M

With the modification shown below, the 16K DRAM board is addressed from E000-FFFF and 0000-1FFF and the RAM from 0000-1FFF is enabled only when CPM* is asserted.



1. Cut trace between IC13-3 and IC13-4 (frees A2 on the 3-8 decoder from ground)
2. Cut trace between IC2-10 and IC2-12 (frees up the fourth input to a 4-input NAND for enabling the data bus drivers for reads)
3. Jumper from bus pin 16 to IC3-12
4. Jumper from IC3-11 to IC10-5

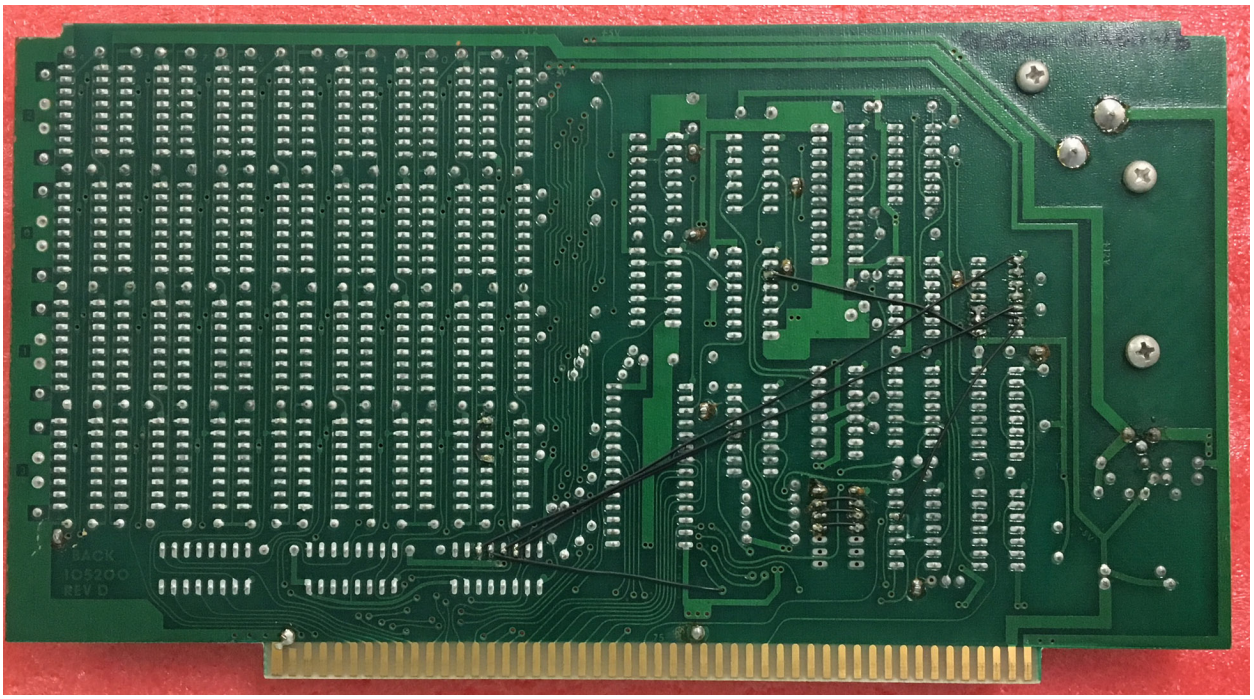
5. Jumper from IC10-6 to IC10-9 and 10
6. Jumper from IC10-6 to IC2-12
7. Jumper from IC10-8 to IC13-3
8. Jumper from IC8-12 to IC3-14
9. Jumper from IC3-13 to IC10-1 and 2
10. Jumper from IC10-3 to IC10-4

The two boards I have seen with this mod also force the board to address E000h by shorting across three of the address DIP switches and cutting one trace:

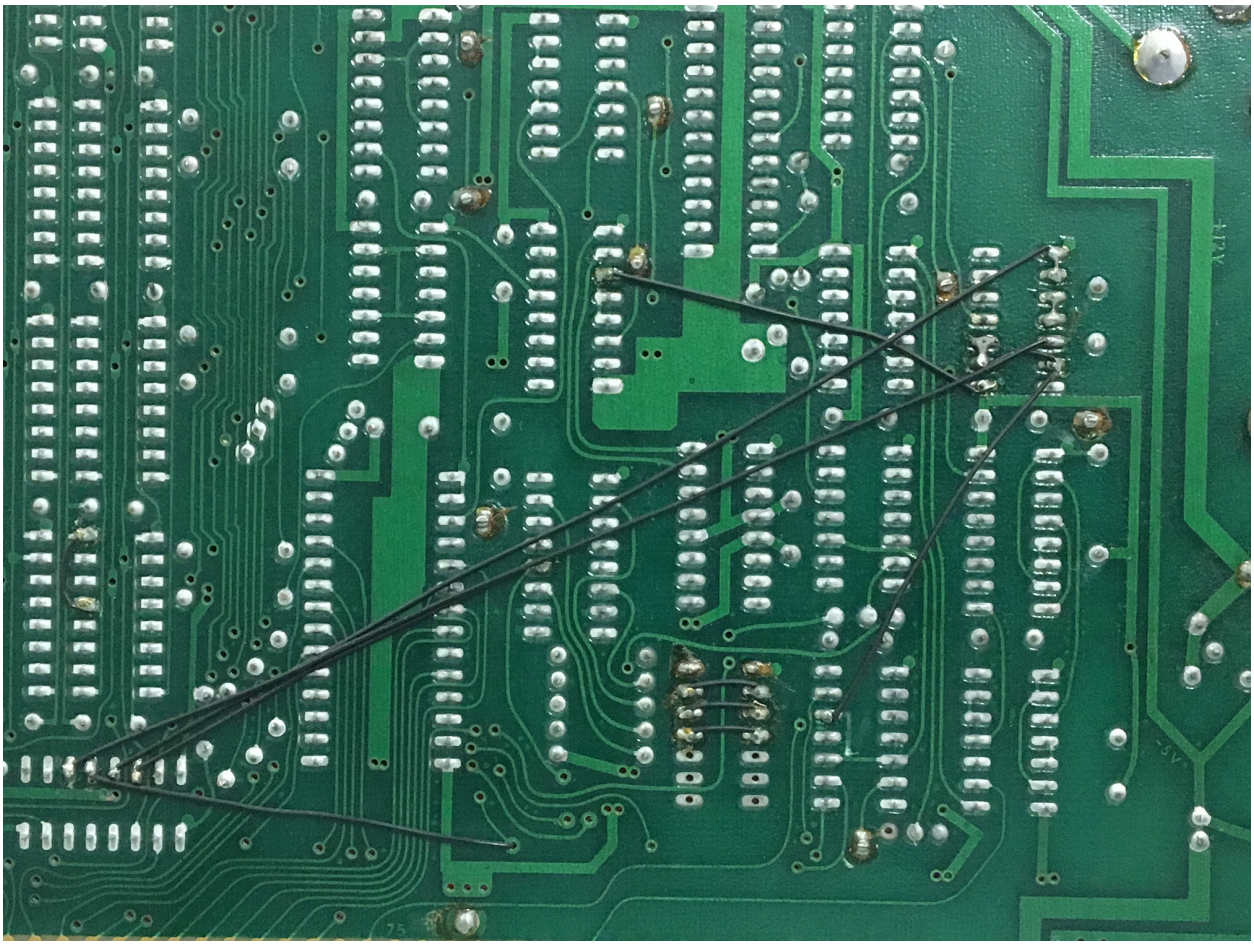
1. Jumper from SW1-2 to SW1-13
2. Jumper from SW1-3 to SW1-12
3. Jumper from SW1-4 to SW1-11
4. Cut trace from SW1 to R20

I also have a 16K DRAM board modified for CP/M that is populated with 4116 DRAMs (16Kx1) instead of 4096's (4Kx1). However, the board is still treated as a 16K board and just 4K of each DRAM chip is used. In the case of this board, the following additional mods are made:

1. Cut trace from IC17-9 on top side of board (leads to CE, pin 13 on all DRAM chips)
2. Jumper from pin 13 to pin 16 on any DRAM chip (grounds MA6 on all DRAMs)



16K DRAM board with CP/M Modifications



Close up of 16K DRAM Modifications for CP/M