Memory Functions of the Poly 88 CPU

1.1 Introduction

Memory external to the CPU board is normally quite simple to use. Memory cards simply plug into the POLY 88 bus after you have selected an appropriate starting address. One exception is the block of memory between addresses ØØØØ hex and ØFFF hex; the CPU disregards any external memory at this address unless you have made the appropriate modification.

1.2 External lower memory.

The CPU hardware modifications necessary for use of a second block of memory at lower addresses is fairly simple, as it was considered when the board was designed. Some memory cards (including those manufactured by PolyMorphic Systems) have "phantom" capabilities on bus pin 67. These offer an advantage when making this modification but are not necessary in many cases. The POLY 88 monitor PROM will be disabled; so some software additions will be necessary. The software additions can be lengthy or short depending on your particular application.

1.3 Hardware changes for external lower memory.

As a general rule, make sure the normal functions of the system are operational before attempting any special alterations. Cut trace "HH" and remove a small section. This trace is near the upper left corner of the CPU board when viewing the bottom (non-component side). Install a jumper (on the non-component side of the

board) between the pad at the right end of the trace "HH" (ungrounded pad) and pad "H" directly above capacitor C9. Pad "H" is labeled only on the component side. Two pads are provided so you can use a jumper to replace trace "HH" if it becomes necessary.

If the memory card you will use as a second block of lower memory has a "phantom" facility at bus pin 67, connect a jumper between bus pin 67 and pin 6 of IC12, on the non-component side of the CPU board. Bus pin 67 has a jumper pad attached, pin 6 of IC12 does not have a jumper pad.

Be sure to double check the connections you make before applying power; misplaced jumpers are a common source of serious damage to integrated circuits.

1.4 Theory behind hardware changes.

IC35 is a 74LS138 3-line to 8-line decoder. Address lines A13 through A15 are decoded by this chip to porduce a LO TTL level signal at one of its outputs. A12 is connected to an active-LO enable input of IC35, thus the chip can produce a LO output only when A12 is LO. When all four address lines are LO (indicating the first 4K of memory), the output at IC35 pin 15 is LO creating an active onboard signal (ONBD-). One function of ONBD- is to provide an enable to IC36, another 3-line to 8-line decoder. IC36 is completely enabled when ONBD- and INTA+ (interrupt acknowledge) are both LO. At this time, address lines A1Ø and A11 are decoded to select 1K of onboard memory (memory select signals = MSØ- through MS3-) or one of four onboard I/O signals (peripheral select signals = PSØ- through PS3-).

The output of IC37 pin 3 determines whether memory blocks or I/O signals are decoded. The output of IC37 pin 3 is HI if an input or output instruction is being executed.

Returning to the discussion of IC35, notice the enable at pin 5 (active LO) is normally grounded through trace "HH". If trace "HH" is broken and pin 5 is connected to pad "H", IC35 is enabled only when A12 and output pin 13 of IC11 are both LO. IC11 pin 13 goes LO when the output of IC37 to pin 3 is LO (indicating neither input nor output instructions are being performed) and IC30 pin 7 is HI.

IC30 is used as a latch to store baud rate, serial device select, and onboard disable status; it will be referred to by the name BRG (baud rate generator latch) for ease of discussion. The BRG output pins continually display the aforementioned status according to Figure 1.

To disable the onboard memory, set bit 5 (of bits Ø through 7) HI in the accumulator and output to port 4 (BRG).

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3E 20       Example: MVI A,2ØH; SET BIT 5 HI
D3 04                OUT 4    ; LATCH NEW STATUS IN BRG
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To re-enable the onboard memory set bit 5 of port 4 LO or press the front panel reset button. The latter resets the BRG and executes the monitor which places a given status in the BRG.

The other hardware change suggested for memory cards having a

"phantom" facility enables the memory card when pin 7 of BRG is HI (onboard memory disable) and disables the memory card when pin 7 is LO (assuming bus pin 67 disables the memory card when HI). The "phantom" facility is not absolutely necessary but without it, writing into onboard memory (including stack ops performed by the monitor) also writes into the corresponding offboard memory location.

Remember, when the onboard memory is disabled, the POLY 88 monitor ROM is disabled. Thus, you must have any necessary control software (such as keyboard input, video display, and cassette tape reader routines) located in memory external to the CPU board.

1.5 Relocation of CPU onboard memory.

The onboard memory address can be shifted up if you do not wish to use the POLY 88 monitor ROM. It is important to remember the POLY 88 monitor will work only if its starting address is ØØØØ.

There are three possible starting addresses that are easily implemented on the POLY 88 CPU, ØØØØ (which is preselected on the PC card), 8ØØØ hex (32K), and E ØØ (56K). If you wish to select a starting location other than ØØØØ, cut trace "J" and remove a small section. Trace "J" is between two closely spaced pads on the non-component side, immediately to the right of IC35. Install a jumper with sleeving between pad "J" (the one nearest the regulators) and pad "R" (which connects to IC35 pin 14 and is labeled "T" in the schematic) for a starting location of 8ØØØ hex; install a jumper between pad "J" (nearest the regulators) and pad "S"(connects to IC35 pin 7) for a starting location of EØØØ hex.

These changes simply create the ONBD- signal when the new memory block address is decoded by IC35.

Figure 1

D5/7	D4/15	D3/2	D2/12	D1/10	DØ/5	ONBD SERIAL DEVICE	IC29 OUTPUT KHZ	÷16 BAUD RATE
L	X	X	X	X	X	E	X	X	X
H	X	X	X	X	X	D	X	X	X
X	L	X	X	X	X	X	Ø	X	X
X	H	X	X	X	X	X	1	X	X
X	X	L	L	L	L	X	X	0	0
X	X	L	L	L	H	X	X	0.800	50
X	X	L	L	H	L	X	X	1.200	75
X	X	L	L	H	H	X	X	1.760	110
X	X	L	H	L	L	X	X	2.152	134.5
X	X	L	H	L	H	X	X	2.400	150
X	X	L	H	H	L	X	X	4.800	300
X	X	L	H	H	H	X	X	9.600	600
X	X	H	L	L	L	X	X	14.400	900
X	X	H	L	L	H	X	X	19.200	1200
X	X	H	L	H	L	X	X	28.800	1800
X	X	H	L	H	H	X	X	38.400	2400
X	X	H	H	L	L	X	X	57.600	3600
X	X	H	H	L	H	X	X	76.800	4800
X	X	H	H	H	L	X	X	115.20	7200
X	X	H	H	H	H	X	X	153.60	9600

H = TTL HI L = TTL LO X = Irrelevant

E = Enabled D = Disabled

D5/7 means the status bit latched from data line D5 and output from BRG pin 7.