Notes about 4mhz CPU with Single Density North Star FDC

The earliest ROMs on the SD controller could not read/boot a disk when running in a 4mhz computer. The loop that waits for sector sync timed out too soon at 4mhz. Later versions of the ROM doubled this loop count (from 70 to 140) so that the boot operation would work. I have one SD controller with 70 in the loop counter (fails to boot at 4mhz) and another with 140 in the loop counter (boots at 4mhz).

Once the system is booted, a new timing issue comes into play. The North Star controller stalls the processor during data reads and writes using the ready line on the S-100 bus. The stall releases the bus cycle as soon as a new byte is available (read from floppy) or the controller is ready for a new byte (write to floppy). Software cannot issue another stalled controller access until one bit time since the last stalled access (8us), otherwise, the new access will not be stalled.

Running at 4mhz, "standard" disk I/O code for the SD controller meets the 8us timing requirement in its read loop. However, the write sector code violates this timing in several places. To fix the problem in CP/M 2.2b for the single density controller, I added 21 delay cycles in the loop that writes the zero-leader before sector data, 8 delay cycles after the sync byte is written, and another 8 delay cycles prior to writing the CRC byte. This allows reliable operation of the SD controller on a 4mhz machine.

I'm not sure what version of NSDOS first supported 4mhz processors with the single density controller, but I have version 2 without the timing mods and version 4 does have the mods. Note that all versions of NSDOS and CP/M for the double-density controller already have the extra delay cycles inserted.