NorthStar™
North Star Computers, Inc.
14440 Catalina St., San Leandro, CA 94577 USA
(415) 357-8500 TWX/Telex (910) 366-7001

32K Ram Board Manual

25018B

24138A

INTRODUCTION

The North Star 32K byte RAM board (RAM-32-A) will operate at full speed with Z80® microcomputers, even with 4 MHz operation, due to the 200 nanosecond access rating for the 16-pin dynamic RAM chip on which the design is based. Parity detect is provided as a standard feature for maximum system integrity. The RAM-32-A may be addressed to any 32K region beginning at an 8K boundary. The RAM-32-A has a bank switching feature which allows more than 64K bytes of RAM to be used in the computer, and also facilitates special software applications, such as timesharing. Be sure to read the CONFIGURATION section, which discusses how to configure the RAM-32-A for each individual application.

CAUTIONS

1. Correct this document from the errata sheets, if any, before doing anything else.

2. DO NOT insert or remove any boards from the computer when the power is on. Note, that power is not completely off until the capacitors have discharged, several seconds after turning off the computer power switch.

3. DO NOT insert or remove IC's from any board while the power is turned on.

WARRANTY

North Star Computers, Inc., warrants the electrical and mechanical parts and workmanship of this product to be free of defects for a period of 90 days from the date of purchase. If such defects occur, North Star Computers, Inc., will repair the defect at no cost to the purchaser. This warranty does not extend to defects resulting from improper use or assembly by purchaser, nor does it cover transportation to the factory. Also, the warranty is invalid if all instructions included in the accompanying documentation are not carefully followed. Any adjustment, modification, or disassembly of any disk drive unit will void the warranty on that disk drive unit. Should a unit returned for warranty repair be deemed by North Star Computers, Inc., to be defective due to purchaser's action, then a repair charge (not to exceed $50 without purchaser's consent) will be assessed. ANY UNIT(S) OR PART(S) RETURNED FOR WARRANTY REPAIR MUST BE ACCOMPANIED BY A DATED COPY OF THE ORIGINAL SALES RECEIPT. The item should be returned to the dealer from whom the product was purchased, for implementation of the warranty. When sending the item to the factory for repair, the dealer must call the North Star Technical Hotline to receive a Return Material Authorization (RMA) number to accompany the item to the factory. Terminals and printers are covered under separate warranties.

The following warranty limitation applies to units located outside the United States of America: All costs and arrangements for transportation of the product to and from the factory are borne entirely by the customer.

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RAM BOARD CHECKOUT

The following terms are used in specifying expected test results:

GND	ground, 0 volts DC
LOW	logic zero, 0-.7 volts, normally about .3 volts
HIGH	logic one, 2.4-5.0 volts, normally about 3 volts
+5V	+5 volts from power supply
AC	Signal with pulses (as opposed to DC signal)

When referring to the name of a signal from the schematic drawings, if the signal is identified with a bar over its name, then the name is followed by a slash (e.g., STORE/) in the checkout instructions. When describing an AC pulse, the notation + or - W,P) refers to a positive or negative pulse with a width of W, appearing over a period of P. For example, a positive pulse with width 120 nanoseconds appearing every 25 microseconds would be described as (+120ns,25us). As a pulse W may be either positive or negative, the notation "plus/minus" will be used as the sign of W.

When using an oscilloscope to test the board, a "scope ground" may be installed by soldering a "bridge" of jumper wire between two of the three PC board holes that connect edge connector pins 50 and 100 near location 13E. Note that either of the two regulator machine screws can also be used for ground test points.

C1. If your computer has a control panel, then check out control panel operation of the RAM-32-A as described in this step. Otherwise, skip to step C2.

   A. Set the address select switches for the region where the RAM-32-A will be used (refer to the Configuration section for details).

   B. With the computer power off, install the RAM-32-A board into the motherboard.

   C. Using the control panel, attempt to deposit the zero value in the first byte of each 8K address region on the board. Then examine the addresses. If the values examined are not all zeros, then skip to step C3. Otherwise, continue at step C2.

C2. If you do not already have a working computer, then skip to step C3. Otherwise, set the address select switches for an available 32K address region (see Configuration section). Then, with the computer power off, install the RAM-32-A board into the computer motherboard. Now, use a memory test program to verify correct operation of the board. If you do not have a memory test program (such as the TM command in the North Star Monitor or RAMTEST3), then use the program listed in Appendix B.

If the RAM-32-A does not fail the memory test after several hours of operation, then the board is operational and you may skip the remaining checkout steps. If systematic data or addressing errors are detected, then refer to the schematic drawings to diagnose and correct the problem. (The correspondence between addresses and RAM chips is given in Appendix C.) If the RAM-32-A does not operate at all, then continue with step C3.

C3. Set the address switches labeled "2", "3", "4" and "5" on the DIP switch (2nd through 5th from the top) to the ON position. The other four switches should be OFF. With the computer power off, install ONLY the processor board and the RAM-32-A into the computer motherboard. Turn on the power and depress and hold down the computer reset switch so that no memory requests are being made.

A. Check the following memory cycle request signals while the computer reset switch is depressed:

Signal	Location	Description
DEPOSIT-CY	4B pin 4	HIGH
STORE/	4B pin 5	HIGH
FETCH/	4B pin 6	HIGH
INSTRUCTION-FETCH/	4B pin 11	HIGH
RUNNING-REFRESH/	6C pin 6	HIGH

If the signals are not as listed, then refer to the schematic drawings and trace backwards to locate and correct the problem.

B. WAITING-REFRESH cycles should occur approximately every 13 microseconds. In the following table, let T refer to the period of PHI 2 in your computer (e.g., 250ns with a 4MHz processor, and 500ns with a 2Mz processor). Check the following signals while the computer reset switch is depressed:

Signal	Location	Description
WRF	2A pin 3	AC, see note 1
WAITING-REFRESH/	1C pin 12	AC, see note 2
CYCLE START/	4B pin 8	AC, (+225ns,13us)
delay tap T1	5A pin 12	AC, (+225ns,13us)
delay tap T2	5A pin 4	AC, (+225ns,13us)
delay tap T3	5A pin 10	AC, (+225ns,13us)
delay tap T4	5A pin 6	AC, (+225ns,13us)
delay tap T5	5A pin 8	AC, (+225ns,13us)
CYC-END/	8A pin 8	AC, (-60ns)
RAS-A/	9A pin 4	AC, (-225ns)
RAS-B/	9B pin 4	AC, (-225ns)

RAS-C/	9C pin 4	AC, (-225ns)
RAS-D/	9D pin 4	AC, (-225ns)
chip address bit 0	9A pin 5	AC, complex signal
chip address bit 1	9A pin 7	AC, complex signal
chip address bit 2	9A pin 6	AC, complex signal
chip address bit 3	9A pin 12	AC, complex signal
chip address bit 4	9A pin 11	AC, complex signal
chip address bit 5	9A pin 10	AC, complex signal

Note 1: (+T,15us) @ 2MHz, (+T) @ 4MHz
Note 2: (-T,15us) @ 2MHz, (-T,13us) @ 4MHz

If the signals are not as listed, then refer to the schematic drawings and trace backwards to locate and correct the problem.

C4. Use the same setup as step C3. If the computer includes an auto-jump capability, then it should be set to jump to some address outside of the range 2000 hex through 9FFF hex (for example, E800 hex or 0). If the processor board has a PROM option at address 0, it should be disabled for this step. With the computer power on, depress and release the reset switch. The processor should repeatedly execute RST 7 instructions (FF hex) from address 38 hex. This should cause memory store requests to all addresses (resulting from the RST instructions stack pushes). Check the following signals:

Signal	Location	Description
INSTRUCTION-FETCH/	4B pin 11	AC, (-220ns,11T)
FETCH/	4B pin 6	AC, see note 1
STORE/	4B pin 5	AC, (-220ns twice,11T)
RUNNING-REFRESH/	6C pin 6	AC, (-260ns, 11T)
RAS-A/	9A pin 4	AC, see note 2
RAS-B/	9B pin 4	AC, see note 2
RAS-C/	9C pin 4	AC, see note 2
RAS-D/	9D pin 4	AC, see note 2
chip write enable	9A pin 3	AC, (-210ns twice,11T)
CAS-A/	9A pin 15	AC, (-210ns thrice,11T)
CAS-B/	9B pin 15	AC, (-210ns thrice,11T)
CAS-C/	9C pin 15	AC, (-210ns thrice,11T)
CAS-D/	9D pin 15	AC, (-210ns thrice,11T)

Note 1: (-70ns,11T) with Z80A, (-160ns,11T) with 8080.

Note 2: Sometimes (-225ns,11T) and sometimes (-225ns thrice,11T).

If the signals are not as listed, refer to the schematic drawings to locate and correct the problem.

L. Power up the computer with the RAM-32-A board installed in the motherboard. Use a program such as the standard HORIZON DOS initialization to store into each byte on the board, to clear all incorrect parity bytes. Again, enable the parity detection by executing the two instructions shown in the previous step. (It is normal for the LED to turn on momentarily during this sequence: it should turn off when the arming instruction is executed.) It should not now be possible to turn on the LED by examining cells on the RAM board. If the LED does turn on, then either the memory is making errors, or there is a problem with the parity logic. Locate and correct the problem before continuing.

CONFIGURATION

This section describes each of the RAM-32-A options which must be configured before the board can be used. Note that configuration of the parity logic and bank switching logic is described in later sections.

ADDRESS SELECTION

Address selection for the RAM-32-A is determined by the switches at location 7A. To configure the RAM-32-A for a contiguous 32K byte region of addresses beginning at an 8K boundary, four adjacent switches should be ON (right side depressed), and the other four switches should be OFF (left side depressed), according to the following table:

Address Region	Switches ON
0000-7FFF	0, 2, 4, 6 (1st through 4th)
2000-9FFF	2, 4, 6, 8 (2nd through 5th)
4000-BFFF	4, 6, 8, A (3rd through 6th)
6000-DFFF	6, 8, A, C (4th through 7th)
8000-FFFF	8, A, C, E (5th through 8th)

Note: Certain groups of non-adjacent 8K address regions starting on 8K boundaries can be selected if, using the following table, at most one switch is ON from each column:

0	2	4	6
8	A	C	E

Note that it is permissible to use less than the entire board: a 24K, 16K, 8K, or 0K board results having 3, 2, 1, or 0 switches ON, respectively.

Z80 COMPATIBILITY

The RAM-32-A must be configured to specify whether it is being used with a Z80 microprocessor. Connect pin 1 to pin 2 on the DIP header at location 7D if Z80 or Z80A operation is required. (Note that pin 1 should be connected to pin 3, if bank switching will not be used.)

SIGNAL GROUNDING

It is strongly recommended that bus pins 20, 61, and 70 be connected to ground on the computer motherboard. Some S-100 computers (e.g., the HORIZON) already do this. For each of the three bus pins that are connected to ground, connect the appropriate "G" jumper on the RAM-32-A. The "G" jumpers are located at positions 2E, 5E, and 6E.

PHANTOM MEMORY

The RAM-32-A board can be used with some area of ROM superimposed over the address region of the board. If the PH jumper (near location 4E) is installed, then a memory reference to the board will inhibited if the backplane signal PHANTOM (motherboard pin 67) is LOW. Do not connect the PH jumper unless you intend to use this feature.

As for the timing of the PHANTOM signal, in general, it should have the same set-up and hold times as address lines. Specifically, the user is responsible for providing a signal that does not change during the RAS strobes.

USING THE PARITY FEATURE

PARITY ERROR ACTION

The action taken when a parity error occurs (when armed) is determined by connecting a jumper wire between "PE" (near location 3E) and one of the following labeled locations:

PINT/	Causes an interrupt request in systems not using vectored interrupts.
NMI/	Causes a non-maskable interrupt request in Z80 computers.
VIO/-VI7	Connecting to one of these eight locations causes a vectored interrupt request at the corresponding priority level.

NOTE: The on-board LED lights whenever a parity error is detected, whether armed or not.

PARITY ERROR ARMING

The parity error logic is disarmed at power-on and reset. The parity error logic can be armed or disarmed under program control by loading a control value into the A-register and executing an OUT 0C0H instruction. Bit 0 of the control value should be 1 to arm the parity logic and 0 to disarm it. Configuration of the DIP header at location 7D will determine which bit (of bits 1-7) in the control value, if 1, will cause arming or disarming of the parity logic for the RAM-32-A. (Arming or disarming the parity error logic also resets the parity error flip-flop.)

Parity Select Bit	Header Configuration
Bit 1	pin 4 to pin 14
Bit 2	pin 4 to pin 11
Bit 3	pin 4 to pin 9
Bit 4	pin 4 to pin 12
Bit 5	pin 4 to pin 10
Bit 6	pin 4 to pin 10 (Standard)
Bit 7	pin 4 to pin 13

Note that the standard HORIZON convention is to use bit 6 for all RAM-32-A boards in the computer. Using this convention, the following two instructions will reset, then arm the parity logic for all the RAM boards:

```
MVI A,41H
OUT 0C0H
```

and the following two instructions will reset and disarm the parity logic:

```
MVI A,40H
OUT 0C0H
```

After power-on, the memory bytes will contain random values (including the parity bit), and not all bytes will have correct parity. Before arming the parity logic, clear all bytes to correct parity by storing into all bytes of RAM. Note that the standard HORIZON DOS initialization performs this function.

USING BANK SWITCHING

At any time, a RAM-32-A may be in one of two "states":

ON — In this state, the board will respond to memory references made to the addresses specified by the address selection switches.

OFF — In this state, the board will ignore all memory references from the processor. However, all values on the board will be retained, and refresh cycles will continue.

Thus, it is possible for more than one board to share the same address region in the computer. However, for any particular address region, at most one RAM-32-A board should be ON at any given moment.

Configuration of the DIP header at location 7D determines if the board powers up in the ON state (connect pin 6 to pin 7) or in the OFF state (connect pin 5 to pin 6).

The RAM-32-A can be turned on or off under program control by loading a control value into the A-register and executing an OUT 0C0H instruction. Bit 0 of the control value should be 0 to turn the board ON, and 1 to turn the board OFF. Configuration of the DIP header at location 7D will determine which bit (of bits 1-7) of the control value, if one, will cause the board to be set:

Select Bit	Header Connection
Bit 1	pin 3 to pin 14
Bit 2	pin 3 to pin 11
Bit 3	pin 3 to pin 9
Bit 4	pin 3 to pin 12
Bit 5	pin 3 to pin 10
Bit 6	pin 3 to pin 8
Bit 7	pin 3 to pin 13

THEORY OF OPERATION

The RAM-32-A consists of a 4 by 9 (parity is included) array of 200ns 8K dynamic RAM chips, plus additional circuitry, which performs the necessary support functions. Refer to the schematic drawings while reading the following theory of operation.

TYPES OF CYCLES

The RAM-32-A employs three types of cycles in its operation. In each case, the cycle is initiated by the CYCLE-START signal, which is passed through the tapped delay module to provide the cycle timing.

1. Normal memory cycles are RAS, CAS cycles, which use some of the bus address signals as row address bits, then others as column address bits. If the signal WE is asserted, a store cycle is performed, otherwise a fetch cycle is performed.

2. Deselect cycles are CAS-only cycles, performed during normal memory cycles on all BUT the selected chips. The CAS without a preceding RAS leaves the output drivers off, so as not to interfere with the data from the selected chips.

3. Refresh cycles are RAS-only cycles, performed by all chips on the board simultaneously. The row address comes from the 74LS393 refresh counter.

CYCLE TIMING

The following is the nominal (disregarding gate delays) timing for a normal memory cycle with respect to CYCLE-START:

Time	Event
0ns	Begin cycle, allow address and control signals to stabilize.
35ns	Begin RAS pulse to selected chips.
60ns	Switch address multiplexers to column inputs.
110ns	Begin CAS pulse to all chips.
215ns	Begin CYC-END pulse.
245ns	Terminate RAS.
320ns	Terminate CYC-END, terminate CAS.

CONDITIONS LEADING TO CYCLE START

1. The INSTRUCTION-FETCH flip-flop is set by the leading edge of SM1. For a Z80 processor, the instruction fetch presents the tightest access requirement (even though SM1 precedes SMEMR).

2. For a Z80 processor, the FETCH flip-flop is set by the leading edge of SMEMR.

3. Note that it is possible to have INSTRUCTION-FETCH and FETCH set simultaneously, a condition which is redundant, but harmless.

4. The STORE flip-flop is set by the leading edge of PWR, unless blocked by SOUT. STORE causes a CYCLE-START and a WE.

5. A control panel deposit is detected as the AND of MWRITE and SMEMR, which causes first a DEP-RQ and then a DEPOSIT-CY. The deposit cycle is delayed if it would otherwise immediately follow a waiting refresh cycle.

6. The RUNNING-REFRESH flip-flop is set by the trailing edge of SM1 and provides refresh cycles when the processor is running. As long as there are 128 instructions executed in any 2ms period, this type of cycle will satisfy the refresh requirements.

7. Whenever 15us (approximately) elapses with no cycles of any kind, the retriggerable one-shot RECENT goes false, allowing a WAITING-REFRESH cycle. This type of cycle, therefore maintains refresh activity when the reset switch is depressed, during long wait states (control panel or North Star disk controller). See the next section for more information.

NOTES ON WAITING-REFRESH

1. The WAITING-REFRESH flip-flop is clocked on the trailing edge of the PHI 2 clock, and is true for one or two clock periods.

2. The refresh cycle is delayed by a DEP-REQ if a control panel deposit cycle is in progress or will start on the next clock cycle. A refresh and a deposit cycle cannot occur on the same or sequential clock cycles.

3. Since some of its input conditions are asynchronous to the PHI 2 clock, the setup can hold times of the WAITING-REFRESH flip-flop, cannot be guaranteed to be met, and there is a small but finite chance that it will go into a momentary indecisive state. For this reason, a network of a resistor, capacitor, and Schmitt gate filter the output to avoid the chance of sending an erroneous pulse down the delay module. Since a Schottky flip-flop is used, the filter slows down the signal by 10-15ns.

4. Whenever the processor resumes computation following a pause, refresh cycles must be inhibited lest one collide with the first memory cycle. The RAM-32-A recognizes three such cases:

   a. At the end of a wait state, the leading edge of PRDY or XRDY sets the WAIT-EXIT flip-flop, inhibiting refresh cycles. If this flip-flop initially comes up true, CLR will reset it.

   b. At the end of an 8080 halt phase (the Z80 maintains SM1 activity while halted) the trailing edge of SHLTA triggers the HLT/RST-EXIT one-shot, inhibiting refresh cycles for a few mircroseconds.

   c. At the end of a system reset, the trailing edge of POC or PRESET, if so jumpered, (whichever occurs last) triggers the same one-shot.

BOARD SELECT AND CHIP SELECT

The RAM-32-A occupies four 8K regions of a 64K byte address space. Address bits A15, A14, and A13 go to a one-of-eight decoder, the outputs of which go to eight switches. The switches are paired, 0 with 8, 2 with A, 4 with C, and 6 with E. The most common configuration would be to have four adjacent switches ON and the other four OFF. However, the four switches need not be adjacent, as long as no more than one of each pair is ON.

The board has four 8K regions corresponding to "lines" of chips labeled A, B, C, and D. (One hesitates to call them "rows" or "columns" because that terminology is used to designate bit arrays within the chips.) For a normal memory cycle, only one line should receive a RAS; other lines do a deselect (CAS-only) cycle. The line selected for a memory cycle is determined by combining decoder outputs while the RAS timing comes from the delay module. Note, however, that during a refresh cycle REF-SEL causes all four lines to receive a RAS, but not a CAS.

Memory cycles to all four lines on the board are inhibited if OCCLUDE is true (see BANK SWITCHING, below), as none of the outputs of the decoder can go low. Similarly, if the PH jumper is installed, all memory cycles are inhibited whenever the backplane signal PHANTOM/ (pin 67) is low. PHANTOM/ is used in some systems to superimpose a ROM over areas normally occupied by RAM.

ADDRESS JUMPERS

The address jumpers satisfy the requirements of six different 8K RAM chip types:

The Intel 2109-56000 must have row address A6 high.
The Intel 2109-56001 must have row address A6 low.
The Mostek 4108-30 must have column address A0 low.
The Mostek 4108-31 must have column address A0 high.
The National 5298A must have row address A5 low.
The National 5298B must have row address A5 high.

BANK SWITCHING

Provision is made for a system with more than 64K bytes of memory by allowing more than one board to occupy a given address region, as long as only one board responds to any memory reference. This is accomplished by the flip-flop OCCLUDE which, if set, makes the entire board "invisible" to the processor.

The OCCLUDE flip-flop may be set or reset by an OUT instruction to port C0 hex. The port number is hardwired and may only be changed by rearranging the address inputs to the board. Data bit 0 goes to the D input of this flip-flop. The clock to the flip-flop may be gated by any of the other seven data bits (selection made by jumper). Thus, we have a theoretical maximum of seven "banks" of 64K, or 14 boards.

The CLR signal can initialize OCCLUDE either ON or OFF.

PARITY

The PARITY-ARM flip-flop is programmed in the same manner as OCCLUDE: its D input comes from data bit 0 and its clock can be gated via a jumper by any of the other seven data bits. The same pulse that clocks PARITY-ARM on its trailing edge clears the PARITY-ERROR flip-flop.

PARITY-ERROR is set during a memory fetch cycle if a byte with even parity is read and, via a driver, lights the on-board LED. The AND of PARITY-ARM and PARITY-ERROR goes to another driver, the output of which the user may wire to one of the eight vectored interrupts, to PINT/, or to NMI/.

The CLR signal initializes the PARITY-ERROR and PARITY-ARM flip-flops off.

CONTROL PANEL OPERATION

Operation of RAM-32-A with a control panel differs from the RAM-16-A: when doing a DEPOSIT function, the deposited data does not show up on the lights. A subsequent EXAMINE must be performed to see the new contents of the memory location.

SPECIAL DMA APPLICATIONS

This section describes modifications for the RAM-32-A which may be necessary for use with such DMA devices as the Cromenco DAZLER™ . These modifications are only needed if the RAM-32-A is being used with a Z80 or Z80A processor board.

D1. If the DMA device is simulating an 8080 memory cycle, D07 must be true during PSYNC. If the device does not drive D07, a pull-up resistor (say, 1K) to Vcc will suffice. A logical place to add this resistor would be at the DMA controller. (North Star processor board version A2 includes such a pull-up.)

D2. Pass signal CC-DSBL/ (backplane pin 19) through an R/C filter delay of 220 ohms and 47 pF, and through the spare 74S00 inverting gate. Take the output of this gate to 7D, pin 1, after first cutting the trace from 7D, pin 1, to ground.

D3. Pass signal PHLDA (backplane pin 26) through the spare 74LS14 inverter. Take the output of this inverter to 2D pin 12 after first cutting from 2D, pin 10, to the feed through near 2D, pin 12.

D4. The desired effect of this change is that, during DMA cycles, the board leaves Z80 mode and cycles start on the condition

PSYNC AND PHI 1 AND CC-DSBL

D5. On the header location 7D, be sure the jumper from pin 1 to pin 2 is installed, as it should be for Z80 operation.

D6. Mark the changes on the schematic drawings.

D7. This is only one example of a DMA application. Different situations may require careful analysis of the transfer of control of the bus from processor to DMA device and back, and of the cycle start conditions.

APPENDIX A

RAM-32-A PC BOARD ASSEMBLY
BILL OF MATERIALS

ITEM	PART #	QTY	DESCRIPTION	DESIG	LOCA
1	01001	60	Capacitor, .047uF Ceramic Disk		A11
2	01002	3	Capacitor, 47 pF Ceramic Disk	C12,C13, C14	2E,12E, 12E
3	01012	1	Capacitor, 33 pF Dipped Mica	C8	1C
4	01017	2	Capacitor, .0047 uF Dipped Mylar	C7,C9	1A,2A
5	01021	1	Capacitor, 2.2 uF Dipped Tantalum	C1	0A
6	01022	5	Capacitor, 6.8 uF Dipped Tantalum	C3,C4, C5,C6	0B 0D
7	01043	1	Capacitor, 2.2 uF, 35 v Dipped Tantalum	C2	0A
8	05006	1	PC Board, RAM-32-A		
9	13026	1	Socket, 14 pin AMP		7D
10	13028	36	Socket, 16 pin AMP		9-17 A-D
11	19002	1	Data Delay Line, (STTLDM 400)new style		5A
12	22001	1	LED, red		0A
13	38002	2	Lockwasher, internal tooth #6		Q4,Q3
14	38011	2	HEX-NUT, 6-32x1/4 AF MS		Q3,Q4
15	38018	2	6-32x3/8 BHMS		Q3,A4

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ITEM	PART #	QTY	DESCRIPTION	DESIG	LOCA
16	38042	1	Heat Sink 6106		Q4
17	38043	1	Heat Sink 6107		Q3
18	43001	1	IC, 74LS00		2B
19	43002	1	IC, 74LS02		4C
20	43006	1	IC, 74LS08		3B
21	43008	1	IC, 74LS12		1B
22	43009	2	IC, 74LS14		1D,2C
23	43011	1	IC, 74LS30		6D
24	43015	1	IC, 74LS74		6C
25	43016	1	IC, 74LS75		6B
26	43017	1	IC, 74LS109		3A
27	43018	1	IC, 74LS123		1A
28	43019	2	IC, 74LS132		1C,3C
29	43033	2	IC, 74LS241		5D,8D
30	43036	2	IC, 74LS258A		3D,4D
31	43043	2	IC, 74LS280		10E,15E
32	43043	1	IC, 74LS373		17E
33	43044	1	IC, 74LS393		5C
34	43045	3	IC, 74S00		7B,7C, 8B
35	43048	1	IC, 74S20		8A
36	43049	1	IC, 74S30		4B
37	43050	1	IC, 74S74		2D

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ITEM	PART #	QTY	DESCRIPTION	DESIG	LOCA
38	43051	1	IC, 74S113		5B
39	43052	1	IC, 74S138		6A
40	43053	1	IC, 74S175		2A
41	43055	1	IC, 7402		4A
42	43066	1	IC, 74542		0A
43	43075	36	IC, 4108-20		9A-17D
44	43014	1	Header Assembly		7D
45	61003	1	Resistor Network, 2.2K ohm, 6 pin SIP	RN2	7A
46	61006	1	Resistor Network, 4.7K ohm, 10 pin SIP	RN1	16E
47	61007	1	Resistor Network, 47 ohm 16 pin DIP	RN3	8C
48	61013	1	Resistor, 220 ohm, 1/4W 5%	R2	0B
49	61014	3	Resistor, 330 ohm, 1/4W 5%	R3,R10, R12	2D,12E
50	61018	1	Resistor, 1K ohm, 1/4W 5%	R4	4B
51	61020	7	Resistor, 2.2K ohm, 1/4W 5%	R1,R8, R9,R11, R13,R14, R15	0A,9E, 3D,6A, 5C,6C, 1B
52	61043	1	Resistor, 270 ohm, 1/4W 5%	R6	1B
53	61044	2	Resistor, 8.2K ohm, 1/4W 5%	R5,R7	1A,2A
54	65002	1	Regulator, 7805	Q4	

ITEM	PART #	QTY	DESCRIPTION	DESIG	LOCA
55	65003	1	Regulator, 7812	Q3	
56	65006	1	Regulator, 79L05	Q1	
57	68006	1	Switch, 8 position DIP	DIP	7A
58	77081	3"	Solid wire, 26 AWG with green PVC insulation		

SUBSTITUTION LIST

1. IC 74LS258 may be substituted for IC 74LS258A on RAM-32 memory boards which use Mostek 4109-30 or 4108-31 and Texas Instruments 4108-20-1 or 4108-20-0 memory IC's.

2. If IC 74S280 is substituted for IC 74LS280, then RN1 must remain 4.7K ohm in conjunction with the substitution.

3. For IC 4108-20, you may use the following as substitutes: IC 4108-21, IC 4108-30, 4108-31, IC 5298-A (National), IC 5298-B (National). 8K RAM chips of different types should not be mixed on any single RAM 32 board. To avoid confusion, each board should include chips of only one type. IC 4108-20 and 4108-30 may be mixed only if absolutely needed. Also, IC 4108-21 and 4108-31 may be mixed only if absolutely needed. If National IC 5298-A chips are used, then: (1) Cut trace A-B; (2) Cut trace C-D; (3) Add jumper A-D; (4) Add jumper B-C; (5) Add jumper 12-C0; (6) Add jumper H-R6. If National 5298-B chips are used, then do (1)-(5), as with 5298-A, but (6) G-R6.

NOTE: If substitution of non-LS parts are permitted, then at most four (4) non-LS parts may be substituted for LS parts on any single PC board.

APPENDIX B

MEMORY TEST PROGRAM

```
0000            *
0000            *SUBROUTINE TO TEST 4K BLOCK OF RAM
0000            * (MUST BE ORIGINED ON 256-BYTE BLOCK BOUNDARY)
0000            *
0000            *ENTER WITH BLOCK ADDRESS IN DE (MUST BE 4K BOUNDARY)
0000            *
0000            *NOTE THAT ERROR ACTION ROUTINE MUST BE SUPPLIED
0000            *
0000 01ED00     TB LXI B,PATTERN    LOAD B,C WITH PATTERN TABLE PTR
0003 60            MOV H,B          LOAD H WITH MSB OF PTR
0004 69         PASS MOV L,C        LOAD L WITH LSB OF PTR
0005            *  BEGIN WRITE FORWARD TO 4K RAM LOOP
0005 7E         WFL MOV A,M         LOAD A WITH NEXT BYTE OF PATTERN
0006 12            STAX D           WRITE IT TO RAM UNDER TEST
0007 2C            INR L            STEP PATTERN PTR
0008 C20E00        JNZ WFI          SKIP IF NOT AT END OF PATTERN
000B 21ED00        LXI H,PATTERN    RESET PATTERN TABLE PTR
000E IC         WFI INR E           STEP RAM PTR
000F C20500        JNZ WFL          LOOP IF NOT AT 256 BOUNDARY
0012 14            INR D            STEP MSB OF RAM PTR
0013 7A            MOV A,D          TEST MSB OF PTR
0014 E60F          ANI 17Q          DONE FILLING 4K?
0016 C20500        JNZ WFL          LOOP IF NOT AT 4K BOUNDARY
0019 7A            MOV A,D          RESET 4K RAM PTR TO BEGINNING
001A D610          SUI 20Q          "     "  "   "   "  "
001C 57            MOV D,A          "     "  "   "   "  "
001D 69            MOV L,C          RESET PATTERN PTR
001E            *  BEGIN READ FORWARD AND COMPARE LOOP
001E 46         RFL MOV B,M         GET PATTERN VALUE
001F 1A            LDAX D           GET BYTE FROM RAM
0020 B8            CMP B            CMP BYTE WITH PATTERN
0021 C46700        CNZ ERROR
0024 2C            INR              STEP PATTERN PTR
0025 C22B00        JNZ RFI          SKIP IF NOT AT END OF PATTERN
0028 21ED00        LXI H,PATTERN    RESET PATTERN TABLE PTR
002B 1C         RFI INR E           STEP RAM PTR
002C C21E00        JNZ RFL          LOOP IF NOT AT 256 BOUNDARY
002F 14            INR D            STEP MSB OF PTR
0030 7A            MOV A,D          TEST MSB OF PTR
0031 E60F          ANI 17Q          DONE WITH 4K REGION?
0033 C21E00        JNZ RFL          LOOP IF NOT AT 4K BOUNDARY
0036            *  END OF READ LOOP
0036            *
```

```
0036            *
0036            *WE HAVE COMPLETED A READ AND WRITE PASS
0036            *NOW TEST BACKWARDS TO CATCH ADDRESSING ERRORS
0036
0036 69            MOV L,C          DECR RAM PTR
0037 1B         WBL DCX D           BEGIN BACKWARDS WRITE
0038 7E            MOV A,M          LOAD NEXT BYTE OF PATTERN
0039 12            STAX D           WRITE IT TO RAM
003A 2C            INR L            STEP PATTERN PTR
003B C24100        JNZ WBI          SKIP IF NOT AT END OF TABLE
003E 21ED00        LXI H,PATTERN    RESET PATTERN PTR
0041 7A         WBI MOV A,D         GET MSB OF PTR
0042 E60F          ANI 17Q          END OF 4K BOUNDARY?
0044 B3            ORA E            "   "  "  "
0045 C23700        JNZ WBL          LOOP IF NOT AT BLOCK BEGINNING
0048 7A            MOV A,D          RESET PTR TO END OF BLOCK
0049 C610          ADI 20Q          "     "   "  "   "  "
004B 57            MOV D,A          "     "   "  "   "  "
004C 69            MOV L,C          RESTORE TABLE PTR
004D 1B         RBL DCX D           READ PASS (BACKWARDS)
004E 46            MOV B,M          PATTERN
004F 1A            LDAX D           DATA
0050 B8            CMP B            COMPARE
0051 C46700        CNZ ERROR
0054 2C            INR L            STEP TABLE PTR
0055 C24B00        JNZ RBI          SKIP IF NOT AT END OF PATTERN
0058 21ED00        LXI H,PATTERN    RESET PATTERN TABLE PTR
005B 7A         RBI MOV A,D         STEP RAM PTR
005C E60F          ANI 17Q          BEGIN TEST
005E B3            ORA E            CONTINUE TEST
005F C24D00        JNZ RBL          LOOP IF NOT AT END OF 4K
0062 0C            INR C            CHANGE PATTERN
0063 C20400        JNZ PASS
0066 C9            RET              ALL DONE WITH TEST
0067            *
```

```
0067
0067            *ERROR ROUTINE (NOT SUPPLIED)
0067            * ON ENTRY, REGISTERS CONTAIN:
0067            *
0067            *  A  VALUE FOUND IN RAM
0067            *  B  VALUE SHOULD HAVE BEEN FOUND
0067            *  C  PASS NUMBER
0067            * DE  BAD BYTE ADDRESS
0067            * HL  ADDRESS OF PATTERN
0067            ERROR DS 206Q         PUT ERROR SUBROUTINE HERE
00ED
00ED            *  ADD YOUR ERROR ROUTINE HERE
00ED
00ED            *
00ED            *PATTERN TABLE
00ED
00ED 00         PATTERN DB 0
00EE 01            DB 1
00EF 02            DB 2
00F0 04            DB 4
00F1 08            DB 10Q
00F2 10            DB 20Q
00F3 20            DB 40Q
00F4 40            DB 100Q
00F5 80            DB 200Q
00F6 AA            DB 252Q
00F7 7F            DB 177Q
00F8 BF            DB 277Q
00F9 DF            DB 337Q
00FA EF            DB 357Q
00FB F7            DB 367Q
00FC FB            DB 373Q
00FD FD            DB 375Q
00FE FE            DB 376Q
00FF FF            DB 377Q           MUST BE END OF 256-BYTE BLOCK
0100            *
```

APPENDIX C

ORGANIZATION OF RAM CHIP ARRAY

The organization of RAM chips on the PC board layout is as follows:

The row 9A-17A responds to the 8K area of addresses within the 16K region selected by the address select switches with first hex digit of 6, 7, E, or F. For example, if the RAM board select switches with silkscreen markings "2", "4", "6", and "8" are ON, then this row responds to addresses in the range of 6000-7FFF hex.

The row 9B-17B responds to the 8K area of the 16K address region with first hex digit of 4, 5, C, or D.

The row 9C-17C responds to the 8K area of the 16K address region with the first hex digit of 2, 3, A, or B.

The bottom row, 9D-17D responds to the 8K area of the 16K address region with first hex digit of 0, 1, 8, or 9.

The columns of RAM chips each correspond to a different bit of each addressed byte:

The column 9A-9D contains the parity bit.

The column 10A-10D contains bit 5 (the 20 hex bit).

The column 11A-11D contains bit 4 (the 10 hex bit).

The column 12A-12D contains bit 6 (the 40 hex bit).

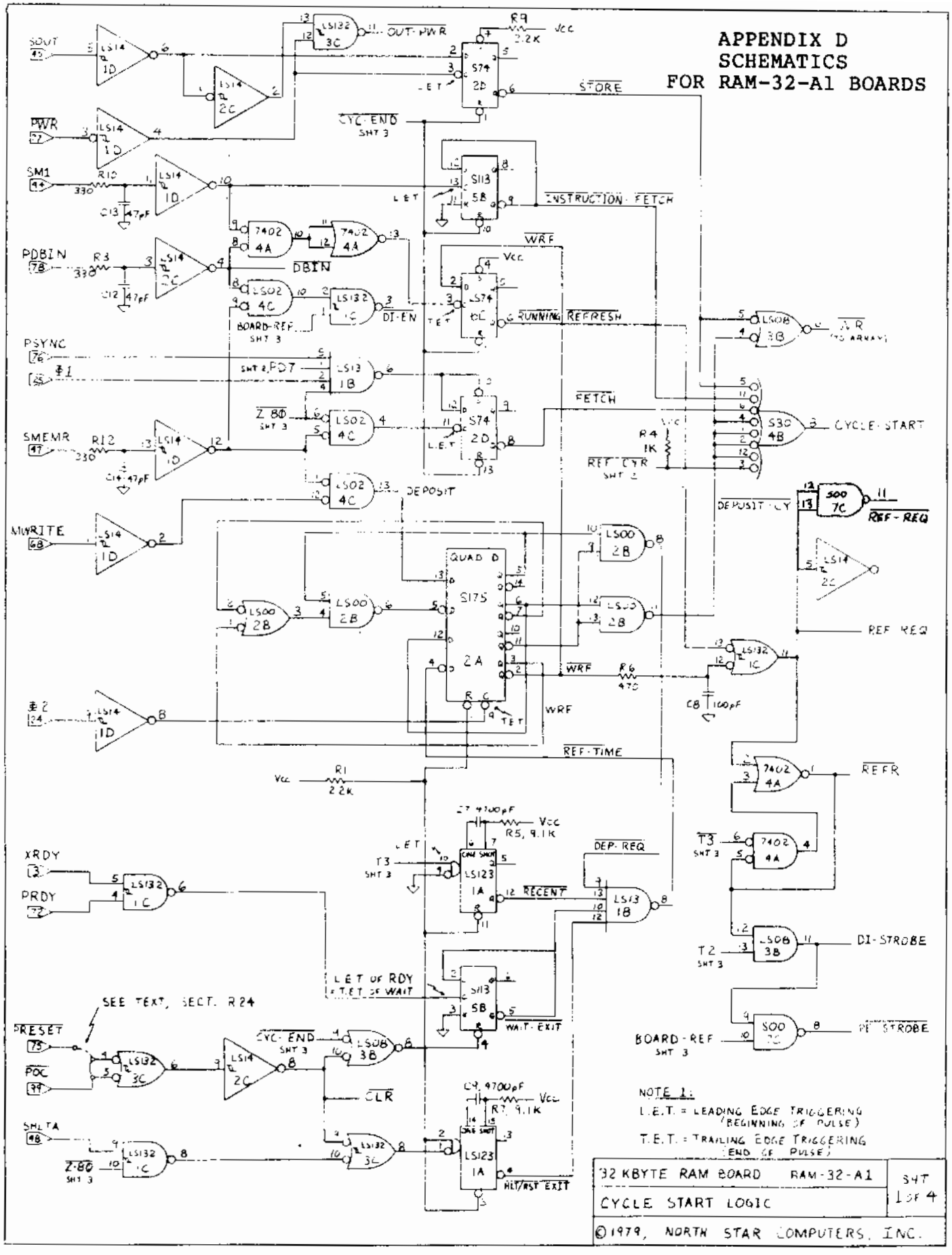
The column 13A-13D contains bit 1 (the 02 hex bit).

The column 14A-14D contains bit 0 (the 01 hex bit).

The column 15A-15D contains bit 2 (the 04 hex bit).

The column 16A-16D contains bit 3 (the 08 hex bit).

The column 17A-17D contains bit 7 (the 80 hex bit).


APPENDIX D
SCHEMATICS
FOR RAM-32-A1 BOARDS
SOUT
PWR
SM1
PDBIN
PSYNC
SMEMR
MWRITE
XRDY
PRDY
SRESET
POC
SMITA
OUT-PWR
STORE
CYC-END
INSTRUCTION-FETCH
DBIN
BOARD-REF
DI-EN
RUNNING
REFRESH
FETCH
CYCLE-START
DEPOSIT
DEPOSIT-CY
REF-REQ
REF REQ
WRF
REF-TIME
REFR
DEP-REQ
RECENT
DI-STROBE
PE-STROBE
WAIT-EXIT
HLT/RST EXIT
CLR
SEE TEXT, SECT. R24
NOTE 1:
L.E.T. = LEADING EDGE TRIGGERING (BEGINNING OF PULSE)
T.E.T. = TRAILING EDGE TRIGGERING (END OF PULSE)
32 KBYTE RAM BOARD RAM-32-A1
CYCLE START LOGIC
SHT 1 OF 4
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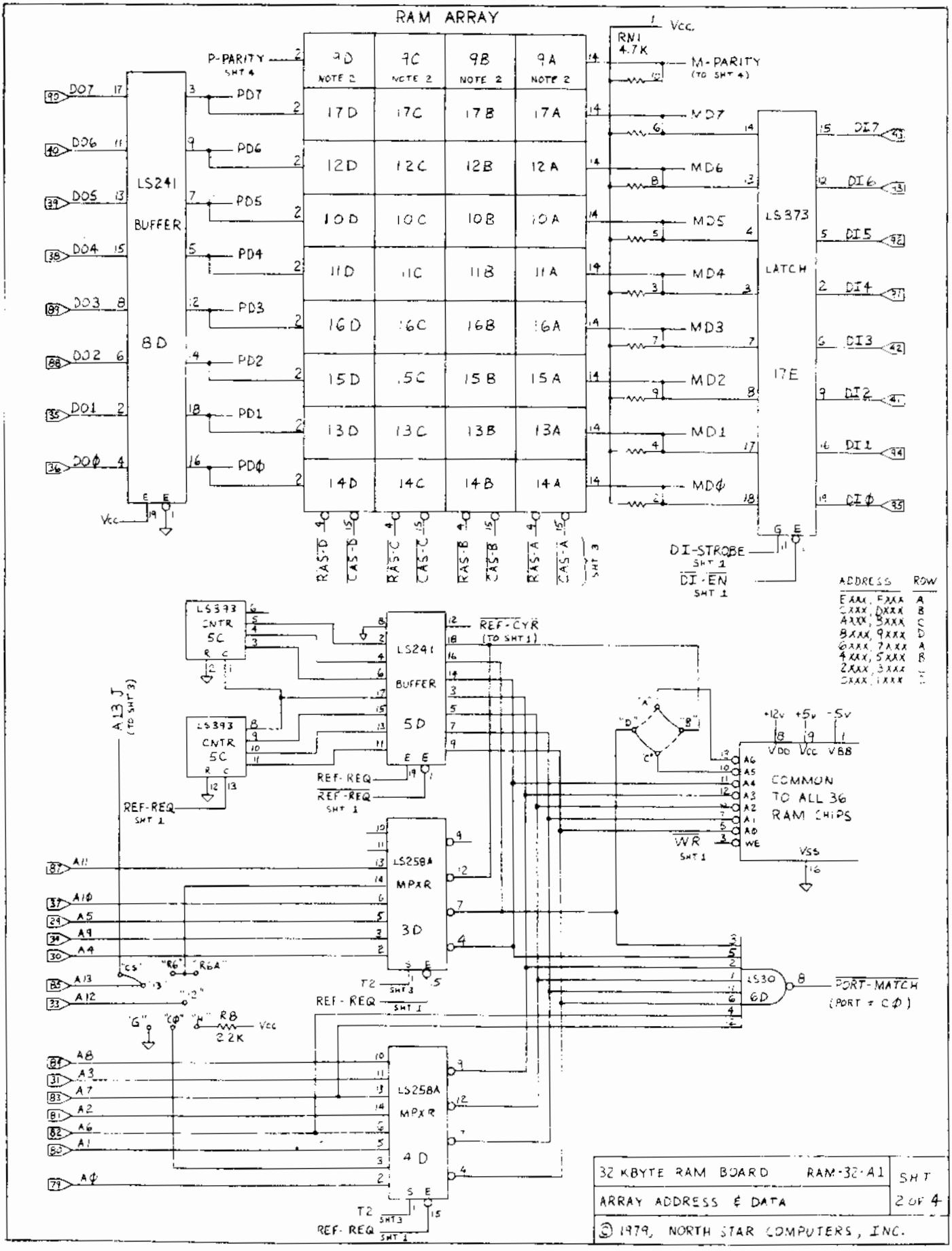
RAM ARRAY
P-PARITY
SHT 4
9D NOTE 2
9C NOTE 2
9B NOTE 2
9A NOTE 2
17D
17C
17B
17A
12D
12C
12B
12A
10D
10C
10B
10A
11D
11C
11B
11A
16D
16C
16B
16A
15D
15C
15B
15A
13D
13C
13B
13A
14D
14C
14B
14A
Vcc
RN1
4.7K
M-PARITY
(TO SHT 4)
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MDØ
LS373
LATCH
17E
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DIØ
DI-STROBE
SHT 1
DI-EN
SHT 1
LS241
BUFFER
8D
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DOØ
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PDØ
RAS-D
CAS-D
RAS-C
CAS-C
RAS-B
CAS-B
RAS-A
CAS-A
SHT 3
ADDRESS
ROW
EXXX, FXXX A
CXXX, DXXX B
AXXX, BXXX C
8XXX, 9XXX D
6XXX, 7XXX A
4XXX, 5XXX B
2XXX, 3XXX C
0XXX, 1XXX D
LS393
CNTR
5C
LS241
BUFFER
5D
REF-CYR
(TO SHT 1)
REF-REQ
REF-REQ
SHT 1
A13 J
(TO SHT 3)
LS258A
MPXR
3D
A11
AIØ
A5
A9
A4
A13
A12
"CS"
"R6"
"R6A"
T2
SHT 3
REF-REQ
SHT 1
"A"
"B"
"C"
"D"
+12v
+5v
-5v
VDD
Vcc
VBB
COMMON
TO ALL 36
RAM CHIPS
WR
SHT 1
VSS
LS30
6D
PORT-MATCH
(PORT = CØ)
"G"
"CØ"
"H"
R8
22K
Vcc
A8
A3
A7
A2
A6
A1
AØ
LS258A
MPXR
4D
T2
SHT 3
REF-REQ
SHT 1
32 KBYTE RAM BOARD RAM-32-A1
ARRAY ADDRESS & DATA
SHT 2 OF 4
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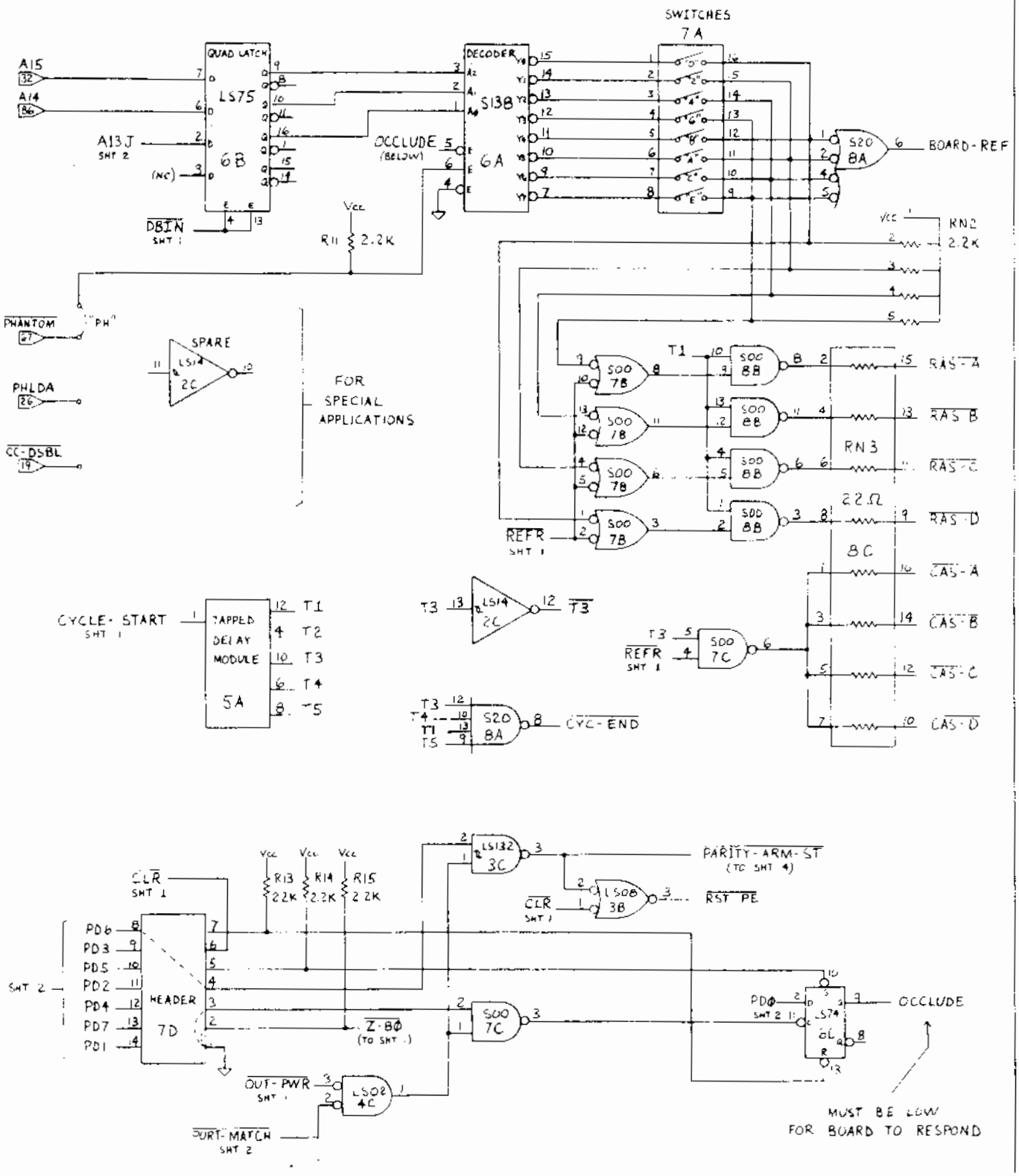
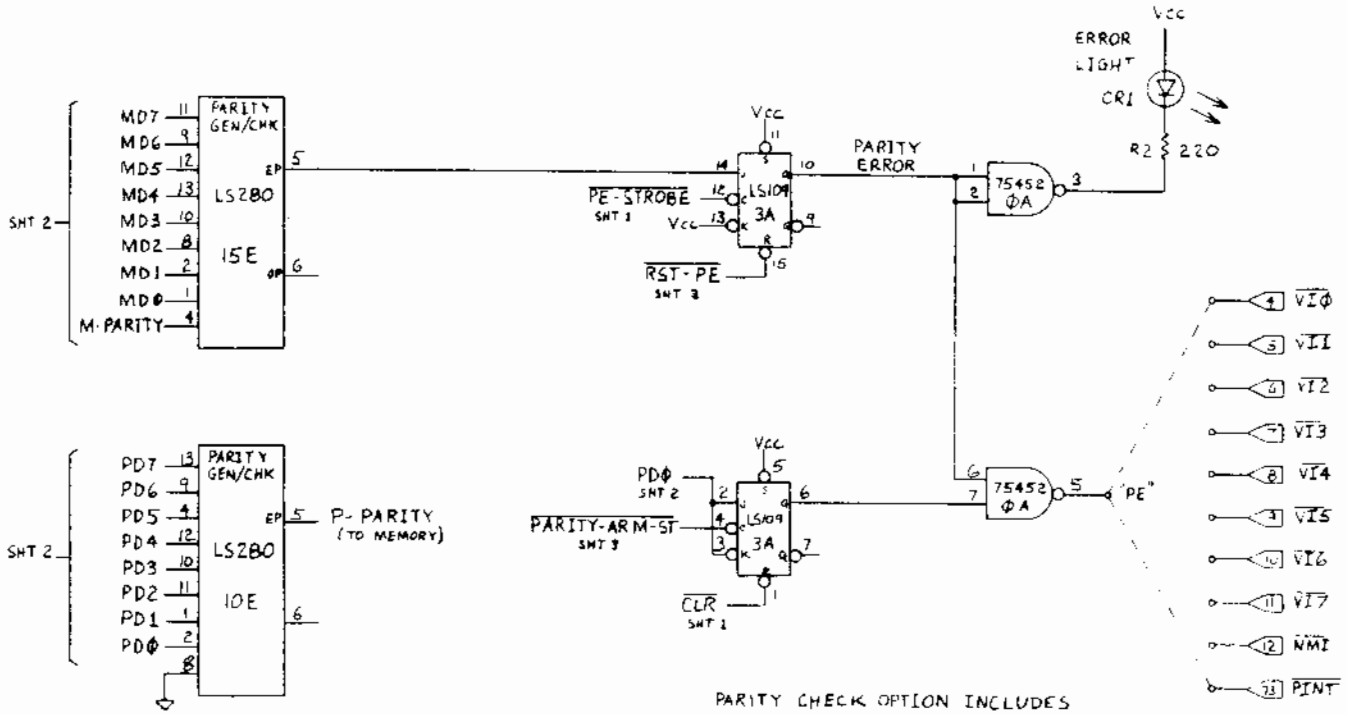
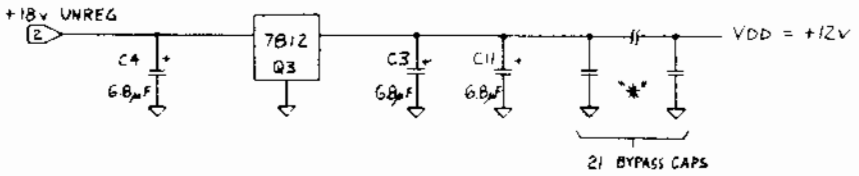
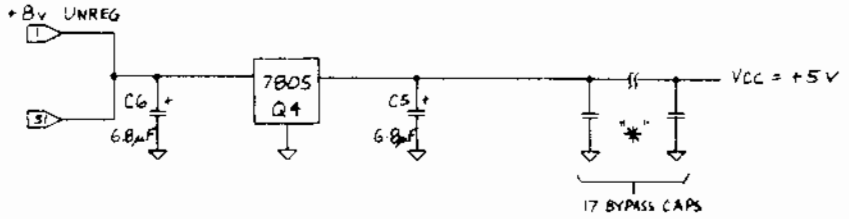


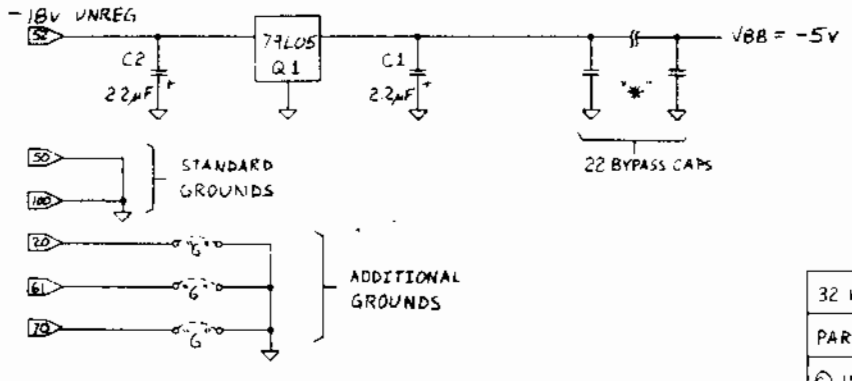
32 kBYTE RAM BOARD	RAM-32-A1	SHT
BOARD SELECT		3 OF 4



PARITY CHECK OPTION INCLUDES
ABOVE LOGIC PLUS
RAM CHIPS IN 9A, 9B, 9C, 9D

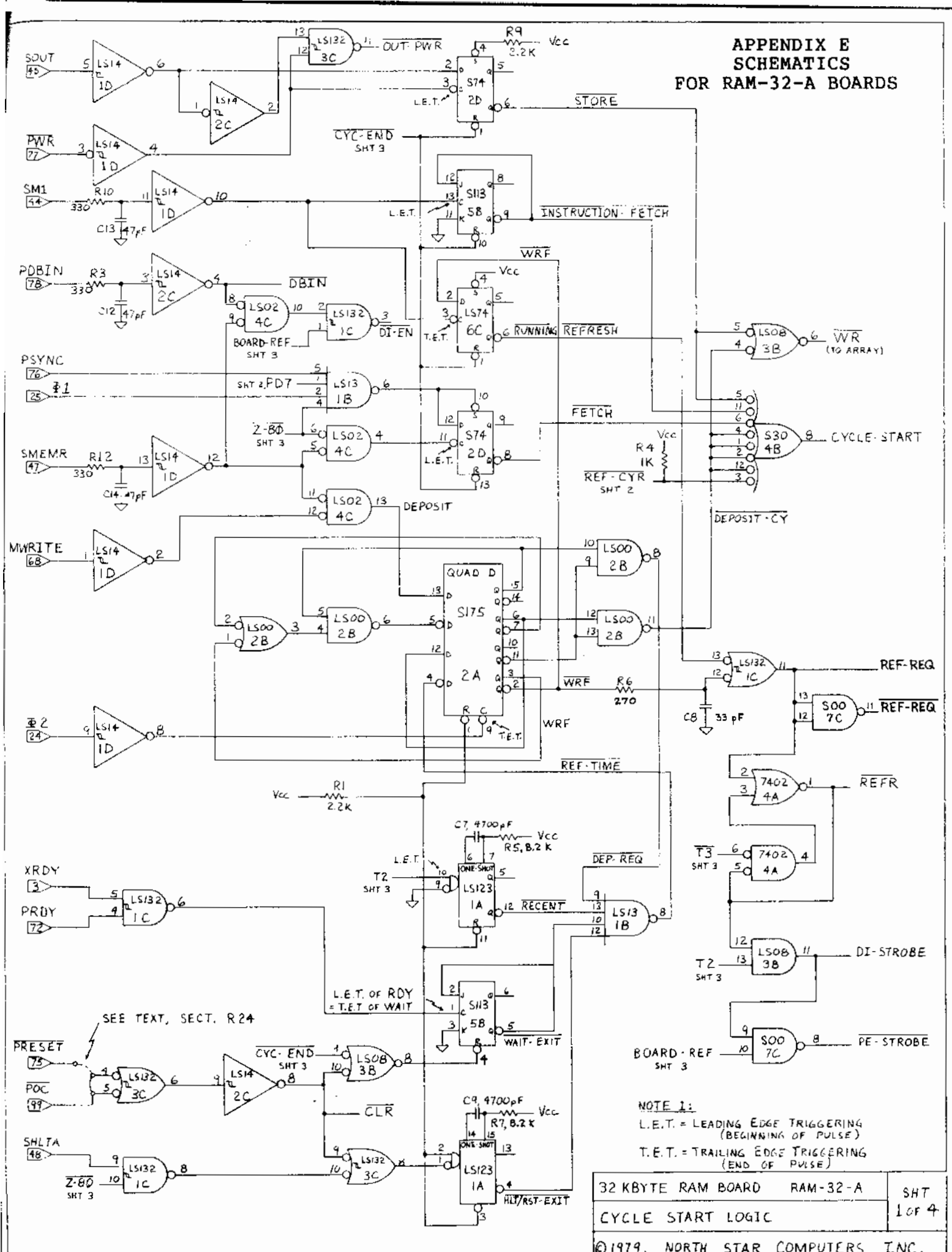






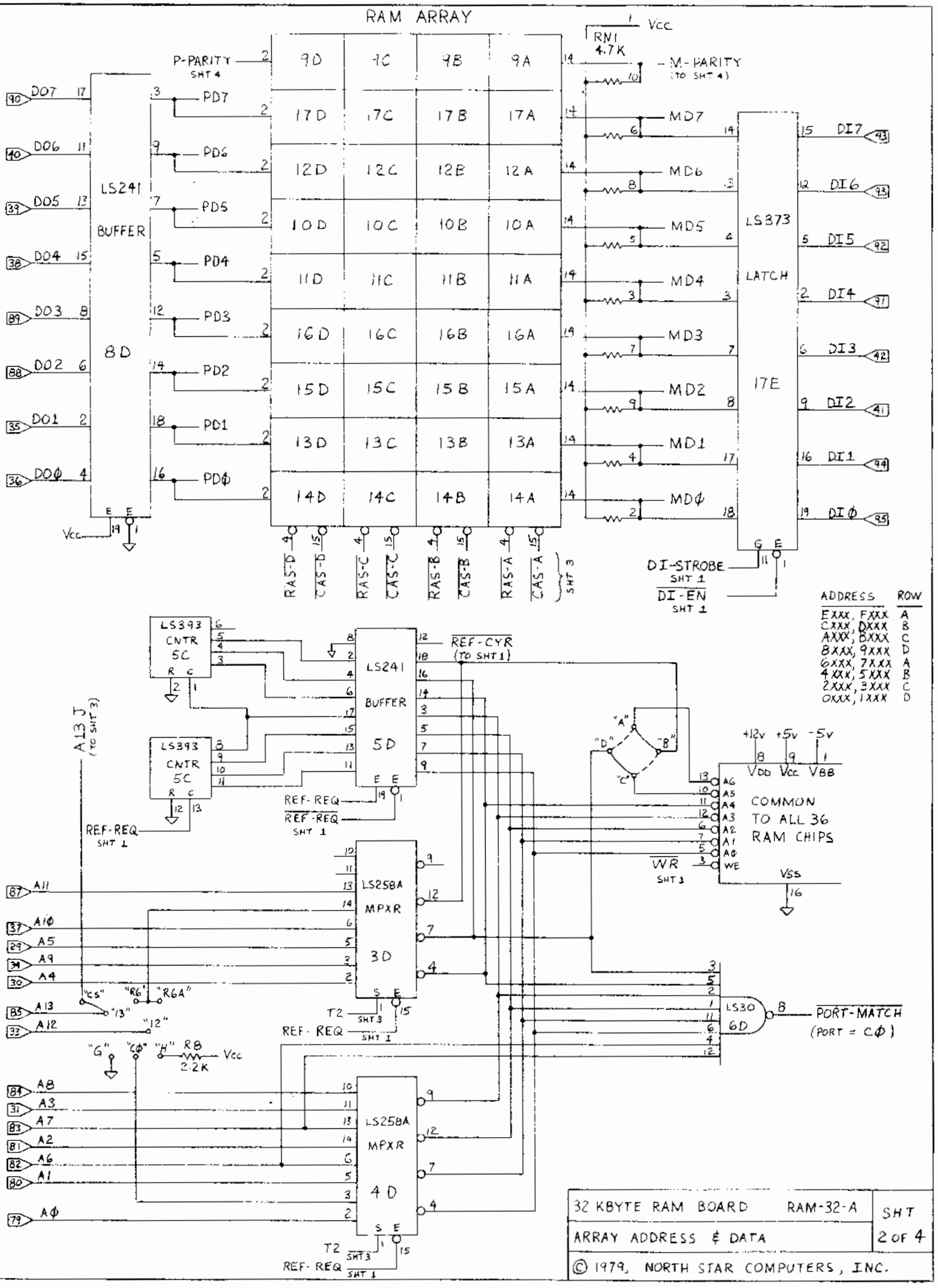
32 KBYTE RAM BOARD RAM-32-A1	SHT 4 of 4
PARITY CHECK OPTION, POWER	

APPENDIX E
SCHEMATICS
FOR RAM-32-A BOARDS



NOTE 1:
L.E.T. = LEADING EDGE TRIGGERING (BEGINNING OF PULSE)
T.E.T. = TRAILING EDGE TRIGGERING (END OF PULSE)

32 KBYTE RAM BOARD RAM-32-A	SHT 1 of 4
CYCLE START LOGIC	


RAM ARRAY
9D
9C
9B
9A
17D
17C
17B
17A
12D
12C
12B
12A
10D
10C
10B
10A
11D
11C
11B
11A
16D
16C
16B
16A
15D
15C
15B
15A
13D
13C
13B
13A
14D
14C
14B
14A
P-PARITY
SHT 4
PD7
PD6
PD5
PD4
PD3
PD2
PD1
PDØ
LS241
BUFFER
8D
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DOØ
Vcc
RAS-D
CAS-D
RAS-C
CAS-C
RAS-B
CAS-B
RAS-A
CAS-A
SHT 3
RN1
4.7K
M-PARITY
(TO SHT 4)
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MDØ
LS373
LATCH
17E
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DIØ
DI-STROBE
SHT 1
DI-EN
SHT 1
ADDRESS
ROW
EXXX, FXXX A
CXXX, DXXX B
AXXX, BXXX C
8XXX, 9XXX D
6XXX, 7XXX A
4XXX, 5XXX B
2XXX, 3XXX C
ØXXX, 1XXX D
LS393
CNTR
5C
LS241
BUFFER
5D
REF-CYR
(TO SHT 1)
REF-REQ
REF-REQ
SHT 1
A13 J
(TO SHT 3)
"A"
"B"
"C"
"D"
+12v
+5v
-5v
VDD
Vcc
VBB
COMMON
TO ALL 36
RAM CHIPS
WR
SHT 1
Vss
LS258A
MPXR
3D
4D
A11
A10
A5
A9
A4
A13
A12
A8
A3
A7
A2
A6
A1
AØ
"CS"
"R6"
"R6A"
"13"
"12"
"G"
"CØ"
"H"
R8
2.2K
T2
SHT 3
LS30
6D
PORT-MATCH
(PORT = CØ)
32 KBYTE RAM BOARD
RAM-32-A
SHT
2 OF 4
ARRAY ADDRESS & DATA
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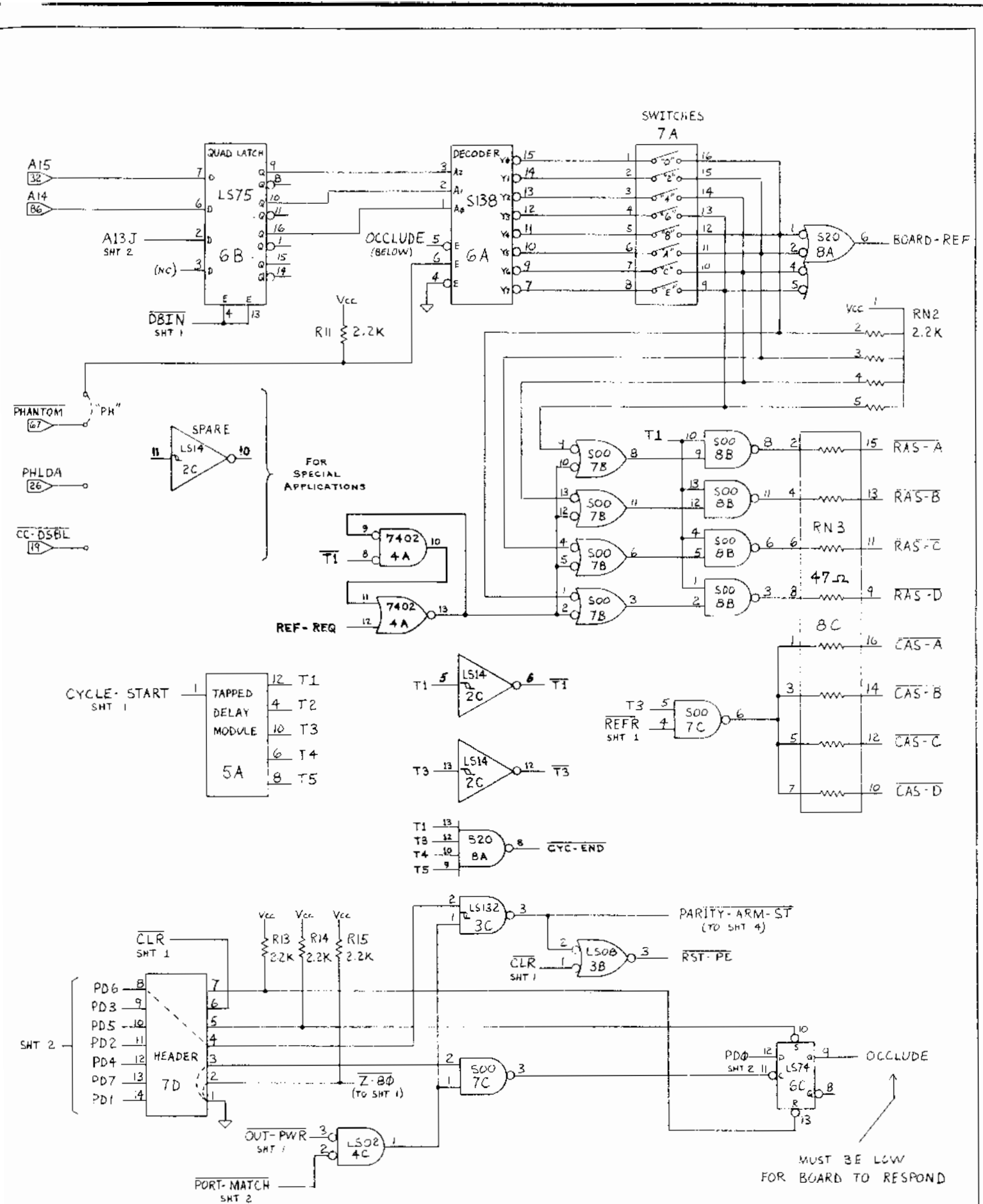
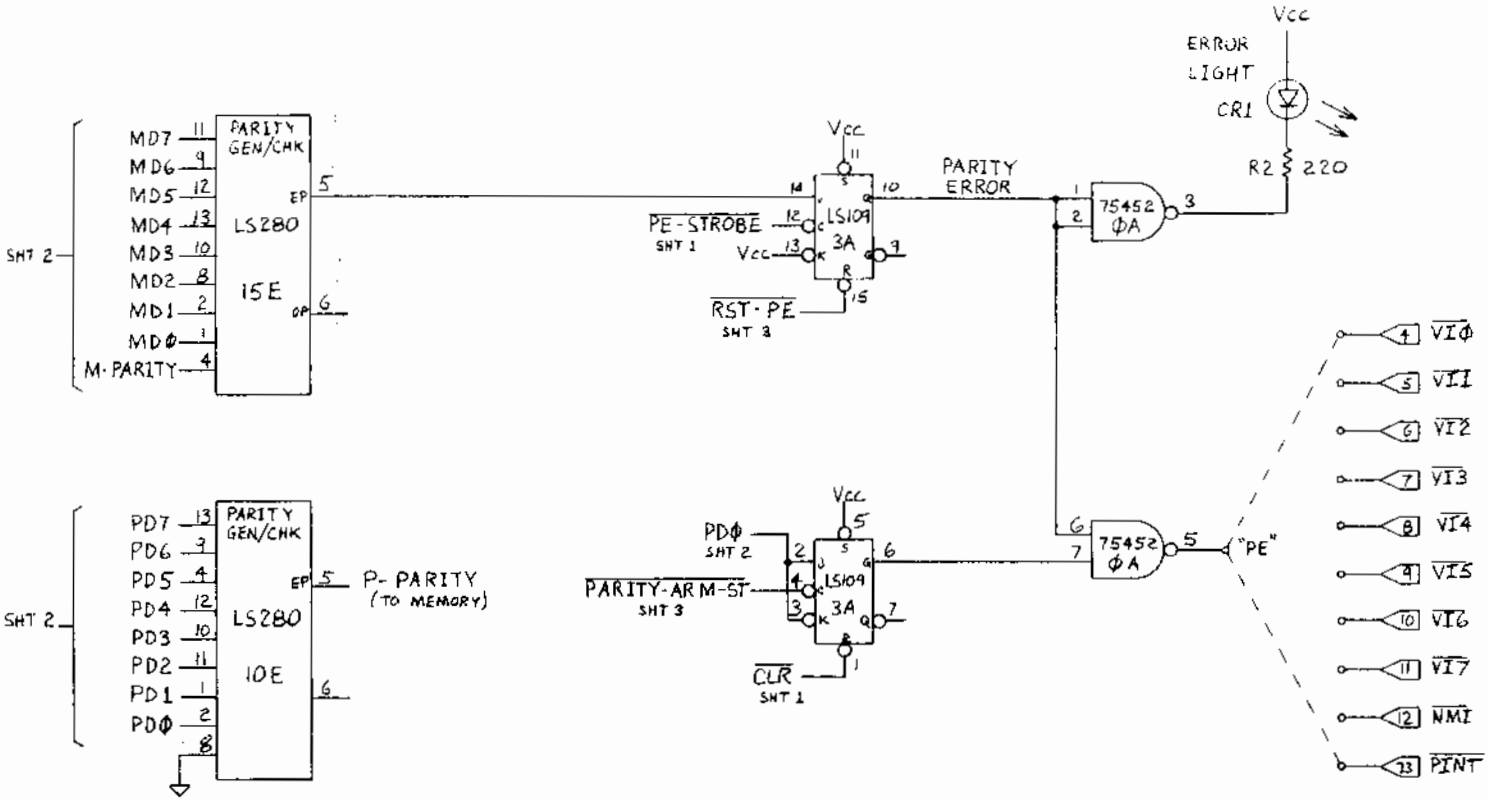
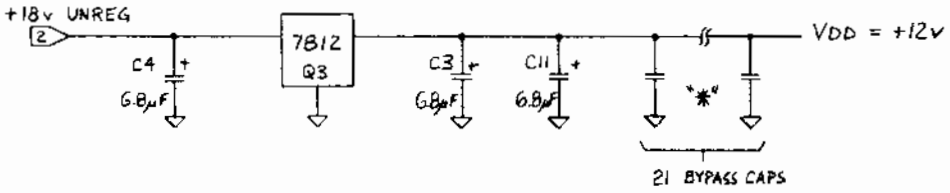
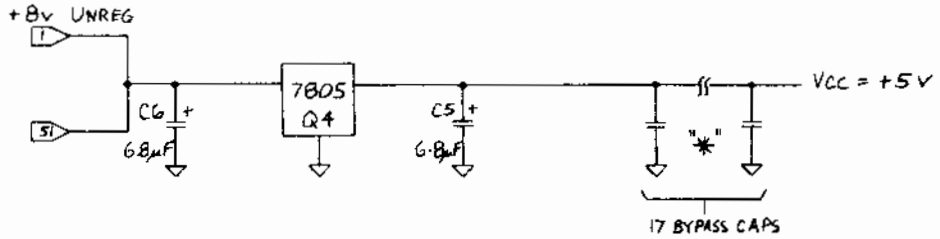


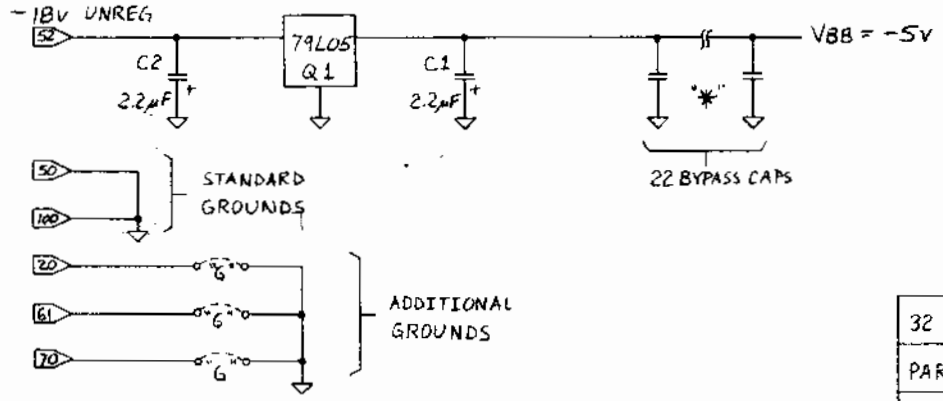
32 KBYTE RAM BOARD	RAM-32-A	SHT
BOARD SELECT		3 OF 4

SC 08006 D









32 KBYTE RAM BOARD	RAM-32-A	SHT 4 of 4
PARITY CHECK AND POWER		

SC 08006-D