Disk Controller PROMs

By Joe Maguire

Of the three PROM chips on the North Star double density disk controller board, two remain a mystery.

The bootstrap program PROM (DPGM) can be read by examining the memory area from E800 to E8FF (standard version) with the Monitor program. A disassembly of this PROM was given in Compass, Vol. 2, No. 1.

The remaining two, DSEL and DWE, do not have their outputs tied to the data bus and cannot be read with the Monitor. They are programmed, however, and do have a purpose. Their contents, and function, will be the subject of this article.

What's a PROM?

PROM stands for Programmable Read Only Memory. The ones used on the controller board are of the TTL variety sometimes referred to as "bipolar." These differ from the NMOS type, such as the 2708 and 2716, by internal construction.

North Star uses two types on the board. The DPGM PROM is a 256x8 or 2048 bit type 74S471. This means that its internal arrangement consists of 256 eight bit bytes. That's easy to see when you dump it. It looks just like any other memory dump.

The DSEL and DWE PROMS are 256x4 or 1024 bit type 74S287. (North Star lists these as 82S129s but that is a Signetics house number.) The internal arrangement is 256 four bit nibbles. Think of a nibble as half a byte. (Honest!)

The true addresses of all these PROMs start at zero and go to FF hex. The circuitry on the controller board shifts them to apparent other addresses.

A PROM is really a do-it-yourself logic block. Some standard TTL ICs, such as the address decoder type 74LS138, are really PROMs in disguise. The 74LS138 has three input lines and eight output lines. Three to eight works nicely when you want to convert binary to decimal. But what type do you select when you have eight input lines and want four outputs? No standard type will give you that. There are just too many possible combinations for an IC manufacturer to attempt to decide what should be "standard." Instead, they offer you a blank IC and tell you to program it yourself.

A blank PROM is filled with all zeros. The user programs the zeros to ones, on a selected basis, to get the functions he wants. The programming is done by special devices which can control the currents (up to half an amp) and voltages (up to 30V) required.

The DSEL PROM

DSEL stands for "disk select." It is really the PROM which determines the memory address at which the controller board will respond. It decodes four addresses out of the possible 256 and, based on the address byte, directs the controller to take various actions.

One way of looking at the required list of actions is by means of a "truth table." When an item in the table comes up true, then some action should be taken. If the item is not true, don't do anything. True can be defined as either a logic high or low. For our table we are going to define true as low or a zero.

Table 1. is the truth table for DSEL. Some explanation of terms is in order:

PROM Select - When this is true, the bootstrap PROM output is enabled. The CPU reads the PROM on startup. After that it is not used.

MUX Enable - MUX stands for multiplex. The multiplexers are used to put the status byte and read data on the data bus.

Orders - Various circuits within the controller must be given instructions from time to time (read, write, step, etc.) When this goes true, the controller knows a command is coming up.

Stall - The disk is a much slower device than the CPU. From time to time the CPU must be held in a wait state until the disk

completes an operation. True on this line makes the CPU wait.

The DWE PROM

DWE stands for "disk write enable." The DWE PROM controls the various functions required for proper writing to the disk. Writing is the most critical of disk operations. Various parameters must be carefully controlled if data integrity is to be maintained. For example, when writing on the innermost tracks, write precompensation must be used because of the slower linear velocity of the disk. DWE takes care of this.

The DWE PROM is not affected by locating the controller board at a different RAM address. Therefore, if a special PROM set is ordered to relocate the disk, DWE need not be changed.

The inputs to DWE are a combination of signals from onboard the controller and not an address as in the case of DSEL. However, the PROM responds as if it were an address and selects the various functions accordingly. The input signals are not as meaningful to the user as those of DSEL and will not be elaborated upon here. Refer to the disk controller schematic for more information.

Table 2. is a dump of the DWE PROM. An input example is given to show what effect it has on the output. Again, refer to the schematic for information about the various output lines.

# # #

	Stall (CPU wait state)	Controller Orders	MUX enable	PROM select	Hex value
RAM address high byte	E8	0	1	1	1	7
" "	E9	1	1	1	0	E
" "	EA	1	1	0	1	D
" "	EB	1	0	1	0	A

Table 1.

PROM "DSEL" truth table. (standard address) 0 = True. All nibbles at addresses other than those shown above contain value F hex.

From the table it can be seen that when the CPU is addressing the E8 block, only the PROM is enabled. When the EA block is addressed, only the orders register is enabled etc.

00	7	1	7	F	7	1	7	F	7	1	7	9	7	1	7	9
10	7	1	7	F	7	1	7	F	7	1	7	9	7	1	7	9
20	7	1	7	F	7	1	7	F	7	1	7	9	7	1	7	9
30	7	1	7	F	7	1	7	F	7	1	7	9	7	1	7	9
40	7	1	7	F	7	1	7	F	7	0	7	9	7	0	7	9
50	7	3	7	F	7	3	7	F	7	1	7	9	7	1	7	9
60	7	1	7	F	7	1	7	F	7	0	7	9	7	0	7	9
70	7	3	7	F	7	3	7	F	7	1	7	9	7	1	7	9
80	1	F	1	F	1	F	1	F	7	9	7	9	7	9	7	9
90	7	F	7	F	7	F	7	F	7	9	7	9	7	9	7	9
A0	1	F	1	F	1	F	1	F	7	9	7	9	7	9	7	9
B0	7	F	7	F	7	F	7	F	7	9	7	9	7	9	7	9
C0	1	F	1	F	3	F	3	F	7	9	7	9	7	8	7	8
D0	7	F	7	F	7	F	7	F	7	B	7	B	7	9	7	9
E0	0	F	0	F	1	F	1	F	7	9	7	9	7	8	7	8
F0	7	F	7	F	7	F	7	F	7	B	7	B	7	9	7	9

Table 2.

PROM "DWE" dump. Left column is address. Display is sixteen nibbles per line in hex.

"Address" is composed of the following:

	1	1	1	0	0	0	1	0
Dbl Dens								
Dirctn/PreComp								
Write Shift 10								
Write Shift 9								
Write Shift 8								
Write Shift 7								
Clock counter 3								
Clock counter 2								

The example shows "address" E2. From table 2., the output is 0, all outputs enabled.