MOSTEK®

MICROCOMPUTER SYSTEMS

Operations Manual

VIDEO DISPLAY INTERFACE

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OPERATIONS MANUAL

(MK78035 and MK78033)

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1.0 General

This double Eurocard CRT interface allows easy interfacing of a user's monitor and keyboard to a microcomputer system using a general purpose serial current loop or RS 232/V24 interface, or using a Z80 PIO (MK3881) for interfacing at high speed to a Z80 CPU.

The display format is 80 characters per line with 24 lines. These 1920 characters are stored in a RAM memory connected to an F8 microprocessor on the card.

This 3 chip F8 Microcomputer receives ASCII commands from the system computer, decodes them, and performs the requested function. Because some commands require several milliseconds to execute (although most are completed in a few hundred microseconds), a 48 character FIFO is implemented with the F8. This allows continuous data rates to 19.200 baud with a typical mix of commands.

The F8 also permits incorporation of extra features such as cursor addressing, cursor address readback, free programmable TAB's, block mode operation and automatic 15Hz repeat of keyboard keys depressed more than .7 seconds. Other features of the card include:

- Upper/Lower Case
- Bell Tone output for a smaller speaker
- Inverse video
- 1 V P-P 75 Ohm video output
- Programmable font
- Programmable functions

1.1 Operation

A bank of 16 MK4102 static RAM's are constantly being read and displayed on the video monitor. This process is largely independent of the F8. The F8's function is to receive data (from the UART or PIO) on a CPU port in response to an interrupt and process this data. In addition, it must respond to a keyboard interrupt and control the passing of the keyboard data to the UART or PIO on the remaining CPU port.

The majority of the commands received by the F8 are characters to be written onto the screen. The character write operation is accomplished by placing data for the RAM's on an I/O port and strobing a port bit. The next RAM read cycle at the horizontal address which matches the current horizontal cursor address results in a multiplexing of vertical addressing and a write cycle into the cursor location. This requires 64 microseconds worst case. The remainder of the commands received are control codes and cause the F8 ports to be modified to perform the required function.

Because a 80 x 24 display counter generates 14 bits of addressing which must be compacted to 13 bits for addressing a 2K byte RAM array, an algorithm is used which is basically 80 x V + H where V is the vertical address and H is the horizontal. This requires one adder.

The scroll operation is performed using a modulo-24 adder (1-4 bit adder plus a PROM) with the displacement provided by the F8. Scroll is the mode of operation where the screen contents move up/down one line after a line feed/up cursor command at the bottom/top of the screen.

A single 11.0592MHz crystal provides timing for the entire card including CPU, baud rate generator and video. The video output which is strap programmable for 525/60Hz or 625 Line/50Hz provides actual vertical output frequencies of 60.95Hz

SCROLL OPERATION

Figure 1

Scroll Address	Cursor Address	4 Bit Adder Carry Out	Output
00	00	0	00
00	00	1	01
00	01	0	01
00	01	1	10
00	10	0	10
00	10	1	00
00	11	0	11*
00	11	1	11*
01	00	0	01
01	00	1	10
01	01	0	10
01	01	1	00
01	10	0	00
01	10	1	01
01	11	0	11*
01	11	1	11*
10	00	0	10
10	00	1	00
10	01	0	00
10	01	1	01
10	10	0	01
10	10	1	10
10	11	0	11*
10	11	1	11*

* = not valid input combination for modulo-24, only used by TAB logic

and 49.87Hz. Baud rate frequencies are accurate to crystal tolerances except 110 which is actually 109.1 baud.

To allow rapid line clearing, a port pin allows writing into all memory locations on a given line, also requiring 64 microseconds worst case.

The TAB locations (horizontal addresses where TAB's are set) are stored in the unused locations in the display ROM.
2048 bytes - 80 x 24 =1920 display locations = 128 extra bytes. 16 of these bytes are used to store a bit map corresponding to horizontal locations.

1.2 CRT Functions

CONTROL-G	(07H)	initiates a 300ms ±5%, burst of 500Hz on pin SK2A28. This pin is normally high. The duty cycle of the 500Hz pulse averages 45% one level, 55% zero. An amplified signal capable of driving a 50 Ohm speaker direct is available on pin SK2C27.
CONTROL-H	(08H)	backspace, after column 0, then NOP
CONTROL-I	(09H)	TAB, cursor skips to the next Tab location. TAB locations are set by the set TAB and reset TAB commands. If no TAB's exist between the cursor and the rest of the line, then the cursor will move down 1 line and be set to the next TAB. If no TAB's are set anywhere, then perform CONTROL-L.
CONTROL-J	(0AH)	line feed, move cursor down 1 line. If at bottom then scroll the display up one line.
CONTROL-K	(0BH)	vertical backspace, the cursor moves up 1 line, after the top of the display the display scrolls down 1 line.
CONTROL-L	(0CH)	advance cursor horizontally 1 character right, after column 79, NOP.
CONTROL-M	(0DH)	return, set cursor to column 0
CONTROL-N	(0EH)	reset TAB at the current cursor position.
CONTROL-0	(OFH)	set TAB at the current cursor position.
CONTROL-P	(1OH)	downshift,following character in the range of ASCII 40-5FH will be displayed as one of the special non-ASCII characters stored in the ROM at addresses 0-1FH.
ESCAPE	(1BH)	enables escape sequence: following character determines exact function.
=		set cursor address, the next 2 received characters will determine the new cursor Y (vertical) and X (horizontal) addresses.
+		set cursor relative, the next 2 received characters will move the cursor to Y+ (first char.) and X+ (second char.) The 2 characters are 2's complement, 6 bit numbers.
?		cursor position readback, the VDI-S will send a STX (02H) then the Y and X address of the current cursor position. A bias of 30H will be added to each address byte to avoid conflict with control characters.
]	(7DH)	local command, set VDI-S to local mode, all further keyboard inputs will affect the display directly without transmission to the I/O Channel.
)		read one character, transmits the contents of the current cursor position to the I/O channel. CONTROL-L command is then done.

<		read line, first a STX (02H) is sent, , then the current cursor position up to and including the last non blank character on line is sent, then the cursor is reset to the original position and a return (ODH), ETX (O3H) is sent.
>		read page, first a STX (O2H) is sent, then the rest of the current line up to and including the last non blank character is sent, then a return/line feed is done and the process continues until the last non blank character on the last line is sent. Then a ETX (O3H) is sent. The cursor is returned to the original position. The intermediate returns are sent. Empty lines will cause only a return to be sent.
CONTROL-W	(17H)	Enable inverse video. All subsequent characters or line clears will cause a white background to be written.
CONTROL-Y	(19H)	Disable inverse video.
CONTROL-\	(1CH)	set line mode, resets terminal to remote mode. Terminal acknowledges with a CONTROL-F(06H) to indicate that remote mode has been set.
CONTROL-]	(1DH)	clear display, rest of display from the current cursor position is cleared.
CONTROL-Λ	(IEH)	home. Cursor is moved to the home position, Y=23, X=0.
CONTROL-_	(1FH)	clear line. Rest of line from current cursor position is cleared.
Characters 20H-7EH		ASCII characters, these will be displayed on the screen at the current cursor address. After column 79 is reached the cursor remains at column 79, if additional characters are outputted without moving the cursor (line overflow) then the bell function will be activated for each character outputted. The extra characters outputted will be written into column 79.
DEL	(7FH)	Delete, this is a NOP to the display controller.

2.0 The F8 Microprocessor

The three chip F8 microprocessor with expansion capabilities is provided on the card. The production card contains 1-3850 CPU, 1-3871 PIO and 1-3851 PSU. The operating program will fit into the 3851 PSU. If a custom function is required (or during prototyping) a 3853 SMI and a MK2708 1K Byte PROM may be inserted to hold the operating program. All bits of the 6 ports and both interrupts are used in the basic system. If an SMI is inserted, its interrupt is available.

3.0 Parallel I/O MK78035

A Z80 PIO MK3881 plus buffering and address decoding logic is used for transfer of data between the card and a Z80 CPU. Typically the card will be used with the MOSTEK SDB-80E Single Board Computer. 64 programmable card addresses are provided allowing the user to attach multiple VDI-P boards to a single CPU. The 48 character FIFO can be filled at a 95 μs/character rate, the FIFO is emptied by the VDI-P as it processes the received characters. The transfer of data into the FIFO and from the keyboard is controlled by the ready and strobe handshake lines of the PIO. Once the FIFO is full, the PIO receives no strobe until the FIFO has been emptied by a character. Therefore, after the first 48 characters, the transfer rate is a function of the character stored in the FIFO. See section 6.

When a character from the keyboard is to be transferred to the CPU, a strobe pulse is given to the PIO.

3.1 PIO Programming

A fully buffered PIO is on the VDI-P card. Its addresses are programmable by the 6 port address pins on SK2.
These 6 bits correspond to the most significant 6 bits of an I/O address.
They are 'true' inputs, a one in any bit position corresponds to a one in the PIO address. Internal pullups are provided on the card. The two remaining, non-programmable bits are the bits needed to decode PIO control/data ports and B/A port select. The 4 fixed addresses are as follows:

7							0	
X	X	X	X	X	X	0	0	KB CONTROL
						0	1	KB DATA
						1	0	DISPLAY CONTROL
						1	1	DISPLAY DATA

The following control sequence will correctly program the PIO.

```
: to port X X X X X X 0 0 ; 4FH, vector, 83H
: to port X X X X X X 1 0 ; 0FH, vector, 83H
```

After programming the KB port, an input should be executed from the KB data port to initialize the PIO. The data from this input should be ignored. Once the PIO has been initialized, every input or output will automatically handshake between the Z80 and F8. When the F8 has a character from the KB, an interrupt will occur at the input vector. When the F8 has finished processing a character or command, an interrupt will be caused at the output vector. For proper interrupt operation the Z80 must be operating in interrupt mode 2. Important, no reset is provided on the card for the PIO. M1 must be 'OR'ed with reset externally in some systems.

3.2 Serial I/O MK78033

Industry standard, asynchronous serial I/O using 10 or 11 bits per character is supported by the MK78033. The card can be used either with current loop (20mA) or RS232/V24 (note that -5V is required for RS232/V24 operation). An on-board baud rate generator can be used at any of the following baud rates:

9.600 4.800 2.400 1.200 600 300 110

An on-board switch can be used to select the speed, or it can be selected externally. If parity, either even or odd, is required, it can be selected by connections to the SK2 connector. The VDI-S does not test received parity, but will transmit parity. The number of stop bits is also programmable. See section 7.0 for pinout.

4.0 Keyboard (KB) Interface

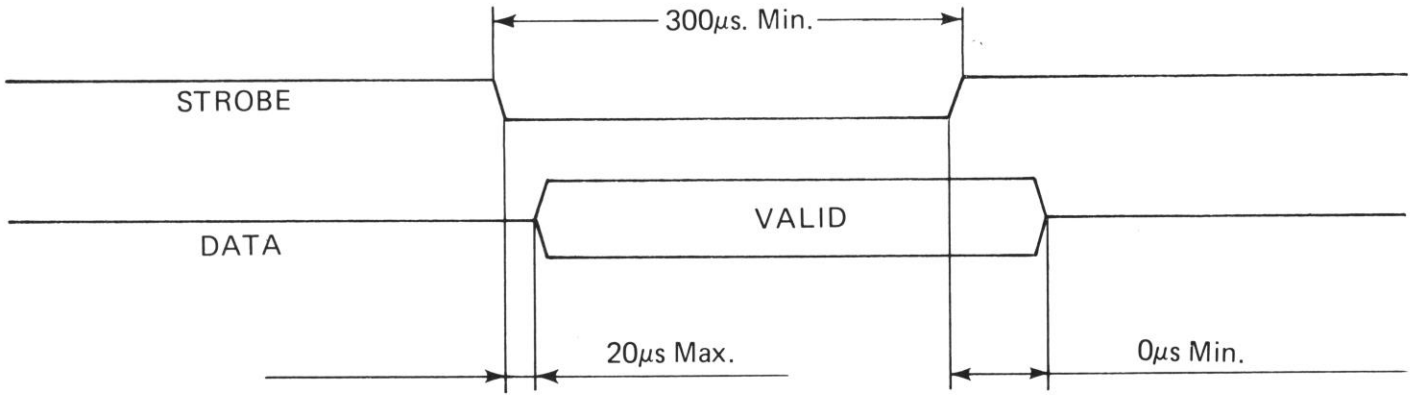
The ASCII keyboard is interfaced to the CRT board over the peripheral connector (SK2 A 17-A 25). The active edge of the strobe can be programmed with pin SK2 C 25 for either positive or negative edge triggering. The keyboard should have a strobe output which remains active whenever a key is depressed and data is valid. Using this type of strobe an autorepeat feature is implemented. Whenever the strobe is active longer than .7 seconds, then the data from the keyboard will be repeated at a 15Hz rate. A feature of the card allows lower case characters to be generated from an upper case only keyboard. Whenever SK2 C22 is allowed to go high (internal pull-up is provided), all upper case characters received from the keyboard will be converted into lower case for transmission.

5.0 Power Supply Requirements

+5 ± 5%	2.5 Amps worst case
+12V ± 5%	.1 Amps worst case

-5V is for PROM or RS232/V24 only. PROM current requirements are not included in the above figures.

KEYBOARD INTERFACE
Figure 2



EDGE = I, IF KEYBOARD SUPPLIES POSITIVE ACTIVE
(SK2 C25) STROBE, THEN PROGRAM EDGE = 0

6.0 Execution Times

The basic execution time for character processing is 320 microseconds. Other commands require different execution times. All times include 95μs for loading the FIFO (μ=micro)

EXECUTION TIMES

Table 1

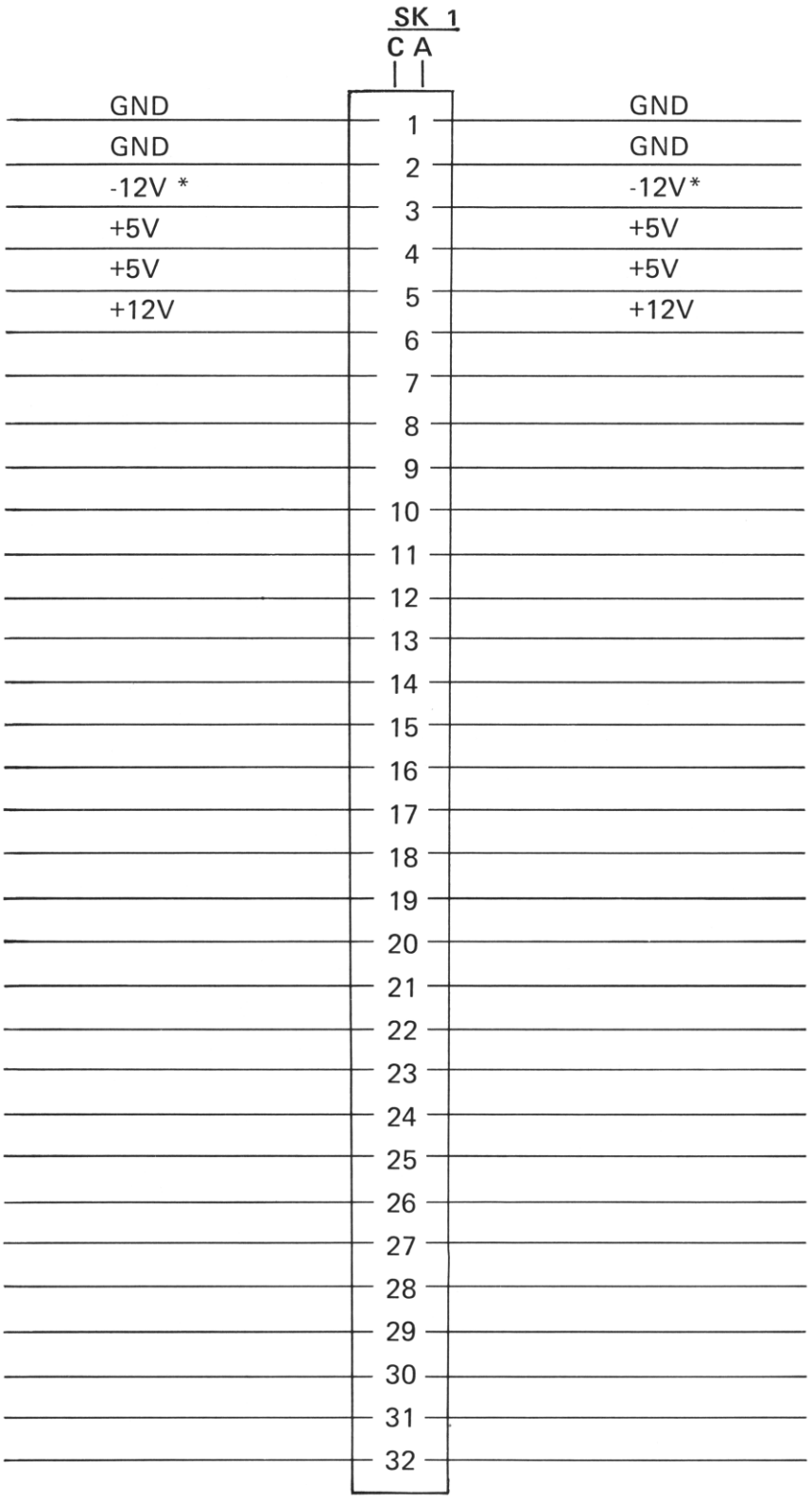
ASCII	FUNCTION	EXECUTION TIME**
00	NOP	265 μs
01	NOP	
02	NOP	
03	NOP	
04	NOP	
05	NOP	
06	NOP	265 μs
07	BELL	320 μs
08	BS	290 μs
09	HT	1.6ms typ, 5.2ms max
OA	LF	290 μs typ, 440 max
OB	UP	290 μs typ, 440 max
OC	RIGHT	290 μs
OD	RETURN	280 μs
OE	CLEAR TAB	980 μs
OF	SET TAB	990 μs
10	DOWNSHIFT	
	(2 Char.)	500 μs
11	NOP	
12	NOP	
13	NOP	
14	NOP	
15	NOP	
16	NOP	
17	INVERSE VIDEO	310 μs
18	NOP	
19	NORMAL VIDEO	310 μs
IA	NOP	
IB	ESC	
	= (4 chars)	920 μs
	+ (4 chars)	1020 μs
	? (2 chars)	760 μs +3 x 10/BAUD *
	} LOCAL (2 Chars)	500 μs
	) READ 1 CHAR (2 Chars)	810 μs
	<READ LINE (2 Chars)	810 μs +83 x 10/BAUD *
	>READ PAGE (2 chars)	810 μs +1992 x 10/BAUD *
IC	LINE	400 μs
ID	CLEAR DISPLAY	9.33ms
IF	HOME	285μs
IF	CLEAR LINE	6.85ms
FF	NOP	225 μs
KEYBOARD SERVICE		310 μs

* In serial mode. In Parallel Mode speed depends on the Z80 CPU.
** Worst Case

7.0 SK2 External Signals MK78033
Table 2

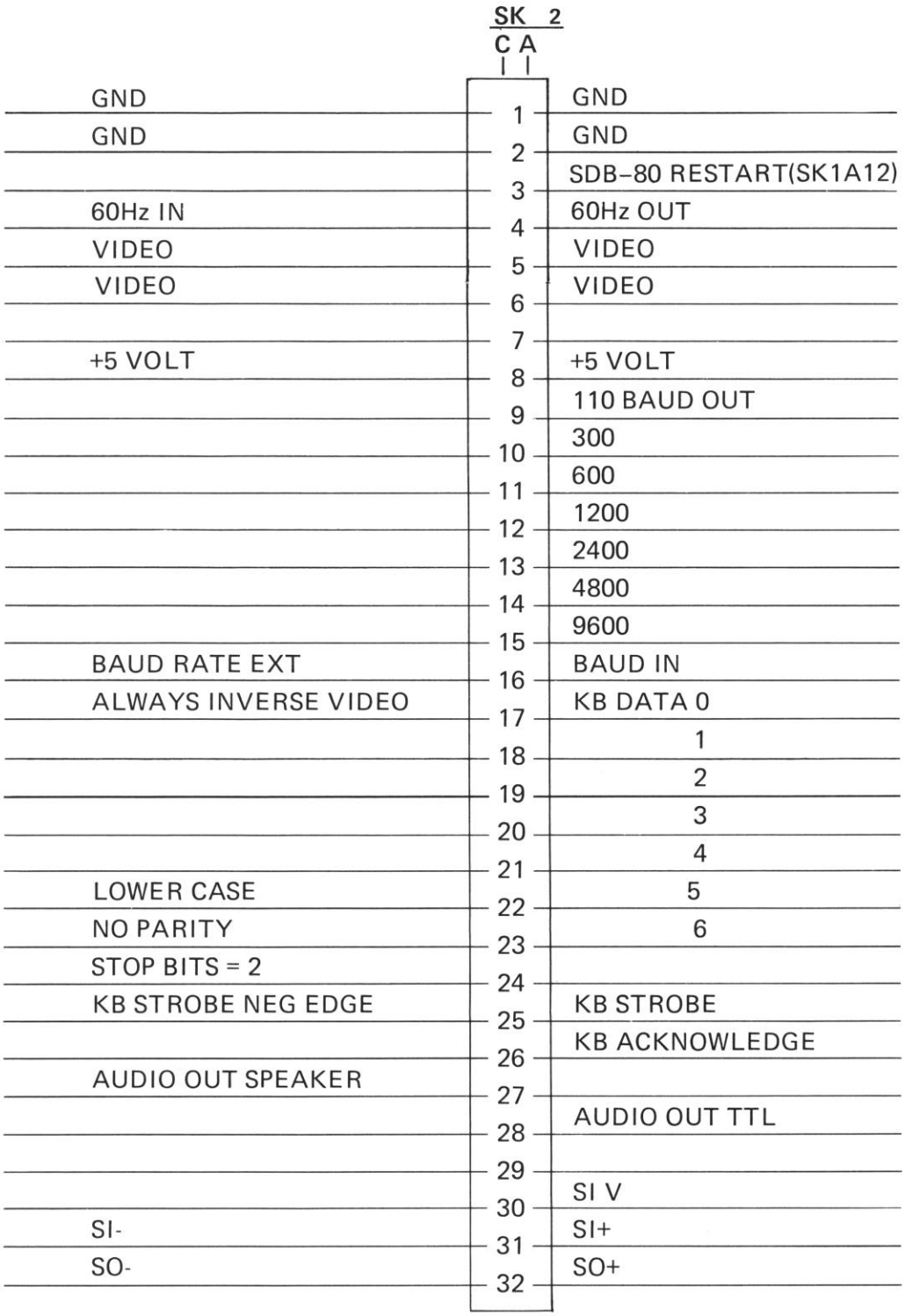
C4, A4	50/60 Hz,	shorting SK2C4 to SK2A4 SELECTS a 50Hz fram rate, open is 60Hz;
C16	Baud rate ext.,	this input would be used to allow baud rates other than those provided on the card. Maximum baud rate depends on the character mix. See section 6;
SK2 A16	Baud in,	if the on-board baud switch is placed in the 'ext' position, then an external baud switch may be connected between the 'baud in' line and the desired baud rate. Note that in this mode the baud rate ext pin is left open;
A17-23	KB data,	true high;
A25	KB strobe,	level indicating valid data. Active together with an after data, response time.
C25	KB strobe edge,	1=data strobed on neg. edge 0=data strobed on pos. edge
C22	Upper and lower case,	1=convert upper case characters to lower 0=keyboard data normal, this signal only affects the keyboard data. Computer data will be displayed as received;
C23	No parity,	1=no parity, 8 data bits 0=even parity, 7 data bits
C24	Stop bits,	1=2 stop bits 0=1 stop bit
A28	Audio Out,	TTL oscillator output
C27	Audio out,	50 Ohm speaker drive
A30	SI V	RS 232 input
A31	SI +	current loop plus input
C31	SI -	current loop minus input
A32	SO +	current loop or RS 232 output
C32	SO -	current loop output
C5, A5 C6, A6	VIDEO	EIA video output (comp sync) 1.0V 75Ω
C17	INVERSE	1=Inverted video 0=Programmable Inverse or Normal Video

7.1a



* only required if MK2708's are used

7.1b


SK 2
C A
GND
GND
60Hz IN
VIDEO
VIDEO
+5 VOLT
BAUD RATE EXT
ALWAYS INVERSE VIDEO
LOWER CASE
NO PARITY
STOP BITS = 2
KB STROBE NEG EDGE
AUDIO OUT SPEAKER
SI-
SO-
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
GND
GND
SDB-80 RESTART(SK1A12)
60Hz OUT
VIDEO
VIDEO
+5 VOLT
110 BAUD OUT
300
600
1200
2400
4800
9600
BAUD IN
KB DATA 0
1
2
3
4
5
6
KB STROBE
KB ACKNOWLEDGE
AUDIO OUT TTL
SI V
SI+
SO+

7.1 External Signals SK2 MK78035

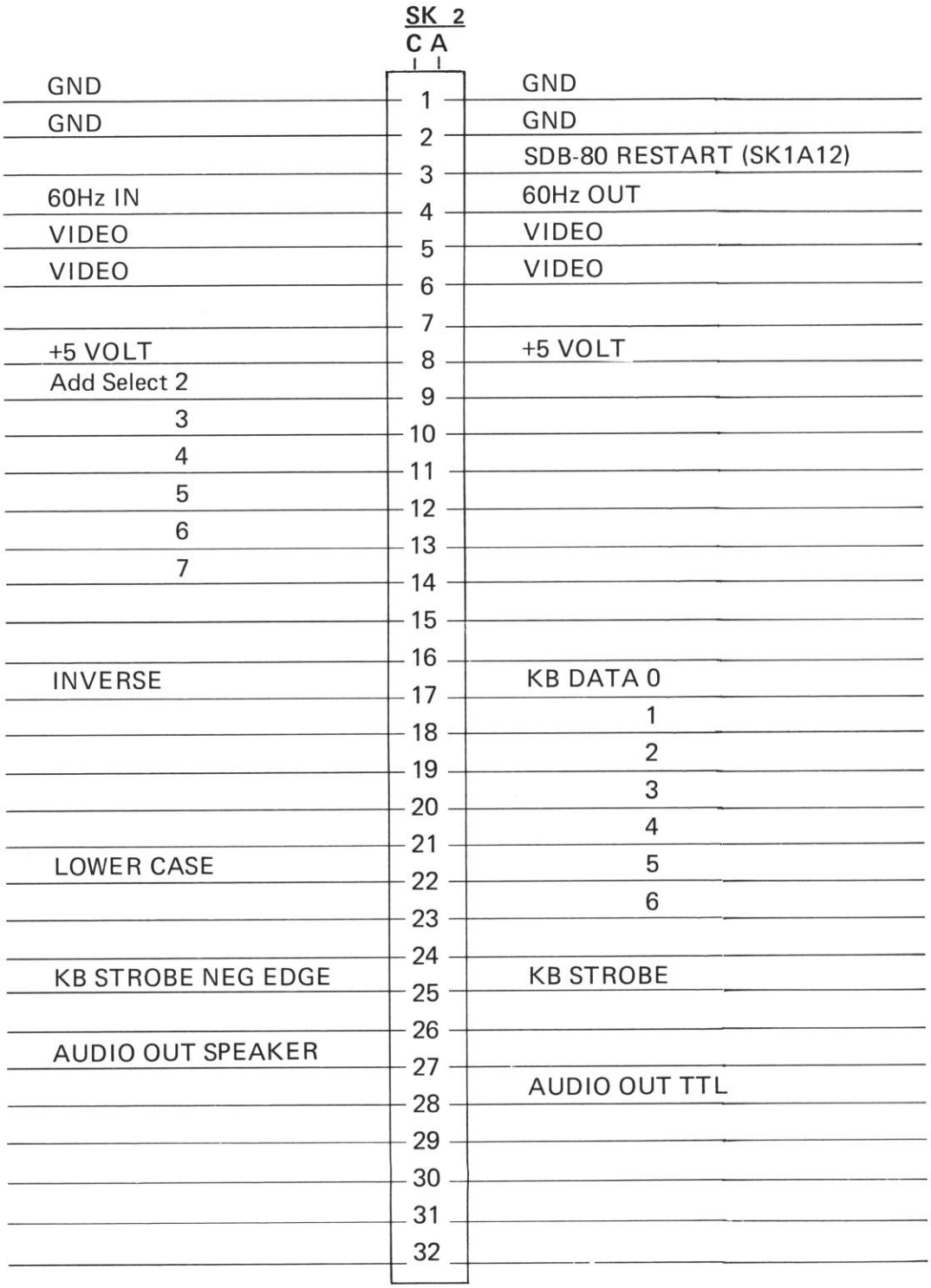
Table 3

C4, A4	50/60Hz	shorting SK2 C4 to SK2 A4 selects a 50Hz frame rate, open is 60Hz;
A17 - 23	KB data	true high
A25	KB strobe	level indicating valid data. Active together with an after data. Response time, max. 130 μs.
C25	KB strobe	edge 1 = data strobed on neg. edge 0 = data strobed on pos. edge
C22	Upper and lower case	1 = convert upper case to lower 0 = normal keyboard data This signal only affects the keyboard data. Computer data will be displayed as received.
SK2, C17	INVERSE	1 = Inverted video 0 = Programmable inverted or Normal video.
A28	Audio out	TTL oscillator output
C27	Audio out	50 Ohm speaker direct drive
C5, A5 C6, A6	Video	EIA video output (comp sync)
C9 C14	Port address	bits 2-7 of the addressing for the on-board PIO
SK1	$\overline{RD}$, $\overline{IORQ}$, $\overline{MI}$, $\overline{INT}$, Φ, DO-7, AO-7, $\overline{DIN}$	These are Z80 control signals
SK1 C8 A8	IEI IEO	Interrupt priority in Interrupt priority out
SK1 C9 A9	BAI BAO	Bus acknowledge in Bus acknowledge out

7.oa

* only required for 2708 PROMs

7.ob


SK 2
C A
GND
GND
60Hz IN
VIDEO
VIDEO
+5 VOLT
Add Select 2
3
4
5
6
7
INVERSE
LOWER CASE
KB STROBE NEG EDGE
AUDIO OUT SPEAKER
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
GND
GND
SDB-80 RESTART (SK1A12)
60Hz OUT
VIDEO
VIDEO
+5 VOLT
KB DATA 0
1
2
3
4
5
6
KB STROBE
AUDIO OUT TTL

8.0 Options

Table 4

	Open	Closed
Current loop	BR 3 BR 4	
RS 232		BR 3 BR 4
ROM char. Gen. PROM char. Gen.	BR7 1-2 BR7 3-2	BR7 2-3 BR7 1-2

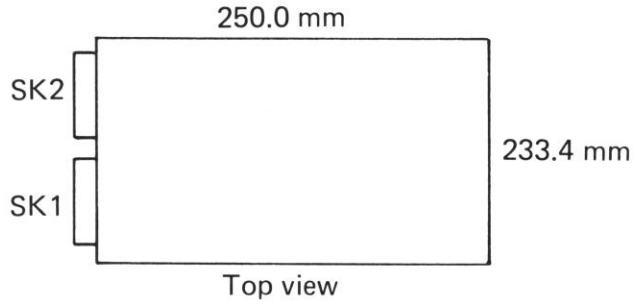
9.0 On Board -5V Regulator

Insert:	AI	LM 320
	R20	22 Ohm 1 Watt
	C30	10 μF/16 Volt

This optional Regulator is provided for cases where 2708 PROMs are used and -12 V is available.

10.0 Mechanical

The VDI-S and VDI-P cards are constructed on an extended double Eurocard format, 233.4 x 250.0 mm. The card thickness is maximum 14 mm above the top of the card, and 4 mm maximum below the top of the card.



2- 64 pin, row A-C assembled, DIN type 41612 indirect connectors are used on the card for all interconnections to the rest of the system.

VDI (S) = Serial only (P) = Parallel only

11.0 Circuit Description

Table 5

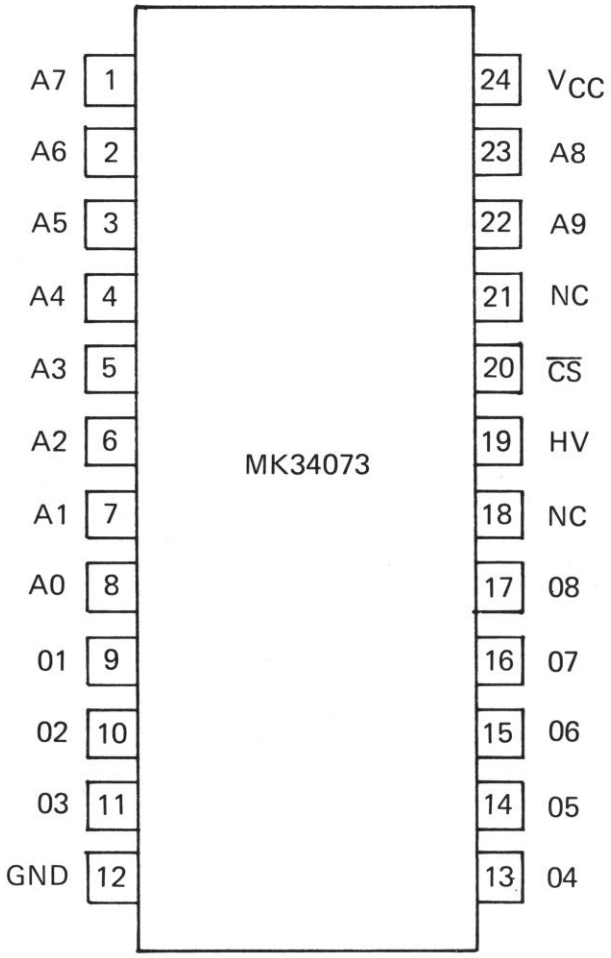
IC	TYPE	FUNCTION
1A	LM320	-5 V Regulator from -12 V for PROM operation (optional)
2A	TIL111	Opto Isolator for current loop data in (S)
3A	74SL14	Control Bus receiver (P)
4A	8T28	Data bus buffer (P)
5A	8T28	Data bus buffer (P)
6A	74LS266	A - Keyboard edge programming B - RS 232 - current loop data in or function C - Video data inverter, cursor or invert video D - Horizontal and vertical sync mixer
7A	74LS266	A - B - Chip select decoding (P) C - Data in enable to SDB-80 D - Priority interrupt in buffer
10A	74LS266	Chip select decode (P)
11A	74LS244	Receiver of KB data
12A		2.2K pullup resistor for KB input
14A	TIL111	Opto Isolator for current loop/RS232 data out (S)
1B	74163	Vertical row Generator for character ROM ÷9 for 60Hz, 11 for 50Hz
2B	7496	5 bit shift register of video data
3B	7404	A-RS232 receiver B-110 Baud generator C- UART/PIO data ready
4B	74393	Baud rate generator (S)
5B	switch	Baud rate switch (S)
6B	7404	Bus direction control (P)
7B	74121	Bell pulse width
8B	74LS51	Bus buffer direction control (P)
9B	7406	a,b,c - bus direction control (P) d - current driver for TIL111 (S) e,f - INT (P)
10B	2.2K	pullup resistor network
11B	7400	a - PROM/ROM program enable b- c- CPU RAM cycle enable d- line clear enable
13B	74200	a- write/$\overline{\text{read}}$ buffer b- write pulse generator for RAM
1C	34073	Character generator
3C	IM6402	UART (S)
4C	MK3881	Z80 PIO (P)
6C	3850	F8 CPU
8C	3871	F8 PIO
9C	74LS266	a- cursor/invert video b- c- force inverted video d- mix cursor + inverse video

Circuit Description (Cont'd)

Table 5 (Cont'd)

IC	TYP	FUNCTION
10C	7474	Blanking delay
11C	3861	F8 PIO
12C	3853	F8 SMI
13C	2708/34xxx	Program Storage Unit
14C	7410	a- RAM data strobe
		b-
		c- Data strobe inverter
IE	74273	RAM data latch
		cursor delay buffer
2E	7492	Baud rate generator,
		÷6 for master
		÷2 for 300 baud (S)
3E	7410	a-UC/LC buffer
		b-110 Baud generator (S)
		c-Audio out gate
4E, 5E	74173	RAM data latch for CPU readback
6E	74LS266	horizontal address match, for cursor and read/write
7E	74161	horizontal counter, LSB
8E	74161	horizontal counter, MSB
10E	7474	a - read/write cycle
		b- CPU strobe latch
11E	7404	
12E	7400	a- advance char strobe for cursor/inverse video
		b- blanking mixer, sync and RAM access
		c- force space during blanking
		d- vertical sync timing
13E	7470	stores previous invert status during read/write. Delays invert status.
14E	7408	a- vertical bland and short count
		b- horizontal sync
		c-
		d- horizontal sync
1-8F	4102	odd line display storage
9F	7402	a- horizontal sync
		b- 7496 preload, 1 bit time
		c- blanking mixer, vert. + horz.
		d- vert. sync generator
10F	74LS51	a- horizontal blank generator
		b- bit 0 of vert. address mux.
11F	7474	a- cursor delay
		b- cursor/invert delay
12F	7492	a- main timing generator ÷ 6
		b- vertical counter ÷ 2
13F	7404	
1-8G	4102	even line display storage
9G	74283	address compactor
10G	82S123	modulo 3 adder for scroll
11G	74283	scroll offset adder
12G	74157	CPU/Display cycle vert. mux
13G	74LS266	vert. cursor address match
14G	7493	vert. counter, 14

Note: All standard TTL may be replaced by LS.



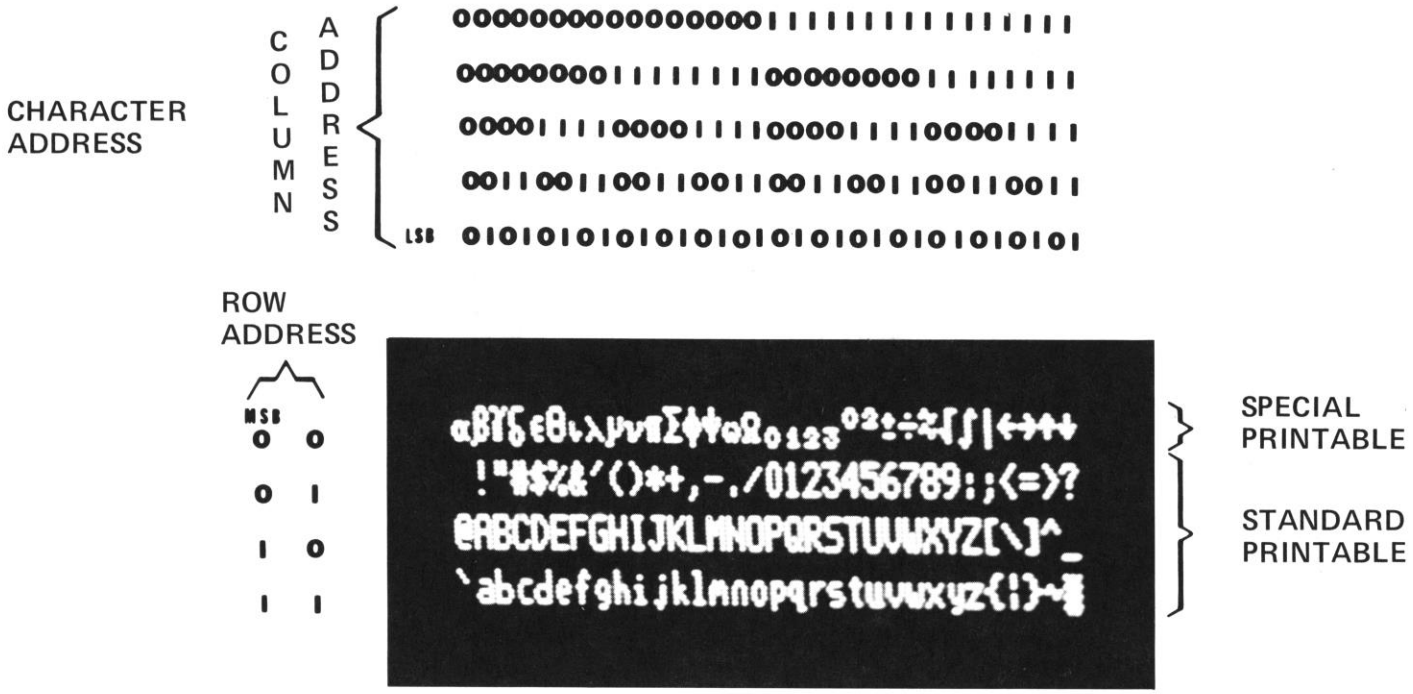
CHARACTER GENERATOR

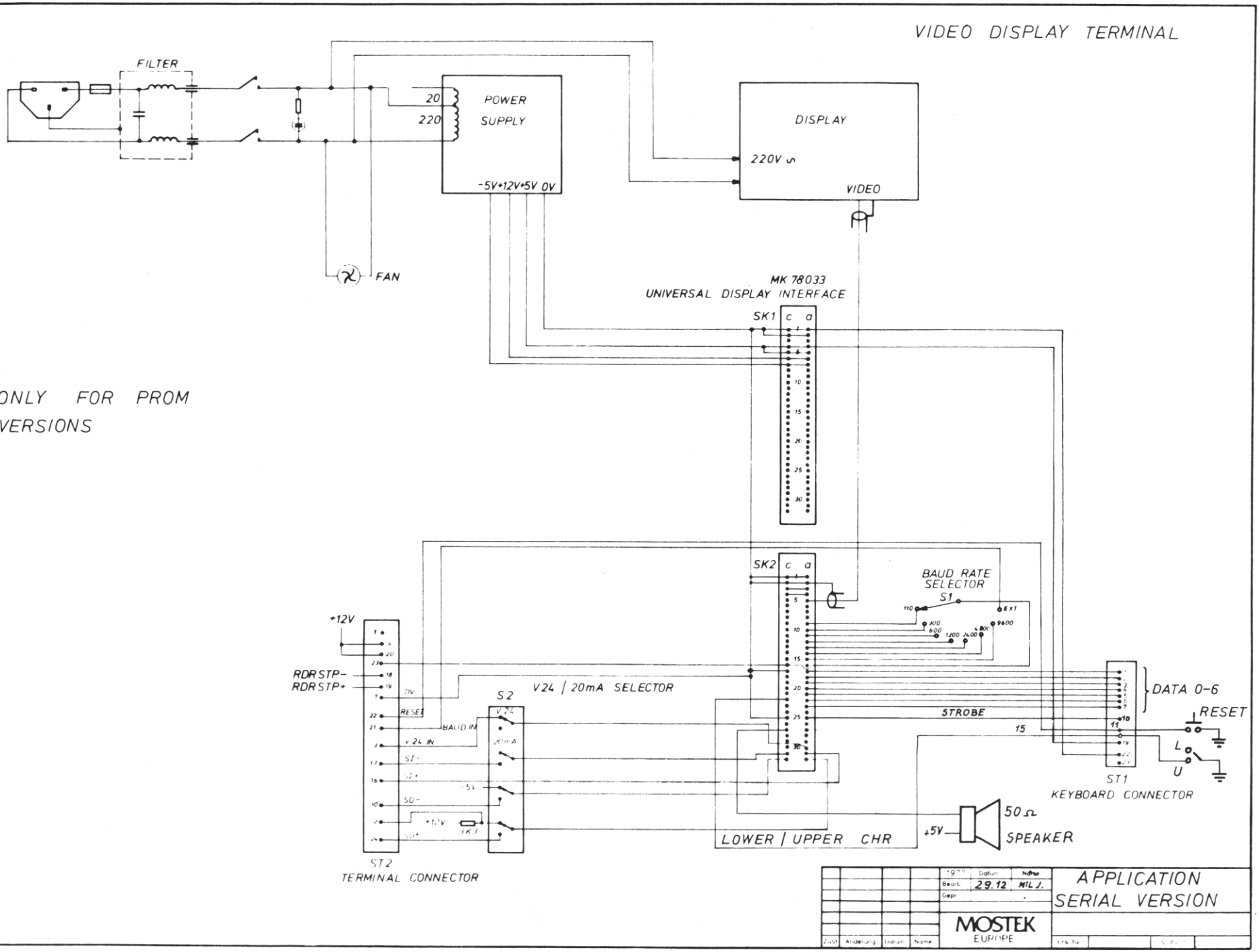
A2-A0 Line/Column Address

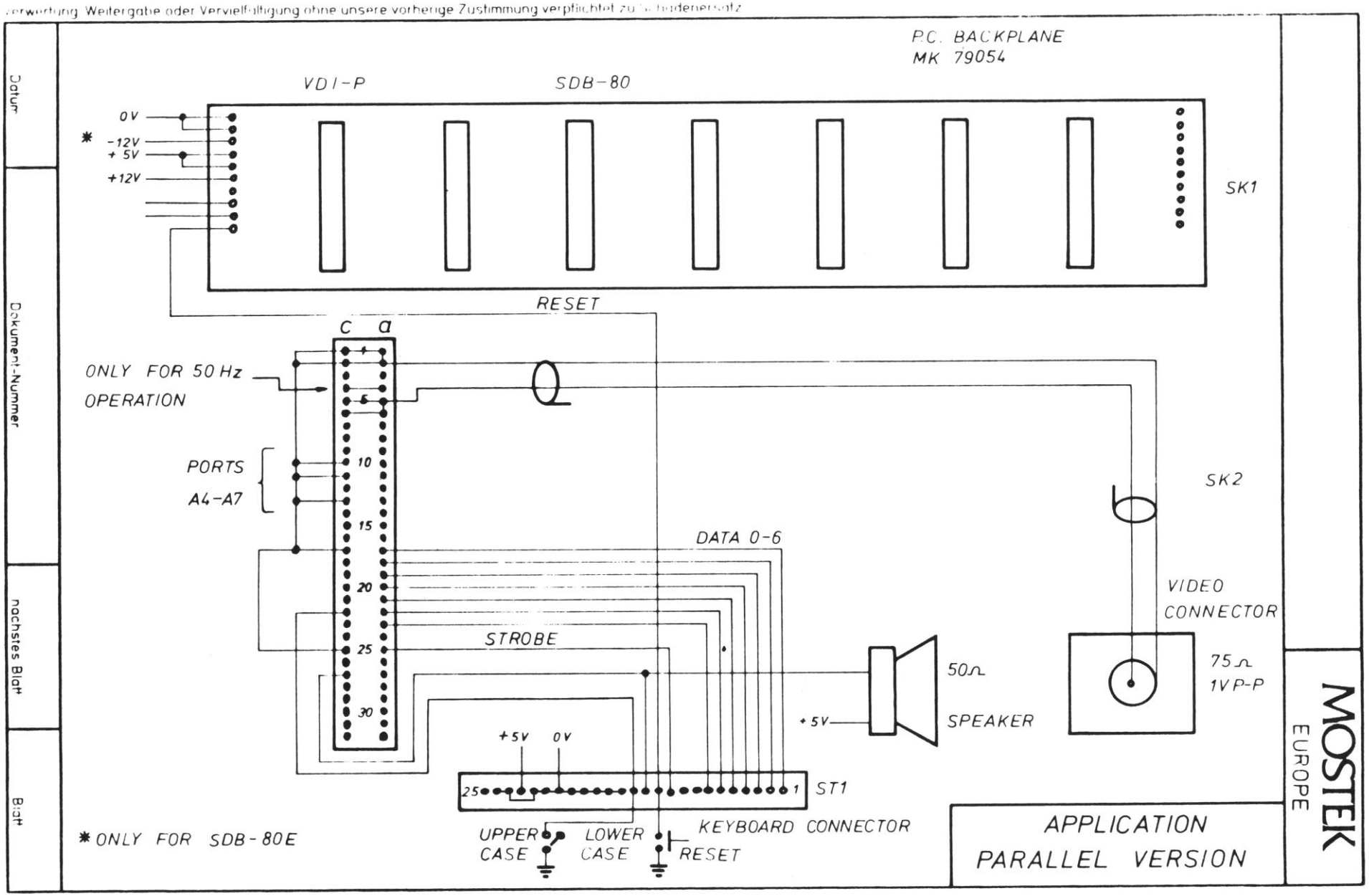
A9-A3 Seven bit ASCII Code

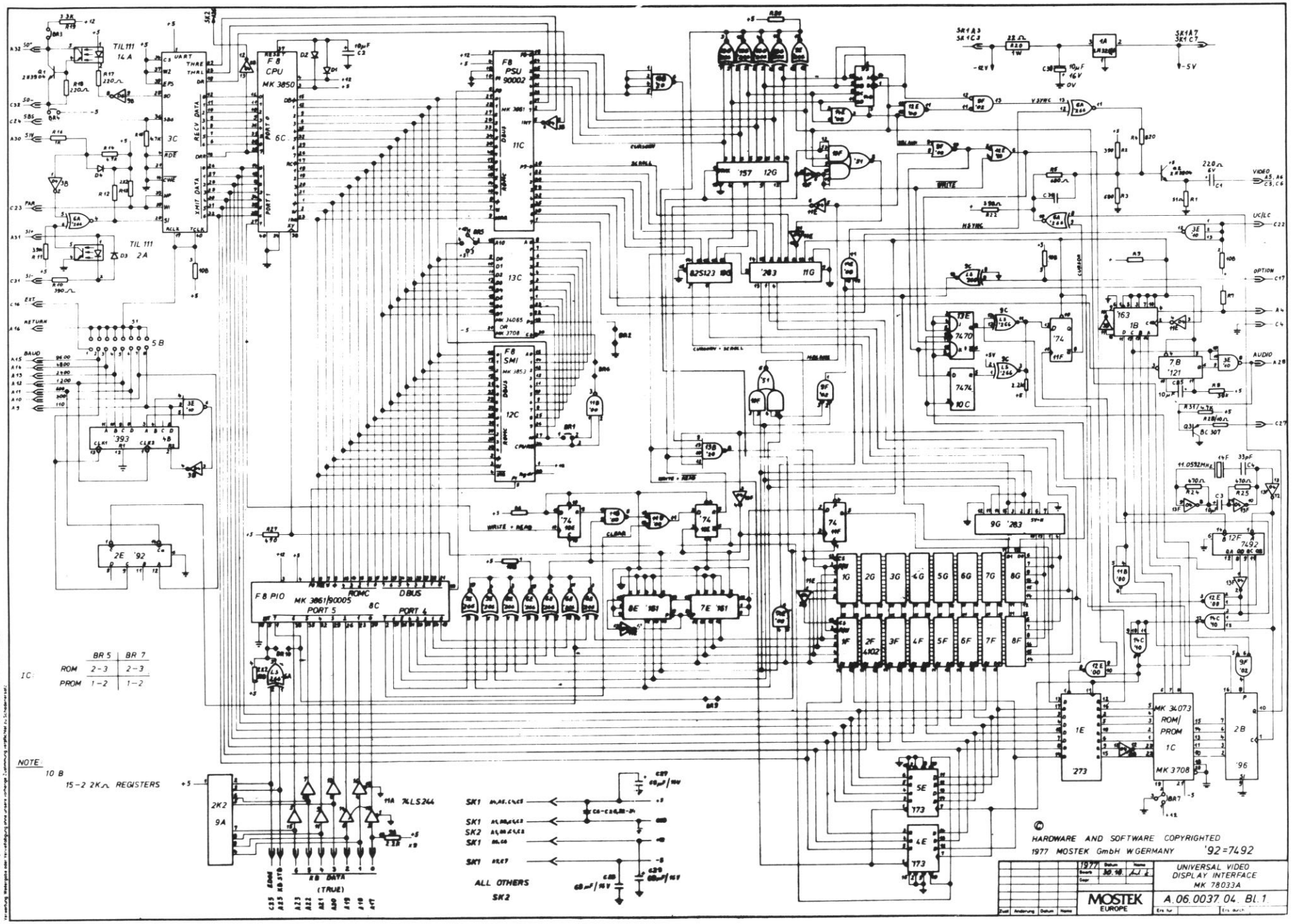
HV GND for Horiz. Out, V_{CC} for Vert. Out

ASCII CHARACTER SET
Figure 3-1



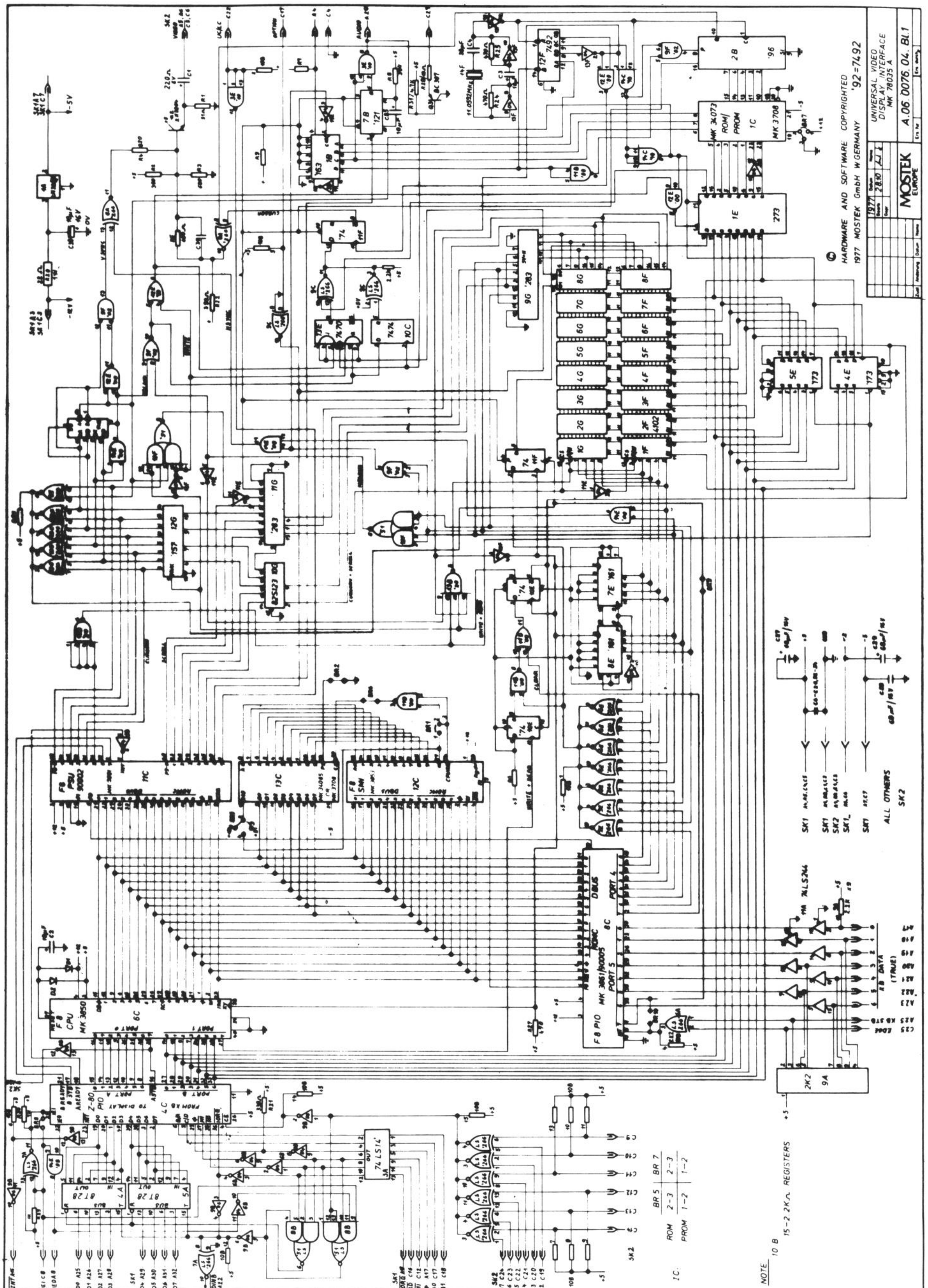

VIDEO DISPLAY TERMINAL
FILTER
20
220
POWER
SUPPLY
-5V+12V+5V 0V
DISPLAY
220V ~
VIDEO
FAN
MK 78033
UNIVERSAL DISPLAY INTERFACE
SK1
SK2
BAUD RATE
SELECTOR
S1
EXT
+12V
RDRSTP-
RDRSTP+
V24 / 20mA SELECTOR
S2
RESET
BAUD IN
V.24 IN
STROBE
DATA 0-6
RESET
L
U
ST1
KEYBOARD CONNECTOR
50 Ω
+5V
SPEAKER
LOWER / UPPER CHR
ST2
TERMINAL CONNECTOR
* ONLY FOR PROM
VERSIONS
APPLICATION
SERIAL VERSION
MOSTEK
EUROPE





IC:	BR 5	BR 7
ROM	2-3	2-3
PROM	1-2	1-2

NOTE:
10 B
15-2 2KΩ REGISTERS


HARDWARE AND SOFTWARE COPYRIGHTED
1977 MOSTEK GmbH W.GERMANY
'92 = 7492
UNIVERSAL VIDEO DISPLAY INTERFACE
MK 78035 A
A.06.0076.04. Bl.1
MOSTEK EUROPE
NOTE
IC 10 B
15 - 2.2KΩ REGISTERS
BR 5 BR 7
ROM 2-3 2-3
PROM 1-2 1-2
ALL OTHERS SK2

APPENDIX A

```
                                VDITST LISTING    PAGE   0001
 LOC   OBJ CODE   STMT SOURCE STATEMENT

                  0001 ;  VDI-P TEST PROGRAM
                  0002 ;
                  0003 ; EACH TIME A KEYBOARD KEY IS PUSHED, THE SCREEN
                  0004 ; REWRITTEN WITH THE DEPRESSED KEY DISPLAYED.
                  0005 ; SET VDI-P TO RESPOND TO PORTS 0-3
                  0006 ; IF THE KEY PUSHED WAS A CURSOR CONTROL CHARACTE
                  0007 ;    WILL BE MOVED INTHE DIRECTION THAT THE CURSO
                  0008 ;
                  0009 ; INITIALIZE PIO:
0000   21F201     0010 START     LD      HL,INIT     ; SEND CONTROL WORDS
0003   0603       0011           LD      B,3         ; # OF BYTES
0005   0E00       0012           LD      C,INCNTL    ; INPUT CONTROL PORT
0007   EDB3       0013           OTIR                ; SEND 3 CONTROL BYTES
0009   0603       0014           LD      B,3
000B   0E02       0015           LD      C,OTCNTL    ; OUTPUT CONTROL PORT
000D   EDB3       0016           OTIR                ; OUTPUT CONTROL FOLLOWS INPUT
000F   DB41       0017           IN      A,(INDATA) ; INIT INPUT PORRT
0011   3E01       0018           LD      A,IVECTOR/256 ; SET UP REGISTER I
0013   ED47       0019           LD      I,A
0015   ED5E       0020           IM      2           ; SET MODE 2
                  0021 ;
                  0022 ; OUTPUT DATA
                  0023 ;
0017   214801     0024 OUTPUT    LD      HL,MESSAGE
001A   0606       0025           LD      B,LENGTH    ; # BYTES IN MESSAGE
001C   0E03       0026           LD      C,OTDATA    ; PORT ADDRESS
001E   EDA3       0027           OUTI                ; START SEQUENCE
                  0028 ;
                  0029 ; SET UP INPUT
                  0030 ;
0020   DD214801   0031           LD      IX,MESSAGE ; KB DATA WILL BE STORED HERE
0024   FB         0032           EI                  ; ENABLE INTERRUPTS
0025   76         0033 WAIT      HALT
0026   18FD       0034           JR      WAIT-$
                  0035 ;
                  0036 ; VECTOR TABLES
                  0037 ;
0180              0038           ORG     180H
0180   8201       0039 JVECTOR   DEFW    OUTRTN
0182   0401       0040 IVECTOR   DEFW    INRTN
                  0041 ;
                  0042 ; INTERRUPT ROUTINES
                  0043 ;
0184   DB01       0044 INRTN     IN      A,(INDATA) ; INPUT ROUTINE, GET DATA
0186   FE3E       0045           CP      '>'         ; IS IT CONTROL?
0188   3007       0046           JR      C,CONTROL-$; CONTROL FCN
018A   5F7F36     0047           LD      (IX+MS-MESSAGE),A ; SAVE IN (MESSAGE)
018D   78         0048           LD      A,B         ; TEST IF OUTPUT BUSY
018E   FE00       0049           CP      LENGTH+1    ; WAITING FOR NEW INPUT?
0190   2000       0050           JR      NZ,EXIT-$   ; NO, DON'T GO TO OUTPUT
                  0051 ;
                  0052 OUTRTN:                       ; OUTPUT ROUTINE
0192   20E7       0053           JRNZ    UNDONE-$
0194   214801     0054           LD      HL,MESSAGE
0197   0606       0055           LD      B,LENGTH+1
0199   1803       0056           JR      EXIT-$
019B   EDA3       0057 UNDONE    OUTI
019D   04         0058           INC     B           ; B IS ALWAYS 1+
```

```
 LOC   OBJ CODE    STMT SOURCE STATEMENT

0A1E   FB         0059 EXIT    EI                ; ENABLE INTERRUPTS
0A1F   ED4D       0060         RETI              ; EXIT
                  0061 ;
0A21   DD3424     0062 CONTROL INC   (IX+V-MESSAGE)
0A24   FE08       0063         CP    08H         ; CURSOR UP?
0A26   28EA       0064         JR    Z,OUTRTN-$
0A28   DD3524     0065         DEC   (IX+V-MESSAGE)
0A2B   DD3524     0066         DEC   (IX+V-MESSAGE)
0A2E   FE0A       0067         CP    0AH         ; DOWN CURSOR
0A30   28E0       0068         JR    Z,OUTRTN-$
0A32   DD3424     0069         INC   (IX+V-MESSAGE)
0A35   DD3425     0070         INC   (IX+H-MESSAGE)
0A38   FE0C       0071         CP    0CH         ; CURSOR RIGHT
0A3A   28D6       0072         JR    Z,OUTRTN-$
0A3C   DD3525     0073         DEC   (IX+H-MESSAGE)
0A3F   FE08       0074         CP    08H         ; CURSOR LEFT
0A41   2009       0075         JR    NZ,EXIT-$
0A43   DD3525     0076         DEC   (IX+H-MESSAGE)
0A46   18CA       0077         JR    OUTRTN-$
                  0078 ;
                  0079 DTDATA  EQU   3
                  0080 CTCNTL  EQU   2
                  0081 INCNTA  EQU   1
                  0082 IPCNTL  EQU   0
                  0083 ;
0A48   1E         0084 MESSAGE DEFB  1EH         ; HOME
0A49   19         0085         DEFB  19H
0A4A   1D         0086         DEFB  1DH         ; CLEAR SCREEN
0A4B   204120     0087         DEFM  ' A '
0A4E   2A         0088 KB      DEFB  '*'         ; KEYBOARD DATA
0A4F   2057415320 0089         DEFM  ' WAS TYPED ON THE KEYBOARD'
0A69   18         0090         DEFB  18H
0A6A   18         0091         DEFB  18H         ; ESCAPE
0A6B   3D         0092         DEFB  '='         ; SET CURSOR
0A6C   08         0093 V       DEFB  8           ; VERTICAL LINE 8
0A6D   0A         0094 H       DEFB  10          ; HORIZONTAL POSITION 10
0A6E   4041424300 0095         DEFM  '@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_'
0A8E   2021222300 0096         DEFM  ' !"#$%&''()*+,-./0123456789:;<=>?'
0AAE   0D0A       0097         DEFW  0A0DH       ; RETURN LINE FEED
0AB0   18         0098         DEFB  ''
0AB1   1840414200 0099         DEFM  '@ABCDEFGHIJKLMNOP'
0AD1   1051525300 0100         DEFM  'QRSTUVWXYZ[\]^_'
0AE5   19         0101         DEFB  ''
0AF0   0A0A       0102         DEFW  0A0AH       ; 2 X LINE FEED
                  0103 LENGTH  EQU   $-MESSAGE
                  0104 ;
                  0105 ; PIO INIT DATA
                  0106 ;
0AF2   4F         0107 INIT    DEFB  4FH         ; INPUT PIO, SET MODE
0AF3   02         0108         DEFB  IVECTOR&0FFH ; VECTOR ADDRESS
0AF4   83         0109         DEFB  83H         ; ENABLE INTERRUPTS
                  0110 ;
0AF5   0F         0111         DEFB  0FH         ; OUTPUT MODE
0AF6   02         0112         DEFB  OVECTOR&0FFH ; VECTOR
0AF7   83         0113         DEFB  83H         ; ENABLE INT.
                  0114         END
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