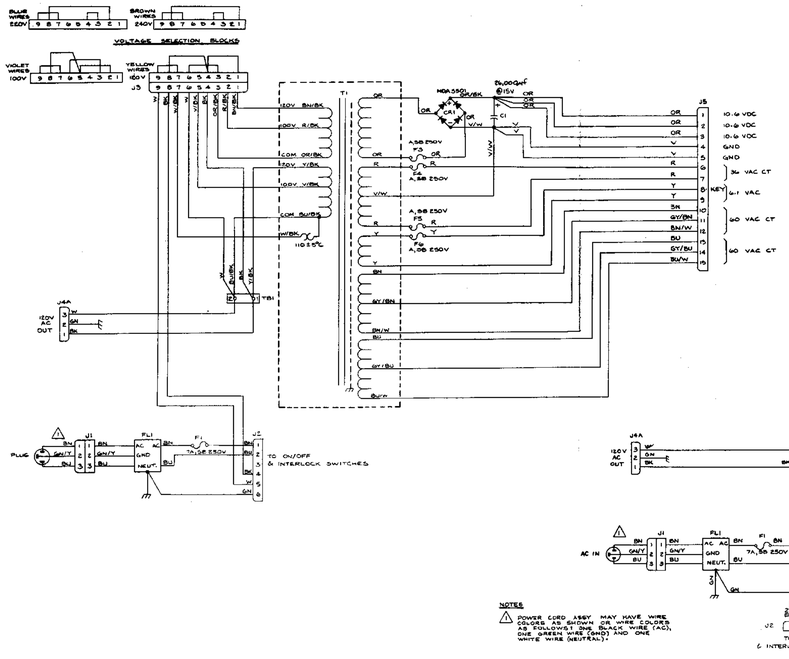
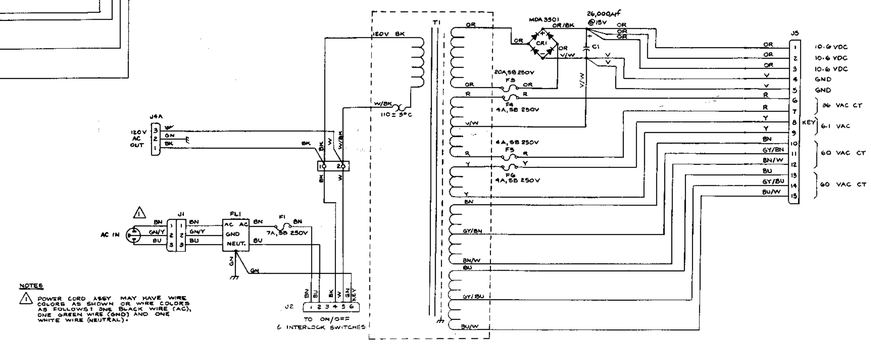
INTERNATIONAL X-Y POWER SUPPLY WIRING DIAGRAM (035887-01 A)



NOTES

⚠ POWER CORD ASSY MAY HAVE WIRE COLORS (3) SHOWN OR WIRE COLORS AS FOLLOWS: (ONE BLACK WIRE (HOT) ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).

U.S. X-Y POWER SUPPLY WIRING DIAGRAM (036352-01 A)



REGULATOR/AUDIO I PCB SCHEMATIC (034485-03 A)

Regulator/Audio I PCB

The Regulator/Audio I PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

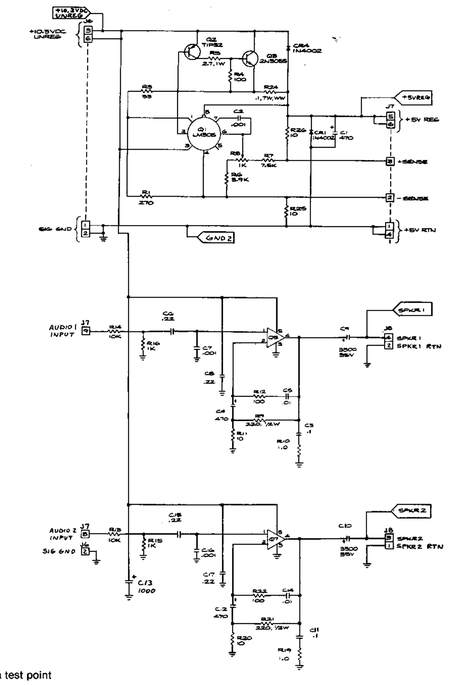
The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high-impedance inputs +SENSE and −SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio I PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio I PCB. Voltage reading must not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio I PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio I PCB and plus lead to GND test point of game PCB. Note the voltage.
   Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio I PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

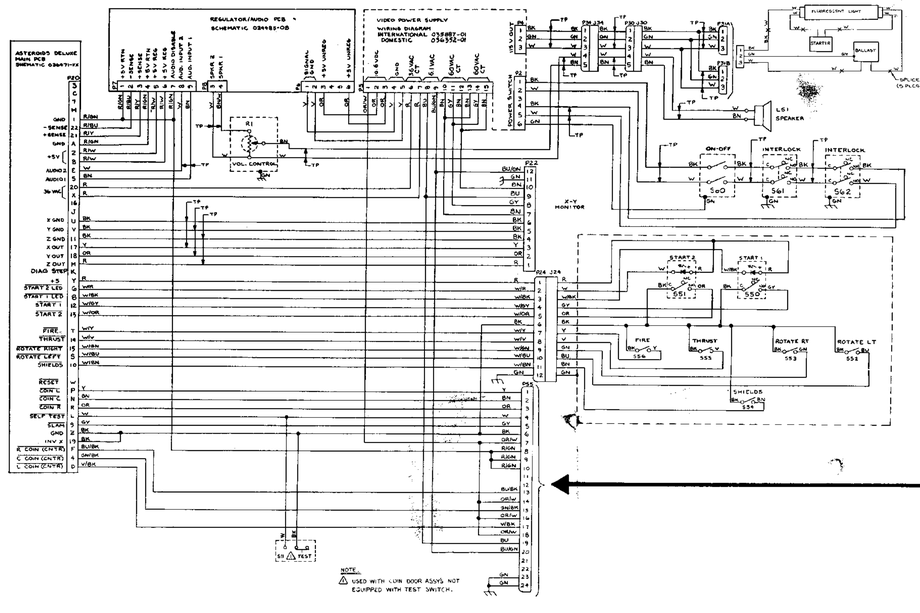
Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten.

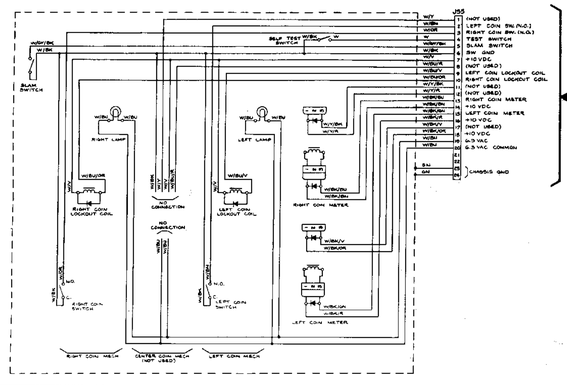


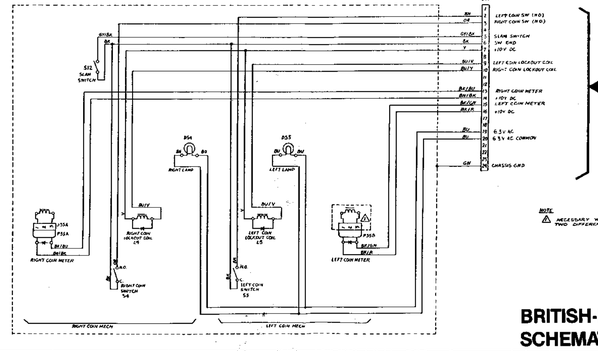
Denotes a test point

ASTEROIDS DELUXE™ WIRING DIAGRAM (036687-01 A)



U.S. COIN DOOR SCHEMATIC (034988-01)





NOTE
⚠ NECESSARY WITH COIN DOORS USING TWO DIFFERENT DENOMINATIONS.

BRITISH-MADE COIN DOOR SCHEMATIC (037050-01 A)

Drawing Package Supplement

to

ASTEROIDS DELUXE™

Operation, Maintenance and Service Manual

Contents of this Drawing Package

ATARI®
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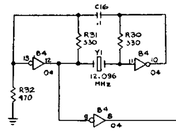
Sheet 1, Side A
DP-165-01 1st printing

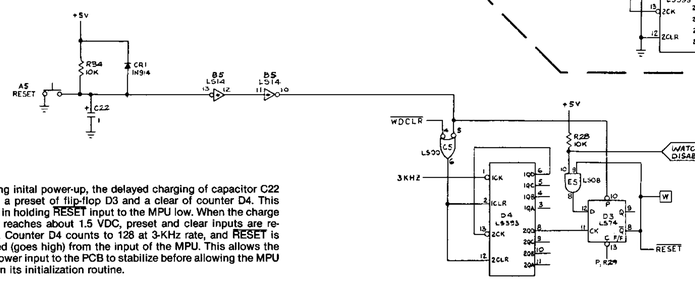
CLOCK CIRCUIT



The clock circuit consists of crystal Y1 and associated inverters and counters C3 and B3. Counters C3 and B3 count the crystal frequency down to the frequencies necessary for the Asteroids Deluxe™ game.

NOTE:
The MPU in this game operates at a frequency of 1.5 MHz. Therefore the MPU chip must be the 6502A. The 6502's maximum frequency is 1 MHz and is not compatible with this game.

POWER RESET AND WATCHDOG COUNTER

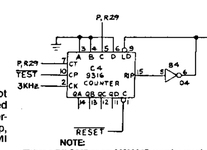


During inital power-up, the delayed charging of capacitor C22 causes a preset of flip-flop D3 and a clear of counter D4. This results in holding RESET input to the MPU low. When the charge of C22 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D4 counts to 128 at 3-KHz rate, and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D4 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D4 will count up to the RESET state and cause the MPU to return to its initialization routine.

Denotes a test point

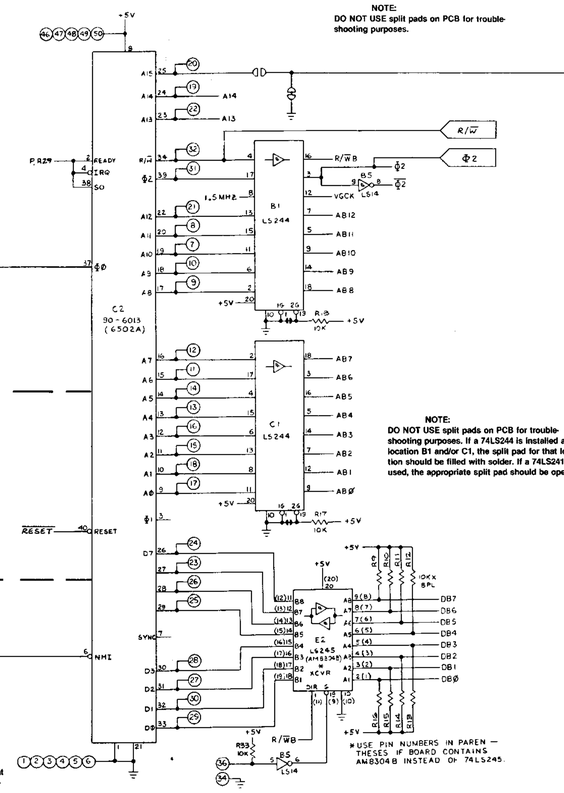
NMI COUNTER



The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C4. The interrupt occurs when pin 6 of inverter B4 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

NOTE:
Either a 74LS245 or an AM8304B may be used at location E2. Pin numbers not enclosed in parentheses are for 74LS245. Pin numbers in parentheses are for an AM8304B.

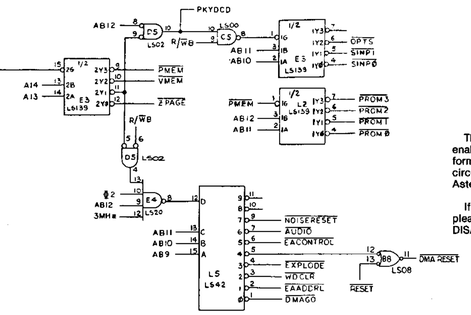
MPU CIRCUITRY



NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes.

NOTE:
DO NOT USE split pads on PCB for trouble-shooting purposes. If a 74LS244 is installed at location B1 and/or C1, the split pad for that location should be filled with solder. If a 74LS241 is used, the appropriate split pad should be open.

ADDRESS DECODING CIRCUITRY



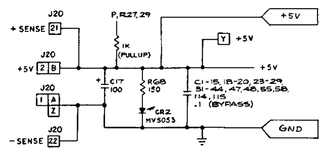
The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids Deluxe™ game.

If you are going to use the Automatic RAM/ROM Tester, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

MEMORY MAP

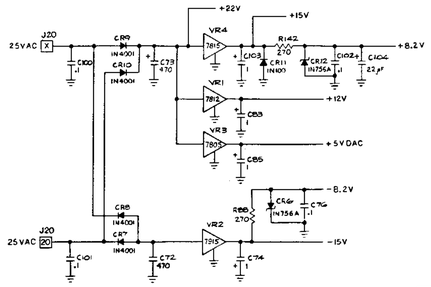
	HEXADECIMAL	ADDRESS A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0-3FF																										Scratch RAM
INPUTS	2000		0	1	0	0	0								0	0	0	R									Not used
	2001		0	1	0	0	0								0	0	1	R	D								3 KHz
	2002		0	1	0	0	0								0	1	0	R	D								VG halted
	2003		0	1	0	0	0								0	1	1	R	D								Shield switch
	2004		0	1	0	0	0								1	0	0	R	D								Fire switch
	2006		0	1	0	0	0								1	1	0	R	D								Slam switch
	2007		0	1	0	0	0								1	1	1	R	D								Self-test switch
	2400		0	1	0	0	1								0	0	0	R	D								Left coin switch
	2401		0	1	0	0	1								0	0	1	R	D								Center coin switch
	2402		0	1	0	0	1								0	1	0	R	D								Right coin switch
	2403		0	1	0	0	1								0	1	1	R	D								1-player start switch
	2404		0	1	0	0	1								1	0	0	R	D								2-player start switch
	2405		0	1	0	0	1								1	0	1	R	D								Thrust switch
	2406		0	1	0	0	1								1	1	0	R	D								Rotate right switch
	2407		0	1	0	0	1								1	1	1	R	D								Rotate left switch
	2800		0	1	0	1	0										0	R							D	D	Option switch 8, 7 (at P5)
	2801		0	1	0	1	0										1	R							D	D	Option switch 6, 5
	2802		0	1	0	1	0										0	R							D	D	Option switch 4, 3
	2803		0	1	0	1	0										1	R							D	D	Option switch 2, 1
OUTPUTS	2000		0	1	0	1	1		0				A	A	A	A	A	R									POKEY
	2C40		0	1	0	1	1		1	A	A	A	A	A	A	A	A	R									EAROM read
	3000		0	1	1	0	0	0										W									Start VG
	3200		0	1	1	0	0	1			A	A	A	A	A	A	A	W	D	D	D	D	D	D	D	D	Latch EA address/data
	3400		0	1	1	0	1	0										W									Watchdog reset
	3600		0	1	1	0	1	1										W	D	D							Explosion pitch
	3600		0	1	1	0	1	1										W			D	D	D	D			Explosion volume
	3800		0	1	1	1	0	0										W									3800 VG reset
	3A00		0	1	1	1	0	1										W							D	D	EA control latch
	3C00		0	1	1	1	1	0										W	D								1-player start LED
	3C01		0	1	1	1	1	0										0	D								2-player start LED
	3C02		0	1	1	1	1	0										1	D								Not used
	3C03		0	1	1	1	1	0										0	D								Ship thrust sound
	3C04		0	1	1	1	1	0										1	D								Bank select
	3C05		0	1	1	1	1	0										0	D								Left coin counter
	3C06		0	1	1	1	1	0										1	D								Center coin counter
	3C07		0	1	1	1	1	0										1	D								Right coin counter
	3E00		0	1	1	1	1	1										W									Noise generator reset
RAM, ROM	4000		1	0	0	0	0																				Vector RAM
	4400		1	0	0	0	1																				Vector RAM
	4800		1	0	0	1																					Vector ROM
	5000		1	0	1	0												R									Vector ROM
	6000		1	1	0	0												R									Program ROM
	6800		1	1	0	1												R									Program ROM
	7000		1	1	1	0												R									Program ROM
	7800		1	1	1	1												R									Program ROM

POWER INPUT



This circuitry consists of the PCB inputs and outputs for the + 5 VDC logic power and 25 VAC input to the on board regulators. The + 5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 25 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR8 rectify the negative cycle of the input and the 7915 regulates the voltage at -15 VDC. Diodes CR9 and CR10 rectify the positive pulse of the 25 VAC input and the 7815 regulates the voltage at + 15 VDC. The 7812 regulates at + 12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR12 supplies the + 8.2 VDC for the sample and hold circuit. The + 22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.

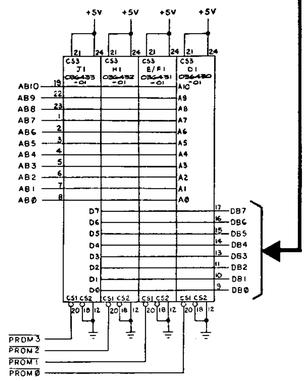


Denotes a test point

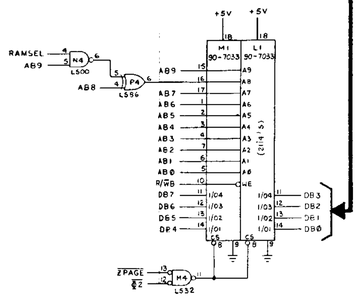
ROM/PROM CIRCUITRY

FROM SWITCH INPUTS SHEET 2, SIDE B

Program memory for the Asteroids Deluxe™ game is contained in three ROMs.



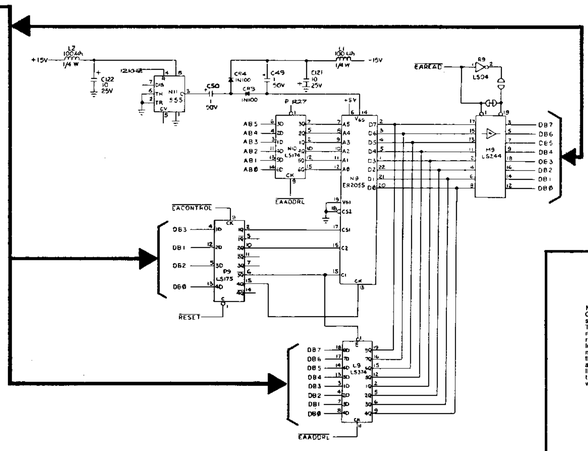
RAM CIRCUITRY



The RAM is the temporary storage space for the MPU and is enabled when ZPAGE (Zero Page enable) is low. When R/WB (from the MPU) is low, the RAM stores the data byte input (DB0 thru DB7) at the location addressed by the MPU address bus (AB0 thru AB7). When R/WB is high, the MPU reads the stored data byte at the addressed location.

The signal RAMSEL, when low, has the effect of swapping pages 2 and 3 within the RAM. This allows greater programming flexibility.

HIGH SCORE CIRCUITRY



The High Score Memory circuit consists of an erasable reprogrammable ROM N9, latches L9, P9, N10 buffer M9, and timer N11.

N11 produces a 12KHz O-15V squarewave. This signal when + 15, forward biases diode CR4 and allows capcitor C50 to charge th -29V. When it's 0V, CR4 is then cut-off and CR3 is forward biased which causes C49 to develop a charge. C49 charges to approximately -28V. This is the potential required for EAROM N9 to operate.

The MPU addresses the EAROM (AB0-AB5) via latch N10, when EAADDRL goes high, and data is latched into the EAROM on DB0-DB7 through latch L9.

The function of the EAROM (read, write or erase) is determined by the MPU on data lines DB0-DB3. Latch D9 receives a high EACONTROL signal from the MPU address decoder and function data is passed to the EAROM.

Data in the EAROM is read by the MPU when the EAREAD is addressed by the MPU after a reset pulse or during self-test.

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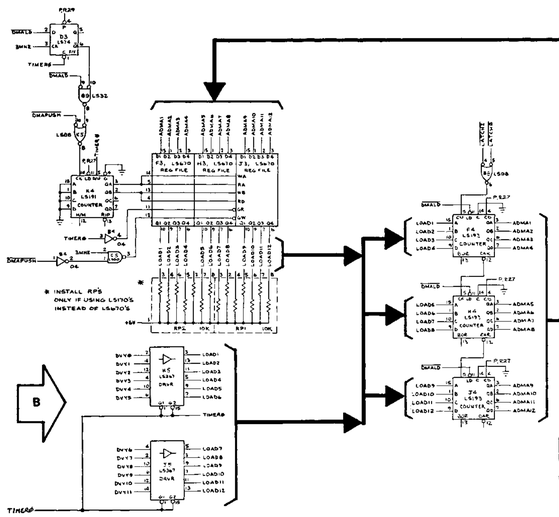
Sheet 1, Side B

ASTEROIDS DELUXE™
Microprocessor
Section of 036471-02 A

Sheet 1, Side B
DP-165-01 1st printing

PROGRAM COUNTER

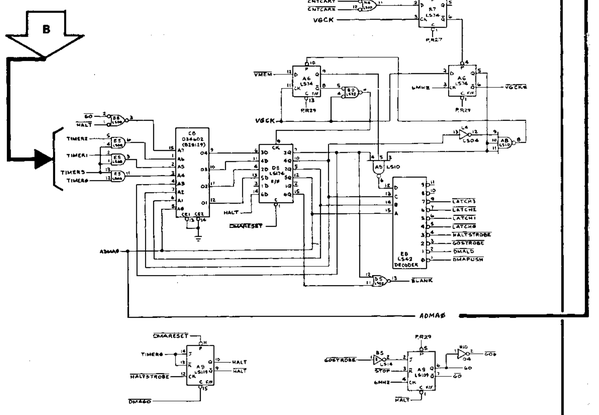


Counters F4, H4 and J4 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be retrieved and performed, they are called the program counter. This program counter is incremented one count (to the next sequential address) each time the information at its current address is loaded into data latch 0 or data latch 2.

The program counter may also be preset to "jump" to a new address. This new address can be loaded into the program counter from the vector generator memory via data latches F6 and H6 and buffers H5 and J5.

The program counter may also be preset to "return" to a previous address which it had stored in its "stack". The stack consists of register files F3, H3, & J3, and down/up counter K4. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMAPUSH is low. Immediately after information is written into the stack, counter K4 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.

STATE MACHINE



The state machine is the "master controller" of the vector-generator circuitry. It receives instructions from the game MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector-generator ROM memory, using the vector-generator program counter to do so. The state machine reads the vector-generator ROM data (via Timer 0-3) and decodes this information to determine how it should use this data: 1) to draw a vector; 2) to move the monitor beam to a new position on the monitor display; 3) to "jump" to a new vector memory address; 4) to return to a previous vector memory address; or 5) to tell the game MPU that it has completed its current instructions, and is waiting for its next command.

The state machine consists of input gates B8 and E5, ROM C8, latch D8, clock circuitry A6, and decoder E8. Four-bit input TIMER0 thru TIMER3 is the operation-code input to the state machine. The A4 thru A6 address input to ROM C8 tells the ROM which instructions to perform. Address inputs A0 thru A3 from latch D8 tells the ROM which state was last performed. The address A7 input GO tells the ROM that the position counters are presently drawing a vector. The HALT input to A7 tells the ROM that the vector generator has completed its operations.

During initial power-up of the game, the HALT signal is preset low. The microcomputer reads the high HALT signal through its switch input port (sel/mux L10) on data line DB7. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT, clocked through latch D8, results in a low BLANK to the Z-axis output.

The microcomputer outputs an address that results in a DMAGO signal that causes HALT to go high, and clears the vector-generator data latches. This makes TIMER0 thru TIMER3 signals all low. The state machine now begins executing instructions, starting at vector memory location 0.

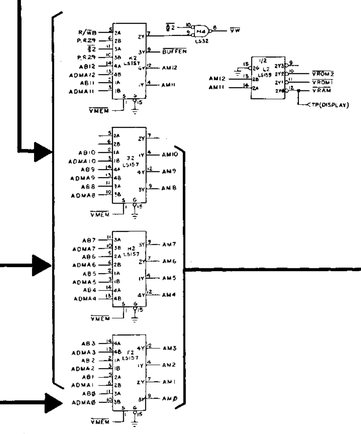
When the state machine receives the operation code for a HALT instruction, it outputs a low HALTSTROBE, setting the HALT flip-flop A9, and suspending state machine operation.

The GO signals load and enable the vector timer and the X and Y position counters and tell the ROM that the vector generator is now actively drawing a vector. The HALT input to GO flip-flop A9 sets the outputs to ensure that the vector timer and position counters are not active when the state machine is halted. When a low GOSTROBE is clocked through A9, the vector timer and X- and Y-position counters begin to operate from the GO, GO and GO* signals. When STOP is clocked through A9, the vector timer has reached its maximum count, and GO goes high. This means the vector has been drawn.

The VGCK input to the clock circuitry is a buffered 1.5-MHz clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (when VMEM goes low). Then the clock input to latch D8 goes high and stays high until VMEM goes high.

FROM MICROCOMPUTER SHEET 1, SIDE B

VECTOR GENERATOR MEMORY ADDRESS SELECTOR

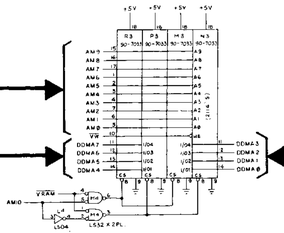


The address selector consists of multiplexers F2, H2, J2 and K2. When VMEM is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, BUFFEN is from Φ2 and VW (vector generator write) is low when Φ2 and R/WB are both low. When VMEM is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, BUFFEN and VW are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer K2.

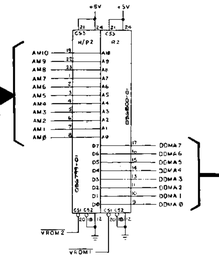
Address decoder L2 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the vector-generator memory.

This address-selecting arrangement allows the game MPU to access the vector-generator memory, i.e., write data into the vector-generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector-generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

VECTOR GENERATOR RAM

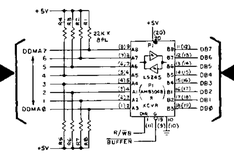


VECTOR GENERATOR ROM

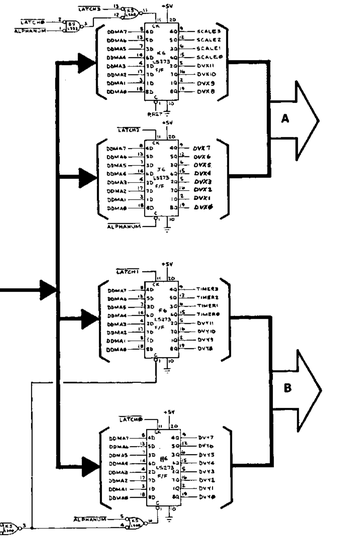


VECTOR GENERATOR DATA BUFFER

TO/FROM MPU DATA BUS SHEET 1, SIDE B



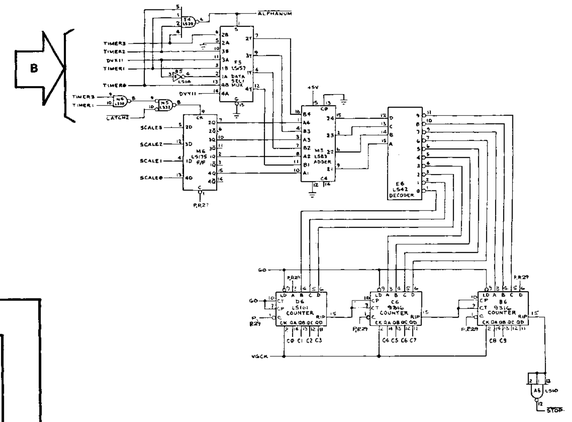
VECTOR GENERATOR MEMORY DATA LATCHES



The data latches consist of latch 0 (H6), latch 1 (F6), latch 2 (J6), and latch 3 (K6). Inputs DDMA0 thru DDMA7 are the data outputs from the vector-generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 1 is cleared by ALPHANUM.

VECTOR TIMER

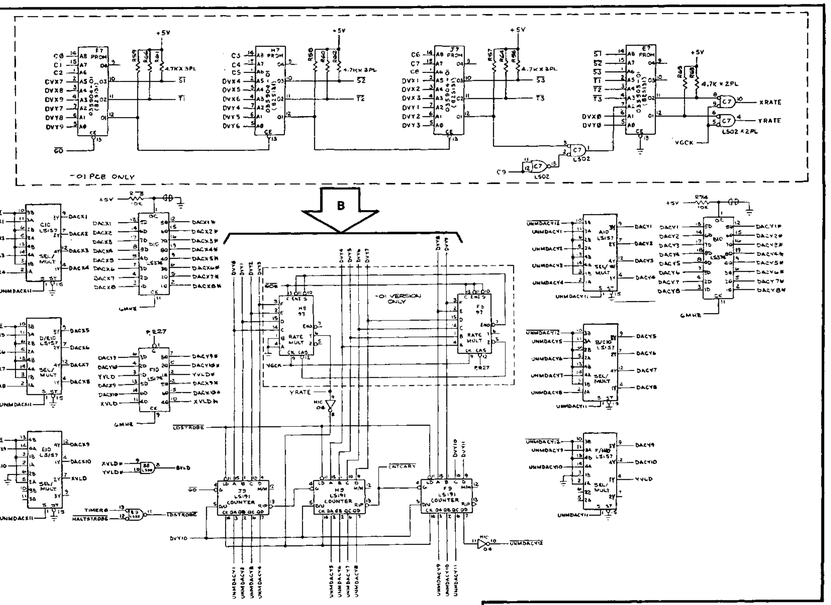


The purpose of the vector timer is to time out the length of time it takes to "draw" an actual vector on the monitor display. During the interval when the X- and Y-position counters are actually drawing the vector, STOP is high. This prevents the vector-generator state machine from advancing to its next state until the vector currently being drawn is completed. As soon as the vector has been drawn, STOP goes low, allowing the state machine to advance to the next state in its intended sequence.

The vector timer consists of multiplexer F5, decoder E6, latch M6, adder M5, and counters B6, C8, and D6. M6 contains a scale factor which is added in M5 to the four timer signals. If TIMER0 thru TIMER3 inputs are any state but all high, decoder E6 directly decodes the sum and loads the decoded low into one of the counters. When GO goes low, the counters count from the loaded count until the counters all reach their maximum count. This count is a maximum length of 1024. At this time STOP goes low and clears the GO flip-flop of the state machine.

If the TIMER signals are all high, ALPHANUM goes low and data signals DVX11 and DVY11 are decoded by decoder E6. This is added to the scale factor and loaded into the counters.

X- AND Y-POSITION COUNTERS



The X- and Y-position counters are two identical circuits. Therefore, the following description discusses only the X-position counters.

The X-position counters contain rate multipliers (J8 and K8), down/up counters (C9, D9 and E9), multiplexers (C10, D/E10, E10), latch (F10), and associated gates (B8 and H10). The output of the down/up counters is a 12-bit binary number that represents the horizontal location of the beam on the monitor screen (or X axis), with 0 being the far left side of the screen and 1023 being the far right side of the screen. Increasing or decreasing this binary number output will cause the beam to move to the right or left, respectively. The vector generator state machine decodes instructions from its memory, and then is capable of using that data to alter the binary count of these counters in one of two ways.

The state machine can preset these counters to an entirely different number from their previous contents. This will cause the beam to "jump" to a new location on the monitor screen instantaneously, i.e., for drawing a new vector from a different starting position than where the previous vector ended. While the beam is "jumping" to this new position, the beam itself is turned off to prevent unwanted lines from appearing on the screen. To preset this new position into the counters, the state generator causes LOSTROBE to go low. At this time, a new 12-bit number (DVX0-11) is loaded into the counters from the vector generator memory data latches.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific distance relative to where it was. During this beam movement, the beam is turned on with the desired intensity. This is the procedure used to draw a vector on the monitor screen. The direction (to the left or right) and length (0 to 1023) of the vector to be drawn relative to the beam's current position is determined by DVX0-11 (from the vector generator memory data latches). This data contains information that determines how many clock pulses the counters will receive and whether the counters will count up or down.

DVX0-9 memory data is loaded into rate multipliers J8 and K8. The function of these devices is to space the desired number of counter clock pulses at equal intervals over the time period that it will take to draw the desired vector. This insures that vectors of different lengths will still be displayed with the same relative beam intensity. DVX10 and 11 are loaded directly into the counters. DVX10 determines whether the counters count up or down. DVX11 determines the quadrant of the vector being drawn.

The UNMDACX1 thru UNMDACX10 (X-axis unmultiplexed digital-to-analog converter signals) are transferred and stored at the output of the multiplexers on each rising edge of the 6-MHz clock (from the microcomputer clock circuitry). The DACX1 thru DACX10 signals are sent to the digital-to-analog converters (DACs) in the X video output.

The DACX1 and DACX10 outputs represent the physical placement of the beam on the monitor. The far left of the monitor screen is 0, the center is 512, and the far right is 1023. Therefore, if the DACX1 thru DACX10 signal was greater than 1023, the monitor beam would go off the right side of the screen and start again on the left side of the screen, a "wraparound" condition. To prevent a wraparound, the multiplexers' select input from UNMDACX11 goes high when the count is greater than 1023 or less than 0. This selects UNMDACX12 to be output from the multiplexers to the DACs, forcing all zeros or all ones, and thus keeping the beam on the appropriate side on the screen, instead of allowing it to wraparound.

The XVLD and YVLD (X and Y valid) outputs from the X- and Y-position counter multiplexers are latched (F10) and gated together to enable the Z axis output, BVLD (beam valid).

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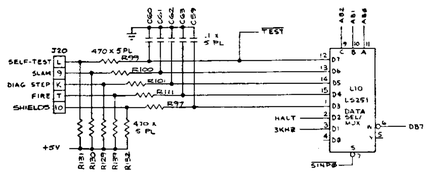
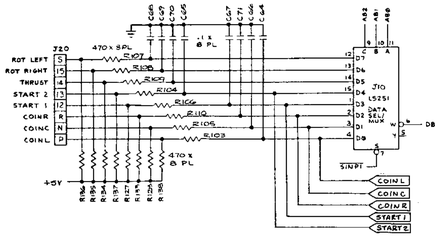
ASTEROIDS DELUXE™
Video Generator
Section of 036471-02 C

Sheet 2, Side A
DP-165-02 2nd printing

INPUTS

PLAYER INPUT CIRCUITRY



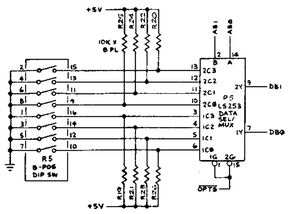


Denotes a test point

DIAG STEP (diagnostic step), 3 KHz, SELF-TEST SLAM, HALT, FIRE, and SHIELDS inputs are read by the MPU when $\overline{\text{SINP0}}$ (switch input zero enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on DB7. Switch inputs are active when pulled to ground. DIAG STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the anti-slam switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

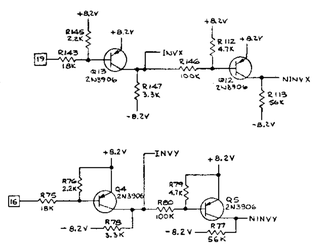
The coin door and some control panel switches are read by the MPU when $\overline{\text{SINP1}}$ (switch input one enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

OPTIONS INPUT CIRCUITRY



The game option switches are read by the MPU when $\overline{\text{OPTS}}$ (option switch enable) is low. Switch toggles to be read are selected by AB0 and AB1 from the MPU. Switch toggles 1, 3, 5 and 7 are read on data line DB0 and toggles 2, 4, 6 and 8 are read on DB1. Toggle inputs are "on" when pulled to ground.

VIDEO INVERTER



The x- and y-video inverter circuits are identical; therefore, only the x-video inverter circuit is explained. For invertered video operation, pin 19 is grounded which turns on transistor Q13 and turns off transistor Q12. In this state INV is + 8.2 VDC and NONINV is -8.2 VDC.

For a noninverted video output, pin 19 is unconnected and floats. In cocktail games, pins 19 and 7 are shorted and have a potential of + 5 VDC. This causes transistor Q13 to be cut off and transistor Q12 to be turned on. INV is then -8.2 VDC and NONINV is approximately + 8.2 VDC.

In upright games, only the x-video inverter is used. In cocktail games both x- and y-video inverters are used, and in cabaret games video inversion is not necessary, so neither is used.

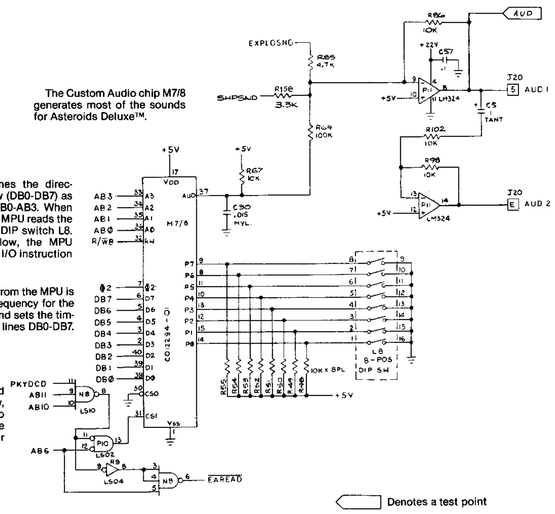
OUTPUTS

The Custom Audio chip M7/8 generates most of the sounds for Asteroids Deluxe™.

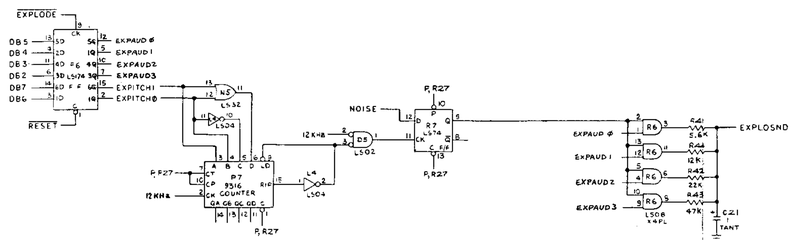
R/$\overline{\text{W}}$ determines the direction of data flow (DB0-DB7) as addressed by AB0-AB3. When R/$\overline{\text{W}}$ is high, the MPU reads the input data from DIP switch L8. When R/$\overline{\text{W}}$ is low, the MPU writes the audio I/O instruction for an output.

The φ2 input from the MPU is the operating frequency for the audio I/O chip and sets the timing for data bus lines DB0-DB7.

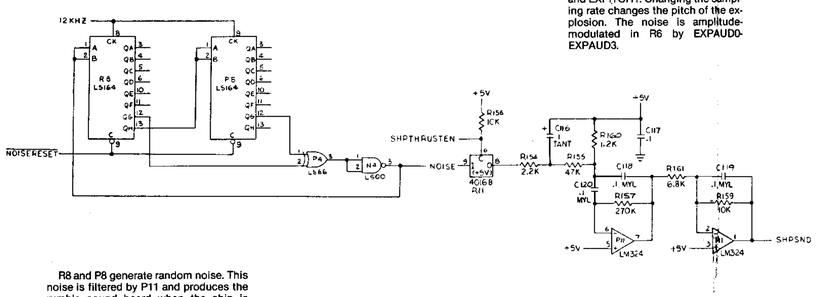
When PKYDCD, AB10, and AB11 are high and AB6 is low, a chip select pulse is gated to the audio I/O chip. This pulse prepares the audio I/O for operation.



Denotes a test point

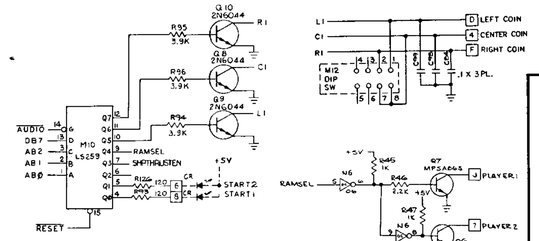


The EXPLODE sound is heard when any object explodes. Noise is sampled at a frequency determined by P7, and control bits EXPITCH0 and EXPITCH1. Changing the sampling rate changes the pitch of the explosion. The noise is amplitude-modulated in R6 by EXPAUD0-EXPAUD3.



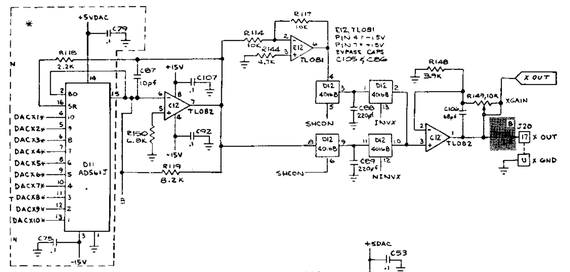
R8 and P8 generate random noise. This noise is filtered by P11 and produces the rumble sound heard when the ship is thrusting.

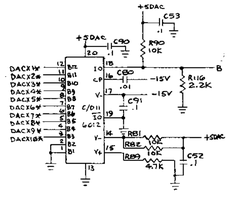
LAMP, LED, AND COIN COUNTER OUTPUT



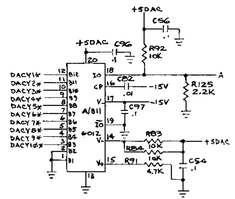
This circuit consists of coin counter drivers Q8, Q9, Q10 and data latch M10, clocked by the microcomputer's address decoder. When the input to a driver is clocked high, its collector goes low, grounding the return of the coin counter in the coin door. When START1 or START2 is clocked low, it grounds the START LEDs in the control panel.

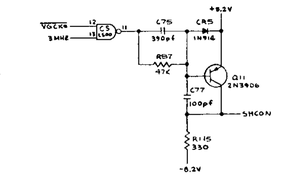
VIDEO OUTPUTS

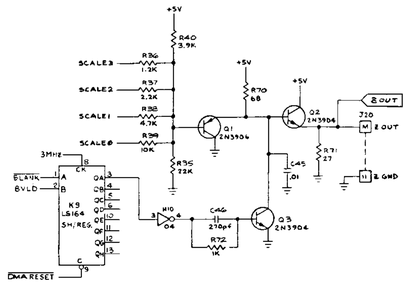


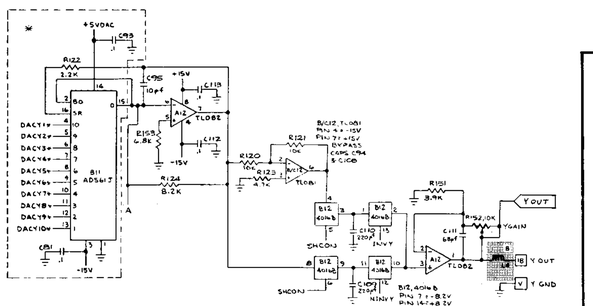


* The circuitry within the dotted lines is optional circuitry for DAC 8012 at positions B11 and D11.









denotes change by indicated revision

Denotes a test point

The video-output circuit consists of three individual circuits: X-axis, Y-axis, and Z-axis. The X-axis and Y-axis video-output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample and holds, and amplifier. The Z-axis video-output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (D11 and B11) each receive binary numbers from the vector generator's position counter outputs. These numbers represent the location of the beam on the monitor. For the non-inverted X axis, the numbers range from 0 to 1023, where 0 is at the far left of the monitor screen, 512 is at the center, and 1023 is at the far right. For the non-inverted Y axis, the numbers range from 128 to 996, where 128 is at the bottom of the monitor screen, 512 is at the center, and 996 is at the top. When the X axis and Y axis are inverted, the monitor picture is turned upside down. This is used for a two-player cocktail game.

The DACs convert these binary number inputs to current outputs. The DACs' current outputs are applied to the pin-6 inputs of current-to-voltage converters C12 and A12.

From the current-to-voltage converters, the signal is fed to two sample-and-hold circuits: One is non-inverted and the other is inverted. The non-inverted sample and hold consists of one stage of analog switch D12 and capacitor C89 for the X axis, and B12 and C109 for the Y axis. The inverting sample and hold consists of inverter E12, one stage of analog switch D12, and capacitor C88 for the X axis and B/C12, B12 and C110 for the Y axis.

The sample-and-hold circuits are controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer clock circuitry and VGCK* from the vector generator's state generator. The result of these inputs insures that the non-inverted and inverted analog signals that are applied to the analog switches have sufficiently stabilized before being applied to the sample-and-hold capacitors.

The output swing of SHCON is −8 to +8 VDC. When SHCON is high, the voltage charges or discharges the sample-and-hold capacitors to the X and Y analog voltage value. The voltages are then applied to the inputs of the second analog switch. These switches select either the non-inverted or inverted X-axis and Y-axis outputs. The outputs are then amplified by the second stages of C12 and A12 for an impedance-matched output to the X and Y inputs to the monitor. Since the monitor doesn't have field-adjustable X and Y gains, the gains are adjustable by variable resistors R120 and R126.

Z Output

The Z-axis video output receives six inputs. BVLD (beam valid), from the output of the vector generator's position counters, tells the Z axis to draw the line. $\overline{\text{BLANK}}$ (vector line blank), from the vector generator's state machine, tells the Z axis to stop drawing a line. SCALE0 thru SCALE3 (grey-level shading scale), from the output of the vector generator's data latch, tells the Z axis the grey-level shading of the line that is being drawn on the monitor.

When BVLD and $\overline{\text{BLANK}}$ are both high, a high is clocked through shift register K9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When $\overline{\text{BLANK}}$ goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determine Q1's emitter voltage, during the line draw period. The SCALE0 thru SCALE3 resistors R36 thru R39, resistor R35, and resistor R40 result in a range of about + 1.0 VDC when all are low and + 4.0 VDC when all are high. The emitter of Q1 follows at about + 1.7 to 4.7 VDC, while the emitter of transistor Q2 follows at about + 1.0 to 4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.

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Sheet 2, Side B

ASTEROIDS DELUXE™
Switch Inputs, Coin Counter, LED and Audio Outputs