PROM PROGRAMMER
Program Card Set
909/919-1183-1

025-1183-1 REV J OCT 81

FOREWORD

Before attempting to use the 909-1183-1 Program Card Set in a Data I/O Model 1 or 2, read the following.

1. **Power Supply.** The power supply must be either the Data I/O 702-1087 linear power supply assembly, or, in the case of the older, 4-card power supply, a 701-1041 Rev. A "Programmable Power Supply" card must be present in the power supply.

2. **Control Card.** If the programmer has a 201-24811 control card, a modification is required. With insulated wire, connect card edge fingers 22 and 27.

   No modification is required in the event your programmer is equipped with a 701-1083 control card.

   After power-up with the MOS cardset installed, the calibration of the high voltage power supply must be checked. With the common lead of a DVM connected to card edge pin 29, pin 31 should read between 49.2 and 49.5 V.

   If you require any additional information or programmer updating services, please contact your nearest Data I/O Service Representative.

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SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
ADVANCED MICRO DEVICES				
256x8 MOS	1702/ AM9702	VOL TS	24 PIN	1047
256x8 MOS	1702A/ AM9702A	VOH TS	24 PIN	1047
INTEL				
256x8 MOS	1702A/ 4702A/ 8702A	VOH TS	24 PIN	1047
MITSUBISHI				
256x8 MOS	58563S (1702A)	VOH TS	24 PIN	1047
MOSTEK				
256x8 MOS	3702 (1702A)	VOH TS	24 PIN	1047
NATIONAL SEMICONDUCTOR				
256x8 MOS	1702A	VOH TS	24 PIN	1047

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences and shapes of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909-part number. See Figure 1-1 b).

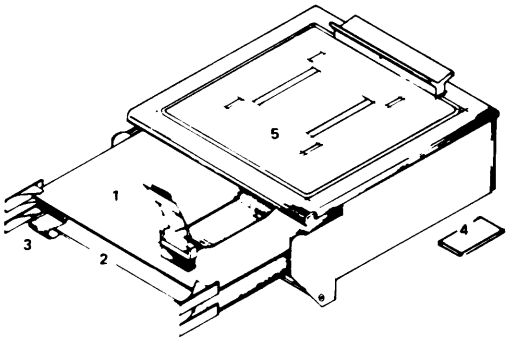
1.2 PROGRAMMING ALGORITHM

An intelligent programming scheme is used in the MOS digital card to provide an equation (x + Ax) that determines the level of normal program acceptance for verification of data. The digital card keeps track of the number of program pulses or amount of energy that was required to attain the basic verification of data. At that time, an overprogram sequence is initiated which allows a fixed amount of energy to be programmed into the device at each word count to deeply program the data into the MOS memory cells. Following the overprogram sequence, normal digital verification occurs.

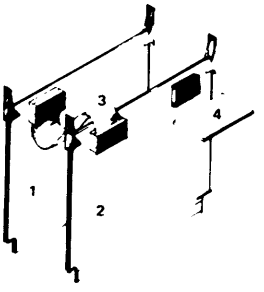
1.3 CALIBRATOR PROGRAM ADAPTER

The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1-9 Programmers

1. DIGITAL CARD 701-1173
2. ANALOG CARD 701-1183-1
3. INTERCONNECT CABLE 709-1608
4. CALIB. PROGRAM ADAPTER 910-1182-1
5. PROGRAMMING PAK CARRIER 940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

1.4 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable-jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

Table 2-1. Customer-Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP2	Word Limit	256	Selection defaults to socket adapter

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 and 2 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

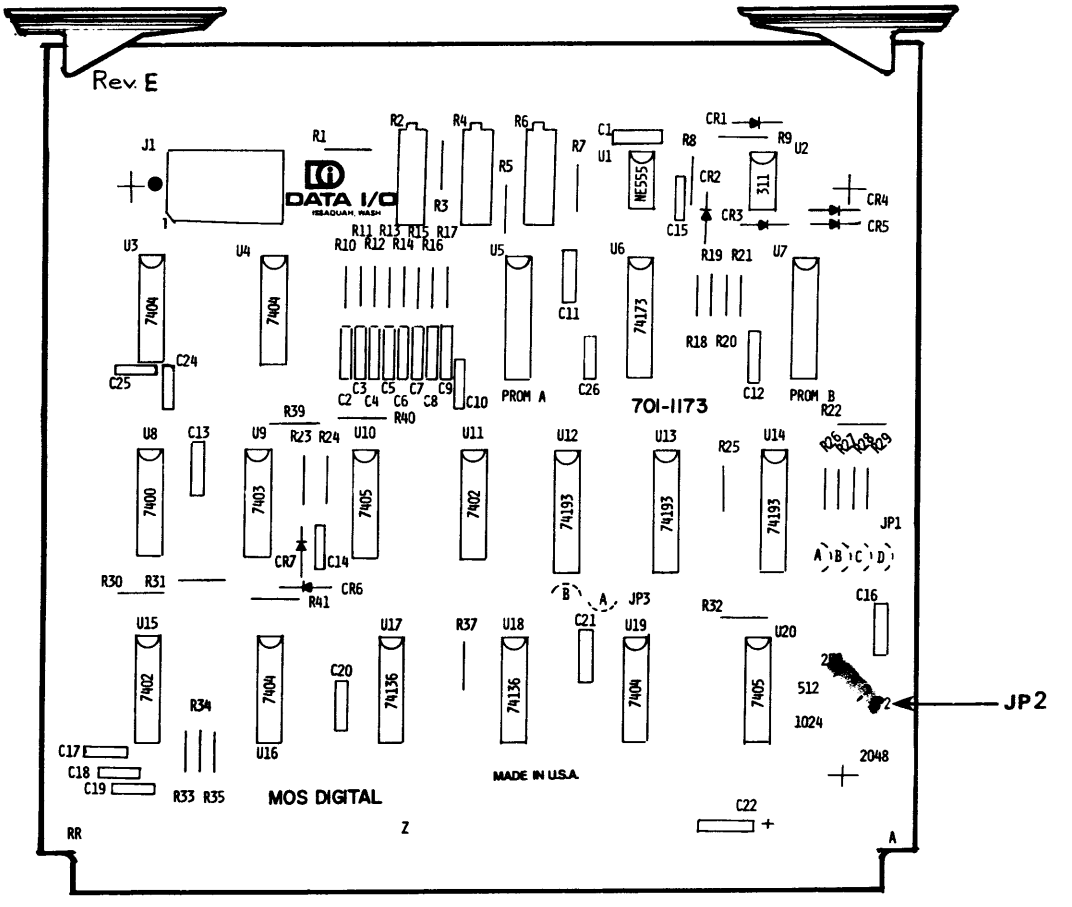


Figure 2-1. Digital Card Jumper Locations

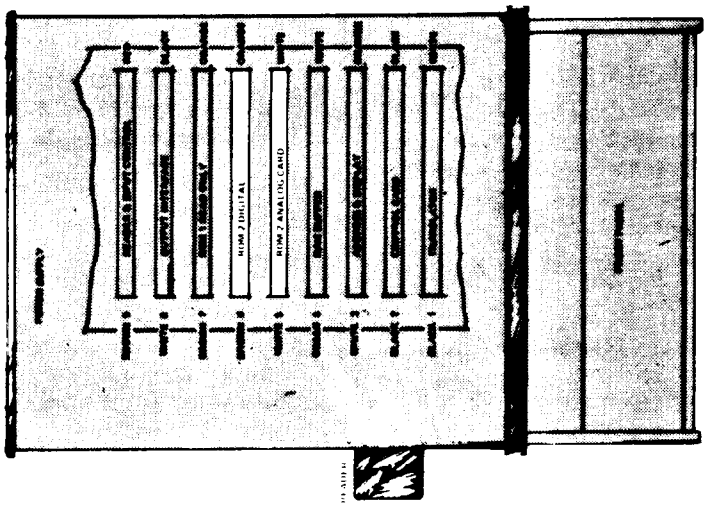


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

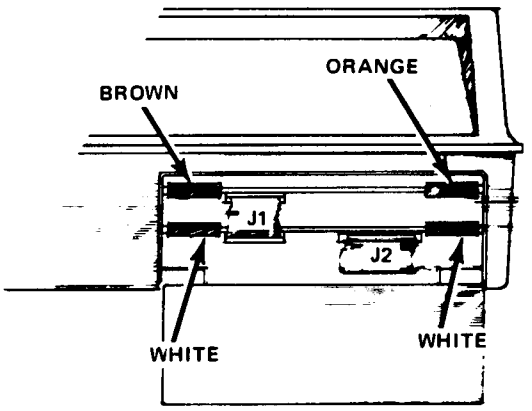


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

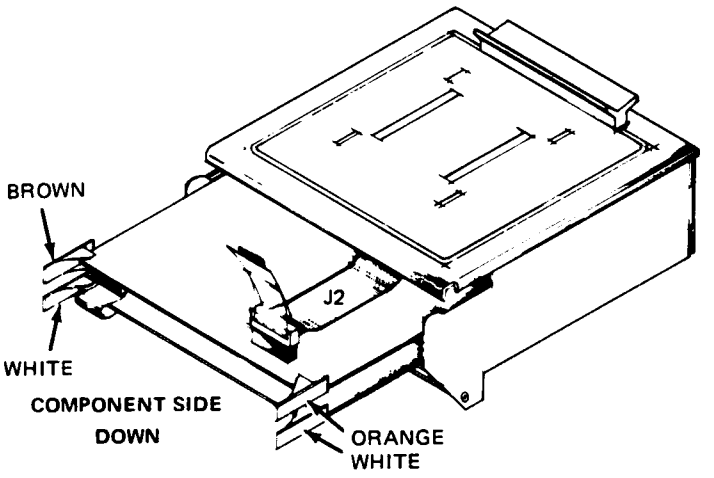


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

3.1 DUTY CYCLE JUMPER

JP1, located on the left side of the analog card shown in Figure 3-1, determines the program waveform duty cycle. 1702 PROMs are programmed with JP1 in position "A" (2% duty cycle); 1702A PROMs are programmed with JP1 in position "B" (20% duty cycle).

3.2 SHORT AND REVERSE DETECTION

If a PROM is plugged in backwards or if it contains an internal short, program card set 909-1183-1 automatically signals a reset and causes the programmer to Stop.

3.3 INTELLIGENT PROGRAMMING

The number (n) of program pulses applied to a PROM word is a function of the number of pulses required to program the word (x) times a multiplier A, according to the equation,

$$n = x + A(x+1) - 1$$

On the 909-1183-1 program card set A is set at 4 by JP1 on the digital card.

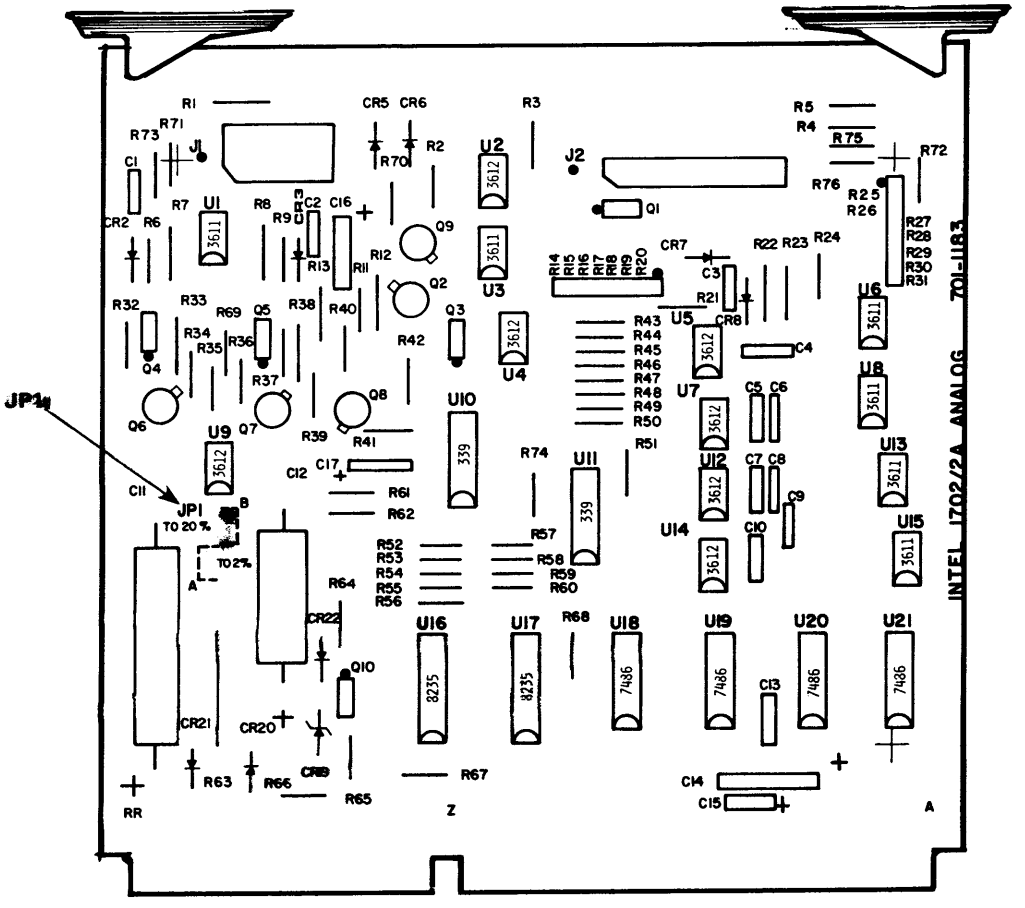


Figure 3-1. Analog Card Duty Cycle Jumper.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

a. Data I/O Universal Calibrator, P/N 910-1071

b. Calibration Extender:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1521

c. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.

d. A potentiometer adjustment tool

e. Dual-trace oscilloscope — Tektronix 465 or equivalent

f. A jumper wire approximately 12 inches in length

g. Data I/O interconnection cables:

Models 1-5	P/N 709-1613
Model 9	P/N 709-2608, 709-1613
System 19	P/N 709-2612, 709-1613

h. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1-5

Refer to Figure 4-1.

a. Make sure the programmer power is OFF.

b. Remove the cover from the programmer and remove the Program Card Set from the card cage.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

d. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

Figure 4-1. Set-up of Models 1-5 for DC Calibration.

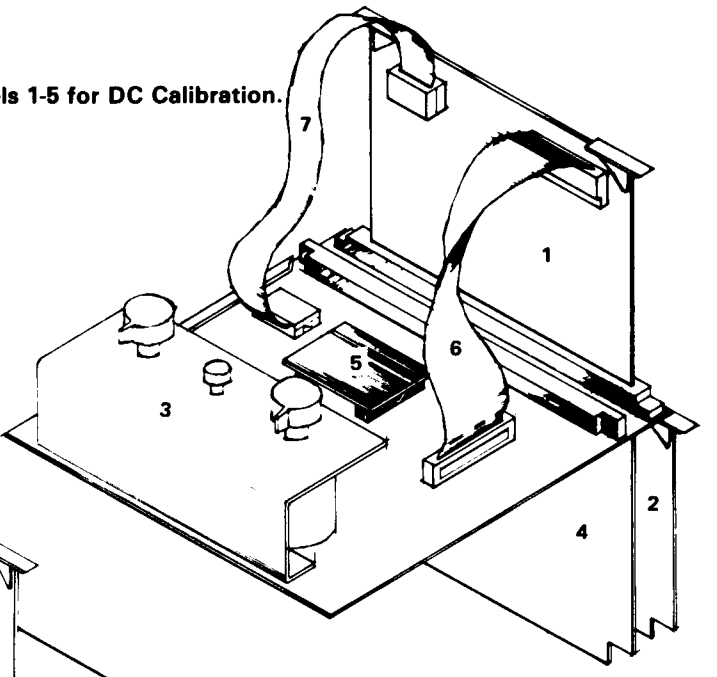
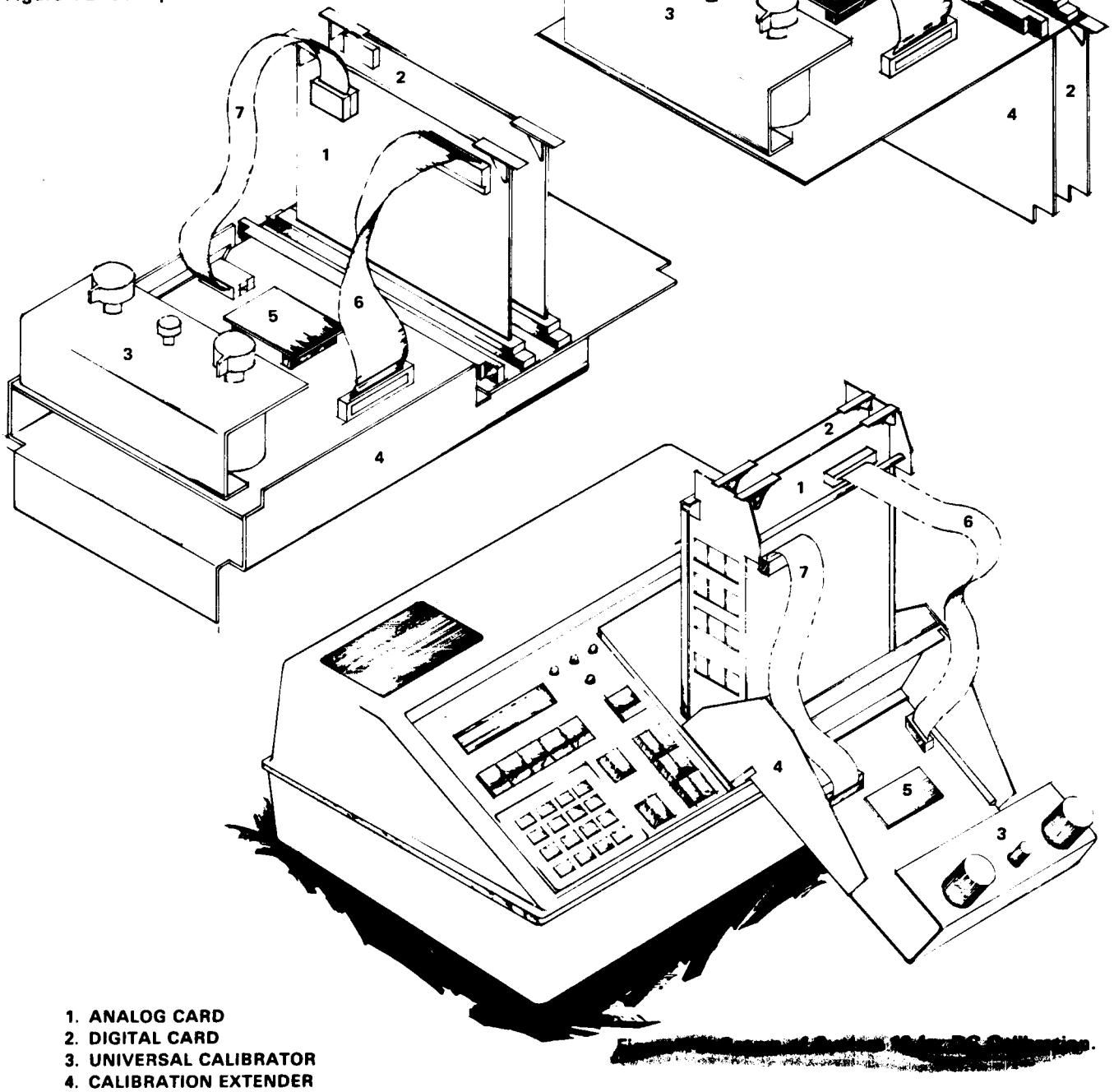


Figure 4-2. Set-up of Model 9 for DC Calibration.



1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATION EXTENDER
5. CALIBRATOR PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

4.2.2 MODEL 9

Refer to Figure 4-2.

a. Make sure the programmer power is OFF.

b. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

d. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's digital card position (brown/orange). Be sure that the edge of the Extender Card is securely seated. Install the Digital and Analog cards into the 1074 calibration extender according to Figure 4-2.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

KEYBOARD
EXECUTE
NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

a. Make sure the programmer power is OFF.

b. Remove the Programming Pak from the programmer.

c. Insert the Calibration Extender, P/N 910-1521, in the same way as the Programming Pak, being sure to seat it properly in the programmer's mating connector.

d. With the handle of the Programming Pak down, connect the 64-pin connectors of the Programming Pak and Calibration Extender. Be sure the connectors mate securely.

e. Slide the Universal Calibrator securely into the card slots at the front of the Calibration Extender.

f. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe with the connector dot.

g. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe with the connector dot.

h. Plug the Calibrator Program Adapter into the Program Adapter slot on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 919-XXXX part number of the Programming Pak.

i. Connect the DVM ground lead to GND test point on the Universal Calibrator.

j. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

SELECT
C1 (calibrate ON)
START

k. Press:

KEYBD
ENTER

The TEST light comes ON and remains ON throughout calibration.

NOTE

To exit calibration, press:
SELECT
CØ (calibrate OFF)
START
(Test light goes OFF.)

l. Press START.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

- The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond ØØØ for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

- The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance.

- The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer.

- The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the Calibration Chart may require changing of switch positions. With the proper S2 and S3 positions selected press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

- The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

- The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

- The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4.3.1 — 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 — 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1183-1
FIXTURE 702-1071
PROGRAM ADAPTER 910-1183-1
PROGRAM CARD 909-1183-1
MANUFACTURER AMD, INTEL, NATIONAL, MOSTEK
PROM 1702, 1702A/4702A/8702A AM 9702

DATE	REV	REVISION RECORD	DR	CK
2-80	D	ECN #3403	EF	VEB
6-6-80	D	ECN #3671	KJB	VEB
2-27-81	D	ECN #4009	EF	CRR
9-25-81	D	ECN #4312	EF	
3-1-82	D	ECN #4492	KB	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U4	U5	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
07	40	+24	1-1	000	00	000			+24	R26	23.5	24.5	24.5
07	40	Power +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8
07	40	Supply + 5	1-3	000	00	000			+ 5	R18	5.05	5.1	5.15
07	40	- 9	1-4	000	00	000			- 9	R40	-9.2	-9.0	-8.8
07	40	Programmable Supply	1-5	000	00	000			PROGV		14.2		15.2
06	40	VCC Program ①	2-1	001	01	001	2	24	TP3		47.0		49.0
07	40	VCC Verify	2-3	002	02	002	3	3			13.3		14.7
05	40	VBB Program ②	2-4	003	03	003	2	10			57.8		62.2
07	40	VBB Verify	2-6	004	04	004	3	10			13.3		14.7
07	40	VDD Program	2-7	005	05	005	8	1			0.0		0.4
07	40	VDD Current, IDD Limit	2-8	005	05	005	9	1			0.0		2.0
06	40	VGG Program ④	2-9	006	06	006	7	9			6.0		13.0
47	40	VGG Verify	2-10	007	07	007	7	9			0.0		0.4
27	40	CE Program ③	3-1	008	08	010	7	11			13.3		14.7
07	40	CE Verify	3-2	009	09	011	7	11			0.0		0.3
07	40	Reference Level	4-1	009	09	011	7	U11P8			11.5		12.8
07	C0	Bit 8 Program	5-2	010	0A	012	7	23			13.3		14.7
07	C0	Bit 7 No Program	5-3	010	0A	012	7	22			0.0		0.3
07	C0	Bit 6 Program	5-4	010	0A	012	7	21			13.3		14.7
07	C0	Bit 5 No Program	5-5	010	0A	012	7	20			0.0		0.3
07	C0	Bit 4 Program	5-6	010	0A	012	7	19			13.3		14.7
07	C0	Bit 3 No Program	5-7	010	0A	012	7	18			0.0		0.3
07	C0	Bit 2 Program	5-8	010	0A	012	7	17			13.3		14.7
07	C0	Bit 1 No Program	5-9	010	0A	012	7	16			0.0		0.3
07	C0	Bit 8 No Program	5-11	010	0A	012	7	23			0.0		0.3
07	C0	Bit 7 Program	5-12	010	0A	012	7	22			13.3		14.7
07	C0	Bit 6 No Program	5-13	010	0A	012	7	21			0.0		0.3
07	C0	Bit 5 Program	5-14	010	0A	012	7	20			13.3		14.7
07	C0	Bit 4 No Program	5-15	010	0A	012	7	19			0.0		0.3

COMMENTS

Switch S1 must be depressed for accurate readings.
CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

Adjustments are located on the power supply board. See programmer manual.

CAUTION: See Note 1.

CAUTION: See Note 1.

Test point located on analog card.

	Model 1-5	9	19	
LOAD	Bits 1,3,5,7,ON	55	AA	DI Bus
Confirm	Bits 2,4,6,8,ON	AA	AA	DO Bus
LOAD	Bits 2,4,6,8,ON	AA	55	DI Bus
Confirm	Bits 1,3,5,7,ON	55	55	DO Bus

CALIBRATION CHART 017-1183-1

PAGE 2 OF 2

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U4	U5	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
07	C0	Bit 3 Program	5-16	010	0A	012	7	18	3		13.3		14.7
07	C0	Bit 2 No Program (7)	5-17	010	0A	012	7	17	3		0.0		0.3
07	C0	Bit 1 Program (6)	5-18	010	0A	012	7	16	3		13.3		14.7
83	C0	Data Disable	5-20	011	0B	013	7	23	3		13.3		14.7
87	40	Program Line Program (5)	5-21	012	0C	014	7	12	3		0.0		0.3
17	40	Program Line Verify	5-22	013	0D	015	7	12	3		13.3		14.7
07	C0	Address Test VIL (8)	7-1	170	AA	252	7	15	3		0.0		0.3
07	C0	Address Test VIH	7-2	170	AA	252	7	14	3		13.3		14.7
07	C0	Address Test VIL	7-3	170	AA	252	7	13	3		0.0		0.3
07	C0	Address Test VIH	7-4	170	AA	252	7	4	3		13.3		14.7
07	C0	Address Test VIL	7-5	170	AA	252	7	5	3		0.0		0.3
07	C0	Address Test VIH	7-6	170	AA	252	7	6	3		13.3		14.7
07	C0	Address Test VIL	7-7	170	AA	252	7	7	3		0.0		0.3
07	C0	Address Test VIH	7-8	170	AA	252	7	8	3		13.3		14.7
87	40	Address Test VIH (8)	7-9	172	AC	254	7	15	3		13.3		14.7
83	C0	Address Test VIL	7-10	171	AB	253	7	14	3		0.0		0.3
83	C0	Address Test VIH	7-11	171	AB	253	7	13	3		13.3		14.7
83	C0	Address Test VIL	7-12	171	AB	253	7	4	3		0.0		0.3
83	C0	Address Test VIH	7-13	171	AB	253	7	5	3		13.3		14.7
83	C0	Address Test VIL	7-14	171	AB	253	7	6	3		0.0		0.3
83	C0	Address Test VIH	7-15	171	AB	253	7	7	3		13.3		14.7
83	C0	Address Test VIL	7-16	171	AB	253	7	8	3		0.0		0.3
07	41	Abort Test	8-1	28	1C	034							
07	42	Interactive Test	8-2	29	1D	035							
07	42	Interactive Test	8-3	30	1E	036							
07	07	Duty Cycle Test	8-4	31	1F	037							
07	40	Data Pattern for All Words Not Shown											

For detailed instructions refer to Instruction Manual.

	Model 1-5	9	19	
LOAD	Bits 2,4,6,8 ON	AA	55	DI Bus
Confirm	Bits 1,3,5,7,ON	55	55	DO Bus
Confirm	All Bits ON	FF	FF	DO Bus

U3 CAL ADAPTERS	
Words	Data
0-47	B
48-62	9
63	A
64-79	B
80-84	9
85	d
86-91	9
92	A
93-95	9
96-111	B
112	A
113-127	9
128-255	F

Notes: 1. Do not leave Programmer at this word count longer than required to obtain measurement.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5: Observe the START and STOP indicators.

Model 9: Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.

System 19: Observe the START light. If the START light is on, the programmer is in START.

4.3.2 SET THE STATE OF THE START/STOP LINE

Models 1, 2, 3 and 5: Press the START/STOP key.

Model 9:
a. Press KEYBOARD to stop.
b. Press EXECUTE to start.

System 19:
a. To set the programmer in START, press KEYBD, ENTER and START.
b. To set programmer in STOP, press KEYBD.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5: Press the FWD key or the REV key.

Model 9: See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.

Revision "A" Software: Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:

a. Ground J1-16 on the analog card.
b. Press LOAD.
c. Press EXECUTE.
d. Press KEYBOARD.
e. Key in data — Ø hex — at address ØØ1.
f. Press VERIFY.
g. Press EXECUTE. The programmer will mis-verify at the address containing data and will STOP in FWD.
h. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD. Press ENTER and then REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the Calibration Chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.)

Revision "A" Software

Halt the programmer in the automatic program mode with data on the DI bus.

a. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.

b. Press the KEYBOARD key, and key in the Model 9 hex data called out on the Calibration Chart.

c. Press the PROGRAM key.

d. Ground J1-16 on the analog card.

e. Press EXECUTE and wait for the programmer to abort.

f. Press STOP, KEYBOARD and EXECUTE.

g. Disconnect J1-16 from ground.

h. SET the address specified on the Calibration Chart in order to make the measurement.

Revision "B" or later Software:

With the EXECUTE indicator illuminated and all the others OFF, use the hex keypad to key in the Model 9 hex data called out on the Calibration Chart.

System 19:

a. Press KEYBD, key in the address and press ENTER.

b. Key the System 19 hex data into RAM at the specified address.

c. Press ENTER and then REVIEW.

4.3.5 CONFIRM DATA ON THE DO BUS

Models 1, 2, 3 and 5:

Compare the bit callout on the Calibration Chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF.

Model 9:

With the EXECUTE light ON, press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the Calibration Chart.

System 19:

With KEYBD selected, press the DEVICE DATA key. Hold it down while reading the hex data. The programmer must be in START.

4.3.6 INTERACTIVE-FUNCTION TESTS

This MOS Program Card Set uses interactive programming techniques. This means that pulse duty-cycles are controlled by PROM temperature, and the overprogram pulse train lengths are proportional to the number of pulses required to initially program particular PROM words.

Test the interactive functions of the digital card following the analog card tests on the calibration chart, and before making the waveform observations. If a failure is indicated in any test, DO NOT use the card set for programming. The following instructions assume that the programmer is properly set-up for calibration as described in subsection 4.2.

Set-up

1. Turn programmer power OFF.

2. Disconnect the 16-conductor cable from J1 on the analog card and the 26-conductor cable from J2 on the Universal Calibrator.

3. Remove the analog card from the Universal Calibrator, with the 26-conductor cable attached, from the Universal Calibrator and set it aside.

4. Models 1-5 only: Insert the digital card, component-side forward, into the card slot on the calibrator assembly.

5. Models 1-5 only: Install the calibrator assembly into the digital card position (front brown/orange) in the card cage.

6. Connect the free end of the 16-conductor cable to digital card J1 with the red stripe to pin 1. The other end of the cable remains in J1 of the Universal Calibrator.

7. Refer to the Calibrator Program Adapter installed in the Universal Calibrator. If the circuit board, 702-1073, is of Revision "E" or later, install JP1 and JP2 to position "A".

8. Turn programmer power ON.

9. Models 1-5: Press RESET
ROM2-ROM2
PROGRAM
MANUAL
START

Model 9: Press KEYBOARD

System 19: Press SELECT
C1
START

Abort Test

1. Advance to address 1C (hex), 28 (dec), or 34 (oct).

Model 5: Press FWD repeatedly until the proper address is reached.
Press STOP
START

Model 9: Press FWD repeatedly until the proper address is reached.

System 19: Press KEYBD
1C
ENTER

2. Load bit 1 ON (hex Ø1) to the DI bus (RAM) at address 1C.

Models 1-5: Press 1

Model 9: Press Ø1
FWD
REV

System 19: Press Ø1
ENTER
REVIEW

3. Initiate a programming sequence.

Models 1-5: Press FWD

Model 9: See MODEL 9 USER'S NOTE in subsection 4.3 to determine the proper revision level of your unit.

Revision "A" software: Press
PROGRAM
EXECUTE

Revision "B" or later software: Press
EXECUTE
Hold SET; Press FWD

System 19: Press PROG
START

4. Confirm that the PASS indicator on the Calibrator Program Adapter is ON, and that the programmer is at address 1C. Also:

Models 1-5: The data A and B lights should be OFF

Model 9: The P indicator should be blinking.

System 19: The display should flash.

Interactive-Function Test

1. Models 1-5: Press STOP
START

Model 9: Press STOP
KEYBOARD

System 19: Press KEYBD
ENTER

2. Load all bits OFF (hex ØØ) at address 1C.

3. Advance the programmer to address 1D (hex), 29 (dec), or 35 (oct).

Models 1-5: Press FWD

Model 9: Press FWD

System 19: Press ENTER

4. Load bit 1 ON (hex Ø1) to the DI bus (RAM) at address 1D.

Models 1-5: Press 1.

Model 9: Press Ø1
FWD
REV

System 19: Press Ø1
ENTER
REVIEW

5. Initiate a programming sequence.

Models 1-5: Press FWD

Model 9, with Revision "A" software: Press
PROGRAM
EXECUTE

Model 9, with Revision "B" or later software: Press
EXECUTE
Hold SET; Press FWD

System 19: Press PROG
START

6. Confirm that the PASS indicator is on, with the programmer at the correct address, shown below.

Models 1-5: 1E (hex), 30 (dec), or 36 (oct).

Model 9, Revision "A" software: 1D, with the "V" indicator blinking.

Model 9, Revision "B" or later software:
1E

System 19: 1E

Duty-Cycle Test

1. Models 1-5: Press STOP
START

Model 9: Press STOP
KEYBOARD

System 19: Press KEYBD
ENTER

2. Return to address 1D and load all bits OFF (hex 00).

Models 1-5: Press REV
00

Model 9, Revision "A" software: Press
00

Model 9, Revision "B" or later software: Press
REV
00

System 19: Press REVIEW
00

3. Advance to address 1F (hex), 31 (dec) or 37 (oct).

Models 1-5: Press FWD twice

Model 9: Press FWD twice

System 19: Press ENTER twice

4. Load bit 1 ON (hex 01) to the DI bus (RAM) at address 1D.

Models 1-5: Press 1

Model 9: Press 01
FWD
REV

System 19: Press 01
ENTER
REVIEW

5. Initiate a programming sequence.

Models 1-5: Press FWD

Model 9, Revision "A" software: Press
PROGRAM
EXECUTE

Model 9, Revision "B" or later software: Press
EXECUTE
Hold SET; Press FWD

System 19: Press PROG
START

6. Confirm that the PASS indicator is on, with the programmer at address 1F. Model 9 will not display an address.)

Conclusion

This completes the DC tests of the Program Card Set. If PASS is indicated in all three interactive tests, proceed to the Waveform Observation instructions, subsection 4.4. Replace the analog card and set up the equipment as shown in Figure 4-5.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the Timing Diagram, have the same reference on the Calibration Chart. Waveforms are selected using Universal Calibrator switches S2 and S3 as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

a. Make sure that the programmer power is OFF.

b. Make sure that analog card jumper JP1 is in position A (see Figure 3-1)

c. Remove the digital card from the card slot.

d. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

e. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.

f. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point (top of R25).

g. Reinstall the digital card in the slot from which it was removed.

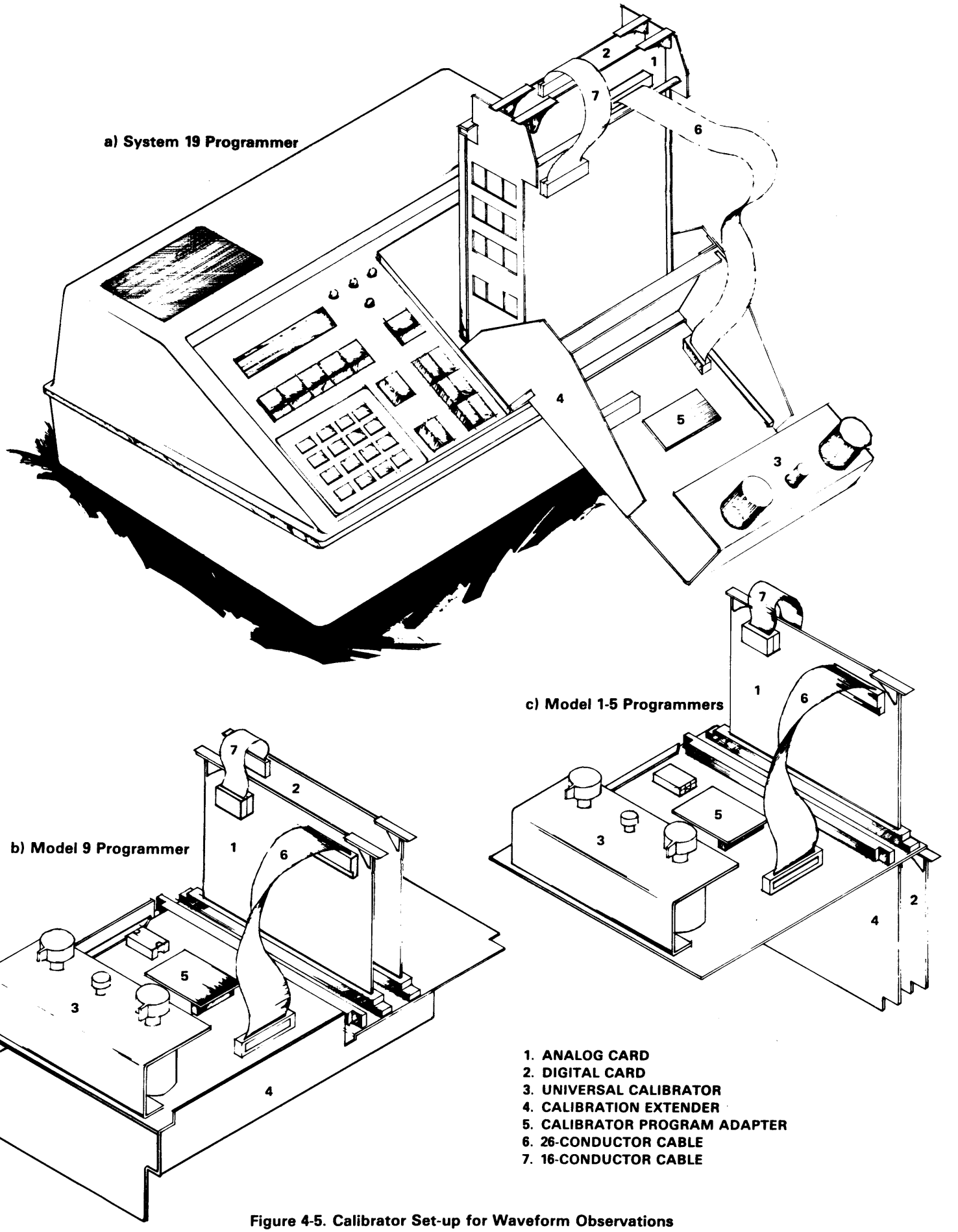


Figure 4-5. Calibrator Set-up for Waveform Observations

h. Ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1 — 5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL. Press KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresses:

Models 1 — 5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.
Model 9:	Enter hex data "Ø1" at several addresses.
System 19:	Enter hex data "Ø1" at several addresses. Return to address Ø.

4. Select the PROGRAM mode:

Models 1 — 5, press:	RESET PROGRAM AUTO RAM-ROM2
Model 9, press:	PROGRAM
System 19, press:	SELECT C1 START PROG

5. Initiate waveforms:

Models 1 — 5, press:	START
Model 9, press:	EXECUTE
System 19, press:	START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the Timing Diagram and Calibration Chart by the circled digits (1 , 2 , 3 , ...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the Calibration Chart is of no importance during waveform observation.

CAUTION

When S1 is depressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1 — 5 and 9, press:	STOP
System 19, press	KEYBD

NOTE

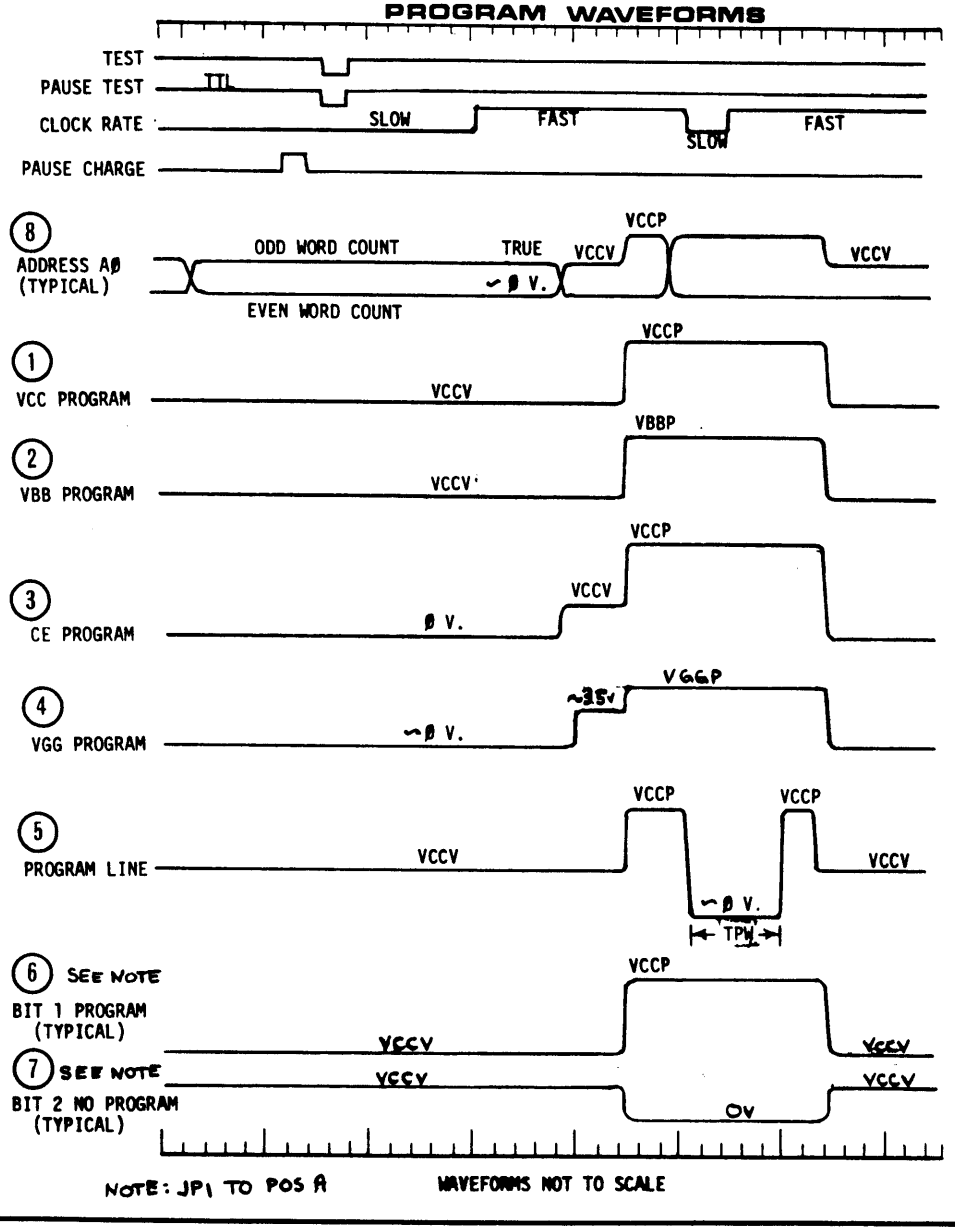
The digital card has one or more potentiometers for calibrating various timing functions of the card set. In normal usage, the card set will rarely need to have these functions re-calibrated.

However, in the event that the card set waveforms do not conform to the specifications of the Timing Diagram contact your nearest Data I/O Service Representative for calibration information.

1-78 CN #1920
1-79 CN #2594

	DATE	SYM	REVISION RECORD	DR.	CK.
FS T	-75	A	RELEASE		
10	-75	B	CN #339		
2	-76	C	CN #515	VB	
	7-77	–	ECR 1576		
	7-77	–	ECR 2076		

PROGRAM WAVEFORMS



NOTE: JP1 TO POS A WAVEFORMS NOT TO SCALE

NOTES

1173 DIGITAL JUMPERS

JP1	A, B, D	SHORT	A=4
JP1	C	OPEN	A=4
JP2	256 (Word Limit)		
JP3	A	SHORT	Reject at 256
JP3	B	OPEN	Reject at 256

1183 ANALOG CARD JUMPERS

JP1 B=1702A = 20% Duty
JP1 A=1702 = 2% Duty

WAVEFORM VARIABLES

VCCP = + 47.0 TO +49.0 VOLTS
VCCV = + 13.3 TO +14.7 VOLTS
VGGP = +6.0 TO +13.0 VOLTS
VBBP = 60 ± 1.5 VOLTS
TPW = 2.0 ± 0.1 MSEC

ABORT IS SET AT 256 PULSES

1702A TIME ON APPROX. 3 SEC
1702 TIME ON APPROX. 30SEC

INTELLIGENT PROGRAMMING EQUATION:

N = X + A(X+1) -1
N = TOTAL NUMBER PULSES
A = MULTIPLIER = 4
X ≤ 256

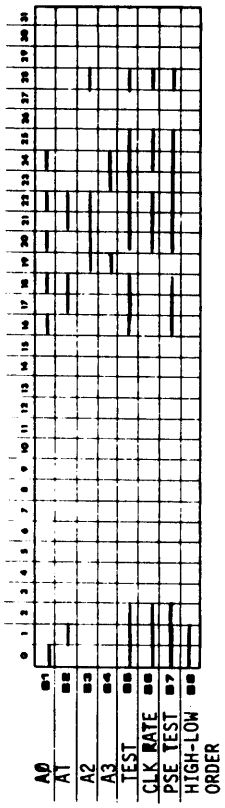
CARD SET POLARITY IS JUMPER-SELECTABLE (JP1 ON THE ANALOG CARD). FOR CALIBRATION, GROUND DIGITAL CARD J1 PIN 16.

These waveforms correspond to call-outs on Calibration Chart 017-1183-1. Switch S2 and S3 of Universal Calibrator to indicated positions to obtain waveforms. Refer to dynamic test instructions in performance check section for detailed instructions.

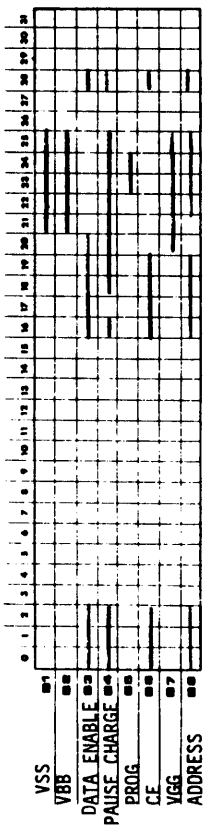
TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

LOGIC ROM U7



TIMING ROM U5



DATA I/O ISSAQUAH, WASH.

DRAWN BY
APPROVED BY

TITLE
1702/1702A TIMING DIAGRAM

DATE 6/21/76

DRAWING NUMBER 007-1183-1

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual — refer to these for pin-out and interconnection information.

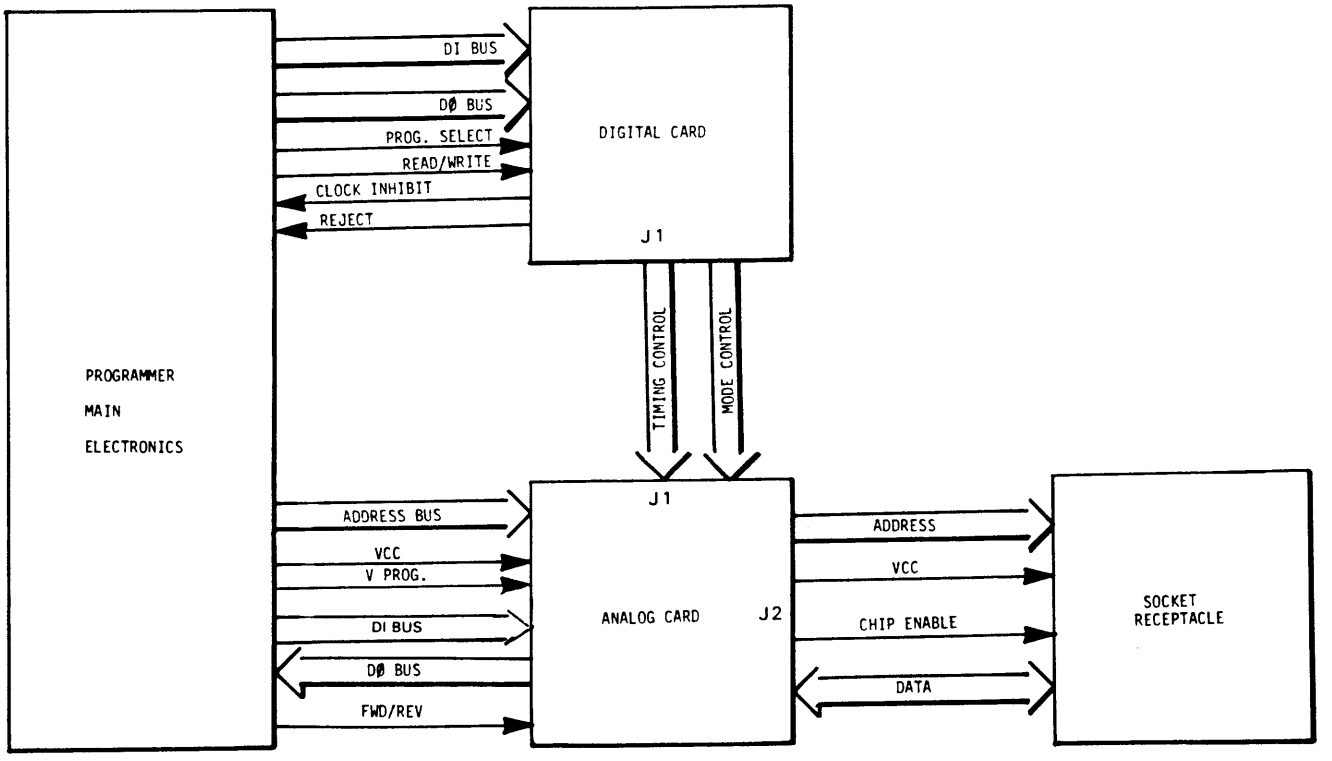


Figure 5-1. Simplified Block Diagram of Program Card Set.

5.2 DIGITAL CARD

The MOS Digital Card 701-1173 is a general purpose control system which is used in conjunction with analog cards of different configurations to program MOS PROMs. Figure 5-2 is a generalized block diagram of the digital card. The diagram shows signal flow and functional relationships between the blocks but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.1 SELECTION GATES

Refer to the Schematic Diagram 008-1173. Input signals arrive on the control lines on the left side of the drawing. Data Input and Output signals are on the top of the drawing. The interface connector to the analog card, labeled J1, is on the right side of the drawing.

In order to select the card set for programming, the Program line (pin LL) must be low, and the Write Inhibit Line (pin PP) must also be low. As the Write Inhibit line is driven low, Input Select gate U15 Pin 1 becomes high, provided word limit has not been reached. This line becoming high enables the Verify A and B lines. The Input Select gate also enables the Write Select gate U8 which, along with a high on pin 4, signals a Write condition.

5.2.2 CLOCK

During the programming sequence, the programmer issues a low-going Write pulse to pin AA. As this line becomes low, the output of the Write Select gate (U15) becomes high, which enables the Write Enable gate (U8). Prior to this, the Stop line became high. The Start condition allows the system to pass through a power-up cycle which enables the Power On gate to release the Clear clamp on the Program Register (U6). When clear is released, NOR gate U15 pin 13 goes low, allowing pin 8 of inverter U10 to become High, thus turning on the Clock Timer (U1).

The Timer output provides a pulse into the clock input of the Program Register whose data inputs arrive from ROM U7, signaling the next position to be addressed. The Program Register will be commanded to jump to any location that the ROM signals.

The start-up procedure allows power to be applied to the MOS device. The Program Register commands the

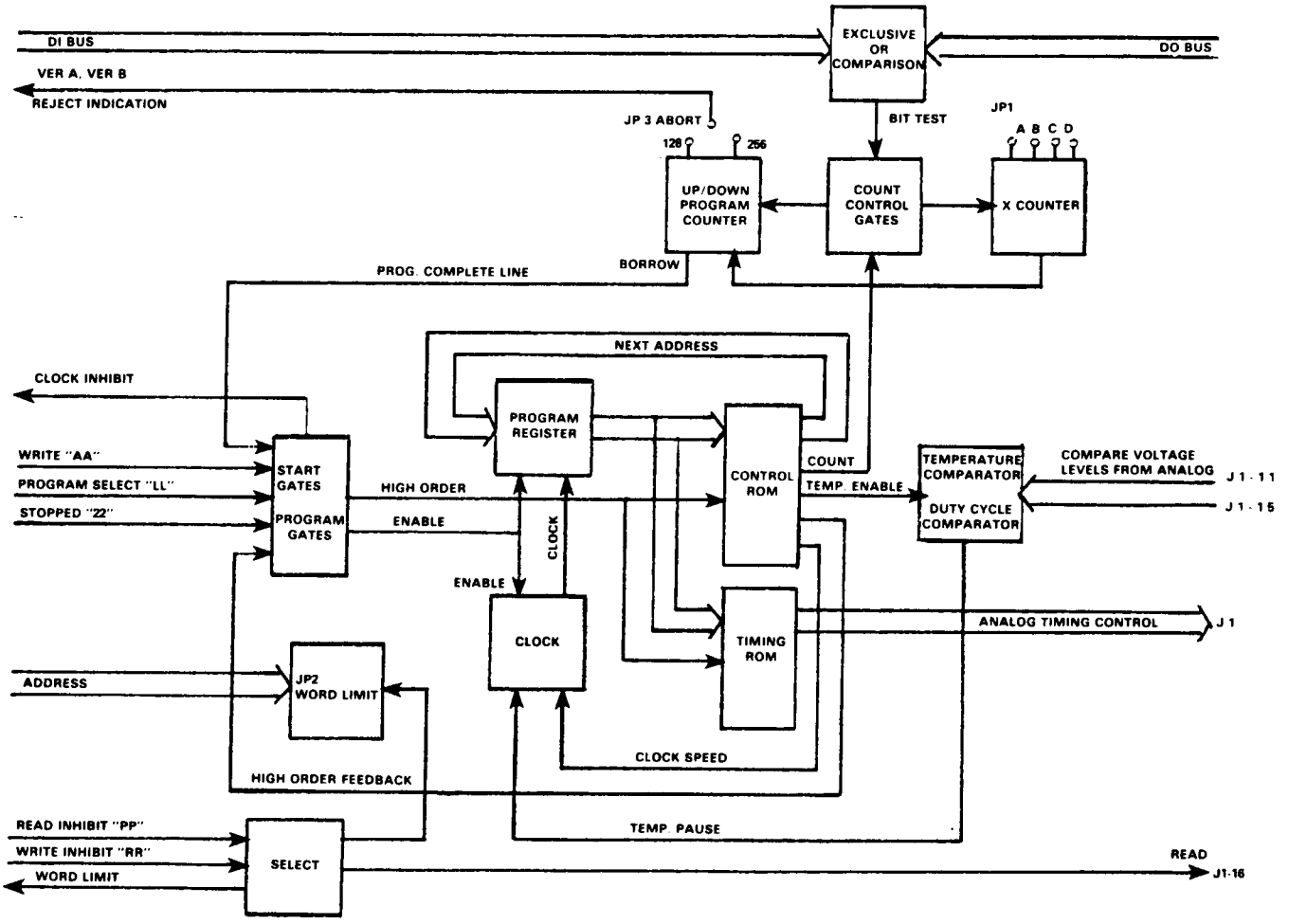


Figure 5-2. Block Diagram, 1173 Digital Card.

Logic ROM to jump from 0 to 1 to 2 and then to 16. As the jump arrives at 16, bit 8 of the logic ROM (pin 9) becomes low making pin 14 of U7 high, which causes a sector jump. The low on pin 9 also falsifies the Power ON gate (U8) so that the system returns to a clamp state with the Clock OFF and the Chip Enable on the Logic ROM (pin 15) low.

5.2.3 JUMP CONTROL SYSTEM

Logic ROM Pins 1, 2, 3 and 4 comprise a 4 bit binary counter whose output is presented to the input of the Program Register. The Program Register is a D-type latch whose output follows the input when clocked. Therefore, as the input is told to move to a certain location, the output moves to that location when clocked, addressing the ROM for the next location desired at the next clock pulse.

5.2.4 TIMING ROM

A second ROM (U5) follows the Logic ROM on its input addresses, and has eight output lines which are buffered and presented to the analog card. The low-pass filter networks at the output buffers are to filter out spikes caused by address changes when Chip Enable is asserted. The Timing ROM is programmed to perform Voltage Control, Chip Enable, Temperature Test and other voltage and level controls for the particular cardset. The Timing Diagram shows the data in this ROM.

5.2.5 PROGRAM COUNTER

For an attempt to program data into the PROM, a test pulse is issued prior to enabling Program, and slightly afterwards the PROM is enabled to test for Data Compare. The test pulse is presented to the Count Enable gate (U11) as a low-going pulse. The Input Data arriving on the DI Bus and the output of the PROM arriving on the DO Bus are exclusive-ORed together by gates U18 and U17. If any one of the eight lines don't verify, the wire-ORed output line becomes low, thereby enabling the Count Enable gate. The Test Pulse arriving from the ROM exits U11 pin 10 to create a Count-Up Pulse applied to the Program Counter (U13).

5.2.6 OVERPROGRAM OPERATION

As the program passes through one sequence of operation, the Program Counter is incremented by 1 and the Overprogram Count Multiplier (U14) is loaded by NOR gate U11 pin 13 to the preset value of JP1. The program sequence will continue to loop until a verification occurs between the DO and DI Buses. The result is that the minimum number of pulses required to program the PROM will be recorded in the Program Counter. As soon as verification has occurred, the test pulse is applied through Inverter U9 pin 11, delayed by the integrating network, and passed through Inverter U10 to cause a decrement of the Overprogram Count Multiplier U14. The Overprogram Count Multiplier decrements one time for each Program Pulse in the Overprogram Mode until a borrow pulse exits U14 pin 13. The borrow pulse is applied to the downcount, pin 4, of the main counter, U13, and also through pin 5 of inverter U10 to load the Overprogram Count Multiplier once again to the value of JP1. Overprogramming continues until U12 issues a borrow pulse on pin 13. This indicates that the Program Counter has arrived at Count 0. As that occurs, the low-going pulse at U12 pin 13 drives the Clock U1 OFF via Diode CR6, and drives pin 5 of gate U9 low, thereby releasing the Clock Inhibit line (pin Y). The programmer is then allowed to continue into the Verify Mode, at which time card pin AA goes high awaiting the next Write command.

5.2.7 TEMPERATURE SENSING

A Pause/Temperature Sense network (U1) is shown in the lower right hand corner of the schematic. This device is a comparator with a selectable reference level adjusted by potentiometer R6, which provides a .25 V drop across resistor R1. Temperature Sensing occurs within the PROM via a Diode network whose resistance increases as the temperature increases. If the V_{BB} input line is above the reference, the output pin 7 goes to ground, thereby stopping the clock until the PROM cools. This device, therefore, allows for programming control by its temperature, as well as overprogramming requirements, as determined by the PROM itself.

5.2.8 WORD LIMIT

Word Limit on this card is accomplished by Jumper selection. JP2 is used so that as a particular address line becomes high (such as A_8 with JP2 in position 256), the output of inverter U20 pin 12 becomes low, and passes through double inverter U20 pin 6 to exit on pin CC. This signals Word Limit to the programmer.

5.2.9 OUTPUT SELECTION

Read gate, U8 pin 3, when high, selects the Analog Data Output gates to present the data to the DO Bus. This gate functions as follows:

1) WRITE MODE. When Write Select is present, and Word Limit has not yet been reached, gate U15 pin 1 is high. If the Read Pulse is **not** at pin X, that line being low allows U16 pin 6 to become high, allowing the Write Output Enable gate U8 pin 6 to become low, enabling the Read gate, U8 pin 2.

2) READ MODE. If Read Inhibit is selected, pin RR is low. If the Read Pulse is present, pin X becomes high, enabling the Read Output Select gate, U15 pin 4, which when inverted by U3 Pin 6 enables the Read gate, U8 pin 1.

5.3 ANALOG CARD

The following paragraphs describe the electrical operation of the 701-1183-1 Analog Card, which is shown in block diagram form in Figure 5-3. This card is used in conjunction with the MOS Digitral Card to program the read 1702 and 1702A MOS 256x8 PROMs. The 1702 programmed logic level is VOL, while the 1702A is VOH. Either device may be programmed or read simply by changing a jumper on the analog card, as shown in Figure 3-1 on page 3-1.

The MOS Digital Card provides control signals to the analog card through the 16-pin DIP connector J1. The PROM being programmed or read is connected through the 26-pin connector to the Analog Card.

5.3.1 ADDRESS BUFFERS

Address Buffers accommodate the eight incoming address lines, A_0-A_7, emanating from the programmer. The Buffers consist of exclusive-OR gates U20-U21 followed by High Voltage Drivers U6, U8, U13 and U15. The OR gates allow the addresses to be complemented by simply applying a high logic level to the common inputs. The High Voltage Drivers with pull-up resistors are used to provide the high voltages necessary when an address is asserted.

5.3.2 DATA PROGRAM BUFFERS AND DRIVERS

The Input Data Bus (DI_1-DI_8) carries TTL data arriving from the programmer. This data is presented to exclusive-OR gates U18-U19. Jumper JP1 controls data inversion; in the A position (1702 PROMs) incoming data is inverted, in the B position (1702A-PROMs) data is not inverted. The following description assumes JP1 is in the A position.

The outputs of the OR gates drive gates U5, U7, U12, U14, which invert the data to a high Bit-to-Program. Buffer outputs are applied directly to the 26-pin connector on lines B_1-B_8. Buffer outputs are also connected to the inputs of Comparators U10 and U11. During Program, J1-3 goes high, and DI Bus data is transferred to the PROM. During Read, J1-3 is low, the Buffers are disabled, and data from the PROM is presented to the Comparator.

5.3.3 DATA COMPARATOR

During Read, data from the PROM is presented to Comparators U10 and U11. The Read reference voltage at the negative comparator input is derived by R74 and R57. The crossover point from high to low determines the output level of the Comparator. A low detected in the PROM causes a low comparator output.

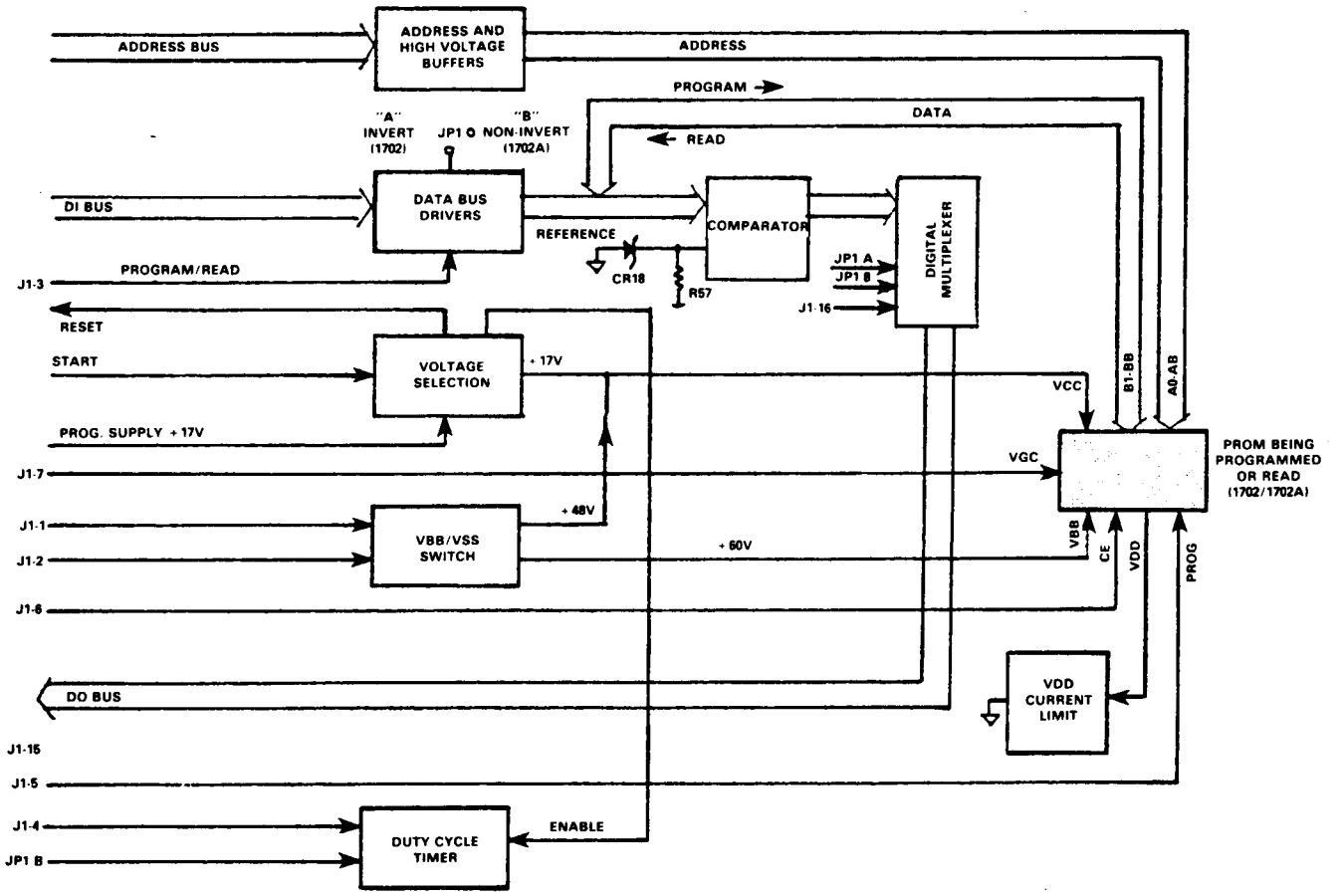


Figure 5-3. Block Diagram, 1183-1 Analog Card.

5.3.4 DIGITAL MULTIPLEXER

Comparator outputs are fed to the Digital Multiplexer, U16 and U17, which can invert input data, not invert the data, or float its outputs. The outputs float if J1-16 is low. If J1-16 is high and if J1 is in position B, the input data will be inverted (1702A PROMs); a high (programmed bit) will cause a low on the DO Bus. If J1 is in position A, a low (programmed 1702 bit) will cause a low on the DO Bus. Data on the DO Bus is used for comparison on the MOS Digital Card, and for verification by the programmer.

5.3.5 VOLTAGE SELECTION

Voltage is applied to the PROM only after Start goes high. This level is inverted by U9(see schematic) which turns on transistor Q3. This allows the +17V output from the programmable power supply to reach the PROM through current is drawn by the +17V line, the voltage drop across R12 becomes excessive (0.3 V or above), and transistor Q2 turns on. This supplies base current to Q8, which saturates and causes a Reset on line DD.

5.3.6 V_{BB}-V_{CC} SWITCH

J1-1 and J1-2 provide control to the V_{CC} and V_{BB} switch circuitry, Q4-Q7. When J1-1 goes high, it is inverted in U1, causing Q4 to saturate, hence connecting +48 V to the V_{CC} line. Operation is similar with J1-2, which connects the V_{BB} line to +60 V. These switches operate in Program only, overriding the +17 V line from the voltage selection network. The +48 V and +60 V supplies are applied through current limit resistors R33 and R38. Diode CR5 is cut off by the +60 V potential applied to V_{BB}. If excessive current is drawn on either of these lines the voltage drop allows conduction from the positive source through R39 or R35, which turns on Q8 and drives the Reset line (DD) low.

5.3.7 DUTY CYCLE TIMER

The temperature control circuitry of the MOS Digital Card is used in conjunction with the timer (Q9, C16, R71 and U2) on the Analog Card to achieve the 2% duty cycle required to program the 1702 PROM. When JP1 is in the A (1702) position, gate U2 pin 5 is enabled. A pulse arrives on J1 pin 4 to turn on transistor Q9 to charge C16. The voltage on C16 is monitored by the temperature test comparator on the Digital Card. Two clock pulses later, the temperature test comparator is strobed on the Digital Card. Since the voltage on C16 is still high the Digital Card will pause. The pause will continue until the voltage on C16 drops to a level selected on the Digital Card, and the clock will step through the remaining portion of the program at the normal rate. If JP1 is in the B (1702A) position, U2 is disabled and the duty cycle is determined by the Digital Card.

5.3.8 V_{DD} CURRENT LIMIT

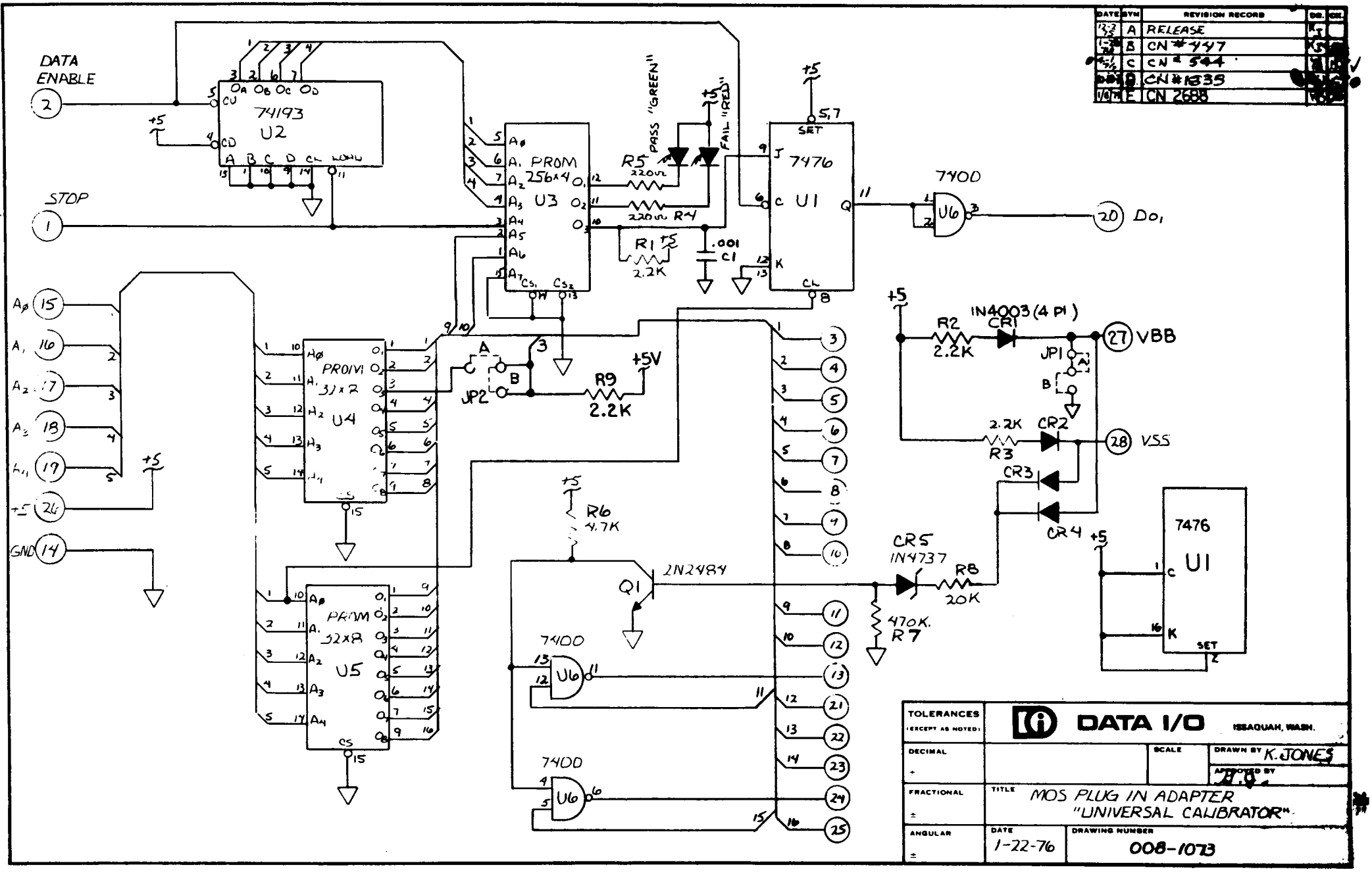
The Transistor Q1 is used for current limiting on the V_{DD} line. Two diodes CR7 and CR8 provide a standoff bias characteristic for transistor Q1 so that if excessive current is driven through R23, Q1 is current limited for short circuit protection by the standoff bias and shutoff characteristic of the transistor.

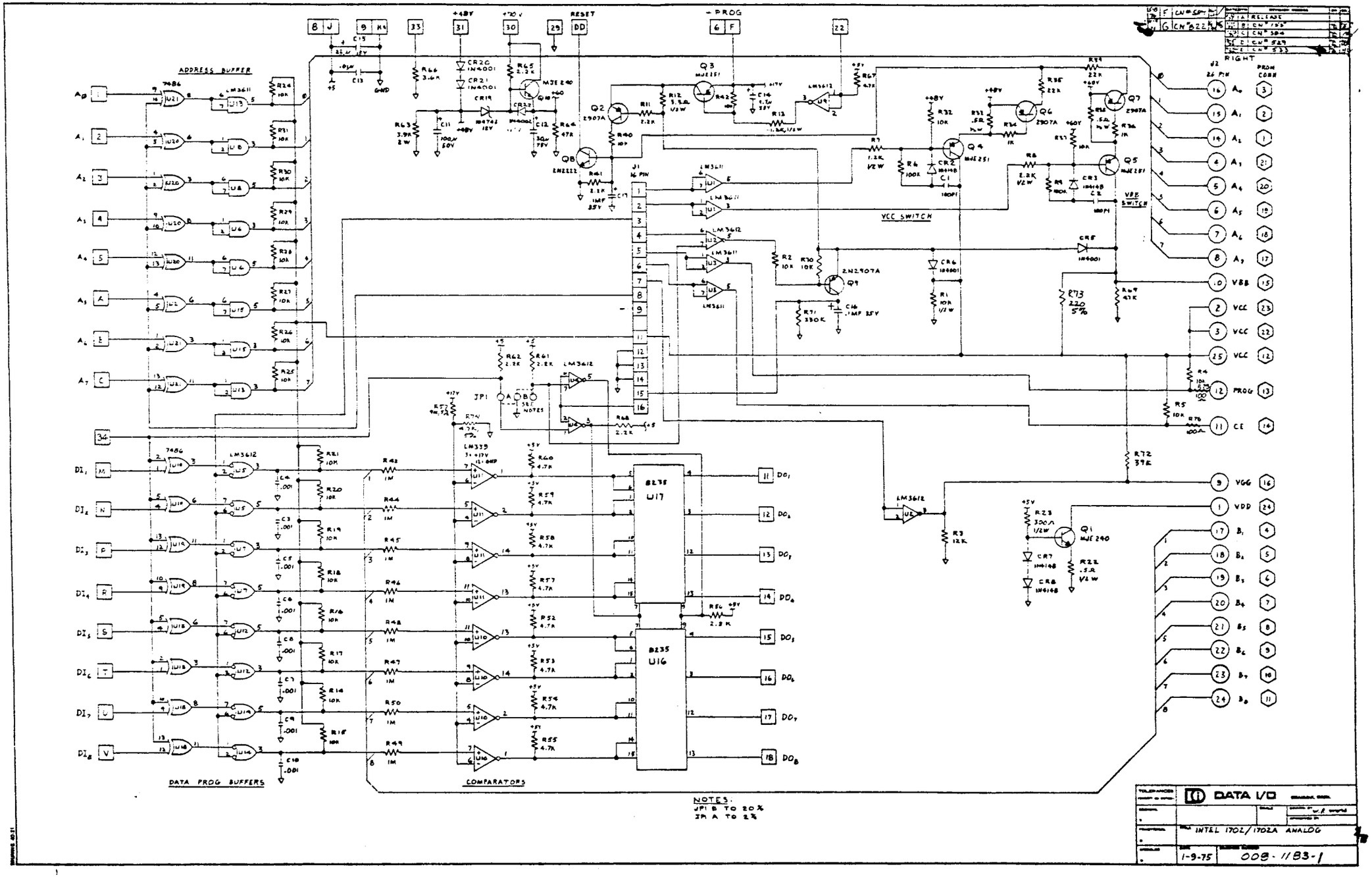
5.3.9 BACKWARDS DEVICE TEST

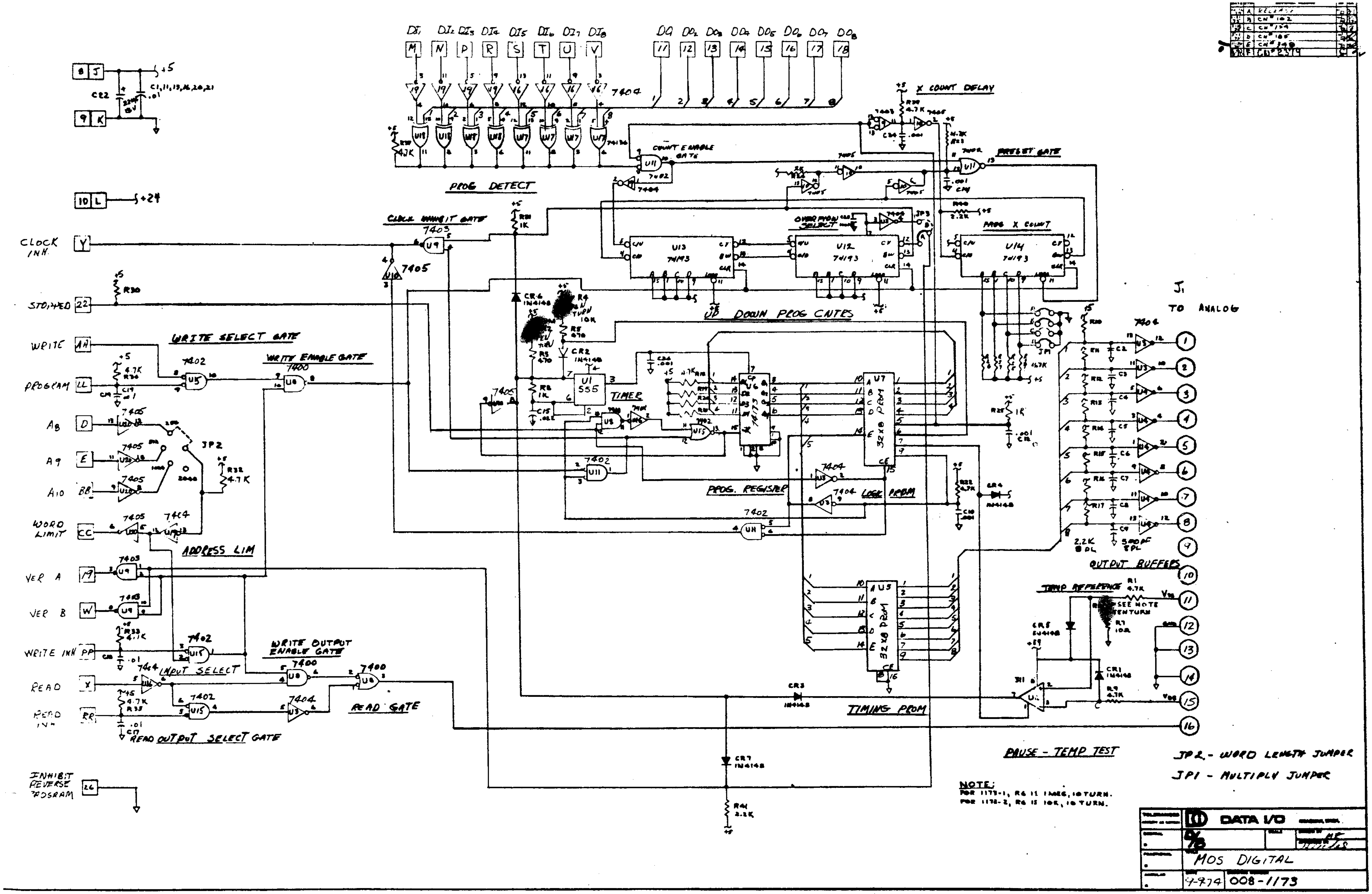
The 1702 or 1702A PROM has a characteristic that allows detection of backwards insertion in the socket adapter. The instrument goes into a current limit state, which prevents Start from occurring.

SECTION 6
SCHEMATICS

008-1173	MOS Digital
008-1183-1	1702/1702A Analog
008-1073	Calibration Adapter


DATA ENABLE
STOP
74193 U2
PROM 256x4 U3
R5 220Ω
R4 220Ω
PASS "GREEN"
FAIL "RED"
R1 2.2K
.001 C1
7476 U1
7400 U6
Do1
PROM 32x1 U4
PROM 32x8 U5
JP2
R9 2.2K
+5V
R6 4.7K
Q1 2N2484
7400 U6
7400 U6
IN4003 (4 PI)
R2 2.2K
CR1
JP1
VBB
R3 2.2K
CR2
VSS
CR3
CR4
CR5 IN4737
R8 20K
470K R7
7476 U1
A0 15
A1 16
A2 17
A3 18
A4 19
+5 26
GND 14
DATE | SYM | REVISION RECORD
A RELEASE
B CN #447
C CN # 544
D CN #1835
E CN 2688
TOLERANCES (EXCEPT AS NOTED)
DECIMAL ±
FRACTIONAL ±
ANGULAR ±
DATA I/O ISSAQUAH, WASH.
SCALE
DRAWN BY K. JONES
APPROVED BY
TITLE MOS PLUG IN ADAPTER "UNIVERSAL CALIBRATOR"
DATE 1-22-76
DRAWING NUMBER 008-1073


ADDRESS BUFFER
DATA PROG BUFFERS
COMPARATORS
VCC SWITCH
VBB SWITCH
- PROG
RESET
+48V
+30V
+12V
+5
GND
JP1
SEE NOTES
J1 36 PIN
J2 24 PIN
PROM CODE
8235 U17
8235 U16
LM339
LM3611
LM3612
7486
2N2907A
MJE240
MJE251
MJE15I
IN4001
IN4148
IN4748
A0
A1
A2
A3
A4
A5
A6
A7
VBB
VCC
PROG
CE
VGG
VDD
B1
B2
B3
B4
B5
B6
B7
B8
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
NOTES:
JP1 B TO 20%
JP1 A TO 2%
RIGHT
DATA I/O
INTEL 1702/1702A ANALOG
1-9-75
008-1183-1



PROG DETECT
COUNT ENABLE GATE
X COUNT DELAY
PRESET GATE
CLOCK INHIBIT GATE
OVERFLOW SELECT
PROG X COUNT
UP DOWN PROG CNTRS
WRITE SELECT GATE
WRITE ENABLE GATE
TIMER
ADDRESS LIM
PROG. REGISTER
LOGIC PROM
TIMING PROM
OUTPUT BUFFERS
TEMP REFERENCE
WRITE OUTPUT ENABLE GATE
INPUT SELECT
READ GATE
READ OUTPUT SELECT GATE
PAUSE - TEMP TEST
CLOCK INH
STOPPED
WRITE
PROGRAM
WORD LIMIT
VER A
VER B
WRITE INH
READ
READ INH
INHIBIT REVERSE PROGRAM
J1 TO ANALOG
JP2 - WORD LENGTH JUMPER
JP1 - MULTIPLY JUMPER
NOTE:
FOR 1173-1, R6 IS 1MEG, 10 TURN.
FOR 1173-2, R6 IS 10K, 10 TURN.
DATA I/O
MOS DIGITAL
008-1173