Ordering Information
High-Performance CMOS Products

WS57C----- **-35** **D** **I** **B**

Basic Part Number

Manufacturing Process:

(Blank) = WSI Standard Manufacturing Flow

B = MIL-STD-883C Manufacturing Flow

Operating Temperature Range:

(Blank) = Commercial: 0° to +70°C
V_{CC}: +5V ± 5%

I = Industrial: −40° to +85°C
V_{CC}: +5V ± 10%

M = Military: −55° to +125°C
V_{CC}: +5V ± 10%

Package:

		Window
A	= PPGA Plastic Pin Grid Array	No
B	= 0.900" Size Brazed Ceramic DIP	No
C	= CLLCC Ceramic Leadless Chip Carrier	Yes*
D	= 0.600" CERDIP	Yes
F	= Ceramic Flatpack	Yes*
G	= CPGA Ceramic Pin Grid Array	No
H	= Ceramic Flatpack	No*
J	= Plastic Leaded Chip Carrier	No*
K	= 0.300" Thin CERDIP	No
L	= CLDCC Ceramic Leaded Chip Carrier	Yes*
N	= CLDCC Ceramic Leaded Chip Carrier	No*
P	= 0.600" Plastic DIP	No
Q	= Plastic Quad Flatpack	No*
R	= Ceramic Side Brazed	Yes
S	= 0.300" Thin Plastic DIP	No
T	= 0.300" Thin CERDIP	Yes
W	= Waffle Packed Dice	—
X	= Ceramic Pin Grid Array	Yes
Y	= 0.600" CERDIP	No
Z	= CLLCC	No

Speed:

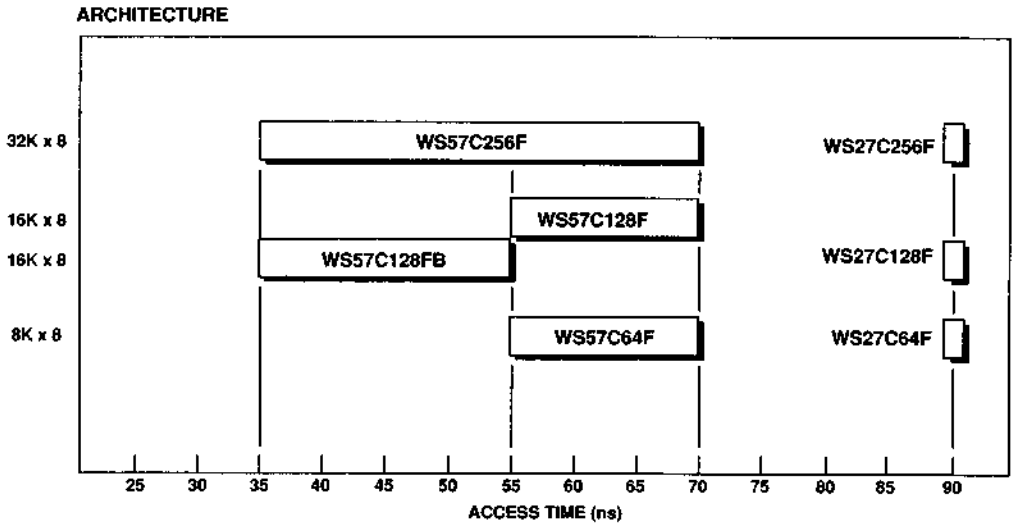
−35 = 35 ns
−55 = 55 ns
−70 = 70 ns
Etc.

*Surface Mount

FAMILY OF HIGH PERFORMANCE CMOS EPROMs

PART NUMBER	PAGE NO.	DENSITY (BITS)	ARCHITECTURE	SPEED (NS)	DRAWING NO.	NO. OF PINS	PACKAGE
WS57C64F	2-5	64K	8K x 8	55–70	C2 D2 J4	32 28 32	CLLCC CERDIP, 0.6" PLDCC
WS27C64F	2-11	64K	8K x 8	90	C2 D2	32 28	CLLCC CERDIP, 0.6"
WS57C128F	2-17	128K	16K x 8	55–70	C2 D2	32 28	CLLCC CERDIP, 0.6"
WS57C128FB	2-23	128K	16K x 8	35–55	C2 D2 J4 L3	32 28 32 32	CLLCC CERDIP, 0.6" PLDCC CLDCC
WS27C128F	2-29	128K	16K x 8	90	C2 D2	32 28	CLLCC CERDIP, 0.6"
WS57C256F	2-35	256K	32K x 8	35–70	C2 D2 J4 L3 T2	32 28 32 32 28	CLLCC CERDIP, 0.6" PLDCC CLDCC CERDIP, 0.3"
WS27C256F	2-41	256K	32K x 8	90	C2 D2 L3	32 28 32	CLLCC CERDIP, 0.6" CLDCC

WSI's Family of High Performance CMOS EPROMs are available in all three operating temperature ranges: Commercial (0 to +70°C), Industrial (–40 to +85°C) and Military (–55 to +125°C). In addition, several versions are available as Standard Military Drawing (SMD) products.


ARCHITECTURE
32K x 8
16K x 8
16K x 8
8K x 8
WS57C256F
WS57C128F
WS57C128FB
WS57C64F
WS27C256F
WS27C128F
WS27C64F
25
30
35
40
45
50
55
60
65
70
75
80
85
90
ACCESS TIME (ns)

AMD	WSI
Am27C128	WS57C128FB
Am27C256	WS57C256F
Am27C64	WS57C64F

ATMEL	WSI
AT27HC256/L	WS57C256F
AT27HC256R/R	WS57C256F
AT27HC64/L	WS57C64F
AT27HC64R/RL	WS57C64F

CATALYST	WSI
CAT27128A	WS57C128FB
CAT27256	WS57C256F
CAT2764A	WS57C64F
CAT27HC256	WS57C256F

CYPRESS	WSI
CY7C274	WS57C256F

GOLDSTAR	WSI
GL3620	WS57C64F
GM27HC64	WS57C64F

HITACHI	WSI
HN27C256HG	WS57C256F

INTEL	WSI
27C128B	WS57C128FB
27C256	WS57C256F

MICROCHIP	WSI
27HC256	WS57C256F
27HC64	WS57C64F

OKI	WSI
MSM27C256	WS57C256F

SANYO	WSI
LA7620	WS57C64F

SGS-T	WSI
M27128/A	WS57C128FB
M27256	WS57C256F
TS27C64A	WS57C64F

SHARP	WSI
LH57126	WS57C128FB
LH5763	WS57C64F
LH5762	WS57C64F

SIGNETICS	WSI
27HC128	WS57C128FB

SPRAGUE	WSI
SCM27C256	WS57C256F

TOSHIBA	WSI
TMM27128`	WS57C128FB
TMM27256	WS57C256F
TMM2764	WS57C64F

TI	WSI
TMS27C64	WS57C64F
TMS27C128	WS57C128FB

HIGH SPEED 8K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **Low Power Consumption**
- **DESC SMD No. 85102**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**

GENERAL DESCRIPTION

The WS57C64F is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming very little power.

Two major features of the WS57C64F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited. Examples of these applications are modems, secure telephones, servo controllers, and industrial controllers.

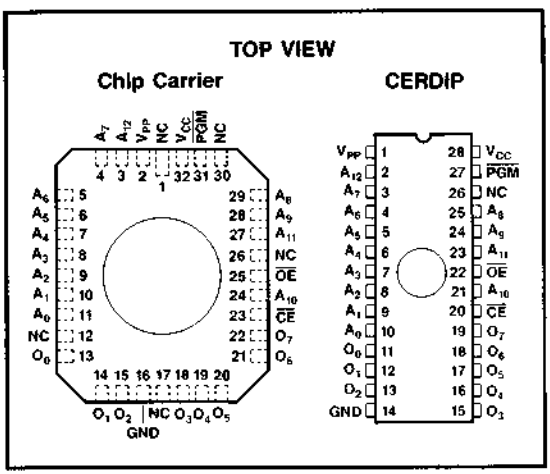
The WS57C64F is configured in the standard EPROM pinout which provides an easy upgrade path to higher density EPROMs.

MODE SELECTION

MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	5.0V	5.0V	D_{OUT}
Output Disable	X	X	V_{IH}	5.0V	5.0V	High Z
Standby	X	V_{IH}	X	5.0V	5.0V	High Z
Programming	V_{IL}	V_{IL}	V_{IH}	V_{PP}	5.8V	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{IL}	V_{PP}	5.8V	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	5.0V	High Z

X can be V_{IL} or V_{IH}.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C64F-55	WS57C64F-70
Address Access Time (Max)	55ns	70ns
Chip Select Time (Max)	55ns	70ns
Output Enable Time (Max)	20ns	25ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

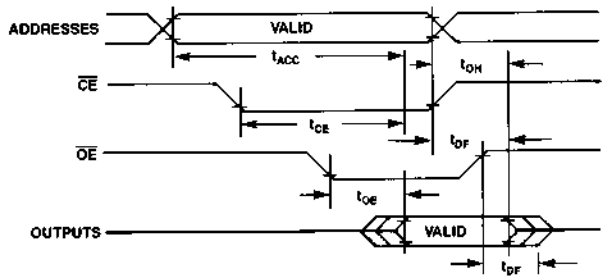
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 5)		−0.1	0.8	V
V_{IH}	Input High Level	(Note 5)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OH} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$ (Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$ (Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 4) Outputs Not Loaded	Comm'l		20	mA
			Military		30	
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		25	mA
			Military		35	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 3 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS57C64F-55		WS57C64F-70		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay		55		70	
t_{OE}	$\overline{OE}$ to Output Delay		20		25	
t_{DF}	Output Disable to Output Float		20		25	
t_{OH}	Address to Output Hold	10		10		

AC READ TIMING DIAGRAM

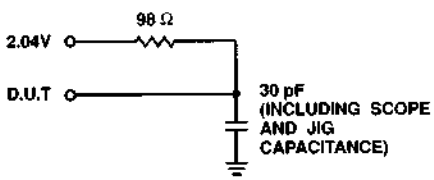


CAPACITANCE[6] T_A = 25°C, f = 1 MHz

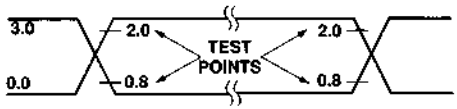
SYMBOL	PARAMETER	CONDITIONS	TYP[7]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		25	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = − 4mA)	2.4		V

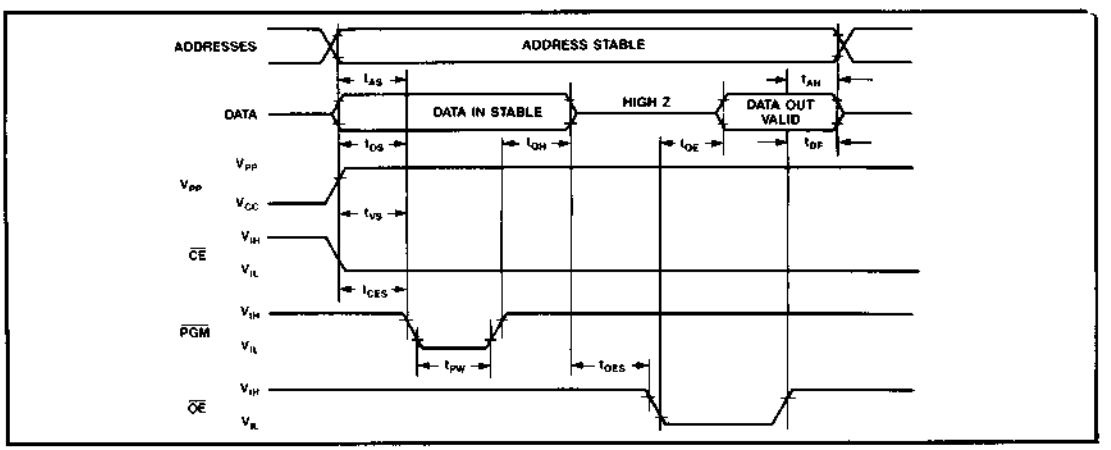
NOTES: 9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

NOTE: 12. Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C64F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C64F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C64F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C64F-70DI	70	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C64F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C64F-70J	70	32 Pin PLDCC	J4	Comm'l	Standard

NOTE: 13. The actual part marking will not include the initials "WS."

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

MILITARY 8K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 90 ns Over Full Mil Temp Range
- **Low Power Consumption**
- **DESC SMD No. 85102**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Military Temperature Operating Range**

2

GENERAL DESCRIPTION

The WS27C64F is a High Performance 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full Military temperature operating range.

The WS27C64F is a direct drop-in replacement for the industry standard 27C64 and/or 2764 EPROMs. It was developed specifically for this purpose and requires no board or software modifications to complete the change.

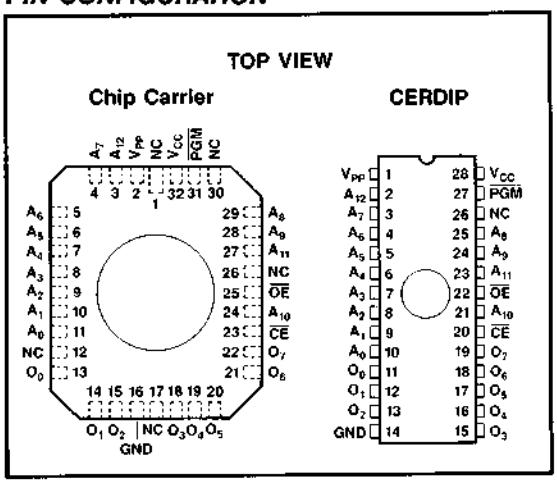
The WS27C64F is configured in the standard EPROM pinout which provides an easy upgrade path to the WS27C128F and WS27C256F.

MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. $A_0 = V_{IL}$ = MFGR 23H, $A_0 = V_{IH}$ = DEVICE A8H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C64F-90
Address Access Time (Max)	90 ns
Chip Select Time (Max)	90 ns
Output Enable Time (Max)	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

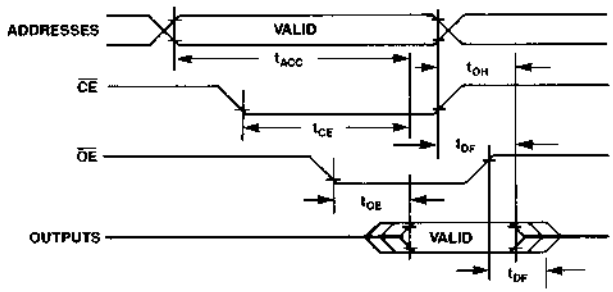
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 4)	−0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	(Note 1)		200	µA
I_{SB2}	V_{CC} Standby Current (TTL)	(Note 2)		10	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)		25	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3)		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd	−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS27C64F-90		UNITS
		MIN	MAX	
t_{ACC}	Address to Output Delay		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		90	
t_{OE}	$\overline{OE}$ to Output Delay		30	
t_{DF}	Output Disable to Output Float		30	
t_{OH}	Address to Output Hold	0		

AC READ TIMING DIAGRAM

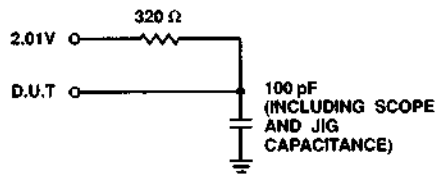


CAPACITANCE (5) T_A = 25°C, f = 1 MHz

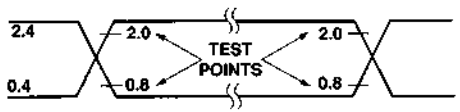
SYMBOL	PARAMETER	CONDITIONS	TYP (6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0"

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current (Note 3)		50	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 4 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = − 1mA)	2.4		V

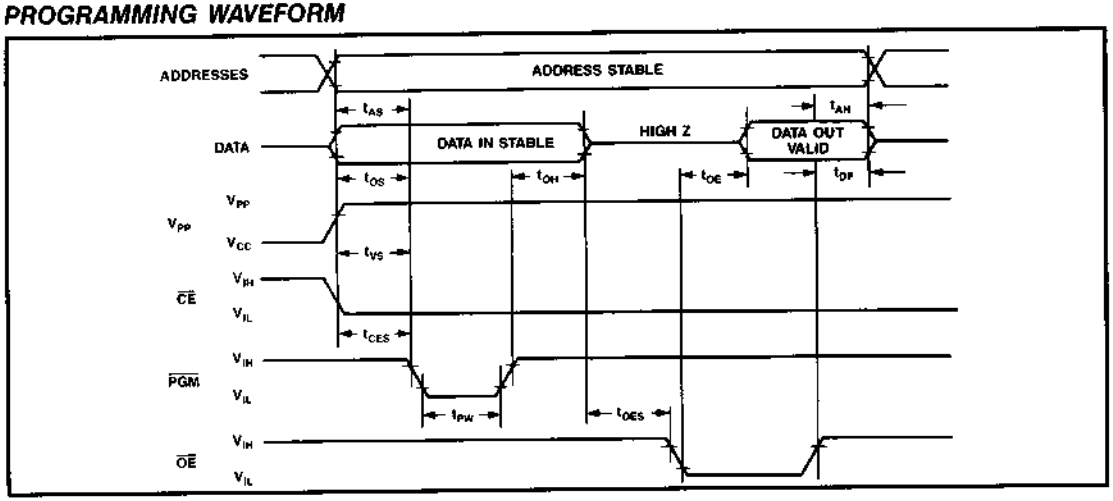
NOTES: 8. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
9. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
10. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{DS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{DH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

NOTE: 11. Single shot programming algorithms should use one 10 ms PGM pulse per byte.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C64F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C64F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTE: 12. The actual part marking will not include the initials "WS."

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-87661**
- **EPI Processing**
  — Latch-up Immunity Up to 200 mA
- **Standard EPROM Pinout**

GENERAL DESCRIPTION

The WS57C128F is a High Performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with an advanced CMOS technology which enables it to operate at Bipolar speeds while consuming only 90 mA.

Two major features of the WS57C128F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited. Examples of these applications are modems, secure telephones, servo controllers, and industrial controllers.

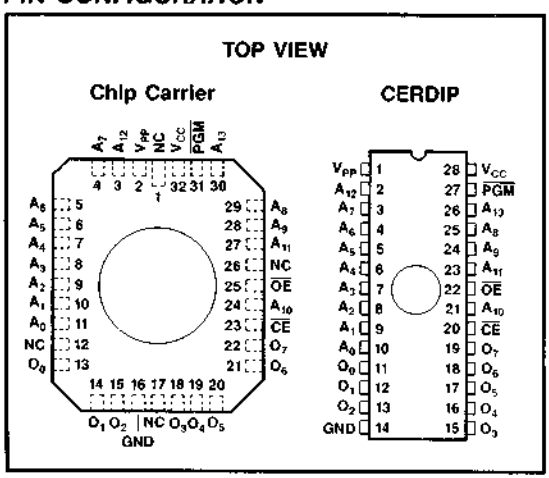
The WS57C128F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	5.0V	5.0V	D_{OUT}
Output Disable	X	X	V_{IH}	5.0V	5.0V	High Z
Standby	X	V_{IH}	X	5.0V	5.0V	High Z
Programming	V_{IL}	V_{IL}	V_{IH}	V_{PP}	5.8V	D_{IN}
Program Verify	V_{IH}	V_{IH}	V_{IL}	V_{PP}	5.8V	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	5.0V	High Z

X can be V_{IL} or V_{IH}.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C128F-55	WS57C128F-70
Address Access Time (Max)	55 ns	70 ns
Chip Select Time (Max)	55 ns	70 ns
Output Enable Time (Max)	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ±10%
Military	−55°C to +125°C	+5V ±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

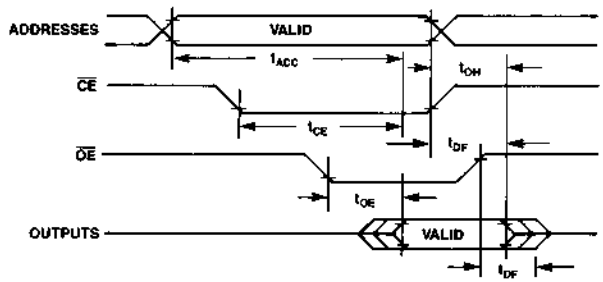
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 5)		−0.1	0.8	V
V_{IH}	Input High Level	(Note 5)		2.0	V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	(Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	(Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 4) Outputs Not Loaded	Comm'l		30	mA
			Military		40	
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		50	mA
			Military		60	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 4 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS57C128F-55		WS57C128F-70		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay		55		70	
t_{OE}	$\overline{OE}$ to Output Delay		25		25	
t_{DF}	Output Disable to Output Float		25		25	
t_{OH}	Address to Output Hold	0		0		

AC READ TIMING DIAGRAM



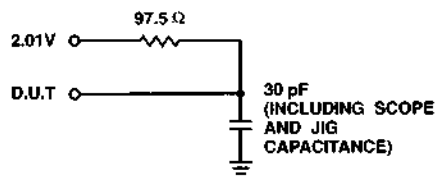
2

CAPACITANCE[6] T_A = 25°C, f = 1 MHz

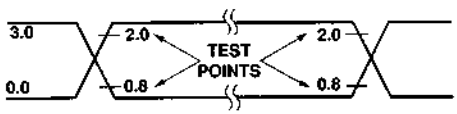
SYMBOL	PARAMETER	CONDITIONS	TYP[7]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		30	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 4mA)	2.4		V

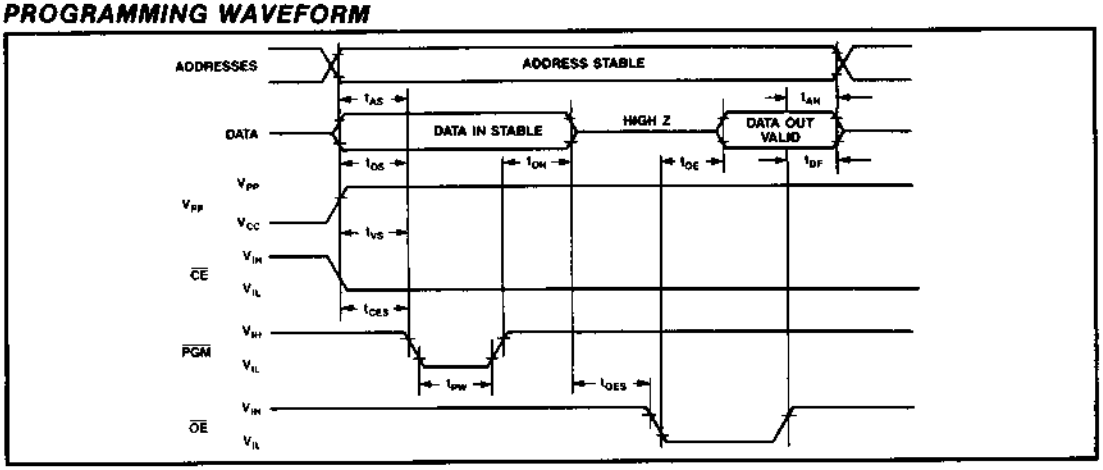
NOTES:
9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

NOTE: 12. Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C128F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C128F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128F-70DM	70	28-Pin CERDIP, 0.6"	D2	Military	Standard
WS57C128F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTE: 13. The actual part marking will not include the initials "WS."

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-87661**
- **EPI Processing**
  — Latch-up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **DIP and Surface Mount Packaging Available**

GENERAL DESCRIPTION

The WS57C128FB is a High Performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with an advanced CMOS technology which enables it to operate at Bipolar speeds while consuming only 90 mA.

Two major features of the WS57C128FB are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited.

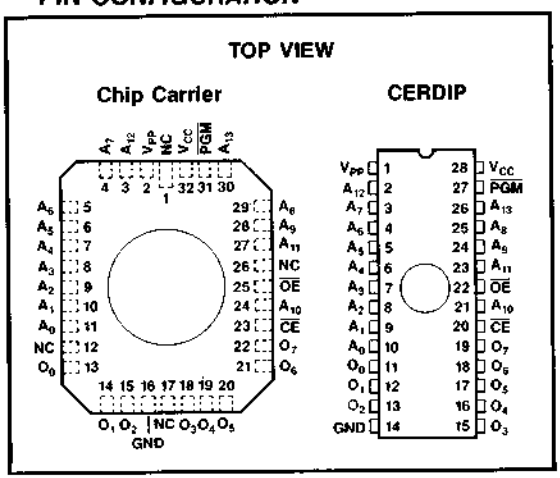
The WS57C128FB is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs. The EPROMs are available in both 600 Mil Dip packages, and both J-leaded and leadless surface mount packages.

MODE SELECTION

MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	5.0V	5.0V	D_{OUT}
Output Disable	X	X	V_{IH}	5.0V	5.0V	High Z
Standby	X	V_{IH}	X	5.0V	5.0V	High Z
Programming	V_{IL}	V_{IL}	V_{IH}	V_{PP}	5.8V	D_{IN}
Program Verify	V_{IH}	V_{IH}	V_{IL}	V_{PP}	5.8V	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	5.0V	High Z

X can be V_{IL} or V_{IH}.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C128FB-35	WS57C128FB-45	WS57C128FB-55
Address Access Time (Max)	35 ns	45 ns	55 ns
Chip Select Time (Max)	35 ns	45 ns	55 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

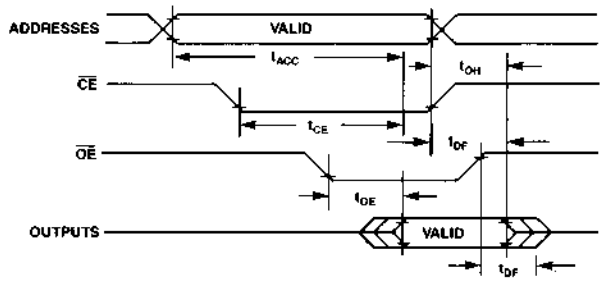
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 5)		−0.1	0.8	V
V_{IH}	Input High Level	(Note 5)		2.0	V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	(Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	(Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 4) Outputs Not Loaded	Comm'l		30	mA
			Military		40	
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		50	mA
			Military		60	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 4 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	-35		-45		-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		35		45		55	ns
t_{CE}	$\overline{CE}$ to Output Delay		35		45		55	
t_{OE}	$\overline{OE}$ to Output Delay		20		25		25	
t_{DF}	Output Disable to Output Float		20		25		25	
t_{OH}	Address to Output Hold	0		0		0		

AC READ TIMING DIAGRAM

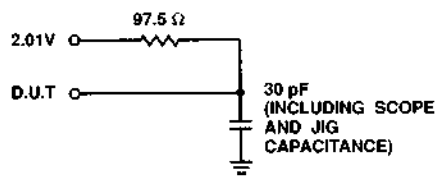


CAPACITANCE (6) T_A = 25°C, f = 1 MHz

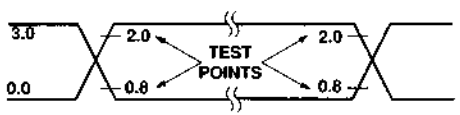
SYMBOL	PARAMETER	CONDITIONS	TYP (7)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0"

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.5V \pm 5\%$, $V_{PP} = 12.5 \pm 0.5V$)

SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current ($V_{IN} = V_{CC}$ or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE} = \overline{PGM} = V_{IL}$)		60	mA
I_{CC}	V_{CC} Supply Current		30	mA
V_{OL}	Output Low Voltage During Verify ($I_{OL} = 16$ mA)		0.4	V
V_{OH}	Output High Voltage During Verify ($I_{OH} = -4$mA)	2.4		V

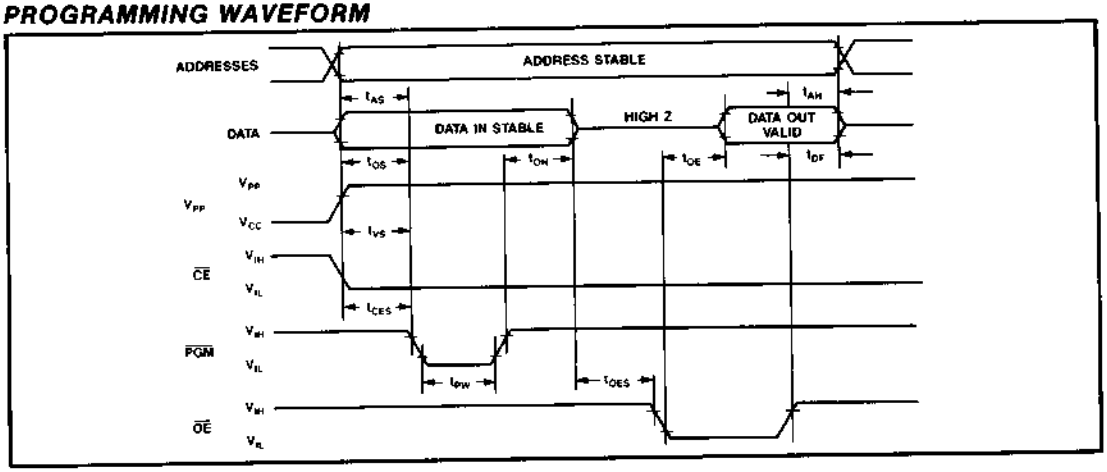
NOTES: 9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.5V \pm 5\%$, $V_{PP} = 12.5 \pm 0.5V$)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms

NOTE: 12. Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C128FB-35D	35	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128FB-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128FB-45J	45	32 Pin PLDCC	J4	Comm'l	Standard
WS57C128FB-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C128FB-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C128FB-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTE: 13.The actual part marking will not include the initials "WS."

2

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

MILITARY 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 90 ns Over Full Mil Temp Range
- **Low Power Consumption**
- **DESC SMD No. 5962-87661**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Military Operating Range**

GENERAL DESCRIPTION

The WS27C128F is an extremely High Perfoprmance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full military temperature operating range.

The WS27C128F was specifically designed to replace standard EPROMs in military environments. No hardware or software changes are required to replace standard military 27128 EPROMs with the WSI WS27C128F.

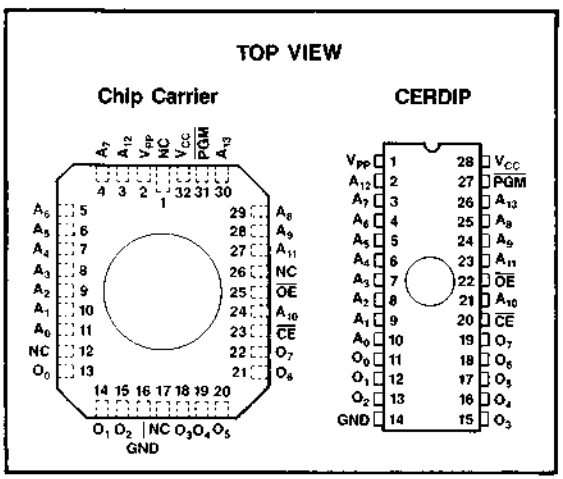
The WS27C128F is configured in the standard EPROM pinout which provides an easy upgrade path for the WS27C64F.

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE A8H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C128F-90
Address Access Time (Max)	90 ns
Chip Select Time (Max)	90 ns
Output Enable Time (Max)	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

*Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 4)	−0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	(Note 1)		200	µA
I_{SB2}	V_{CC} Standby Current (TTL)	(Note 2)		10	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)		25	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3)		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd	−10	10	µA

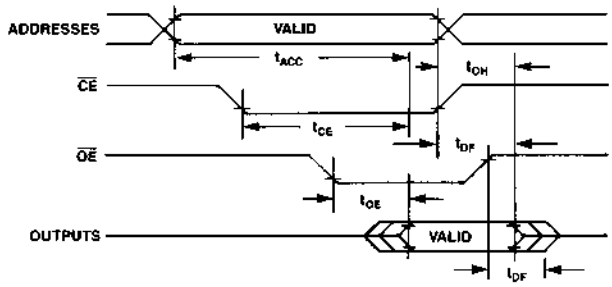
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS27C128F-90		UNITS
		MIN	MAX	
t_{ACC}	Address to Output Delay		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		90	
t_{OE}	$\overline{OE}$ to Output Delay		30	
t_{DF}	Output Disable to Output Float		30	
t_{OH}	Address to Output Hold	0		

NOTE: 5. Single shot programming algorithms should use one 10 ms PGM pulse per word.

AC READ TIMING DIAGRAM

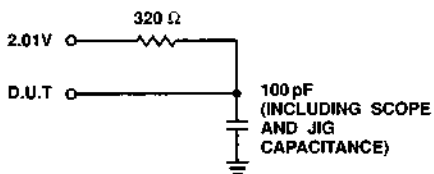


CAPACITANCE[6] T_A = 25°C, f = 1 MHz

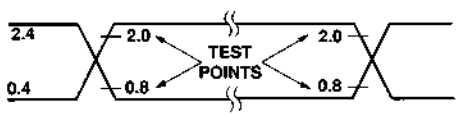
SYMBOL	PARAMETER	CONDITIONS	TYP[7]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})		30	mA
I_{CC}	V_{CC} Supply Current		50	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 4 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = − 1mA)	2.4		V

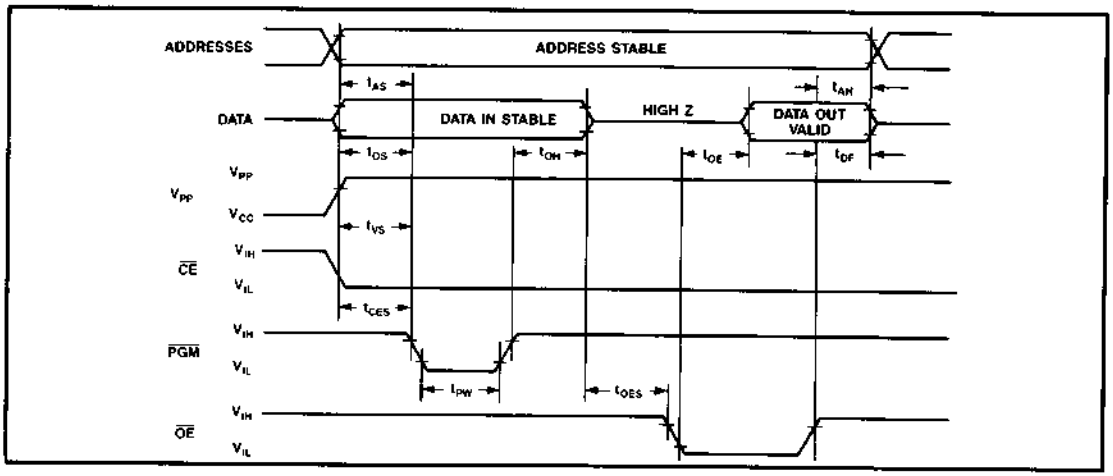
NOTES: 9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{CES}	Chip Enable Setup Time	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{DS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{DH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	5		ms

NOTE: 12. Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C128F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C128F-90DM	90	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS27C128F-90DMB	90	28-Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

NOTE: The actual part marking will not include the initials "WS."

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 32K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-86063**
- **EPI Processing**
  — Latch-up Immunity Up to 200 mA
- **Standard EPROM Pinout**

GENERAL DESCRIPTION

The WS57C256F is a High Performance 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with an advanced CMOS technology which enables it to operate at speeds as fast as 35 ns Access Time.

Two major features of the WS57C256F are its Low Power and High Speed. While operating in a TTL environment it consumes only 120 mA while cycling at full speed. Additionally, the WS57C256F can be placed in a standby mode which drops operating current below 15 mA in a TTL environment and 500 µA in a CMOS environment.

The WS57C256F also has exceptional output drive capability. It can source 4 mA and sink 16 mA per output.

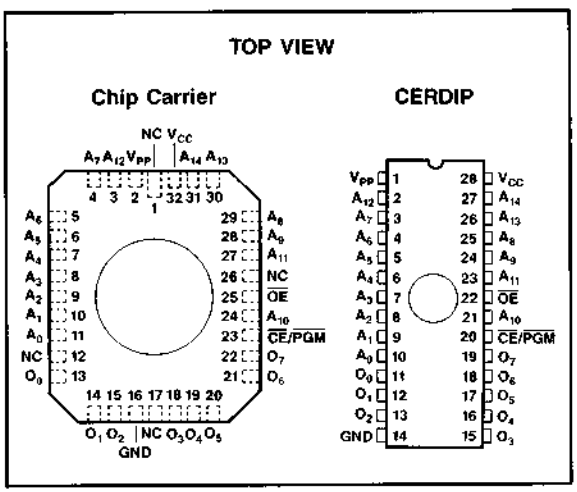
The WS57C256F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	X	X	V_{CC}	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	V_{PP}[2]	5.8V	D_{IN}
Program Verify	X	V_{IL}	X	X	V_{PP}[2]	5.8V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	V_{PP}[2]	5.0V	High Z
Signature[3]	V_{IL}	V_{IL}	V_H[2]	V_{IL}	V_{CC}	5.0V	23 H[4]
	V_{IL}	V_{IL}	V_H[2]	V_{IH}	V_{CC}	5.0V	A8 H[5]

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $V_H = V_{PP} = 12.75 \pm 0.25V$.
3. A_1–A_8, A_{10}–$A_{14} = V_{IL}$.
4. Manufacturer
5. Device

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C256F-35	WS57C256F-45	WS57C256F-55	WS57C256F-70
Address Access Time (Max)	35ns	45 ns	55 ns	70 ns
Chip Select Time (Max)	20ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20ns	20 ns	25 ns	30 ns

NOTE: Shaded area describes product available Q4 '91.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

*Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Military	−55°C to +125°C	+5V ±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

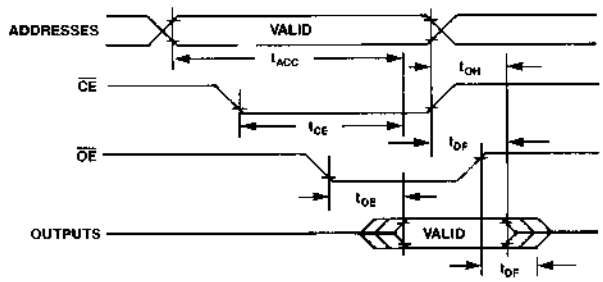
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 5)		−0.1	0.8	V
V_{IH}	Input High Level	(Note 5)		2.0	V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = − 4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$ (Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$ (Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 4) Outputs Not Loaded	Comm'l		20	mA
			Military		25	
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		50	mA
			Military		60	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 4 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	-35		-45		-55		-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		35		45		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay		35		45		55		70	
t_{OE}	$\overline{OE}$ to Output Delay		20		20		25		30	
t_{DF}	Output Disable to Output Float		20		20		25		30	
t_{OH}	Address to Output Hold	0		0		0		0		

AC READ TIMING DIAGRAM

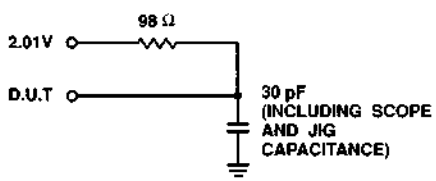


CAPACITANCE (6) T_A = 25°C, f = 1 MHz

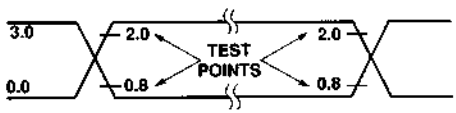
SYMBOL	PARAMETER	CONDITIONS	TYP (7)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 6. This parameter is only sampled and is not 100% tested.
7. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current (Note 4)		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.4	V
V_{OH}	Output High Voltage During Verify (I_{OH} = −4mA)	2.4		V

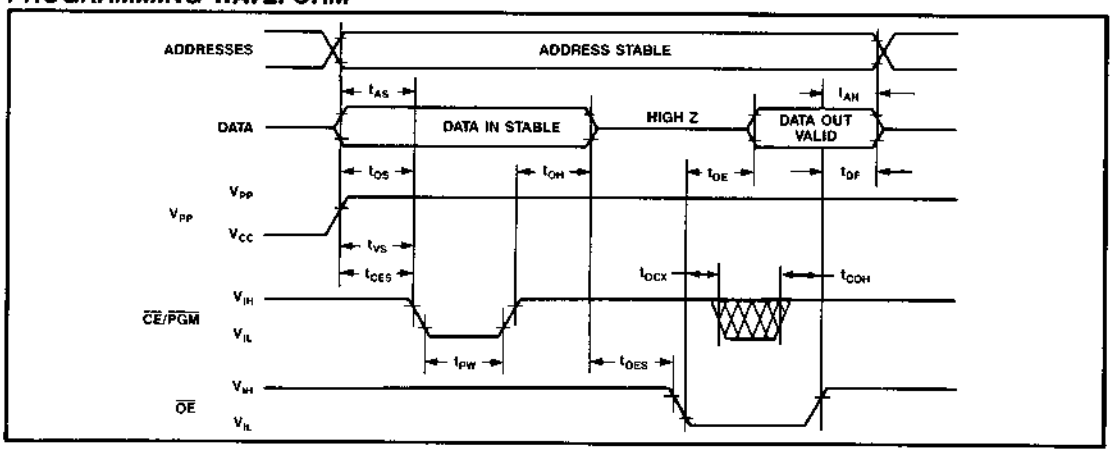
NOTES: 9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{COH}	$\overline{CE}$ High to $\overline{OE}$ High	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/$\overline{CE}$ Setup time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	0.1	1	10	ms
t_{OCX}	$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	2			µs

NOTE: 12. Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C256F-35D	35	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-35T	35	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C256F-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C256F-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C256F-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C256F-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C256F-70CM	70	32 Pad CLLCC	C2	Military	Standard
WS57C256F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-70DM	70	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS57C256F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C256F-70J	70	32 Pin PLDCC	J4	Comm'l	Standard
WS57C256F-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard

NOTE: 13.The actual part marking will not include the initials "WS."
14. Shaded area describes product available Q4 '91. Contact your WSI Sales Representative for availability.

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

MILITARY 32K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — 90 ns Over Full Mil Temp Range
- **Low Power Consumption**
- **DESC SMD No. 5962-86063**
- **EPI Processing**
  - — Latch-up Immunity Up to 200 mA
  - — ESD Protection Exceeds 2000V
- **Standard EPROM Pinout**
- **Military Operating Range**

2

GENERAL DESCRIPTION

The WS27C256F is an extremely High Performance 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full military temperature operating range.

The WS27C256F was specifically designed to replace standard EPROMs in military environments. No hardware or software changes are required to replace standard military 27256 EPROMs with the WSI WS27C256F.

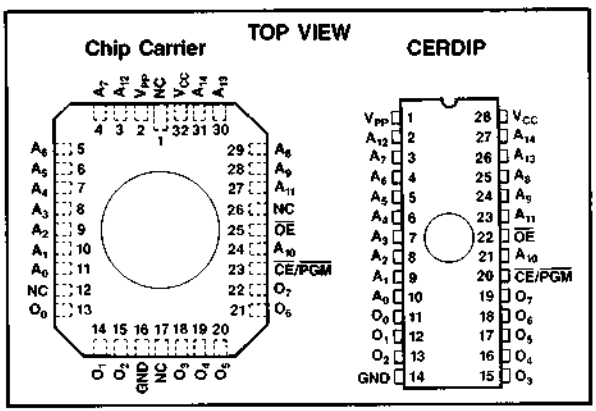
The WS27C256F is configured in the standard EPROM pinout which provides an easy upgrade path from the WS27C64F, and the 128K Bit WS27C128F.

MODE SELECTION

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE E0H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C256F-90
Address Access Time (Max)	90 ns
Chip Select Time (Max)	90 ns
Output Enable Time (Max)	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

*Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

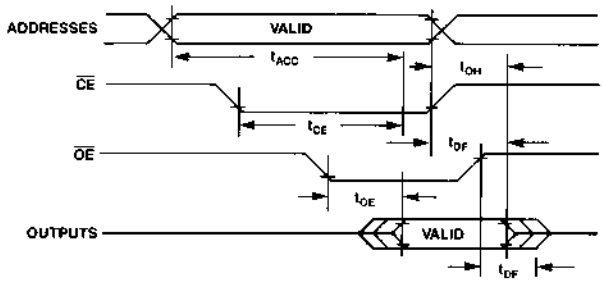
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IL}	Input Low Level	(Note 4)	−0.1	0.8	V
V_{IH}	Input High Level	(Note 4)	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$ (Note 1)		500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$ (Note 2)		5	mA
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)		40	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3)		45	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd	−10	10	µA

NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	WS27C256F-90		UNITS
		MIN	MAX	
t_{ACC}	Address to Output Delay		90	ns
t_{CE}	$\overline{CE}$ to Output Delay		90	
t_{OE}	$\overline{OE}$ to Output Delay		30	
t_{DF}	Output Disable to Output Float		30	
t_{OH}	Address to Output Hold	0		

AC READ TIMING DIAGRAM



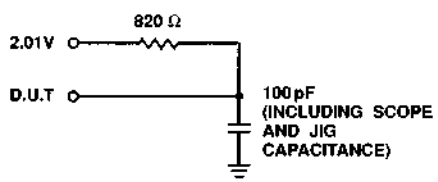
2

CAPACITANCE (5) T_A = 25°C, f = 1 MHz

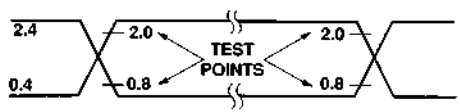
SYMBOL	PARAMETER	CONDITIONS	TYP (6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 2.4V for a logic "1" and 0.4V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	MAX	UNIT
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	−10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ / $\overline{PGM}$ = V_{IL})		60	mA
I_{CC}	V_{CC} Supply Current		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = − 4mA)	2.4		V

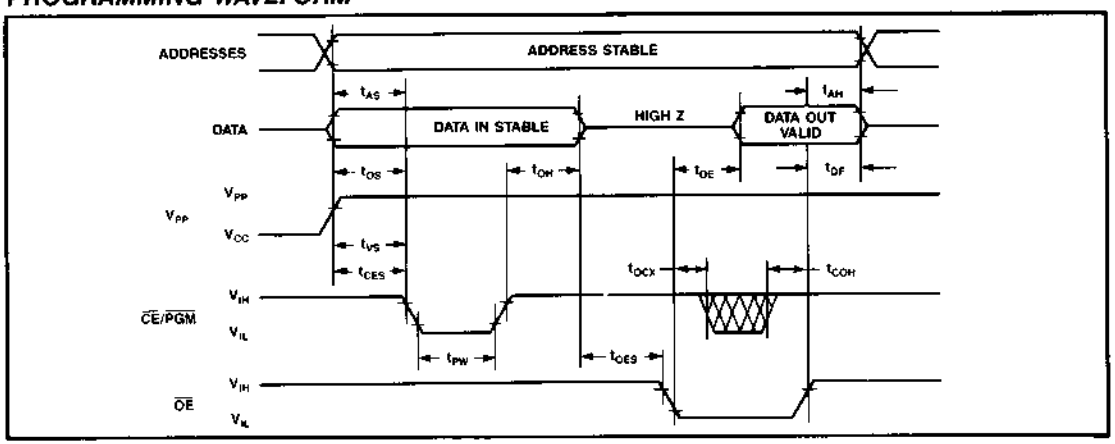
NOTES: 8. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
9. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
10. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{COH}	$\overline{CE}$ High to $\overline{OE}$ High	2			µs
t_{OES}	Output Enable Setup Time	2			µs
t_{OS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{OH}	Data Hold Time	2			µs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid From Output Enable			130	ns
t_{VS}/t_{CES}	V_{PP} Setup Time/$\overline{CE}$ Setup Time	2			µs
t_{PW}	$\overline{PGM}$ Pulse Width	1	3	10	ms
t_{OCX}	$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	2			µs

NOTE: 11. These values are for standard programming — actual programming algorithm may use different limitations.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C256F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C256F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256F-90LMB	90	32 Pin CLDCC	L3	Military	MIL-STD-883C

NOTE: 12. The actual part marking will not include the initials "WS."

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

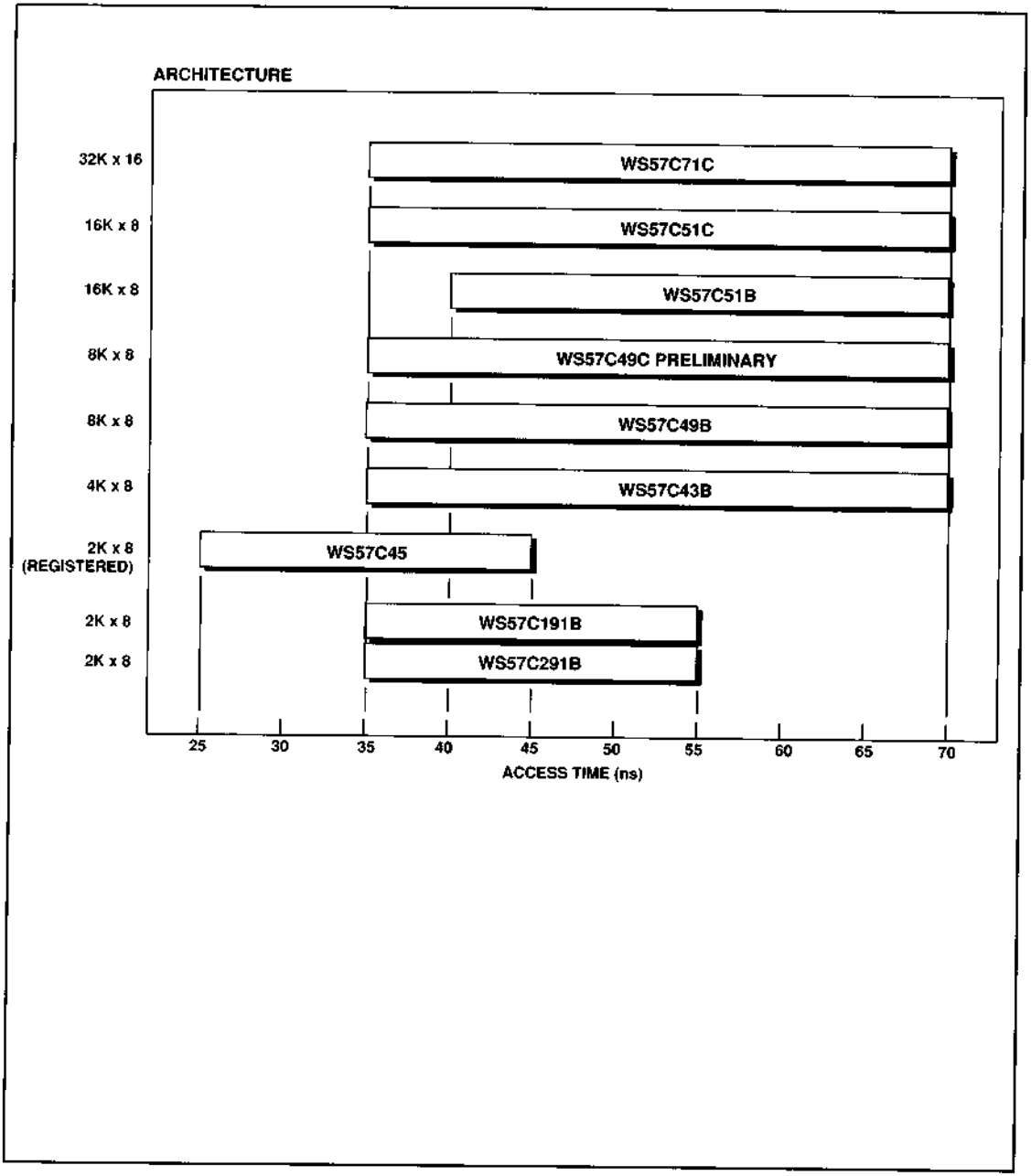
Section Index

PROM/RPROM Memory Products

FAMILY OF HIGH PERFORMANCE CMOS PROMs AND RPROMs

PART NUMBER	PAGE NO.	DENSITY (BITS)	ARCHITECTURE	SPEED (NS)	DRAWING NO.	NO. OF PINS	PACKAGE
WS57C191B	3-5	16K	2K x 8	35 – 55	D1 J3 P2	24 28 24	CERDIP, 0.6" PLDCC Plastic Dip, 0.6"
WS57C291B	3-5	16K	2K x 8	35 – 55	S1 T1	24 24	Plastic Dip, 0.3" CERDIP, 0.3"
WS57C45 (Registered)	3-11	16K	2K x 8	25 – 45	C1 S1 T1	28 24 24	CLLCC Plastic Dip, 0.3" CERDIP, 0.3"
WS57C43B	3-19	32K	4K x 8	35 – 70	D1 J3 S1 T1 Y3	24 28 24 24 24	CERDIP, 0.6" PLDCC Plastic Dip, 0.3" CERDIP, 0.3" CERDIP, 0.3"
WS57C49B	3-25	64K	8K x 8	35 – 70	C1 D1 F1 J3 S1 T1	28 24 24 28 24 24	CLLCC CERDIP, 0.6" Ceramic Flatpack PLDCC Plastic Dip, 0.3" CERDIP, 0.3"
WS57C49C	3-31	64K	8K x 8	35 – 70	C1 D1 F1 J3 L2 S1 T1	28 24 24 28 28 24 24	CLLCC CERDIP, 0.6" Ceramic Flatpack PLDCC CLDCC Plastic Dip, 0.3" CERDIP, 0.3"
WS57C51B	3-37	128K	16K x 8	40 – 70	C2 D2 J4 L3 T2	32 28 32 32 28	CLLCC CERDIP, 0.6" PLDCC CLDCC CERDIP, 0.3"
WS57C51C	3-43	128K	16K x 8	35 – 70	C2 D2 L3 T2	32 28 32 28	CLLCC CERDIP, 0.6" CLDCC CERDIP, 0.3"
WS57C71C	3-49	256K	32K x 8	35 – 70	C2 D2 J4 L3 T2	32 28 32 32 28	CLLCC CERDIP, 0.6" PLDCC CLDCC CERDIP, 0.3"

WSI's Family of High Performance CMOS PROMs and RPROMs (Re-Programmable Read Only Memory) are available in all three operating temperature ranges: Commercial (0 to +70°C), Industrial (–40 to +85°C) and Military (–55 to +125°C). In addition, several versions are available as Standard Military Drawing (SMD) products.


ARCHITECTURE
32K x 16
16K x 8
16K x 8
8K x 8
8K x 8
4K x 8
2K x 8
(REGISTERED)
2K x 8
2K x 8
WS57C71C
WS57C51C
WS57C51B
WS57C49C PRELIMINARY
WS57C49B
WS57C43B
WS57C45
WS57C191B
WS57C291B
25
30
35
40
45
50
55
60
65
70
ACCESS TIME (ns)

AMD	WSI
AM27C49	WS57C49/49B
AM27C191	WS57C291B
AM27C291	WS57C291B
AM27PS43	WS57C43/43B
AM27S43	WS57C43/43B
AM27S43A	WS57C43/43B
AM27S45	WS57C45
AM27S49	WS57C49/49B
AM27S51	WS57C51/51B/51C
AM27S51A	WS57C51/51B/51C
AM27S191	WS57C191B
AM27S291	WS57C291B

ATMEL	WSI
AT27HC191	WS57C191B
AT27HC291	WS57C291B
AT27HC641/2	WS57C49/49B
AT27HC641R/2R	WS57C49/49B

CYPRESS	WSI
CY7C245	WS57C45
CY7C245A	WS57C45
CY7C251	WS57C51/51B/51C
CY7C253	WS57C51/51B/51C
CY7C254	WS57C51/51B/51C
CY7C261	WS57C49/49B
CY7C263	WS57C49/49B
CY7C264	WS57C49/49B
CY7C271	WS57C71C
CY7C291	WS57C291/B
CY7C292	WS57C191/B

EXCEL	WSI
46C16	WS57C291B

FAIRCHILD	WSI
93Z510	WS57C291B
93Z511	WS57C191B
93Z511	WS57C291B
93Z512	WS57C291B
93Z565	WS57C49/49B
93Z667	WS57C49/49B

FUJITSU	WSI
MBH38H	WS57C191B
MBH38-SK	WS57C291B
MB7142	WS57C43/43B
MB7143	WS57C49/49B
MB7144E	WS57C49/49B
MB7144H	WS57C49/49B

GI	WSI
27HC641	WS57C49/49B

HARRIS	WSI
HM-76161	WS57C191B
HM-76641	WS57C49/49B
HM-76641A	WS57C49/49B

HITACHI	WSI
HN25169	WS57C191B
HN25169	WS57C291B

ICT	WSI
27CX321	WS57C43/43B
27CX322	WS57C43/43B
27CX641	WS57C49/49B
27CX642	WS57C49/49B

MMI	WSI
53S3281	WS57C43/43B
63S1681	WS57C191B
63S1681A	WS57C191B
63S1681A	WS57C291B
63S3281	WS57C43/43B
631681	WS57C291B

MOTOROLA	WSI
MCM76	WS57C191B
MCM76160	WS57C291B
MCM76161	WS57C291B

NATIONAL	WSI
87S321	WS57C43/43B
93Z665C	WS57C49/49B
93Z667C	WS57C49/49B
DM77S321	WS57C43/43B
DM87S291	WS57C291B
DM87S291A	WS57C291B
DM87S291B	WS57C291B
DM87S321	WS57C43/43B
DM87SR191	WS57C191B
DM87SR193	WS57C191B

NEC	WSI
27HC65	WS57C49/49B
µPB 429	WS57C191B
µPB 429	WS57C291B

RAYTHEON	WSI
29671	WS57C43/43B
29671A	WS57C43/43B
29681	WS57C291B
29681A	WS57C291B
29683A	WS57C191B
39VP864	WS57C49/49B

SEEQ	WSI
36C16	WS57C191B
36C32	WS57C43/43B
36S16	WS57C291B

SHARP	WSI
LH5749	WS57C49/49B
LH57127	WS57C51/51B/51C
LH57191	WS57C191/B
SH5762	WS57C49/49B

SIGNETICS	WSI
27HC641	WS57C49/49B
27HC642	WS57C49/49B
N82HS321	WS57C43/43B
N82HS641	WS57C49/49B
N82HS1281	WS57C51/51B/51C
N82S191	WS57C191B
N82S191	WS57C291B
N82S191A	WS57C191B
N82S191A	WS57C291B
N82S191B	WS57C191B
N82S191B	WS57C291B
N82S641	WS57C49/49B

SSI	WSI
SS1203	WS57C49/49B

THOMSON	WSI
JBP38S165	WS57C191B
JBP38S165	WS57C291B

TI	WSI
38S165	WS57C191B
38S165	WS57C291B
TMS27C291	WS57C191B
TMS27C292	WS57C291B
TMS27PC49	WS57C49/49B

HIGH SPEED 2K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD Nos. 5962-87650/5962-88734**
- **Pin Compatible with AM27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C191B/291B is an extremely High Performance 16K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts. The WS57C191B/291B is also configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

The WS57C191B is packaged in a conventional 600 mil DIP package as well as a leadless chip carrier. The WS57C291B is packaged in a space saving 300 mil Dip package configuration. Both are available in commercial, industrial, and military operating temperature ranges.

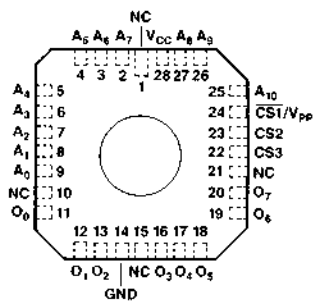
MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	CS2	CS3	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Program	V_{PP}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IL}	V_{CC}	High Z

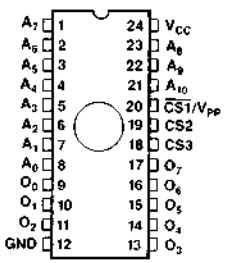
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C191B/291B-35	WS57C191B/291B-45	WS57C191B/291B-55
Address Access Time (Max)	35 ns	45 ns	55 ns
Output Enable Time (Max)	20 ns	20 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		40	mA
			Military		40	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

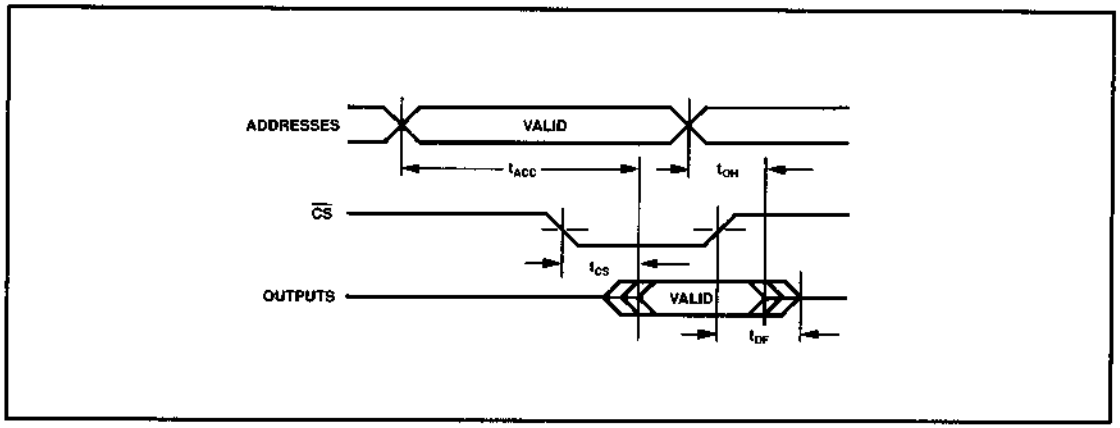
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 3 mA/MHz for A.C. power component
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	191B/291B-35		191B/291B-45		191B/291B-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		20	
Output Disable to Output Float*	t_{DF}		20		20		20	
Address to Output Hold	t_{OH}	0		0		0		

*Sampled, Not 100% Tested

AC READ TIMING DIAGRAM

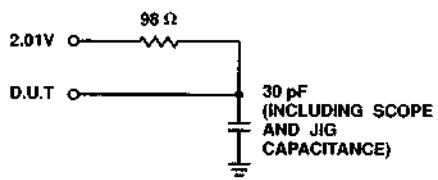


CAPACITANCE (5) T_A = 25°C, f = 1 MHz

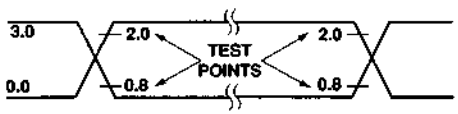
SYMBOL	PARAMETER	CONDITIONS	TYP (6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.5V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	MAX	UNITS
Input Leakage Current ($V_{IN} = V_{CC}$ or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

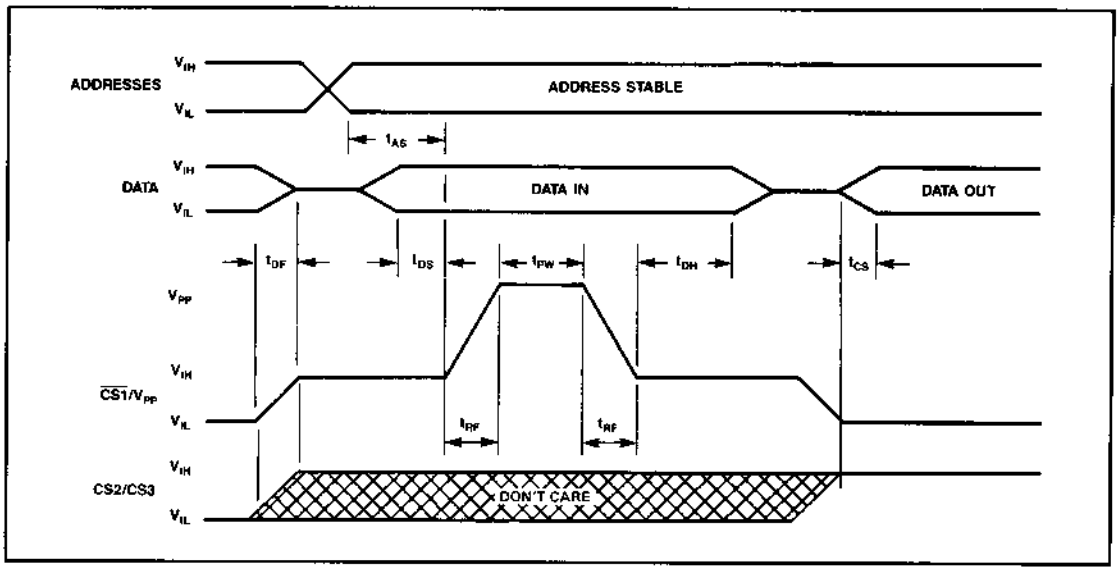
NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}	2		30	ns
Data Setup Time	t_{DS}				µs
Program Pulse Width (Note 7)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 9. For programmers utilizing a one shot programming pulse, a 10 ms pulse width should be used.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191B-35P	35	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191B-45DI	45	24 Pin CERDIP, 0.6"	D1	Industrial	Standard
WS57C191B-45DMB	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C191B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191B-45P	45	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191B-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191B-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C291B-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C291B-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C291B-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH-SPEED 2K × 8 REGISTERED CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 25 ns Setup
  - — 12 ns Clock to Output
- **Low Power Consumption**
- **Fast Programming**
- **Programmable Synchronous or Asynchronous Output Enable**
- **DESC SMD Nos. 5962-88735/5962-87529**
- **Pin Compatible with AM27S45 and CY7C245**
- **Immune to Latch-Up**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**
- **Programmable Asynchronous Initialize Register**

GENERAL DESCRIPTION

The WS57C45 is an extremely HIGH PERFORMANCE 16K UV Erasable Registered CMOS RPROM. It is a direct drop-in replacement for such devices as the AM27S45 and CY7C245.

To meet the requirements of systems which execute and fetch instructions simultaneously, an 8-bit parallel data register has been provided at the output which allows RPROM data to be stored while other data is being addressed.

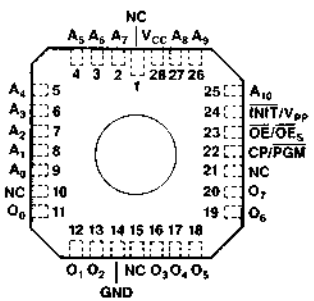
An asynchronous initialization feature has been provided which enables a user programmable 2049th word to be placed on the outputs independent of the system clock. This feature can be used to force an initialize word or provide a preset or clear function.

A further advantage of the WS57C45 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C45 RPROM is 100% tested with worst case test patterns both before and after assembly.

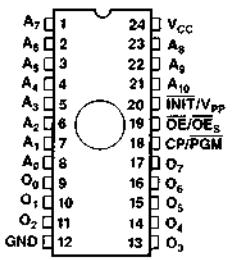
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP/ Flatpack



PRODUCT SELECTION GUIDE

PARAMETER	WS57C45-25	WS57C45-35	WS57C45-45
Set Up Time (Max)	25 ns	35 ns	45 ns
Clock to Output (Max)	12 ns	15 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5 ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3)	Comm'l		20	mA
			Military		30	
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 1 and 3)	Comm'l		25	
			Military		35	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$
3. Add 2 mA/MHz for A.C. power component.
4. This parameter is only sampled and is not 100% tested.

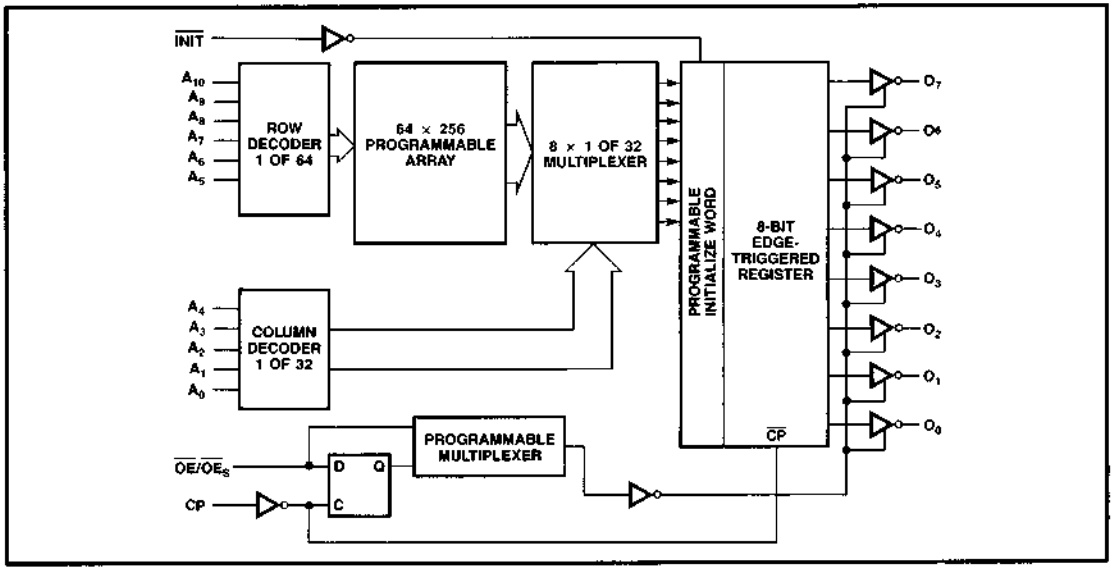
CAPACITANCE[4]

PARAMETERS	DESCRIPTION	TEST CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V	8	

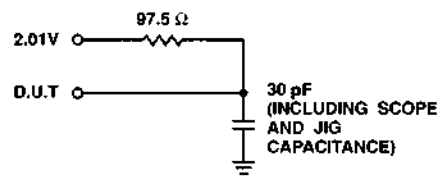
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C45-25		WS57C45-35		WS57C45-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Setup to Clock HIGH	t_{SA}	25		35		45		ns
Address Hold From Clock HIGH	t_{HA}	0		0		0		
Clock HIGH to Valid Output	t_{CO}		12		15		25	
Clock Pulse Width	t_{PWC}	15		20		20		
$\overline{OE}_S$ Setup to Clock HIGH	t_{SOE_S}	12		15		15		
$\overline{OE}_S$ Hold From Clock HIGH	t_{HOE_S}	5		5		5		
Delay From $\overline{INIT}$ to Valid Output	t_{DI}		20		20		35	
$\overline{INIT}$ Recovery to Clock HIGH	t_{RI}	15		20		20		
$\overline{INIT}$ Pulse Width	t_{PWI}	15		20		25		
Active Output From Clock HIGH	t_{LZC}		15		20		30	
Inactive Output From Clock HIGH	t_{HZC}		15		20		30	
Active Output From $\overline{OE}$ LOW	t_{LZOE}		15		20		30	
Inactive Output From $\overline{OE}$ HIGH	t_{HZOE}		15		20		30	

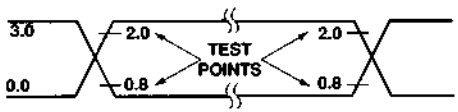
BLOCK DIAGRAM



TEST LOAD (High Impedance Test Systems)

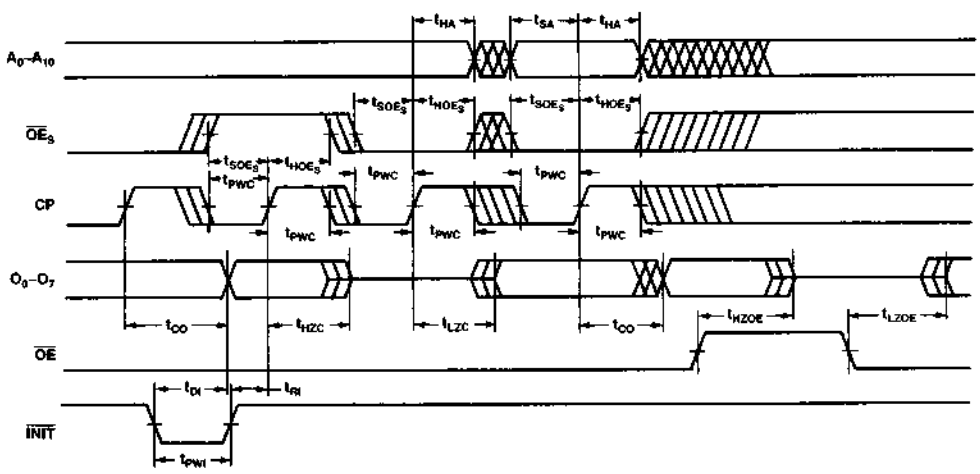


A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

AC READ TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

The WS57C45 is an electrically programmable read only memory produced with WSI's patented high-performance self-aligned split-gate CMOS EPROM technology. It is organized as 2048 × 8 bits and is pin-for-pin compatible with bipolar TTL fuse link PROMs. The WS57C45 includes a D-type 8-bit data register on-chip which reduces the complexity and cost of microprogrammed pipelined systems where PROM data is held temporarily in a register. The circuit features a programmable synchronous ($\overline{OE_S}$) or asynchronous ($\overline{OE}$) output enable and asynchronous initialization ($\overline{INIT}$).

The programmed state of the enable pin ($\overline{OE_S}$ or $\overline{OE}$) will dictate the state of the outputs at power up. If $\overline{OE_S}$ has been programmed, the outputs will be in the OFF or high impedance state. If $\overline{OE}$ has been programmed, the outputs will be OFF or high impedance only if the $\overline{OE}$ input is HIGH. Data is read by applying the address to inputs A_{10}–A_0 and a LOW to the enable input. The data is retrieved and loaded into the master section of the 8-bit data register during the address set-up time. The data is transferred to the slave output of the data register at the next LOW to HIGH clock (CP) transition. Then the output buffers present the data on the outputs (0_7–0_0).

When using the asynchronous enable ($\overline{OE}$), the output buffers may be disabled at any time by switching the enable input to a logic HIGH. They may be re-enabled by switching the enable to a logic LOW.

When using the synchronous enable ($\overline{OE_S}$), the outputs revert to a high impedance or OFF state at the next positive clock edge following the $\overline{OE_S}$ input transition to a HIGH state. The output will revert to the active state following a positive clock edge when the $\overline{OE_S}$ input is at a LOW state. The address and synchronous enable inputs are free to change following a positive clock edge since the output will not change until the next low to high clock transition. This enables accessing the next data location while previously addressed data is present on the outputs.

To avoid race conditions and simplify system timing, the 8-bit edge triggered data register clock is derived directly from the system clock.

The WS57C45 has an asynchronous initialize input ($\overline{INIT}$). This function can be used during power-up and time-out periods to implement functions such as a start address or initialized bus control word. The $\overline{INIT}$ input enables the contents of a 2049th 8-bit word to be loaded directly into the output data register. The $\overline{INIT}$ input can be used to load any 8-bit data pattern into the register since each bit is programmable by the user. When unprogrammed, activating $\overline{INIT}$ will result in clearing the register (outputs LOW). When all bits are programmed, activating $\overline{INIT}$ results in PRESETting the register (outputs HIGH).

When activated LOW, the $\overline{INIT}$ input results in an immediate load of the 2049th word into both the master and slave sections of the output register. This is independent of any other input including the clock (CP) input. The initialize data will be present at the outputs after the asynchronous enable ($\overline{OE}$) is taken to a LOW state.

Programming Information

Apply power to the WS57C45 for normal read mode operation with CP/$\overline{PGM}$, $\overline{OE}$/$\overline{OE_S}$ and $\overline{INIT}$/V_{PP} at V_{IH}. Then take $\overline{INIT}$/V_{PP} to V_{PP}. The part is then in the program inhibit mode operation and the output lines are in a high impedance state. Refer to figure 5. As shown in figure 5, address, program and verify one byte of data. Repeat this sequence for each location to be programmed.

When intelligent programming is used, the program pulse width is 1 ms in length. Each address location is programmed and verified until it verifies correctly up to and including 5 times. After the location verifies, an additional programming pulse should be applied that is X1 times in duration of the sum of the previous programming pulses before proceeding on to the next address and repeating the process.

Initialization Byte Programming

The WS57C45 has a 2049th byte of data that can be used to initialize the value of the data register. This byte contains the value "0" when it is shipped from the factory. The user must program the 2049th byte with a value other than "0" for data register initialization if that value is not desired. Except for the following details, the user may program the 2049th byte in the same manner as the other 2048 bytes. First, since all 2048 addresses are used up, a super voltage address feature is used to enable an additional address. The actual address includes V_{PP} on A_1 and V_{IL} on A_2. Refer to the Mode Selection table. The programming and verification of the Initial Byte is accomplished operationally by performing an initialize function.

Synchronous Enable Programming

The WS57C45 contains both a synchronous and asynchronous enable feature. The part is delivered configured in the asynchronous mode and only requires alteration if the synchronous mode is required. This is accomplished by programming an on-chip EPROM cell. Similar to the Initial Byte, this function is enabled and addressed by using a super voltage. Referring to the Mode Selection table, V_{PP} is applied to A_1 followed by V_{IH} applied to A_2. This procedure addresses the EPROM cell that programs the synchronous enable feature. The EPROM cell is programmed with a 10 ms program pulse on CP/$\overline{PGM}$. It does not require any data since there is no selection as to how synchronous enable may be programmed, only if it is to be programmed.

Synchronous Enable Verification

The WS57C45's synchronous enable function is verified operationally. Apply power for read operation with $\overline{OE}/\overline{OE_S}$ and $\overline{INIT}/V_{PP}$ at V_{IH} and take the clock (CP/$\overline{PGM}$) from V_{IL} to V_{IH}. The output data bus should be in a high impedance state. Next take $\overline{OE}/\overline{OE_S}$ to V_{IL}. The outputs will remain in the high impedance state. Take the clock (CP/$\overline{PGM}$) from V_{IL} to V_{IH} and the outputs will now contain the data that is present. Take $\overline{OE}/\overline{OE_S}$ to V_{IH}. The output should remain driven. Clocking CP/$\overline{PGM}$ once more from V_{IL} to V_{IH} should place the outputs again in a high impedance state.

Blank Check

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C45 has all 2048 bytes in the '0' state. "1's" are loaded into the WS57C45 through the procedure of programming.

MODE SELECTION

MODE	READ OR OUTPUT DISABLE	PIN FUNCTION					OUTPUTS
		A_2	CP/$\overline{PGM}$	$(\overline{OE}/\overline{OE_S})/\overline{VFY}$	$\overline{INIT}/V_{PP}$	A_1	
Read[6]		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable		X	X	V_{IH}	V_{IH}	X	High Z
Program[5,7]		X	V_{IL}	V_{IH}	V_{PP}	X	Data In
Program Verify[5,7]		X	V_{IH}	V_{IL}	V_{PP}	X	Data Out
Program Inhibit[5,7]		X	V_{IH}	V_{IH}	V_{PP}	X	High Z
Intelligent Program[5,7]		X	V_{IL}	V_{IH}	V_{PP}	X	Data In
Program Synch Enable[7]		V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{PP}	High Z
Program Initial Byte[7]		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{PP}	Data In
Initial Byte Read		X	X	V_{IL}	V_{IL}	X	Data Out

NOTES:

5. X = Don't care but not to exceed V_{PP}.
6. During read operation, the output latches are loaded on a "0" to "1" transition of CP
7. During programming and verification, all unspecified pins to be at V_{IL}.

FIGURE 5. PROM PROGRAMMING WAVEFORMS

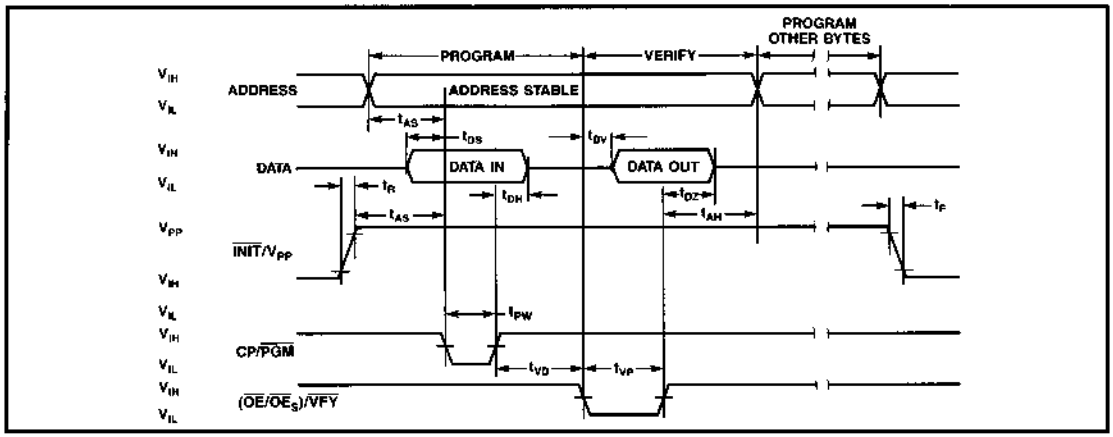


FIGURE 6. INITIAL BYTE PROGRAMMING WAVEFORMS

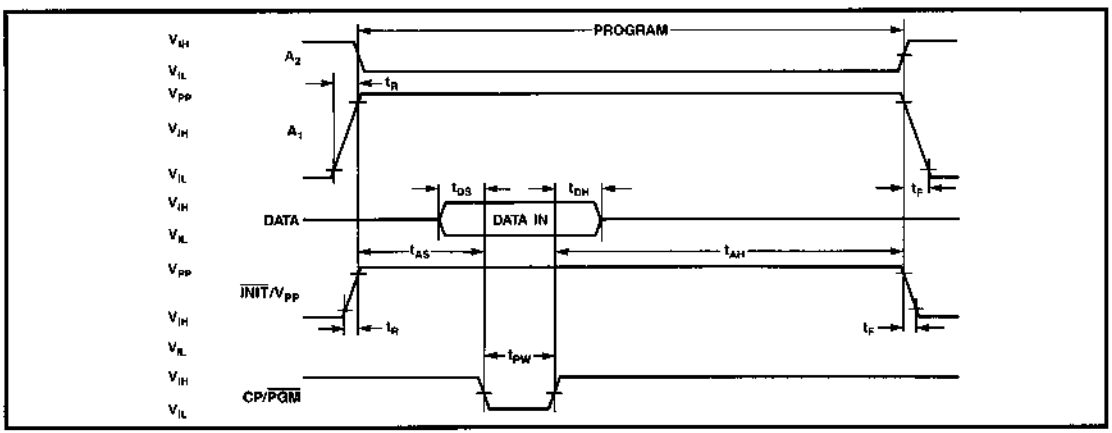
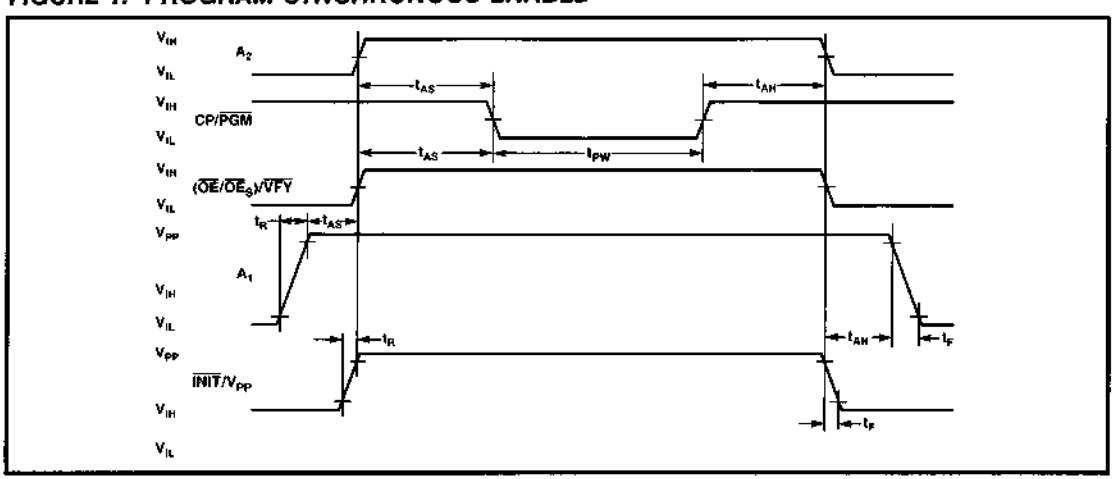


FIGURE 7. PROGRAM SYNCHRONOUS ENABLE



PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Voltage	V_{IL}	−0.1	0.8	V
Input High Voltage	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{PW}	Programming Pulse Width	0.1	10	ms
t_{AS}	Address Setup Time	1.0		µs
t_{DS}	Data Setup Time	1.0		µs
t_{AH}	Address Hold Time	1.0		µs
t_{DH}	Data Hold Time	1.0		µs
t_R, t_F	V_{PP} Rise and Fall Time	1.0		µs
t_{VD}	Delay to $\overline{VFY}$	1.0		µs
t_{VP}	$\overline{VFY}$ Pulse Width	2.0		µs
t_{DV}	$\overline{VFY}$ Data Valid		1.0	µs
t_{DZ}	$\overline{VFY}$ HIGH to High Z		1.0	µs

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C45-25T	25	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-35CMB	35	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C45-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C45-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-35TMB	35	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C45-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C45-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 4K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with AM27S43 and N82S321 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **Available in 300 Mil Dip**

GENERAL DESCRIPTION

The WS57C43B is an extremely HIGH PERFORMANCE 32K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C43B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C43B is 100% tested with worst case test patterns both before and after assembly.

The WS57C43B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs. It also uses the same programming algorithm as its predecessor the WS57C43.

3

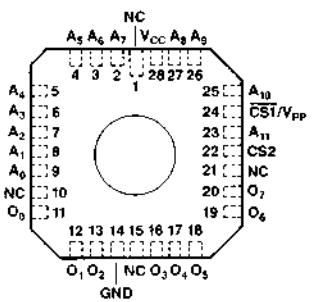
MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	CS2	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	V_{CC}	High Z
Output Disable	X	V_{IL}	V_{CC}	High Z
Program	V_{PP}	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{CC}	D_{OUT}

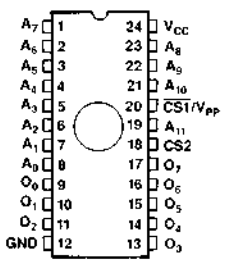
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C43B-35	WS57C43B-45	WS57C43B-55	WS57C43B-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		30	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Military		40	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

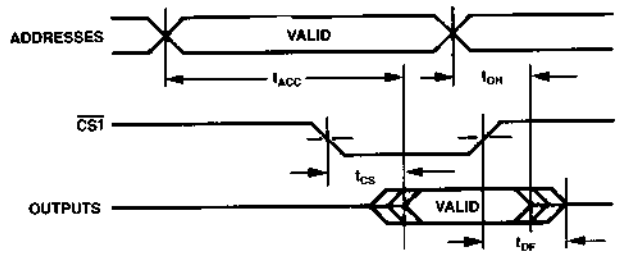
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \le 0.8V$, $V_{IH} \ge 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C43B-35		57C43B-45		57C43B-55		57C43B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		25		25		25	
Output Disable to Output Float*	t_{DF}		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested

AC READ TIMING DIAGRAM

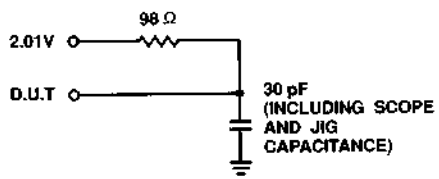


CAPACITANCE (5) T_A = 25°C, f = 1 MHz

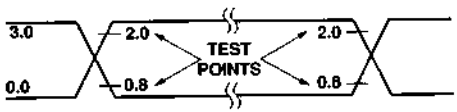
SYMBOL	PARAMETER	CONDITIONS	TYP (6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNITS
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 & 3)	I_{CC}		30	mA
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

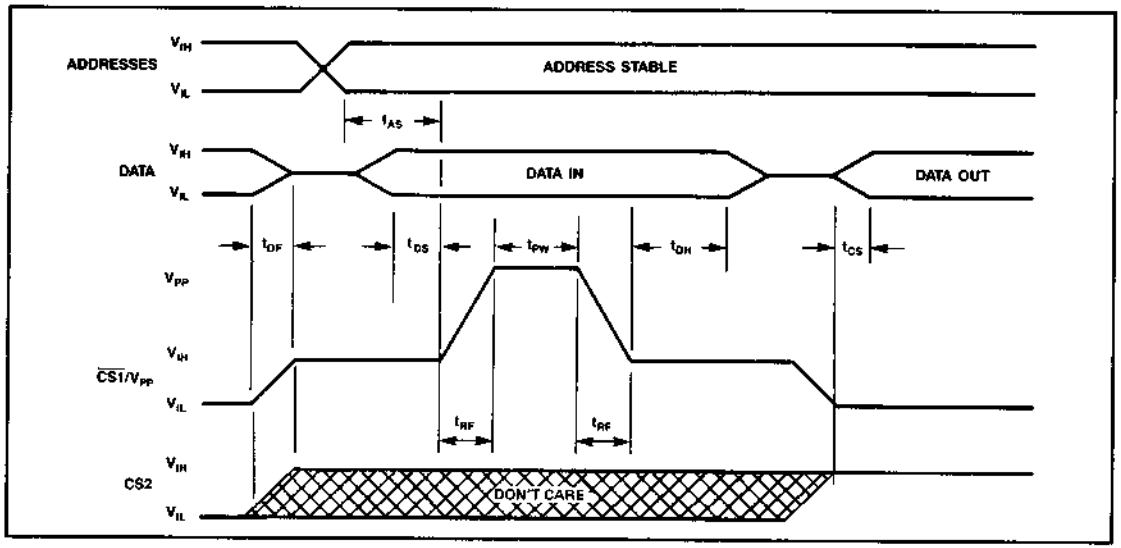
NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 9. A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C43B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43B-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C43B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C43B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C43B-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C43B-45Y	45	24 Pin CERDIP, 0.6"	Y3	Comm'l	Standard
WS57C43B-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43B-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C43B-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-70TMB	70	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 8K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD 5962-87515**
- **Pin Compatible with Am27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-UP**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

Note: Not recommended for new designs after December 15, 1991. Use the improved WS57C49C for new designs.

GENERAL DESCRIPTION

The WS57C49B is a High Performance 64K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C49B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS5749B is 100% tested with worst case test patterns both before and after assembly.

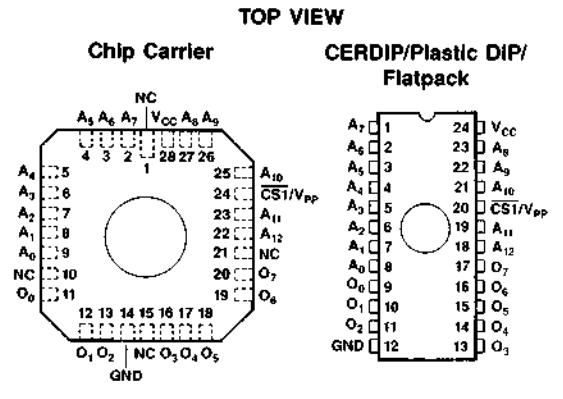
A unique feature of the WS57C49B is a designed-in output hold from address change. This enables the WS57C49B to be run at a cycle time equal to the address access time. While addresses are changing, output data is held long enough to be latched into external circuitry.

The WS57C49B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C49B-35	WS57C49B-45	WS57C49B-55	WS57C49B-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Military		40	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

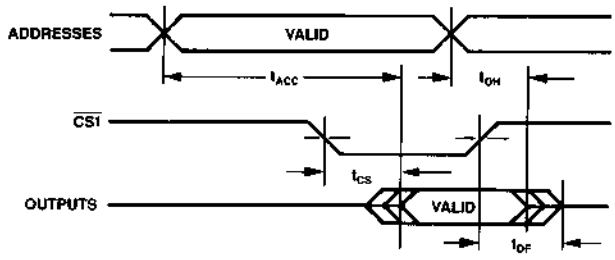
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C49B-35		57C49B-45		57C49B-55		57C49B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS1}$ to Output Delay	t_{CS}		20		25		25		25	
Output Disable to Output Float*	t_{DF}		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested

AC READ TIMING DIAGRAM

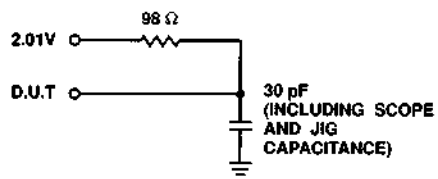


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

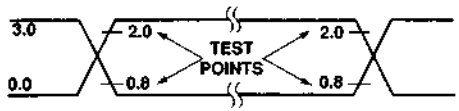
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNITS
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		35	mA
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

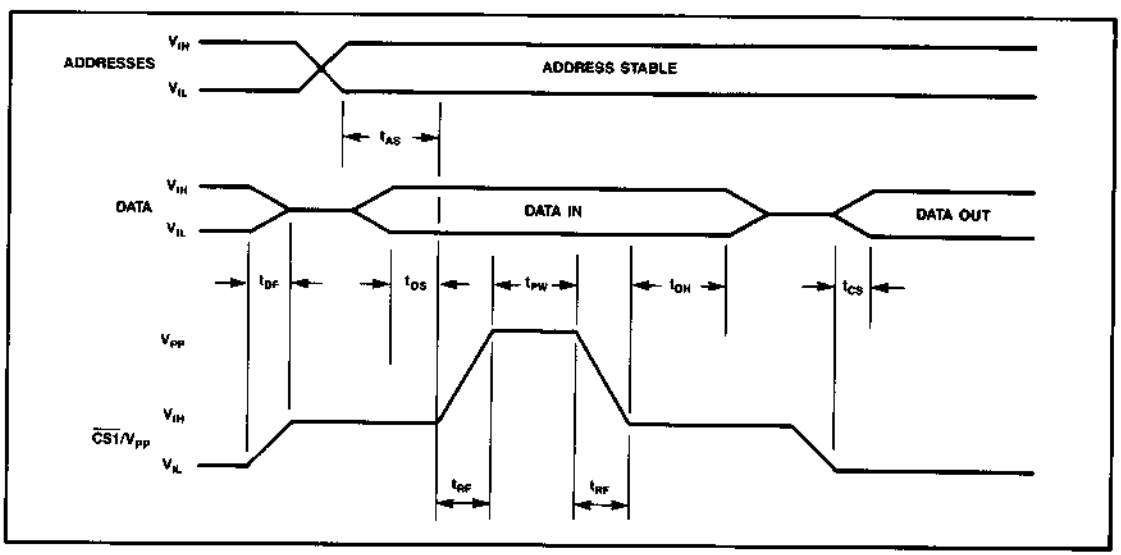
NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 9. A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-45DMB	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C49B-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49B-55CMB	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49B-55FMB	55	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C49B-55J	55	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-55S	55	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49B-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49B-70CMB	70	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-70T	70	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-70TMB	70	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

Note: Not recommended for new designs after December 15, 1991.
Use the Improved WS57C49C for new designs.

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 8K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD 5962-87515**
- **Pin Compatible with Am27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-UP**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C49C is a High Performance 64K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which enables it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C49C over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functinality after assembly. Unlike devices which cannot be erased, every WS5749C is 100% tested with worst case test patterns both before and after assembly.

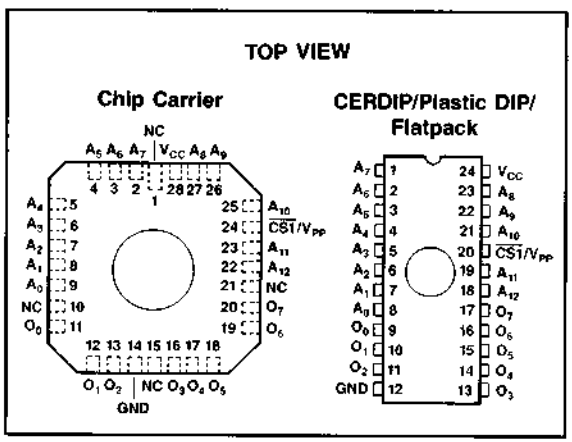
A unique feature of the WS57C49C is a designed-in output hold from address change. This enables the WS57C49C to be run at a cycle time equal to the address access time. While addresses are changing, output data is held long enough to be latched into external circuitry.

The WS57C49C is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C49C-35	WS57C49C-45	WS57C49C-55	WS57C49C-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +13V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 10%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 1)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 1)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		30	mA
			Industrial		35	
			Military		35	
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 3 and 4) Outputs Not Loaded	Comm'l		40	mA
			Industrial		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

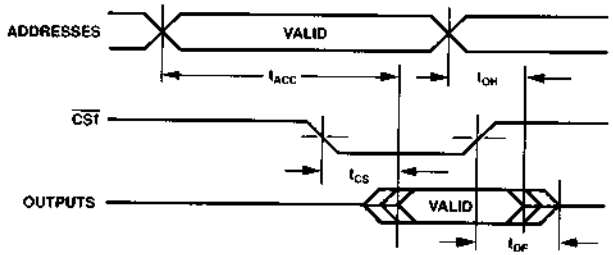
NOTES:
1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
4. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C49C-35		57C49C-45		57C49C-55		57C49C-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS1}$ to Output Delay	t_{CS}		20		25		25		25	
Output Disable to Output Float*	t_{DF}		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM

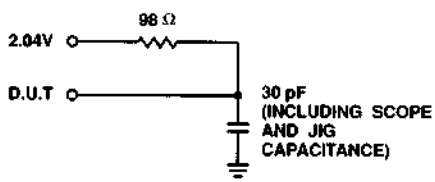


CAPACITANCE (5) T_A = 25°C, f = 1 MHz

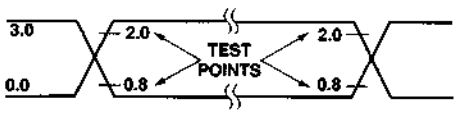
SYMBOL	PARAMETER	CONDITIONS	TYPE (6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	MAX	UNITS
I_{LI}	Input Leakage Current (V_{IN} = V_{CC} or Gnd)	–10	10	µA
I_{PP}	V_{PP} Supply Current During Programming Pulse		60	mA
I_{CC}	V_{CC} Supply Current		35	mA
V_{OL}	Output Low Voltage During Verify (I_{OL} = 16 mA)		0.45	V
V_{OH}	Output High Voltage During Verify (I_{OH} = – 4mA)	2.4		V

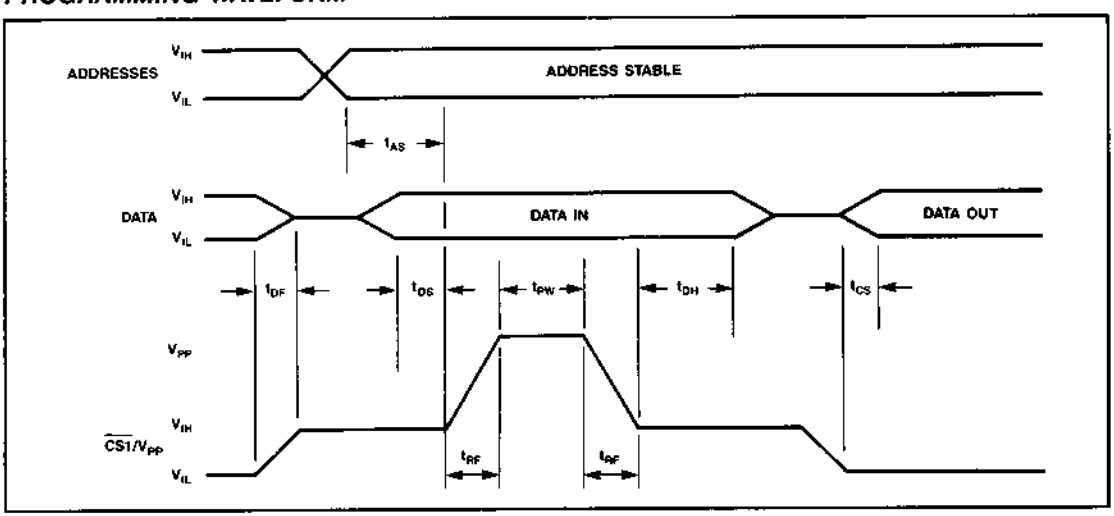
NOTE: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

SYMBOLS	PARAMETER	MIN	TYP	MAX	UNITS
t_{AS}	Address Setup Time	2			µs
t_{DF}	Chip Disable Setup Time			30	ns
t_{DS}	Data Setup Time	2			µs
t_{PW}	Program Pulse Width	1	3	10	ms
t_{DH}	Data Hold Time	2			µs
t_{CS}	Chip Select Delay			30	ns
t_{RF}	V_{PP} Rise and Fall Time	1			µs

NOTE: 9. Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49C-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49C-35L	35	28 Pin CLDCC	L2	Comm'l	Standard
WS57C49C-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49C-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49C-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-45DMB	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49C-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49C-45L	45	28 Pin CLDCC	L2	Comm'l	Standard
WS57C49C-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49C-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C49C-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49C-55CMB	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49C-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49C-55FMB	55	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C49C-55J	55	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49C-55S	55	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49C-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49C-70CMB	70	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49C-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49C-70T	70	28 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49C-70TMB	70	28 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

3

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 16K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 40 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with AM27S51**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

Note: Not recommended for new designs after September 1, 1991. Use the improved WS57C51C for new designs.

GENERAL DESCRIPTION

The WS57C51B is a High Performance 128K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C51B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C51B is 100% tested with worst case test patterns both before and after assembly.

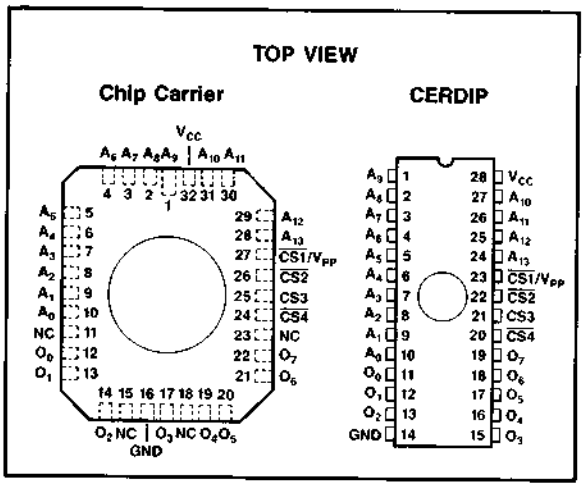
The WS57C51B provides a low power alternative to those designs which are committed to a Bipolar PROM footprint. It is a direct drop-in replacement for a Bipolar PROM of the same architecture (16K x 8). No software, hardware or layout changes need be performed.

3

MODE SELECTION

PINS / MODE	$\overline{CS1}$/V_{PP}	$\overline{CS2}$	CS3	$\overline{CS4}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	X	V_{CC}	High Z
Output Disable	X	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	X	V_{IL}	X	V_{CC}	High Z
Output Disable	X	X	X	V_{IH}	V_{CC}	High Z
Program	V_{PP}	X	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C51B-40	WS57C51B-45	WS57C51B-55	WS57C51B-70
Address Access Time (Max)	40 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	20 ns	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		40	mA
			Military		40	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

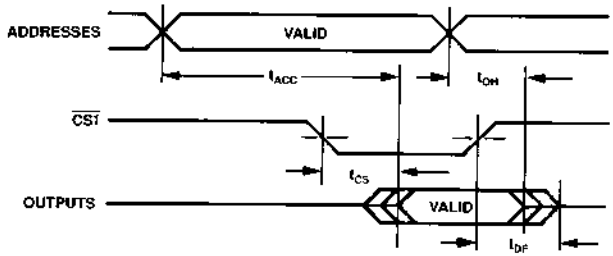
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C51B-40		WS57C51B-45		WS57C51B-55		WS57C51B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		40		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		25		30	
Output Disable to Output Float*	t_{DF}		20		20		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested

AC READ TIMING DIAGRAM

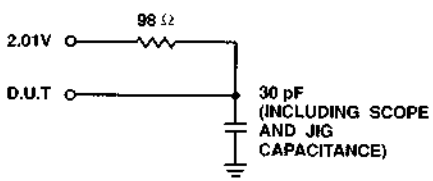


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

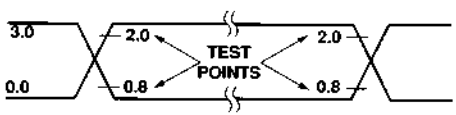
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNITS
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

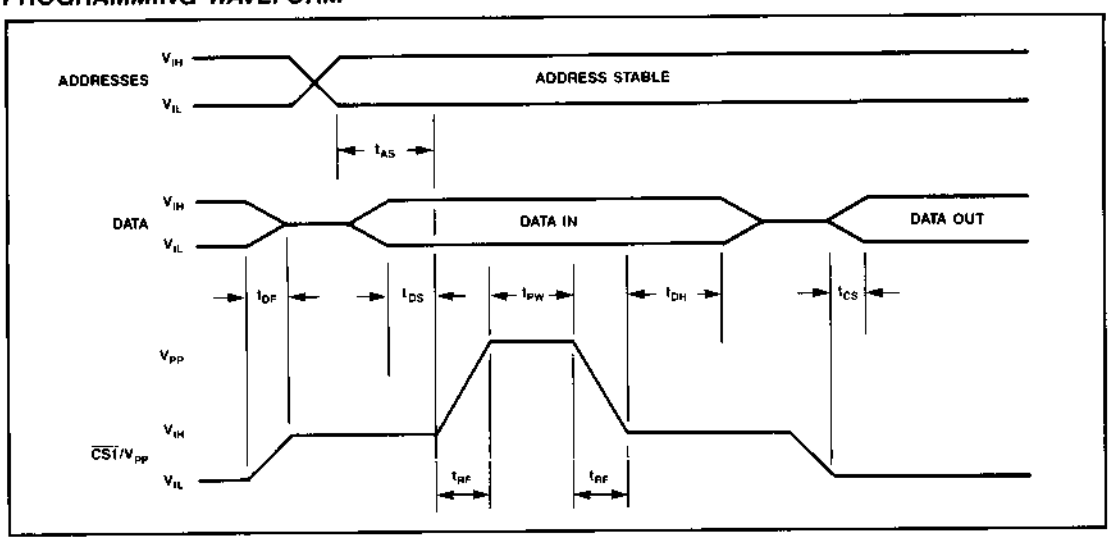
NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width (Note 7)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 9. A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C51B-40D	40	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51B-40L	40	32 Pin CLDCC	L3	Comm'l	Standard
WS57C51B-40T	40	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51B-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51B-45DI	45	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C51B-45DMB	45	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C51B-45J	45	32 Pin PLDCC	J4	Comm'l	Standard
WS57C51B-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C51B-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51B-45TI	45	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C51B-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51B-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51B-55DI	55	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C51B-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C51B-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C51B-55LMB	55	32 Pin CLDCC	L3	Military	MIL-STD-883C
WS57C51B-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51B-55TI	55	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C51B-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C51B-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51B-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51B-70DI	70	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C51B-70DMB	70	28 Pin CERDIP, 0.6	D2	Military	MIL-STD-883C
WS57C51B-70J	70	32 Pin PLDCC	J4	Comm'l	Standard
WS57C51B-70JI	70	32 Pin PLDCC	J4	Industrial	Standard
WS57C51B-70LMB	70	32 Pin CLDCC	L3	Military	MIL-STD-883C
WS57C51B-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51B-70TI	70	28 Pin CERDIP, 0.3"	T2	Industrial	Standard

Note: Not recommended for new designs after September 1, 1991.
Use the Improved WS57C51C for new designs.

3

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 16K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with Am27S51 and N82HS1281**
- **Immune to Latch-UP**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C51C is a High Performance 128K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C51C over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C51C in a windowed package is 100% tested with worst case test patterns both before and after assembly.

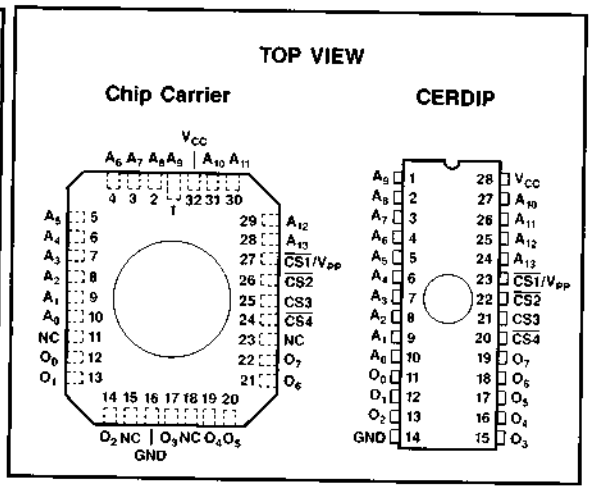
The WS57C51C provides a low power alternative to those designs which are committed to a Bipolar PROM footprint. It is a direct drop-in replacement for a Bipolar PROM of the same architecture (16K x 8). No software, hardware or layout changes need be performed.

3

MODE SELECTION

PINS / MODE	$\overline{CS1}$/V_{PP}	$\overline{CS2}$	CS3	$\overline{CS4}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	X	V_{CC}	High Z
Output Disable	X	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	X	V_{IL}	X	V_{CC}	High Z
Output Disable	X	X	X	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{IH}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	57C51C-35	57C51C-40	57C51C-45	57C51C-55	57C51C-70
Address Access Time (Max)	35 ns	40 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	20 ns	20 ns	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 4)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 4)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 1 and 3) Outputs Not Loaded	Comm'l		30	mA
			Military		35	mA
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 2 and 3) Outputs Not Loaded	Comm'l		50	mA
			Military		60	mA
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

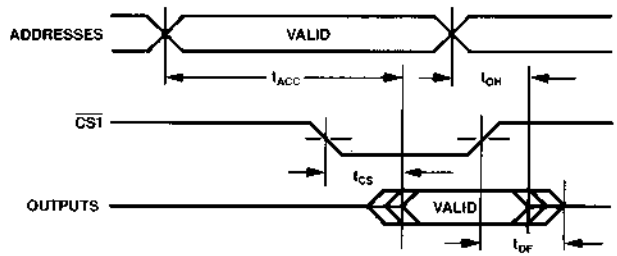
NOTES:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 4 mA/MHz for A.C. power component.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C51C-35		57C51C-40		57C51C-45		57C51C-55		57C51C-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		40		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		20		25		30	
Output Disable to Output Float*	t_{DF}		20		20		20		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		0		

*Sampled, Not 100% Tested

AC READ TIMING DIAGRAM

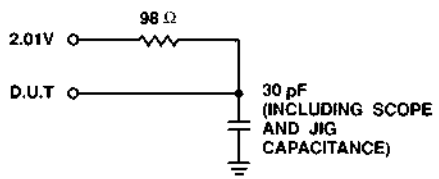


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

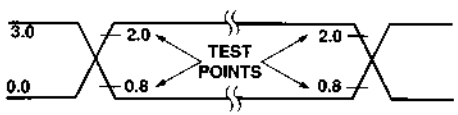
SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.5V \pm 5\%$, $V_{PP} = 12.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	MAX	UNITS
Input Leakage Current ($V_{IN} = V_{CC}$ or Gnd)	I_{LI}	–10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = –4 mA)	V_{OH}	2.4		V

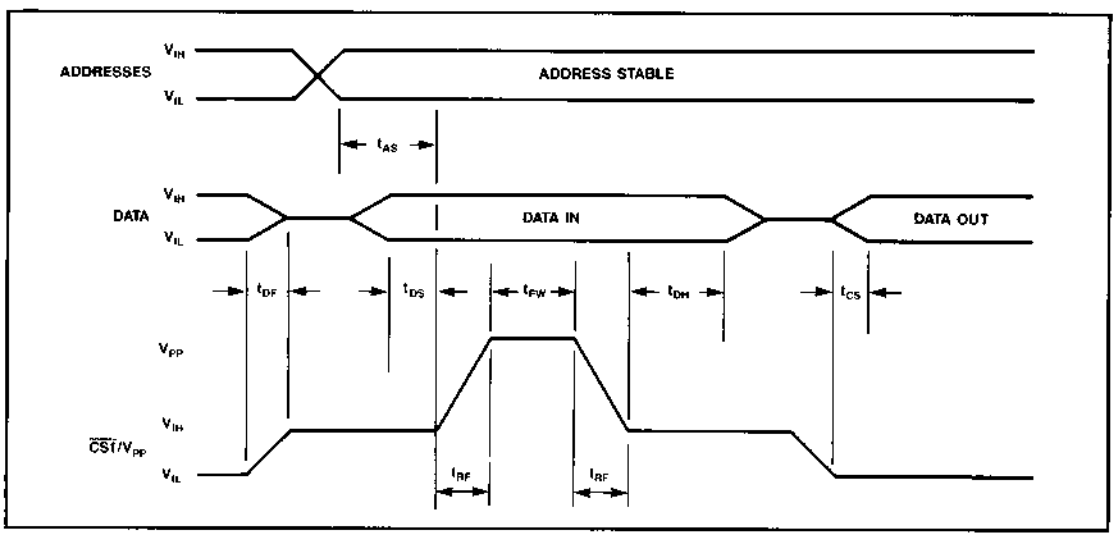
NOTE: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width (Note 7)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 9. A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C51C-35D	35	28 Pin CERDIP,0.6"	D2	Comm'l	Standard
WS57C51C-35T	35	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51C-35TI	35	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C51C-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51C-45J	45	32 Pin PLDCC	J4	Comm'l	Standard
WS57C51C-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C51C-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51C-45TI	45	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C51C-45TMB	45	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C51C-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51C-55D	55	28-Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51C-55DMB	55	28-Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C51C-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C51C-55JI	55	32 Pin PLDCC	J4	Industrial	Standard
WS57C51C-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C51C-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51C-55TI	55	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C51C-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C51C-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51C-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

HIGH SPEED 32K x 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **Immune to Latch-UP**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C71C is a High Performance 256K UV Erasable Electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology and utilizes WSI's patented self-aligned split gate EPROM cell.

The industry standard PROM pin configuration of the WS57C71C provides an easy upgrade path from a 16K x 8 device as well as providing a future upgrade path to 64K x 8 and 128K x 8 devices.

This RPROM is capable of operating at speeds as fast as 35 ns address access time, which enables it to be used directly with today's fast microprocessors and DSP processors without introducing any wait states. All inputs and outputs are TTL compatible. The WS57C71C is a low power device even when operated at its fastest speed. The DIP version is packaged in a 300 mil wide DIP package saving board space for the user.

3

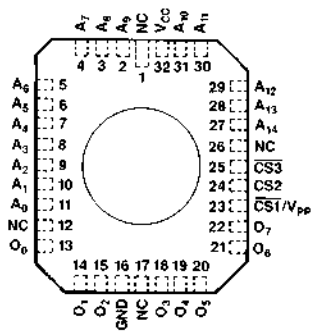
MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	CS2	$\overline{CS3}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Output Disable	X	X	V_{IH}	V_{CC}	High Z
Program	V_{PP}	X	V_{IH}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Program Inhibit	V_{PP}	X	V_{IL}	V_{CC}	High Z

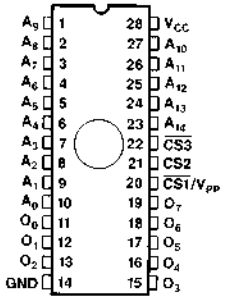
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP



NOTE:
J-Package (PLDCC) only: Pins No. 1 and 17 are common and tied to the die attach pad. They must therefore be D.U. (don't use or float) or tied to GND.

PRODUCT SELECTION GUIDE

PARAMETER	WS57C71C-35	WS57C71C-45	WS57C71C-55	WS57C71C-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	20 ns	20 ns	30 ns

NOTE: Shaded area describes product available Q4 '91.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +13V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Voltage	(Note 1)		−0.1	0.8	V
V_{IH}	Input High Voltage	(Note 1)		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{CC1}	V_{CC} Active Current (CMOS)	(Notes 2 and 4) Outputs Not Loaded	Comm'l		20	mA
			Industrial		25	
			Military		25	
I_{CC2}	V_{CC} Active Current (TTL)	(Notes 3 and 4) Outputs Not Loaded	Comm'l		50	mA
			Industrial		60	
			Military		60	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5 V or Gnd		−10	10	µA

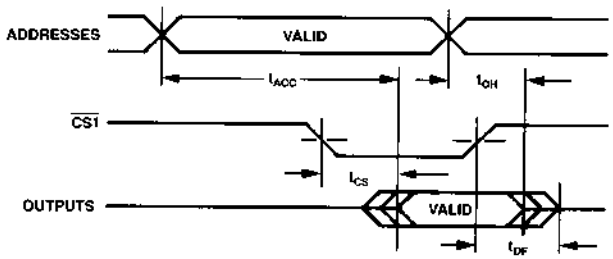
NOTES:
1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
3. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
4. Add 4 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C71C-35		57C71C-45		57C71C-55		57C71C-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		20		30	
Output Disable to Output Float*	t_{DF}		20		20		20		25	
Address to Output Hold	t_{OH}	0		0		0		0		

*Sampled, Not 100% Tested.

AC READ TIMING DIAGRAM

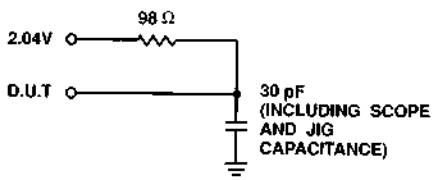


CAPACITANCE (5) T_A = 25°C, f = 1 MHz

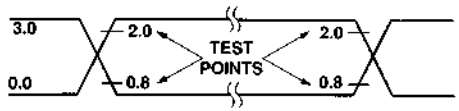
SYMBOL	PARAMETER	CONDITIONS	TYP (6)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5.This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS



A.C testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

NOTE: 7. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 1.0 microfarad capacitor in parallel with a 0.1 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNITS
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	–10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = –4 mA)	V_{OH}	2.4		V

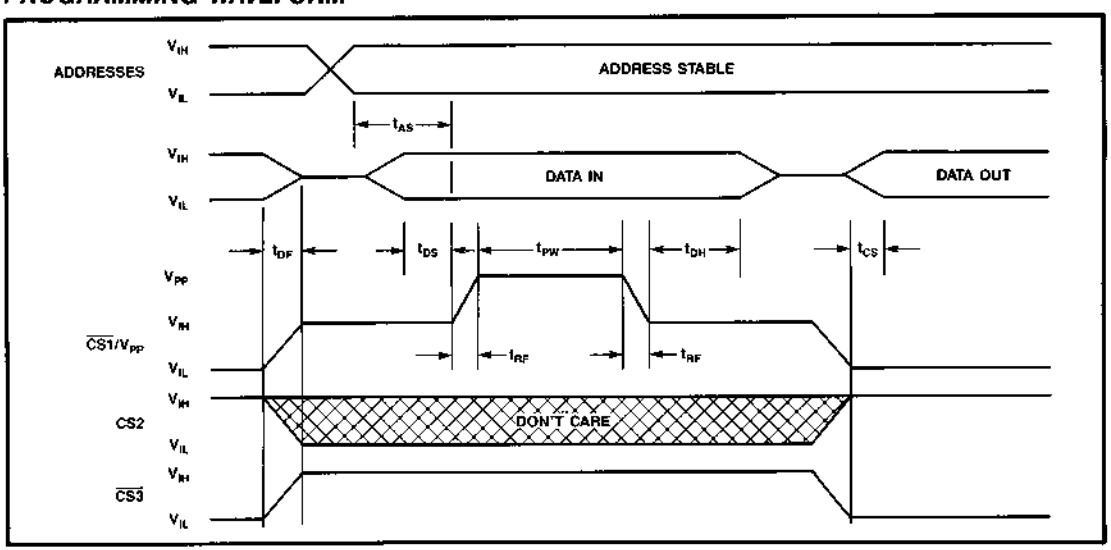
NOTES: 8. V_{PP} must not be greater than 13 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 9. Single shot programming algorithms should use one 10 ms pulse.

PROGRAMMING WAVEFORM



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C71C-35J	35	32 Pin PLDCC	J4	Comm'l	Standard
WS57C71C-35L	35	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-35T	35	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C71C-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-55J	55	32 Pin PLDCC	J4	Comm'l	Standard
WS57C71C-55JI	55	32 Pin PLDCC	J4	Industrial	Standard
WS57C71C-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-55TI	55	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
WS57C71C-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C71C-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-70J	70	32 Pin PLDCC	J4	Comm'l	Standard
WS57C71C-70L	70	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-70TMB	70	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C

NOTE: Shaded area describes product available Q4 '91.

PROGRAMMING/ERASURE/PROGRAMMERS

REFER TO PAGE 4-1

PROGRAMMING/ERASURE/ PROGRAMMERS

PROGRAMMING

Upon delivery from WSI or after erasure, the EPROM has all bits in the "1" or high state. "0's" are loaded into the device through the procedure of programming.

Programming is performed by raising V_{CC} to 5.5V, disabling the outputs, raising V_{PP} to its appropriate programming voltage (12.5 or 13.5 Volts), enabling chip enable, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a programming pulse $\overline{PGM}$. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the EPROM to an ultra-violet light source. A dosage of 15W second/cm² is required to completely erase an EPROM. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm² from 15 to 20 minutes. The EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that EPROMs and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase an EPROM and exposure to these light sources should be prevented to realize maximum system reliability. If used in such an environment, the EPROM package window should be covered by an opaque label or substance.

PROGRAMMERS

WSI's MagicPro™ IBM PC compatible engineering programmer and several commercially available engineering and production programmers support the WSI EPROM product family. A reference chart of Data I/O programmers follows.

WS6000

MagicPro™ Memory and Programmable Peripheral Programmer

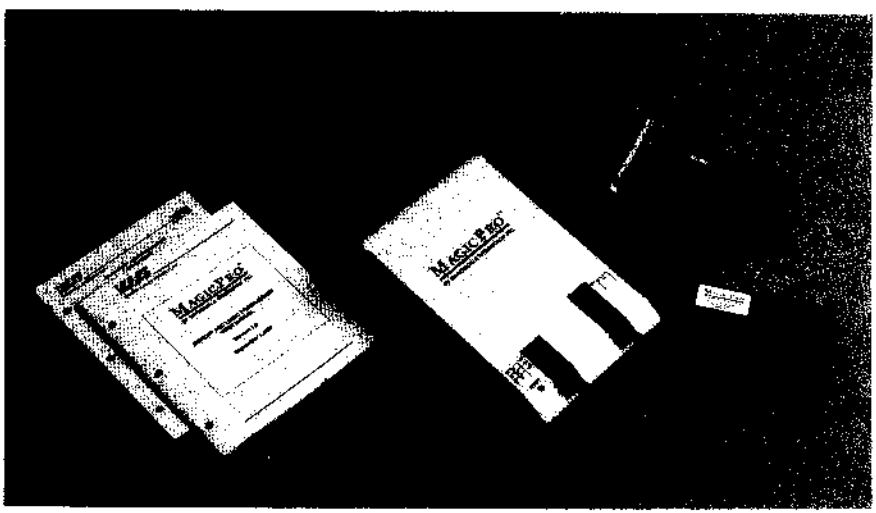
Key Features

- ❑ Programs All WSI CMOS Memory and and Programmable Peripheral Products and All Future Programmable Products
- ❑ Programs 24, 28, 32 and 40 Pin Standard 600 Mil or Slim 300 Mil Dip Packages without Adaptors
- ❑ Programs LCC, PGA and QFP Packaged Product by Using Adaptors
- ❑ Easy-to-Use Menu-Driven Software
- ❑ Compatible with IBM PC/XT/AT Family of Computers (and True Plug-Compatible

General Description

MagicPro is an engineering development tool designed to program existing WSI EPROMs, RPROMs, Programmable Peripherals, and future WSI programmable products. It is used within the IBM-PC® and compatible computers. The MagicPro is meant to bridge the gap betweeen the introduction of a new WSI programmable product and the availability of programming support from programmer manufacturers (e.g., Data I/O, etc.). The MagicPro programmer and accompanying software enable quick programming of newly released WSI programmable products, thus accelerating the system design process.

The MagicPro plug-in board is integrated easily into the IBM-PC. It occupies a short expansion slot and its software requires only 256K bytes of computer memory. The two external ZIF-Dip sockets in the Remote Socket Adaptor (RSA) support 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil Dip packages without adaptors. LCC, PGA and QFP packages are supported using adaptors.



General Description (Cont.)

Many features of the MagicPro Programmer show its capabilities in supporting WSI's future products. Some of these are:

- ❑ 24 to 40 pin JEDEC Dip Pinouts
- ❑ 1 Meg Address Space (20 address lines)
- ❑ 16 Data I/O Lines

The MagicPro menu driven software makes using different features of the MagicPro an easy task. Software updates are done via floppy disk which eliminates the need for adding a new memory device for system upgrading. Please call 800-TEAM-WSI for information regarding programming WSI products not listed herein. The MagicPro reads Intel Hex format for use with assemblers and compilers.

MagicPro Commands

- ❑ Help
- ❑ Upload RAM from Device
- ❑ Load RAM from Disk
- ❑ Write RAM to Disk
- ❑ Display RAM Data
- ❑ Edit RAM
- ❑ Move/Copy RAM
- ❑ Fill RAM
- ❑ Blank Test Device
- ❑ Verify Device
- ❑ Program Device
- ❑ Select Device
- ❑ Configuration
- ❑ Quit MagicPro

Technical Information

- ❑ ***Size:***
  IBM-PC Short Length Card
- ❑ ***Port Address Location:***
  100H to 1FFH – default 140H (if a conflict exists with this address space, the address location can be changed in software and with the switches on the plug-in board.)
- ❑ ***System Memory Requirements:***
  256K Bytes of RAM
- ❑ ***Power:***
  + 5 Volts, 0.03 Amp; +12 Volts, 0.04 Amp
- ❑ ***Remote Socket Adaptor (RSA):***
  The RSA contains two ZIF-Dip sockets that are used to program and read WSI programmable products. The 32 pin ZIF-Dip socket supports 24, 28 and 32 pin standard 600 mil or slim 300 mil Dip packaged product. The 40 pin ZIF-Dip socket supports all 40 pin Dip packages. Adaptor sockets are available for LCC, PGA and QFP packages.

Ordering Information

The WS6000 MagicPro Systems Contains:

- ❑ MagicPro IBM-PC Plug-in Programmer Board
- ❑ MagicPro Remote Socket Adaptor and Cable
- ❑ MagicPro Operating System Floppy Disk and Operating Manual

The WS6000 MagicPro Adaptors Include:

- ❑ WS6001 28-Pin CLLCC Package Adaptor for Memory.
- ❑ WS6008 28-Pin 0.3" Wide Dip Adaptor for SAM448
- ❑ WS6009 28-Pin PLDCC/CLDCC/ CLLCC Package Adaptor for SAM448
- ❑ WS6010 88-Pin PGA Package Adaptor for PAC1000
- ❑ WS6012 32-Pin CLDCC Package Adaptor for Memory
- ❑ WS6013 100-Pin QFP Package Adaptor for PAC1000
- ❑ WS6014 44-Pin CLDCC/PLDCC Package Adaptor for MAP168 and PSD3XX
- ❑ WS6015 44-Pin PGA Package Adaptor for MAP168 and PSD3XX
- ❑ WS6016 44-Pin CLDCC/PLDCC Package Adaptor for Memory
- ❑ WS6020 52-Pin PQFP Package Adaptor for PSD3XX
- ❑ WS6021 44-Pin CLDCC/PLDCC Package Adaptor for PSD3XX

DATA I/O PROGRAMMING SUPPORT

All WSI memory products program easily on standard commercially available EPROM programmers. Manufacturers of these EPROM programmers offer a broad range of products which cover prototyping through high volume production requirements. The table below covers that portion of Data I/O's and WSI's product line which supports WSI's programmable products. For more information regarding programming support for WSI products call toll-free 800-TEAM WSI (800-832-6974) or 800-451-5970 (CA).

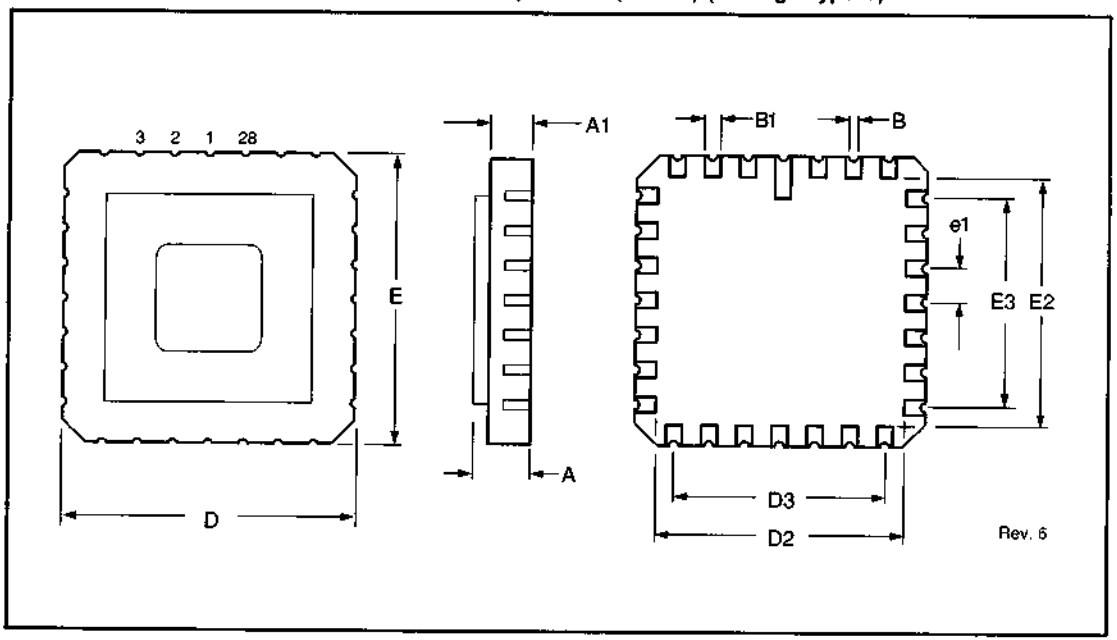
DATA I/O AND MagicPro™ REFERENCE FOR HIGH PERFORMANCE EPROMs

Device	Package	Pins	Family/ Pinout Code	Unisite Site 40	Unisite Site 48	Unisite Chipsite	Unisite Pinsite	2900	29B Unipak 2B	Unipak 2B 351B	212	S1000	Handler Site	Unisite Setsite	29B Gang-Pack	288	288A	Board Site	WSI's MagicPro
57C64F	DIP	28	3C/33	V2.0	V2.0	–	–	V1.3	V12	086	V1.1	V01	V2.0	V2.0	V07	V2.0	V4.1	V02	Rev.4.02
57C64F	LCC	32	3C/C1	–	–	V2.4	V3.0	V1.3	V17	099	–	–	–	–	–	–	–	V02	Rev.4.02
27C64F	DIP	28	3C/33	V2.0	V2.0	–	–	V1.0	V12	086	V1.1	V07	V2.0	V2.0	–	V2.0	V4.1	V02	Rev.4.02
27C64F	LCC	32	3C/–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	V02	Rev.4.02
57C128F	DIP	28	3C/51	V2.5	V2.5	–	–	V1.3	V12	086	V1.1	V01	V2.5	V2.8	–	V2.0	V4.1	V02	Rev.4.02
57C128FB	CONSULT FACTORY																		
27C128F	DIP	28	3C/51	V2.0	V2.0	–	–	V1.0	V12	086	V1.1	V07	V2.0	V2.0	V07	V2.0	V4.1	V02	Rev.4.02
27C128F	LCC	32	3C/C2	–	–	V2.4	V3.0	V1.3	V17	099	–	–	–	–	–	–	–	V02	Rev.4.02
57C256F	DIP	28	124/032	V2.4	V2.4	–	–	V1.3	V17	086	–	–	V2.4	–	–	V5.0	V5.0	V02	Rev.4.02
27C256F	DIP	28	124/032	V2.4	V2.4	–	–	V1.0	V17	086	–	–	V2.4	V3.0	–	–	–	V02	Rev.4.02
27C256F	LCC	32	124/0C9	–	–	V2.4	V3.0	V1.2	V17	099	–	–	–	–	–	–	–	V02	Rev.4.02

DEVICE	PKG TYPE	FAMILY/ PINOUT CODE	29B UNIPAK 2B	S1000	UNISITE	UNISITE MODULE	2900	SETSITE	GANG PACK	288	289	212	BOARD SITE
57C191	DIP	7B/21	V12	V12	V2.0	SITE40/48	V1.3	V2.0	V07	V4.1	V1.0	V1.1	V02
	LCC	7B/8B	–	–	V2.8/V3.0	CHIPSITE/PINSITE	V1.3	–	–	–	–	–	V02
57C191B	DIP	7B/21	V17	V13	V2.5	SITE40/48	V1.3	V2.8	–	V4.1	V1.0	–	V04.1
	PLCC	7B/8B	V18	–	V2.5/V3.0	CHIPSITE/PINSITE	V1.3	–	–	–	–	–	V02
57C291	DIP	7B/21	V12	–	V2.5	SITE 40/48	V1.3	V2.8	V08	V4.1	V1.0	V1.1	V02
	LCC	7B/-	–	–	–	–	–	–	–	–	–	–	V02
57C291B	DIP	7B/21	V17	–	–	–	–	–	–	V4.1	V1.0	–	V02
57C291BT	DIP	7B/21	V19	–	V2.5	SITE40/48	–	–	–	–	–	–	–
57C43	DIP	7B/63	V12	V12	V2.0	SITE40/48	–	V2.0	V07	V4.1	–	–	V02
	LCC	7B/-	–	–	–	–	–	–	–	–	–	–	V02
57C43B	DIP	7B/63	V17	V13	V2.5	SITE40/48	V1.3	V2.5	–	V4.1	V1.0	–	V02
	PLCC	7B/8E	V18	–	V2.5/V3.0	CHIPSITE/PINSITE	V1.3	–	–	–	–	–	V02
57C43BT	DIP	7B/63	V19	V17	V2.5	SITE40/48	V1.3	–	–	–	–	–	–
57C45	DIP	122/0B0	V17	–	V2.7	SITE40/48	V1.2	–	–	–	–	–	–
	LCC	122/153	–	–	V2.8/V3.0	CHIPSITE/PINSITE	V1.2	–	–	–	–	–	–
57C45T	DIP	122/0B0	V19	–	–	–	–	–	–	–	–	–	–
57C49	DIP	3C/67	V12	–	–	–	–	–	V07	–	–	–	–
	DIP	7B/67	–	–	V2.0	SITE40/48	V1.3	V2.0	–	V4.1	V1.0	V1.1	V02
	DIP	F3C/067	–	V12	–	–	–	–	–	–	–	–	–
	LCC	7B/9A	–	–	V2.5/V3.0	CHIPSITE/PINSITE	–	–	–	–	–	–	V02
57C49B	DIP	3C/67	V17	–	–	–	–	–	–	–	–	–	–
	DIP	7B/67	–	–	V2.5	SITE40/48	V1.3	V2.8	–	V4.1	V1.0	–	V02
	DIP	F3C/067	–	V13	–	–	–	–	–	–	–	–	–
	PLCC	3C/9A	V18	–	–	–	–	–	–	–	–	–	–
	PLCC	7B/9A	–	–	V2.5/V3.0	CHIPSITE/PINSITE	V1.3	–	–	–	–	–	V02
	LCC	7B/9A	–	–	V2.5/V3.0	CHIPSITE/PINSITE	V1.3	–	–	–	–	–	V02
	FP	7B/-	–	–	–	–	–	–	–	–	–	–	V02
57C49BT	DIP	3C/67	V19	–	–	–	–	–	–	–	–	–	–
	DIP	7B/67	–	–	V2.5	SITE40/48	V1.3	–	–	–	–	–	–
	DIP	F3C/067	–	V17	–	–	–	–	–	–	–	–	–
57C49C	DIP	12D/067	V18	V13	–	–	V1.3	–	–	–	–	–	V04.3
57C51	DIP	7B/78	V13	–	V2.0	SITE40/48	–	V2.0	–	V4.1	V1.0	V1.1	V04.1
	DIP	F7B/078	–	V12	–	–	–	–	–	–	–	–	–
	PLCC	7B/-	–	–	–	–	–	–	–	–	–	–	V02
57C51B	DIP	7B/78	V17	–	V2.5	SITE40/48	V1.3	V3.0	–	V4.1	V1.0	–	V02
	DIP	F7B/078	–	V13	–	–	–	–	–	–	–	–	–
	LCC	07B/123	–	–	V2.5/V3.0	CHIPSITE/PINSITE	V1.3	–	–	–	–	–	–
	LCC	7B/-	–	–	–	–	–	–	–	–	–	–	V02
57C51BT	DIP	7B/78	V19	–	V2.5	SITE40/48	V1.3	V2.5	–	–	–	–	–
	DIP	F7B/078	–	V17	–	–	–	–	–	–	–	–	–
57C51C	DIP	12D/078	V18	–	V3.4[4]	SITE40/48	V1.5[4]	–	–	–	–	–	V04.3
	DIP	12D/F78	–	V20	–	–	–	–	–	–	–	–	V04.3
57C71C	DIP	12D/169	–	–	V3.0	SITE40/48	V1.3[4]	–	–	–	–	–	–

NOTES: 1. Site 40/48 is the standard DIP socket on the UNISITE.
2. CHIPSITE is the PLCC module on the UNISITE. This has to be purchased if needed.
3. PINSITE will be the PGA module on the UNISITE. This has to be purchased if needed.
4. Contact Data I/O Bulletin Board for the latest programming information.

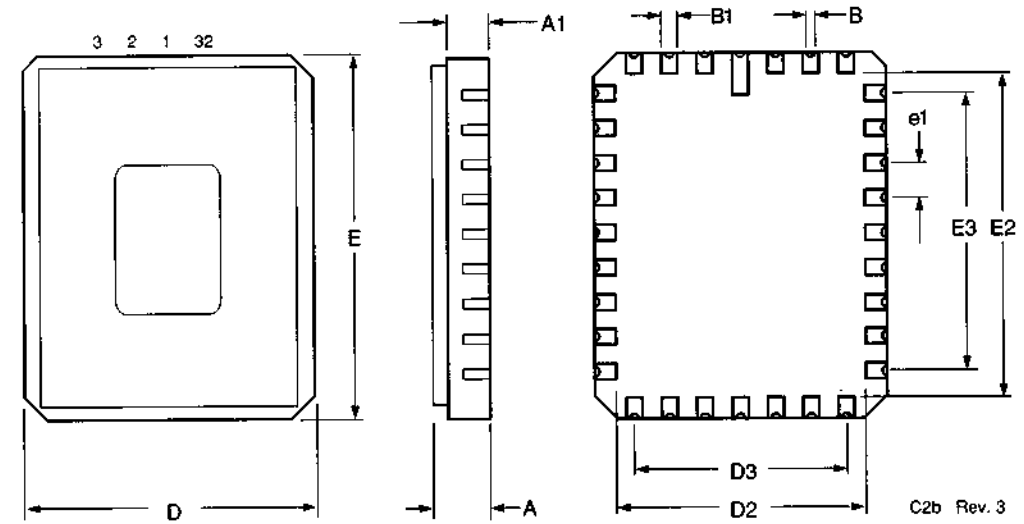
DRAWING C1 28 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



Family: Ceramic Leadless Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.41	3.30		0.095	0.130	
A1	1.52	1.96		0.060	0.077	
B	0.41		Typical Dia.	0.016		Typical Dia.
B1	0.56	0.71		0.022	0.028	
D	11.23	11.68		0.442	0.460	
D2	8.89		Typical	0.350		Typical
D3	7.62		Reference	0.300		Reference
E	11.30	11.68		0.442	0.460	
E2	8.89		Typical	0.350		Typical
E3	7.62		Reference	0.300		Reference
e1	1.27		Reference	0.050		Reference
N	28			28		

C1

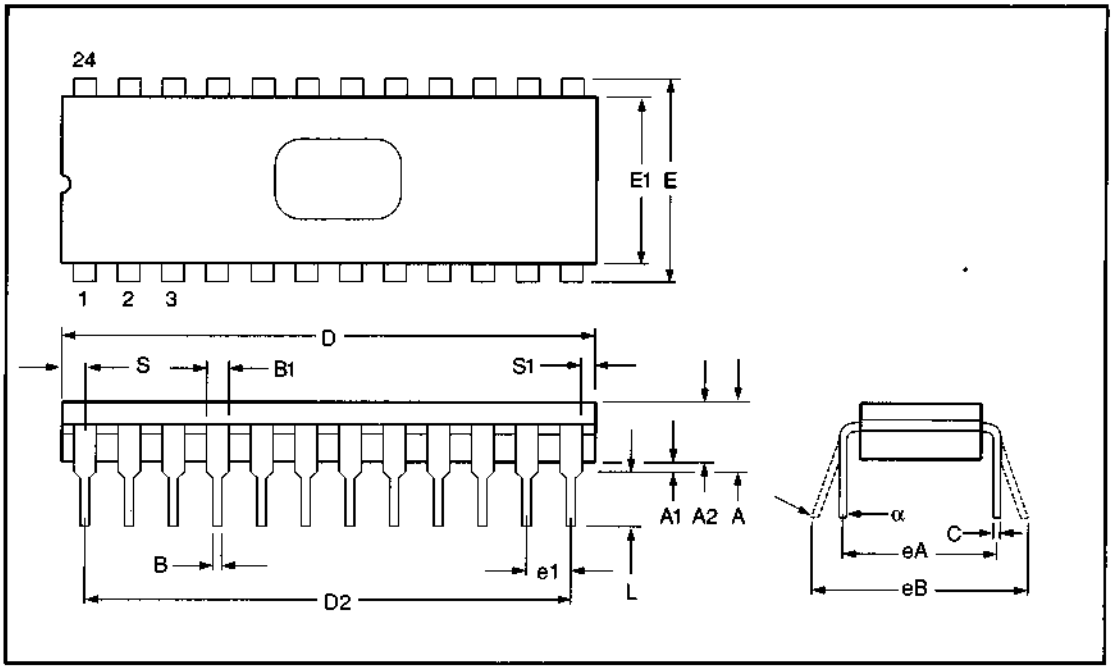
DRAWING C2 32 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



Family: Ceramic Leadless Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	2.41	3.05		0.095	0.120	
A1	1.27	2.03		0.050	0.080	
B	0.41		Typical Dia.	0.016		Typical Dia.
B1	0.56	0.71		0.022	0.028	
D	11.23	11.63		0.442	0.458	
D2	8.89		Typical	0.350		Typical
D3	7.62		Reference	0.300		Reference
E	13.72	14.22		0.540	0.560	
E2	11.43		Typical	0.450		Typical
E3	10.16		Reference	0.400		Reference
e1	1.27		Reference	0.050		Reference
N	32			32		

C2B

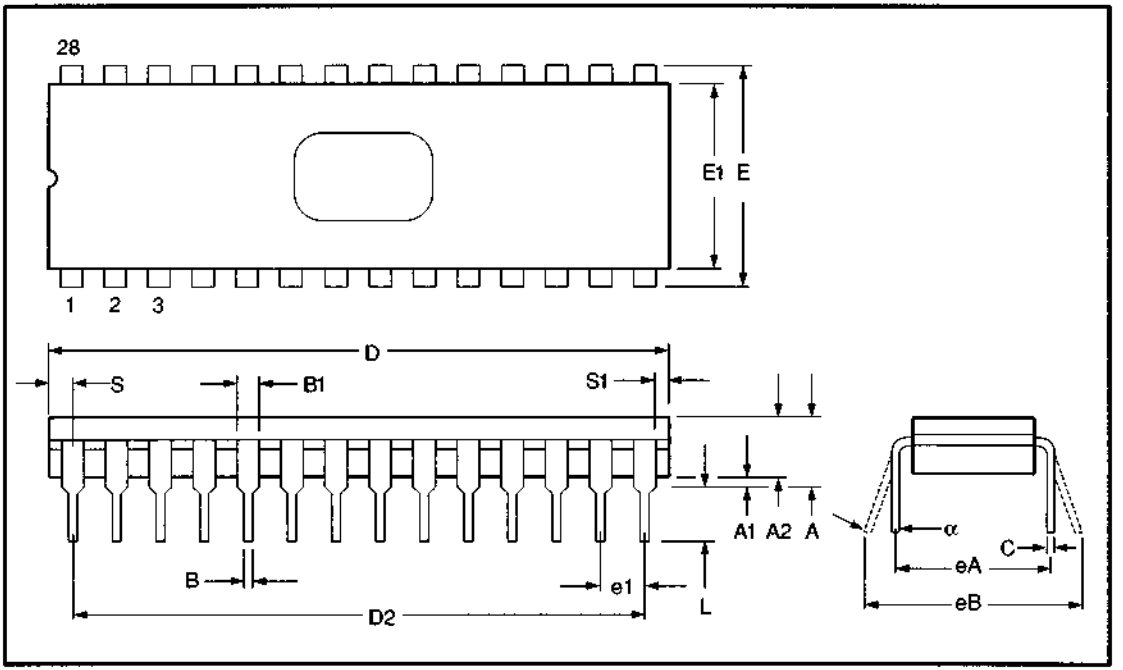
DRAWING D1 24 Pin CERDIP (Package Type D)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.81	5.72		0.150	0.225	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.38	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	31.50	32.77		1.240	1.290	
D2	27.94		Reference	1.100		Reference
E	15.24	15.75		0.600	0.620	
E1	13.08	15.37		0.515	0.605	
e1	2.54		Reference	0.100		Reference
eA	15.49		Reference	0.610		Reference
eB	15.75	17.78		0.620	0.700	
L	3.18	4.70		0.125	0.185	
N	24		600 MIL	24		600 MIL
S	1.40	2.29		0.055	0.090	
S1	0.25	-		0.010	-	

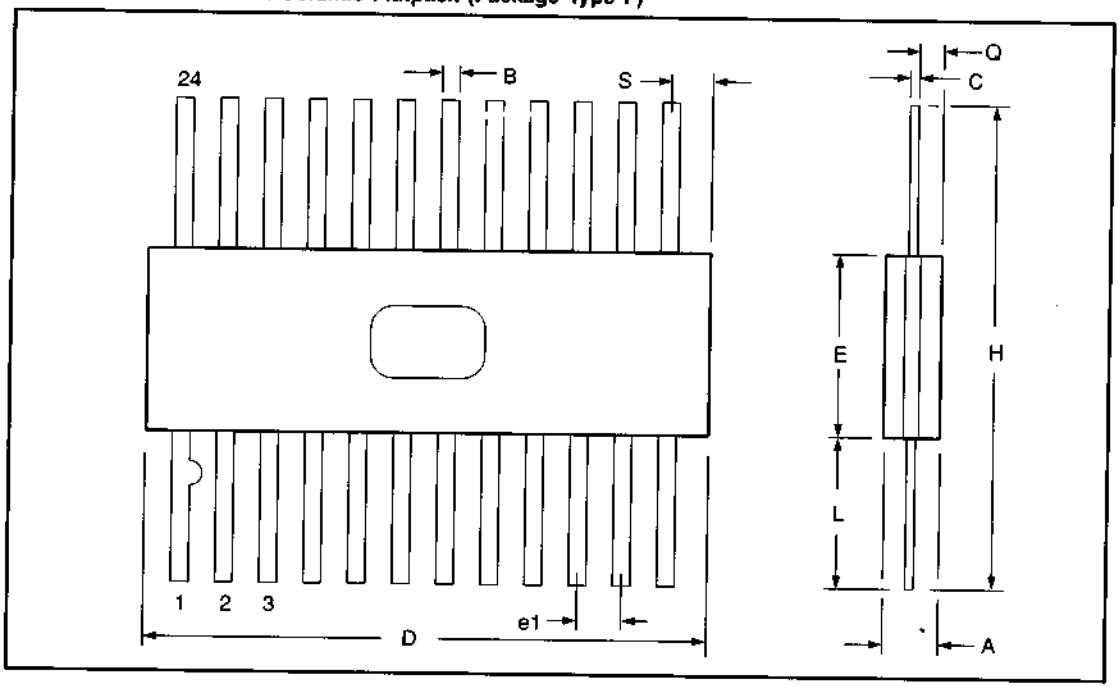
5

DRAWING D2 28 Pin CERDIP (Package Type D)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.81	5.72		0.150	0.225	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.38	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	36.58	37.85		1.440	1.490	
D2	33.02		Reference	1.300		Reference
E	15.24	15.75		0.600	0.620	
E1	13.08	15.37		0.515	0.605	
e1	2.54		Reference	0.100		Reference
eA	15.49		Reference	0.610		Reference
eB	15.75	17.78		0.620	0.700	
L	3.18	4.70		0.125	0.185	
N	28		600 MIL	28		600 MIL
S	1.40	2.29		0.055	0.090	
S1	0.25	-		0.010	-	

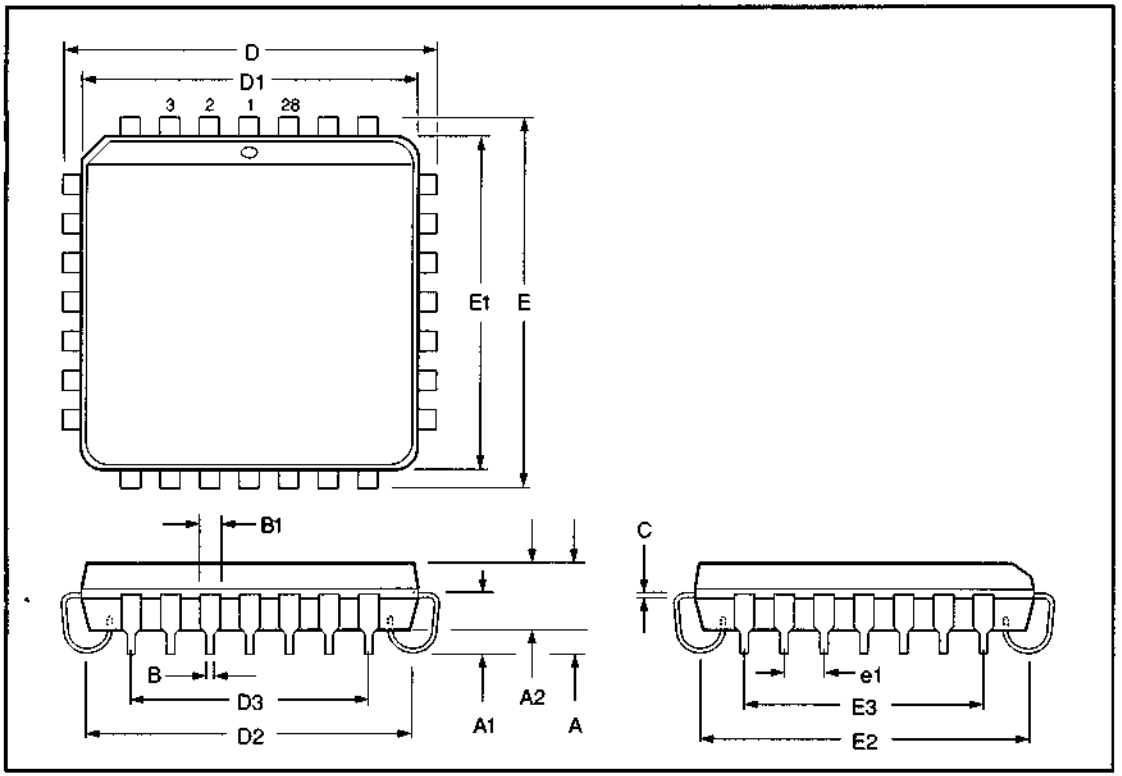
DRAWING F1 24 Pin Ceramic Flatpack (Package Type F)



Family: Ceramic Flatpack						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	1.52	2.29		0.060	0.090	
B	0.38	0.48		0.015	0.019	
C	0.08	0.15		0.003	0.006	
D	14.73	16.26		0.580	0.640	
E	8.64	10.67		0.340	0.420	
e1	1.27		Reference	0.050		Reference
H	22.86	25.40		0.900	1.000	
L	6.35	-		0.250	0.350	
N	24			24		
Q	0.66	1.14		0.026	0.045	
S	-	1.14		-	0.045	

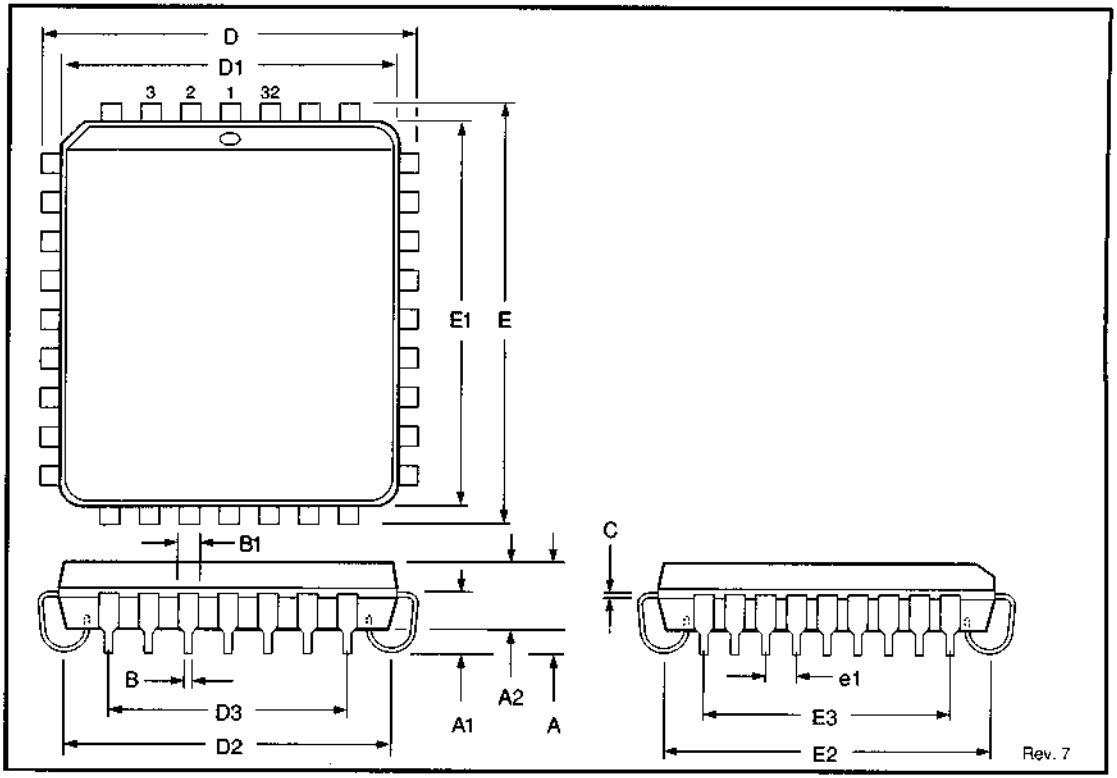
5

DRAWING J3 28 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



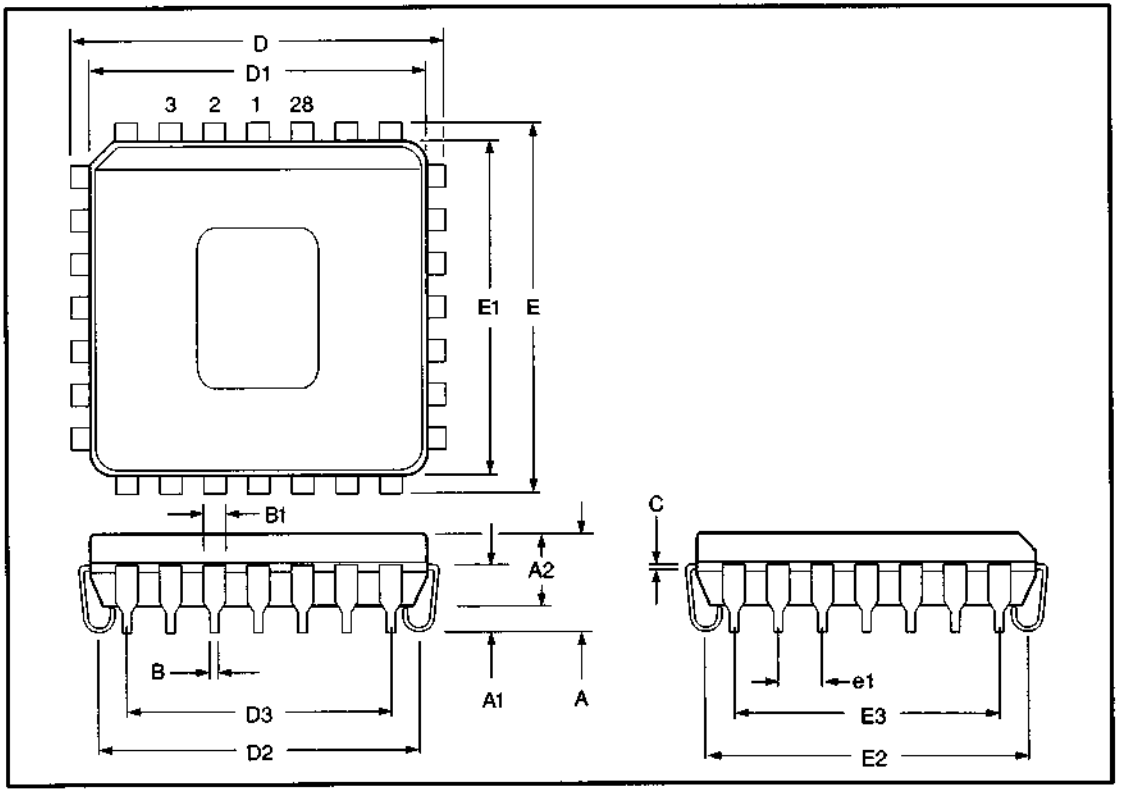
Family: Plastic Leaded Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		0.165	0.180	
A1	2.54	2.79		0.100	0.110	
A2	3.76	3.96		0.148	0.156	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.262		0.0097	0.0103	
D	12.32	12.57		0.485	0.495	
D1	11.43	11.53		0.450	0.454	
D2	9.91	10.92		0.390	0.430	
D3	7.62		Reference	0.300		Reference
E	12.32	12.57		0.485	0.495	
E1	11.43	11.53		0.450	0.454	
E2	9.91	10.92		0.390	0.430	
E3	7.62		Reference	0.300		Reference
e1	1.27		Reference	0.050		Reference
N	28			28		

DRAWING J4 32 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



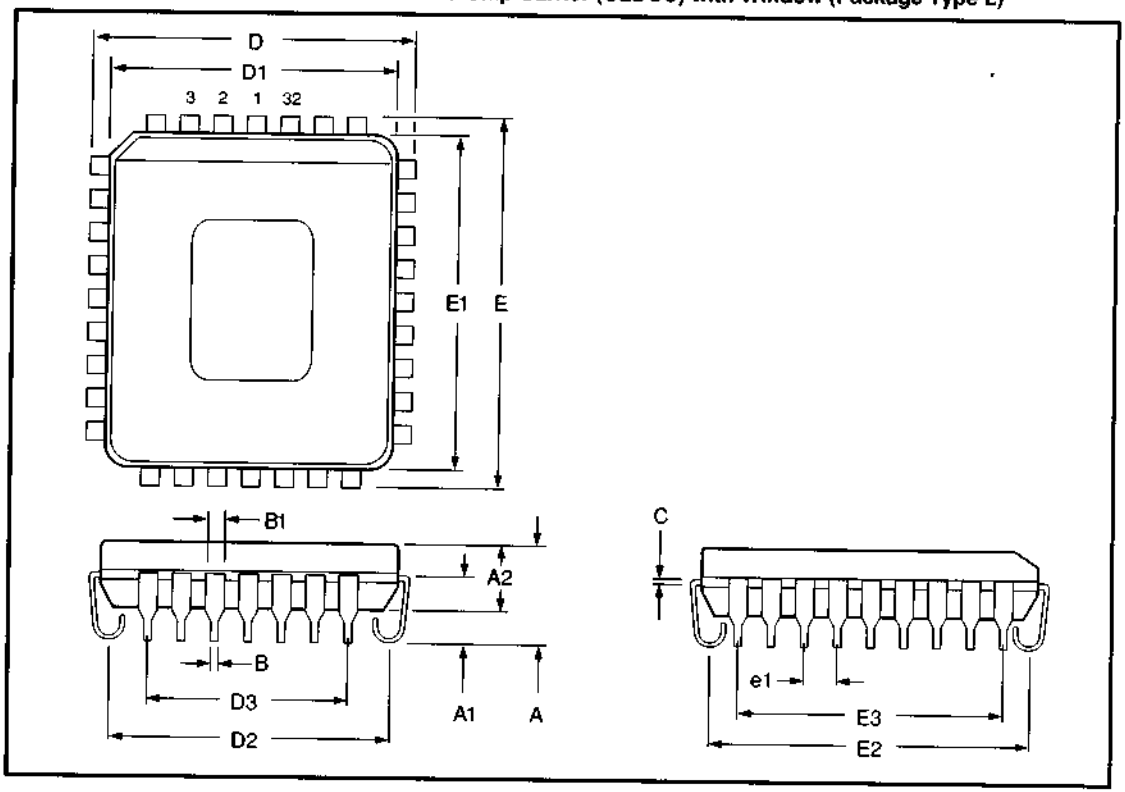
Family: Plastic Leaded Chip Carrier						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.12	3.56		0.123	0.140	
A1	1.98	2.41		0.078	0.095	
A2	2.69	2.84		0.106	0.112	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.262		0.0097	0.0103	
D	12.32	12.57		0.485	0.495	
D1	11.40	11.51		0.449	0.453	
D2	9.91	10.92		0.390	0.430	
D3	7.62		Reference	0.300		Reference
E	14.86	15.11		0.585	0.595	
E1	13.94	14.05		0.549	0.553	
E2	12.45	13.46		0.490	0.530	
E3	10.16		Reference	0.400		Reference
e1	1.27		Reference	0.050		Reference
N	32			32		

DRAWING L2 28 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)



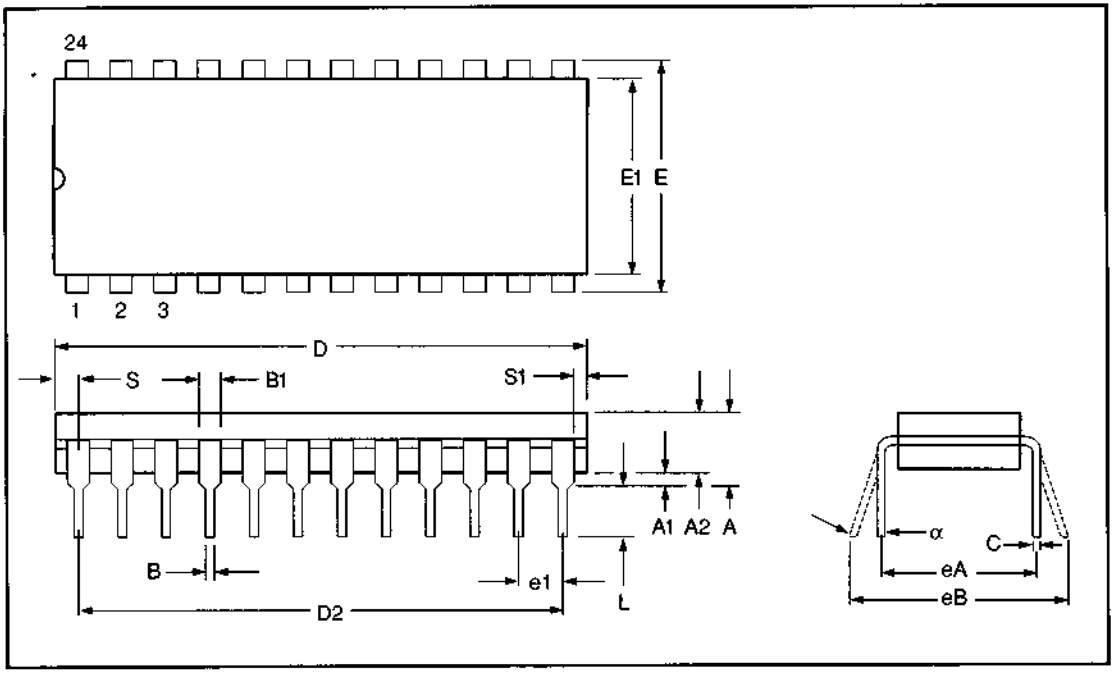
Family: Ceramic Leaded Chip Carrier-CERQUAD						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.94	4.57		0.155	0.180	
A1	2.29	2.92		0.090	0.115	
A2	3.05	3.68		0.120	0.145	
B	0.43	0.53		0.017	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.15	0.25		0.006	0.010	
D	12.32	12.57		0.485	0.495	
D1	10.92	11.56		0.430	0.455	
D2	9.91	10.92		0.390	0.430	
D3	7.62		Reference	0.300		Reference
E	12.32	12.57		0.485	0.495	
E1	10.92	11.56		0.430	0.455	
E2	9.91	10.92		0.390	0.430	
E3	7.62		Reference	0.300		Reference
e1	1.27		Reference	0.050		Reference
N	28			28		

DRAWING L3 32 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)



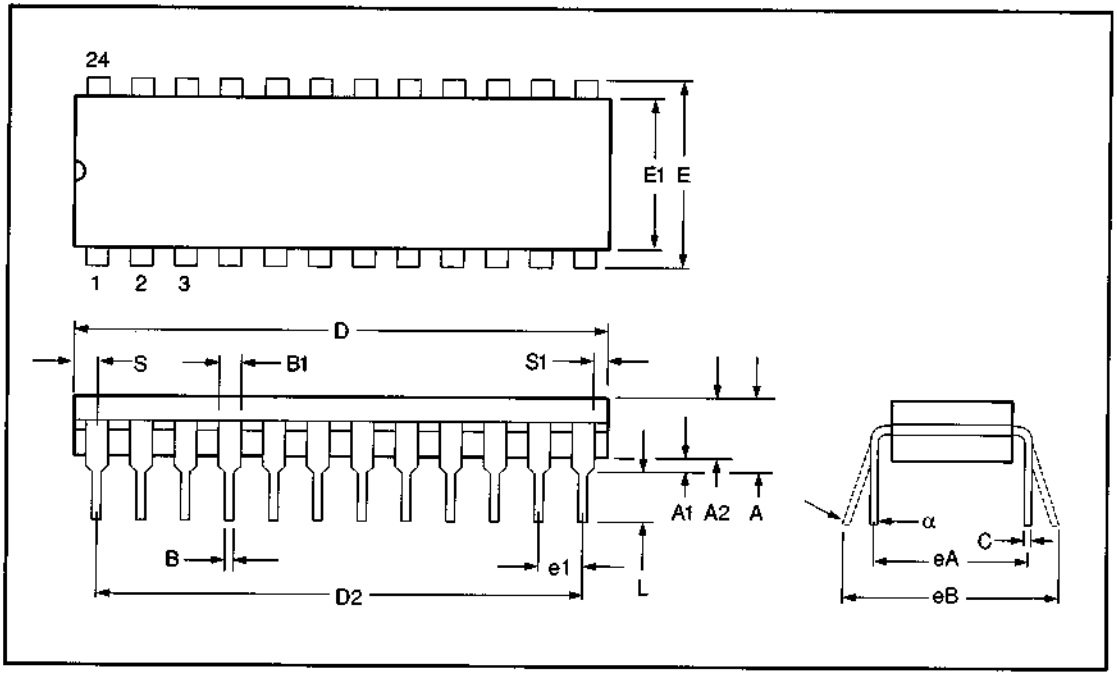
Family: Ceramic Leaded Chip Carrier-CERQUAD						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	3.30	4.06		0.130	0.160	
A1	1.91	2.29		0.075	0.090	
A2	2.29	3.05		0.090	0.120	
B	0.43	0.53		0.017	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.15		Typical	0.006		Typical
D	12.32	12.57		0.485	0.495	
D1	10.92	11.56		0.430	0.455	
D2	9.91	10.92		0.390	0.430	
D3	7.62		Reference	0.300		Reference
E	14.86	15.11		0.585	0.595	
E1	13.77	14.12		0.542	0.556	
E2	12.95	13.46		0.510	0.530	
E3	10.16		Reference	0.400		Reference
e1	1.27		Reference	0.050		Reference
N	32			32		

DRAWING P2 24 Pin Plastic DIP (Package Type P)



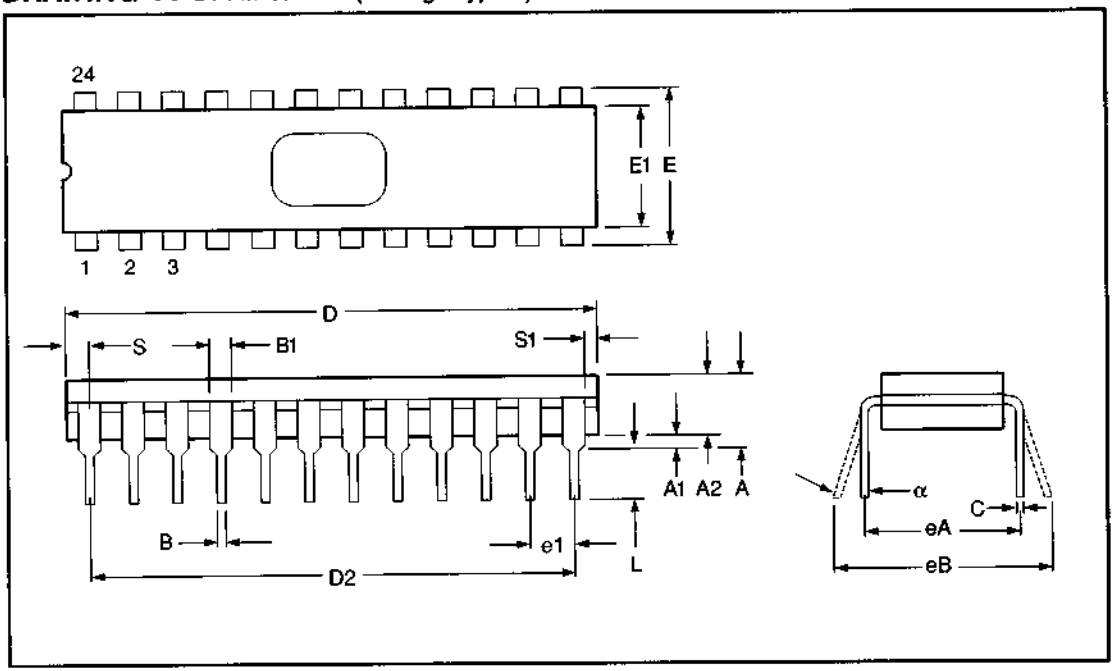
Family: Plastic Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	-	4.83		-	0.190	
A1	0.38	-		0.015	-	
A2	3.81		Typical	0.150		Typical
B	0.38	0.56		0.015	0.022	
B1	1.40	1.52		0.055	0.060	
C	0.20	0.30		0.008	0.012	
D	31.62	31.88		1.245	1.255	
D2	27.94		Reference	1.100		Reference
E	15.24	15.88		0.600	0.625	
E1	13.46	14.22		0.530	0.560	
e1	2.54		Reference	0.100		Reference
eA	15.24		Reference	0.600		Reference
eB	15.24	17.78		0.600	0.700	
L	3.18	3.43		0.125	0.135	
N	24		600 Mil	24		600 Mil
S	1.78	2.03		0.070	0.080	
S1	0.76	-		0.030	-	

DRAWING S1 24 Pin Plastic .300 DIP (Package Type S)



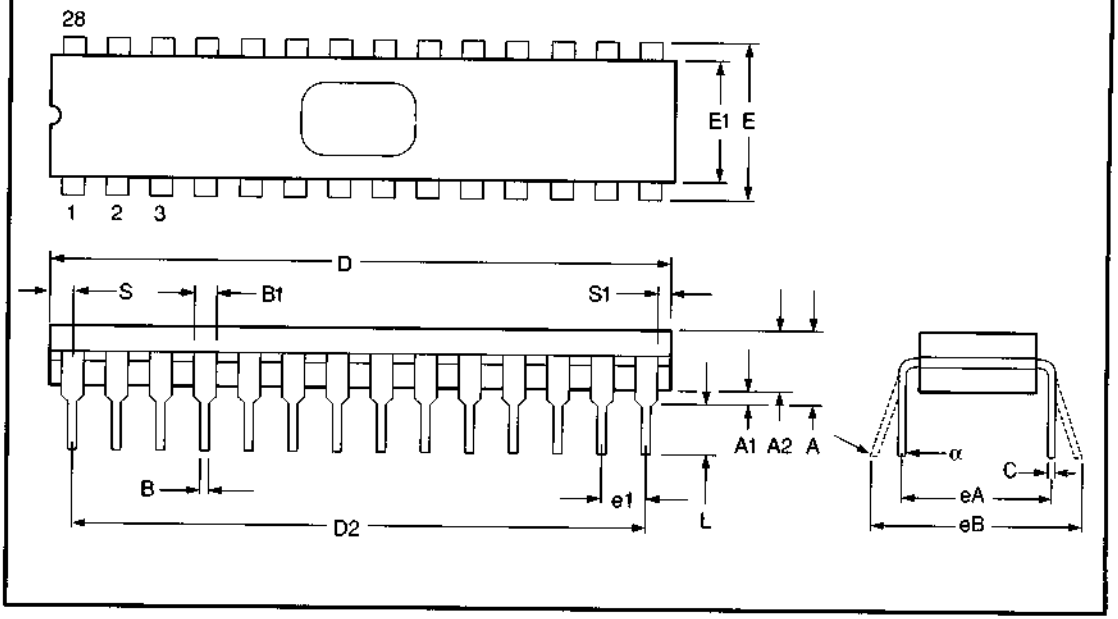
Family: Plastic Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	-	4.32		-	0.170	
A1	0.38	-		0.015	-	
A2	3.30		Typical	0.130		Typical
B	0.38	0.56		0.015	0.022	
B1	1.14	1.65		0.045	0.065	
C	0.20	0.30		0.008	0.012	
D	31.88	31.13		1.255	1.265	
D2	27.94		Reference	1.100		Reference
E	7.62	8.26		0.300	0.325	
E1	6.35	6.86		0.250	0.270	
e1	2.54		Reference	0.100		Reference
eA	7.62		Reference	0.300		Reference
eB	7.62	10.16		0.300	0.400	
L	3.18	3.43		0.125	0.135	
N	24		300 Mil	24		300 Mil
S	1.78	2.16		0.070	0.085	

DRAWING T1 24 Pin CERDIP (Package Type T)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.68	5.08		0.145	0.200	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.41	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	31.55	32.51		1.240	1.280	
D2	27.94		Reference	1.100		Reference
E	7.62	8.13		0.300	0.320	
E1	7.11	7.87		0.280	0.310	
e1	2.54		Reference	0.100		Reference
eA	7.87		Reference	0.310		Reference
eB	7.62	10.16		0.300	0.400	
L	3.18	4.70		0.125	0.185	
N	24		300 MIL	24		300 MIL
S	1.40	2.29		0.055	0.090	
S1	0.13	-		0.005	-	

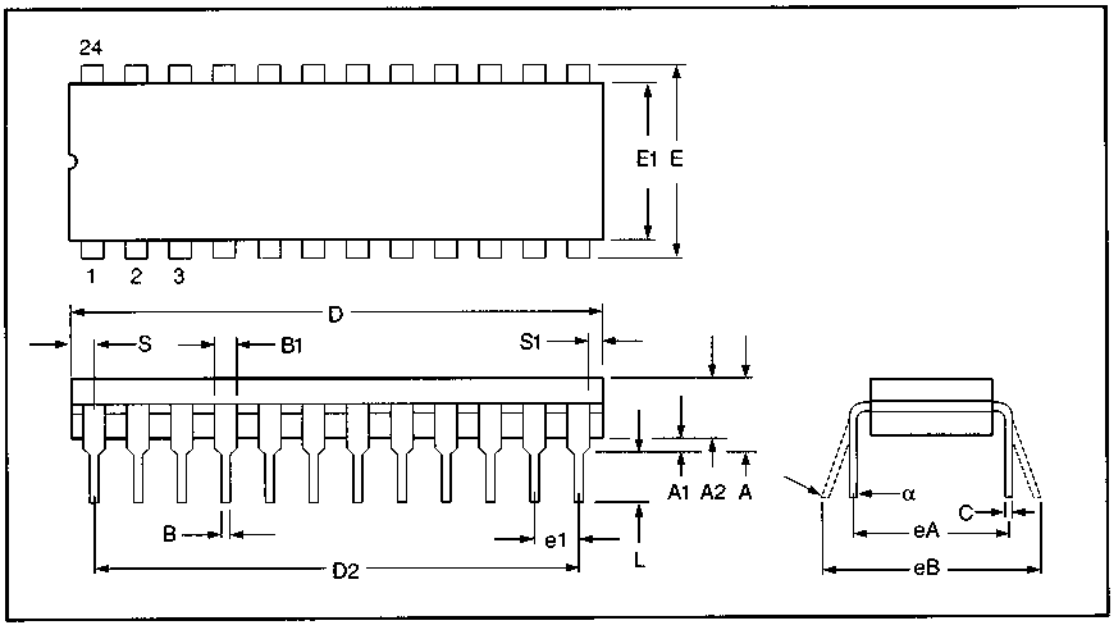
DRAWING T2 28 Pin CERDIP (Package Type T)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.68	5.08		0.145	0.200	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.38	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.20	0.33		0.008	0.013	
D	36.58	37.59		1.440	1.480	
D2	33.02		Reference	1.300		Reference
E	7.62	8.13		0.300	0.320	
E1	7.11	7.87		0.280	0.310	
e1	2.54		Reference	0.100		Reference
eA	7.87		Reference	0.310		Reference
eB	7.62	10.16		0.300	0.400	
L	3.18	4.70		0.125	0.185	
N	28		300 MIL	28		300 MIL
S	1.40	2.29		0.055	0.090	
S1	0.13	-		0.005	-	

5

DRAWING Y3 24 Pin CERDIP (Package Type Y)



Family: Cerdip Dual In-Line Package						
	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
α	0°	15°		0°	15°	
A	3.81	5.72		0.150	0.225	
A1	0.38	1.14		0.015	0.045	
A2	3.56	4.83		0.140	0.190	
B	0.38	0.51		0.015	0.020	
B1	1.27	1.65		0.050	0.065	
C	0.230	0.33		0.008	0.013	
D	31.50	32.77		1.240	1.290	
D2	27.94		Reference	1.100		Reference
E	15.24	15.75		0.600	0.620	
E1	13.08	15.37		0.515	0.605	
e1	2.54		Reference	0.100		Reference
eA	15.49		Reference	0.610		Reference
eB	15.75	17.78		0.620	0.700	
L	3.18	4.70		0.125	0.185	
N	24		600 MIL	24		600 MIL
S	1.40	2.29		0.055	0.090	
S1	0.25	-		0.010	-	