High Performance CMOS Memory and Programmable VLSI

1990 Data Book

PROMs/RPROMs
EPROMs
Programmable System™ Devices

WAFERSCALE INTEGRATION, INC

WAFERSCALE INTEGRATION, INC.

HIGH PERFORMANCE CMOS MEMORY AND PROGRAMMABLE VLSI DATABOOK

1990

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WAFERSCALE INTEGRATION, INC.

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WAFERSCALE INTEGRATION, INC.

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INTRODUCTION

WaferScale Integration, Inc. (WSI) designs and produces the world's broadest and fastest families of CMOS PROMs, RPROMs, EPROMs, and Programmable System™ Devices (PSD). These product families target the needs of system designers who must reduce system development time and deliver market competitive products in continuously shorter periods of time. WSI's programmable VLSI products additionally enable higher system performance from smaller, more compact end products due to higher levels of system integration at the chip level.

WSI's mission is clear — to build a great company by serving its customers with a portfolio of high-performance programmable VLSI products that enable designers to achieve faster time to market with new, advanced electronic systems.

The company's patented self-aligned, split-gate EPROM technology forms the core of WSI's programmable products and delivers higher performance and greater density than competing "stacked gate" EPROM technologies. This core technology has enabled WSI to be first in the industry with numerous breakthroughs in speed, density, process and packaging. WSI has leveraged this technology into the broadest family of CMOS PROMs, RPROMs, and EPROMs available.

WSI's new "off the shelf" user-configurable PSDs provide system level building blocks on a single chip that enable quick implementation of application specific controllers and peripherals. They are the first to integrate high-performance EPROM, SRAM and logic and deliver a performance and integration breakthrough to the programmable products market. PSDs are user-configurable on a PC or compatible and can be tailored for use in a variety of system applications. As a result, WSI has established itself as a leading supplier of high-performance programmable VLSI solutions to a broad customer base that includes some of the world's largest and most technologically advanced electronics companies.

Founded in 1983, WSI is headquartered in a 66,000 square foot facility in Fremont, California and has more than 125 employees. Through a long-term equity, manufacturing and technology license agreement with Sharp Corporation of Japan, WSI produces its products in a world-class production facility that guarantees the highest quality at competitive costs.

MARKETS AND APPLICATIONS

WSI's high-performance non-volatile memory and PSD products are used by the world's leading suppliers of high-performance electronic systems in communications, data processing, military and industrial markets. Customer end products cover a broad spectrum and typically include cellular telephones, workstations, DSP computers, navigation controllers, T1 multiplexers, modems, image processors, missiles, LAN controllers, high density disk drives and the like. Customer applications include image processing, digital signal processing, bus control, LAN data and file control, real time process control, graphics processing, hard disk control, flight simulators, DMA control, and others. WSI products are ideally suited for these applications where designers are faced with increasingly shorter product life cycles and must develop new, competitive high-performance products in short periods of time.

PRODUCTS

Memory Products

EPROMs

WSI offers the broadest line of CMOS EPROM products available featuring architectures ranging from 8K x 8 to 128K x 8, plus several x16 products, with speeds ranging from 40 to 200 ns. Commercial, industrial and MIL-STD-883C/SMD products are available. A wide variety of package selections are available including plastic and hermetic, through-hole and surface mount types.

"L" Family

WSI's "L" family memory products are the industry's fastest, low power JEDEC pinout EPROMs and meet the requirements of many mainstream system applications. With speeds ranging from 90 to 200 ns and architectures from 8K x 8 to 128K x 8 including several x16 products, "L" family EPROMs are ideal for high-performance personal computers and workstations. Taking advantage of its split-gate EPROM technology, WSI uses a conservative 1.2 micron lithography to achieve world-class memory densities that traditionally require lower yielding sub-micron technologies.

"F" Family

The "F" family is WSI's fastest line of EPROMs, featuring speeds ranging from 40 to 110 ns and architectures from 8K x 8 to 32K x 8, plus several x16 products. The high speed and word width options of the "F" family EPROMs make them attractive for use in high-end engineering and scientific workstations, data communications and other high-performance applications.

RPROMs

RPROMs provide bipolar PROM pin-out with matching speed and CMOS low power operation. The RPROM (Re-Programmable Read Only Memory) product series includes architectures ranging from 2K x 8 to 32K x 8 with speeds ranging from 25 to 70 ns.

Commercial, industrial and MIL-STD-883C/SMD configurations are available in a variety of hermetic and plastic package styles.

Programmable System™ Devices (PSDs)

WSI's family of Programmable System Devices (PSDs) represent a new class of programmable VLSI products, achieving unparalleled levels of performance, configurability and integration. Offering a significantly higher level of integration over programmable logic, PSDs are the first programmable VLSI products to integrate high-speed EPROM, SRAM and logic on a single chip thereby providing complete system solutions to the design engineer. PSDs are off-the-shelf system building elements that can be quickly configured and programmed for a variety of system applications thus enabling system designers to shorten system development time.

The PSD is a new solution for system designers who build high-end systems around embedded controllers and advanced microprocessors. These new systems require faster, more highly integrated and lower cost VLSI solutions as well as rapid design cycles. WSI's new PSD family meets this demanding set of needs.

The initial members of WSI's PSD family includes:

- The PAC1000 User-Configurable Microcontroller
- The MAP168 User-Configurable Peripheral with Memory
- The PSD301 User-Configurable Peripheral with Memory
- The SAM448 User-Configurable Microsequencer

Design Tools and Support

WSI's development tools minimize the time required for designers to program PSDs for use in a variety of system applications. PSDs are supported with complete easy-to-use program development, simulation and programming software, the PC hosted MagicPro™ Memory and PSD Programmer, a dial-in applications bulletin board and WSI's team of factory and field applications engineers. As a result, WSI customers achieve their goal of shorter system development time and reach new markets sooner.

PRODUCTS (Cont.)

Custom Circuits

To serve the needs of its customers with unique requirements, WSI offers its custom circuit capability using its cell based library of EPROM, static RAM and logic functions. Standard products described in this catalog can usually be modified on a custom basis to serve particular requirements. New customer defined custom products that incorporate high-performance non-volatile memory, SRAM and logic can be produced that deliver significant speed or system integration advantages. Contact your local WSI sales office for additional information.

MANUFACTURING

A key ingredient for success in leading-edge semiconductors is a world-class fabrication facility that ensures high volume capacity and prompt delivery of highly reliable and high yielding VLSI circuits. To this end, WSI has licensed its proprietary CMOS EPROM and logic process technology to Sharp Corporation of Osaka, Japan. This long term alliance ensures high quality, high-volume production, competitive costs and fast delivery. The Sharp facility in Fukuyama, Japan employs the most advanced sub-micron VLSI integrated circuit manufacturing equipment available including ion implantation, reactive ion etch, and wafer stepper lithographic systems.

QUALITY AND RELIABILITY

WSI is deeply committed to product excellence. This begins with proper management attitude and direction and with this focus, the Quality and Reliability Program is able to operate efficiently. As a result, product quality becomes part of each employee's responsibility.

Quality and Reliability begin with the proper product and process designs and is supported by material and process controls. Examples are products manufactured on an epitaxial silicon layer to reduce latch-up sensitivity, all pins are designed to withstand >2,000 volts ESDS, numerous ground taps are used which increases product noise immunity, metal traces are designed to carry a current density of $>2.0 \times 10^5$ amps/cm^2, top passivation extends over into the scribe lane to seal the die edges, data retention is performed 100% on re-programmable products (T_A = +225°C, T = 72 hours), automated die attach and bonding is used extensively, wafers are fabricated in a Class 10 clean room, raw materials, chemicals and gases are inspected before use, and statistical controls are used to keep the process on course.

Product and process introductions or changes are routinely evaluated for worthiness. Life tests are conducted at higher than typical stress levels (T_A = +150°C, V_{CC} = +6.5V) and even at these stress levels, WSI products have demonstrated low failure rates (see the Quality and Reliability section in this databook).

WSI is active in Military programs and its Quality and Reliability System supports Compliant Non-Jan products. WSI also supports DESC's (Defense Electronics Supply Center) Standardized Military Drawings (SMD) program. As of October, 1989, WSI has eighteen products on SMDs with additional products pending. Several additional products not on SMDs are available per MIL-STD-883C. See Section 7 (Military Products) in this databook.

SALES NETWORK

WSI's international sales network includes regional sales managers, field applications engineers, manufacturers representatives and many of the leading component distributors in the United States, Europe and Asia. See Section 10 in this catalog.

United States

Direct sales and field applications engineering offices in Boston, Chicago, Huntsville, Philadelphia, Los Angeles areas and Fremont, CA; more than 25 manufacturers' representatives for major national accounts; national distributors including Schweber Electronics, Time Electronics and Wyle Laboratories; and regional distributors.

International

Distributors in West Germany, England, France, Italy, Sweden, Finland, Denmark, Norway, Spain, Belgium, Luxembourg, the Netherlands, and Israel. Distributors for the Asia/Pacific Rim region in Japan, Korea, Taiwan, Hong Kong and Australia.

Each generation of systems involved with data processing, communications, military and industrial control historically requires faster and more efficient system functions to accomplish greater productivity. Issues of performance, reliability, design time, system integration, power, and cost must be successfully treated to insure the market success of competitive end products. WSI's CMOS technology forms the foundation of a portfolio of programmable VLSI integrated circuits that are used by leading systems manufacturers worldwide to address the above issues and retain their competitive edge.

WSI's core technology begins with its patented self-aligned, split-gate single transistor EPROM cell (U.S. patents #4,639,893 and 4,795,719). The self-aligned, split-gate EPROM cell pioneered by WSI is the only major EPROM technology/architecture innovation since 1972. This advancement beyond the traditional "stacked gate" EPROM cell, when coupled with several memory array design enhancements, provides WSI with a broad product line of high-performance PROMs, RPROMs, EPROMs and Programmable System™ Devices.

The WSI self-aligned, split-gate EPROM cell will not program in the reverse direction. This feature has enabled the development of a high density virtual ground array EPROM architecture that has resulted in smaller EPROM die sizes than competitive products even when fabricated with less aggressive photolithography.

WSI's 1.2 micron double metal/double poly N-well CMOS process enables the combining of high-performance EPROM memory, static random access memory and logic all on the same low power circuit. This capability has enabled the development of the Programmable System Devices product family. These standard product integrated circuits shorten system development time by enabling the design engineer to quickly configure and program them for use in various portions of the system. Their high level of integration and versatility enable designers to develop end products faster and reach markets ahead of their competition.

WSI's use of epi wafers and design innovations result in products that exhibit immunity to latch-up and provide ESD protection far in excess of that specified by MIL-STD-883C.

Technology and design patents held by WSI are listed below. Several additional patents are pending.

#4,328,656	Non-Volatile EPROM with Increased Efficiency
#4,361,847	Non-Volatile EPROM and EEPROM with Increased Efficiency
#4,409,723	Non-Volatile EPROM and EEPROM with Increased Efficiency
#4,639,893	A Self-Aligned, Split-Gate EPROM
#4,649,520	A Single Layer Polycrystalline Floating Gate
#4,758,869	Non-Volatile Floating Gate Transistor Structure
#4,763,184	Input Circuit for Protecting Against Damage Caused by Electrostatic Discharge
#4,795,719	A Self-Aligned, Split-Gate EPROM

EPROMs FOR MODERN TIMES

HIGH SPEED EPROMs:

Early generations of microprocessors (e.g., 6809, 8085, 8086, etc.) and microcontrollers (8048, 8051, 6805, etc.) operated at frequencies in the 1-5 MHz range. At these operating frequencies, memory access time requirements varied from 200-500 ns. The EPROM technology available at the time was well suited for such applications. This technology, based upon a single transistor "stacked gate" EPROM cell (see Figure 1), was optimized for programmability and density, not speed. Many manufacturers were quite successful with this technology and manufactured EPROMs from 16K bits up to 1 Mbit.

However, today's generation of high performance microprocessors (80286, 80386, 68000, 68020, etc.), microcontrollers (8096, etc.) and dedicated DSP processors (TMS320xx, MC56000, etc.) operate in the 12-40 MHz range and require memories with access times well below 100 ns (see Table 1).

Table 1
MEMORY ACCESS TIME REQUIREMENTS

PART #	FREQUENCY	MEMORY ACCESS
80386	16 MHz	70 ns
68020	20 MHz	70 ns
32020	20 MHz	75 ns
56000	20 MHz	55 ns
320C25	40 MHz	40 ns

As will be shown, the traditional single transistor "stacked gate" approach is not able to provide such high speeds. As a result, system designers are forced into alternatives such as down loading from slow EPROM into fast SRAM, which provides non-volatility and high speed. Unfortunately, these techniques result in higher system costs (board space, components, power, etc.).

Semiconductor manufacturers are attempting to solve this problem at the I.C. level with various approaches. This article explains the various techniques for achieving high speed EPROMs and allows the reader to determine which technique is best suited for their application and which technique provides the best path for the future.

HIGH SPEED NVM: A GENERAL DISCUSSION

Memory arrays are laid out in two-dimensional row and column formats. These are referred to as word lines and bit lines, respectively. Selecting a word line determines which row of cells in the array has been chosen to provide the programmed output. The bit line, or column, is used to determine which of the selected cells in the row is to be read from an output. Although this technique singles out a particular EPROM cell for reading, the output of the selected EPROM is still connected to the outputs of several non-selected EPROM cells which share the same column, or bit line. Each of these non-selected cells adds some capacitance to the bit line. This capacitance must be overcome by the selected cell before the proper state ("1" or "0") can be sent to the output. The selected cell must have enough drive to be able to discharge the combined bit line capacitance. Higher drive, or read current, results in a faster capacitive discharge and, therefore, faster reading. Lower bit line capacitance and/or increasing read current are the fundamental goals associated with developing high speed, dense EPROMs. Lowering bit line capacitance is easily achieved by reducing the number of memory cells. Although this results in a speed improvement, it severely limits density.

The main problem to solve, therefore, is how to manufacture an EPROM cell which can provide high read current (for speed), high density (for small size), high reliability and ease of programming.

The following paragraphs discuss four approaches for developing a fast, dense, reliable and programmable EPROM memory.

SINGLE TRANSISTOR ("STACKED GATE")

The industry standard single transistor stacked gate EPROM cell (Figure 1) is optimized for efficient programming and high density. It is not well suited for high speed because of its low read current. The typical read current for a single unprogrammed stacked gate EPROM cell is between 20-50 microamps and the total bit line capacitance for a typical EPROM can be as high as 3-5 pF. Consequently, at 40 microamps of worst-case read current, it would take a "stacked gate" EPROM cell 70 ns to discharge the bit line by enough voltage to detect an unprogrammed condition. Address decoding and output buffers add another 25-50 ns (depending upon technology). Clearly, this makes it very difficult to achieve a worst-case total access time which will allow an EPROM to run with today's generation of processors (see Table 1). Several semiconductor manufacturers are looking for alternatives to surmount the inherent limitations of the older single transistor "stacked gate" EPROM.

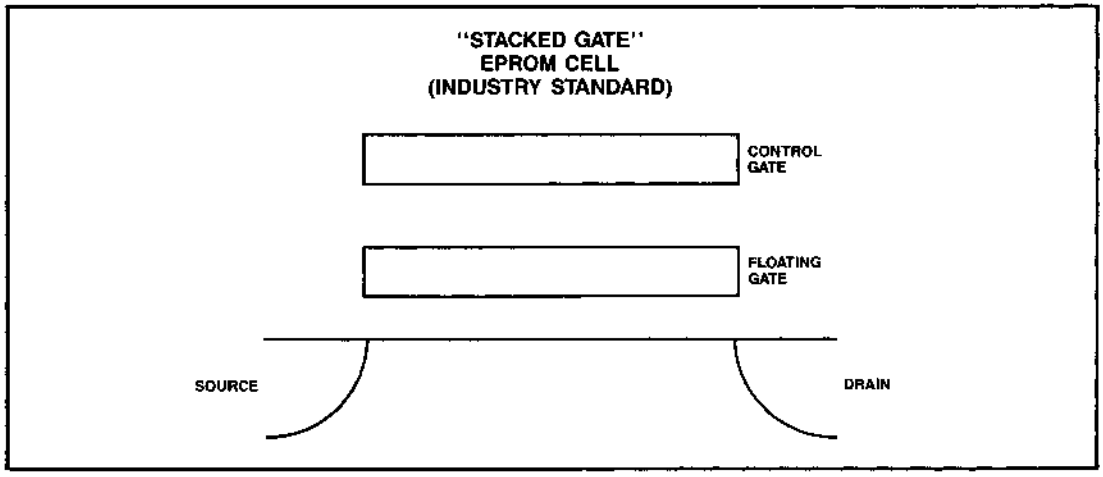

Figure 1

TWO TRANSISTOR FAST CELL ("STACKED GATE" EPROM)

In this approach each bit consists of *two stacked gate EPROM cells* in a differential pair. With this architecture, it is possible to employ a differential sensing technique which allows a programmed or unprogrammed state ("0" or "1") to be detected with a very small voltage swing. As a result, a memory cell can be read much faster than with a standard sensing technique. However, this incurs the penalty of twice the area of the single cell memory array as well as implications of lower yields, higher costs and lower reliability than a single cell approach.

FOUR TRANSISTOR FAST CELL ("STACKED GATE" EPROM)

In this approach, the differential sensing technique is also used. However, each half bit is constructed with two transistors, one of which is optimized for programming efficiency while the second transistor is optimized to give high read current (typically 150 microamps). This makes it possible to achieve very high speeds. However, a four transistor cell results in a very large memory array resulting in problems more severe than those of the two transistor approach (again, low yields, high costs and low reliability). Consequently, this technique is limited to low density devices.

STACKED GATE SUMMARY

MEMORY TYPE	RELATIVE SPEED	RELATIVE DIE SIZE
Single Transistor	Slow	Small
Two Transistor	Fast	Large
Four Transistor	Fastest	Larger

SINGLE TRANSISTOR FAST CELL ("SPLIT GATE" EPROM)

WaferScale Integration Inc. (WSI) has developed a proprietary technology which embodies all of the benefits of the single transistor "stacked gate" (ease of programming, reliability, and density) and conquers the fundamental problem of low read current. This patented technology is known as the "split gate" EPROM (see Figure 2).

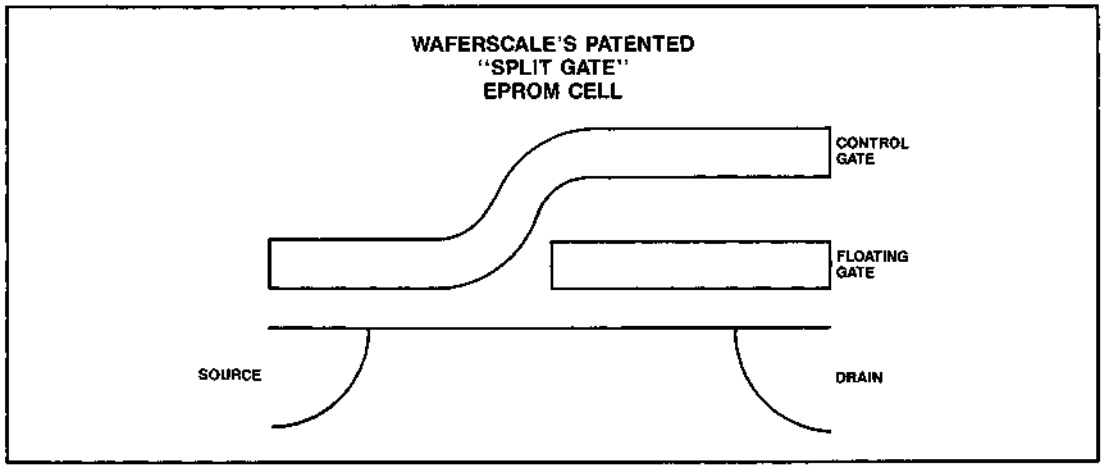

Figure 2

The "split gate" cell uses a single transistor per bit and, although it is nearly the same size as the "stacked gate," each cell provides a read current of at least 160 microamps under worst-case voltage and temperature conditions. This allows the design of very high density and *very fast* memory products. As an example of the capabilities of the "split gate," WaferScale has introduced families of EPROM products varying in density from 16K to 1 Mbits and in speed ranging from 25-200 ns, all manufactured with the same EPROM technology.

SPLIT GATE SUMMARY

MEMORY TYPE	RELATIVE SPEED	RELATIVE DIE SIZE
Single Transistor	Fastest	Small

As is seen from the table above, the WSI split gate EPROM technology provides the high density capability of the single transistor "stacked gate" and the fast speed of the four transistor solution.

REQUIRED FEATURES

Although speed and density are necessary EPROM attributes, they alone are not sufficient for today's memory requirements. Reliability and ease of programming play an equally important role in determining the usefulness of a memory product.

SUMMARY

Although the single transistor "stacked gate" EPROM technology is very well suited for its intended use (slow, dense NVM), it is not well suited for today's high performance memory requirements. Brute force techniques, such as using multiple transistor memory cells, can provide high performance; however, the penalty paid in die size and resultant higher costs limits these techniques to relatively low densities.

WaferScale's patented "split gate" technology combines all of the attributes of the single transistor "stacked gate" (reliability, ease of programming and density) with the speed of the multi-transistor memory cell. The result is a family of dense, high speed EPROM based products. Also, since WaferScale's technology is well suited for device scaling, the technology path for future products is already in place. This will result in products with higher density that utilize both standard and application specific architectures.

IPI-2 DISK CONTROLLERS DOUBLE DATA TRANSFERS

COMPUTER KEYBOARDS GIVE USERS MORE OPTIONS

ELECTRONIC DESIGN

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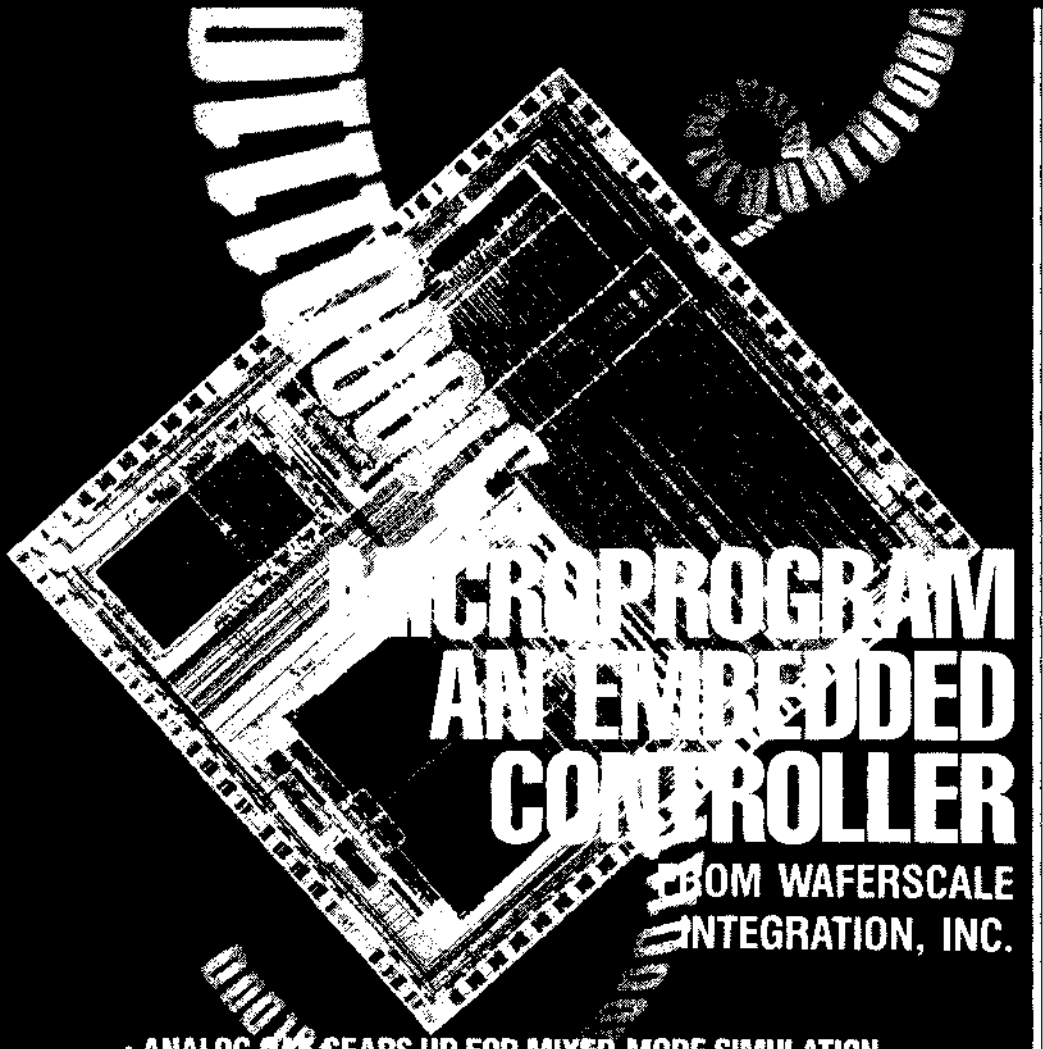


MICROPROGRAM AN EMBEDDED CONTROLLER

FROM WAFERSCALE INTEGRATION, INC.

• ANALOG CAE GEARS UP FOR MIXED-MODE SIMULATION

• POWER-FACTOR CONTROL CIRCUITS RUN TWO STEPPERS FROM ONE BOARD

COVER FEATURE

PACKING ALL THE MAJOR BLOCKS OF A MICROPROGRAMMABLE SYSTEM, A CMOS IC EASES EMBEDDED CONTROLLER DESIGNS

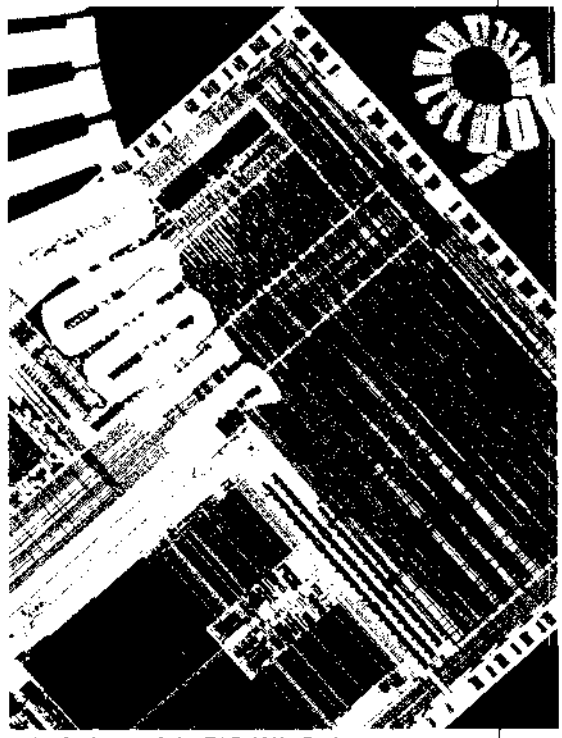
CONFIGURABLE CHIP EASES CONTROL-SYSTEM DESIGN

DAVE BURSKY

Anyone who has ever designed a high-performance controller subsystem using high-speed microprogrammed building blocks, programmable logic devices, gate arrays, or discrete logic realizes the difficulties in integrating the complete solution. In such a system, the chip count escalates, the operating power rises, and the development schedule lengthens.

By integrating all these functions and resources onto one high-speed CMOS chip—the PAC1000 microcontroller—WaferScale Integration Inc. has drastically reduced the chip count from the typically required 50 or so ICs to just one. At the same time, the PAC1000 slashes the power consumption from tens of watts to less than 1.5 W and cuts development time.

The PAC1000 can solve many high-end embedded control applications and is the only available circuit that can tackle system, data, and event control tasks. A C-like language and PC-hosted system-development tools simplify the creation of the control software. Users can configure the circuit as a microprocessor peripheral or as a standalone controller to meet the unique requirements of high-performance system, data, or event controllers. Each of the chip's two bidirectional 16-bit buses, its individual I/O lines, and interrupt inputs can, if necessary, be redefined during each 50-ns instruction cycle.



At the heart of the PAC1000's flexibility lies an internal microprogrammable architecture, including a 16-bit CPU, a fast 10-bit microsequencer, a 32-word-by-16-bit register file, and a 1kword-by-64-bit high-speed EPROM. As product planning manager Yoram Cedar explains, since the circuit executes any of its instructions in one clock cycle, the controller delivers a raw throughput of

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COVER: USER-CONFIGURABLE CONTROLLER

20 MIPS.

Every instruction of the PAC1000 can perform as many as three simultaneous operations: program control, CPU functions, and output control, with all possible combinations allowed. Cedar claims the more powerful instruction format, combined with the higher clock speed, yields a five- to tenfold performance improvement, compared with other one-chip microcontrollers. The high throughput suits many tasks well. It has already found homes in radar, communications, video-graphics, I/O subsystems, bus and DMA controllers, and disk-drive-controllers.

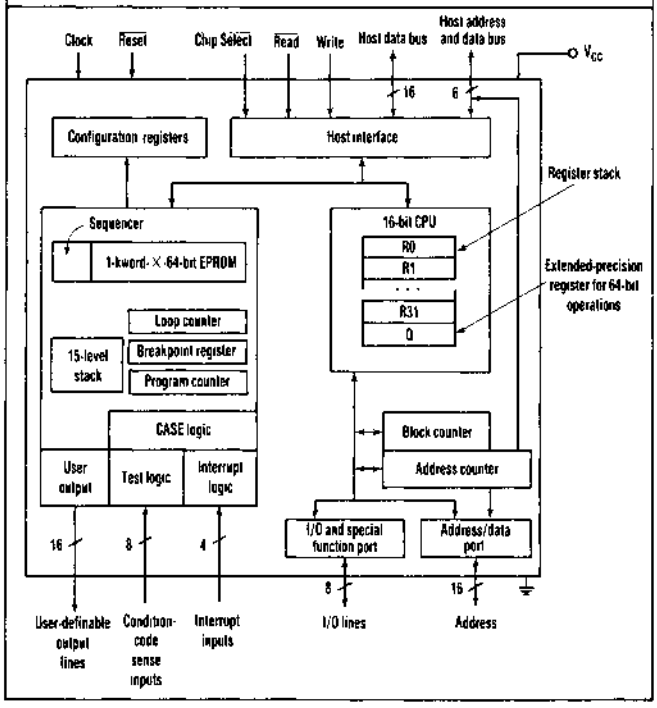
Besides the CPU, register file, and sequencer, the chip includes an auxiliary Q-register for double-word operations, an 8-input interrupt controller, 16 output control lines, 8 bidirectional I/O lines, scan-test and CASE program test logic, and a 22-bit external address bus *(Fig. 1, top)*.

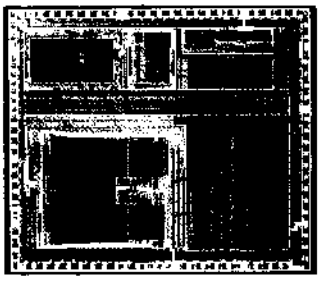
Also, Cedar emphasizes, the circuit deals much more rapidly with interrupts than most controllers do, and that serves embedded control applications well. The chip changes program flow in either of two ways. First, it has four user-definable interrupt input lines plus four dedicated internal interrupts that require just 100 ns, at most, to alter the program flow. Second, another set of input lines—22 condition-code inputs (8 external and 14 internal)—let the processor alter the program flow with condition calls and program jumps in just one 50-ns instruction cycle.

And if on-chip resources don't quite match an application's requirements, chip modifications can be done for large-volume users. The circuit was designed with the company's standard-cell library, and many of the chip's sections are actually cells in WaferScale's library *(Fig. 1, left)*. Noticeable on the chip's left side are the large cells that include the 64-kbit EPROM block on the bottom and the 16-bit CPU on the upper left. On the chip's right side, random logic performs the control and interface functions; small standard cells are used to create those circuits.

For every instruction, a dedicated field specifies the bit pattern on the output lines. Also, designers can individually program eight I/O lines as inputs or outputs or to perform special functions under the control of the chip's mode and I/O registers. The special functions turn the I/O lines into control signals that allow various features and flags to indicate several status conditions. In addition to the eight I/O lines, the circuit has two 16-bit bidirectional buses that go on and off the chip: One links with the host; the other is the upper 16 bits of the address/data bus. Another 16 lines are dedicated, user-programmable latched output lines. These can be changed on a cycle-by-cycle basis.

Thanks to all its buses and control signals, the PAC1000 microcontroller operates as either a memory-





1. PACKING A 16-bit microprogrammable central processor with a 32-word register file, a 1-kword-by-64-bit microcode UV EPROM, sequencer, and other configurable resources, the PAC1000 user-configurable microcontroller from WaferScale Integration delivers a raw instruction throughput of 20 MIPS at 20 MHz (top). Designers can add or alter various blocks to customize versions for high-volume users (left).

COVER: USER-CONFIGURABLE CONTROLLER

mapped peripheral to a microprocessor to offload the CPU *(Fig. 2a)* or as a standalone controller running from its own internally or externally stored program *(Fig. 2b)*. As a peripheral, the chip ties into the host with a straightforward bus interface—a 16-bit data bus and a 6-bit address bus to access the internal resources of the PAC1000—and the standard Chip Select, Read, and Write control lines. In the standalone mode, the chip typically runs the application program from its internal memory and uses its 16-bit output bus and 8-bit I/O port to control the application and communicate to a host system.

To handle multiple operations in parallel, the chip internally takes advantage of a long—64-bit—microcode word so that each word can control multiple sections of the circuitry. The on-chip microcode storage area consists of a fast, reprogrammable UV EPROM, organized as 1 kword by 64 bits. Since the EPROM is read only by the on-chip logic, it doesn't need high-current output buffers, which slow down the memory access. Thus, the EPROM contents can be read very quickly—the chip's 20-MHz version accesses memory in just 30 ns, well within the CPU's 50-ns instruction cycle time. The memory is also secure. Users can program a security bit to prevent an external system from extracting the code from the memory array.

Besides its own program memory, the chip also has a separate address/data bus that can be programmed for either 16 or 22 address lines (with 64-kword or 4-Mword off-chip addressing ranges, respectively). The address generator for the bus is separate from the sequencer that addresses the program memory. The PAC1000 can therefore execute a program while it's using the address bus to move data from memory into the on-chip register file or to an externally controlled device.

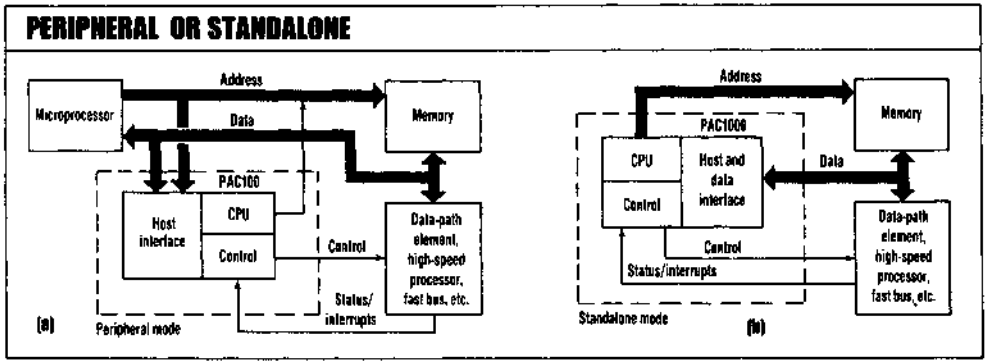
The address bus, in fact, can serve as a simple direct-memory-access controller when used with the on-chip 22-bit address counter and 16-bit block counter. This DMA controller can transfer data from external memory to the on-chip register file or to an external device.

An eight-word FIFO register lets a host microprocessor asynchronously load commands or data into the controller. The 22-bit word length in the FIFO register is employed, so that if data values are to be loaded into the register file, the lower 16 bits of the 22-bit word sent over the host data bus represent the data, and the next five bits—the lower five bits of the host-interface address bus—represent the register location into which the data will be loaded (R0 to R31). The sixth bit of the host-interface address bus signifies whether the word loaded into the FIFO register is a command or data word. If it's a command, the lower 10 bits of the host-data bus are used as a branch address to one of the 1024 memory locations in the EPROM.

The 10-bit sequencer addresses the 1,024 words of program memory and has a 15-level stack that permits multiple subroutine calls to occur without forcing the program to go back to a higher level before calling the next subroutine. Besides having more levels in the stack than WaferScale's 5910 microsequencer, the enhanced sequencer block has a 10-bit loop counter that cuts overhead in programs for loops and nested loops. The application program can load the counter with a constant or a value calculated in the CPU.

Because programming fast, embedded controllers can get complicated, the company includes on-chip programming and test features to ease system development. For starters, a 10-bit breakpoint register simplifies real-time debugging. It can be loaded from either of two sources—a value stored in a CPU register or a constant value specified in the program memory. When the program memory address matches the register contents, the register issues an interrupt, which a service routine in memory could then react to.

Test and CASE logic on the chip also aids program and hardware testing. The condition-code logic responds to 22 different program test conditions that can be tested for true



2. MULTIPLE BUSES, AN ON-CHIP ADDRESS GENERATOR, and sequencer blocks let the microcontroller operate as a memory-mapped peripheral to offload the host microprocessor (a). Or it can be operated as a standalone controller (b).

COVER: USER-CONFIGURABLE CONTROLLER

SAMPLE PROGRAM FOR PAC1000 MICROCONTROLLER

```
/* control memory read/write based on CC0 */
segment memcon ,
  enmem   equ   h'0002',                    /* output control constants          */
  dismem  equ   h'0040',
  wr      equ   h'0000';
  rd      equ   h'1000',
start
  IF CC0 , OUT enmem ;                      /* enable memory                     */
    FOR 6 , AOR  = R0 + R1 , OUT wr ,       /* store begin addr in AOR and loop  */
            AOR  = AOR + 4 , OUT rd ,       /* inc addr by 4 and do rd/wr        */
    ENDFOR , OUT wr ,                       /* end loop body                     */
  ELSE , OUT dismem ,                       /* disable mem if CC0 is not true    */
  ENDIF ,
end ,
```

3. THE HIGH-LEVEL LANGUAGE developed by WaferScale employs C-language-like structures to let designers easily develop complex configuration microcode.

or not-true results. Up to four conditions can be tested simultaneously. Tests can check for the state of various flags or register contents.

The processor handles two types of CASE operations: standard and priority. A CASE group consists of a combination of four test conditions that can be tested in a single cycle. In that same cycle, the PAC1000 branches to any one of 16 locations, depending on the status of the four inputs to the CASE group being tested. The priority CASE instruction operates on internal and external interrupt conditions and treats interrupts as prioritized test conditions. The priority encoder generates a branch to the highest-priority condition.

Thanks to all its on-chip resources, the PAC1000 is a powerful one-chip controller, housed in a windowed, 88-lead pin-grid-array package or an 84-lead ceramic leaded chip carrier. An 84-lead plastic leaded chip carrier package (the one-time-programmable version) is also available. Because the chip employs an EPROM to hold the program, revisions to the code are no more difficult than reprogramming a standard EPROM. Prototype systems and production products can benefit from the ability to revise the code at the last minute.

To alleviate the complexity of microcode program development, WaferScale has assembled a series of PC-hosted system-development tools (PAC-SDT). These make the PAC1000 as easy to program as any one-chip microcontroller. A simple example of a multiple-command expression in the C-like language lets designers combine operations such as FOR6,AOR=R0+R1,OUT WR (loop for six cycles, add the contents of registers R0 and R1 and store the result in the AOR register, output the value WR) in one word *(Fig. 3)*.

The toolset has a system-entry language, a functional simulator, and a device programmer (MagicPro). The system-entry language software is the most critical part. The high-level language uses a structure similar to C's and practically eliminates writing routines in machine or assembly code. But designers who are more comfortable working on that level can write machine-code routines.□

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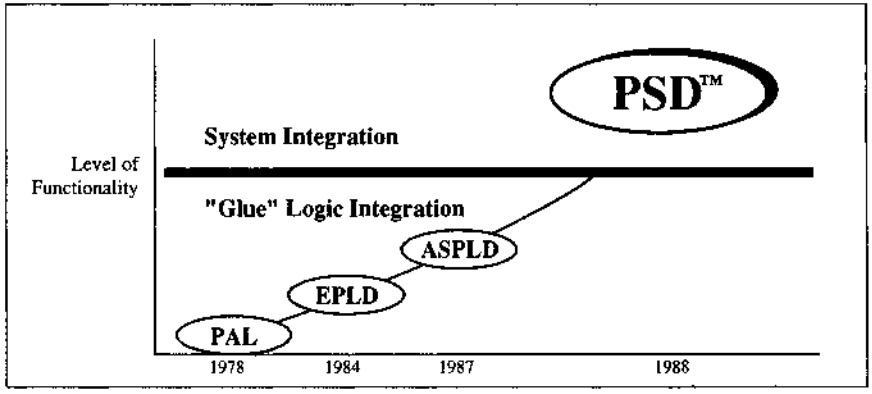

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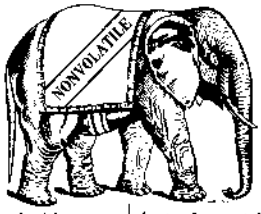
SEMICONDUCTORS

A 'DISADVANTAGE' LEADS TO A FAST 4-MBIT EPROM

By making an advantage out of what a lot of companies would consider a serious drawback, WaferScale Integration Inc. has come up with a 4-Mbit erasable programmable read-only memory in a die size the same as or smaller than memories one fourth its density—and with access times as fast or faster. Moreover, the Fremont, Calif., company fabricated the CMOS EPROM with the same tried-and-tested process that it used in its earlier 256-Kbit and 1-Mbit designs.



Actually, WaferScale more or less had to use the same process—unlike most other EPROM companies, it doesn't have its own fabrication facilities, relying instead on outside foundries. That could be a serious disadvantage, but WaferScale turns it into a boon. "We do not have the luxury of playing around with the process every time we want to improve the speed, increase the density, or reduce the die size," says Boaz Eitan, director of device technology and memory design. "Instead, working within very precise limits, we must rely on circuit and architecture improvements to get the speed and density enhancements we want."

By making those kinds of improvements, WaferScale could use its 1.2-μm process to build the new EPROM and still achieve a 90- to 120-ns read-access time—as fast as any 1-Mbit EPROM available and twice as fast as any of the 4-Mbit EPROMs now being offered as samples. The average cell size is only 9.5 μm^2 and the die area only 320 mil^2. Competitive 4-Mbit EPROMs available as samples from such companies as Intel, NEC, and Toshiba require much tighter 0.8- to 1-μm design rules to achieve die sizes ranging from 375 to 385 mil^2.

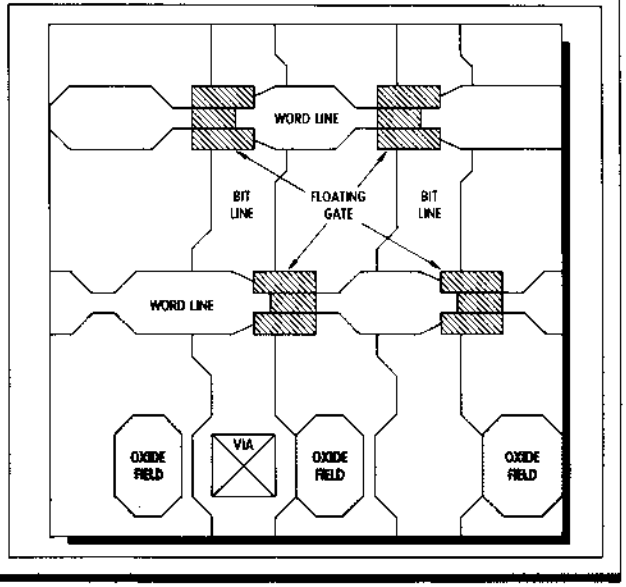
WaferScale's initial parts, specified at 100 to 120 ns, will be available in sample quantities by midyear, with faster parts—90 ns—arriving before the end of the year.

WaferScale expects the new part will find eager users among the manufacturers of high-performance 32-bit processors, in both reduced- and complex-instruction-set systems, says Dale Prull, director of marketing communications.

"Currently, systems designers have had to make a choice when considering memory for program or code storage: low-density, sub-256-Kbit, sub-100-ns EPROMs with no wait states, or 1-Mbit designs with access times anywhere from 100 to 150 ns," he says. "Alternatively, if both speed and density were required, designers had to sacrifice nonvolatility and use static random-access memories in combination with some form of nonvolatile memory."

STAGGERING. The improvements that WaferScale made to boost performance, says Syed Ali, manager of memory design, were largely circuit-design enhancements to the company's proprietary split-gate architecture [*Electronics*, July 9, 1987, p. 65]. The enhancements include a staggered-contact architecture that reduces the number of contacts in an array by almost 25 times, and a staggered-cell design that further improves packing density by alternating the floating gates and reducing bit-line area. *(over)*

STAGGERED GATES GIVE GREATER DENSITY



WaferScale's staggered-contact, staggered-gate architecture enables it to make a 4-Mbit EPROM with its old 1.2-μm process technology and still achieve 90-ns access times.

In addition, some tinkering with the process resulted in a fieldless array that allows devices to be moved closer together while at the same time increasing the effective channel width. Although the bit-line capacitance of this design is much higher due to the longer continuous n+ bit lines, says Eitan, this disadvantage is offset by the fact that the EPROM cell is capable of generating read currents of about 140 to 160 μA at 5 V, about twice what is possible with current EPROMs.

To improve the speed of the device, designers can employ a number of techniques. Chief among them are a differential-balanced amplifier design employing address-transition detection, along with a dual-function column multiplexer and decoder scheme.

The improvements give WaferScale a decided advantage, Eitan says. At most of the companies making EPROMs, circuit designers are running into a brick wall as they try to improve density and speed through scaling. The industry-standard ground-array architecture, with one contact every two cells, limits the scalability of the cell.

WaferScale, by contrast, has eliminated this limitation with its proprietary staggered virtual-ground-array architecture combining staggered contacts and staggered cells. In effect, says Ali, the architecture allows significant reductions in both cell and array size without pushing the lithography. *–Bernard C. Cole*

PART NO.	DESCRIPTION	TEMP	SPEED (ns)	PACKAGES
PROM/RPROM Memory Products				
WS57C191B	2K x 8 CMOS PROM/RPROM	C I M	35/45 45 45/55	24 Pin CERDIP, 0.6" 28 Pin PLDCC 24 Pin Plastic DIP, 0.6" 28 Pad CLLCC
WS57C291B	2K x 8 CMOS PROM/RPROM	C I M	35/45 45 45/55	24 Pin Plastic DIP, 0.3" 24 Pin CERDIP, 0.3"
WS57C43B	4K x 8 CMOS PROM/RPROM	C I M	35/45/55/70 45/55 45/55/70	24 Pin CERDIP, 0.6" 28 Pin PLDCC 24 Pin Plastic DIP, 0.3" 24 Pin CERDIP, 0.3" 28 Pad CLLCC
WS57C43C	4K x 8 CMOS PROM/RPROM	—	25/30	Advance Information
WS57C45	2K x 8 Registered CMOS PROM/RPROM	C M	25/35 35/45	24 Pin CERDIP, 0.3" 28 Pad CLLCC 24 Pin Ceramic Flatpack 24 Pin Plastic DIP, 0.3"
WS57C49B	8K x 8 CMOS PROM/RPROM	C I M	35/45/55/70 45 45/55/70	24 Pin CERDIP, 0.6" 28 Pin PLDCC 24 Pin Plastic DIP, 0.6" 24 Pin CERDIP, 0.3" 28 Pad CLLCC 24 Pin Plastic DIP, 0.3" 24 Pin Ceramic Flatpack
WS57C49C	8K x 8 CMOS PROM/RPROM	—	25/30	Advance Information
WS57C51B	16K x 8 CMOS PROM/RPROM	C M	40/45/55/70 45/55/70	28 Pin CERDIP, 0.6" 32 Pin CLDCC 28 Pin CERDIP, 0.3" 32 Pad CLLCC
WS57C71C	32K x 8 CMOS RPROM	C M	40/45/55 55	28 Pin CERDIP, 0.6" 32 Pin CLDCC 28 Pin CERDIP, 0.3" 32 Pad CLLCC
EPROM Memory Products (Bytewide)				
WS27C64F	Military 8K x 8 CMOS EPROM	M	90/100	32 Pad CLLCC 28 Pin CERDIP, 0.6"
WS27C64L	8K x 8 CMOS EPROM	C I M	90/120/150/200 120 120/150/200	28 Pin CERDIP, 0.6" 28 Pin CERDIP, 0.3" 32 Pin PLDCC 28 Pin Plastic DIP, 0.6"

CMOS PRODUCT SUMMARY (Cont.)

PART NO.	DESCRIPTION	TEMP	SPEED (ns)	PACKAGES
EPROM Memory Products (Bytewide) (Cont.)				
WS57C64F	8K x 8 CMOS EPROM	C I M	55/70 70 70	28 Pin CERDIP, 0.6" 32 Pad CLLCC 32 Pin PLDCC
WS27C128F	Military 16K x 8 CMOS EPROM	M	90	32 Pad CLLCC 28 Pin CERDIP, 0.6"
WS27C128L	16K x 8 CMOS EPROM	C I M	90/120/150 120 120/150/200	28 Pin CERDIP, 0.6" 32 Pin PLDCC 28 Pin Plastic DIP, 0.6" 28 Pin CERDIP, 0.3"
WS57C128F	16K x 8 CMOS EPROM	C I M	55/70 70 70	28 Pin CERDIP, 0.6" 32 Pad CLLCC
WS27C256F	32K x 8 CMOS EPROM	C M	45/55/70 70/90	28 Pin CERDIP, 0.6" 32 Pad CLLCC 32 Pin CLDCC
WS27C256L	32K x 8 CMOS EPROM	C I M	90/120/150 120/150 120/150/200	28 Pin CERDIP, 0.6" 28 Pin CERDIP, 0.3" 32 Pad CLLCC 32 Pin PLDCC 32 Pin CLDCC 28 Pin Plastic DIP, 0.6"
WS57C256F	32K x 8 CMOS EPROM	C I M	40/55/70/90 70/90 55/70/90	28 Pin CERDIP, 0.6" 32 Pad CLLCC 32 Pin CLDCC
WS27C512F	64K x 8 CMOS EPROM	C M	90 90/120	32 Pad CLLCC 28 Pin CERDIP, 0.6"
WS57C512F	64K x 8 CMOS EPROM	—	55/70/90	Advance Information
WS27C512L	64K x 8 CMOS EPROM	C M	100/120/150 150/200	28 Pin CERDIP, 0.6" 32 Pin PLDCC 32 Pad CLLCC 32 Pin CLDCC
WS27C010L	128K x 8 CMOS EPROM	C I M	100/120/150/200 120/150 120/130/150/200	32 Pin CERDIP, 0.6" 32 Pin CLDCC 32 Pad CLLCC 32 Pin PLDCC 32 Pin Plastic DIP, 0.6"
WS57C010M	128K x 8 CMOS EPROM	—	55/70	Advance Information
WS27C010F	128K x 8 CMOS EPROM	—	55/70/90/100	Advance Information
WS27C020L	256K x 8 CMOS EPROM	—	120/150/170/200	Advance Information
WS27C040L	512K x 8 CMOS EPROM	C M	120/150/170/200 150/170/200	32 Pin CERDIP, 0.6" 32 Pad CLLCC

CMOS PRODUCT SUMMARY (Cont.)

PART NO.	DESCRIPTION	TEMP	SPEED (ns)	PACKAGES
EPROM Memory Products (Wordwide)				
WS57C65	4K x 16 CMOS EPROM	C	55/70	44 Pad CLLCC 40 Pin CERDIP, 0.6″
WS57C257	16K x 16 CMOS EPROM	C I M	55/70 70/90 70/90	40 Pin CERDIP, 0.6″ 44 Pad CLLCC 44 Pin CLDCC
WS27C210L	64K x 16 CMOS EPROM	C M	100/120/150/200 120/150/200	40 Pin CERDIP, 0.6″ 44 Pin PLDCC 44 Pad CLLCC 44 Pin CLDCC
WS57C210M	64K x 16 CMOS EPROM Module	C M	55/70/90 70/90	40 Pin Ceramic S/B, 0.6″
WS27C210F	64K x 16 CMOS EPROM	—	55/70/90/100	Advance Information
WS27C220L	128K x 16 CMOS EPROM	—	120/150/170/200	Advance Information
WS27C240L	256K x 16 CMOS EPROM	—	120/150/170/200	Advance Information
Programmable System Devices				
MAP168	User-Configurable Peripheral with Memory	C M	40/45/55 45/55	44 Pad CLLCC 44 Pin PLDCC 44 Pin CLDCC 44 Pin CPGA
PSD301	User-Configurable Peripheral with Memory	—	120/150/200	Advance Information
PAC1000	User-Configurable Microcontroller	C I M	12/16/20 MHz 12/16 MHz 12/16 MHz	100 Pin Ceramic Quad Flatpack, Gull Wing 100 Pin Plastic Quad Flatpack, Gull Wing 88 Pin CPGA
SAM448	User-Configurable Microsequencer	C I M	20/25/30 MHz 20 MHz 20 MHz	28 Pin PLDCC 28 Pin CLDCC 28 Pin Plastic DIP, 0.3″ 28 Pin CERDIP, 0.3″
CMOS Logic Products				
WS5901	CMOS 4-Bit High-Speed Microprocessor Slice	C M	C/D C/D	40 Pin Plastic DIP, 0.6″ 40 Pin CERDIP, 0.6″
WS59016	CMOS 16-Bit High-Speed Microprocessor Slice	C M	C/D C/D	64 Pin Ceramic S/B, 0.9″ 68 Pin PLDCC 68 Pin CLDCC
WS59032	CMOS 32-Bit High-Speed Microprocessor Slice	C M	D/E D/E	101 Pin CPGA
WS5910A/B	CMOS Microprogram Controller	C M	20/30 MHz 20/30 MHz	40 Pin Plastic DIP, 0.6″ 40 Pin CERDIP, 0.6″

CMOS PRODUCT SUMMARY (Cont.)

PART NO.	DESCRIPTION	TEMP	SPEED (ns)	PACKAGES
CMOS Logic Products (Cont.)				
WS59510	CMOS 16 x 16 Multiplier Accumulator	C M	30/35/40/50 ns 40/50 ns	68 Pin PLDCC 68 Pin CPGA 64 Pin Plastic DIP, 0.9"
WS59520/521	CMOS Multilevel Pipeline Register	C M	22 ns 24 ns	24 Pin Plastic DIP, 0.3" 24 Pin CERDIP, 0.3"
WS59820	CMOS Bidirectional Bus Interface Registers	C M	23 ns 25 ns	68 Pin PLDCC 68 Pin CPGA
WS59820B	CMOS Bidirectional Bus Interface Registers	C M	23 ns 25 ns	68 Pin PLDCC 68 Pin CPGA
System Development Tools				
Memory-Silver	WSI EPROM/PROM-RPROM/Flash Programming Software, User's Manual, WSI-Support			
Memory-Gold	Memory-Silver, WS6000 MagicPro Programmer, WSI-Support			
PAC1000-Silver	PAC1000 Software, Software User's Manual, WSI-Support			
PAC1000-Gold	PAC1000-Silver, WS6000 MagicPro Programmer, WSI-Support			
MAP168-Silver	MAP168 Software, Software User's Manual, WSI-Support			
MAP168-Gold	MAP168-Silver, WS6000 MagicPro Programmer, WSI-Support			
SAM448-Silver	SAM448 Software, Software User's Manual, WSI-Support			
SAM448-Gold	SAM448-Silver, WS6000 MagicPro Programmer, WSI-Support			
WSI-Support	12-Month Software Update Service, 24-Hour Bulletin Board, Applications Hotline			
WS6000	Memory and PSD Programmer			
WS6001	MagicPro Adaptor, 28 Pin CLLCC Package, Memory			
WS6003	MagicPro Adaptor, 44 Pin PLDCC/CLDCC/CLLCC Package, MAP168			
WS6008	MagicPro Adaptor, 28 Pin 0.3" DIP, SAM448			
WS6009	MagicPro Adaptor, 28 Pin PLDCC/CLDCC/CLLCC Package, SAM448			
WS6010	MagicPro Adaptor, 88 Pin PGA Package, PAC1000			
WS6011	MagicPro Adaptor, 44 Pin PGA Package, MAP168			
WS6012	MagicPro Adaptor, 32 Pin CLDCC Package, Memory			
WS6013	MagicPro Adaptor, 100 Pin Quad Flatpack Package, PAC1000			
WS6014	MagicPro Adaptor, 44 Pin CLDCC/PLDCC Package, MAP168/PSD301			
WS6015	MagicPro Adaptor, 44 Pin PGA Package, MAP168/PSD301			

PART NO.	DESCRIPTION	TEMP	SPEED (ns)	PACKAGES
MAP168	User-Configurable Peripheral with Memory	C M	40/45/55 45/55	44 Pad CLLCC 44 Pin PLDCC 44 Pin CLDCC 44 Pin CPGA
MAP168-Silver MAP168-Gold	MAP168 Software, Software User's Manual, WSI-Support MAP168-Silver, WS6000 MagicPro Programmer, WSI-Support			
PSD301	User-Configurable Peripheral with Memory	—	120/150/200	Advance Information
SAM448	User-Configurable Microsequencer	C I M	20/25/30 MHz 20 MHz 20 MHz	28 Pin PLDCC 28 Pin CLDCC 28 Pin Plastic DIP, 0.3" 28 Pin CERDIP, 0.3"
SAM448-Silver SAM448-Gold	SAM448 Software, Software User's Manual, WSI-Support SAM448-Silver, WS6000 MagicPro Programmer, WSI-Support			
PAC1000	User-Configurable Microcontroller	C I M	12/16/20 MHz 12/16 MHz 12/16 MHz	100 Pin Ceramic Quad Flatpack, Gull Wing 100 Pin Plastic Quad Flatpack, Gull Wing 88 Pin CPGA
PAC1000-Silver PAC1000-Gold	PAC1000 Software, Software User's Manual, WSI-Support PAC1000-Silver, WS6000 MagicPro Programmer, WSI-Support			
WS27C64F	Military 8K x 8 CMOS EPROM	M	90/100	32 Pad CLLCC 28 Pin CERDIP, 0.6"
WS27C64L	8K x 8 CMOS EPROM	C I M	90/120/150/200 120 120/150/200	28 Pin CERDIP, 0.6" 28 Pin CERDIP, 0.3" 32 Pin PLDCC 28 Pin Plastic DIP, 0.6"
WS57C43B	4K x 8 CMOS PROM/RPROM	C I M	35/45/55/70 45/55 45/55/70	24 Pin CERDIP, 0.6" 28 Pin PLDCC 24 Pin Plastic DIP, 0.3" 24 Pin CERDIP, 0.3" 28 Pad CLLCC
WS57C43C	4K x 8 CMOS PROM/RPROM	—	25/30	Advance Information
WS57C45	2K x 8 Registered CMOS PROM/RPROM	C M	25/35 35/45	24 Pin CERDIP, 0.3" 28 Pad CLLCC 24 Pin Ceramic Flatpack 24 Pin Plastic DIP, 0.3"
WS57C49B	8K x 8 CMOS PROM/RPROM	C I M	35/45/55/70 45 45/55/70	24 Pin CERDIP, 0.6" 28 Pin PLDCC 24 Pin Plastic DIP, 0.6" 24 Pin CERDIP, 0.3" 28 Pad CLLCC 24 Pin Plastic DIP, 0.3" 24 Pin Ceramic Flatpack
WS57C49C	8K x 8 CMOS PROM/RPROM	—	25/30	Advance Information

NUMERICAL PRODUCT LISTING (Cont.)

PART NO.	DESCRIPTION	TEMP	SPEED (ns)	PACKAGES
WS57C51B	16K x 8 CMOS PROM/RPROM	C M	40/45/55/70 45/55/70	28 Pin CERDIP, 0.6" 32 Pin CLDCC 28 Pin CERDIP, 0.3" 32 Pad CLLCC
WS57C64F	8K x 8 CMOS EPROM	C I M	55/70 70 70	28 Pin CERDIP, 0.6" 32 Pad CLLCC 32 Pin PLDCC
WS57C65	4K x 16 CMOS EPROM	C	55/70	44 Pad CLLCC 40 Pin CERDIP, 0.6"
WS57C71C	32K x 8 CMOS RPROM	C M	40/45/55 55	28 Pin CERDIP, 0.6" 32 Pin CLDCC 28 Pin CERDIP, 0.3" 32 Pad CLLCC
WS5901	CMOS 4-Bit High-Speed Microprocessor Slice	C M	C/D C/D	40 Pin Plastic DIP, 0.6" 40 Pin CERDIP, 0.6"
WS5910A/B	CMOS Microprogram Controller	C M	20/30 MHz 20/30 MHz	40 Pin Plastic DIP, 0.6" 40 Pin CERDIP, 0.6"
WS6000	Memory and PSD Programmer			
WS6001	MagicPro Adaptor, 28 Pin CLLCC Package, Memory			
WS6003	MagicPro Adaptor, 44 Pin PLDCC/CLDCC/CLLCC Package, MAP168			
WS6008	MagicPro Adaptor, 28 Pin 0.3" DIP, SAM448			
WS6009	MagicPro Adaptor, 28 Pin PLDCC/CLDCC/CLLCC Package, SAM448			
WS6010	MagicPro Adaptor, 88 Pin PGA Package, PAC1000			
WS6011	MagicPro Adaptor, 44 Pin PGA Package, MAP168			
WS6012	MagicPro Adaptor, 32 Pin CLDCC Package, Memory			
WS6013	MagicPro Adaptor, 100 Pin Quad Flatpack Package, PAC1000			
WS6014	MagicPro Adaptor, 44 Pin CLDCC/PLDCC Package, MAP168/PSD301			
WS6015	MagicPro Adaptor, 44 Pin PGA Package, MAP168/PSD301			
WS27C010F	128K x 8 CMOS EPROM	—	55/70/90/100	Advance Information
WS27C010L	128K x 8 CMOS EPROM	C I M	100/120/150/200 120/150 120/130/150/200	32 Pin CERDIP, 0.6" 32 Pin CLDCC 32 Pad CLLCC 32 Pin PLDCC 32 Pin Plastic DIP, 0.6"
WS27C020L	256K x 8 CMOS EPROM	—	120/150/170/200	Advance Information
WS27C040L	512K x 8 CMOS EPROM	C M	120/150/170/200 150/170/200	32 Pin CERDIP, 0.6" 32 Pad CLLCC
WS27C128F	Military 16K x 8 CMOS EPROM	M	90	32 Pad CLLCC 28 Pin CERDIP, 0.6"

NUMERICAL PRODUCT LISTING (Cont.)

PART NO.	DESCRIPTION	TEMP	SPEED (ns)	PACKAGES
WS27C128L	16K x 8 CMOS EPROM	C I M	90/120/150 120 120/150/200	28 Pin CERDIP, 0.6" 32 Pin PLDCC 28 Pin Plastic DIP, 0.6" 28 Pin CERDIP, 0.3"
WS27C210F	64K x 16 CMOS EPROM	—	55/70/90/100	Advance Information
WS27C210L	64K x 16 CMOS EPROM	C M	100/120/150/200 120/150/200	40 Pin CERDIP, 0.6" 44 Pin PLDCC 44 Pad CLLCC 44 Pin CLDCC
WS27C220L	128K x 16 CMOS EPROM	—	120/150/170/200	Advance Information
WS27C240L	256K x 16 CMOS EPROM	—	120/150/170/200	Advance Information
WS27C256F	32K x 8 CMOS EPROM	C M	45/55/70 70/90	28 Pin CERDIP, 0.6" 32 Pad CLLCC 32 Pin CLDCC
WS27C256L	32K x 8 CMOS EPROM	C I M	90/120/150 120/150 120/150/200	28 Pin CERDIP, 0.6" 28 Pin CERDIP, 0.3" 32 Pad CLLCC 32 Pin PLDCC 32 Pin CLDCC 28 Pin Plastic DIP, 0.6"
WS27C512F	64K x 8 CMOS EPROM	C M	90 90/120	32 Pad CLLCC 28 Pin CERDIP, 0.6"
WS27C512L	64K x 8 CMOS EPROM	C M	100/120/150 150/200	28 Pin CERDIP, 0.6" 32 Pin PLDCC 32 Pad CLLCC 32 Pin CLDCC
WS57C010M	128K x 8 CMOS EPROM Module	—	55/70	Advance Information
WS57C128F	16K x 8 CMOS EPROM	C I M	55/70 70 70	28 Pin CERDIP, 0.6" 32 Pad CLLCC
WS57C191B	2K x 8 CMOS PROM/RPROM	C I M	35/45 45 45/55	24 Pin CERDIP, 0.6" 28 Pin PLDCC 24 Pin Plastic DIP, 0.6" 28 Pad CLLCC
WS57C210M	64K x 16 CMOS EPROM Module	C M	55/70/90 70/90	40 Pin Ceramic S/B, 0.6"
WS57C256F	32K x 8 CMOS EPROM	C I M	40/55/70/90 70/90 55/70/90	28 Pin CERDIP, 0.6" 32 Pad CLLCC 32 Pin CLDCC

NUMERICAL PRODUCT LISTING (Cont.)

PART NO.	DESCRIPTION	TEMP	SPEED (ns)	PACKAGES
WS57C257	16K x 16 CMOS EPROM	C I M	55/70 70/90 70/90	40 Pin CERDIP, 0.6″ 44 Pad CLLCC 44 Pin CLDCC
WS57C291B	2K x 8 CMOS PROM/RPROM	C I M	35/45 45 45/55	24 Pin Plastic DIP, 0.3″ 24 Pin CERDIP, 0.3″
WS57C512F	64K x 8 CMOS EPROM	—	55/70/90	Advance Information
WS59016	CMOS 16-Bit High-Speed Microprocessor Slice	C M	C/D C/D	64 Pin Ceramic S/B, 0.9″ 68 Pin PLDCC 68 Pin CLDCC
WS59032	CMOS 32-Bit High-Speed Microprocessor Slice	C M	D/E D/E	101 Pin CPGA
WS59510	CMOS 16 x 16 Multiplier Accumulator	C M	30/35/40/50 40/40	68 Pin PLDCC 68 Pin CPGA 64 Pin Plastic DIP, 0.9″
WS59520/521	CMOS Multi-Level Pipeline Register	C M	22 24	24 Pin Plastic DIP, 0.3″ 24 Pin CERDIP, 0.3″
WS59820	CMOS Bidirectional Bus Interface Registers	C M	23 25	68 Pin PLDCC 68 Pin CPGA
WS59820B	CMOS Bidirectional Bus Interface Registers	C M	23 25	68 Pin PLDCC 68 Pin CPGA
Memory-Silver	WSI EPROM/PROM-RPROM/Flash Programming Software, User's Manual, WSI-Support			
Memory-Gold	Memory-Silver, WS6000 MagicPro Programmer, WSI-Support			
WSI-Support	12-Month Software Update Service, 24-Hour Bulletin Board, Applications Hotline			

HIGH-PERFORMANCE CMOS PRODUCTS

WS57C----- **-35** **D** **I** **B**

Basic Part Number

Manufacturing Process:

(Blank) = WSI Standard Manufacturing Flow

B = MIL-STD-883C Manufacturing Flow

Operating Temperature Range:

(Blank) = Commercial: 0° to +70°C
V_{CC}: +5V ± 5%

I = Industrial: −40° to +85°C
V_{CC}: +5V ± 10%

M = Military: −55° to +125°C
V_{CC}: +5V ± 10%

Package:

		Window
A	= PPGA Plastic Pin Grid Array	No
B	= 0.900″ Size Brazed Ceramic DIP	No
C	= CLLCC Ceramic Leadless Chip Carrier	Yes*
D	= 0.600″ CERDIP	Yes
F	= Ceramic Flatpack	Yes*
G	= CPGA Ceramic Pin Grid Array	No
H	= Ceramic Flatpack	No*
J	= Plastic Leaded Chip Carrier	No*
K	= 0.300″ Thin CERDIP	No*
L	= CLDCC Ceramic Leaded Chip Carrier	Yes*
N	= CLDCC Ceramic Leaded Chip Carrier	No*
P	= 0.600″ Plastic DIP	No
Q	= Plastic Quad Flatpack	No*
R	= Ceramic Side Brazed	Yes
S	= 0.300″ Thin Plastic DIP	No
T	= 0.300″ Thin CERDIP	Yes
W	= Waffle Packed Dice	—
X	= Ceramic Pin Grid Array	Yes
Y	= 0.600″ CERDIP	No
Z	= CLLCC	No

Speed:

−35 = 35 ns
−55 = 55 ns
−70 = 70 ns
Etc.

*Surface Mount

ANALOG DEVICES	WSI
ADSP1010	WS59510
ADSP1010A	WS59510

AMD	WSI
AM27C49	WS57C49/49B
AM27C191	WS57C291B
AM27C256	WS27C256L,F
AM27C291	WS57C291B
AM27C1024	WS27C210L
AM27PS43	WS57C43/43B
AM27S43	WS57C43/43B
AM27S43A	WS57C43/43B
AM27S45	WS57C45
AM27S49	WS57C49/49B
AM27S51	WS57C51/51B
AM27S51A	WS57C51/51B
AM27S191	WS57C191B
AM27S291	WS57C291B
AM27010	WS27C010L
AM27512	WS27C512L
AM29C101	WS59016*
AM29L510	WS59510
AM2901	WS5901
AM2910A	WS5910A/B
AM29510	WS59510
AM29520	WS59520/21
AM29521	WS59520/21

ATMEL	WSI
27C512	WS27C512L,F
AT27C256	WS27C256L,F
AT27HC64	WS57C64F
AT27HC191	WS57C191B
AT27HC256	WS57C256F
AT27HC291	WS57C291B
AT27HC641/2	WS57C49/49B

CYPRESS	WSI
CY2901	WS5901
CY7C245	WS57C45
CY7C245A	WS57C45
CY7C251	WS57C51/51B
CY7C253	WS57C51/51B
CY7C254	WS57C51/51B
CY7C261	WS57C49/49B
CY7C263	WS57C49/49B
CY7C264	WS57C49/49B
CY7C274	WS57C256F
CY7C291	WS57C291/B
CY7C292	WS57C191/B
CY7C510	WS59510
CY7C910	WS5910A/B
CY7C9101	WS59016*

EXCEL	WSI
46C16	WS57C291B

FAIRCHILD	WSI
29F01	WS5901
29F10	WS59510A/B
93Z510	WS57C291B
93Z511	WS57C191B
93Z511	WS57C291B
93Z512	WS57C291B
93Z565	WS57C49/49B
93Z667	WS57C49/49B

FUJITSU	WSI
MBM27C256	WS27C256L,F
MBM27C512	WS27C512L
MBH38H	WS57C191B
MBH38-SK	WS57C291B
MB7142	WS57C43/43B
MB7143	WS57C49/49B
MB7144E	WS57C49/49B
MB7144H	WS57C49/49B

GI	WSI
27C256	WS27C256L,F
27C512	WS27C512L
27C1024	WS27C010L
27HC64	WS57C64F
27HC641	WS57C49/49B
27256	WS27C256L,F
RO9256	WS27C256L,F

GOLDSTAR	WSI
GL3620	WS57C64F
GM27HC64	WS57C64F

HARRIS	WSI
HM-76161	WS57C191B
HM-76641	WS57C49/49B
HM-76641A	WS57C49/49B

HITACHI	WSI
HN25169	WS57C191B
HN25169	WS57C291B
HN27C128	WS27C128L
HN27C256	WS27C256L,F
HN27C101G	WS27C010L
HN27C301	WS27C010L
HN27512G	WS27C512L

ICT	WSI
27CX321	WS57C43/43B
27CX322	WS57C43/43B
27CX641	WS57C49/49B
27CX642	WS57C49/49B

PRODUCT CROSS REFERENCE (Cont.)

IDT	WSI
IDTT4210	WS59510
IDT39C01	WS5901
IDT39C10	WS59510A/B
IDT49C401	WS59016*
29FCT521	WS59520/521

INTEL	WSI
1M29C510	WS59510
27C128/A	WS27C128L
27C256	WS27C256L,F
27010	WS27C010L
27210	WS27C210L
27512	WS27C512L

LDI	WSI
LMA1010	WS59510
LMA2010	WS59510
L29C520	WS59520/21
L29C521	WS59520/21
L429C01	WS5901

LSI LOGIC	WSI
L64010	WS59510
L64012	WS59510

MATRA-HARRIS	WSI
MS2010	WS59510

MITEL	WSI
M27C256	WS27C256L,F
M27256	WS27C256L,F
M5L27256	WS27C256L,F

MITSUBISHI	WSI
M5L27C128	WS27C128L
M5L27256K	WS27C256L,F
M27C512	WS27C512L

MMI	WSI
53S3281	WS57C43/43B
63S1681	WS57C191B
63S1681A	WS57C191B
63S1681A	WS57C291B
63S3281	WS57C43/43B
631681	WS57C291B

MOTOROLA	WSI
MCM76	WS57C191B
MCM76160	WS57C291B
MCM76161	WS57C291B

NATIONAL	WSI
87S321	WS57C43/43B
93Z665C	WS57C49/49B
93Z667C	WS57C49/49B
DM77S321	WS57C43/43B
DM87S291	WS57C291B
DM87S291A	WS57C291B
DM87S291B	WS57C291B
DM87S321	WS57C43/43B
DM87SR191	WS57C191B
DM87SR193	WS57C191B
NMC27C256	WS27C256L,F
NMC27C512A	WS27C512L
NMC27C1023	WS27C010L
NMC27C1024	WS27C210L
VM27C256	WS27C256L,F

NEC	WSI
27HC65	WS57C49/49B
M27C256	WS27C256L,F
µPB429	WS57C191B
µPB429	WS57C291B
µPD27C256	WS57C256F
µPD27C512D	WS27C512L
µPD27C1024	WS27C210L

OKI	WSI
MSM27C256	WS27C256L,F
M27512	WS27C512L

RAYTHEON	WSI
29671	WS57C43/43B
29671A	WS57C43/43B
29681	WS57C291B
29681A	WS57C291B
29683A	WS57C191B
39VP864	WS57C49/49B

SANYO	WSI
LA7620	WS57C64F

SEEQ	WSI
36C16	WS57C191B
36C32	WS57C43/43B
36S16	WS57C291B
27C256	WS57C256L,F
2764	WS57C64F
27256	WS57C256L,F

SHARP	WSI
LH5749	WS57C49/49B
LH5763	WS57C64F
LH57127	WS57C51/51B
LH57191	WS57C191B
LH57256	WS57C256F
SH5762	WS57C49/49B

PRODUCT CROSS REFERENCE (Cont.)

SIGNETICS	WSI
27C256	WS57C256L,F
27C512	WS27C512L
27HC641	WS57C49/49B
27HC642	WS57C49/49B
N82HS321	WS57C43/43B
N82HS641	WS57C49/49B
N82HS1281	WS57C51/51B
N82S191	WS57C191B
N82S191	WS57C291B
N82S191A	WS57C191B
N82S191A	WS57C291B
N82S191B	WS57C191B
N82S191B	WS57C291B
N82S641	WS57C49/49B

SPRAGUE	WSI
SCM27C256	WS27C256L,F

SSI	WSI
SS1203	WS57C49/49B

THOMSON	WSI
JBP38S165	WS57C191B
JBP38S165	WS57C291B
TS27C256	WS27C256L,F

TI	WSI
38S165	WS57C191B
38S165	WS57C291B
SMJ27C128	WS27C128L
SMJ27C256	WS27C256L,F
SMJ27C512	WS27C512L
SN74HCT9510	WS59510
TICPAL1010	WS59510
TMS27C128	WS27C128L
TMS27C256	WS27C256L,F
TMS27C292	WS57C191B
TMS27C292	WS57C291B
TMS278C49	WS57C49/49B

TOSHIBA	WSI
TMM27256	WS27C256L,F
TMM27512D	WS27C512L

TRW	WSI
TMC2210	WS59510

WEITEK	WSI
WTL1010	WS59510
WTL2010	WS59510
WTL2245	WS59510

*Functional Equivalent

ADVANCE INFORMATION/PRELIMINARY/ FINAL DEFINED

ADVANCE INFORMATION:
A WSI product data sheet marked "Advance Information" on its cover page describes a product that is in the planning stages at WSI at the time this book went to press. Design parameters and objectives are included in the data sheet but are subject to change before the actual product is formally introduced. Please contact your WSI Sales Representative or Distributor for availability status.

PRELIMINARY:
A WSI product data sheet marked "Preliminary" on its cover page describes a product that requires further characterization testing. Functional parameters are "frozen" but certain electrical limits may be subject to slight change before the data sheet is "Final." Please contact your WSI Sales Representative or Distributor for price and availability.

FINAL:
A WSI product data sheet without either "Advance Information" or "Preliminary" on the cover page describes a product that has completed all characterization and reliability testing. All functional and electrical parameters are "frozen." Please contact your WSI Sales Representative or Distributor for price and availability.

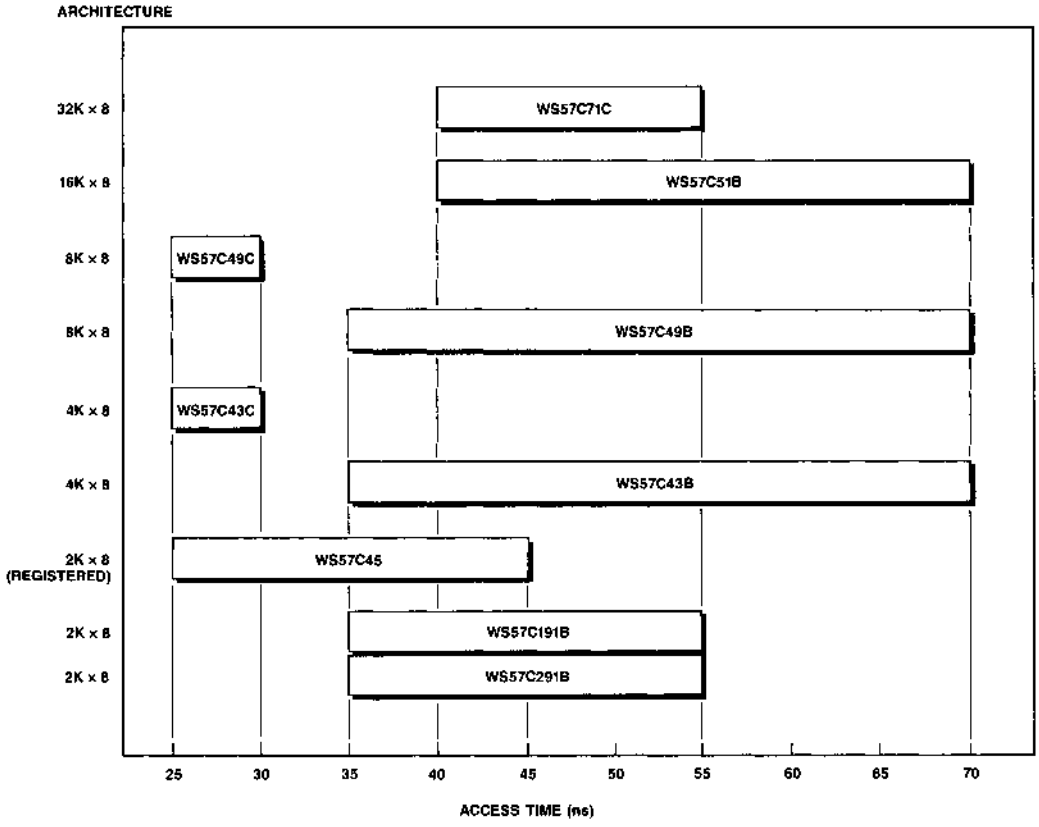
WAFERSCALE INTEGRATION, INC.

SECTION INDEX

PROM/RPROM MEMORY PRODUCTS

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 800-562-6363.

PROM/RPROM SELECTION GUIDE



WAFERSCALE INTEGRATION, INC.

HIGH SPEED 2K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD Nos. 5962-87650/5962-88734**
- **Pin Compatible with AM27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C191B/291B is an extremely HIGH PERFORMANCE 16K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power of its Bipolar counterparts.

A further advantage of the WS57C191B/291B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C191B/291B is 100% tested with worst case test patterns both before and after assembly.

The WS57C191B/291B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

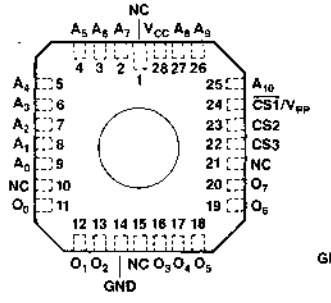
MODE SELECTION

MODE \ PINS	$\overline{CS1}/V_{PP}$	CS2	CS3	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Program	V_{PP}	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	X	X	V_{IL}	V_{CC}	High Z

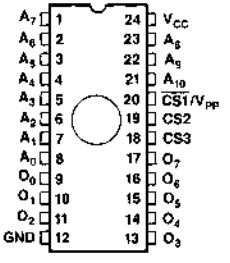
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C191B/291B-35	WS57C191B/291B-45	WS57C191B/291B-55
Address Access Time (Max)	35 ns	45 ns	55 ns
Output Enable Time (Max)	20 ns	20 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

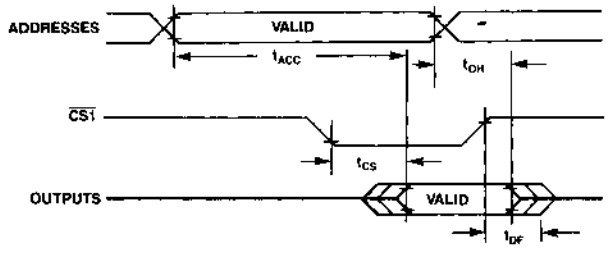
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		35	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C191B/291B-35		57C191B/291B-45		57C191B/291B-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55	ns
$\overline{CS}$ to Output Delay	t_{CE}		20		20		20	
Output Disable to Output Float	t_{DF}		20		20		20	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM

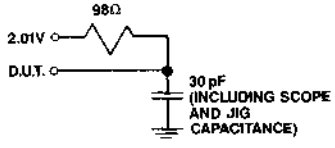


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES:
4. This parameter is only sampled and is not 100% tested.
5 Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

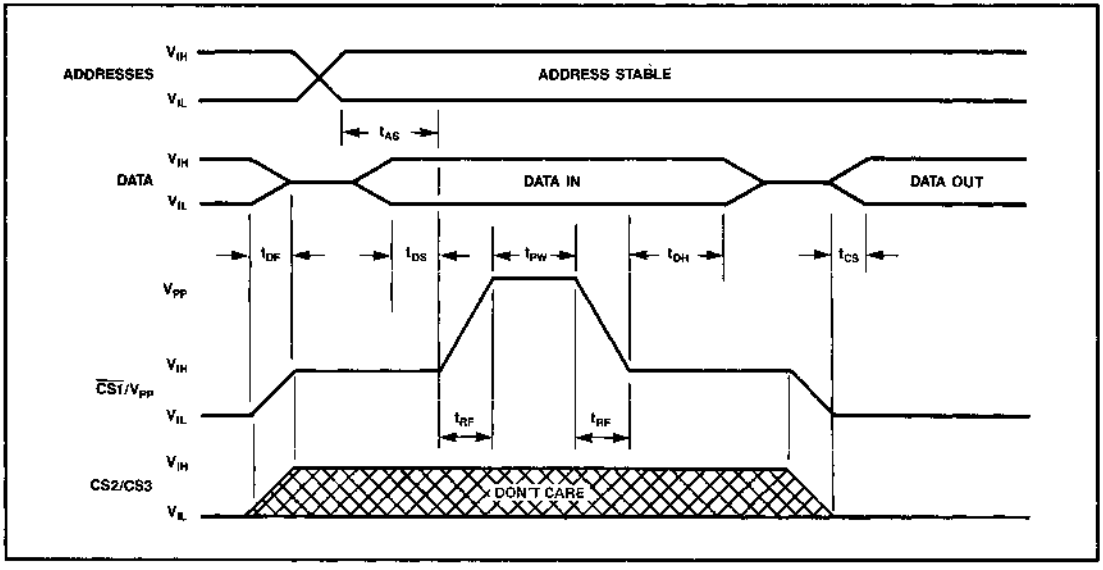
NOTE: 6. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}	2		30	ns
Data Setup Time	t_{DS}				µs
Program Pulse Width (Note 7)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 7. For programmers utilizing a one shot programming pulse, a 10 ms pulse width should be used.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191B-35P	35	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C191B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C191B-45DI	45	24 Pin CERDIP, 0.6"	D1	Industrial	Standard
WS57C191B-45DMB	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C191B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C191B-45P	45	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C191B-55CMB	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C191B-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C291B-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C291B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C291B-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C291B-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C291B-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 4K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with AM27S43 and N82S321 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **Available in 300 Mil Dip**

2

GENERAL DESCRIPTION

The WS57C43B is an extremely HIGH PERFORMANCE 32K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C43B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C43B is 100% tested with worst case test patterns both before and after assembly.

The WS57C43B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs. It also uses the same programming algorithm as its predecessor the WS57C43.

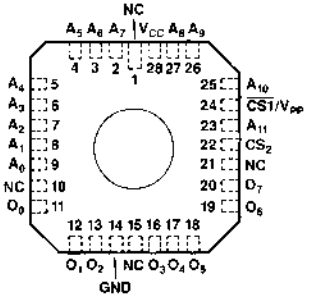
MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	CS2	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	V_{CC}	High Z
Output Disable	X	V_{IL}	V_{CC}	High Z
Program	V_{PP}	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{CC}	D_{OUT}

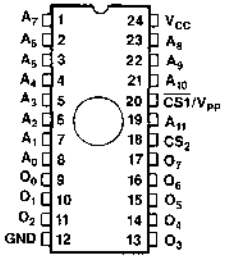
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C43B-35	WS57C43B-45	WS57C43B-55	WS57C43B-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

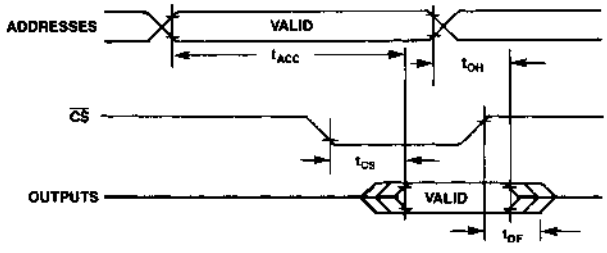
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		35	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs. $V_{IL} \leq 0.8V$. $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C43B-35		57C43B-45		57C43B-55		57C43B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		25		25		25	
Output Disable to Output Float	t_{DF}		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM

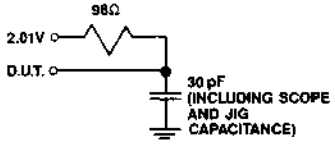


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		30	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

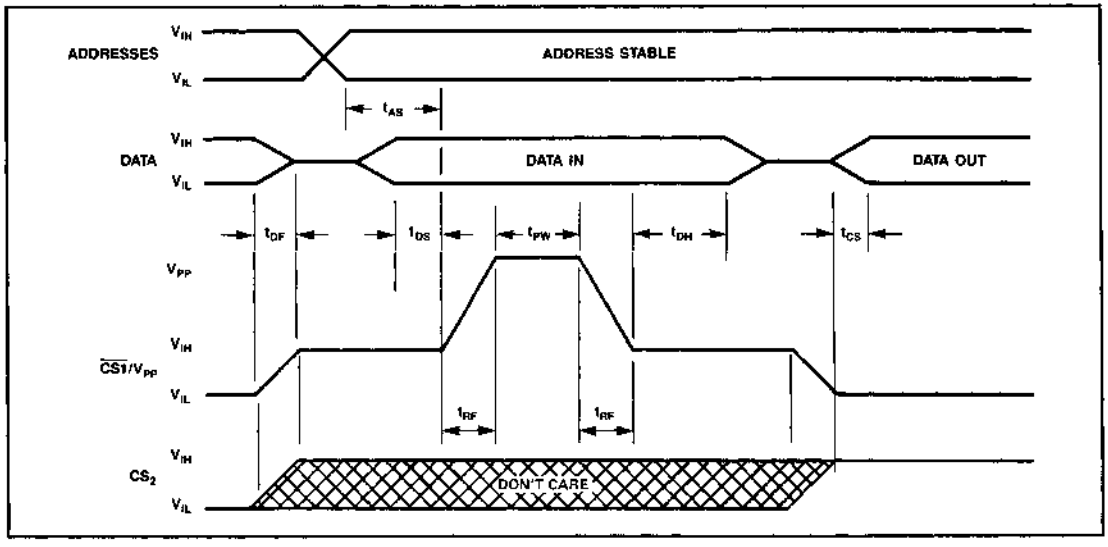
NOTE: 6. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C43B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43B-35S	35	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C43B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C43B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-45DI	45	24 Pin CERDIP, 0.6"	D1	Industrial	Standard
WS57C43B-45DMB	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C43B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C43B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C43B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C43B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C43B-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C43B-45Y	45	24 Pin CERDIP, 0.6"	Y3	Comm'l	Standard
WS57C43B-55CMB	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C43B-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C43B-55TI	55	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C43B-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C43B-55Y	55	24 Pin CERDIP, 0.6"	Y3	Comm'l	Standard
WS57C43B-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C43B-70TMB	70	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

HIGH SPEED 4K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 25 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with AM27S43 and N82S321 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **Available in 300 Mil Dip**

GENERAL DESCRIPTION

The WS57C43C is an extremely HIGH PERFORMANCE 32K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C43C over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C43C is 100% tested with worst case test patterns both before and after assembly.

The WS57C43C is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs. It also uses the same programming algorithm as its predecessor the WS57C43.

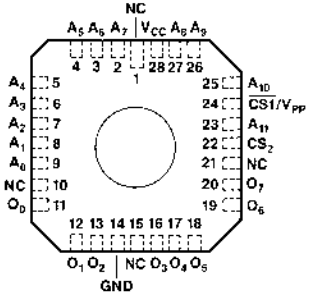
MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	CS2	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	V_{CC}	High Z
Output Disable	X	V_{IL}	V_{CC}	High Z
Program	V_{PP}	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{CC}	D_{OUT}

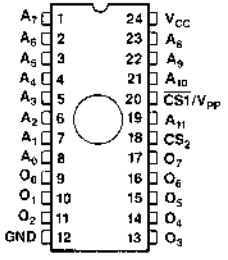
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C43C-25	WS57C43C-30
Address Access Time (Max)	25 ns	30 ns
Output Enable Time (Max)	15 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

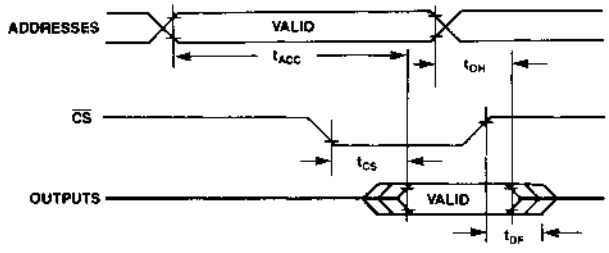
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		35	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1. CMOS Inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C43C-25		WS57C43C-30		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		25		30	ns
$\overline{CS}$ to Output Delay	t_{CS}		15		20	
Output Disable to Output Float	t_{DF}		20		25	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM

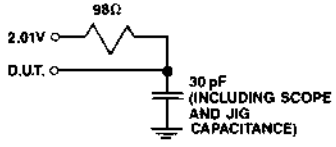


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		30	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

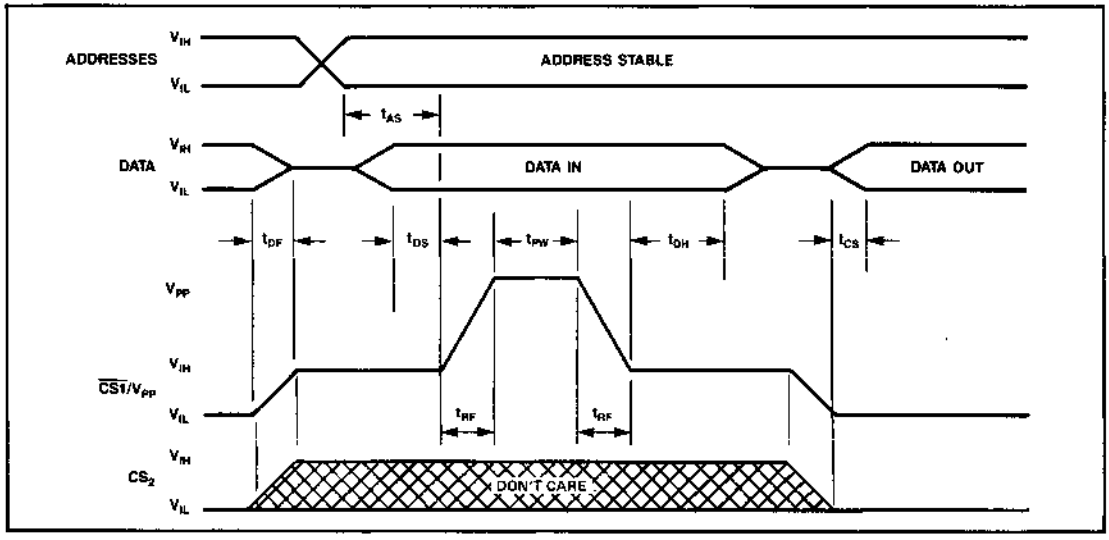
NOTE: 6. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



WAFERSCALE INTEGRATION, INC.

HIGH-SPEED 2K × 8 REGISTERED CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 25 ns Setup
  - — 12 ns Clock to Output
- **Low Power Consumption**
- **Fast Programming**
- **Programmable Synchronous or Asynchronous Output Enable**
- **DESC SMD Nos. 5962-88735/5962-87529**
- **Pin Compatible with AM27S45 and CY7C245**
- **Immune to Latch-Up**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**
- **Programmable Asynchronous Initialize Register**

2

GENERAL DESCRIPTION

The WS57C45 is an extremely HIGH PERFORMANCE 16K UV Erasable Registered CMOS RPROM. It is a direct drop-in replacement for such devices as the AM27S45 and CY7C245.

To meet the requirements of systems which execute and fetch instructions simultaneously, an 8-bit parallel data register has been provided at the output which allows RPROM data to be stored while other data is being addressed.

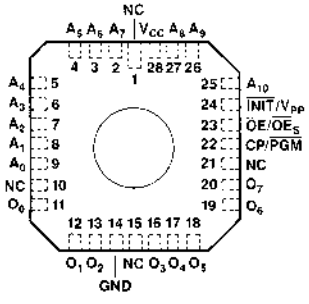
An asynchronous initialization feature has been provided which enables a user programmable 2049th word to be placed on the outputs independent of the system clock. This feature can be used to force an initialize word or provide a preset or clear function.

A further advantage of the WS57C45 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This enables the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C45 RPROM is 100% tested with worst case test patterns both before and after assembly.

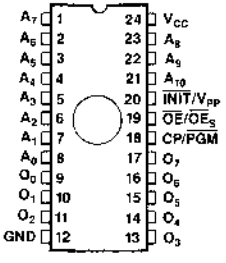
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP/ Flatpack



PRODUCT SELECTION GUIDE

PARAMETER	WS57C45-25	WS57C45-35	WS57C45-45
Set Up Time (Max)	25 ns	35 ns	45 ns
Clock to Output (Max)	12 ns	15 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5 ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		20	mA
			Military		30	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		25	
			Military		35	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 2 mA/MHz for A.C. power component.
4. This parameter is only sampled and is not 100% tested.

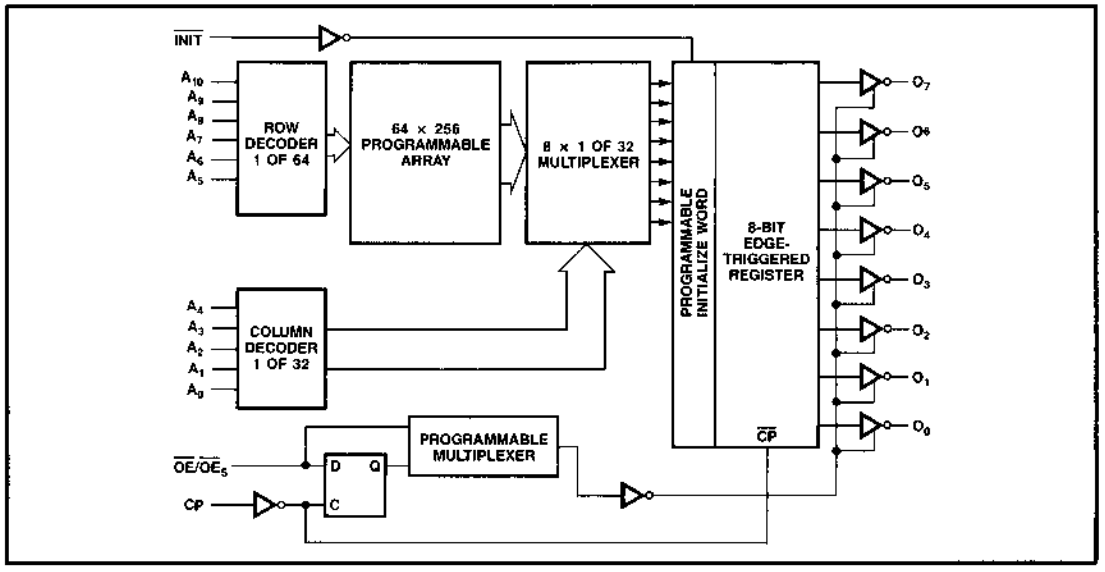
CAPACITANCE[4]

PARAMETERS	DESCRIPTION	TEST CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V	8	

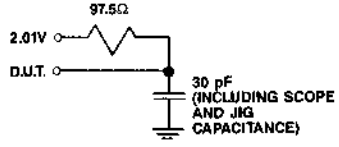
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C45-25		WS57C45-35		WS57C45-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Setup to Clock HIGH	t_{SA}	25		35		45		ns
Address Hold From Clock HIGH	t_{HA}	0		0		0		
Clock HIGH to Valid Output	t_{CO}		12		15		25	
Clock Pulse Width	t_{PWC}	15		20		20		
$\overline{OE}_S$ Setup to Clock HIGH	t_{SOE_S}	12		15		15		
$\overline{OE}_S$ Hold From Clock HIGH	t_{HOE_S}	5		5		5		
Delay From $\overline{INIT}$ to Valid Output	t_{DI}		20		20		35	
$\overline{INIT}$ Recovery to Clock HIGH	t_{RI}	15		20		20		
$\overline{INIT}$ Pulse Width	t_{PWI}	15		20		25		
Active Output From Clock HIGH	t_{LZC}		15		20		30	
Inactive O .tput From Clock HIGH	t_{HZC}		15		20		30	
Active Output From $\overline{OE}$ LOW	t_{LZOE}		15		20		30	
Inactive Output From $\overline{OE}$ HIGH	t_{HZOE}		15		20		30	

BLOCK DIAGRAM



TEST LOAD (High Impedance Test Systems)

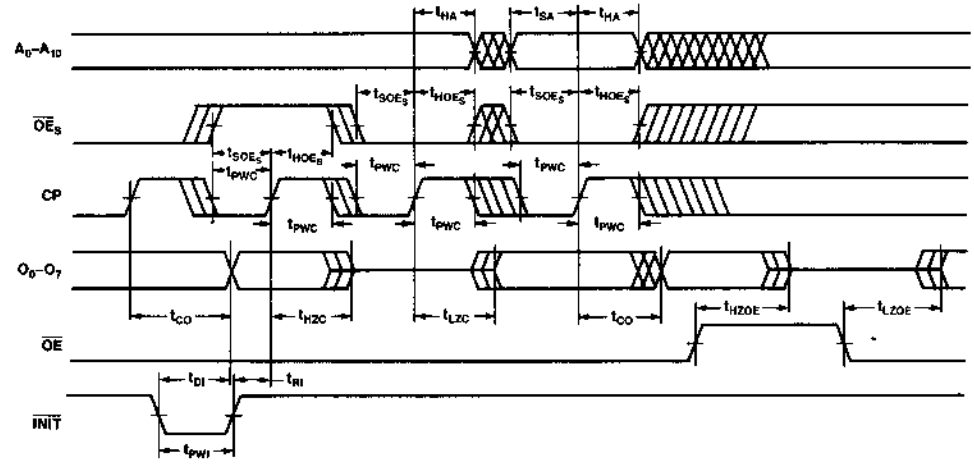


TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

AC READ TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

The WS57C45 is an electrically programmable read only memory produced with WSI's patented high-performance self-aligned split-gate CMOS EPROM technology. It is organized as 2048 x 8 bits and is pin-for-pin compatible with bipolar TTL fuse link PROMs. The WS57C45 includes a D-type 8-bit data register on-chip which reduces the complexity and cost of microprogrammed pipelined systems where PROM data is held temporarily in a register. The circuit features a programmable synchronous ($\overline{OE_S}$) or asynchronous ($\overline{OE}$) output enable and asynchronous initialization ($\overline{INIT}$).

The programmed state of the enable pin ($\overline{OE_S}$ or $\overline{OE}$) will dictate the state of the outputs at power up. If $\overline{OE_S}$ has been programmed, the outputs will be in the OFF or high impedance state. If $\overline{OE}$ has been programmed, the outputs will be OFF or high impedance only if the $\overline{OE}$ input is HIGH. Data is read by applying the address to inputs A_{10}–A_0 and a LOW to the enable input. The data is retrieved and loaded into the master section of the 8-bit data register during the address set-up time. The data is transferred to the slave output of the data register at the next LOW to HIGH clock (CP) transition. Then the output buffers present the data on the outputs (0_7–0_0).

When using the asynchronous enable ($\overline{OE}$), the output buffers may be disabled at any time by switching the enable input to a logic HIGH. They may be re-enabled by switching the enable to a logic LOW.

When using the synchronous enable ($\overline{OE_S}$), the outputs revert to a high impedance or OFF state at the next positive clock edge following the $\overline{OE_S}$ input transition to a HIGH state. The output will revert to the active state following a positive clock edge when the $\overline{OE_S}$ input is at a LOW state. The address and synchronous enable inputs are free to change following a positive clock edge since the output will not change until the next low to high clock transition. This enables accessing the next data location while previously addressed data is present on the outputs.

To avoid race conditions and simplify system timing, the 8-bit edge triggered data register clock is derived directly from the system clock.

The WS57C45 has an asynchronous initialize input ($\overline{INIT}$). This function can be used during power-up and time-out periods to implement functions such as a start address or initialized bus control word. The $\overline{INIT}$ input enables the contents of a 2049th 8-bit word to be loaded directly into the output data register. The $\overline{INIT}$ input can be used to load any 8-bit data pattern into the register since each bit is programmable by the user. When unprogrammed, activating $\overline{INIT}$ will result in clearing the register (outputs LOW). When all bits are programmed, activating $\overline{INIT}$ results in PRESETting the register (outputs HIGH).

When activated LOW, the $\overline{INIT}$ input results in an immediate load of the 2049th word into both the master and slave sections of the output register. This is independent of any other input including the clock (CP) input. The initialize data will be present at the outputs after the asynchronous enable ($\overline{OE}$) is taken to a LOW state.

Programming Information

Apply power to the WS57C45 for normal read mode operation with CP/$\overline{PGM}$, $\overline{OE}/\overline{OE_S}$ and $\overline{INIT}/V_{PP}$ at V_{IH}. Then take $\overline{INIT}/V_{PP}$ to V_{PP}. The part is then in the program inhibit mode operation and the output lines are in a high impedance state. Refer to figure 5. As shown in figure 5, address, program and verify one byte of data. Repeat this sequence for each location to be programmed.

When intelligent programming is used, the program pulse width is 1 ms in length. Each address location is programmed and verified until it verifies correctly up to and including 5 times. After the location verifies, an additional programming pulse should be applied that is X1 times in duration of the sum of the previous programming pulses before proceeding on to the next address and repeating the process.

Initialization Byte Programming

The WS57C45 has a 2049th byte of data that can be used to initialize the value of the data register. This byte contains the value "0" when it is shipped from the factory. The user must program the 2049th byte with a value other than "0" for data register initialization if that value is not desired. Except for the following details, the user may program the 2049th byte in the same manner as the other 2048 bytes. First, since all 2048 addresses are used up, a super voltage address feature is used to enable an additional address. The actual address includes V_{PP} on A_1 and V_{IL} on A_2. Refer to the Mode Selection table. The programming and verification of the Initial Byte is accomplished operationally by performing an initialize function.

Synchronous Enable Programming

The WS57C45 contains both a synchronous and asynchronous enable feature. The part is delivered configured in the asynchronous mode and only requires alteration if the synchronous mode is required. This is accomplished by programming an on-chip EPROM cell. Similar to the Initial Byte, this function is enabled and addressed by using a super voltage. Referring to the Mode Selection table, V_{PP} is applied to A_1 followed by V_{IH} applied to A_2. This procedure addresses the EPROM cell that programs the synchronous enable feature. The EPROM cell is programmed with a 10 ms program pulse on CP/$\overline{PGM}$. It does not require any data since there is no selection as to how synchronous enable may be programmed, only if it is to be programmed.

Synchronous Enable Verification

The WS57C45's synchronous enable function is verified operationally. Apply power for read operation with $\overline{OE}/\overline{OE_S}$ and $\overline{INIT}/V_{PP}$ at V_{IH} and take the clock (CP/$\overline{PGM}$) from V_{IL} to V_{IH}. The output data bus should be in a high impedance state. Next take $\overline{OE}/\overline{OE_S}$ to V_{IL}. The outputs will remain in the high impedance state. Take the clock (CP/$\overline{PGM}$) from V_{IL} to V_{IH} and the outputs will now contain the data that is present. Take $\overline{OE}/\overline{OE_S}$ to V_{IH}. The output should remain driven. Clocking CP/$\overline{PGM}$ once more from V_{IL} to V_{IH} should place the outputs again in a high impedance state.

Blank Check

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C45 has all 2048 bytes in the '0' state. "1's" are loaded into the WS57C45 through the procedure of programming.

MODE SELECTION

MODE	READ OR OUTPUT DISABLE	PIN FUNCTION					OUTPUTS
		A_2	CP/$\overline{PGM}$	($\overline{OE}/\overline{OE_S}$)/$\overline{VFY}$	$\overline{INIT}/V_{PP}$	A_1	
Read[6]		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable		X	X	V_{IH}	V_{IH}	X	High Z
Program[5,7]		X	V_{IL}	V_{IH}	V_{PP}	X	Data In
Program Verify[5,7]		X	V_{IH}	V_{IL}	V_{PP}	X	Data Out
Program Inhibit[5,7]		X	V_{IH}	V_{IH}	V_{PP}	X	High Z
Intelligent Program[5,7]		X	V_{IL}	V_{IH}	V_{PP}	X	Data In
Program Synch Enable[7]		V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{PP}	High Z
Program Initial Byte[7]		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{PP}	Data In
Blank Check		X	V_{PP}	V_{IH}	V_{IL}	X	Zeros

NOTES:
5. X = Don't care but not to exceed V_{PP}.
6. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
7. During programming and verification, all unspecified pins to be at V_{IL}.

FIGURE 5. PROM PROGRAMMING WAVEFORMS

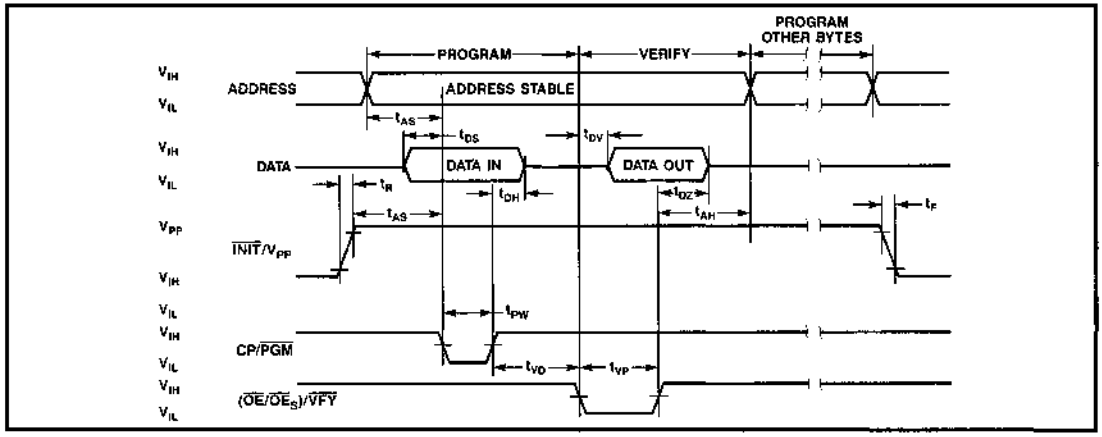


FIGURE 6. INITIAL BYTE PROGRAMMING WAVEFORMS

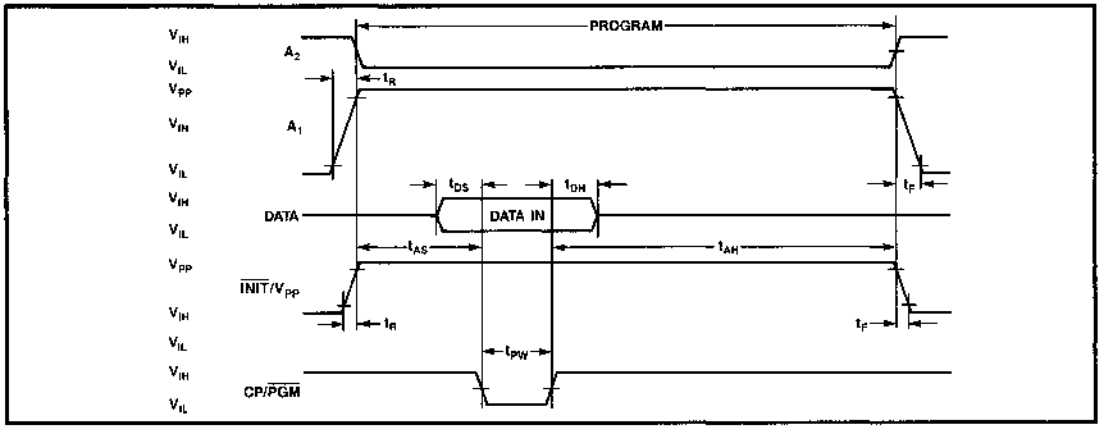
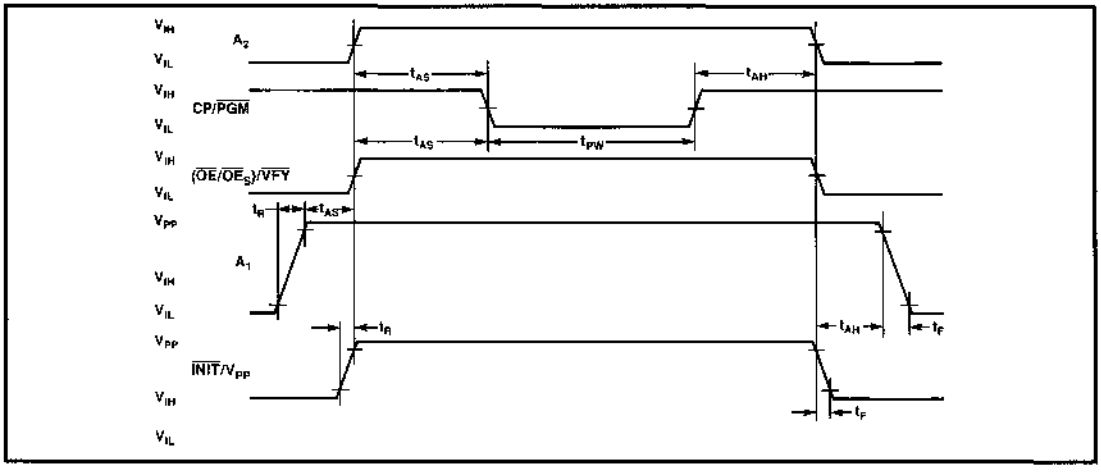


FIGURE 7. PROGRAM SYNCHRONOUS ENABLE



PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current $V_{IN} = V_{CC}$ or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

NOTE: 8. V_{PP} must not be greater than 14 volts including overshoot

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{PW}	Programming Pulse Width	0.1	10	ms
t_{AS}	Address Setup Time	1.0		µs
t_{DS}	Data Setup Time	1.0		µs
t_{AH}	Address Hold Time	1.0		µs
t_{DH}	Data Hold Time	1.0		µs
t_R, t_F	V_{PP} Rise and Fall Time	1.0		µs
t_{VD}	Delay to $\overline{VFY}$	1.0		µs
t_{VP}	$\overline{VFY}$ Pulse Width	2.0		µs
t_{DV}	$\overline{VFY}$ Data Valid		1.0	µs
t_{DZ}	$\overline{VFY}$ HIGH to High Z		1.0	µs

PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C45-25T	25	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-35CMB	35	28 pad CLLCC	C1	Military	MIL-STD-883C
WS57C45-35FMB	35	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C45-35S	35	24 Pin Plastic Dip, 0.3"	S1	Comm'l	Standard
WS57C45-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C45-35TMB	35	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C45-45KMB	45	24 Pin CERDIP, 0.3"	K1	Military	MIL-STD-883C
WS57C45-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 8K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD 5962-87515**
- **Pin Compatible with AM27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C49B is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C49B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C49B is 100% tested with worst case test patterns both before and after assembly.

A unique feature of the WS57C49B is a designed-in output hold from address change. This allows the WS57C49B to be run at a cycle time equal to the address access time. While addresses are changing, output data is held long enough to be latched into external circuitry.

The WS57C49B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

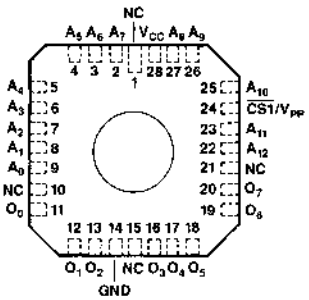
MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{CC}	D_{OUT}

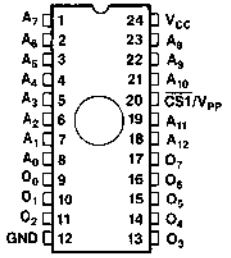
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP/ Flatpack



PRODUCT SELECTION GUIDE

PARAMETER	WS57C49B-35	WS57C49B-45	WS57C49B-55	WS57C49B-70
Address Access Time (Max)	35 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

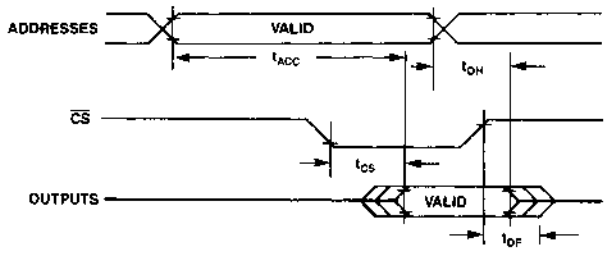
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		35	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1. CMOS Inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL Inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C49B-35		57C49B-45		57C49B-55		57C49B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		25		25		25	
Output Disable to Output Float	t_{DF}		25		25		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM

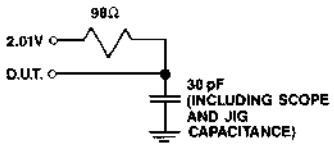


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

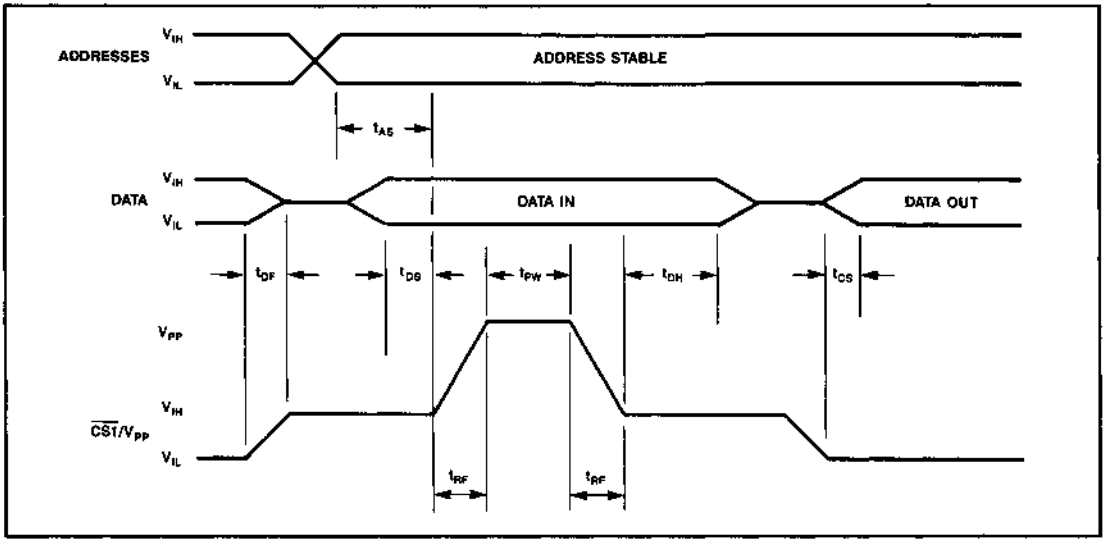
NOTE: 6 V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49B-35D	35	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-35J	35	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-35P	35	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C49B-35T	35	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-45DI	45	24 Pin CERDIP, 0.6"	D1	Industrial	Standard
WS57C49B-45DMB	45	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49B-45J	45	28 Pin PLDCC	J3	Comm'l	Standard
WS57C49B-45P	45	24 Pin Plastic DIP, 0.6"	P2	Comm'l	Standard
WS57C49B-45S	45	24 Pin Plastic DIP, 0.3"	S1	Comm'l	Standard
WS57C49B-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-45TI	45	24 Pin CERDIP, 0.3"	T1	Industrial	Standard
WS57C49B-45TMB	45	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49B-55CMB	55	28 Pad CLLCC	C1	Military	STD-MIL-883C
WS57C49B-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49B-55FMB	55	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C49B-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C
WS57C49B-70CMB	70	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C49B-70DMB	70	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C49B-70T	70	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C49B-70TMB	70	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

HIGH SPEED 8K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 25 ns
- **Low Power Consumption**
- **Fast Programming**
- **DESC SMD 5962-87515**
- **Pin Compatible with AM27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C49C is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C49C over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C49C is 100% tested with worst case test patterns both before and after assembly.

A unique feature of the WS57C49C is a designed-in output hold from address change. This allows the WS57C49C to be run at a cycle time equal to the address access time. While addresses are changing, output data is held long enough to be latched into external circuitry.

The WS57C49C is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

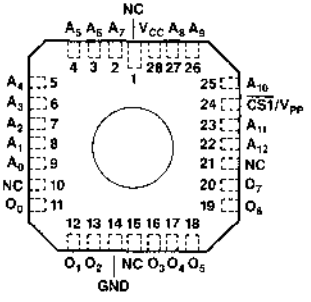
MODE SELECTION

PINS / MODE	$\overline{CS1}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	V_{CC}	High Z
Program	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{CC}	D_{OUT}

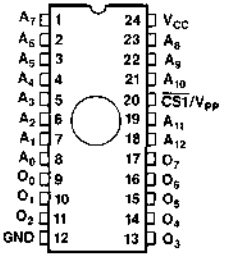
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP/Plastic DIP/ Flatpack



PRODUCT SELECTION GUIDE

PARAMETER	WS57C49C-25	WS57C49C-30
Address Access Time (Max)	25 ns	30 ns
Output Enable Time (Max)	15 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
ESD Protection ..... > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

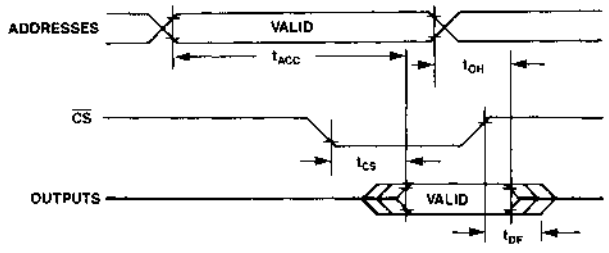
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		35	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C49C-25		WS57C49C-30		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		25		30	ns
$\overline{CS}$ to Output Delay	t_{CS}		15		20	
Output Disable to Output Float	t_{DF}		20		25	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM

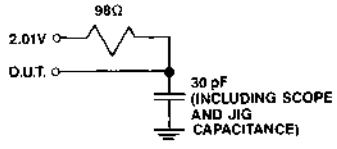


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4 This parameter is only sampled and is not 100% tested
5 Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

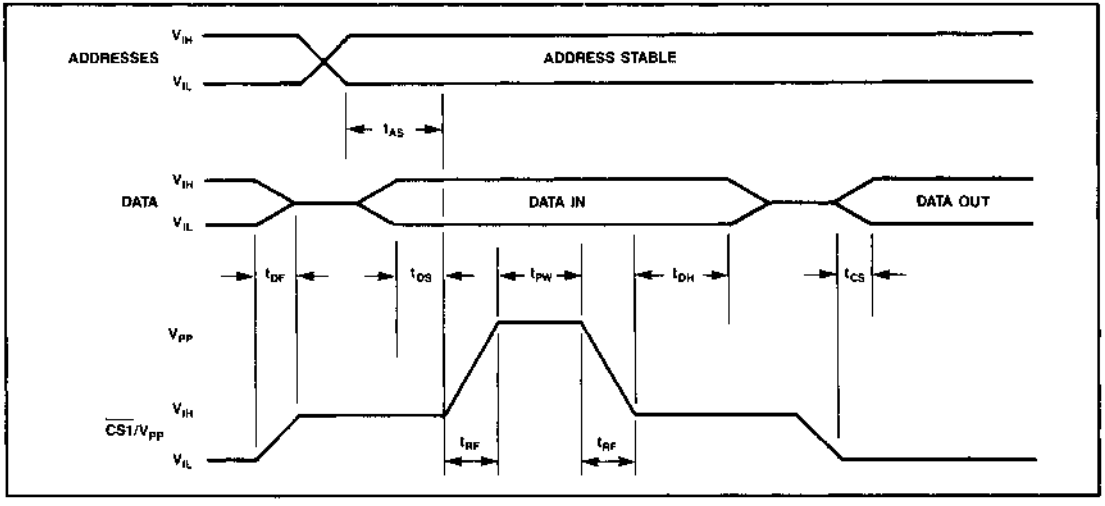
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

NOTE: 6. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

PROGRAMMING WAVEFORM



WAFERSCALE INTEGRATION, INC.

HIGH SPEED 16K × 8 CMOS PROM/RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 40 ns
- **Low Power Consumption**
- **Fast Programming**
- **Pin Compatible with AM27S51**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C51B is a High Performance 128K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

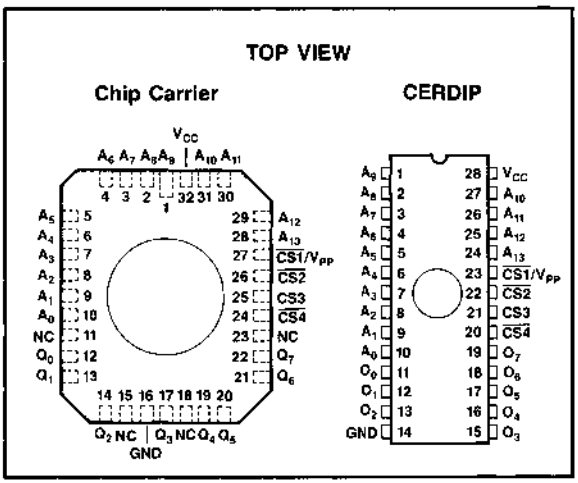
A further advantage of the WS57C51B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C51B is 100% tested with worst case test patterns both before and after assembly.

The WS57C51B provides a low power alternative to those designs which are committed to a bipolar PROM footprint. It is a direct drop-in replacement for a bipolar PROM of the same architecture (16K × 8). No software, hardware or layout changes need be performed.

MODE SELECTION

PINS / MODE	$\overline{CS1}$/V_{PP}	$\overline{CS2}$	CS3	$\overline{CS4}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	X	V_{CC}	High Z
Output Disable	X	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	X	V_{IL}	X	V_{CC}	High Z
Output Disable	X	X	X	V_{IH}	V_{CC}	High Z
Program	V_{PP}	X	X	X	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C51B-40	WS57C51B-45	WS57C51B-55	WS57C51B-70
Address Access Time (Max)	40 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	20 ns	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

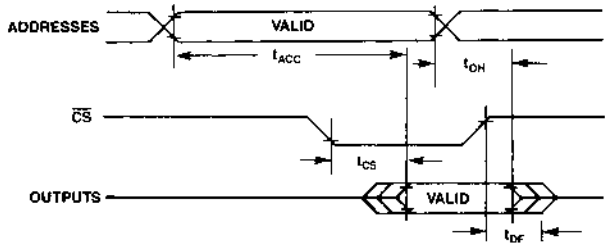
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX		UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4		V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4			
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	Note 3	mA
			Military		35		
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	Note 3	
			Military		40		
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10		µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10		

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C51B-40		WS57C51B-45		WS57C51B-55		WS57C51B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		40		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		25		30	
Output Disable to Output Float	t_{DF}		20		20		25		25	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM

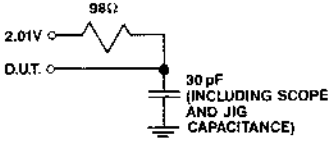


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

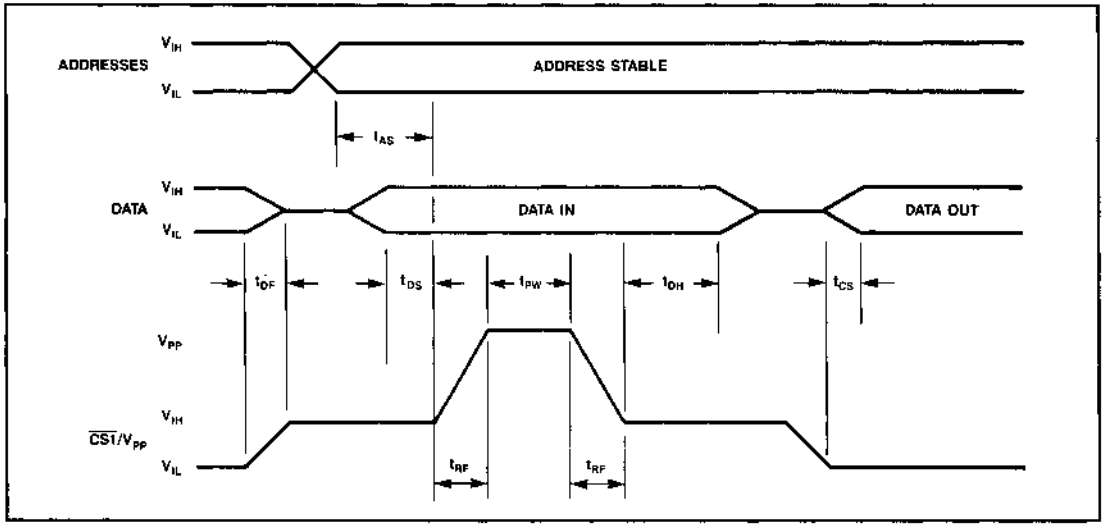
NOTE: 6. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width (Note 7)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 7. A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C51B-40D	40	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51B-40L	40	32 Pin CLDCC	L3	Comm'l	Standard
WS57C51B-40T	40	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51B-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51B-45DMB	45	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C51B-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C51B-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51B-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51B-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51B-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C51B-55LMB	55	32 Pin CLDCC	L3	Military	MIL-STD-883C
WS57C51B-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C51B-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS57C51B-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51B-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C51B-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C51B-70LMB	70	32 Pin CLDCC	L3	Military	MIL-STD-883C
WS57C51B-70T	70	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard

HIGH SPEED 32K × 8 CMOS RPROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 40 ns
- **Low Power Consumption**
- **Fast Programming**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

2

GENERAL DESCRIPTION

The WS57C71C is an extremely High-Performance 256K UV erasable electrically Re-Programmable Read Only Memory (RPROM). It is manufactured in an advanced CMOS technology and utilizes WSI's patented self-aligned split gate EPROM cell (see WSI Technical Brief 001).

The WS57C71C was developed for High-Performance Embedded Control applications. Its very high speed enables it to run at full speed with embedded processors such as the TMS320XX, 80960, M56/96000, etc.

The industry standard RPROM pin configuration of the WS57C71C provides an easy upgrade path from a 16K × 8 device as well as providing an upgrade path to 64K × 8 and 128K × 8 devices.

The WS57C71C utilizes WSI's patented split gate EPROM cell. This technology enables WSI to manufacture high density low power CMOS EPROMs that operate at the high speed of bipolar PROMs.

For further information on WSI products, contact the nearest WSI sales office, sales representative, or call WSI at 800-TEAM-WSI (832-6974).

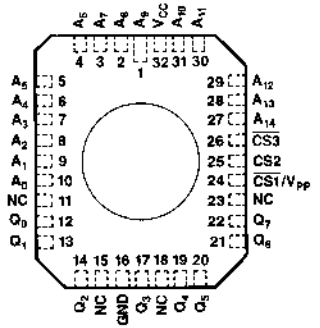
MODE SELECTION

MODE \ PINS	$\overline{CS1}$/V_{PP}	CS2	$\overline{CS3}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	V_{IH}	X	X	V_{CC}	High Z
Output Disable	X	V_{IL}	X	V_{CC}	High Z
Output Disable	X	X	V_{IH}	V_{CC}	High Z
Program	V_{PP}	X	V_{IH}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IH}	V_{IL}	V_{CC}	D_{OUT}
Program Inhibit	V_{PP}	X	V_{IL}	V_{CC}	High Z

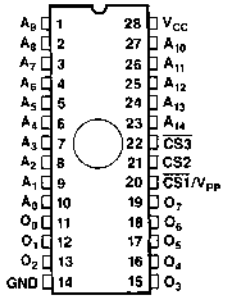
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C71C-40	WS57C71C-45	WS57C71C-55
Address Access Time (Max)	40 ns	45 ns	55 ns
Output Enable Time (Max)	20 ns	20 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	−40°C to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

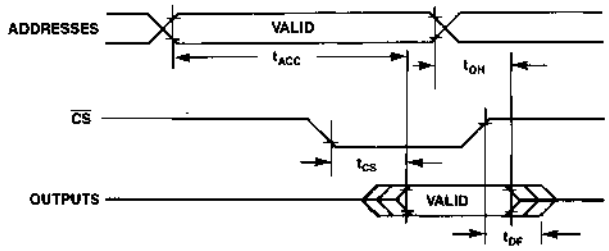
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX		UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4		V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4			
V_{IL}	Input Low Voltage				0.8		V
V_{IH}	Input High Voltage			2.0			
I_{CC}	V_{CC} Active Current	Note 3	Comm'l		30	Note 3	mA
			Military		40		
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10		µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10		

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 2 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	57C71C-40		57C71C-45		57C71C-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		40		45		55	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		20	
Output Disable to Output Float	t_{DF}		20		20		20	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM

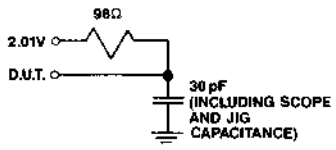


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

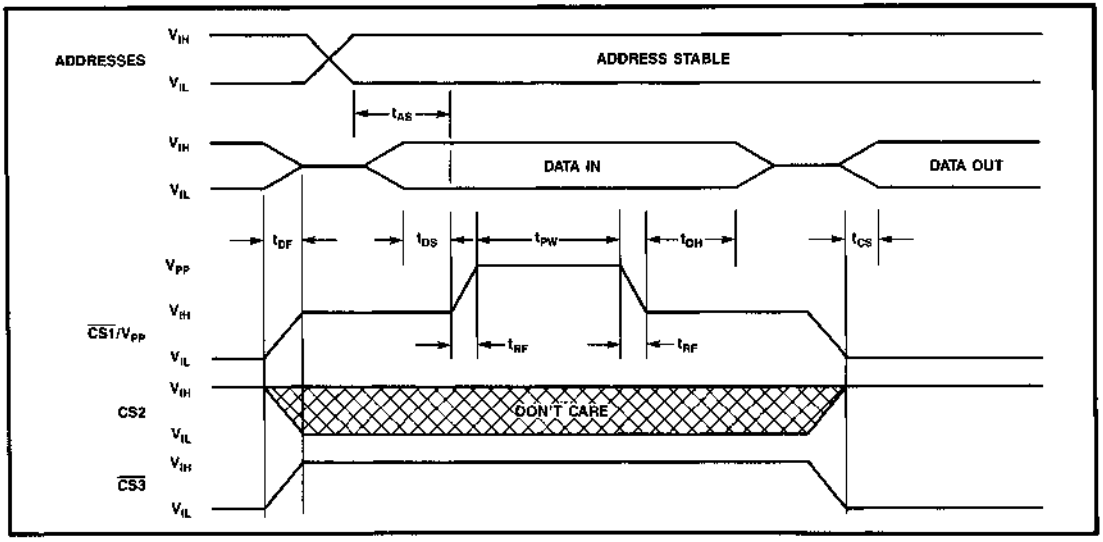
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	i_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

NOTE: 6. V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup Time	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C71C-40D*	40	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-40L*	40	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-40T*	40	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-45D	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-45L	45	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-45T	45	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-55CM	55	32 Pad CLLCC	C2	Military	Standard
WS57C71C-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C71C-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C71C-55DM	55	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS57C71C-55DMB	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C71C-55L	55	32 Pin CLDCC	L3	Comm'l	Standard
WS57C71C-55LM	55	32 Pin CLDCC	L3	Military	Standard
WS57C71C-55LMB	55	32 Pin CLDCC	L3	Military	MIL-STD-883C
WS57C71C-55T	55	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS57C71C-55TM	55	28 Pin CERDIP, 0.3"	T2	Military	Standard
WS57C71C-55TMB	55	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C

*These products are Advance Information

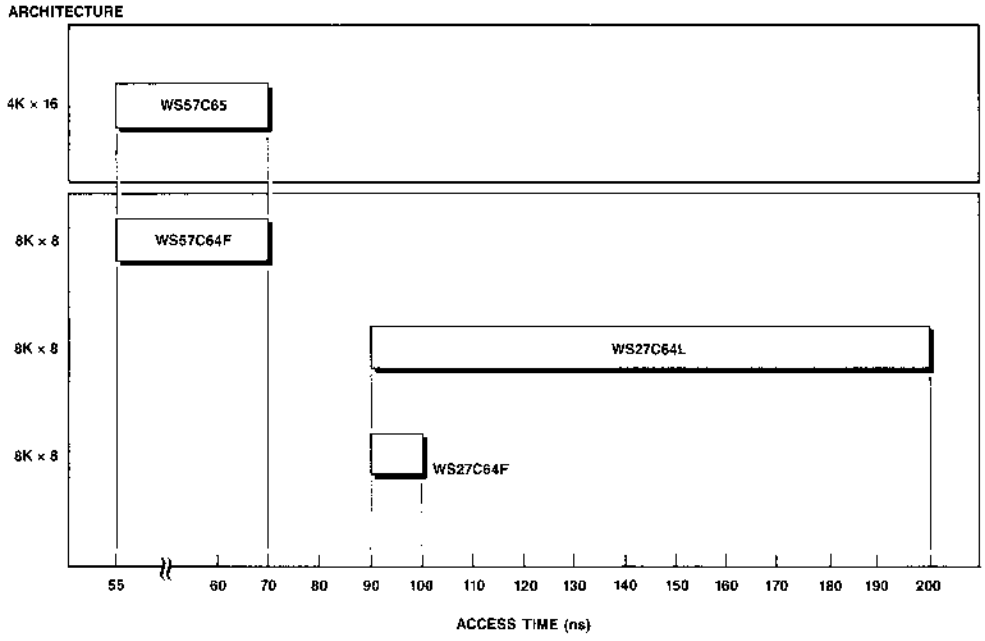
WAFERSCALE INTEGRATION, INC.

SECTION INDEX

EPROM MEMORY PRODUCTS

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 800-562-6363.

64K EPROM SELECTION GUIDE



WAFERSCALE INTEGRATION, INC.

MILITARY 8K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 90 ns (Military)
- **Low Power Consumption**
- **DESC SMD No. 85102**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Industrial/Military Temperature Operating Range**

3

GENERAL DESCRIPTION

The WS27C64F is a HIGH PERFORMANCE 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full Industrial and Military temperature operating range.

The WS27C64F is a direct drop-in replacement for the industry standard 27C64 and/or 2764 EPROMs. It was developed specifically for this purpose and requires no board or software modifications to complete the change.

The WS27C64F is configured in the standard EPROM pinout which provides an easy upgrade path to the WS27C128F and WS27C256F.

MODE SELECTION

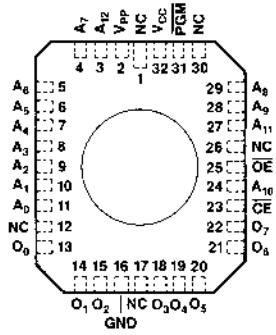
PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE A8H

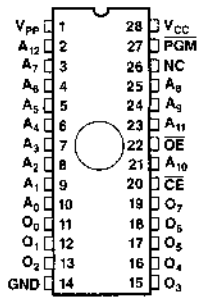
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP



PRODUCT SELECTION GUIDE

PARAMETER	WS27C64F-90	WS27C64F-10
Address Access Time (Max)	90 ns	100 ns
Chip Select Time (Max)	90 ns	100 ns
Output Enable Time (Max)	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65° to +150°C
Voltage on Any Pin with
Respect to GND ..... −0.6V to +7V
V_{PP} with respect to GND ..... −0.6V to +14V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

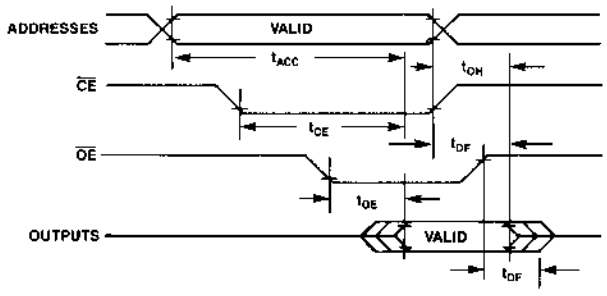
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	Note 1		200	µA
I_{SB2}	V_{CC} Standby Current (TTL)	Note 2		10	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3		25	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd	−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$. $V_{IH} \geq 2.0V$
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS27C64F-90		WS27C64F-10		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		90		100	ns
$\overline{CE}$ to Output Delay	t_{CE}		90		100	
$\overline{OE}$ to Output Delay	t_{OE}		30		30	
Output Disable to Output Float	t_{DF}		30		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



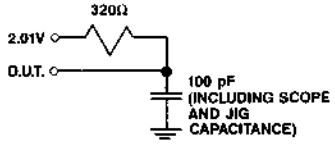
3

CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: .45 and 2.4V
Reference Levels: .8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 4 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −1 mA)	V_{OH}	2.4		V

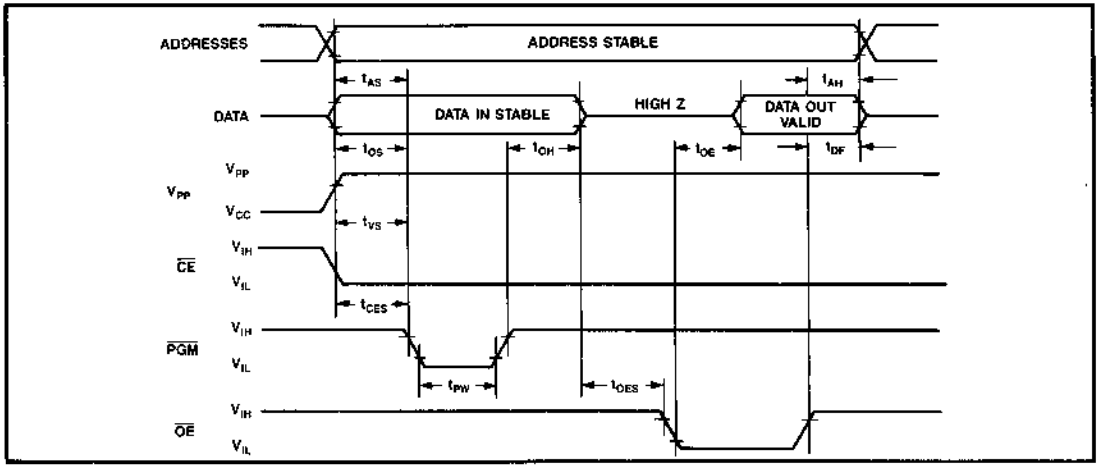
NOTES: 6. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
8. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1	3	10	ms

NOTE: Single pulse programming algorithms should use one 10 ms PGM pulse per byte.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C64F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C64F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C64F-10CMB	100	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C64F-10DMB	100	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

8K × 8 CMOS EPROM

KEY FEATURES

- **High Performance CMOS**
  - 90 ns Access Time
- **Fast Programming**
- **Drop-In Replacement for 27C64 or 2764**
- **300 Mil Dip or Standard 600 Mil Dip**
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000V
- **Standard JEDEC EPROM Pinout**
- **DESC SMD No. 85102**

3

GENERAL DESCRIPTION

The WS27C64L is a HIGH PERFORMANCE 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in WSI's latest CMOS EPROM technology which enables it to operate at speeds as fast as 90 ns access time over the full operating range.

The WS27C64L can directly replace any 8K × 8 EPROM which conforms to the JEDEC standard. Examples of this would be as follows: 2764 or 27C64. It can be easily programmed using standard EPROM programmers or the MagicPro™ IBM PC compatible engineering programmer offered by WSI.

The WS27C64L is also available in a 300 mil Dip. The pin configuration remains the same as the 600 mil wide package and the programming algorithms are unchanged. This allows for a simple PCB layout change to take advantage of a 50% reduction in required board space.

The WS27C64L provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 90-ns access time provides no-wait-state operation with high-performance CPUs such as the 16-MHz 80186, 16-MHz 68020, or 12-MHz 80386. The WS27C64L offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The WS27C64L is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The WS27C64L is one member of a high-density EPROM Family which ranges in density from 64K to 4 Megabit.

PRODUCT SELECTION GUIDE

PARAMETER	27C64L-90	27C64L-12	27C64L-15	27C64L-20
Address Access Time (Max)	90 ns	120 ns	150 ns	200 ns
Chip Select Time (Max)	90 ns	120 ns	150 ns	200 ns
Output Enable Time (Max)	30 ns	35 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Commercial	0°C to +70°C	+5V	±5% or ±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

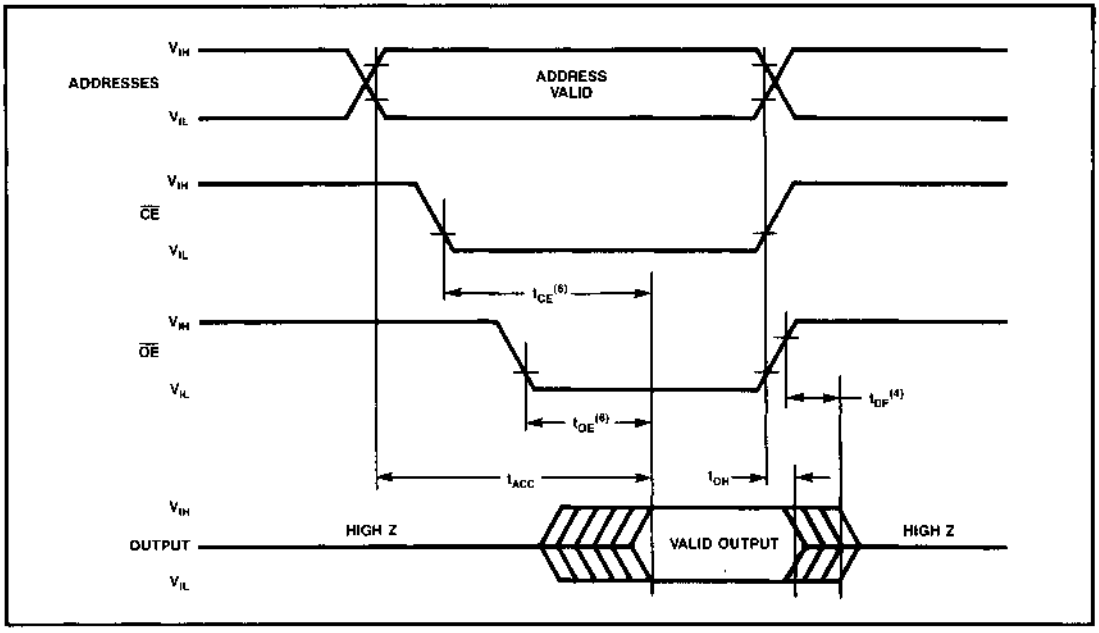
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}[3]	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}[1]	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	F = 5 MHz		40	mA
			F = 8 MHz		50	
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	27C64L-90		27C64L-12		27C64L-15		27C64L-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		30		35		40		40	
t_{DF}[2]	Output Disable to Output Float		30		35		40		40	
t_{OH}[2]	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ± 0.3V.

A.C. WAVEFORMS



CAPACITANCE[4] T_A = 25°C, f = 1 MHz

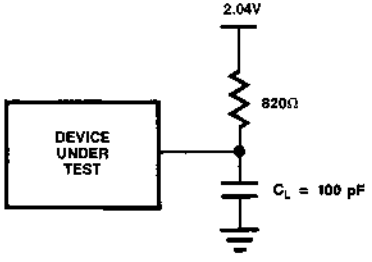
SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

MODE SELECTION

The modes of operation of the WS27C64L are listed in Table 1. A single 5V power supply is required in the read mode.

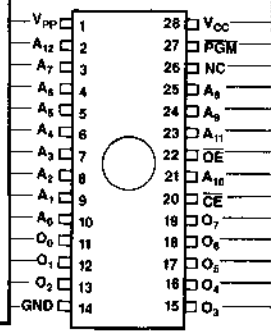
Table 1. Modes Selection

MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	5.0V	5.0V	D_{OUT}
Output Disable	X	X	V_{IH}	5.0V	5.0V	High Z
Standby	X	V_{IH}	X	5.0V	5.0V	High Z
Programming	V_{IL}	V_{IL}	V_{IH}	V_{PP}	5.8V	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{IL}	V_{PP}	5.8V	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	5.0V	High Z

NOTES:
7. X can be V_{IL} or V_{IH}.

DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	27C010L	27C256L
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_8
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



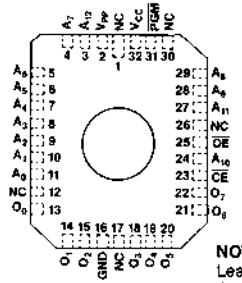
27C256L	27C010L	2 Mbit	4 Mbit	8 Mbit
	V_{CC} XX/$\overline{PGM}$	V_{CC} XX/$\overline{PGM}$	V_{CC} A_{18}	V_{CC} A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE: 8. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C64L pins.

PIN NAMES

A_0–A_{12}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

LCC PIN CONFIGURATION



TOP

NOTE: Leadless or Leaded, Plastic or Ceramic Package

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.8V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

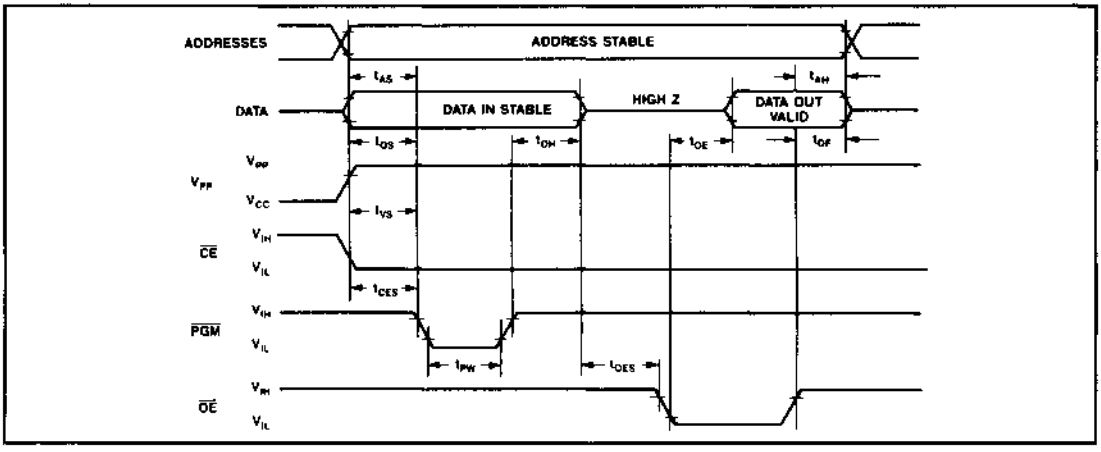
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$, $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current, See I_{CC2}	I_{CC}		40	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES:
9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$, $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.8V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING RANGE		WSI MANUFACTURING PROCEDURE
				TEMPERATURE	V_{CC}	
WS27C64L-90D/5	90	28 Pin CERDIP, 0.6″	D2	Comm'l	±5%	Standard
WS27C64L-12D	120	28 Pin CERDIP, 0.6″	D2	Comm'l	±10%	Standard
WS27C64L-12DI	120	28 Pin CERDIP, 0.6″	D2	Industrial	±10%	Standard
WS27C64L-12DMB	120	28 Pin CERDIP, 0.6″	D2	Military	±10%	MIL-STD-883C
WS27C64L-12J	120	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C64L-12P	120	28 Pin Plastic DIP, 0.6″	P3	Comm'l	±10%	Standard
WS27C64L-12T	120	28 Pin CERDIP, 0.3″	T2	Comm'l	±10%	Standard
WS27C64L-15D	150	28 Pin CERDIP, 0.6″	D2	Comm'l	±10%	Standard
WS27C64L-15DMB	150	28 Pin CERDIP, 0.6″	D2	Military	±10%	MIL-STD-883C
WS27C64L-15J	150	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C64L-20D	200	28 Pin CERDIP, 0.6″	D2	Comm'l	±10%	Standard
WS27C64L-20DMB	200	28 Pin CERDIP, 0.6″	D2	Military	±10%	MIL-STD-883C
WS27C64L-20J	200	32 Pin PLDCC	J4	Comm'l	±10%	Standard

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 8K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **Low Power Consumption**
- **DESC SMD No. 85102**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**

3

GENERAL DESCRIPTION

The WS57C64F is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming very little power.

Two major features of the WS57C64F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited. Examples of these applications are modems, secure telephones, servo controllers, and industrial controllers.

The WS57C64F is configured in the standard EPROM pinout which provides an easy upgrade path to higher density EPROMs.

MODE SELECTION

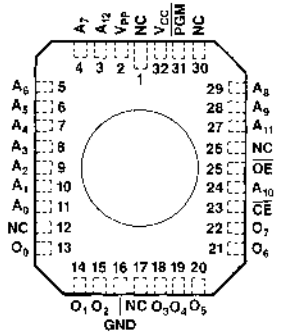
MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	5.0V	5.0V	D_{OUT}
Output Disable	X	X	V_{IH}	5.0V	5.0V	High Z
Standby	X	V_{IH}	X	5.0V	5.0V	High Z
Programming	V_{IL}	V_{IL}	V_{IH}	V_{PP}	5.8V	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{IL}	V_{PP}	5.8V	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	5.0V	High Z

X can be V_{IL} or V_{IH}.

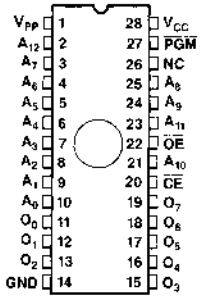
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C64F-55	WS57C64F-70
Address Access Time (Max)	55ns	70ns
Chip Select Time (Max)	55ns	70ns
Output Enable Time (Max)	20ns	25ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

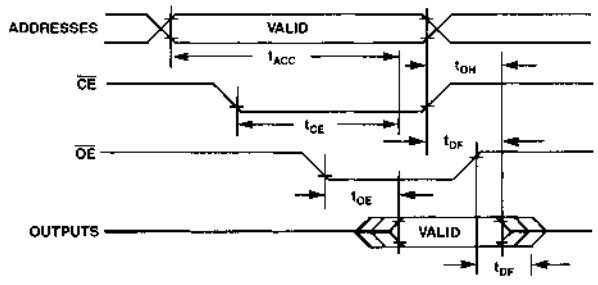
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	CE = V_{CC} ± 0.3V (Notes 1 & 3)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	CE = V_{IH} (Notes 2 & 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 4	Comm'l		20	mA
			Military		30	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 4	Comm'l		25	mA
			Military		35	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS57C64F-55		WS57C64F-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		20		25	
Output Disable to Output Float	t_{DF}		20		25	
Address to Output Hold	t_{OH}	10		10		

AC READ TIMING DIAGRAM



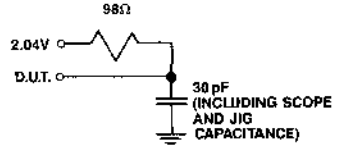
3

CAPACITANCE[5] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

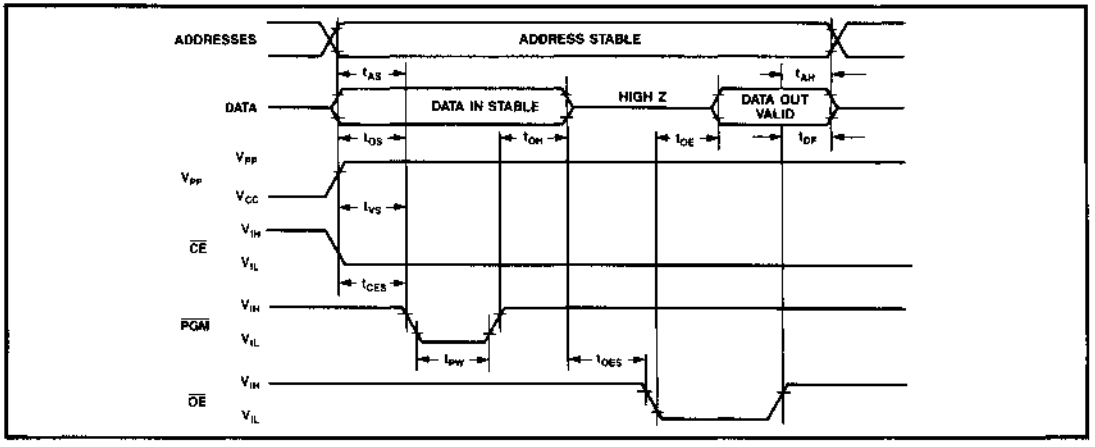
NOTES: 7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
9. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1	3	10	ms

NOTE: For simple, one pulse only, programming algorithms, use a 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C64F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C64F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C64F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C64F-70DI	70	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C64F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C64F-70J	70	32 Pin PLDCC	J4	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 4K x 16 WORDWIDE CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **Low Power Consumption**
- **Ideal for 16/32 Bit Processors**
  — TMS320, 68000, 80386, etc.
- **2 to 1 Package Reduction**
- **30%+ Space Savings**
- **Single Chip Solution**
- **Compatible with JEDEC pinout**

3

GENERAL DESCRIPTION

The WS57C65 is a High Performance EPROM memory with a 4K x 16 architecture. It is manufactured in an advanced CMOS process which consumes very little power while operating at speeds which rival that of bipolar PROMs.

The major features of the WS57C65 are its 4K x 16 architecture and its high speed. This combination makes the WS57C65 an ideal solution for applications which utilize 16/32 bit data paths. Examples include systems which are based on such processors as the TMS320 family of DSP processors as well as high performance general purpose processors such as the MC68000 family and the 80286 and 80386 microprocessors.

The word wide architecture of the WS57C65 results in a 2 to 1 savings in EPROM component count and a minimum 30% savings in board space.

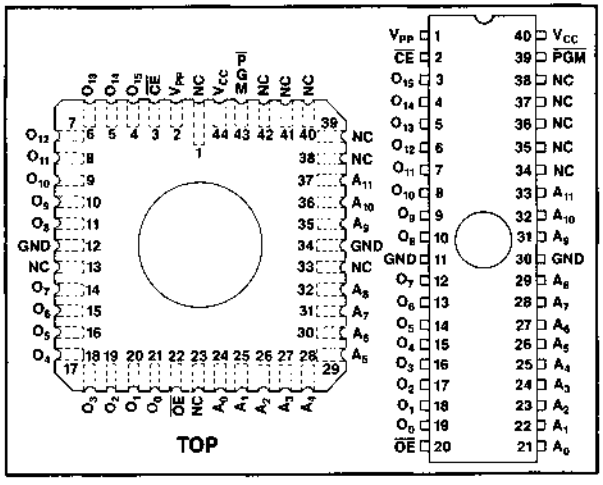
The pin configuration utilized is upward compatible with the JEDEC standard pinout for word wide EPROMs. This allows an easy upgrade path to higher density memories such as the WS57C257. No board changes or jumper wires are required to complete the upgrade.

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 0023H, A_0 = V_{IH} = DEVICE 00B1H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C65-55	WS57C65-70
Address Access Time	55 ns	70 ns
Chip Select Time	55 ns	70 ns
Output Enable Time	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

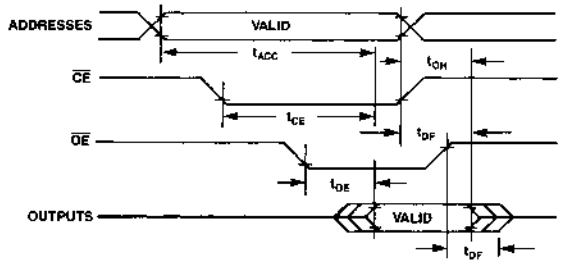
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	Notes 1 and 3			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	Notes 2 and 3			20	mA
I_{CC1}	Active Current (CMOS)	Notes 1 and 4	Comm'l		35	mA
			Military		45	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 4	Comm'l		45	mA
			Military		55	
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 3 mA/MHz for A.C. power component

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C65-55		WS57C65-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		25		30	
Output Disable to Output Float	t_{DF}		25		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



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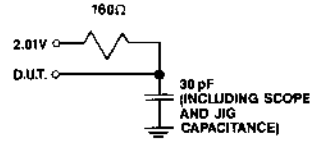
CAPACITANCE[5] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		50	mA
V_{CC} Supply Current (Note 4)	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 8 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −2 mA)	V_{OH}	2.4		V

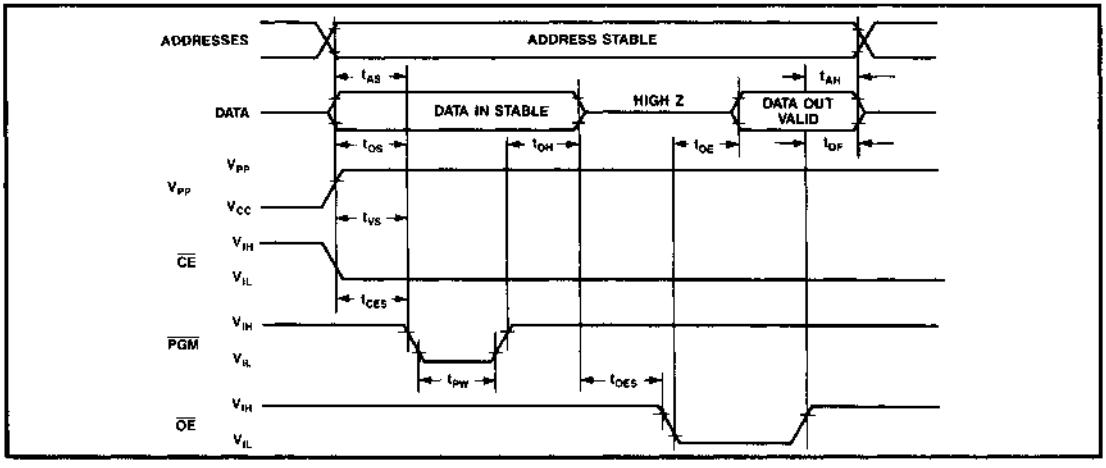
NOTES: 7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa
9. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1	3	10	ms

NOTE: Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



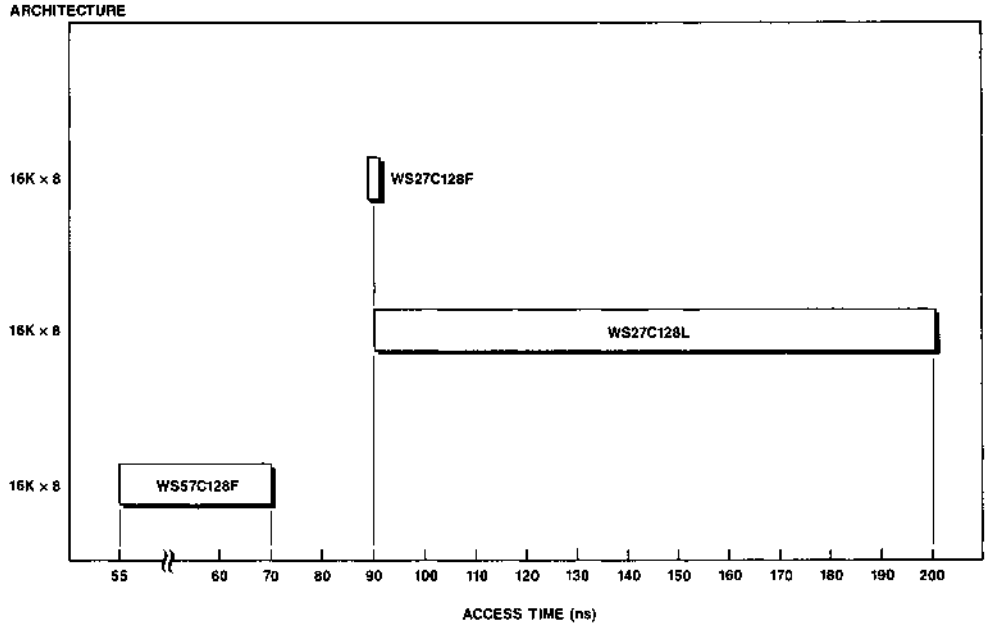
PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C65-55C	55	44 Pad CLLCC	C3	Comm'l	Standard
WS57C65-55D	55	40 Pin CERDIP, 0.6"	D3	Comm'l	Standard
WS57C65-70D	70	40 Pin CERDIP, 0.6"	D3	Comm'l	Standard

128K EPROM SELECTION GUIDE



WAFERSCALE INTEGRATION, INC.

MILITARY 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 90 ns (Military)
- **Low Power Consumption**
- **DESC SMD No. 5962-87661**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Industrial/Military Operating Range**

3

GENERAL DESCRIPTION

The WS27C128F is an extremely HIGH PERFORMANCE 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at high speeds and very low power over the full industrial and military temperature operating range.

The WS27C128F was specifically designed to replace standard EPROMs in industrial and military environments. No hardware or software changes are required to replace standard military 27128 EPROMs with the WSI WS27C128F.

The WS27C128F is configured in the standard EPROM pinout which provides an easy upgrade path for the WS27C64F and the 256K bit WS27C256F.

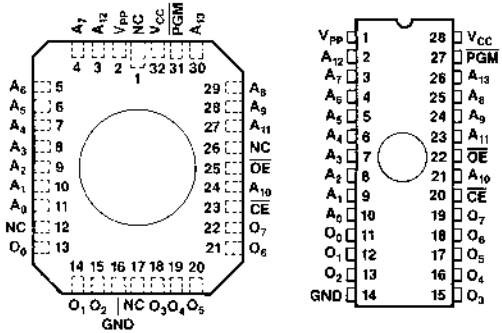
MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE A8H.

PIN CONFIGURATION

TOP VIEW



PRODUCT SELECTION GUIDE

PARAMETER	WS27C128F-90
Address Access Time (Max)	90 ns
Chip Select Time (Max)	90 ns
Output Enable Time (Max)	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	Note 1		200	µA
I_{SB2}	V_{CC} Standby Current (TTL)	Note 2		10	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3		25	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3		35	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd	−10	10	µA

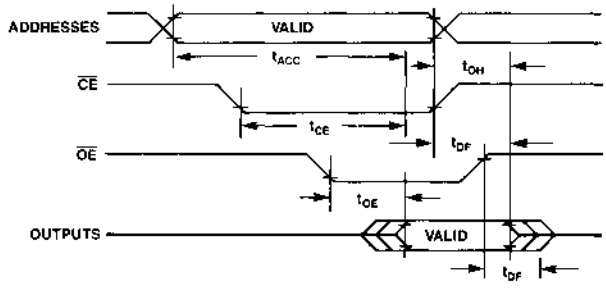
NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS27C128F-90		UNITS
		MIN	MAX	
Address to Output Delay	t_{ACC}		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		90	
$\overline{OE}$ to Output Delay	t_{OE}		30	
Output Disable to Output Float	t_{DF}		30	
Address to Output Hold	t_{OH}	0		

NOTE: Single shot programming algorithms should use one 10 ms PGM pulse per word.

AC READ TIMING DIAGRAM



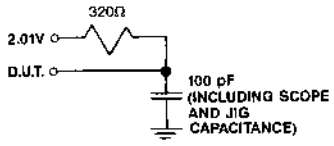
3

CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: .45 and 2.4V
Reference Levels: .8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		30	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 4 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −1 mA)	V_{OH}	2.4		V

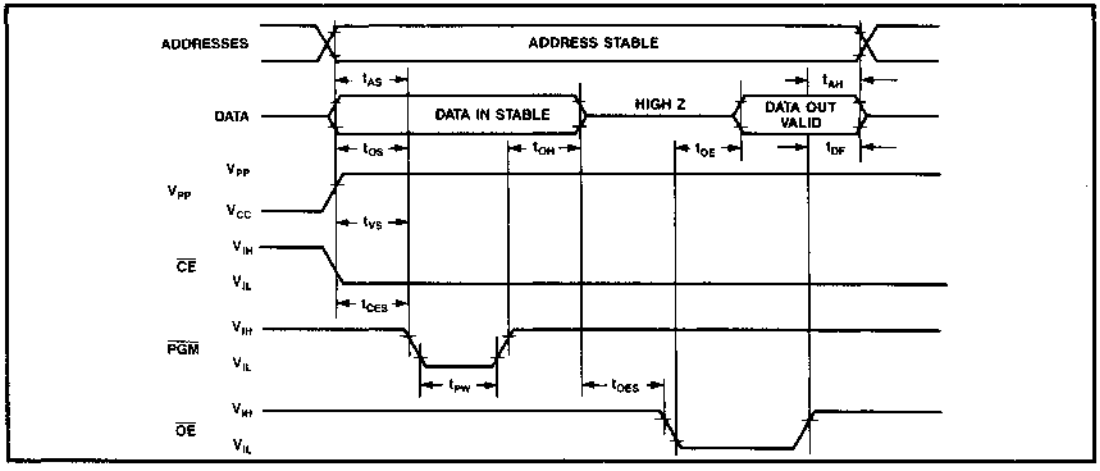
NOTES: 6. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
8. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width (Note 9)	t_{PW}	1	5		ms

NOTE: 9. For single pulse programming algorithms, use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C128F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C128F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

16K x 8 CMOS EPROM

KEY FEATURES

- **High Performance CMOS**
  - 90 ns Access Time
- **Fast Programming**
- **Drop-In Replacement for 27C128 or 27128**
- **DESC SMD No. 5962-87661**
- **300 Mil Dip or Standard 600 Mil Dip**
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000V
- **Standard JEDEC EPROM Pinout**

3

GENERAL DESCRIPTION

The WS27C128L is a HIGH PERFORMANCE 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in WSI's latest CMOS EPROM technology which enables it to operate at speeds as fast as 90 ns access time over the full operating range. (If faster speeds are required, contact your WSI sales representative.)

The WS27C128L can directly replace any 16K x 8 EPROM which conforms to the JEDEC standard. Examples of this would be as follows: 27128 or 27C128. It can be easily programmed using standard EPROM programmers or the MagicPro™ IBM PC compatible engineering programmer offered by WSI.

The WS27C128L is also available in a 300 mil Dip. The pin configuration remains the same as the 600 mil wide package and the programming algorithms are unchanged. This allows for a simple PCB layout change to take advantage of a 50% reduction in required board space.

The WS27C128L provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 90-ns access time provides no-wait-state operation with high-performance CPUs such as the 16-MHz 80186, 16-MHz 68020, or 12-MHz 80386. The WS27C128L offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The WS27C128L is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The WS27C128L is one member of a high density EPROM Family which ranges in density from 64K to 4 Megabit.

PRODUCT SELECTION GUIDE

PARAMETER	27C128L-90	27C128L-12	27C128L-15	27C128L-20
Address Access Time (Max)	90 ns	120 ns	150 ns	200 ns
Chip Select Time (Max)	90 ns	120 ns	150 ns	200 ns
Output Enable Time (Max)	30 ns	35 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +150°C
Voltages on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7V
ESD Protection ..... > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Commercial	0°C to +70°C	+5V	±5% or ±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

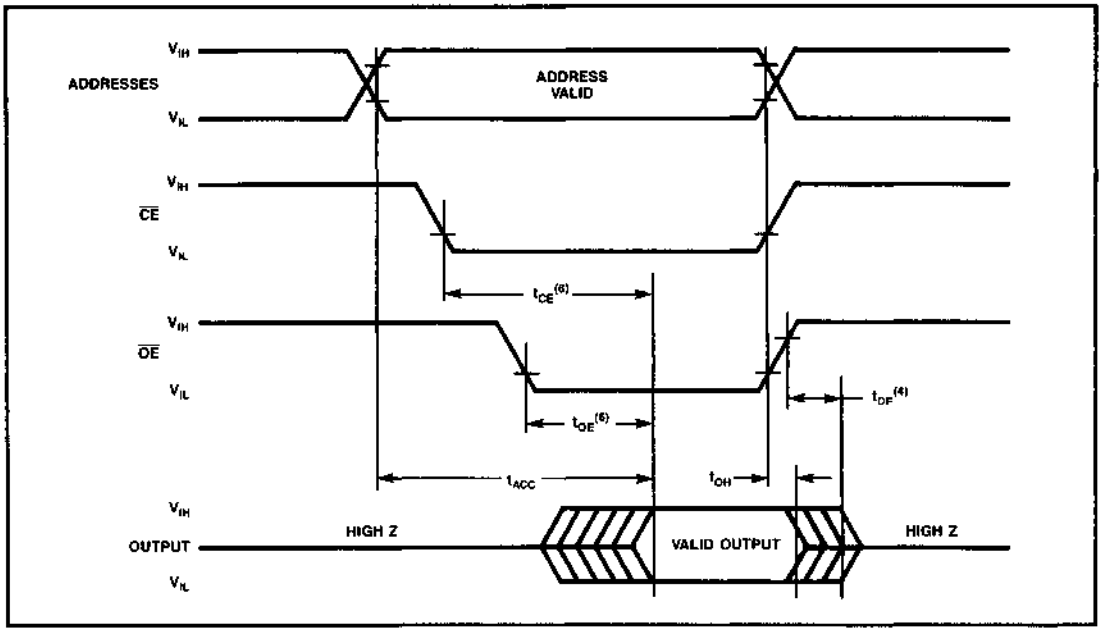
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}(3)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}(1)	V_{CC} Active Current	CE = OE = V_{IL}	F = 5 MHz		40	mA
			F = 8 MHz		50	
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	27C128L-90		27C128L-12		27C128L-15		27C128L-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		30		35		40		40	
t_{DF}(2)	Output Disable to Output Float		30		35		40		40	
t_{OH}(2)	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ± 0.3V.

A.C. WAVEFORMS

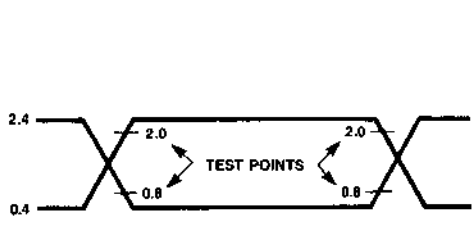


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

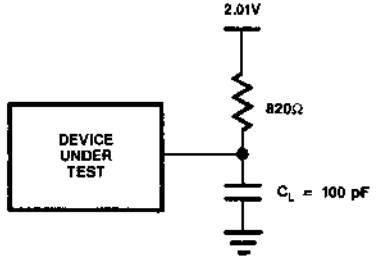
NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to t_{CE}–t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

MODE SELECTION

The modes of operation of the WS27C128L are listed in Table 1. A single 5V power supply is required in the read mode.

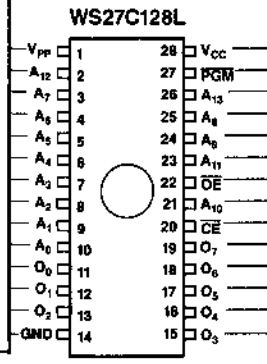
Table 1. Modes Selection

MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	5.0V	5.0V	D_{OUT}
Output Disable	X	X	V_{IH}	5.0V	5.0V	High Z
Standby	X	V_{IH}	X	5.0V	5.0V	High Z
Programming	V_{IL}	V_{IL}	V_{IH}	V_{PP}	5.8V	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{IL}	V_{PP}	5.8V	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	5.0V	High Z

NOTES:
7. X can be V_{IL} or V_{IH}.

DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	27C010L	27C512L
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	A_{15}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



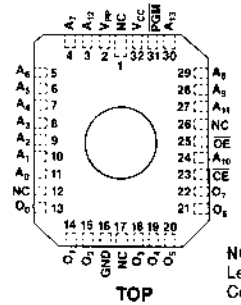
27C512L	27C010L	2 Mbit	4 Mbit	8 Mbit
	V_{CC} XX/$\overline{PGM}$	V_{CC} XX/$\overline{PGM}$	V_{CC} A_{16}	V_{CC} A_{16}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE: 8. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C128L pins.

PIN NAMES

A_0–A_{13}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

LCC PIN CONFIGURATION



TOP

NOTE: Leadless or Leaded, Plastic or Ceramic Package

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.8V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

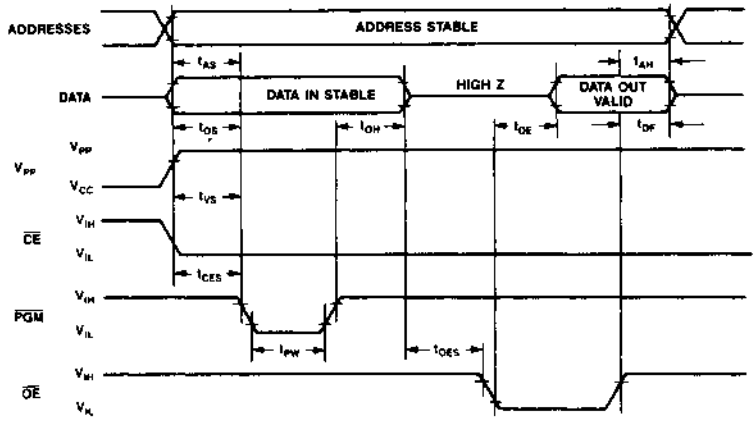
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$, $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		40	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES:
9. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
10. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$, $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
11. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.8V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING RANGE		WSI MANUFACTURING PROCEDURE
				TEMPERATURE	V_{CC}	
WS27C128L-90D/5	90	28 Pin CERDIP, 0.6"	D2	Comm'l	±5%	Standard
WS27C128L-12D	120	28 Pin CERDIP, 0.6"	D2	Comm'l	±10%	Standard
WS27C128L-12DI	120	28 Pin CERDIP, 0.6"	D2	Industrial	±10%	Standard
WS27C128L-12DMB	120	28 Pin CERDIP, 0.6"	D2	Military	±10%	MIL-STD-883C
WS27C128L-12J	120	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C128L-12P	120	28 Pin Plastic DIP, 0.6"	P3	Comm'l	±10%	Standard
WS27C128L-12T	120	28 Pin CERDIP, 0.3"	T2	Comm'l	±10%	Standard
WS27C128L-12TI	120	28 Pin CERDIP, 0.3"	T2	Industrial	±10%	Standard
WS27C128L-12TMB	120	28 Pin CERDIP, 0.3"	T2	Military	±10%	MIL-STD-883C
WS27C128L-15D	150	28 Pin CERDIP, 0.6"	D2	Comm'l	±10%	Standard
WS27C128L-15DMB	150	28 Pin CERDIP, 0.6"	D2	Military	±10%	MIL-STD-883C
WS27C128L-15TMB	150	28 Pin CERDIP, 0.3"	T2	Military	±10%	MIL-STD-883C
WS27C128L-20DMB	200	28 Pin CERDIP, 0.6"	D2	Military	±10%	MIL-STD-883C
WS27C128L-20TMB	200	28 Pin CERDIP, 0.3"	T2	Military	±10%	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-87661**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**

3

GENERAL DESCRIPTION

The WS57C128F is an extremely HIGH PERFORMANCE 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming only 60mA.

Two major features of the WS57C128F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited. Examples of these applications are modems, secure telephones, servo controllers, and industrial controllers.

The WS57C128F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

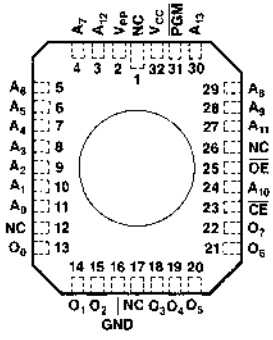
MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	X	V_{IL}	V_{IL}	5.0V	5.0V	D_{OUT}
Output Disable	X	X	V_{IH}	5.0V	5.0V	High Z
Standby	X	V_{IH}	X	5.0V	5.0V	High Z
Programming	V_{IL}	V_{IL}	V_{IH}	V_{PP}	5.8V	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{IL}	V_{PP}	5.8V	D_{OUT}
Program Inhibit	X	V_{IH}	X	V_{PP}	5.0V	High Z

X can be V_{IL} or V_{IH}.

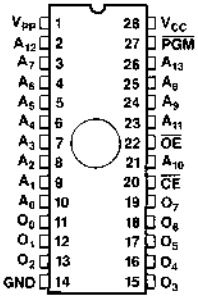
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C128F-55	WS57C128F-70
Address Access Time (Max)	55ns	70ns
Chip Select Time (Max)	55ns	70ns
Output Enable Time (Max)	25ns	25ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65° to +150°C
Voltage on Any Pin with
Respect to GND ..... −0.6V to +7V
V_{PP} with Respect to GND ..... −0.6V to +14V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

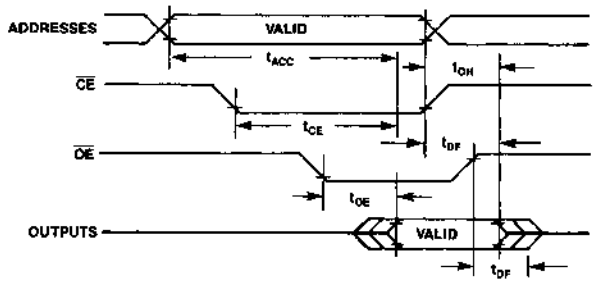
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	Notes 1 and 3			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	Notes 2 and 3			20	mA
I_{CC1}	Active Current (CMOS)	Notes 1 and 4	Comm'l		25	mA
			Military		30	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 4	Comm'l		35	mA
			Military		40	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS57C128F-55		WS57C128F-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		25		25	
Output Disable to Output Float	t_{DF}		25	0	25	
Address to Output Hold	t_{OH}	10		10		

AC READ TIMING DIAGRAM

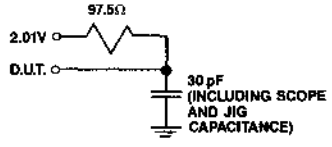


CAPACITANCE[5] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		30	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

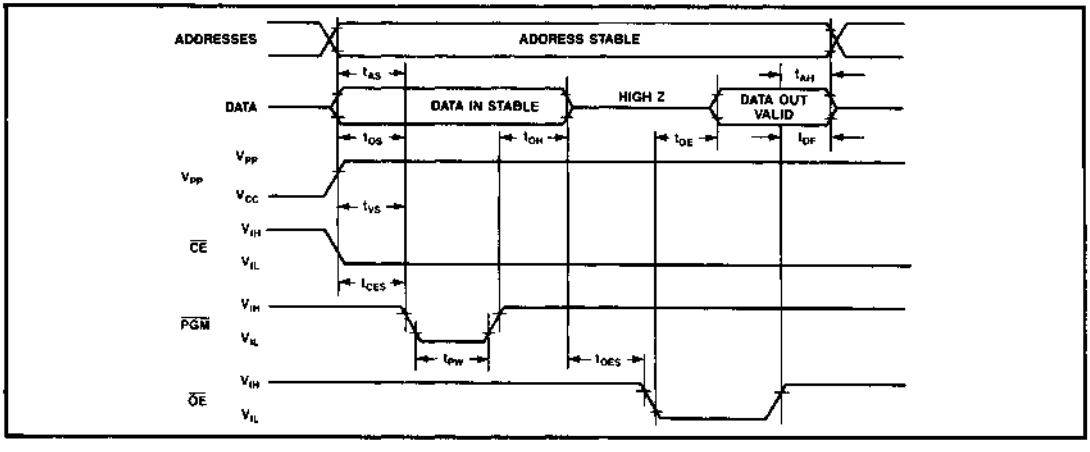
NOTES: 7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
9. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1	3	10	ms

NOTE: Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



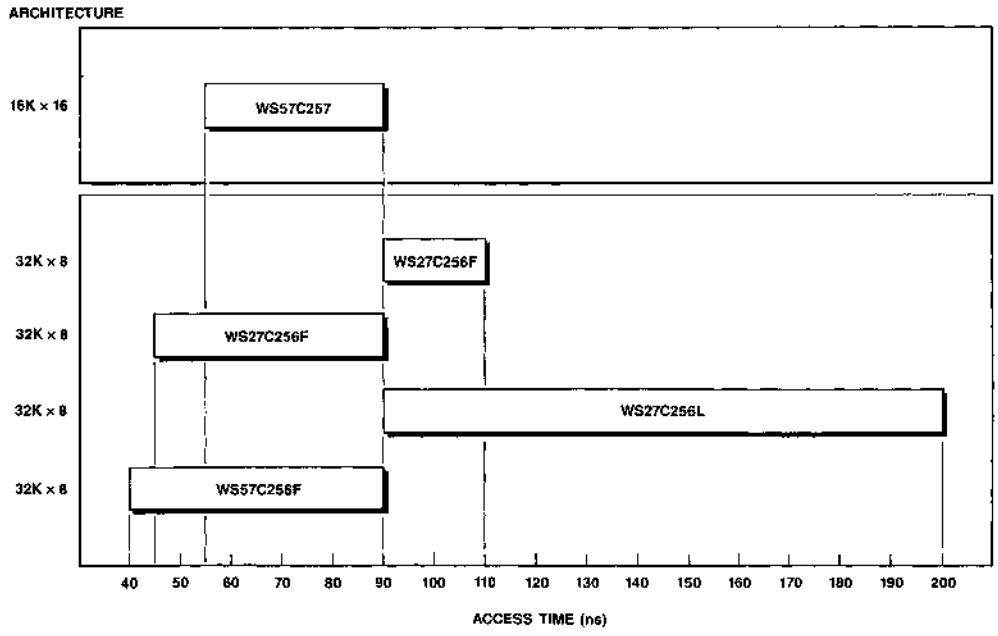
PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C128F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128F-70CI	70	32 Pad CLLCC	C2	Industrial	Standard
WS57C128F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C128F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128F-70DI	70	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C128F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

256K EPROM SELECTION GUIDE



HIGH SPEED 32K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — 45 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-86063**
- **EPI Processing**
  - — Latch-Up Immunity Up to 200 mA
  - — ESD Protection Exceeds 2000V
- **Standard EPROM Pinout**

GENERAL DESCRIPTION

The WS27C256F is a 32K x 8 CMOS EPROM which has been speed-enhanced to 45 ns. It is based upon WaferScale's patented CMOS Split Gate EPROM technology.

The 45 ns access time of the WS27C256F is a key parameter. Traditionally, as memory densities increase, memory access times become slower. This forces microprocessors to insert Wait States which negatively impact system throughput. Real Time applications cannot afford Wait States regardless of memory density. WSI's unique memories can keep pace with the fastest microprocessors. The combination of speed and density available in the WS27C256F enables the use of more complex and comprehensive algorithms in real time applications.

WSI's patented CMOS Split-Gate EPROM technology not only enables the development of fast and dense memory products, it also provides a higher level of Quality and Reliability. Tests have proven that WSI EPROM products program very efficiently and quickly. Also, the WSI EPROM retains its data an order of magnitude better than traditional EPROM technologies. This combination of speed, density, quality and reliability make WSI the obvious choice when selecting a non-volatile memory supplier.

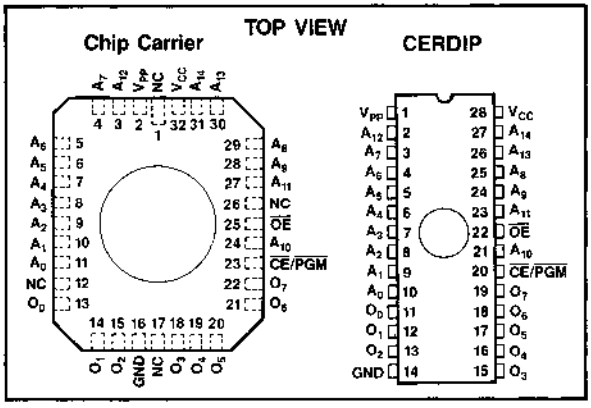
The WS27C256F is configured in the JEDEC standard EPROM pin configuration. It is also easily programmed on popular EPROM programmers as well as the MagicPro™ IBM PC compatible engineering programmer offered by WSI.

MODE SELECTION

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE E0H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C256F-45	WS27C256F-55	WS27C256F-70	WS27C256F-90
Address Access Time (Max)	45 ns	55 ns	70 ns	90 ns
Chip Select Time (Max)	45 ns	55 ns	70 ns	90 ns
Output Enable Time (Max)	25 ns	25 ns	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65° to +150°C
Voltage on Any Pin with
Respect to GND ..... −0.6V to +7V
V_{PP} with respect to GND ..... −0.6V to +13V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0°C to +70°C	+5V ± 5%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

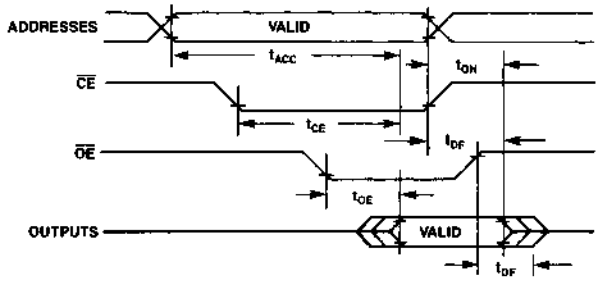
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} ± 0.3V (Note 1)		500	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = V_{IH} (Note 2)		5	mA
I_{CC1}	V_{CC} Active Current[3]	Commercial		30	mA
		Military		40	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd	−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	27C256F-45		27C256F-55		27C256F-70		27C256F-90		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		45		55		70		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		45		55		70		90	
$\overline{OE}$ to Output Delay	t_{OE}		25		25		30		30	
Output Disable to Output Float	t_{DF}		25		25		30		30	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM

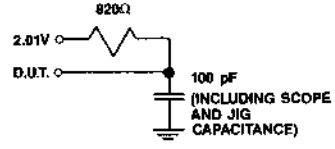


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0.45 and 2.4V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

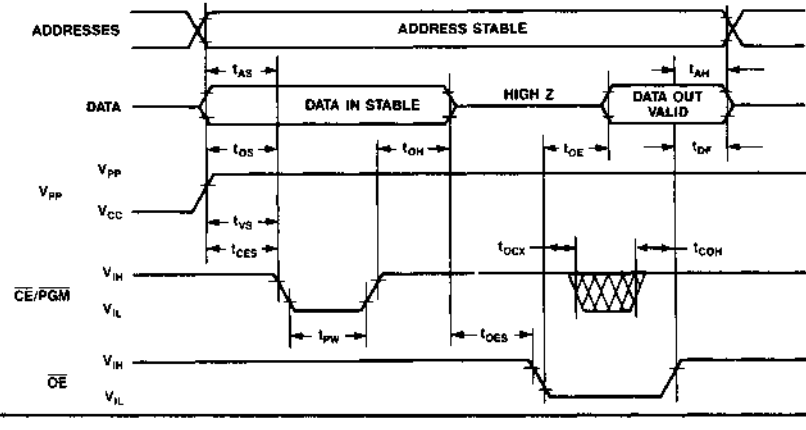
NOTES: 6. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
8. During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1	3	10	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

NOTE: These values are for standard programming — actual programming algorithm may use different limitations.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C256F-45D*	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C256F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256F-90LMB	90	32 Pin CLDCC	L3	Military	MIL-STD-883C

*This product is Advance Information.

WAFERSCALE INTEGRATION, INC.

32K × 8 CMOS EPROM

KEY FEATURES

- **High Performance CMOS**
  — 90 ns Access Time
- **Fast Programming**
- **Drop-In Replacement for 27C256 or 27256**
- **DESC SMD No. 5962-86063**
- **300 Mil Dip or Standard 600 Mil Dip**
- **EPI Processing**
  — Latch-Up Immunity to 200 mA
  — ESD Protection Exceeds 2000V
- **Standard JEDEC EPROM Pinout**

3

GENERAL DESCRIPTION

The WS27C256L is a HIGH PERFORMANCE 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in WSI's latest CMOS EPROM technology which enables it to operate at speeds as fast as 90 ns access time over the full operating range. (If faster speeds are required, contact your WSI sales representative.)

The WS27C256L can directly replace any 32K × 8 EPROM which conforms to the JEDEC standard. Examples of this would be as follows: 27256, 27C256, or 27C256F. It can be easily programmed using standard EPROM programmers or the MagicPro™ IBM PC compatible engineering programmer offered by WSI.

The WS27C256L is also available in a 300 mil Dip. The pin configuration remains the same as the 600 mil wide package and the programming algorithms are unchanged. This allows for a simple PCB layout change to take advantage of a 50% reduction in required board space. An upgrade path to a 512K product (WS27C512L) is provided.

The WS27C256L provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 90-ns access time provides no-wait-state operation with high-performance CPUs such as the 16-MHz 80186, 16-MHz 68020, or 12-MHz 80386. The WS27C256L offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The WS27C256L is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The WS27C256L is one member of a high-density EPROM Family which ranges in density from 64K to 4 Megabit.

PRODUCT SELECTION GUIDE

PARAMETER	27C256L-90	27C256L-12	27C256L-15	27C256L-20
Address Access Time (Max)	90 ns	120 ns	150 ns	200 ns
Chip Select Time (Max)	90 ns	120 ns	150 ns	200 ns
Output Enable Time (Max)	30 ns	35 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Commercial	0°C to +70°C	+5V	±5% or ±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

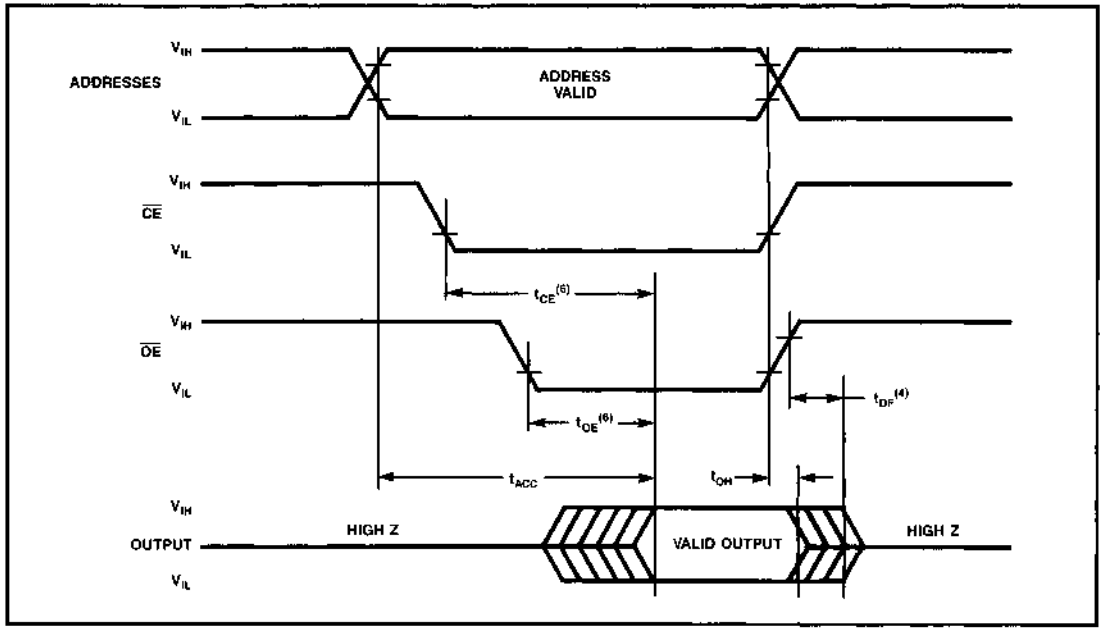
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}(3)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}(1)	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	F = 5 MHz		40	mA
			F = 8 MHz		50	
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	27C256L-90		27C256L-12		27C256L-15		27C256L-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		30		35		40		40	
t_{DF}(2)	Output Disable to Output Float		30		35		40		40	
t_{OH}(2)	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ± 0.3V.

A.C. WAVEFORMS



CAPACITANCE(4) T_A = 25°C, f = 1 MHz

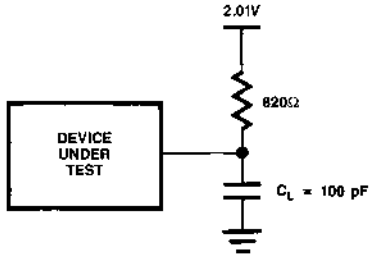
SYMBOL	PARAMETER	CONDITIONS	TYP(5)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages
6. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0". Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

MODE SELECTION

The modes of operation of the WS27C256L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

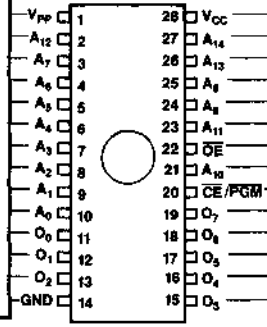
Table 1. Modes Selection

MODE \ PINS		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X	X	V_{CC}	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby		V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming		V_{IL}	V_{IH}	X	X	V_{PP}[8]	5.8V	D_{IN}
Program Verify		X	V_{IL}	X	X	V_{PP}[8]	5.8V	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}[8]	5.0V	High Z
Signature	Manufacturer[9]	V_{IL}	V_{IL}	V_H[8]	V_{IL}	V_{CC}	5.0V	23 H
	Device[9]	V_{IL}	V_{IL}	V_H[8]	V_{IH}	V_{CC}	5.0V	C0 H

NOTES:
7. X can be V_{IL} or V_{IH}.
8. $V_H = V_{PP} = 12.75 \pm 0.25V$.
9. A_1–A_8, A_{10}–$A_{14} = V_{IL}$.

DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	27C010L	27C512L
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{18}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	A_{15}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



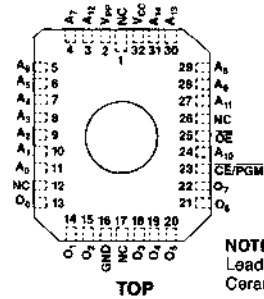
27C512L	27C010L	2 Mbit	4 Mbit	8 Mbit
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/$\overline{PGM}$	XX/$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE: 10. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C256L pins.

PIN NAMES

A_0–A_{14}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

LCC PIN CONFIGURATION



NOTE: Leadless or Leaded, Plastic or Ceramic Package

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.8V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

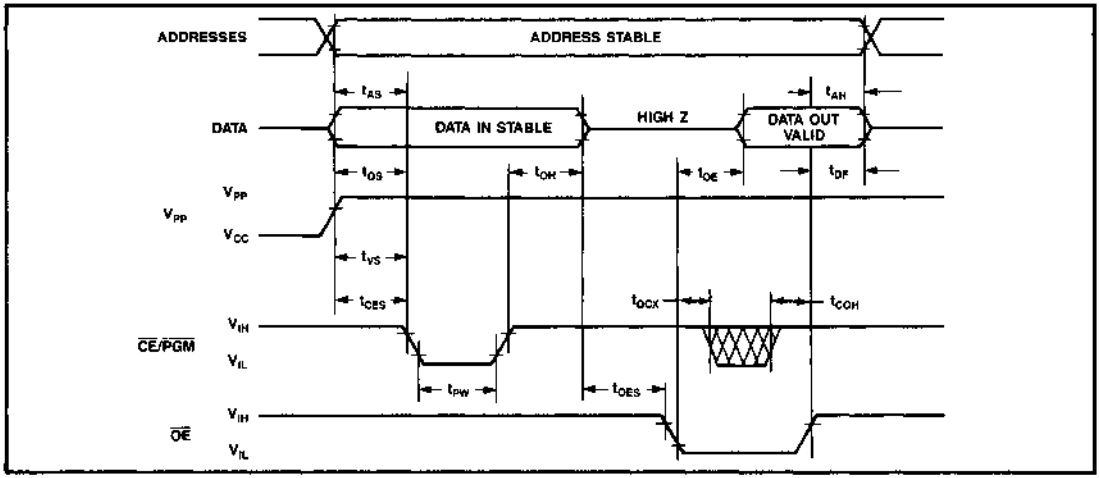
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		40	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES: 11. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
12. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
13. During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.8V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING RANGE		WSI MANUFACTURING PROCEDURE
				TEMPERATURE	V_{CC}	
WS27C256L-90D/5	90	28 Pin CERDIP, 0.6"	D2	Comm'l	±5%	Standard
WS27C256L-90T/5	90	28 Pin CERDIP, 0.3"	T2	Comm'l	±5%	Standard
WS27C256L-12CI	120	32 Pad CLLCC	C2	Industrial	±10%	Standard
WS27C256L-12CMB	120	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C256L-12D	120	28 Pin CERDIP, 0.6"	D2	Comm'l	±10%	Standard
WS27C256L-12DI	120	28 Pin CERDIP, 0.6"	D2	Industrial	±10%	Standard
WS27C256L-12DM	120	28 Pin CERDIP, 0.6"	D2	Military	±10%	Standard
WS27C256L-12DMB	120	28 Pin CERDIP, 0.6"	D2	Military	±10%	MIL-STD-883C
WS27C256L-12J	120	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C256L-12L	120	32 Pin CLDCC	L3	Comm'l	±10%	Standard
WS27C256L-12LMB	120	32 Pin CLDCC	L3	Military	±10%	MIL-STD-883C
WS27C256L-12P	120	28 Pin Plastic DIP, 0.6"	P3	Comm'l	±10%	Standard
WS27C256L-12T	120	28 Pin CERDIP, 0.3"	T2	Comm'l	±10%	Standard
WS27C256L-12TI	120	28 Pin CERDIP, 0.3"	T2	Industrial	±10%	Standard
WS27C256L-12TMB	120	28 Pin CERDIP, 0.3"	T2	Military	±10%	MIL-STD-883C
WS27C256L-15CI	150	32 Pad CLLCC	C2	Industrial	±10%	Standard
WS27C256L-15CMB	150	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C256L-15D	150	28 Pin CERDIP, 0.6"	D2	Comm'l	±10%	Standard
WS27C256L-15DMB	150	28 Pin CERDIP, 0.6"	D2	Military	±10%	MIL-STD-883C
WS27C256L-15J	150	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C256L-15L	150	32 Pin CLDCC	L3	Comm'l	±10%	Standard
WS27C256L-15LI	150	32 Pin CLDCC	L3	Industrial	±10%	Standard
WS27C256L-15LMB	150	32 Pin CLDCC	L3	Military	±10%	MIL-STD-883C
WS27C256L-15P	150	28 Pin Plastic Dip, 0.6"	P3	Comm'l	±10%	Standard
WS27C256L-20CMB	200	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C256L-20DMB	200	28 Pin CERDIP, 0.6"	D2	Military	±10%	MIL-STD-883C

HIGH SPEED 32K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 40 ns
- **Low Power Consumption**
- **DESC SMD No. 5962-86063**
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**

3

GENERAL DESCRIPTION

The WS57C256F is a HIGH PERFORMANCE 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at speeds as fast as 40 ns Access Time.

Two major features of the WS57C256F are its Low Power and High Speed. While operating in a TTL environment it consumes only 110 mA while cycling at full speed. Additionally, the WS57C256F can be placed in a standby mode which drops operating current below 15 mA in a TTL environment and 500 µA in a CMOS environment.

The WS57C256F also has exceptional output drive capability. It can source 4 mA and sink 16 mA per output.

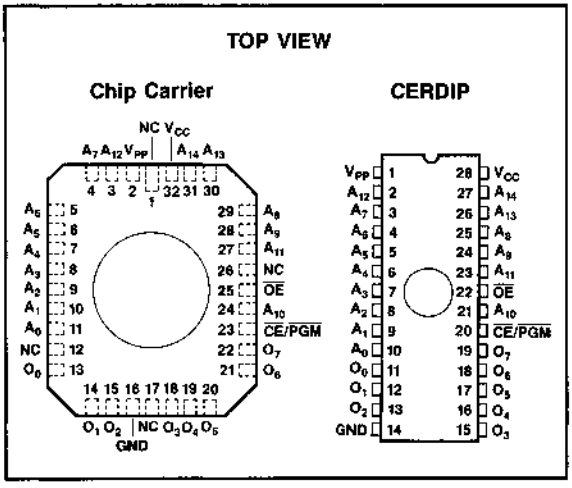
The WS57C256F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

MODE \ PINS	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	X	X	V_{CC}	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	X	X	V_{PP}[2]	5.8V	D_{IN}
Program Verify	X	V_{IL}	X	X	V_{PP}[2]	5.8V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	X	V_{PP}[2]	5.0V	High Z
Signature[3]	V_{IL}	V_{IL}	V_H[2]	V_{IL}	V_{CC}	5.0V	23 H[4]
	V_{IL}	V_{IL}	V_H[2]	V_{IH}	V_{CC}	5.0V	A8 H[5]

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $V_H = V_{PP} = 12.75 \pm 0.25V$.
3. A_1–A_8, A_{10}–$A_{14} = V_{IL}$.
4. Manufacturer
5. Device

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	57C256F-40	57C256F-45	57C256F-55	57C256F-70	57C256F-90
Address Access Time (Max)	40 ns	45 ns	55 ns	70 ns	90 ns
Chip Select Time (Max)	40 ns	45 ns	55 ns	70 ns	90 ns
Output Enable Time (Max)	20 ns	20 ns	25 ns	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

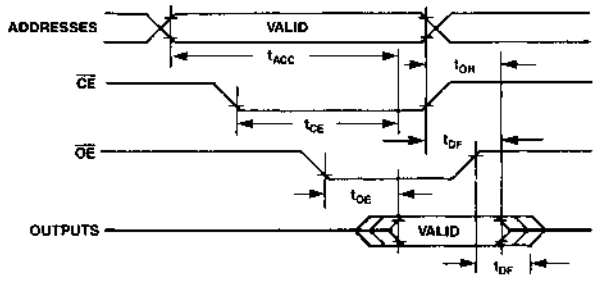
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} \pm 0.3V$ (Notes 1 and 3)			500	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = V_{IH}$ (Notes 2 and 3)			15	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 4	Comm'l		30	mA
			Military		40	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 4	Comm'l		35	mA
			Military		45	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1 mA/MHz for A.C. power component.
4. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	-40		-45		-55		-70		-90		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		40		45		55		70		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		40		45		55		70		90	
$\overline{OE}$ to Output Delay	t_{OE}		20		20		25		30		30	
Output Disable to Output Float	t_{DF}		20		20		25		30		30	
Address to Output Hold	t_{OH}	0		0		0		0		0		

AC READ TIMING DIAGRAM



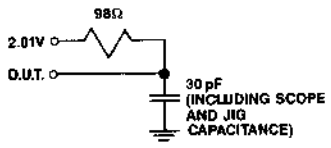
3

CAPACITANCE[5] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current (Note 4)	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

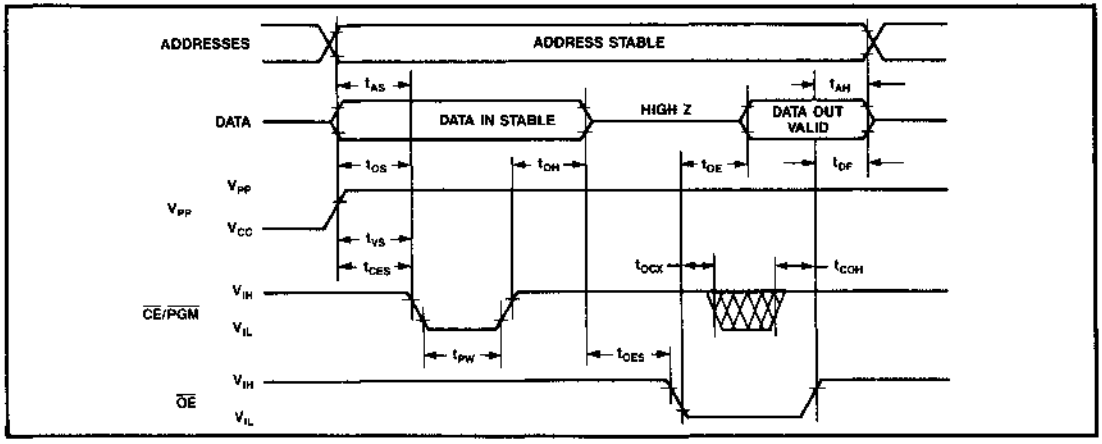
NOTES: 7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
9. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1	3	10	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

NOTE: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C256F-40D*	40	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-45D*	45	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-55CMB*	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-55DI*	55	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C256F-55DMB*	55	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C256F-55LI*	55	32 Pin CLDCC	L3	Industrial	Standard
WS57C256F-55LMB*	55	32 Pin CLDCC	L3	Military	MIL-STD-883C
WS57C256F-70CI	70	32 Pad CLLCC	C2	Industrial	Standard
WS57C256F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS57C256F-70LMB	70	32 Pin CLDCC	L3	Military	MIL-STD-883C
WS57C256F-90CI	90	32 Pad CLLCC	C2	Industrial	Standard
WS57C256F-90CM	90	32 Pad CLLCC	C2	Military	Standard
WS57C256F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-90D	90	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C256F-90DI	90	28 Pin CERDIP, 0.6"	D2	Industrial	Standard
WS57C256F-90DM	90	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS57C256F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

*These products are Advance Information.

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 16K x 16 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **Low Power Consumption**
- **Ideal for 16/32 Bit Processors**
  — TMS320, 68000, 80386, etc.
- **16-Bit Data Bus**
- **Simplifies Board Routing**
- **Single Chip Solution**
- **Compatible with JEDEC Pinout**

GENERAL DESCRIPTION

The WS57C257 is an extremely High Performance EPROM based memory with a 16K x 16 architecture. It is manufactured in an advanced CMOS process which consumes very little power while operating at speeds which rival that of bipolar PROMs.

The major features of the WS57C257 are its 16K x 16 architecture and its high speed. This combination makes the WS57C257 an ideal solution for applications which utilize 16/32 bit data paths. Examples include systems which are based on such processors as the TMS320 family of DSP processors as well as high performance general purpose processors such as the MC68000 family and the 80286 and 80386 microprocessors.

The wordwide architecture of the WS57C257 results in a 4 to 1 savings in EPROM component count and a minimum 60% savings in board space.

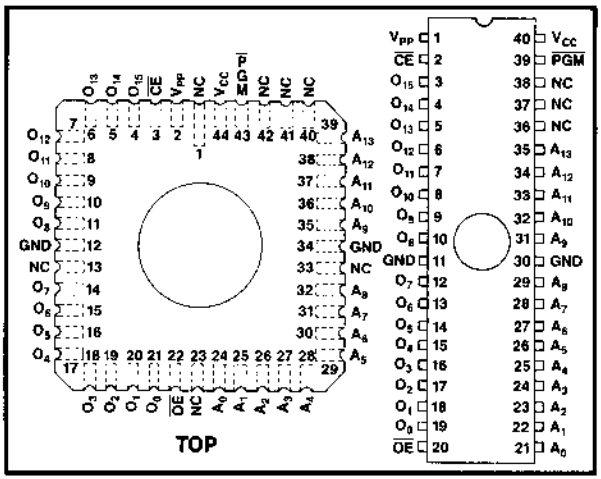
The pin configuration utilized is upward compatible with the JEDEC standard pinout for word wide EPROMs. This allows an easy upgrade path from lower density memories such as the WS57C65. No board changes or jumper wires are required to complete the upgrade.

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Encoded Data

X can be V_{IL} or V_{IH}.
*For signature, A_9 = 12V. A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 0023H. A_0 = V_{IH} = DEVICE 00B2H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C257-55	WS57C257-70	WS57C257-90
Address Access Time	55 ns	70 ns	90 ns
Chip Select Time	55 ns	70 ns	90 ns
Output Enable Time	25 ns	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55°C to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

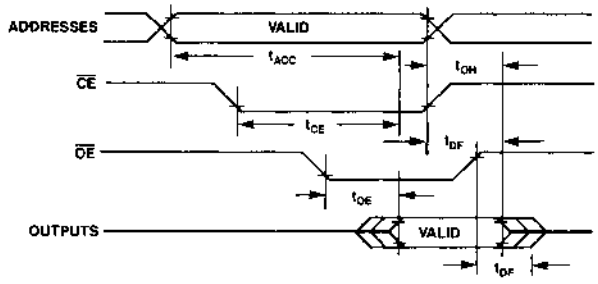
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	Notes 1 and 3			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	Notes 2 and 3			20	mA
I_{CC1}	Active Current (CMOS)	Notes 1 and 4	Comm'l		40	mA
			Military		50	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 4	Comm'l		50	mA
			Military		60	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs. $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$
3. Add 1 mA/MHz for A.C. power component.
4. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS57C257-55		WS57C257-70		WS57C257-90		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70		90	
$\overline{OE}$ to Output Delay	t_{OE}		25		30		30	
Output Disable to Output Float	t_{DF}		25		30		30	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM



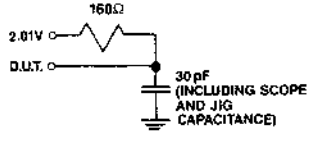
3

CAPACITANCE[5] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[6]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 5. This parameter is only sampled and is not 100% tested.
6. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

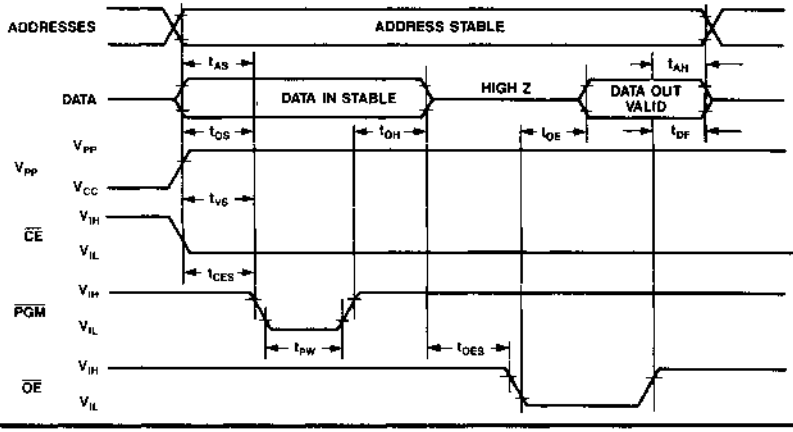
NOTES: 7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
9. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1	3	10	ms

NOTE: Single shot programming algorithms should use one 10 ms pulse per word.

PROGRAMMING WAVEFORM



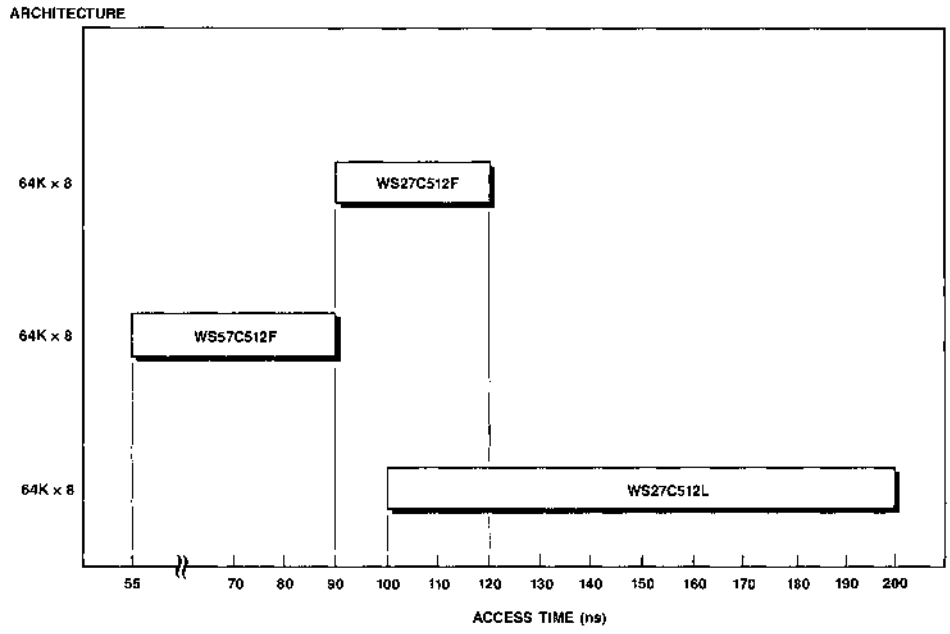
PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C257-55D	55	40 Pin CERDIP, 0.6"	D3	Comm'l	Standard
WS57C257-70CI	70	44 Pad CLLCC	C3	Industrial	Standard
WS57C257-70CMB	70	44 Pad CLLCC	C3	Military	MIL-STD-883C
WS57C257-70D	70	40 Pin CERDIP, 0.6"	D3	Comm'l	Standard
WS57C257-70DI	70	40 Pin CERDIP, 0.6"	D3	Industrial	Standard
WS57C257-70DMB	70	40 Pin CERDIP, 0.6"	D3	Military	MIL-STD-883C
WS57C257-70LMB	70	44 Pin CLDCC	L4	Military	MIL-STD-883C
WS57C257-90CMB	90	44 Pad CLLCC	C3	Military	MIL-STD-883C
WS57C257-90DI	90	40 Pin CERDIP, 0.6"	D3	Industrial	Standard
WS57C257-90DMB	90	40 Pin CERDIP, 0.6"	D3	Military	MIL-STD-883C

512K EPROM SELECTION GUIDE



WAFERSCALE INTEGRATION, INC.

HIGH SPEED 64K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 90 ns
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Low Power Consumption**
- **Standard EPROM Pinout**
- **Bipolar Speeds**

3

GENERAL DESCRIPTION

The WS27C512F is a High Performance 512K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at speeds as fast as 90 ns Access Time.

Two major features of the WS27C512F are its Low Power and High Speed. While operating in a TTL environment it consumes only 64 mA while cycling at full speed. Additionally, the WS27C512F can be placed in a standby mode which drops operating current below 2 mA in a TTL environment and 200 µA in a CMOS environment.

The WS27C512F also has exceptional output drive capability. It can source 1 mA and sink 4 mA per output.

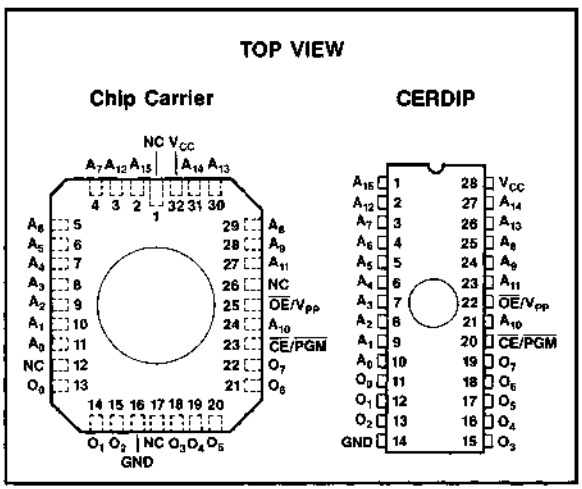
The WS27C512F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

PINS / MODE	$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	X	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{PP}[2]	X	X	5.8V	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	X	5.8V	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}[2]	X	X	5.0V	High Z
Signature[3]	V_{IL}	V_{IL}	V_H[2]	V_{IL}	5.0V	23 H[4]
	V_{IL}	V_{IL}	V_H[2]	V_{IH}	5.0V	AA H[5]

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $V_H = V_{PP} = 12.75 \pm 0.25V$.
3. A_1–A_8, A_{10}–$A_{15} = V_{IL}$.
4. Manufacturer
5. Device

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C512F-90	WS27C512F-12
Address Access Time (Max)	90 ns	120 ns
Chip Select Time (Max)	90 ns	120 ns
Output Enable Time (Max)	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +13V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

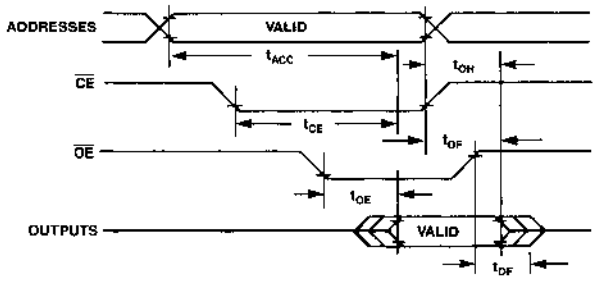
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	CE = V_{CC} ± 0.3V (Note 1)			200	µA
I_{SB2}	V_{CC} Standby Current (TTL)	CE = V_{IH} (Note 2)			2	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		40	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		35	mA
			Military		45	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS27C512F-90		WS27C512F-12		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		90		120	ns
$\overline{CE}$ to Output Delay	t_{CE}		90		120	
$\overline{OE}$ to Output Delay	t_{OE}		30		30	
Output Disable to Output Float	t_{DF}		30		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



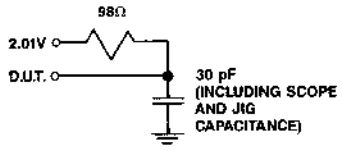
3

CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0.4 and 2.4V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

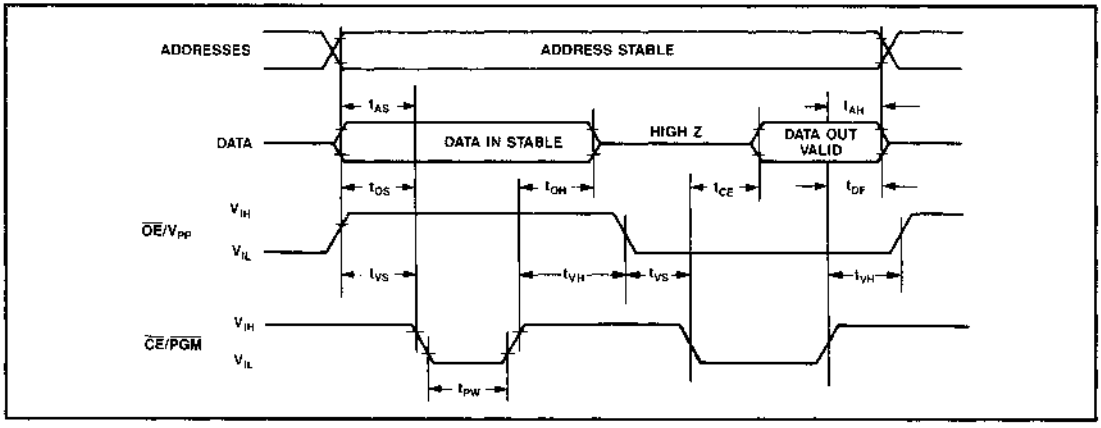
NOTES: 6. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
8. During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
V_{PP} Hold Time	t_{VH}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		70	ns
Data Valid From Chip Enable	t_{CE}			70	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1		10	ms

NOTES: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C512F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C512F-90D	90	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C512F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C512F-12CMB	120	32 Pad CLLCC	C2	Miltary	MIL-STD-883C
WS27C512F-12DMB	120	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

HIGH SPEED 64K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55 ns
- **EPI Processing**
  — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**
- **Low Power Consumption**

3

GENERAL DESCRIPTION

The WS57C512F is a HIGH PERFORMANCE 512K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which enables it to operate at speeds as fast as 55 ns Access Time.

Two major features of the WS57C512F are its Low Power and High Speed. While operating in a TTL environment it consumes only 90 mA while cycling at full speed. Additionally, the WS57C512F can be placed in a standby mode which drops operating current below 2 mA in a TTL environment and 500 µA in a CMOS environment.

The WS57C512F also has exceptional output drive capability. It can source 4 mA and sink 16 mA per output.

The WS57C512F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

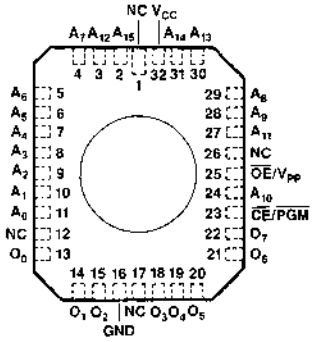
PINS / MODE	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other addresses are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE AAH.

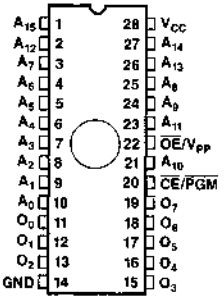
PIN CONFIGURATION

TOP VIEW

Chip Carrier



CERDIP



PRODUCT SELECTION GUIDE

PARAMETER	WS57C512F-55	WS57C512F-70	WS57C512F-90
Address Access Time (Max)	55 ns	70 ns	90 ns
Chip Select Time (Max)	55 ns	70 ns	90 ns
Output Enable Time (Max)	25 ns	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +13V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

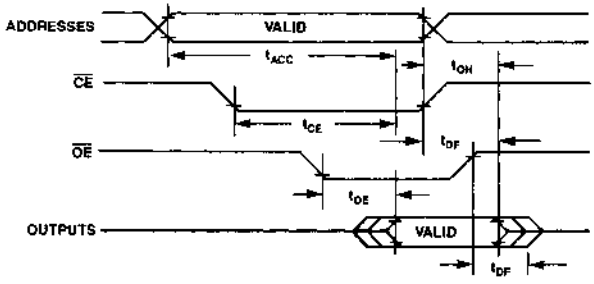
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	CE = V_{CC} ± 0.3V (Note 1)			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	CE = V_{IH} (Note 2)			2	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		40	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		35	mA
			Military		45	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1. CMOS Inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL Inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 3 mA/MHz for A.C. power component.

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS57C512F-55		WS57C512F-70		WS57C512F-90		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70		90	
$\overline{OE}$ to Output Delay	t_{OE}		25		30		30	
Output Disable to Output Float	t_{DF}		25		30		30	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM

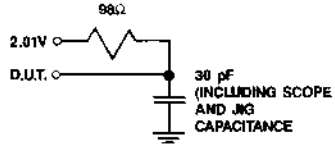


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES: 4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

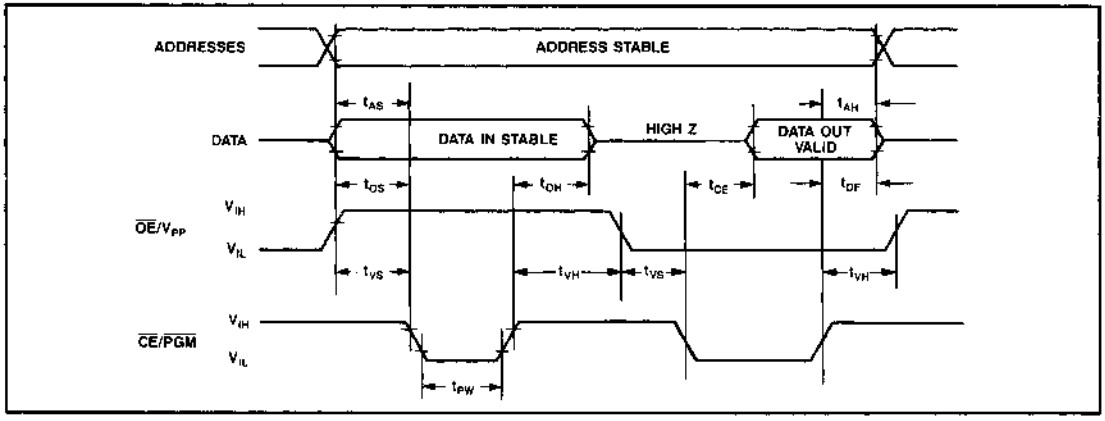
NOTES: 6. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
8. During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
V_{PP} Hold Time	t_{VH}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		70	ns
Data Valid From Chip Enable	t_{CE}			70	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	1		10	ms

NOTE: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



WAFERSCALE INTEGRATION, INC.

64K × 8 CMOS EPROM

KEY FEATURES

- **High Performance CMOS**
  — 100 ns Access Time
- **Fast Programming**
- **Drop-In Replacement for 27C512 or 27512**
- **DESC SMD #5962-87648**
- **300 Mil Dip or Standard 600 Mil Dip**
- **EPI Processing**
  — Latch-Up Immunity to 200 mA
  — ESD Protection Exceeds 2000V
- **Standard JEDEC EPROM Pinout**

3

GENERAL DESCRIPTION

The WS27C512L is a HIGH PERFORMANCE 512K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in WSI's latest CMOS EPROM technology which enables it to operate at speeds as fast as 100 ns access time over the full operating range.

The WS27C512L can directly replace any 64K × 8 EPROM which conforms to the JEDEC standard. Examples of this would be as follows: 27512, 27C512, or 27C512F. It can be easily programmed using standard EPROM programmers or the MagicPro™ IBM PC compatible engineering programmer offered by WSI.

The WS27C512L is also available in a 300 mil Dip. The pin configuration remains the same as the 600 mil wide package and the programming algorithms are unchanged. This enables a simple PCB layout change to take advantage of a 50% reduction in required board space.

The WS27C512L provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 100-ns access time provides no-wait-state operation with high-performance CPUs such as the 16-MHz 80186, 16-MHz 68020, or 12-MHz 80386. The WS27C512L offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The WS27C512L is configured in the standard JEDEC EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The WS27C512L is one member of a high density EPROM Family which ranges in density from 64K to 4 Megabit.

PRODUCT SELECTION GUIDE

PARAMETER	WS27C512L-10	WS27C512L-12	WS27C512L-15	WS27C512L-20
Address Access Time (Max)	100 ns	120 ns	150 ns	200 ns
Chip Select Time (Max)	100 ns	120 ns	150 ns	200 ns
Output Enable Time (Max)	30 ns	35 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Commercial	0°C to +70°C	+5V	±5% or ±10%
Military	−55°C to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

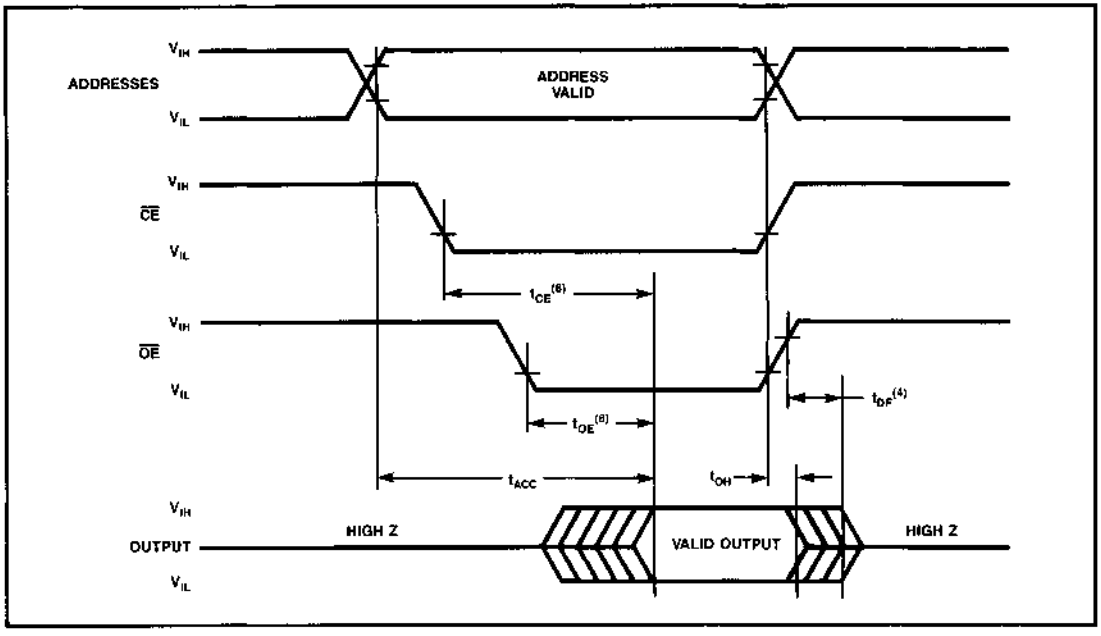
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}(3)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}(1)	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	F = 5 MHz		40	mA
			F = 8 MHz		50	
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	27C512L-10		27C512L-12		27C512L-15		27C512L-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		30		35		40		40	
t_{DF}(2)	Output Disable to Output Float		30		35		40		40	
t_{OH}(2)	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ± 0.3V.

A.C. WAVEFORMS



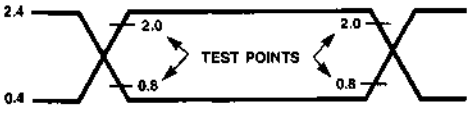
3

CAPACITANCE(4) T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP(5)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

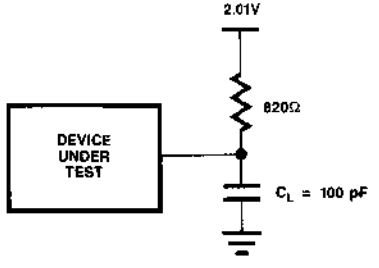
NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages
6. $\overline{OE}$ may be delayed up to t_{CE}–t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

MODE SELECTION

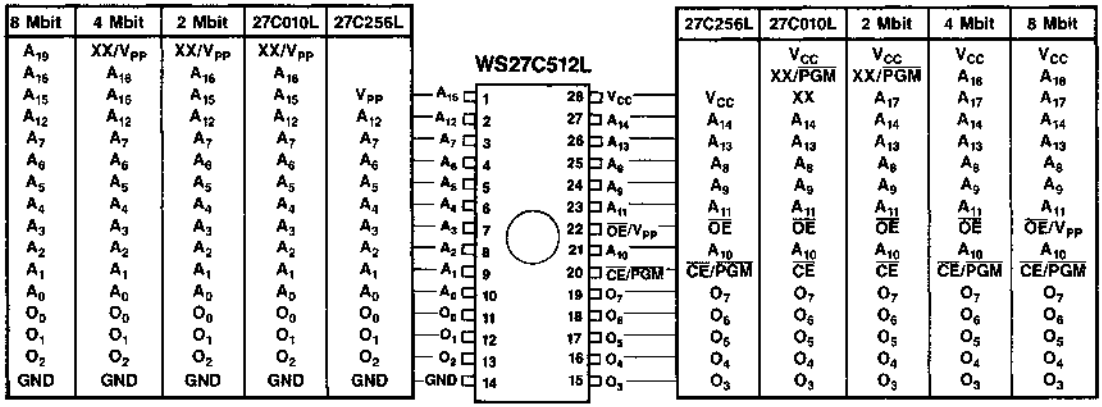
The modes of operation of the WS27C512L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

Table 1. Modes Selection

MODE \ PINS		$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	A_9	A_0	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{PP}[8]	X	X	5.8V	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	5.8V	D_{OUT}
Program Inhibit		V_{IH}	V_{PP}[8]	X	X	5.0V	High Z
Signature	Manufacturer[9]	V_{IL}	V_{IL}	V_H[8]	V_{IL}	5.0V	23 H
	Device[9]	V_{IL}	V_{IL}	V_H[8]	V_{IH}	5.0V	C3 H

NOTES:
7. X can be V_{IL} or V_{IH}.
8. $V_H = V_{PP} = 12.75 \pm 0.25V$.
9. A_1–A_8, A_{10}–$A_{15} = V_{IL}$.

DIP PIN CONFIGURATIONS

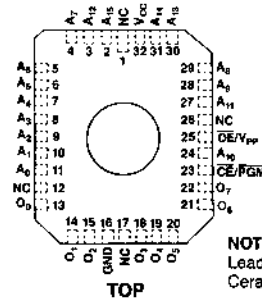


NOTE: 10. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C512L pins.

PIN NAMES

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

LCC PIN CONFIGURATION



NOTE: Leadless or Leaded, Plastic or Ceramic Package

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.8V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

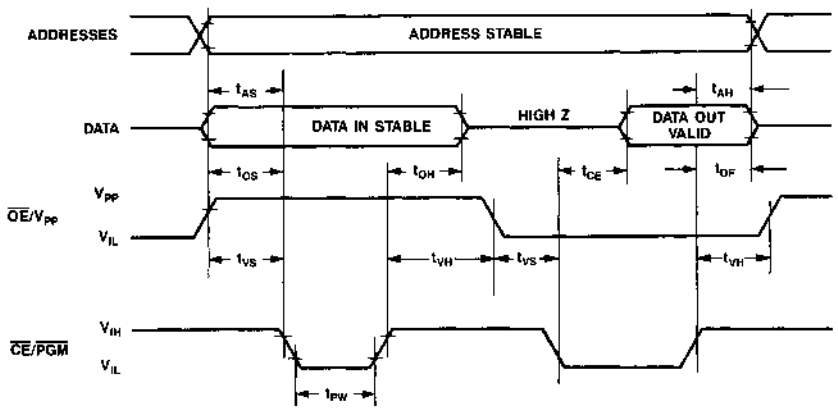
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current, See I_{CC2}	I_{CC}		40	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES: 11. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
12. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
13. During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.8V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
V_{PP} Hold Time	t_{VH}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Chip Enable	t_{CE}			55	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

PROGRAMMING WAVEFORM



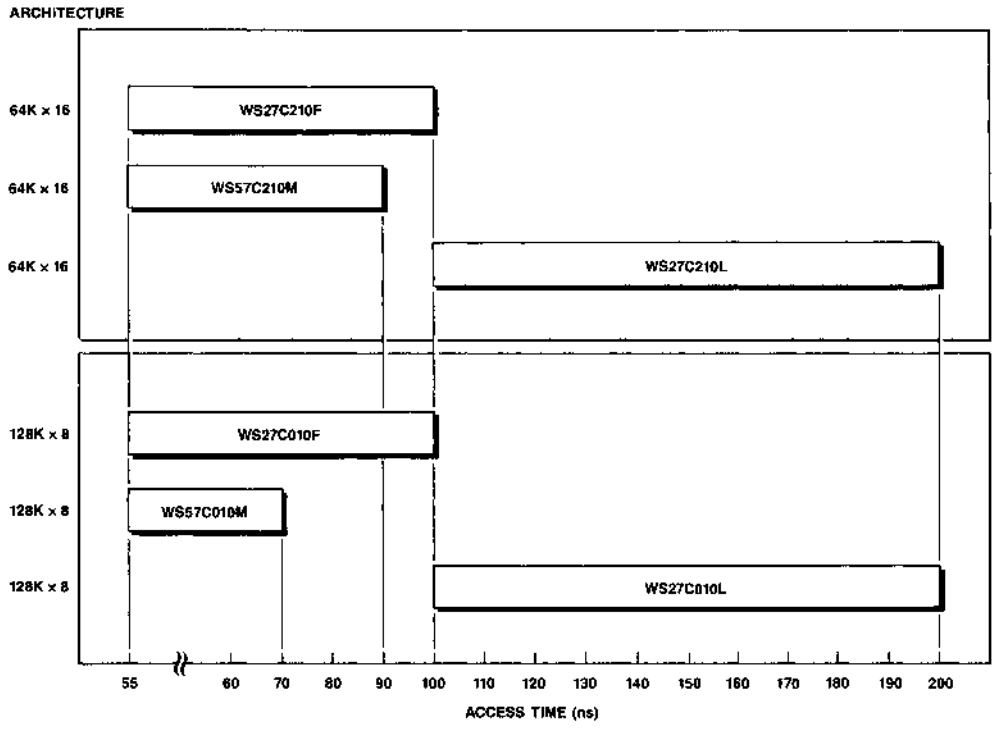
PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING RANGE		WSI MANUFACTURING PROCEDURE
				TEMPERATURE	V_{CC}	
WS27C512L-10D/5	100	28 Pin CERDIP, 0.6″	D2	Comm'l	±5%	Standard
WS27C512L-12D	120	28 Pin CERDIP, 0.6″	D2	Comm'l	±10%	Standard
WS27C512L-12J	120	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C512L-15CMB	150	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C512L-15D	150	28 Pin CERDIP, 0.6″	D2	Comm'l	±10%	Standard
WS27C512L-15DMB	150	28 Pin CERDIP, 0.6″	D2	Military	±10%	MIL-STD-883C
WS27C512L-15J	150	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C512L-15LMB	150	32 Pin CLDCC	L3	Military	±10%	MIL-STD-883C
WS27C512L-20CMB	200	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C512L-20DMB	200	28 Pin CERDIP, 0.6″	D2	Military	±10%	MIL-STD-883C

1 MEG EPROM SELECTION GUIDE



WAFERSCALE INTEGRATION, INC.

128K x 8 CMOS EPROM

KEY FEATURES

- **High Performance CMOS**
  - 100 ns Access Time
- **Fast Programming**
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **DESC SMD No. 5962-89614**
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
- **Compatible with JEDEC 27010 and 27C010 EPROMs**
- **JEDEC Standard Pin Configuration**
  - 32 Pin Dip Package
  - 32 Pin Chip Carrier

3

GENERAL DESCRIPTION

The WS27C010L is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128 K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature during read operations allows memory expansions from 1M to 8M bits with no printed circuit board changes.

The WS27C010L can directly replace lower density 28-pin EPROMs by adding an A_{16} address line and V_{CC} jumper. During the normal read operation PGM and V_{PP} are in a "don't care" state which allows higher order addresses, such as A_{17}, A_{18}, and A_{19} to be connected without affecting the normal read operation. This allows memory upgrades to 8M bits without hardware changes. The WS27C010L will also be offered in a 32-pin plastic Dip with the same upgrade path.

The WS27C010L provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 100-ns access time provides no-wait-state operation with high-performance CPUs such as the 16-MHz 80186, 16-MHz 68020, or 12-MHz 80386. The WS27C010L offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The WS27C010L is one of an eight product megabit EPROM family. Other byte-wide family members are the faster WS27C010F, the faster WS57C010F with high bus drive and the WS57C010M EPROM module. Word-wide (64K x 16) family members are the WS27C210L, the faster WS27C210F, the faster WS57C210F with high bus drive and the WS57C210M EPROM module.

The WS27C010L is manufactured using WSI's advanced CMOS technology.

The WS27C010L is one member of a high density EPROM Family which ranges in density from 64K to 4 Megabit.

PRODUCT SELECTION GUIDE

PARAMETER	27C010L-10	27C010L-12	27C010L-13	27C010L-15	27C010L-20
Address Access Time (Max)	100 ns	120 ns	130 ns	150 ns	200 ns
Chip Select Time (Max)	100 ns	120 ns	130 ns	150 ns	200 ns
Output Enable Time (Max)	30 ns	35 ns	35 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Commercial	0°C to +70°C	+5V	±5% or ±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

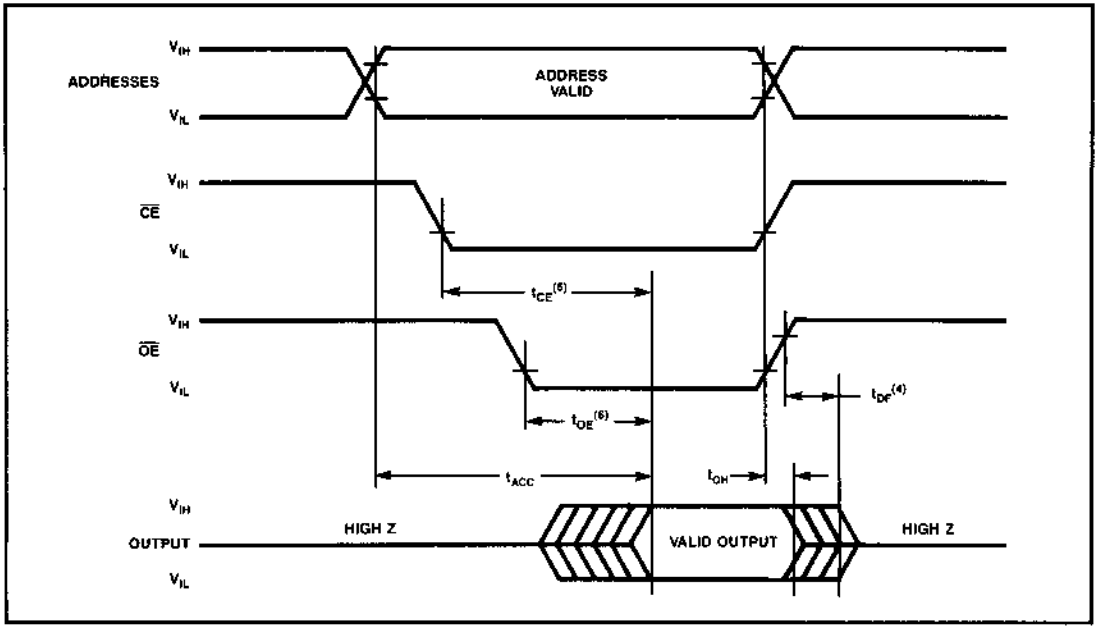
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}(3)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}(1)	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	F = 5 MHz		50	mA
			F = 8 MHz		60	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	-10		-12		-13		-15		-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		100		120		130		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		130		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		30		35		35		40		40	
t_{DF}(2)	Output Disable to Output Float		30		35		35		40		40	
t_{OH}(2)	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ± 0.3V.

A.C. WAVEFORMS

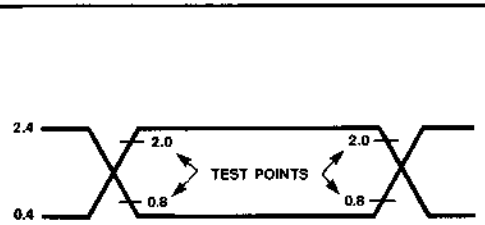


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

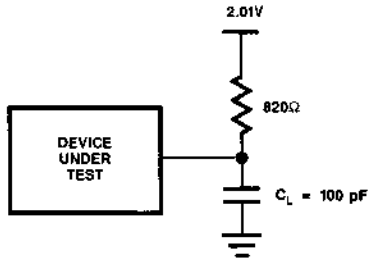
NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to t_{CE}–t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

MODE SELECTION

The modes of operation of the WS27C010L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

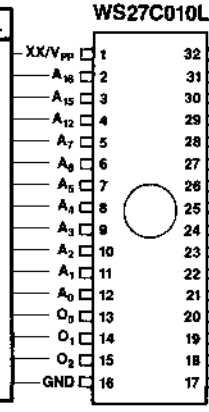
Table 1. Modes Selection

MODE \ PINS		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X[1]	X	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}[8]	6.0V	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}[8]	6.0V	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}[8]	5.0V	High Z
Signature	Manufacturer[9]	V_{IL}	V_{IL}	X	V_H[8]	V_{IL}	X	5.0V	23 H
	Device[9]	V_{IL}	V_{IL}	X	V_H[8]	V_{IH}	X	5.0V	C1 H

NOTES:
7. X can be V_{IL} or V_{IH}
8. $V_H = V_{PP} = 12.75 \pm 0.25V$.
9. A_1–A_8, A_{10}–$A_{16} = V_{IL}$

DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	27C512L	27C256L
A_{19}	XX/V_{PP}	XX/V_{PP}		
A_{18}	A_{18}	A_{18}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



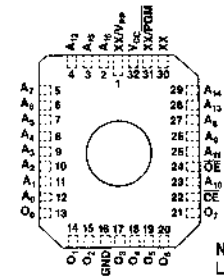
27C256L	27C512L	2 Mbit	4 Mbit	8 Mbit
		V_{CC}	V_{CC}	V_{CC}
		XX/$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$	$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$/$\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE: 9. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C010L pins.

PIN NAMES

A_0–A_{16}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

LCC PIN CONFIGURATION



TOP

NOTE: Leadless or Leaded, Plastic or Ceramic Package

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

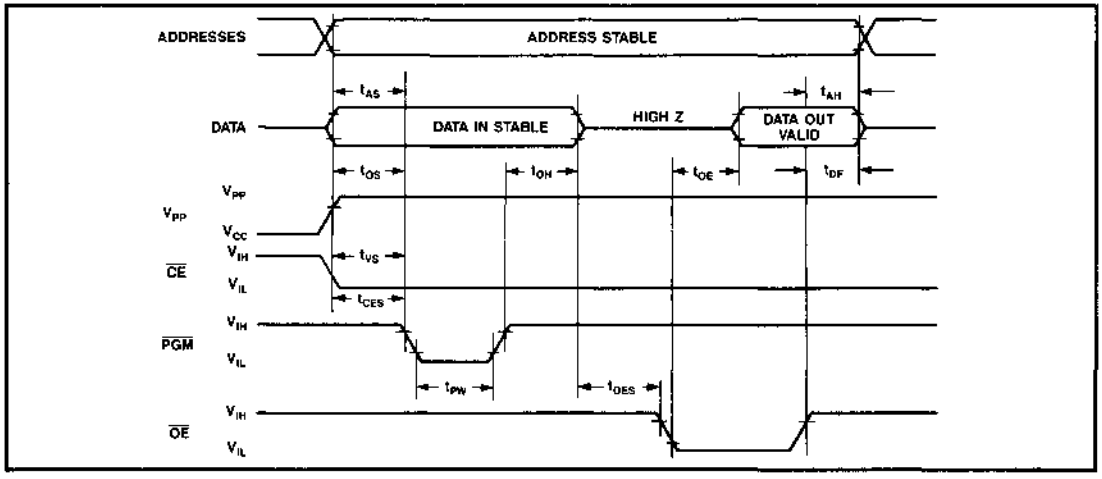
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES: 10. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
11. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
12. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING RANGE		WSI MANUFACTURING PROCEDURE
				TEMPERATURE	V_{CC}	
WS27C010L-10D/5	100	32 Pin CERDIP, 0.6"	D4	Comm'l	±5%	Standard
WS27C010L-10L/5	100	32 Pin CLDCC	L3	Comm'l	±5%	Standard
WS27C010L-12C	120	32 Pad CLLCC	C2	Comm'l	±10%	Standard
WS27C010L-12CMB*	120	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C010L-12D	120	32 Pin CERDIP, 0.6"	D4	Comm'l	±10%	Standard
WS27C010L-12DI	120	32 Pin CERDIP, 0.6"	D4	Industrial	±10%	Standard
WS27C010L-12DMB*	120	32 Pin CERDIP, 0.6"	D4	Military	±10%	MIL-STD-883C
WS27C010L-12J	120	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C010L-12L	120	32 Pin CLDCC	L3	Comm'l	±10%	Standard
WS27C010L-12P	120	32 Pin Plastic Dip, 0.6"	P5	Comm'l	±10%	Standard
WS27C010L-13CMB*	130	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C010L-13DMB*	130	32 Pin CERDIP, 0.6"	D4	Military	±10%	MIL-STD-883C
WS27C010L-15CI	150	32 Pad CLLCC	C2	Industrial	±10%	Standard
WS27C010L-15CMB	150	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C010L-15D	150	32 Pin CERDIP, 0.6"	D4	Comm'l	±10%	Standard
WS27C010L-15DI	150	32 Pin CERDIP, 0.6"	D4	Industrial	±10%	Standard
WS27C010L-15DMB	150	32 Pin CERDIP, 0.6"	D4	Military	±10%	MIL-STD-883C
WS27C010L-15J	150	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C010L-15LMB	150	32 Pin CLDCC	L3	Military	±10%	MIL-STD-883C
WS27C010L-15P	150	32 Pin Plastic Dip, 0.6"	P5	Comm'l	±10%	Standard
WS27C010L-20C	200	32 Pad CLLCC	C2	Comm'l	±10%	Standard
WS27C010L-20CMB	200	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C010L-20D	200	32 Pin CERDIP, 0.6"	D4	Comm'l	±10%	Standard
WS27C010L-20DMB	200	32 Pin CERDIP, 0.6"	D4	Military	±10%	MIL-STD-883C
WS27C010L-20J	200	32 Pin PLDCC	J4	Comm'l	±10%	Standard
WS27C010L-20P	200	32 Pin Plastic Dip, 0.6"	P5	Comm'l	±10%	Standard

*These products are Advance Information.

1 Meg (128K × 8) EPROM MODULE

KEY FEATURES

- **High-Density 1024K-bit CMOS EPROM Module**
- **Utilizes Four WS57C256F High-Speed CMOS EPROMs**
- **Ultra-High Speed Access Time**
  - 55 ns
- **Simplified Upgrade Path From**
  - 256K EPROM (32K x 8)
  - 512K EPROM (64K x 8)
- **Fast Programming**
  - 30 Seconds Typical
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 32 Pin Ceramic Side-Brazed Dip Package

3

GENERAL DESCRIPTION

The WS57C010M is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128 K-words of 8 bits each. The WS57C010M is constructed using four high-performance WS57C256F EPROMs in a 32-pin side-brazed multi-layer co-fired package. The WS57C256F is manufactured using WSI's advanced CMOS split-gate EPROM technology. The 55 ns access time of the WS57C010M enables it to operate in high performance systems.

High performance microprocessors such as the 80386 and 68020 require sub-70 ns memory access times to operate at or near full speed. The WS57C010M enables such systems to incorporate operating systems and/or applications software into EPROM. This in turn enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS57C010M pin configuration was established to enable memory upgrades from 256K and 512K EPROMs. V_{PP} is "don't care" and $\overline{PGM}$ is held low during normal read operation.

The WS57C010M is part of a three product megabit EPROM module family. Other family members are the WS57C210M (64K x 16) and the WS27C240M (256K x 16).

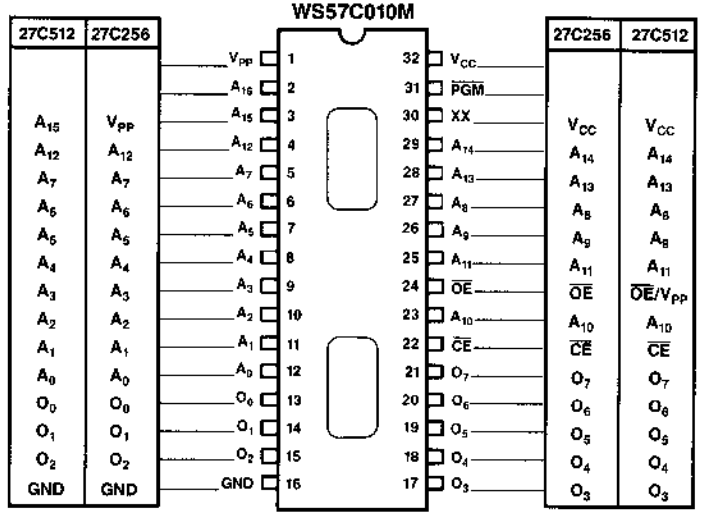
PRODUCT SELECTION GUIDE

PARAMETER	WS57C010M-55	WS57C010M-70
Address Access Time (Max)	55 ns	70 ns
Chip Select Time (Max)	55 ns	70 ns
Output Enable Time (Max)	35 ns	40 ns

PIN NAMES

A_0–A_{16}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program Control
XX	Don't Care (During Read)

DIP PIN CONFIGURATIONS



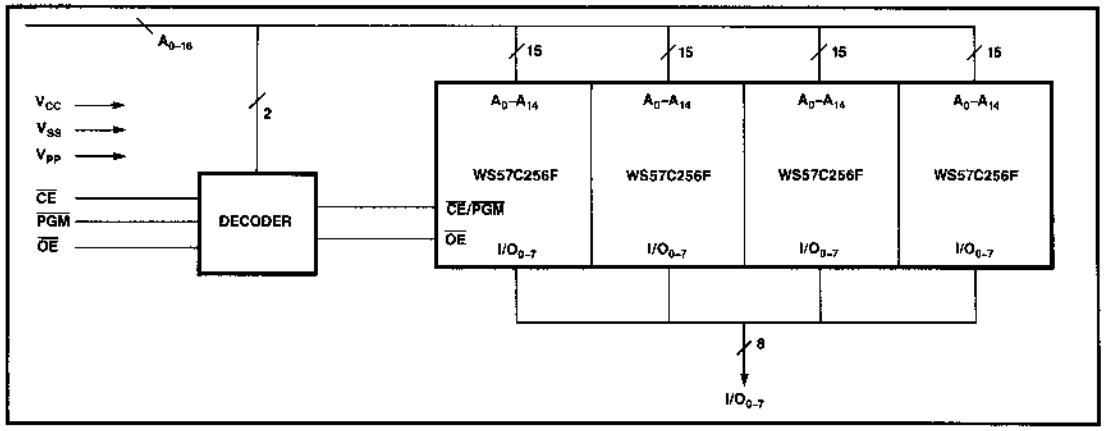
NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS57C010M pins.

MODE SELECTION

MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IL}	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	X	V_{IH}	X	V_{CC}	High Z
Standby	V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z

NOTE: X can be either V_{IL} or V_{IH}.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

3

READ OPERATION

DC CHARACTERISTICS Over Operating Range (See Above)

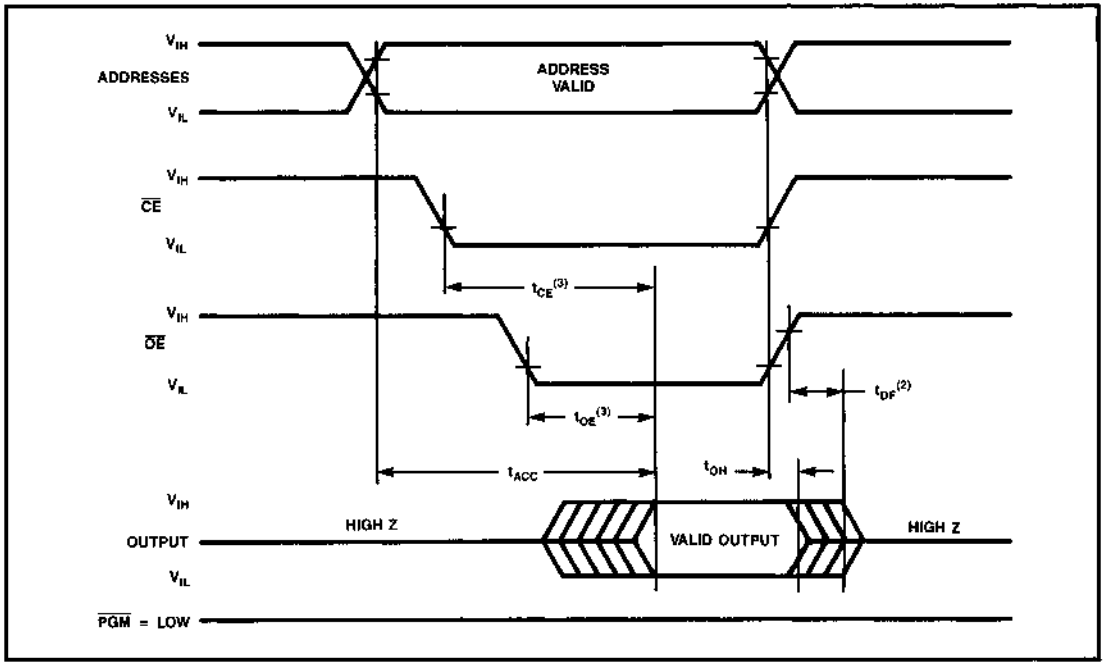
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 5.5V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V		10	µA
I_{PP1}	V_{PP} Load Current	$V_{PP} \leq V_{CC}$		10	µA
I_{SB} (TTL)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		20	mA
I_{SB} (CMOS)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		5	mA
I_{CC} (TTL)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		200	mA
V_{IL}	Input Low Voltage		−0.1	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA	2.4		V
V_{PP}	V_{PP} Read Voltage		−0.1	V_{CC} +1	V

AC CHARACTERISTICS Over Operating Range (See Above)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	57C010M-55		57C010M-70		UNITS
			MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		55		70	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		35		40	ns
t_{DF}[1]	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	35	0	40	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		ns

NOTE: 1. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

AC READ TIMING DIAGRAM



NOTES:
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE

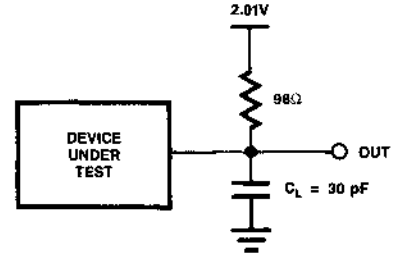
SYMBOL	PARAMETER	CONDITIONS	TYP[2,4]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	20	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	24	32	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	54	75	pF

NOTE: 4. Typical values are for T_A = 25°C and nominal supply voltages, f = 1 MHz.

AC TESTING INPUT/OUTPUT WAVEFORM

A.C. testing inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

AC TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

PROGRAMMING INFORMATION[5,6,7]

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		30	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

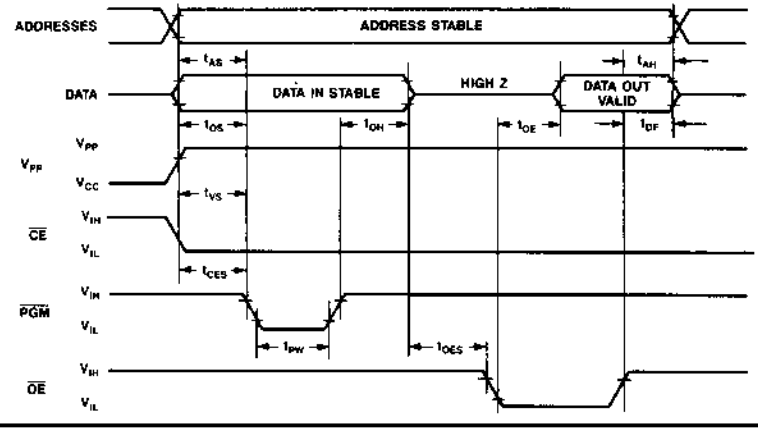
NOTES: 5. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
6. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
7. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1	0.2	4	ms

NOTE: Single shot programming algorithms should use a single 4 ms pulse.

PROGRAMMING WAVEFORM



1 Meg (128K x 8) CMOS EPROM

KEY FEATURES

- **High Performance**
  - 55 ns
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **Pin Compatible with WS27C010L**
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 32 Pin Dip Package

3

GENERAL DESCRIPTION

The WS27C010F is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128 K-words of 8 bits each. The 55 ns access time of the WS27C010F enables it to operate in high performance systems. The "Don't Care" feature during read operations enables memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 80386 and 68020 require 55 ns memory access times to operate at or near full speed. The WS27C010F enables such systems to incorporate operating systems and/or applications software into EPROM. This enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS27C010F pin configuration was established to enable memory upgrades to 8M bits without hardware changes to the printed circuit board. Pins 1 and 31 are "don't care" during normal read operation. This enables higher order addresses to be connected to these pins (see DIP Pin Configurations). When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS27C010F is part of an eight product megabit EPROM family. Byte-wide family members (128K x 8) are the WS27C010L, WS27C010F (described herein) and WS57C010F as the high-speed version. Word-wide (64K x 16) family members are the WS27C210L, WS27C210F and the high-speed WS57C210F. The WS57C010M and WS57C210M are high speed, high bus drive EPROM modules.

The WS27C010F is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	WS27C010F-55	WS27C010F-70	WS27C010F-90	WS27C010F-10
Address Access Time (Max)	55 ns	70 ns	90 ns	100 ns
Chip Select Time (Max)	55 ns	70 ns	90 ns	100 ns
Output Enable Time (Max)	25 ns	25 ns	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

READ OPERATION

DC CHARACTERISTICS 0°C ≤ T_A ≤ +70°C; V_{CC} (Comm'l/Military) = +5V ± 10%.

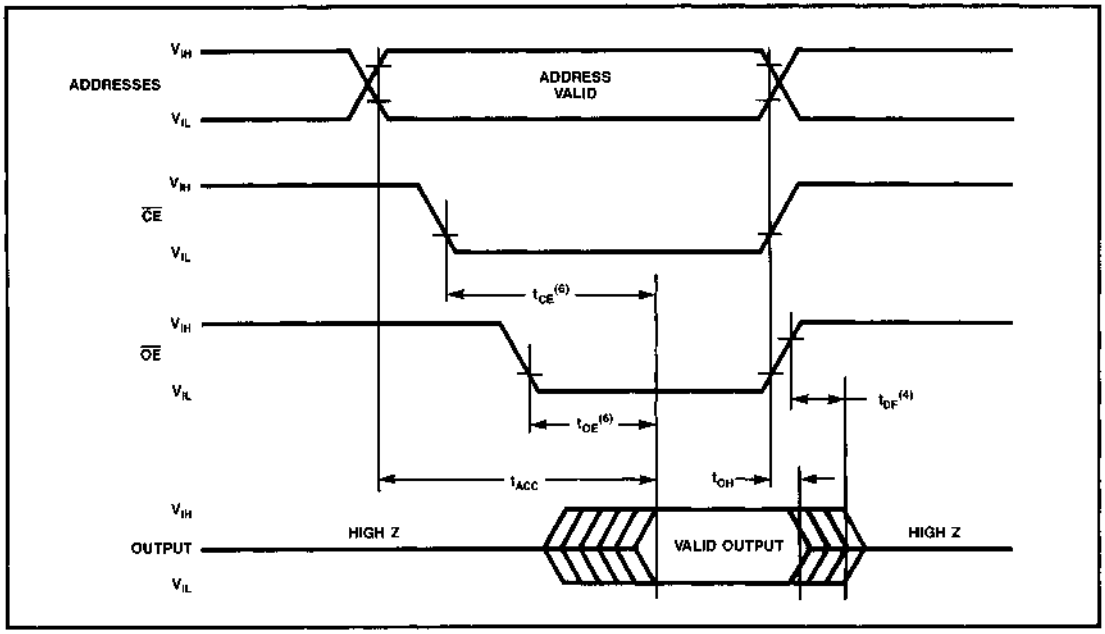
SYMBOL	PARAMETER	CONDITIONS	LIMITS		
			MIN	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 5.5V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V		10	µA
I_{PP}(1)	V_{PP} Load Current	$V_{PP} \leq V_{CC}$		10	µA
I_{SB} TTL	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		2	mA
I_{SB} CMOS	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		500	µA
I_{CC}(1)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		40(3)	mA
V_{IL}	Input Low Voltage		−0.1	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
V_{PP}(1)	V_{PP} Read Voltage	V_{CC} = 5.0V ± 0.25	−0.1	V_{CC}+1	V

AC CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	-55		-70		-90		-10		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		55		70		90		100	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		55		70		90		100	
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		25		25		30		30	
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	25	0	25	0	30	0	30	
t_{OH}	Output Hold From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		0		

NOTES:
1. V_{PP} should be at a TTL level except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Add 2 mA/MHz for A.C. power component.

AC READ TIMING DIAGRAM



CAPACITANCE[4] T_A = 25°C, f = 1 MHz

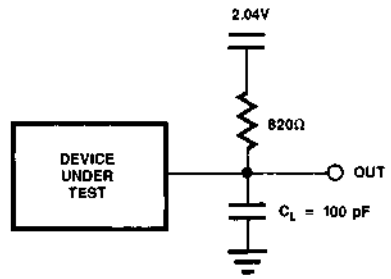
SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM

A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

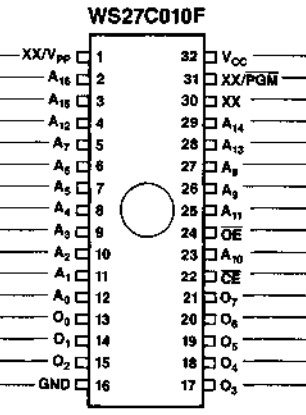
A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	27512	27256
A_{19}	XX/V_{PP}	XX/V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



27256	27512	2 Mbit	4 Mbit	8 Mbit
		V_{CC}	V_{CC}	V_{CC}
		$XX/\overline{PGM}$	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C010F pins.

PIN NAMES

A_0–A_{16}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

1 Meg (64K x 16) CMOS EPROM

KEY FEATURES

- **Ultra-High Performance**
  - 100 ns
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 40 Pin Dip Package
  - 44 Pin Chip Carrier

3

GENERAL DESCRIPTION

The WS27C210L is an ultra-high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 64 K-words of 16 bits each. The 100 ns access time of the WS27C210L enables it to operate in high performance systems. The "Don't Care" feature during read operations enables memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 80386 and 68020 require sub-120 ns memory access times to operate at or near full speed. The WS27C210L enables such systems to incorporate operating systems and/or applications software into EPROM. This in turn enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS27C210L pin configuration was established to allow memory upgrades to 8M bits without hardware changes to the printed circuit board. Pins 1 and 39 are "don't care" during normal read operation. This enables higher order addresses to be connected to these pins. When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS27C210L is part of a high density EPROM family which spans densities from 64K to 4 Meg.

The WS27C210L is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	27C210L-10	27C210L-12	27C210L-15	27C210L-20
Address Access Time (Max)	100 ns	120 ns	150 ns	200 ns
Chip Select Time (Max)	100 ns	120 ns	150 ns	200 ns
Output Enable Time (Max)	30 ns	35 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Commercial	0°C to +70°C	+5V	±5% or ±10%
Military	−55°C to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

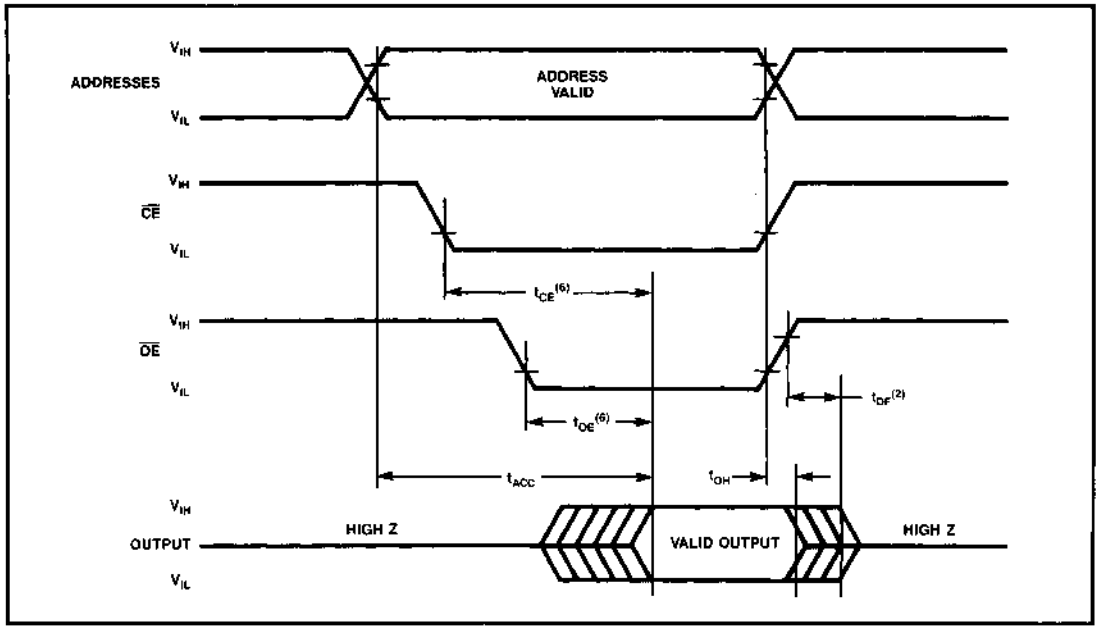
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}[3]	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}[1]	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$	F = 5 MHz		60	mA
			F = 8 MHz		70	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	-10		-12		-15		-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		30		35		40		40	
t_{DF}[2]	Output Disable to Output Float		30		35		40		40	
t_{OH}[2]	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, $V_{IH} = V_{CC} \pm 0.3V$.

AC READ TIMING DIAGRAM

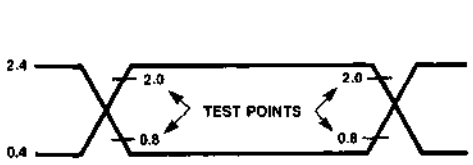


NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}

CAPACITANCE[4] T_A = 25°C, f = 1 MHz

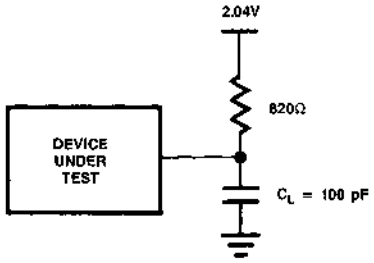
SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

A.C. TESTING INPUT/OUTPUT WAVEFORM



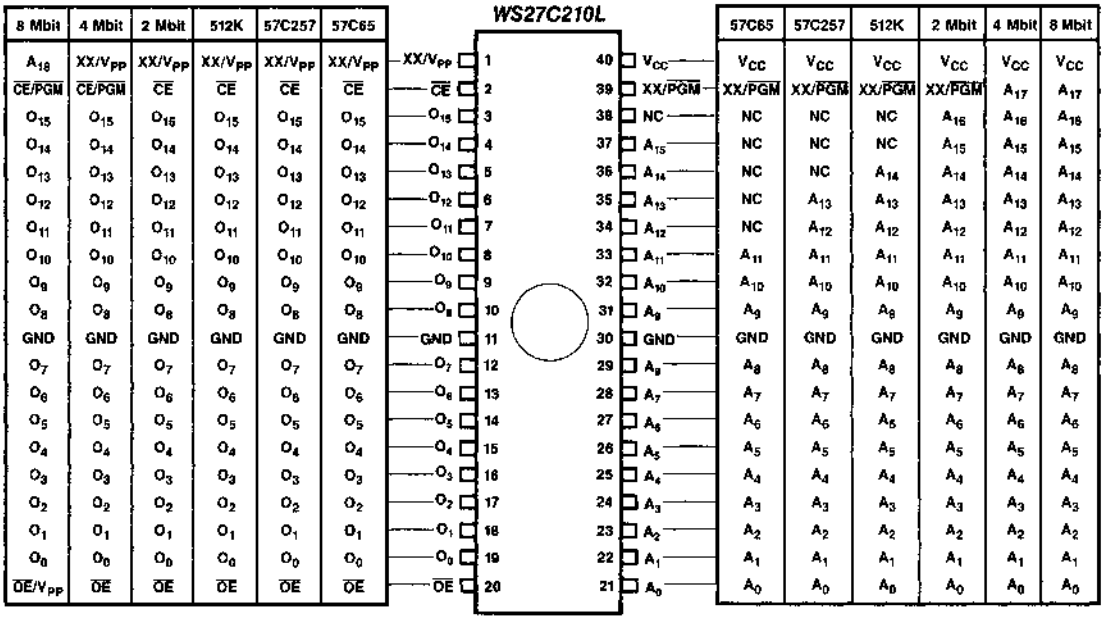
A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

DIP PIN CONFIGURATIONS

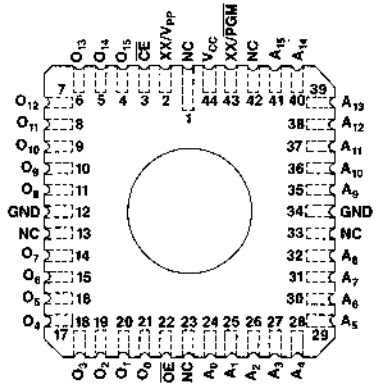


NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C210L pins.

PIN NAMES

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
NC	No Connection
XX	Don't Care (During Read)
$\overline{PGM}$	Program

LCC PIN CONFIGURATION (TOP)



PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

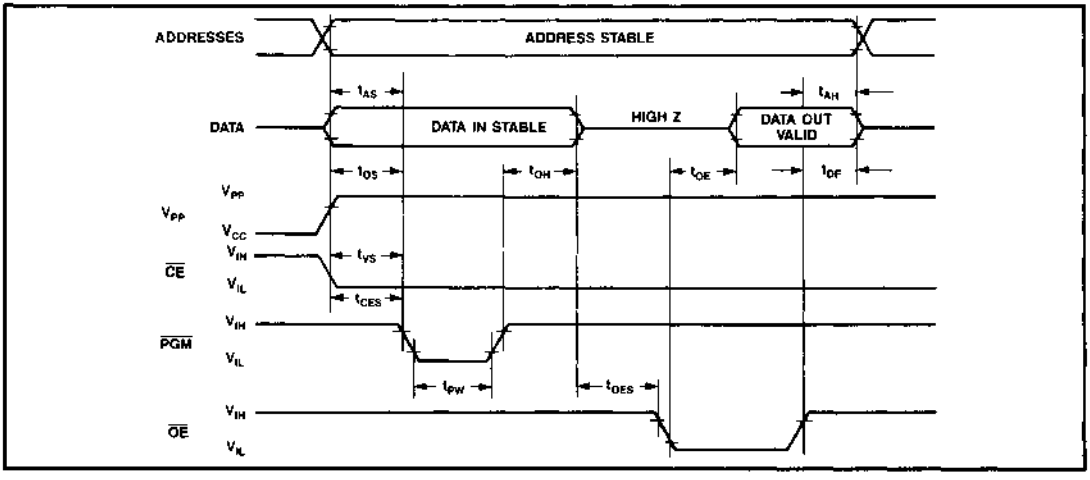
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES: 7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
9. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

PROGRAMMING WAVEFORM



MODE SELECTION

The modes of operation of the WS27C210L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and on A_9 for device signature.

Table 1. Modes Selection

MODE \ PINS		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X[10]	X	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	6.2V	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	6.2V	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	6.2V	High Z
Signature	Manufacturer[12]	V_{IL}	V_{IL}	X	V_H[11]	V_{IL}	X	5.0V	23 H
	Device[12]	V_{IL}	V_{IL}	X	V_H[11]	V_{IH}	X	5.0V	C9 H

NOTES: 10. X can be V_{IL} or V_{IH} 11. $V_H = V_{PP}$ 12. A_1–A_8, A_{10}–$A_{15} = V_{IL}$

PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING RANGE		WSI MANUFACTURING PROCEDURE
				TEMPERATURE	V_{CC}	
WS27C210L-10D/5*	100	40 Pin CERDIP, 0.6"	D3	Comm'l	±5%	Standard
WS27C210L-10J/5*	100	44 Pin PLDCC	J2	Comm'l	±5%	Standard
WS27C210L-12CMB*	120	44 Pad CLLCC	C3	Military	±10%	MIL-STD-883C
WS27C210L-12D	120	40 Pin CERDIP, 0.6"	D3	Comm'l	±10%	Standard
WS27C210L-12DMB*	120	40 Pin CERDIP, 0.6"	D3	Military	±10%	MIL-STD-883C
WS27C210L-12J	120	44 Pin PLDCC	J2	Comm'l	±10%	Standard
WS27C210L-12L	120	44 Pin CLDCC	L4	Comm'l	±10%	Standard
WS27C210L-12LMB*	120	44 Pin CLDCC	L4	Military	±10%	MIL-STD-883C
WS27C210L-15CMB	150	44 Pad CLLCC	C3	Military	±10%	MIL-STD-883C
WS27C210L-15D	150	40 Pin CERDIP, 0.6"	D3	Comm'l	±10%	Standard
WS27C210L-15DMB	150	40 Pin CERDIP, 0.6"	D3	Military	±10%	MIL-STD-883C
WS27C210L-15J	150	44 Pin PLDCC	J2	Comm'l	±10%	Standard
WS27C210L-15L	150	44 Pin CLDCC	L4	Comm'l	±10%	Standard
WS27C210L-15LMB	150	44 Pin CLDCC	L4	Military	±10%	MIL-STD-883C
WS27C210L-20CMB	200	44 Pad CLLCC	C3	Military	±10%	MIL-STD-883C
WS27C210L-20D	200	40 Pin CERDIP, 0.6"	D3	Comm'l	±10%	Standard
WS27C210L-20DMB	200	40 Pin CERDIP, 0.6"	D3	Military	±10%	MIL-STD-883C
WS27C210L-20J	200	44 Pin PLDCC	J2	Comm'l	±10%	Standard
WS27C210L-20L	200	44 Pin CLDCC	L4	Comm'l	±10%	Standard
WS27C210L-20LMB	200	44 Pin CLDCC	L4	Military	±10%	MIL-STD-883C

*These products are Advance Information.

1 Meg (64K x 16) EPROM MODULE

KEY FEATURES

- **High-Density 64K x 16 CMOS EPROM Module**
- **Utilizes Four WS57C256F High-Speed CMOS EPROMs**
- **Ultra-High Speed Access Time**
  — 55 ns
- **Simplified Upgrade Path From**
  — WS57C65 (4K x 16 EPROM)
  — WS57C257 (16K x 16 EPROM)
- **Fast Programming**
  — 15 Seconds Typical
- **EPI Processing**
  — Latch-Up Immunity to 200 mA
  — ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  — 40 Pin Ceramic Side-Brazed Dip Package

GENERAL DESCRIPTION

The WS57C210M is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 64 K-words of 16 bits each. The WS57C210M is constructed using four high-performance WS57C256F EPROMs in a 40-pin side-brazed multi-layer co-fired package. The WS57C256F is manufactured using WSI's advanced CMOS split-gate EPROM technology. The 55 ns access time of the WS57C210M enables it to operate in high performance systems.

High performance microprocessors such as the 80386 and 68020 require sub-70 ns memory access times to operate at or near full speed. The WS57C210M enables such systems to incorporate operating systems and/or applications software into EPROM. This in turn enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS57C210M pin configuration was established to enable memory upgrades from WS57C65 or WS57C257. V_{PP} is "don't care" and $\overline{PGM}$ is held low during normal read operation.

The WS57C210M is part of a three product EPROM module family. Other family members are the WS57C010M (128K x 8) and the WS27C240M (256K x 16).

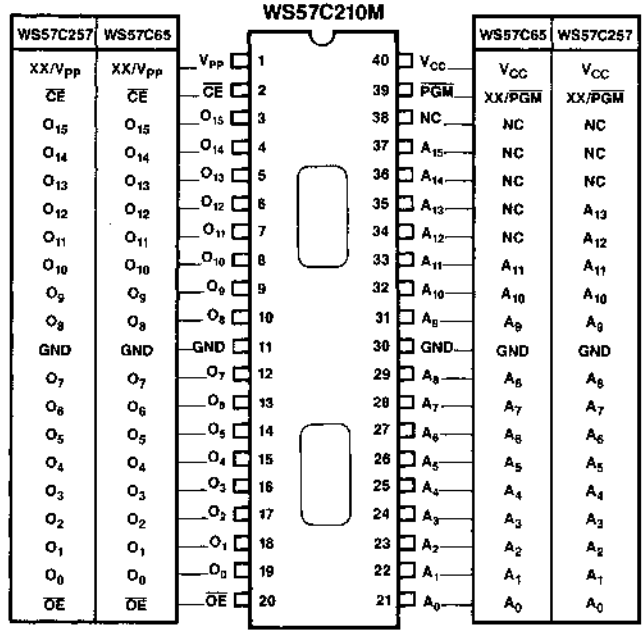
PRODUCT SELECTION GUIDE

PARAMETER	WS57C210M-55	WS57C210M-70	WS57C210M-90
Address Access Time (Max)	55 ns	70 ns	90 ns
Chip Select Time (Max)	55 ns	70 ns	90 ns
Output Enable Time (Max)	35 ns	40 ns	40 ns

PIN NAMES

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
$\overline{PGM}$	Program Control
NC	No Connection
XX	Don't Care (During Read)

DIP PIN CONFIGURATIONS



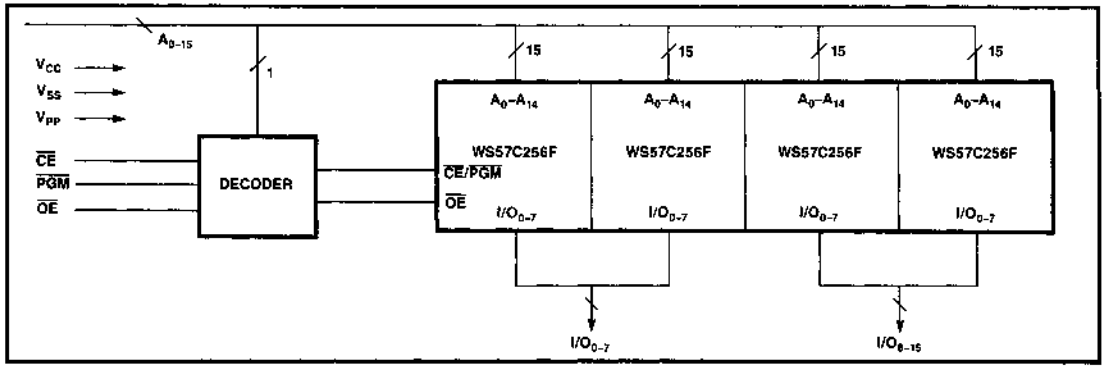
NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS57C210M pins.

MODE SELECTION

MODE \ PINS	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IL}	X	V_{CC}	D_{OUT}
Output Disable	V_{IL}	X	V_{IH}	X	V_{CC}	High Z
Standby	V_{IL}	V_{IH}	X	X	V_{CC}	High Z
Program	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z

NOTE: X can be either V_{IL} or V_{IH}.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

READ OPERATION

DC CHARACTERISTICS Over Operating Range (See Above)

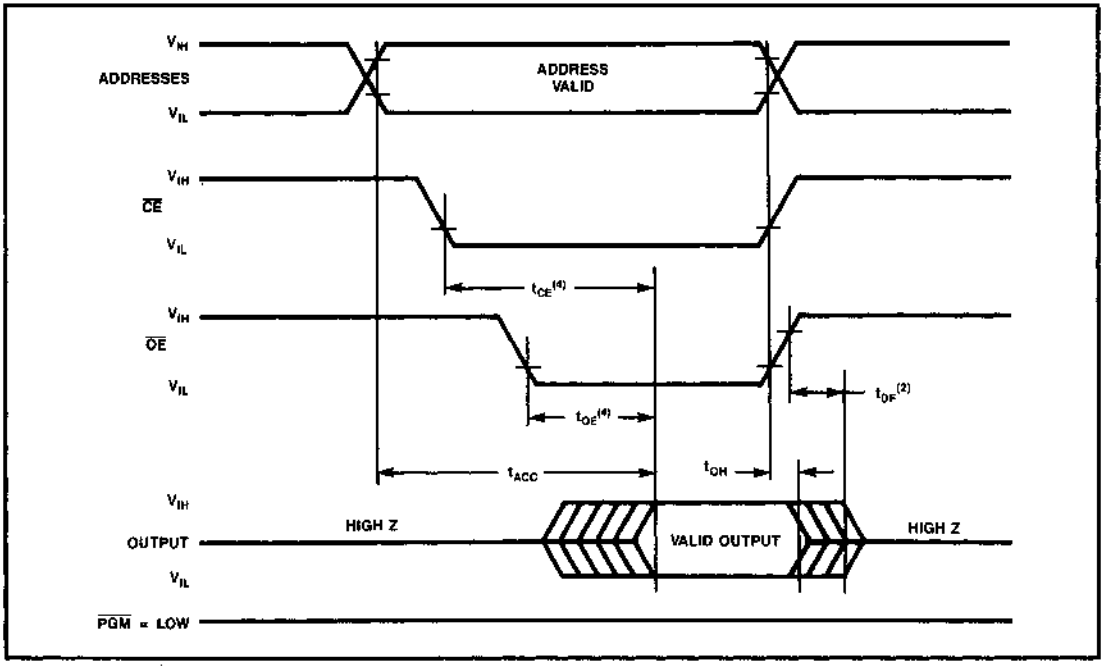
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 5.5V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V		10	µA
I_{PP1}	V_{PP} Load Current	$V_{PP} \leq V_{CC}$		10	µA
I_{SB} (TTL)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		20	mA
I_{SB} (CMOS)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		5	mA
I_{CC} (TTL)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		200	mA
V_{IL}	Input Low Voltage		−0.1	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2 mA	2.4		V
V_{PP}	V_{PP} Read Voltage		−0.1	V_{CC} +1	V

AC CHARACTERISTICS Over Operating Range (See Above)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	57C210M-55		57C210M-70		57C210M-90		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		55		70		90	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		55		70		90	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		35		40		40	ns
t_{DF}[1]	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	35	0	40	0	40	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		ns

NOTE: 1. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

AC READ TIMING DIAGRAM

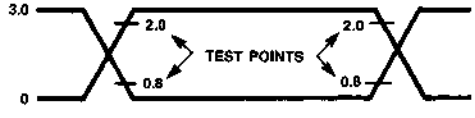


CAPACITANCE(2)

SYMBOL	PARAMETER	CONDITIONS	TYP(3)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	20	30	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	30	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	54	75	pF

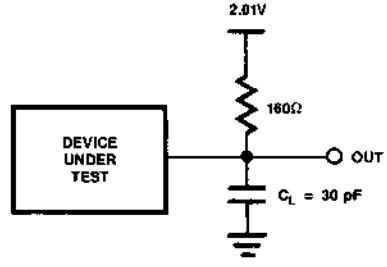
NOTES: 2. This parameter is only sampled and is not 100% tested.
3. Typical values are for T_A = 25°C and nominal supply voltages, f = 1 MHz.
4. $\overline{OE}$ may be delayed up to t_{CE}–t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.

AC TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 3.0V for a Logic "1" and 0V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

AC TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

PROGRAMMING INFORMATION[5,6,7]

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		120	mA
V_{CC} Supply Current	I_{CC}		60	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

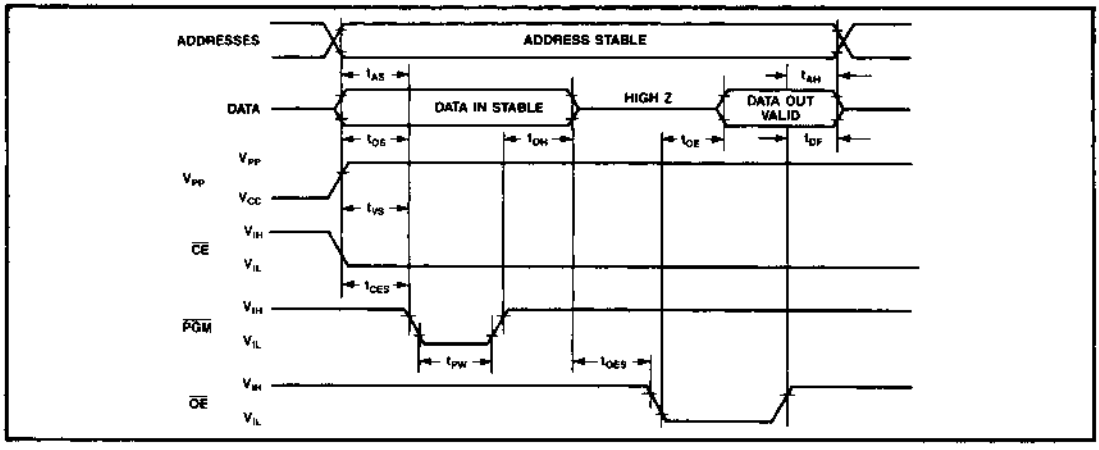
NOTES:
5. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
6. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
7. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Enable Setup Time	t_{CE}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1	0.2	4	ms

NOTE: Single shot programming algorithms should use a single 4 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C210M-55R	55	40 Pin Ceramic S/B, 0.6"	R1	Comm'l	Standard
WS57C210M-70R	70	40 Pin Ceramic S/B, 0.6"	R1	Comm'l	Standard
WS57C210M-70RM	70	40 Pin Ceramic S/B, 0.6"	R1	Military	Standard
WS57C210M-70RMB	70	40 Pin Ceramic S/B, 0.6"	R1	Military	MIL-STD-883C
WS57C210M-90R	90	40 Pin Ceramic S/B, 0.6"	R1	Comm'l	Standard
WS57C210M-90RM	90	40 Pin Ceramic S/B, 0.6"	R1	Military	Standard
WS57C210M-90RMB	90	40 Pin Ceramic S/B, 0.6"	R1	Military	MIL-STD-883C

1 Meg (64K x 16) CMOS EPROM

KEY FEATURES

- **High Performance**
  - 55 ns
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 40 Pin Dip Package

GENERAL DESCRIPTION

The WS27C210F is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 64 K-words of 16 bits each. The 55 ns access time of the WS27C210F enables it to operate in high performance systems. The "Don't Care" feature during read operations enables memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 80386 and 68020 require 55 ns memory access times to operate at or near full speed. The WS27C210F enables such systems to incorporate operating systems and/or applications software into EPROM. This in turn enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS27C210F pin configuration was established to enable memory upgrades to 8M bits without hardware changes to the printed circuit board. Pins 1 and 39 are "don't care" during normal read operation. This enables higher order addresses to be connected to these pins (see DIP Pin Configurations). When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS27C210F is part of an eight product megabit EPROM family. Byte-wide family members are: WS27C010L, WS27C010F and WS57C010F. These three are 128K x 8 EPROMs with the WS57C010F as the highest speed member. The 64K x 16 EPROMs are the WS27C210L, WS27C210F (described herein) and the highest speed version WS57C210F. The WS57C010M and WS57C210M are high speed, high bus drive megabit EPROM modules.

The WS27C210F is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	WS27C210F-55	WS27C210F-70	WS27C210F-90	WS27C210F-10
Address Access Time (Max)	55 ns	70 ns	90 ns	100 ns
Chip Select Time (Max)	55 ns	70 ns	90 ns	100 ns
Output Enable Time (Max)	25 ns	25 ns	30 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Industrial	−40° to +85°C	+5V ± 10%
Military	−55° to +125°C	+5V ± 10%

READ OPERATION

DC CHARACTERISTICS 0°C ≤ T_A ≤ +70°C; V_{CC} (Comm'l/Military) = +5V ± 10%.

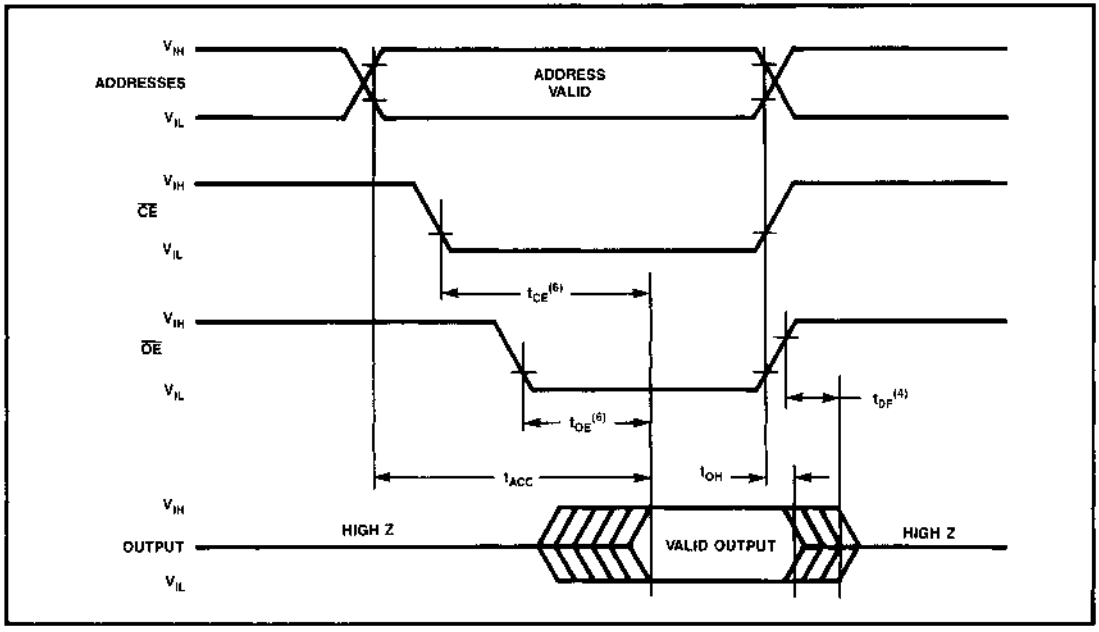
SYMBOL	PARAMETER	CONDITIONS	LIMITS		
			MIN	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 5.5V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V		10	µA
I_{PP}(1)	V_{PP} Load Current	$V_{PP} \leq V_{CC}$		10	µA
I_{SB} TTL	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		2	mA
I_{SB} CMOS	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		500	µA
I_{CC}(1)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		50(3)	mA
V_{IL}	Input Low Voltage		−0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4		V
V_{PP}(1)	V_{PP} Read Voltage	V_{CC} = 5.0V ± 0.25	−0.1	V_{CC} +1	V

AC CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	-55		-70		-90		-10		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		55		70		90		100	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		55		70		90		100	
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		25		25		30		30	
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	25	0	25	0	30	0	30	
t_{OH}	Output Hold From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		0		

NOTES:
1. V_{PP} should be at a TTL level except during programming. The supply current would then be the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_{15} unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. Add 3 mA/MHz for A.C. power component.

AC READ TIMING DIAGRAM

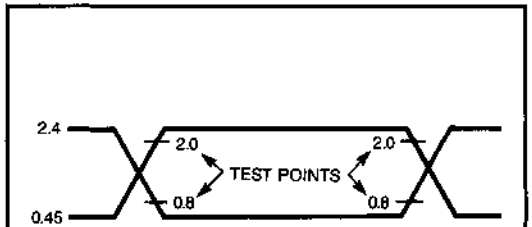


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

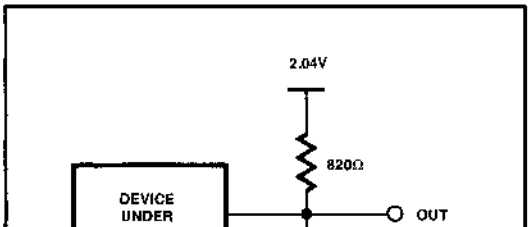
NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. OE may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM



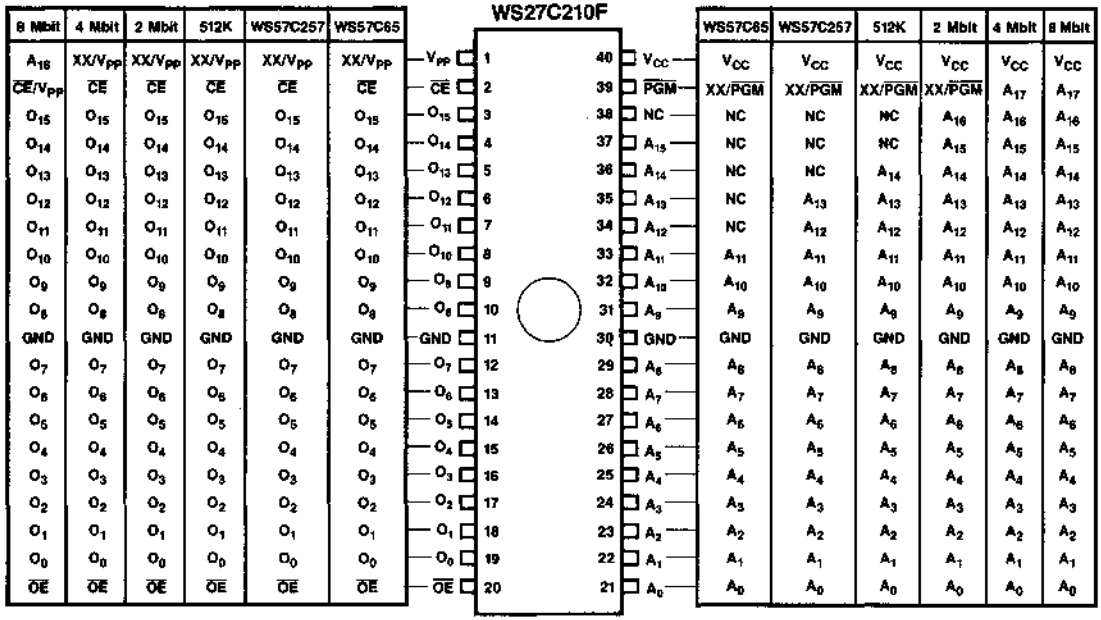
A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

DIP PIN CONFIGURATIONS

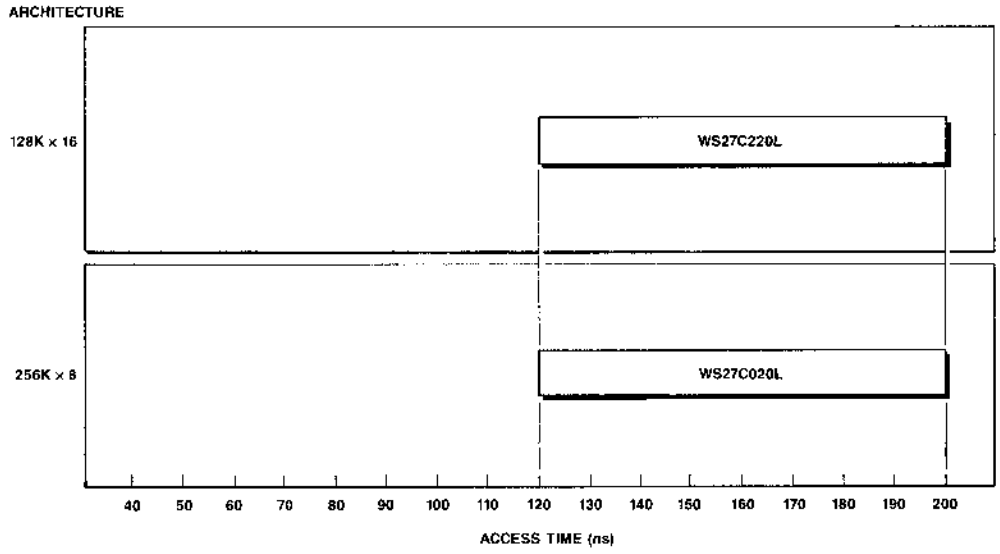


NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C210F pins.

PIN NAMES

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
NC	No Connection
XX	Don't Care (During Read)

2 MEG EPROM SELECTION GUIDE



2 Meg (256K x 8) CMOS EPROM

KEY FEATURES

- **High Performance CMOS**
  - 120 ns Access Time
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
- **Compatible with JEDEC 27020 and 27C020 EPROMs**
- **JEDEC Standard Pin Configuration**
  - 32 Pin Dip Package
  - 32 Pin Chip Carrier

GENERAL DESCRIPTION

The WS27C020L is a high performance, 2,097,152-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 256 K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature during read operations enables memory expansions up to 8M bits with no printed circuit board changes.

The WS27C020L can directly replace lower density 28-pin EPROMs by adding an A_{17} address line and V_{CC} jumper. During the normal read operation PGM and V_{PP} are in a "don't care" state which allows higher order addresses, such as A_{18} and A_{19} to be connected without affecting the normal read operation. This allows memory upgrades to 8M bits without hardware changes. The WS27C020L will also be offered in a 32-pin plastic Dip with the same upgrade path.

The WS27C020L provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 120-ns access time provides no-wait-state operation with high-performance CPUs such as the 16-MHz 80186, 16-MHz 68020, or 12-MHz 80386. The WS27C020L offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The WS27C020L is manufactured using WSI's advanced CMOS technology.

The WS27C020L is one member of a high density WSI EPROM series which ranges in density from 64K to 4 Megabit.

PRODUCT SELECTION GUIDE

PARAMETER	27C020L-12	27C020L-15	27C020L-17	27C020L-20
Address Access Time (Max)	120 ns	150 ns	170 ns	200 ns
Chip Select Time (Max)	120 ns	150 ns	170 ns	200 ns
Output Enable Time (Max)	35 ns	40 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Comm'l	0° to +70°C	+5V	±5% or ±10%
Military	−55° to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

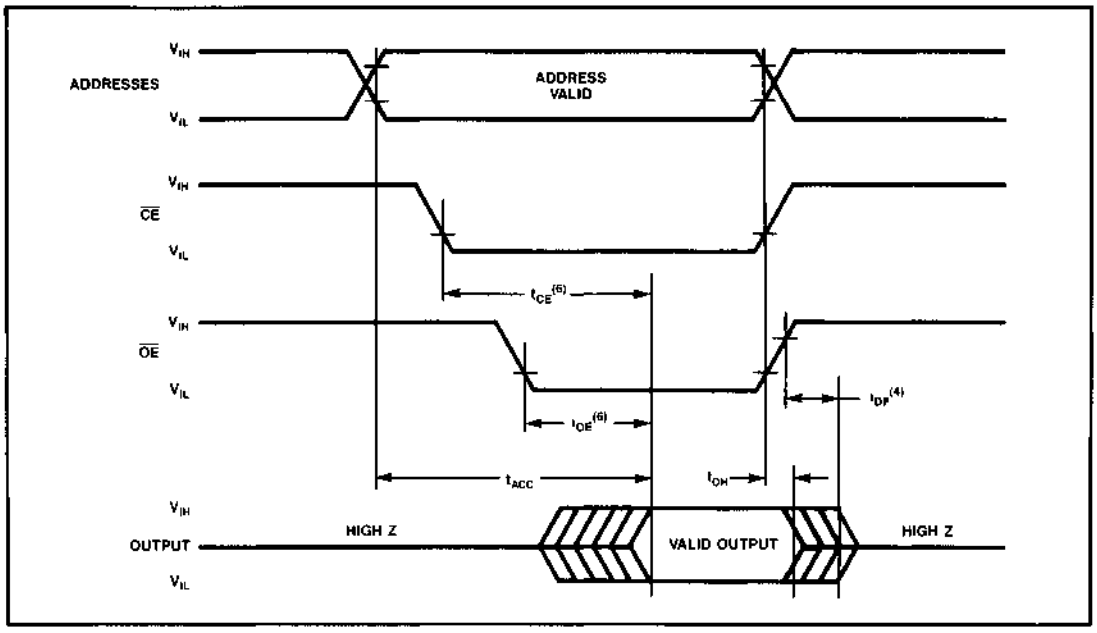
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}[3]	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}[1]	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	F = 5 MHz		50	mA
			F = 8 MHz		60	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	-12		-15		-17		-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		120		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		170		200	
t_{OE}	$\overline{OE}$ to Output Delay		35		40		40		40	
t_{DF}[2]	Output Disable to Output Float		35		40		40		40	
t_{OH}[2]	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ± 0.3V.

AC READ TIMING DIAGRAM

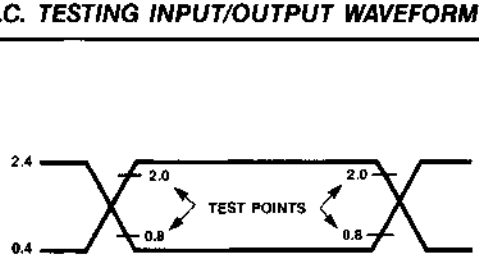


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

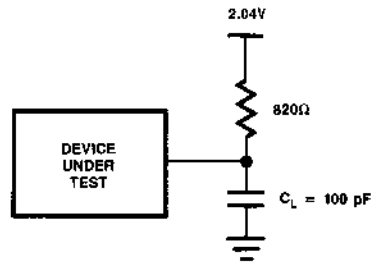
NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

MODE SELECTION

The modes of operation of the WS27C020L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and on A_9 for device signature.

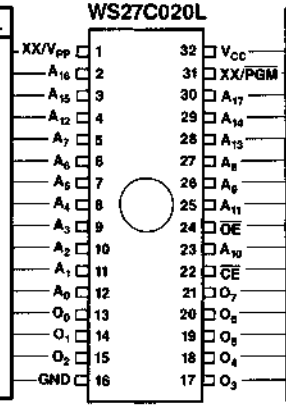
Table 1. Modes Selection

MODE \ PINS		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X[7]	X	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}[8]	6.2V	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}[8]	6.2V	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}[8]	6.2V	High Z
Signature	Manufacturer[9]	V_{IL}	V_{IL}	X	V_H[8]	V_{IL}	X	5.0V	23 H
	Device[9]	V_{IL}	V_{IL}	X	V_H[8]	V_{IH}	X	5.0V	C1 H

NOTES: 7. X can be V_{IL} or V_{IH} 8. $V_H = V_{PP} = 12.75 \pm 0.25V$. 9. A_1–A_8, A_{10}–$A_{17} = V_{IL}$

DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	1 Mbit	27C512L	27C256L
A_{19}	XX/V_{PP}	XX/V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



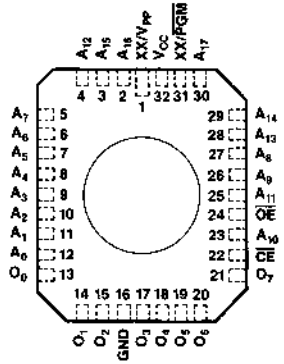
27C256L	27C512L	1 Mbit	4 Mbit	8 Mbit
		V_{CC} / XX/$\overline{PGM}$	V_{CC}	V_{CC}
		XX	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{14}	A_{17}	A_{17}
A_{14}	A_{14}	A_{13}	A_{14}	A_{14}
A_{13}	A_{13}	A_8	A_{13}	A_{13}
A_8	A_8	A_9	A_8	A_8
A_9	A_9	A_{11}	A_9	A_9
A_{11}	A_{11}	$\overline{OE}$	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	A_{10}	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	$\overline{CE}$	A_{10}	A_{10}
$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$	O_7	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_6	O_7	O_7
O_6	O_6	O_5	O_6	O_6
O_5	O_5	O_4	O_5	O_5
O_4	O_4	O_3	O_4	O_4
O_3	O_3		O_3	O_3

NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C020L pins.

PIN NAMES

A_0–A_{17}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

LCC PIN CONFIGURATION



NOTE: Leadless or Leaded, Plastic or Ceramic Package

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

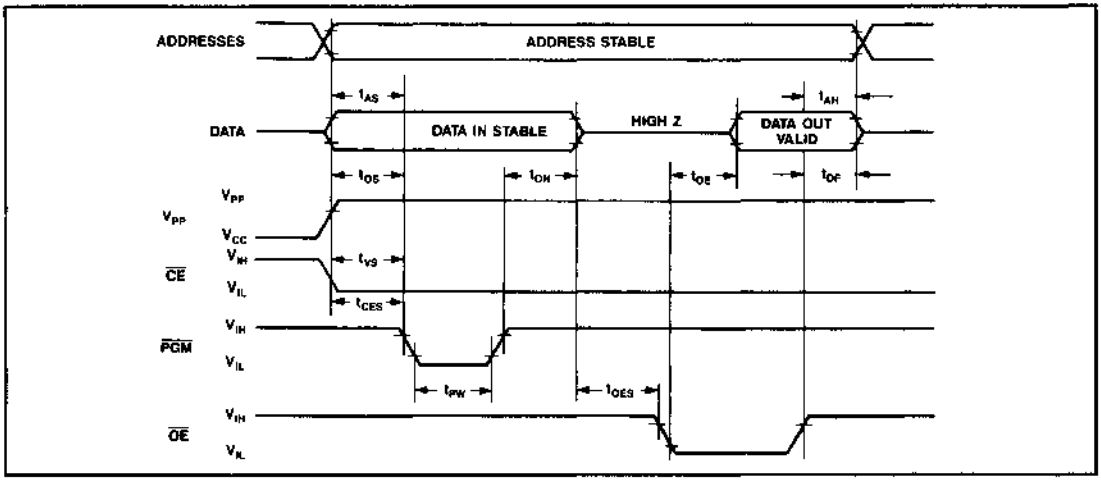
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES:
10. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
11. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
12. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

PROGRAMMING WAVEFORM



2 Meg (128K x 16) CMOS EPROM

KEY FEATURES

- **Ultra-High Performance**
  - 120 ns
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 40 Pin Dip Package
  - 44 Pin Chip Carrier

GENERAL DESCRIPTION

The WS27C220L is an ultra-high performance, 2,097,152-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128K-words of 16 bits each. The 120 ns access time of the WS27C220L enables it to operate in high performance systems. The "Don't Care" feature during read operations enables memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 12 MHz 80386 and 16 MHz 68020 require 120 ns memory access times to operate at or near full speed. The WS27C220L enables such systems to incorporate operating systems and/or applications software into EPROM. This in turn enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS27C220L pin configuration was established to allow memory upgrades to 8M bits without hardware changes to the printed circuit board. Pins 1 and 39 are "don't care" during normal read operation. This enables higher order addresses to be connected to these pins (see DIP Pin Configurations). When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS27C220L is part of a high density EPROM family which spans densities from 64K to 4 Meg.

The WS27C220L is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	27C220L-12	27C220L-15	27C220L-17	27C220L-20
Address Access Time (Max)	120 ns	150 ns	170 ns	200 ns
Chip Select Time (Max)	120 ns	150 ns	170 ns	200 ns
Output Enable Time (Max)	35 ns	40 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +125°C
Voltages on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7V
ESD Protection ..... > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Comm'l	0° to +70°C	+5V	±5% or ±10%
Military	−55° to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

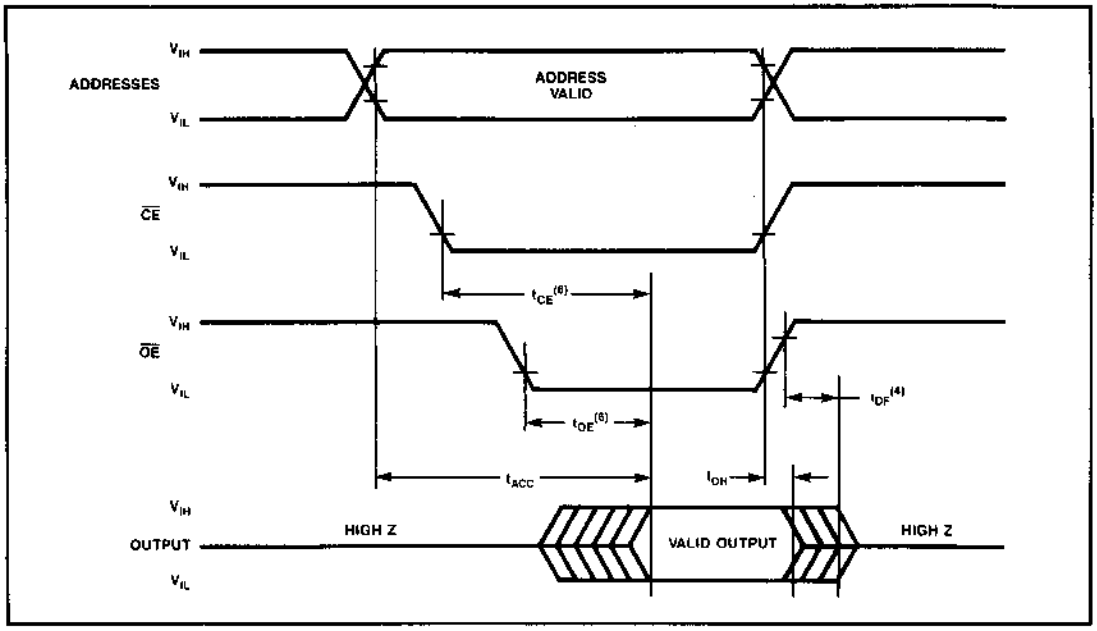
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}[3]	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}[1]	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$	F = 5 MHz		60	mA
			F = 8 MHz		70	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	-12		-15		-17		-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		120		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		170		200	
t_{OE}	$\overline{OE}$ to Output Delay		35		40		40		40	
t_{DF}[2]	Output Disable to Output Float		35		40		40		40	
t_{OH}[2]	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, $V_{IH} = V_{CC} \pm 0.3V$.

AC READ TIMING DIAGRAM

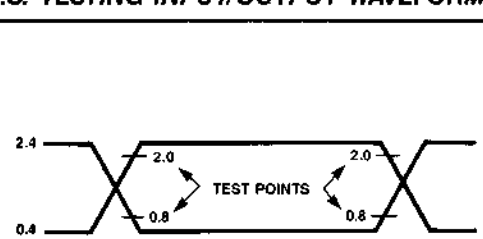


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

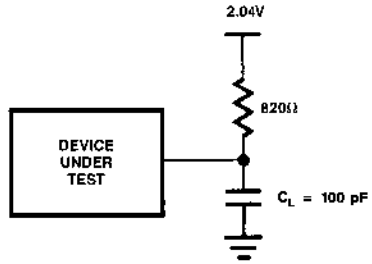
NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to $t_{CE}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}

A.C. TESTING INPUT/OUTPUT WAVEFORM



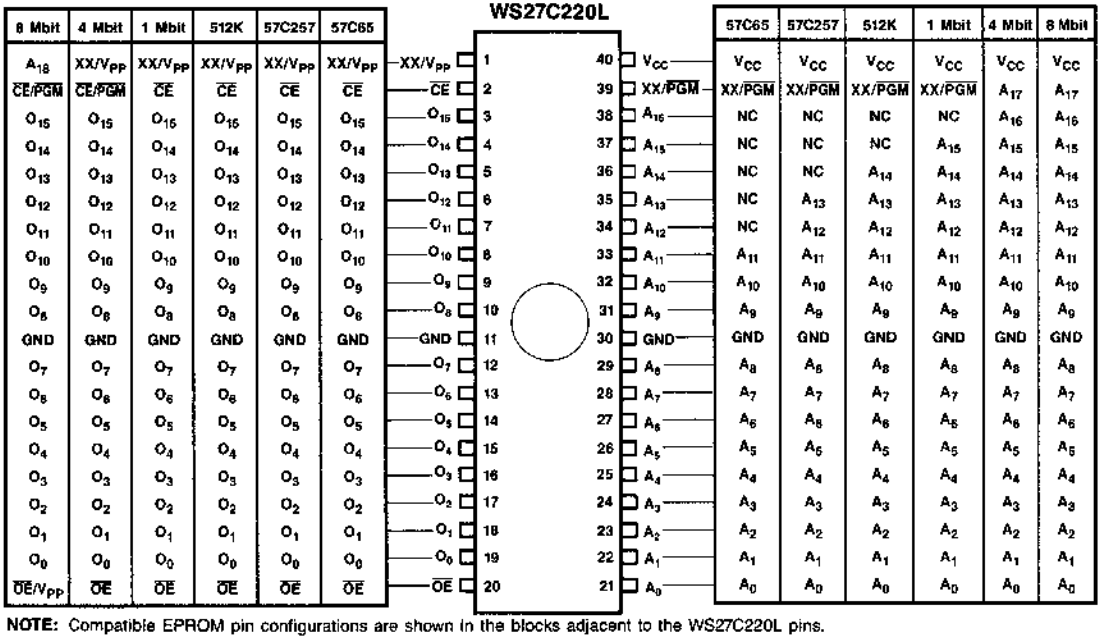
A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

DIP PIN CONFIGURATIONS

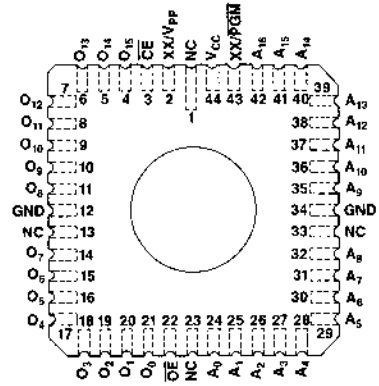


NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C220L pins.

PIN NAMES

A_0–A_{16}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
NC	No Connection
XX	Don't Care (During Read)
$\overline{PGM}$	Program

LCC PIN CONFIGURATION (TOP)



PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

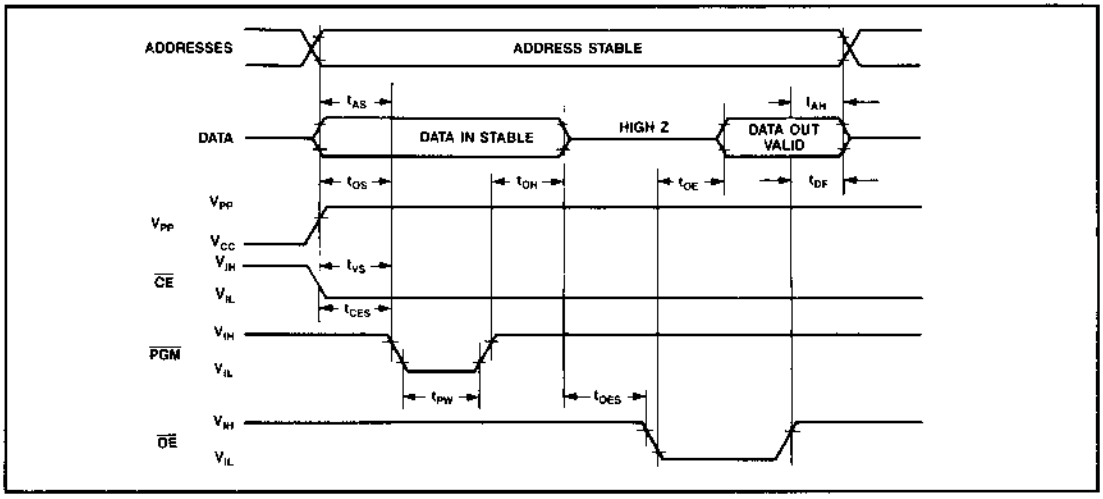
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES: 7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
9. During power up the $\overline{PGM}$ pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

PROGRAMMING WAVEFORM



MODE SELECTION

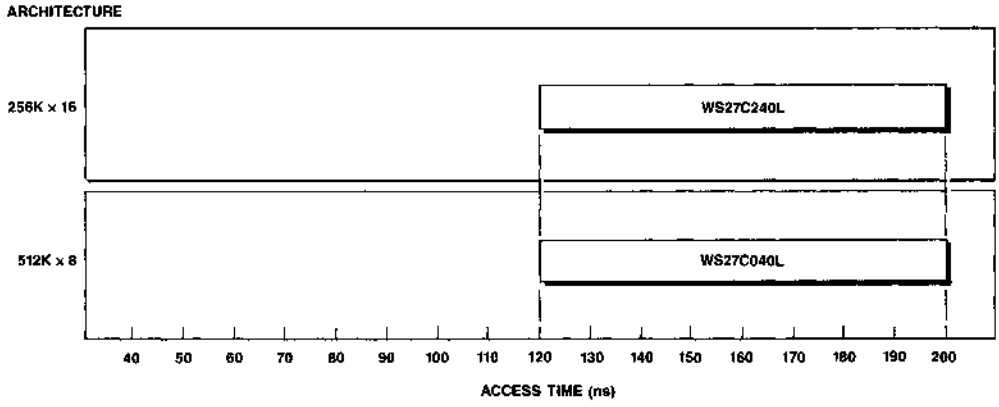
The modes of operation of the WS27C220L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and on A_9 for device signature.

Table 1. Modes Selection

MODE \ PINS		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X[10]	X	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	6.2V	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	6.2V	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	6.2V	High Z
Signature	Manufacturer[12]	V_{IL}	V_{IL}	X	V_H[11]	V_{IL}	X	5.0V	23 H
	Device[12]	V_{IL}	V_{IL}	X	V_H[11]	V_{IH}	X	5.0V	C9 H

NOTES: 10. X can be V_{IL} or V_{IH} 11. $V_H = V_{PP}$ 12. A_1–A_8, A_{10}–$A_{16} = V_{IL}$

4 MEG EPROM SELECTION GUIDE



512K × 8 CMOS EPROM

KEY FEATURES

- **High Performance CMOS**
  - 120 ns Access Time
- **Fast Programming**
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **Simplified Upgrade Path**
  - V_{PP} is a "Don't Care" During Normal Read Operation
- **Upward Compatible with JEDEC EPROM Configurations**
- **JEDEC Standard Pin Configuration**
  - 32 Pin Dip Package

GENERAL DESCRIPTION

The WS27C040L is a high performance, 4,194,304-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 512 K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature on V_{PP} during read operations allows memory expansions from 1M to 8M bits with no printed circuit board changes.

The WS27C040L can directly replace lower density 28-pin EPROMs by adding an A_{16} address line and V_{CC} jumper. During the normal read operation V_{PP} is in a "don't care" state which allows a higher order address, such as A_{19}, to be connected without affecting the normal read operation. This allows memory upgrade to 8M bits without hardware changes. The WS27C040L will also be offered in a 32-pin plastic Dip with the same upgrade path.

The WS27C040L provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 120-ns access time provides no-wait-state operation with high-performance CPUs such as the 16-MHz 80186, 16-MHz 68020, or 12-MHz 80386. The WS27C040L offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The WS27C040L is manufactured using WSI's advanced CMOS split gate EPROM technology.

PRODUCT SELECTION GUIDE

PARAMETER	WS27C040L-12	WS27C040L-15	WS27C040L-17	WS27C040L-20
Address Access Time (Max)	120 ns	150 ns	170 ns	200 ns
Chip Select Time (Max)	120 ns	150 ns	170 ns	200 ns
Output Enable Time (Max)	35 ns	40 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Commercial	0°C to +70°C	+5V	±5% or ±10%
Military	−55°C to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

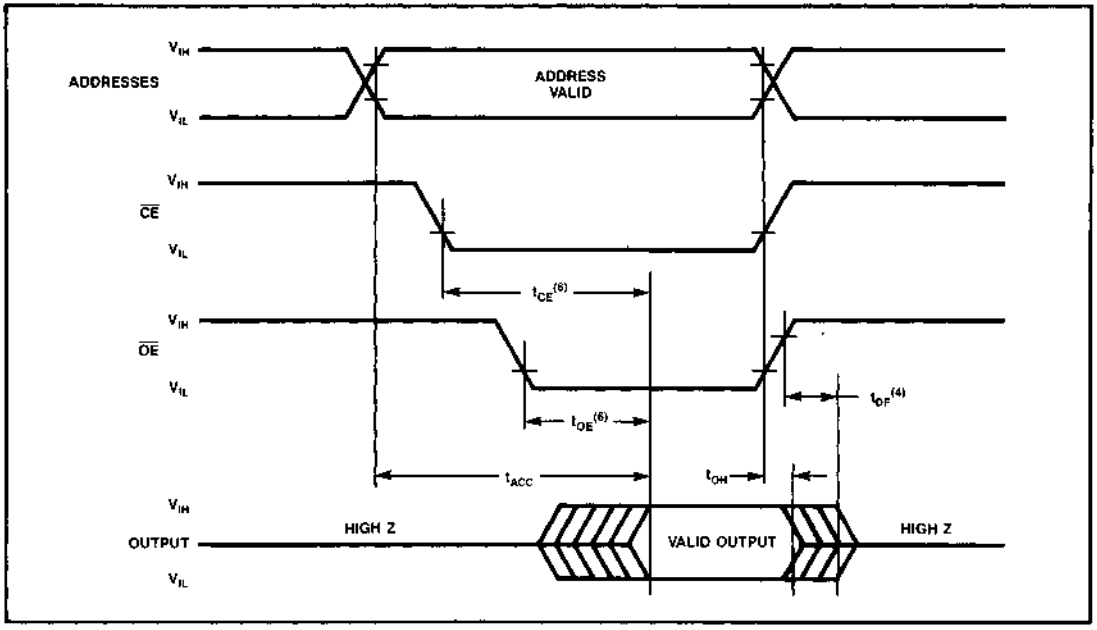
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}(3)	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}(1)	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$	F = 5 MHz		50	mA
			F = 8 MHz		60	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	CHARACTERISTICS	27C040L-12		27C040L-15		27C040L-17		27C040L-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		120		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		170		200	
t_{OE}	$\overline{OE}$ to Output Delay		35		40		40		40	
t_{DF}(2)	$\overline{OE}$ High to Output Float		35		40		40		40	
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, $V_{IH} = V_{CC} \pm 0.3V$.

A.C. WAVEFORMS

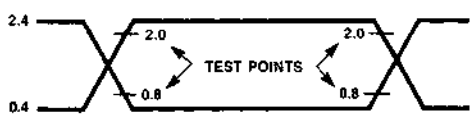


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

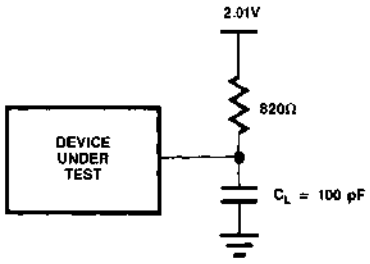
NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L includes Jig Capacitance

MODE SELECTION

The modes of operation of the WS27C040L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

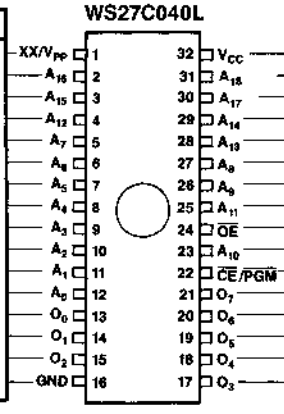
Table 1. Modes Selection

MODE \ PINS		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	X	X	V_{PP}[8]	6.2V	D_{IN}
Program Verify		X	V_{IL}	X	X	V_{PP}[8]	6.2V	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}[8]	5.0V	High Z
Signature	Manufacturer[9]	V_{IL}	V_{IL}	V_H[8]	V_{IL}	X	5.0V	23 H
	Device[9]	V_{IL}	V_{IL}	V_H[8]	V_{IH}	X	5.0V	D0 H

NOTES:
7. X can be V_{IL} or V_{IH}
8. $V_H = V_{PP} = 12.75 \pm 0.25V$
9. A_1–A_8, A_{10}–$A_{18} = V_{IL}$

DIP PIN CONFIGURATIONS

8 Mbit	2 Mbit	27C010L
A_{19}	XX/V_{PP}	XX/V_{PP}
A_{16}	A_{16}	A_{16}
A_{15}	A_{15}	A_{15}
A_{12}	A_{12}	A_{12}
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND



27C010L	2 Mbit	8 Mbit
V_{CC}	V_{CC}	V_{CC}
XX/$\overline{PGM}$	XX/$\overline{PGM}$	A_{18}
XX	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}
A_8	A_8	A_8
A_9	A_9	A_9
A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

NOTE: 10. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C040L pin.

PIN NAMES

A_0–A_{18}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

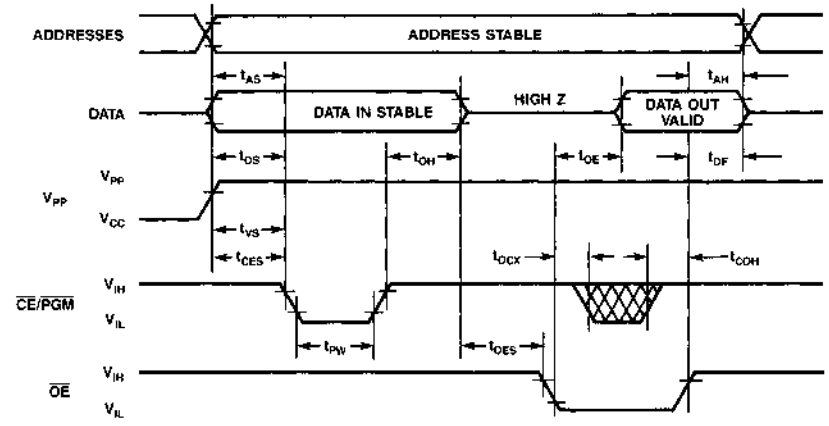
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES: 11. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
12. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.25V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.05		4	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

PROGRAMMING WAVEFORM



PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING RANGE		WSI MANUFACTURING PROCEDURE
				TEMPERATURE	V_{CC}	
WS27C040L-12D/5*	120	32 Pin CERDIP, 0.6"	D4	Comm'l	±5%	Standard
WS27C040L-15C	150	32 Pad CLLCC	C2	Comm'l	±10%	Standard
WS27C040L-15CM*	150	32 Pad CLLCC	C2	Military	±10%	Standard
WS27C040L-15CMB*	150	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C040L-15D	150	32 Pin CERDIP, 0.6"	D4	Comm'l	±10%	Standard
WS27C040L-15DMB*	150	32 Pin CERDIP, 0.6"	D4	Military	±10%	MIL-STD-883C
WS27C040L-17C	170	32 Pad CLLCC	C2	Comm'l	±10%	Standard
WS27C040L-17CM	170	32 Pad CLLCC	C2	Military	±10%	Standard
WS27C040L-17CMB	170	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C040L-17D	170	32 Pin CERDIP, 0.6"	D4	Comm'l	±10%	Standard
WS27C040L-17DMB	170	32 Pin CERDIP, 0.6"	D4	Military	±10%	MIL-STD-883C
WS27C040L-20C	200	32 Pad CLLCC	C2	Comm'l	±10%	Standard
WS27C040L-20CM	200	32 Pad CLLCC	C2	Military	±10%	Standard
WS27C040L-20CMB	200	32 Pad CLLCC	C2	Military	±10%	MIL-STD-883C
WS27C040L-20D	200	32 Pin CERDIP, 0.6"	D4	Comm'l	±10%	Standard
WS27C040L-20DMB	200	32 Pin CERDIP, 0.6"	D4	Military	±10%	MIL-STD-883C

*These products are Advance Information.

4 Meg (256K x 16) CMOS EPROM

KEY FEATURES

- **Ultra-High Performance**
  - 120 ns
- **Simplified Upgrade Path**
  - V_{PP} is a "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 40 Pin Dip Package
  - 44 Pin Chip Carrier

GENERAL DESCRIPTION

The WS27C240L is an ultra-high performance, 4,194,304-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 256K-words of 16 bits each. The 120 ns access time of the WS27C240L enables it to operate in high performance systems. The "Don't Care" feature during read operations enables memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 80386 and 68020 require sub-120 ns memory access times to operate at or near full speed. The WS27C240L enables such systems to incorporate operating systems and/or applications software into EPROM. This in turn enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS27C240L pin configuration was established to enable memory upgrades to 8M bits without hardware changes to the printed circuit board. Pin 1 is a "don't care" during normal read operation. This enables higher order addresses to be connected to this pin (see DIP Pin Configurations). When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS27C240L is part of a high density EPROM family which spans densities from 64K to 4 Meg.

The WS27C240L is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	27C240L-12	27C240L-15	27C240L-17	27C240L-20
Address Access Time (Max)	120 ns	150 ns	170 ns	200 ns
Chip Select Time (Max)	120 ns	150 ns	170 ns	200 ns
Output Enable Time (Max)	35 ns	40 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Comm'l	0° to +70°C	+5V	±5% or ±10%
Industrial	−40° to +85°C	+5V	±10%
Military	−55° to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

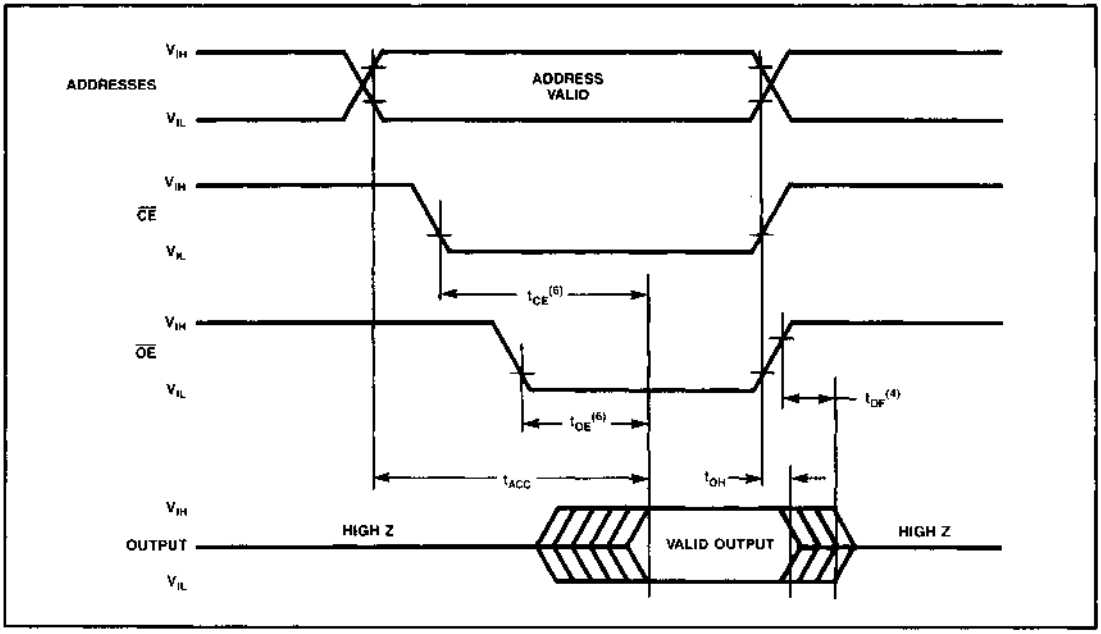
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}[3]	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}[1]	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	F = 5 MHz		60	mA
			F = 8 MHz		70	
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	27C240L-12		27C240L-15		27C240L-17		27C240L-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		120		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		170		200	
t_{OE}	$\overline{OE}$ to Output Delay		35		40		40		40	
t_{DF}[2]	Output Disable to Output Float		35		40		40		40	
t_{OH}[2]	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First[2]	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ± 0.3V.

AC READ TIMING DIAGRAM

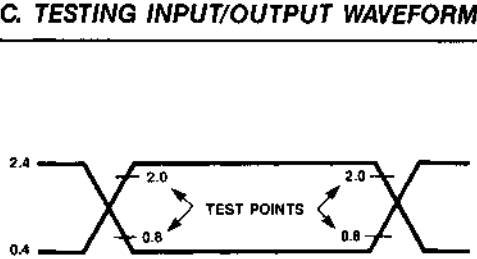


CAPACITANCE[4] T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP[5]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

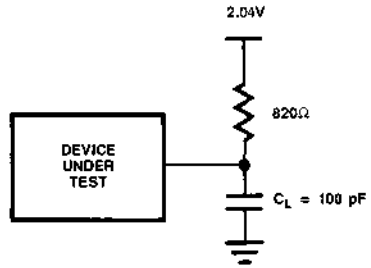
NOTES:
4. This parameter is only sampled and is not 100% tested
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of CE without impact on t_{CE}.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

DIP PIN CONFIGURATIONS

8 Mbit	2 Mbit	1 Mbit	512K	57C257	57C65				57C65	57C257	512K	1 Mbit	2 Mbit	8 Mbit
A_{18}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	1	40	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{CE}$/$\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/$\overline{PGM}$	2	39	A_{17}	XX/$\overline{PGM}$	XX/$\overline{PGM}$	XX/$\overline{PGM}$	XX/$\overline{PGM}$	XX/$\overline{PGM}$	A_{17}
O_{15}	O_{15}	O_{15}	O_{15}	O_{15}	O_{15}	O_{15}	3	38	A_{16}	NC	NC	NC	NC	A_{16}	A_{16}
O_{14}	O_{14}	O_{14}	O_{14}	O_{14}	O_{14}	O_{14}	4	37	A_{15}	NC	NC	NC	A_{15}	A_{15}	A_{15}
O_{13}	O_{13}	O_{13}	O_{13}	O_{13}	O_{13}	O_{13}	5	36	A_{14}	NC	NC	A_{14}	A_{14}	A_{14}	A_{14}
O_{12}	O_{12}	O_{12}	O_{12}	O_{12}	O_{12}	O_{12}	6	35	A_{13}	NC	A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
O_{11}	O_{11}	O_{11}	O_{11}	O_{11}	O_{11}	O_{11}	7	34	A_{12}	NC	A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
O_{10}	O_{10}	O_{10}	O_{10}	O_{10}	O_{10}	O_{10}	8	33	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
O_9	O_9	O_9	O_9	O_9	O_9	O_9	9	32	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
O_8	O_8	O_8	O_8	O_8	O_8	O_8	10	31	A_9	A_9	A_9	A_9	A_9	A_9	A_9
GND	GND	GND	GND	GND	GND	GND	11	30	GND	GND	GND	GND	GND	GND	GND
O_7	O_7	O_7	O_7	O_7	O_7	O_7	12	29	A_8	A_8	A_8	A_8	A_8	A_8	A_8
O_6	O_6	O_6	O_6	O_6	O_6	O_6	13	28	A_7	A_7	A_7	A_7	A_7	A_7	A_7
O_5	O_5	O_5	O_5	O_5	O_5	O_5	14	27	A_6	A_6	A_6	A_6	A_6	A_6	A_6
O_4	O_4	O_4	O_4	O_4	O_4	O_4	15	26	A_5	A_5	A_5	A_5	A_5	A_5	A_5
O_3	O_3	O_3	O_3	O_3	O_3	O_3	16	25	A_4	A_4	A_4	A_4	A_4	A_4	A_4
O_2	O_2	O_2	O_2	O_2	O_2	O_2	17	24	A_3	A_3	A_3	A_3	A_3	A_3	A_3
O_1	O_1	O_1	O_1	O_1	O_1	O_1	18	23	A_2	A_2	A_2	A_2	A_2	A_2	A_2
O_0	O_0	O_0	O_0	O_0	O_0	O_0	19	22	A_1	A_1	A_1	A_1	A_1	A_1	A_1
$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	20	21	A_0	A_0	A_0	A_0	A_0	A_0	A_0

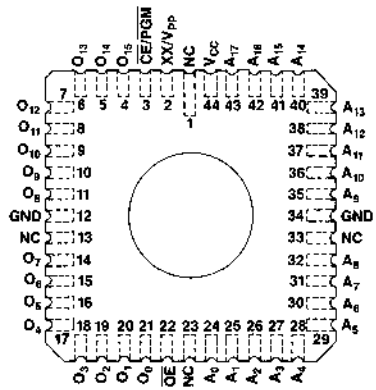
WS27C240L

NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C240L pins.

PIN NAMES

A_0–A_{17}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
NC	No Connection
XX	Don't Care (During Read)
$\overline{PGM}$	Program

LCC PIN CONFIGURATION (TOP)



PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

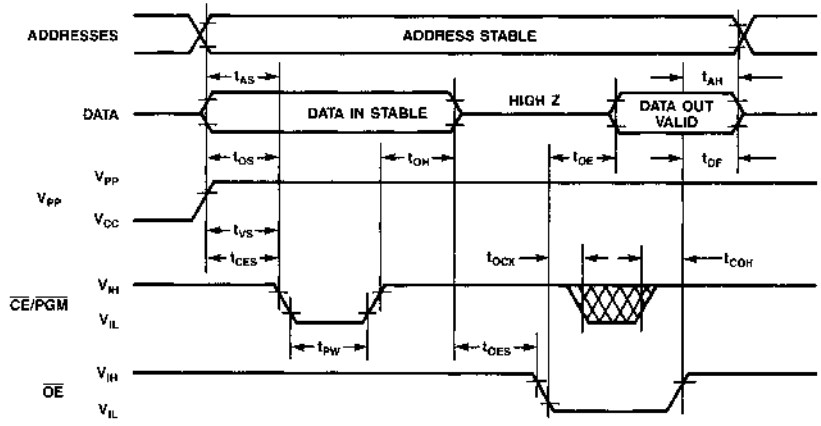
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}/\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES: 7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}/\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.05		4	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

PROGRAMMING WAVEFORM



MODE SELECTION

The modes of operation of the WS27C240L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and on A_9 for device signature.

Table 1. Modes Selection

MODE \ PINS		$\overline{CE}/\overline{PGM}$	$\overline{OE}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	X	X	V_{PP}	6.2V	D_{IN}
Program Verify		X	V_{IL}	X	X	V_{PP}	6.2V	D_{OUT}
Program Inhibit		V_{IH}	V_{IH}	X	X	V_{PP}	6.2V	High Z
Signature	Manufacturer[11]	V_{IL}	V_{IL}	V_H[10]	V_{IL}	X	5.0V	23 H
	Device[11]	V_{IL}	V_{IL}	V_H[10]	V_{IH}	X	5.0V	C9 H

NOTES: 9. X can be V_{IL} or V_{IH} 10. $V_H = V_{PP}$ 11. A_1–A_8, A_{10}–$A_{17} = V_{IL}$

WAFERSCALE INTEGRATION, INC.

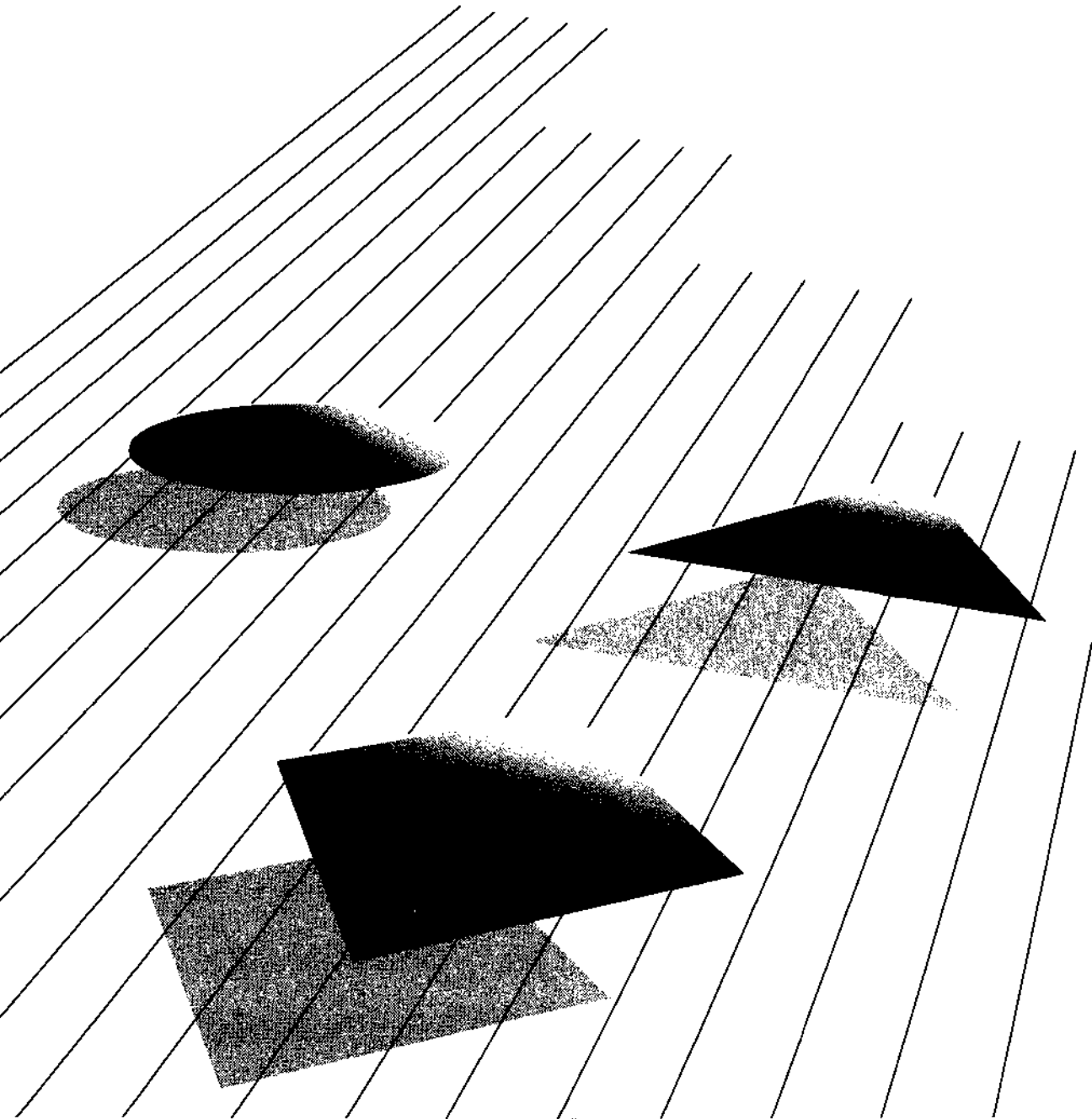
SECTION INDEX

PROGRAMMABLE SYSTEM™ DEVICES (PSD)

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 800-562-6363.

WAFERSCALE INTEGRATION, INC.

Programmable System™ Devices



WAFERSCALE INTEGRATION, INC.

Introduction to Programmable System™ Devices (PSD)

Programmable System Devices, or PSDs, are user-configurable system level building blocks on-a-chip enabling quick implementation of application specific controllers and peripherals.

WSI PSDs are ideal for designers who require fast time-to-market, low risk, greater system integration and lower power consumption. PSDs enable designers to configure their microcontroller/peripheral to meet exact design requirements. WSI's PSDs are unique in that they are the only VLSI devices available today that provides a *user-configurable off-the-shelf solution at the system level.*

The user-configurability of PSDs enables them to be used in many different applications, including:

- Computers (Workstations and PCs) — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- Telecommunications — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- Industrial — Robotics, Power Line Access, Power Line Monitor
- Medical Instrumentation — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- Military — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

PSDs are available in a variety of space saving surface mount and through-hole package configurations for commercial, industrial, and military applications. WSI offers windowed package options for prototyping and low cost OTP (one-time programmable) packages for high volume applications. PSDs utilize WSI's proprietary split-gate CMOS EPROM technology for low power consumption.

There are currently four PSD family devices in production. These include the PAC1000, MAP168, PSD301, and SAM448.

- The PAC1000 is a user-configurable microcontroller. It may be used as a stand-alone microcontroller or as a peripheral to microprocessors. It is ideal for embedded control applications, including graphics, local area network, and disk drive control in both military and commercial applications.
- The MAP168 is a user-configurable peripheral. It is used in DSP applications including modems, motor control and medical instrumentation. The MAP168 is ideal for DSP based applications where fast time-to-market, small form factor and low power consumption are essential. When combined together in an 8- or 16-bit system, virtually any DSP chip (TMS320 series, etc.) and the MAP168 work together to create a very powerful 2-piece chip-set. This combination provides essentially all of the required control and peripheral element of a DSP system.
- The PSD301 is a user-configurable peripheral for microcontroller applications including disk drives, low cost modems, and mobile phones. The PSD301 is ideal for microcontroller based applications where fast time-to-market, small form factor and low power consumption are essential. When combined together in an 8- or 16-bit system, virtually any microcontroller (8051, 8096, 16000, etc.) and the PSD301 work together to create a very powerful 2-piece chip-set. This implementation provides the required control and peripheral element of a microcontroller based system peripheral with no external "glue" logic required.
- The SAM448 is a user-configurable sequencer for state machine and bus interface applications. Its flexible I/O and architecture make it ideal for use in interfacing to both existing bus architectures (AT, VME, MCA-bus), and evolving bus standards (EISA, NuBUS).

Application specific features can be easily programmed into the PSD EPROM array for quick design implementation. Unlike the current generation of programmable gate arrays, which require the use of unpredictable, and often time unavailable routing resources, all PSD logic is fully connected internally. This means that all timing is predictable ahead of design implementation, and routing is assured. This greatly simplifies and reduces the design implementation and simulation process, and provides designers with a significantly more reliable, lower risk path to market. WSI PSDs also eliminate the NRE, turn-around-time, and risks associated with gate arrays and other ASIC solutions.

As product life cycles continue to shrink, designers can win the race from idea to marketable product with WSI PSDs. PSDs are quickly configured and programmed by the designer by using low cost, easy-to-use WSI PC-based development tools. The user-friendly menu-driven software includes high level design entry, simulation and programming packages for rapid system development.

WSI supports its PSD product family with an applications hotline and bulletin board, as well as highly trained, technical Field Applications Engineers. As standard products, WSI PSDs are available from WSI's franchised world-wide distribution network.

WAFERSCALE INTEGRATION, INC.

Programmable System™ Device

MAP168/PSD301 Introduction

User-Configurable Peripheral with Memory

Overview

In 1988 WSI introduced a new concept in programmable VLSI: the Programmable System™ Device (PSD). The PSD is defined as a family of *User-configurable system level building blocks on-a-chip enabling quick implementation of application specific controllers and peripherals.* The first generation PSD series includes the MAP168, a User-Configurable Peripheral with Memory; the SAM448, a User-Configurable Microsequencer; and the PAC1000, a User-Configurable Microcontroller.

The MAP168 is a high-performance, user-configurable peripheral with memory. It is used in DSP applications including modems, motor control and medical instrumentation. The MAP168 is ideal for DSP based applications where fast time-to-market, small form factor and low power consumption are essential. When combined together in an 8- or 16-bit system, virtually any DSP chip (TMS320 series, etc.) and the MAP168 work together to create a very powerful 2-piece chip-set. This implementation provides the core of the required control and peripheral elements of a DSP system.

The MAP168 contains three elements normally associated with discrete solutions to system memory requirements. It incorporates EPROM and SRAM plus a Programmable Address Decoder (PAD), all on the same die. The MAP168 is ideal for the systems designer who wishes to reduce the board space of his final design. By using the MAP168 in a system, five or six EPROM, SRAM and decode logic chips may be reduced into a single 44 pin PLDCC, CLDCC or PGA package.

The second generation PSD301 is a user-configurable peripheral for microcontroller applications including disk drives, low cost modems, and mobile phones. The PSD301 is ideal for microcontroller based applications where fast time-to-market, small form factor and low power consumption are essential. When combined together in an 8- or 16-bit system, virtually any microcontroller (8051, 8096, 16000, etc.) and the PSD301 work together to create a very powerful 2-piece chip-set. Together, this implementation provides all the required control and peripheral elements of a microcontroller based system peripheral with no external "glue" logic required.

4

Architecture

The MAP168 and PSD301 products incorporate the flexibility of using discrete memory addressing and decoding. With the support of WSI's user friendly PSD software called MAPLE, designers may configure their MAP168/PSD301 subsystems for 8 or 16 bit data paths. If the host system uses an 8051 microcontroller, the MAP168/PSD301 can be programmed with an eight bit data path. A sixteen bit data path can be programmed for microcontrollers like Intel's 80196. The depth of the memory organization will be modified accordingly to accept the different data path widths. The low cost MAPLE software package will handle the data path width adjustment automatically. The user can select either 16K bytes of EPROM and 4K bytes of SRAM or 8K words of EPROM and 2K words of SRAM. The flexibility of the MAP168/PSD301 products enables two devices to be cascaded in width. It is possible to double the memory size of a sixteen bit system by using two MAP168 products in parallel but programmed in a byte-wide configuration. For example, with two MAP168 devices, 16K words of EPROM and 4K words of SRAM may be organized as upper and lower data bytes of a 16 bit word. Alternately, two MAP168 chips may expand the system memory vertically as two word organized memory devices. A block diagram of the MAP168 is shown in Figure 1.

An important feature of the MAP168/PSD301 products is their ability to incorporate the memory address decoding on-chip. One

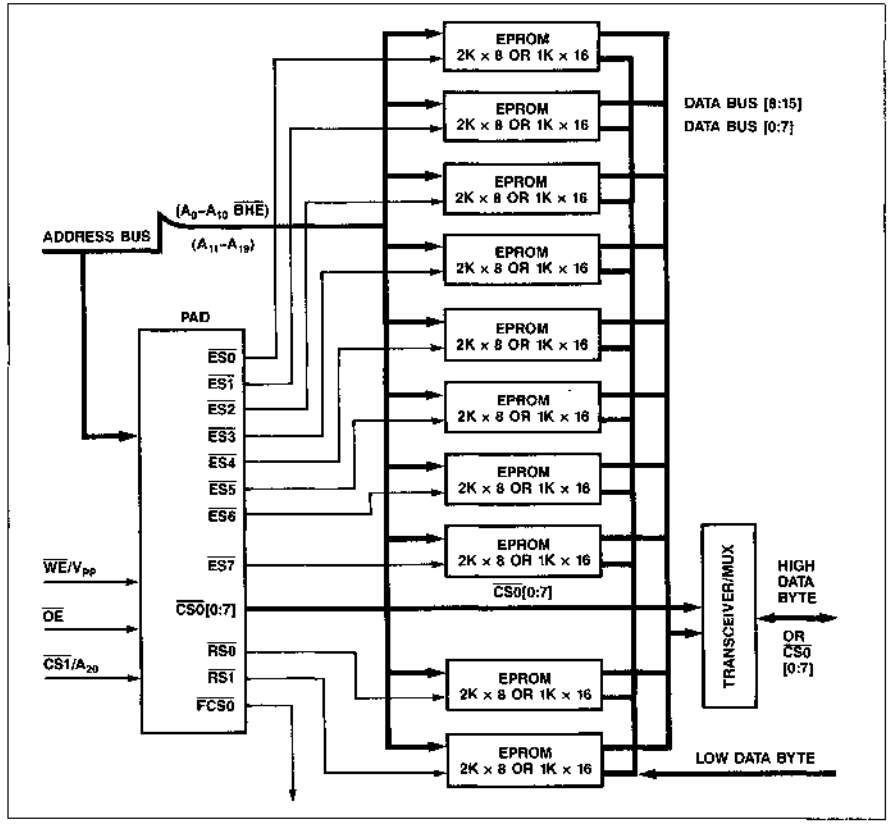
Architecture (Cont.)

MAP168 memory peripheral can reside with other MAP168 devices in the same memory addressing scheme, with the on-chip decoder allocating the memory blocks to different non-conflicting segments of the entire memory area. The decoding function is achieved by an on-chip feature called a Programmable Address Decoder (PAD), which is similar to a single fuse array programmable logic device supporting one product term (AND gate) per output in the MAP168 and four product terms per output in the PSD301.

In the MAP168, eighteen standard chip select outputs from the PAD are available with one fast chip select output generally used to select other external high speed memory devices. The chip select lines may be subdivided into $\overline{ES0}$–$\overline{ES7}$, active low internal EPROM chip selects, and two internal RAM chip selects $\overline{RS0}$ and $\overline{RS1}$. In byte-wide applications, eight chip select outputs drive external pins $\overline{CS0}$–$\overline{CS7}$. These can be used as external chip selects for other MAP168 devices or system memory. These outputs are not available for word-wide MAP168 configurations because the $\overline{CS0}$–$\overline{CS7}$ output pins carry the higher order data byte. Only $\overline{FCS0}$ is available for external chip selection.

Figure 1 shows the organization of the EPROM and SRAM in relation to the PAD, for the MAP168 device.

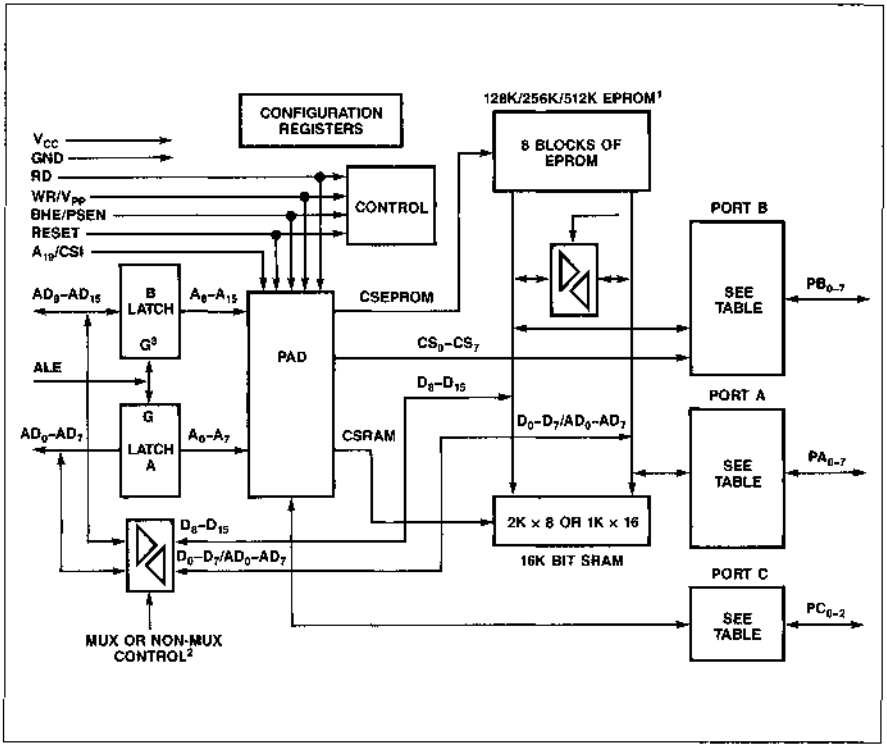
Figure 1. MAP168 Memory Architecture



Important Features:

- 40 ns EPROM/SRAM Access Time.
- Byte or Word Operation, Mappable into 1M Word or 2M Byte Address Space
- 22 ns Chip-Select 8 Outputs, 17 ns Fast Chip Select Output.
- 128K EPROM Bits, 32K SRAM Bits, On-Chip Programmable Decoder, Security Bit.

Figure 2. PSD301 Family Architecture



	By 8 Configuration		By 16 Configuration		
	Port A	Port B	Port A	Port B	Port C
Non-MUX Address Data[5]	D_0–D_7	CS_0–CS_7 or PB_0–PB_7	D_0–D_7[4]	D_8–D_{15}	CS_8–CS_{10}[6] A_{16}–A_{18}
MUX Address Data	A_0–A_7[4] PA_0–PA_7 AD_0–AD_7	CS_0–CS_7[4] PB_0–PB_7	A_0–A_7[4] PA_0–PA_7 AD_0–AD_7	CS_0–CS_7 PB_0–PB_7	

NOTES:
1. Three MAP300 EPROM densities.
2. Internal signal can be set during programming.
3. Latch B can be set to be transparent (not dependent on ALE)
4. Each I/O pin can be individually set to perform one of the two functions.
5. The non-MUX configuration is compatible to MAP168 pinout
6. Port C is independent of any configuration and can be chip select out or address in.

Software Support

The object code generated for the support microprocessor/microcontroller is generated by an assembler. This code, when generated as an Intel MCS file, may be easily programmed into the EPROM section of the MAP168/PSD301 device because the MAPLE software has been designed to accept this standard format.

The programmable address decoder is used to define the mapping of the various EPROM and SRAM memory blocks. This mapping is achieved by the designer in the MAPLE environment. The software provides a safeguard that prevents the designer from inadvertently overlapping the address selection. After selecting the memory block assignments, the MAP168/PSD301 device may be programmed by the WSI MagicPro™ memory and PSD programmer.

WAFERSCALE INTEGRATION, INC.

Programmable System™ Device

MAP168

User-Configurable Peripheral with Memory

Features

- First-generation Programmable System Device (PSD)
  - User-Configurable Peripheral with Memory
  - 16Kx8 EPROM
  - 4Kx8 SRAM
  - Programmable address decoder
- Byte or Word Memory Configurations
  - 16Kx8 or 8Kx16 EPROM
  - 4Kx8 or 2Kx16 SRAM
  - 2Mbyte or 1 Mword address range
- High-Speed Operation
  - 40-nsec memory access
  - 17-nsec fast chip select output
- External Chip Select Outputs
  - 8 external chip selects
  - 1 fast chip-select output
- Programmable Security
  - Protects memory map
  - Protects program code
- Programming Support Tools
  - PSD integrated software environment
  - PC-XT/AT/PS2 platform support
  - MAPLE location entry Software
  - MAPPRO device programming Software
  - MagicPro device programmer (PC-XT, AT)
- Military and Commercial Specifications
  - 44-pin Ceramic Leaded Chip Carrier package
  - 44-pin Plastic Leaded Chip Carrier package
  - 44-pad Ceramic Leadless Chip Carrier package
  - 44-pin Ceramic Pin Grid Array package

4

General Description

In 1988 WSI introduced a new concept in programmable VLSI, Programmable System Devices (PSD). The PSD family consists of user-configurable system-level building blocks on-a-chip, enabling quick implementation of application-specific controllers and peripherals. The first generation PSD series includes the MAP168 User-Configurable Peripheral with Memory; the SAM448, a User-Configurable Microsequencer; and the PAC1000, a User-Configurable Microcontroller.

The MAP168 is the first of WSI's Programmable System Devices (PSD) product line. The device integrates high performance, user-configurable blocks of EPROM, SRAM, and logic in a single circuit. The major functional blocks include a Programmable Address Decoder (PAD), 16K bytes of high speed EPROM, and 4K bytes of high speed SRAM. A block diagram is given in Figure 1.

The MAP168 device is a complete memory subsystem that can be mapped anywhere in a 2M-byte address space of a microprocessor or microcontroller system. The EPROM and SRAM memory blocks can be user-configured in either byte-wide or word-wide organizations. The MAP168 device significantly reduces the board space and power necessary to implement memory subsystems, increases system performance, and provides for secure data or program storage.

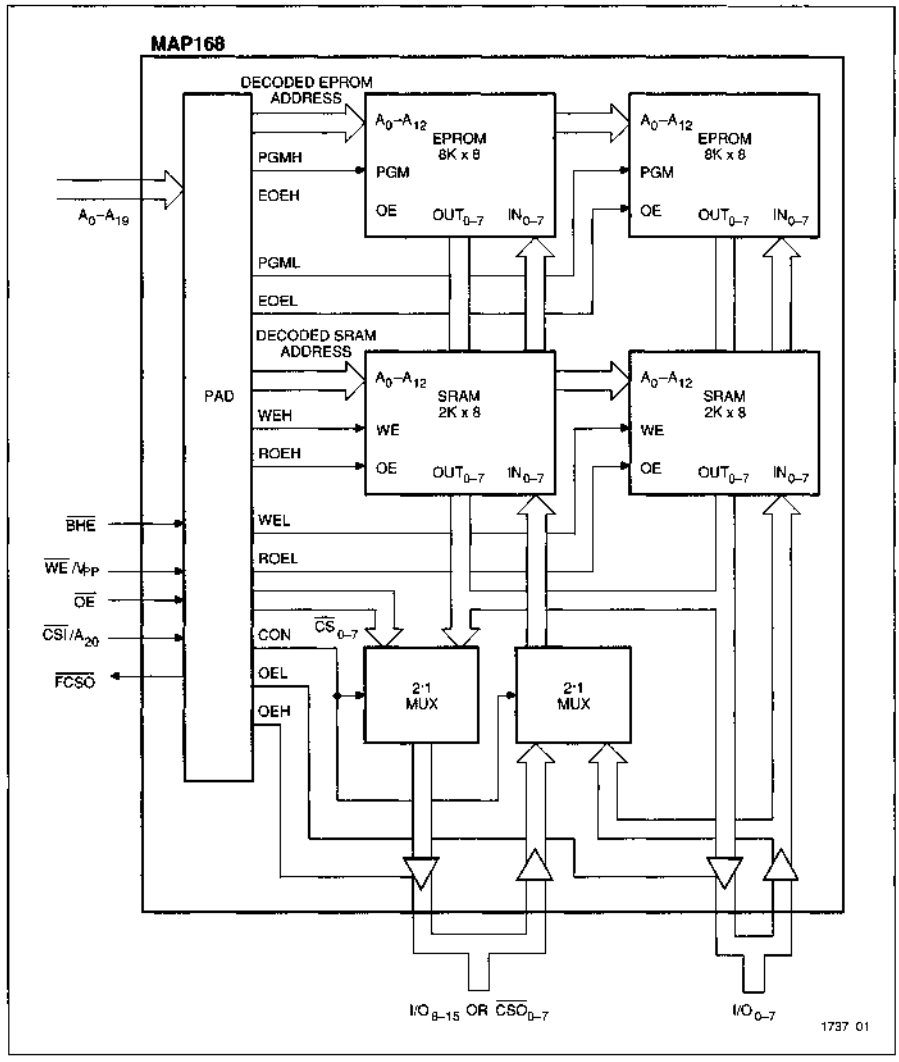
The device's high level of integration and flexibility make it ideal for high-speed microprocessors, microcontrollers, and Digital Signal Processors like the TMS320XX family. The EPROM can be configured either as 16Kx8 or 8Kx16. The SRAM can be configured either as 4Kx8 or 2Kx16. Individual memory blocks of 2Kx8 or 1Kx16 can be selectively mapped anywhere in the address space. Since the Chip Select Input ($\overline{CSI}$) can be programmed as A20, the highest-order address bit, the device's address range can extend from 1M byte with $\overline{CSI}$ to 2M byte without $\overline{CSI}$.

For 16-bit microprocessors capable of byte operations, the MAP168 device provides a Byte High Enable input for accessing bytes on any address boundary.

Pinout is compatible with the JEDEC WS27C257 256K high-speed EPROM. This pinout provides for memory expansion with future WSI EPROM and PSD products.

The device's PAD and EPROM memory are

Figure 1.
Block Diagram



General Description (Con't)

programmed using the same WSI MagicPro programmer used to program other WSI devices. Two software packages, MAPLE Location Entry and MAPPRO Device Programming Software are available in the menu-driven WISPER software environment on an IBM® PC XT/AT or 100% compatible platform.

For additional information on the MAP168 device, refer to *Application Note No. 002, Introduction to the MAP168 User-Configurable Peripheral with Memory*. For additional information on development and programming software for the MAP168 device, refer to the *MAP168 User-Configurable Peripheral with Memory Software User's Manual*.

Functional Description

The user-configurable architecture of the MAP168 consists of an EPROM memory block, an SRAM memory block, and a fast Programmable Address Decoder (PAD) that can be configured to select 2K-byte memory blocks anywhere in a 2M-byte address range. The device can be programmed to operate with memory configured either in a byte or word organization (bytes can be addressed in word mode). A programmable security bit prevents access to the PAD address-decode configuration table.

Table 1. Pin Description

Signal	I/O	Description
A_{0-19}	I	*Address Lines.* For access to EPROM or SRAM.
$\overline{FCSO}$	O	*Fast Chip-Select Output (active low).* Used by the Programmable Address Decoder (PAD).
$\overline{BHE}$	I	*Byte High Enable (active low).* Selects the high-order byte when writing to SRAM.
$\overline{WE}/V_{pp}$	I	*Write Enable (active low) or Programming Voltage.* In normal mode, this pin causes data on the I/O pins to be written into SRAM. In programming mode, the pin supplies the programming voltage, V_{pp}.
$\overline{OE}$	I	*Output Enable (active low).* Enable the I/O pins to drive the external bus.
$\overline{CSI}/A_{20}$	I	*Chip Select Input (active low) or High-Order Address.* This pin can be programmed as the bus-access chip select or as an additional high-order address bit (A_{20}).
I/O_{0-7}	I/O	*Low-Order Byte of EPROM or SRAM.*
I/O_{8-15}, $\overline{CSO}_{0-7}$	I/O	*High-Order Byte or Chip-Select Outputs.* In word mode, these pins serve as the high-order byte (I/O_{8-15}) of EPROM or SRAM. In byte mode, the bits serve as Chip-Select Out signals ($\overline{CSO}_{0-7}$) for the Programmable Address Decoder (PAD).

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Programmable Address Decoder

The MAP168 device has a minimum of 20 address inputs A_0–A_{19} allowing the EPROM and SRAM memory blocks to reside anywhere in a 1M-byte address space. If the $\overline{CSI}/A_{20}$ input is user-configured as an address line, the maximum addressable space increases to 2M bytes, as shown in the Configurations table.

The 16K bytes of EPROM and 4K bytes of SRAM, can be configured into eight independent 2K-byte blocks and two 2K-byte blocks respectively, as shown in the Memory Architecture figure. The PAD is a user-configurable address decoder that compares input addresses to the 2K-byte address range selected for each of the eight EPROM blocks and two SRAM blocks. When the input address A_0–A_{20} is detected to be within one of the EPROM or SRAM address ranges, the PAD enables an internal chip select (ES_0–ES_7 or RS_0–RS_1) to the selected block. If no block is selected, both the EPROM and SRAM memories remain in a power-down mode and the outputs are disabled allowing other devices to drive the data bus. The SRAM retains its data in the power-down mode. The 2K-byte address ranges for any of the eight EPROM or two SRAM blocks may not overlap.

The PAD can also be user-configured to generate up to eight external chip selects, $\overline{CS_0}$–$\overline{CS_7}$. These outputs can be used to decode the input address lines A_0–A_{20} and to select other devices in the system. The outputs $\overline{CS_0}$–$\overline{CS_7}$ are available on the eight higher-order I/O_8–I/O_{15} lines but only when the MAP168 device is configured in the byte mode; the lines are not available as chip-select outputs when the device is configured in the word mode.

The $\overline{CSI}/A_{20}$ input is user-configurable as the most-significant address line or as an active-low chip enable. Its function is programmed as part of the PAD programming cycle.

The PAD also provides $\overline{FSCO}$, a single, fast chip-select output configurable by the user for any address. It can overlap with any of the internal EPROM, SRAM or external $\overline{CSO}$ addresses.

Memory Subsystem

EPROM Memory

The memory configuration of the MAP168 device includes 128K bits of WSI's patented high-speed, split-gate, UV-erasable EPROM. The EPROM is configured in byte mode as 16Kx8 and in word mode as 8Kx16. The memory is organized as eight 2Kx8 or 1Kx16 blocks, as shown in the Block Diagram figure. Each block has a separate and independent address range that cannot overlap. Each block is individually selected by one of the ES_0–ES_7 internal chip selects generated by the PAD when an input address is detected within its designated address range, as shown in the Memory Architecture figure. If not selected, each block of EPROM remains in a power-down mode.

For programming, the EPROM memory requires the $\overline{WE}/V_{PP}$ input to maintain the programming voltage V_{PP}.

SRAM Memory

The device also includes 32K bits of high-speed SRAM. The SRAM is configured in byte mode as 4Kx8 and in word mode as 2Kx16. The memory is organized as two 2Kx8 or one 2Kx16 block(s), each with a separate and independent address range that cannot overlap. Each SRAM block is individually selected by one of the RS_0–RS_1, shown in the Memory Architecture figure, when an input address is detected by the PAD within its designated address range. When not selected, each of the SRAM memory blocks remains in a power down mode but does retain all data stored.

Data can be written into the SRAM only when the $\overline{WE}/V_{PP}$ input is active low.

Memory Subsystem EPROM Memory (Con't)

Byte/Word Mode

The PAD can be programmed to configure the MAP168 device for either a byte or word memory architecture. This allows the device to be used conveniently with either 8-bit or 16-bit microcontrollers, microprocessors or digital signal processor (DSP) systems. See the Configurations table.

In byte mode, the EPROM is organized as 16Kx8 and the SRAM as 4Kx8. The outputs of both are tied to the eight low-order input/output lines I/O_0–I/O_7 and enabled onto the output bus when the $\overline{OE}$ input is low.

Only when configured in byte mode are the eight external chip selects provided by the PAD available on the eight high-order input/output lines I/O_8–I/O_{15} and enabled onto the output bus when the $\overline{OE}$ input is low.

In word mode, the EPROM is organized as 8Kx16 and the SRAM as 2Kx16. The outputs of both are tied to the 16 input/output lines I/O_0–I/O_{15} and enabled onto the bus when $\overline{OE}$ is low.

In word mode, the $\overline{BHE}$ input along with address input A0 allows the eight bits of any 16-bit word on an even or odd boundary to be selected as shown in the High-Low Byte Selection table. This is a useful feature for 16-bit processors that are not restricted to reading or writing memory only on even-word address boundaries.

Mode Selection

The device's operational mode is controlled by three inputs, $\overline{CS}$I, $\overline{OE}$, and $\overline{WE}/V_{PP}$. There are ten separate modes of operation, all of which are shown the Mode Selection table.

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Table 2. Configurations

	x8 Configuration		x16 Configuration	
	$\overline{CS}$I	A_{20}	$\overline{CS}$I	A_{20}
Address Space words	1M bytes	2M bytes	512K words	1M
Block Size words	2K bytes	2K bytes	1K words	1K
Addressable Blocks	512	1024	512	1024
EPROM Blocks	8	8	8	8
SRAM Blocks	2	2	2	2
Chip-Select Outputs	9	9	1	1
EPROM Configuration	16Kx8	16Kx8	8Kx16	8Kx16
SRAM Configuration	4Kx8	4Kx8	2Kx16	2Kx16
I/O Pins	8	8	16	16
Low-power Standby	yes	no	yes	no
Protected Mode	yes	yes	yes	yes
Byte Operations	yes	yes	yes	yes

Table 3. Mode Selection

Mode/Pin	$\overline{CS}$	$\overline{OE}$	$\overline{WE}/V_{pp}$	Address	x16 (I/O_{8-15}) x8 (I/O_{0-7})	x16 ($\overline{FCSO}$) x8 $\overline{FCSO}$, $\overline{CSO}_{6-7}$
Read EPROM/SRAM	V_{IL}	V_{IL}	V_{IH}	EPROM/SRAM Selected	D_{OUT}	CS_{OUT}
Read External	V_{IL}	V_{IL}	V_{IH}	EPROM/SRAM Not Selected	High Z	CS_{OUT}
Output Disable	X	V_{IH}	X	X	High Z	CS_{OUT}
Stand-By	V_{IH}	X	X	X	High Z	CS_{OUT}
Write SRAM	V_{IL}	X	V_{IL}	SRAM Selected	D_{IN}	CS_{OUT}
Write External	V_{IL}	X	V_{IL}	No SRAM Selected	X	CS_{OUT}
Program EPROM	V_{IL}	V_{IH}	V_{PP}	EPROM Program Address	D_{IN}	D_{IN}
Program Verify EPROM	V_{IL}	V_{IL}	V_{IH}	EPROM Program Address	D_{OUT}	CS_{OUT}
Program PAD	V_{IL}	V_{IH}	V_{PP}	PAD Program Address	D_{IN}	D_{IN}
Program Verify PAD	V_{IL}	V_{IL}	V_{IH}	PAD Program Address	D_{OUT}	CS_{OUT}

Table 4. High/Low Byte Selection

x16 Configuration Only

$\overline{BHE}$ (Pin 1)	A_0	Write Operation	Read Operation
0	0	Whole word	Whole word
0	1	Upper byte from/to odd address	Upper byte = Data Out Lower byte = 'FF'
1	0	Lower byte from/to even address	Whole word
1	1	None	Upper byte = Data Out Lower byte = 'FF'

$\overline{WR}$ and $\overline{BHE}$ are used for SRAM functions

Table 5. Product Selection Guide

Parameter	MAP168-40	MAP168-45	MAP168-55	Units
Address Access Time (max)	40	45	55	ns
Chip-Select Access Time (max)	40	45	55	ns
Output Enable Time (max)	18	21	23	ns
Chip-Select Output Time	22	25	27	ns
Fast Chip-Select Output Time (max)	17	20	22	ns

Table 6. DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Units
Output Low Voltage	V_{OL}	I_{OL}=8 mA		0.5	V
Output High Voltage	V_{OH}	I_{OH}=−2 mA	2.4		V
CMOS Standby Current	I_{SB1}	notes 1, 3			
—Commercial				20	mA
—Military				30	mA
TTL Standby Current	I_{SB2}	notes 2, 3			
—Commercial				30	mA
—Military				40	mA
CMOS Active Current No Blocks Selected	I_{CC} 1A	notes 1, 4			
—Commercial				20	mA
—Military				30	mA
CMOS Active Current EPROM Block Selected	I_{CC} 1B	notes 1, 4			
—Commercial				35	mA
—Military				45	mA
CMOS Active Current SRAM Block Selected	I_{CC} 1C	notes 1, 4			
—Commercial				55	mA
—Military				65	mA
TTL Active Current No Blocks Selected	I_{CC} 2A	notes 2, 4			
—Commercial				30	mA
—Military				40	mA
TTL Active Current EPROM Block Selected	I_{CC} 2B	notes 2, 4			
—Commercial				40	mA
—Military				50	mA
TTL Active Current SRAM Block Selected	I_{CC} 2C	notes 2, 4			
—Commercial				65	mA
—Military				75	mA
Input Load Current	I_{LI}	V_{IN}=5.5V or GND	−10	10	µA
Output Leakage Current	I_{LO}	V_{OUT}=5.5V or GND	−10	10	µA

Notes:
1. CMOS inputs: GND ± 0.3V or VCC ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Add 1.5 mA/MHz for AC power component.
4. Add 3.5 mA/MHz for AC power component.

Table 7. AC Characteristics

Parameter	Symbol	MAP168-40 Min	MAP168-40 Max	MAP168-45 Min	MAP168-45 Max	MAP168-55 Min	MAP168-55 Max	Units
Read Cycle Time	t_{RC}	40		45		55		ns
Address to Output Delay	t_{ACC}		40		45		55	ns
$\overline{CSI}$ to Output Delay	t_{CE}		40		45		55	ns
$\overline{OE}$ to Output Delay	t_{OE}		18		21		23	ns
Output Disable to Output Float	t_{OEF}		15		18		20	ns
Chip Disable to Output Float	t_{CSF}		15		18		20	ns
Address to Output Hold	t_{OH}	10		10		10		ns
Address to $\overline{CSO}_{0-7}$ True	t_{CSO}		22		25		27	ns
Address to $\overline{FCSO}$ True	t_{FCSO}		17		20		22	ns
SRAM Write Cycle Time	t_{WC}	40		45		55		ns
Chip Enable to Write End	t_{CSW}	40		45		55		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Address Valid to Write End	t_{AW}	40		45		55		ns
SRAM Write Enable Pulse Width	t_{PWE}	25		30		35		ns
Data Setup Time	t_{DS}	20		20		30		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Data Float	t_{WEF}		18		21		23	ns
Write Disable to Data Low Z	t_{WELZ}	3		3		3		ns
$\overline{BHE}$ Setup Time	t_{BHES}	0		0		0		ns
$\overline{BHE}$ Hold Time	t_{BHEH}	10		10		10		ns

Table 8. Data Retention Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Units
Minimum V_{CC} for Data Retention	V_{DR}	V_{CC}=2.0V,	2.0		V
Current in Data Retention Mode	I_{CCDR}	$\overline{CSI} \geq V_{CC}$–0.2V,		1	mA
Chip Deselect to Data Retention	t_{CSDR}	$V_{IN} \geq V_{CC}$–0.2V	0		ns
Recovery Time from Data Retention	t_{RDR}	or $V_{IN} \leq 0.2V$	t_{RC}		ns

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Voltage to any pin with respect to GND	−0.6V to +7V
V_{PP} with respect to GND	−0.6 V to +14.0V
ESD Protection	>2000V

Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Table 9. Operating Range

Range	Temperature	V_{cc}
Commercial	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

Figure 3. Read Cycle Timing Diagram

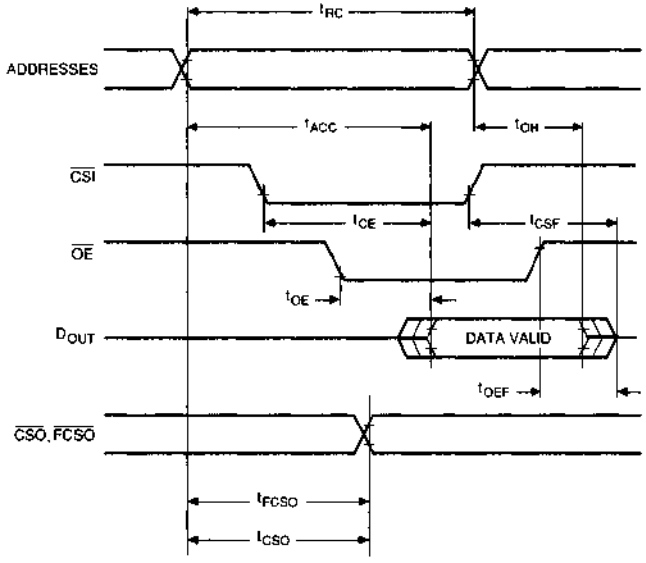

Figure 4. Test Load

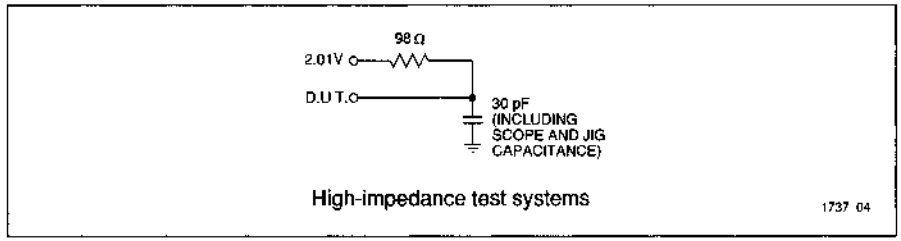

Table 10. Timing Levels

Level	Voltage
Input	0 and 3V
Reference	1.5V

Figure 5. Write Cycle Timing Diagram

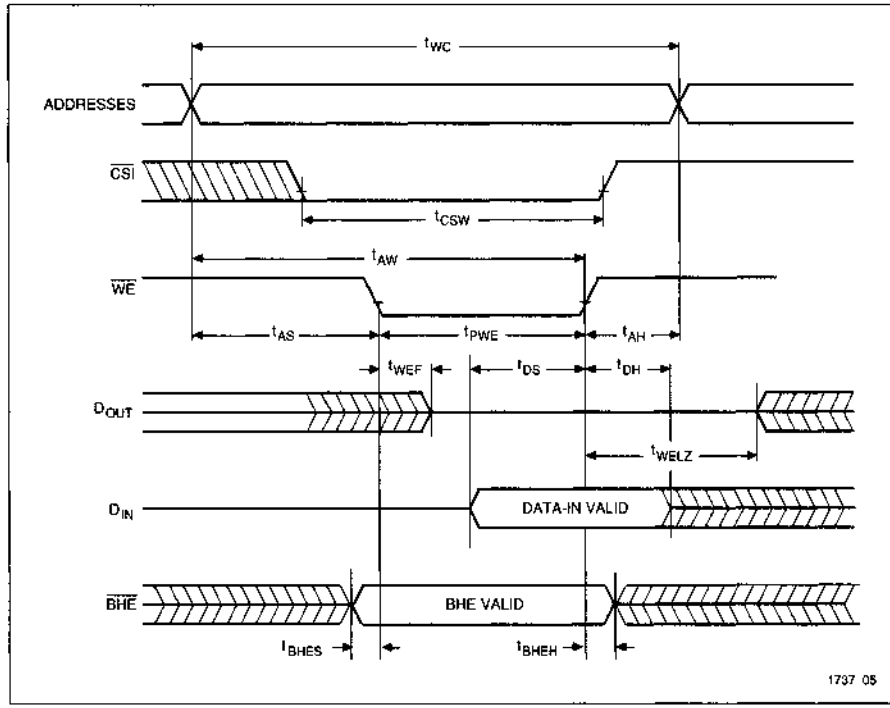

Figure 6. Memory Architecture

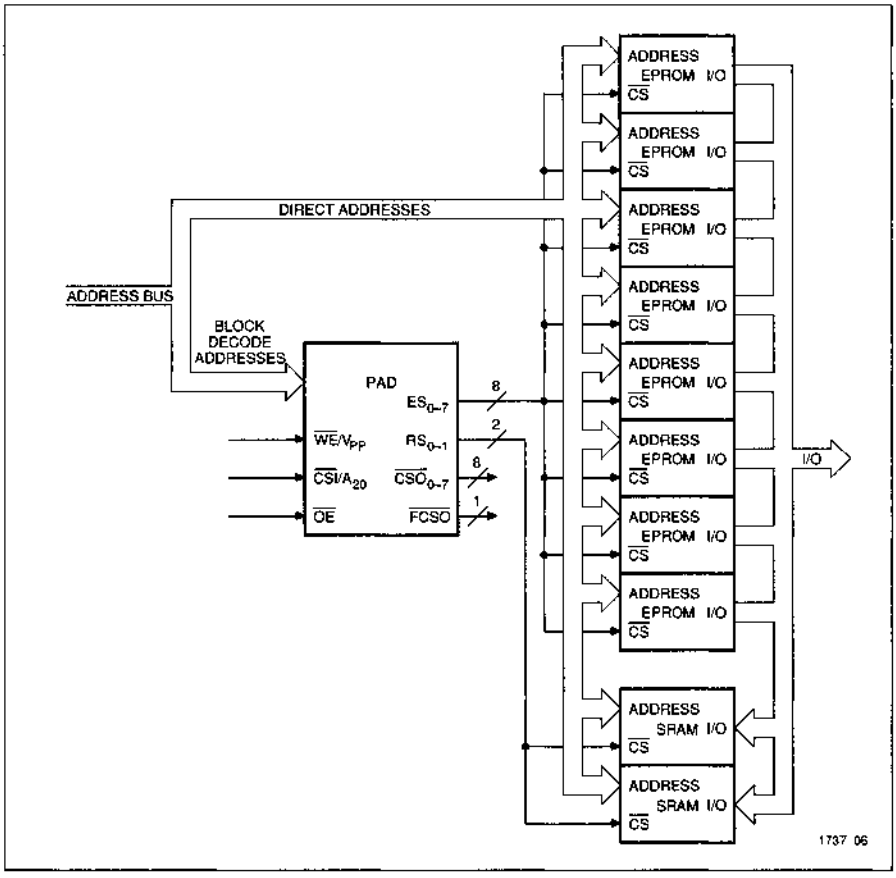

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Table 11. MAP168 Pin Assignments

44-pin CLDCC Package
44-pin PLDCC Package
44-pad CLLCC Package

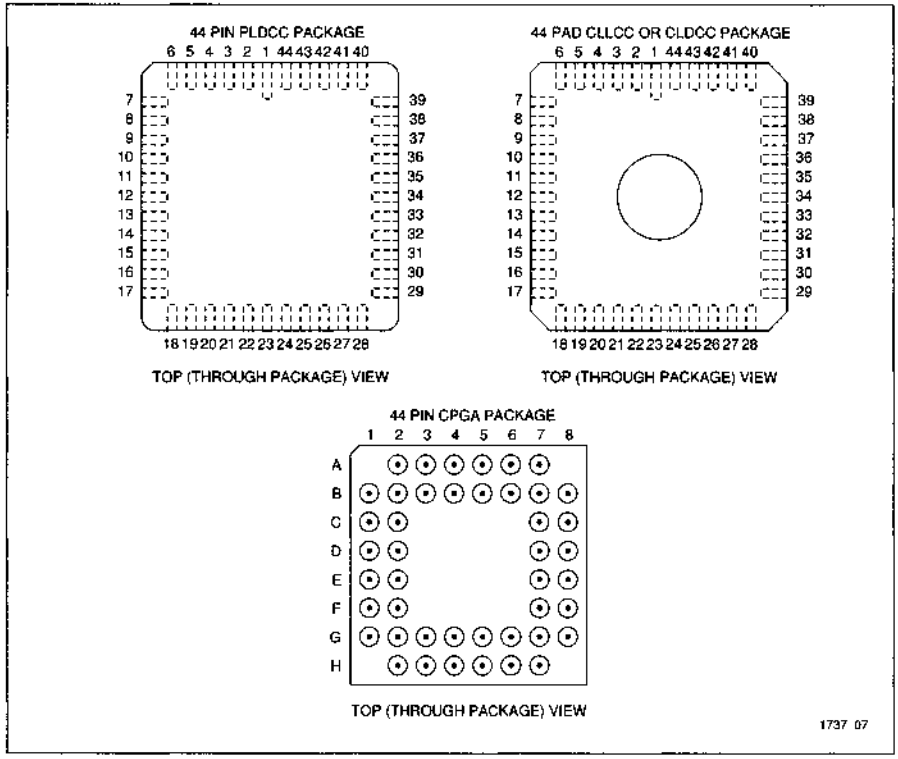
Pin No.	*x8*	*x16*
1	GND	$\overline{BHE}$
2	$\overline{WE}/V_{PP}$	$\overline{WE}/V_{PP}$
3	$\overline{CSI}/A_{20}$	$\overline{CSI}/A_{20}$
4	$\overline{CSO}_7$	I/O_{15}
5	$\overline{CSO}_6$	I/O_{14}
6	$\overline{CSO}_5$	I/O_{13}
7	$\overline{CSO}_4$	I/O_{12}
8	$\overline{CSO}_3$	I/O_{11}
9	$\overline{CSO}_2$	I/O_{10}
10	$\overline{CSO}_1$	I/O_9
11	$\overline{CSO}_0$	I/O_8
12	GND	GND
13	$\overline{FCSO}$	$\overline{FCSO}$
14	I/O_7	I/O_7
15	I/O_6	I/O_6
16	I/O_5	I/O_5
17	I/O_4	I/O_4
18	I/O_3	I/O_3
19	I/O_2	I/O_2
20	I/O_1	I/O_1
21	I/O_0	I/O_0
22	$\overline{OE}$	$\overline{OE}$
23	A_0	A_0
24	A_1	A_1
25	A_2	A_2
26	A_3	A_3
27	A_4	A_4
28	A_5	A_5
29	A_6	A_6
30	A_7	A_7
31	A_8	A_8
32	A_9	A_9
33	A_{10}	A_{10}
34	GND	GND
35	A_{11}	A_{11}
36	A_{12}	A_{12}
37	A_{13}	A_{13}
38	A_{14}	A_{14}
39	A_{15}	A_{15}
40	A_{16}	A_{16}
41	A_{17}	A_{17}
42	A_{18}	A_{18}
43	A_{19}	A_{19}
44	V_{CC}	V_{CC}

$\overline{WE}$ and $\overline{BHE}$ are for SRAM functions.

Table 12. MAP168 Pin Assignments

44-pin CPGA Package		
Pin No.	**x8**	**x16**
A_5	GND	$\overline{BHE}$
A_4	$\overline{WE}/V_{PP}$	$\overline{WE}/V_{PP}$
B_4	$\overline{CSI}/A_{20}$	$\overline{CSI}/A_{20}$
A_3	$\overline{CSO}_7$	I/O_{15}
B_3	$\overline{CSO}_6$	I/O_{14}
A_2	$\overline{CSO}_5$	I/O_{13}
B_2	$\overline{CSO}_4$	I/O_{12}
B_1	$\overline{CSO}_3$	I/O_{11}
C_2	$\overline{CSO}_2$	I/O_{10}
C_1	$\overline{CSO}_1$	I/O_9
D_2	$\overline{CSO}_0$	I/O_8
D_1	GND	GND
E_1	$\overline{FCSO}$	$\overline{FCSO}$
E_2	I/O_7	I/O_7
F_1	I/O_6	I/O_6
F_2	I/O_5	I/O_5
G_1	I/O_4	I/O_4
G_2	I/O_3	I/O_3
H_2	I/O_2	I/O_2
G_3	I/O_1	I/O_1
H_3	I/O_0	I/O_0
G_4	$\overline{OE}$	$\overline{OE}$
H_4	A_0	A_0
H_5	A_1	A_1
G_5	A_2	A_2
H_6	A_3	A_3
G_6	A_4	A_4
H_7	A_5	A_5
G_7	A_6	A_6
G_8	A_7	A_7
F_7	A_8	A_8
F_8	A_9	A_9
E_7	A_{10}	A_{10}
E_8	GND	GND
D_8	A_{11}	A_{11}
D_7	A_{12}	A_{12}
C_8	A_{13}	A_{13}
C_7	A_{14}	A_{14}
B_8	A_{15}	A_{15}
B_7	A_{16}	A_{16}
A_7	A_{17}	A_{17}
B_6	A_{18}	A_{18}
A_6	A_{19}	A_{19}
B_5	V_{CC}	V_{CC}

Figure 7. Pin Assignments Programming



Upon delivery from WSI or after each erasure (see Erasure section), the MAP168 device has all bits in the PAD and EPROM in the "one" or high state. Zeros are loaded through the procedure of programming.

Information for programming the device is available directly from WSI. Please contact your local sales representative.

Erasure

To clear all locations of their programmed contents, expose the device to an ultra-violet light source. A dosage of 15W-second/cm² is required. This dosage can be obtained with exposure to a wavelength of 2537Å and intensity of 1200μW/cm² for 15 to 20 minutes. The device should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

The MAP168 device and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the device; for maximum system reliability, these sources should be avoided. If used in such an environment, the package windows should be covered by an opaque label or substance.

System Development Tools

MAP168 System Development Tools are a complete set of PC-based development tools. Installed on an IBM PC or compatible computer, these tools provide an integrated, easy-to-use software and hardware environment to support MAP168 device development. The tools run on an IBM-XT, AT, or compatible computer running MS-DOS version 3.1 or later. The system must be equipped with 640K bytes of RAM and a hard disk.

System Development Tools (Con't)

Hardware

The MAP168 System Programming Hardware consists of:

- WS6000 MagicPro Memory and PSD Programmer
- WS6003 44-pin LCC Package Adaptor (for 44-pin CLLCC, CLDCC, and PLDCC packages)
- WS6011 44-pin CPGA Package Adaptor

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of the IBM-PC plug-in Programmer Board and the Remote Socket Adaptor Unit.

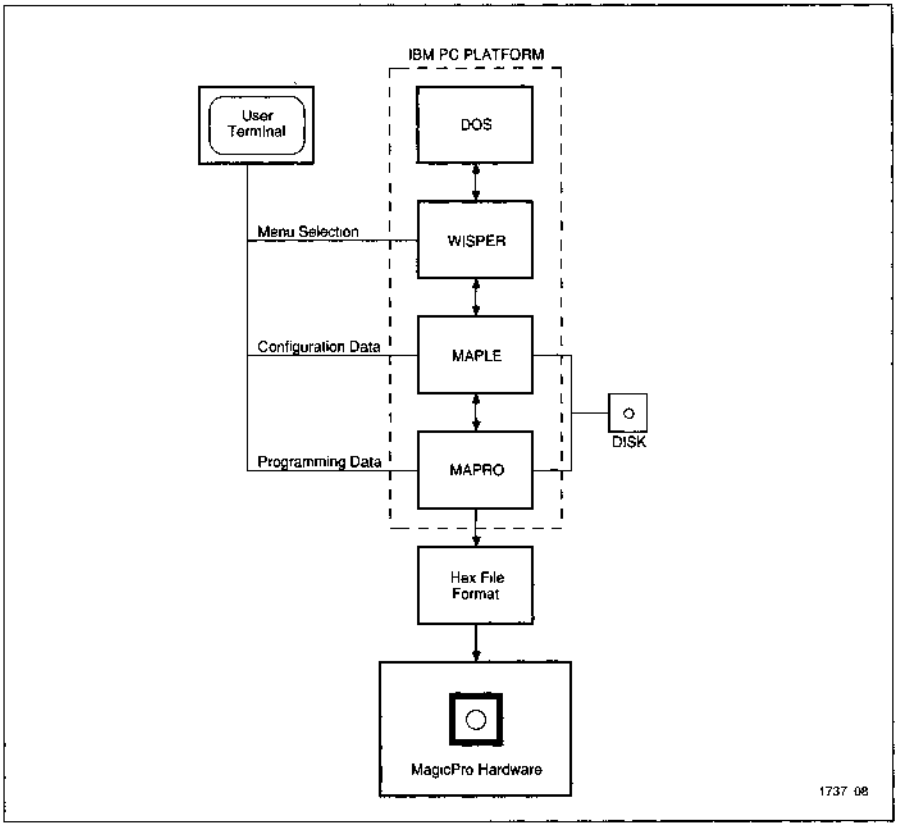
Software

The MAP168 System Development Software consists of the following:

- WISPER Software—PSD Software Environment
- MAPLE Software—MAP168 Location Editor
- MAPPRO Software—Device Programming Software

The configuration of the MAP168 device is entered using MAPLE software. MAPRO software configures MAP168 devices by using the MagicPro programmer and the socket adaptor. The programmed MAP168 is then ready to be used. The development cycle is depicted in Figure 8.

Figure 8. MAP168 Development Cycle



System Development Tools (Con't)

Support

WSI provides a complete set of quality support services to registered System Development Tools owners. These support services include the following:

- ❑ 12-month Software Updates.
- ❑ Hotline to WSI Application Experts—For direct design assistance.
- ❑ 24-Hour Electronic Bulletin Board—For design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the MAP168 device and System Development Tools. Workshop participants learn how to program their own high-performance, user-configurable mappable memory subsystems. Workshops are held at the WSI facility in Fremont, California.

Ordering Information

MAP168 Part Number	Speed (ns)	Package Type	Package Drawing	Operating Temperature	Manufacturing Procedure
MAP168-40C*	40	44-pad CLLCC	C3	Commercial	Standard
MAP168-40J*	40	44-pin PLDCC	J2	Commercial	Standard
MAP168-40L*	40	44-pin CLDCC	L4	Commercial	Standard
MAP168-45C	45	44-pad CLLCC	C3	Commercial	Standard
MAP168-45CM*	45	44-pad CLLCC	C3	Military	Standard
MAP168-45CMB*	45	44-pad CLLCC	C3	Military	MIL-STD-883C
MAP168-45J	45	44-pin PLDCC	J2	Commercial	Standard
MAP168-45L	45	44-pin CLDCC	L4	Commercial	Standard
MAP168-45LM*	45	44-pad CLDCC	L4	Military	Standard
MAP168-45LMB*	45	44-pad CLDCC	L4	Military	MIL-STD-883C
MAP168-45X	45	44-pin CPGA	X2	Commercial	Standard
MAP168-45XM*	45	44-pin CPGA	X2	Military	Standard
MAP168-45XMB*	45	44-pin CPGA	X2	Military	MIL-STD-883C
MAP168-55C	55	44-pad CLLCC	C3	Commercial	Standard
MAP168-55CM	55	44-pad CLLCC	C3	Military	Standard
MAP168-55CMB	55	44-pad CLLCC	C3	Military	MIL-STD-883C
MAP168-55J	55	44-pin PLDCC	J2	Commercial	Standard
MAP168-55L	55	44-pin CLDCC	L4	Commercial	Standard
MAP168-55LM	55	44-pin CLDCC	L4	Military	Standard
MAP168-55LMB	55	44-pin CLDCC	L4	Military	MIL-STD-883C
MAP168-55X	55	44-pin CPGA	X2	Commercial	Standard
MAP168-55XM	55	44-pin CPGA	X2	Military	Standard
MAP168-55XMB	55	44-pin CPGA	X2	Military	MIL-STD-883C

*These products are advanced information.

Ordering Information

System Development Tools

Part Number	Contents
MAP168-GOLD	WISPER Software MAPLE Software User's Manual WSI-SUPPORT WS6000 MagicPro Programmer
MAP168-SILVER	WISPER Software MAPLE Software User's Manual WSI-SUPPORT
WS6000	MagicPro Programmer IBM PC plug-in Adaptor Card Remote Socket Adaptor
WS6003	44-pin LCC Package Adaptor for 44-pin CLLCC, CLDCC, and PLDCC Packages. Used with the WS6000 MagicPro Programmer.
WS6011	44-pin CPGA Package Adaptor. Used with the WS6000 MagicPro Programmer.
WSI-SUPPORT	Support Services including: ❑ 12-month Software Update Service ❑ Hotline to WSI Application Experts ❑ 24-hour access to WSI Electronic Bulletin Board
WSI-TRAINING	Workshops at WSI, Fremont, CA. For details and scheduling, call PSD Marketing, (415) 656-5400.

WAFERSCALE INTEGRATION, INC.

Programmable System™ Device

PSD301

User-Configurable Peripheral with Memory

Preliminary

Key Features

- Second Generation Programmable System Device
- User-Configurable Peripheral for Microcontroller Based Applications — Enables rapid design implementation and fast time to market
- Available in space saving surface mount and through-hole packages
- Windowed package option for prototyping
- Low cost OTP (one-time programmable) package for high volume applications
- CMOS for low power consumption
- User-Configurable to Interface with Any 8- or 16-Bit Microcontroller
  - Programmable Address Decoder (PAD)
  - Programmable Control Signals
  - Programmable Polarity
  - Built-In Address Latches
- Port Expansion/Reconstruction of Up to 16 I/O Lines
  - Individually Configurable as Output or Input
- Highly Configurable, Many Operational Modes
  - Multiplexed or Non-Multiplexed Address/Data Buses
  - Selectable 8- or 16-Bit Bus Width
  - Power-Down
  - Address Inputs Can Be Latched or Transparent
  - Latched Low-Order Address Byte Available as Output
- High-Density UV EPROM
  - 256K Bits Configurable as 32K x 8 or as 16K x 16
  - Divided Into Eight Equal Mappable Blocks
  - EPROM Block Resolution of 4K Bytes or 2K Words
  - EPROM: Up to 120 ns Access Time (Including PAD Decoding Time)
- Static RAM
  - 16K Bits Configurable as 2K x 8 or as 1K x 16
  - SRAM: Up to 120 ns Access Time (Including PAD Decoding Time)
- Addressable Range
  - 1 MByte or 0.5 MWords
- Low Power TTL-Compatible CMOS Device

Applications

- Computers (Workstations and PCs) — Fixed Disk Control, Modem, Imaging, Laser Printer Control
- Telecommunications — Modem, Cellular Phone, Digital PBX, Digital Speech, FAX, Digital Signal Processing
- Industrial — Robotics, Power Line Access, Power Line Monitor
- Medical Instrumentation — Hearing Aids, Monitoring Equipment, Diagnostic Tools
- Military — Missile Guidance, Radar, Sonar, Secure Communications, RF Modems

Product Description

In 1988 WSI introduced a new concept in programmable VLSI, Programmable System Devices. The PSD family consists of user-configurable system-level building blocks on-a-chip, enabling quick implementation of application-specific controllers and peripherals. The first generation PSD series includes the MAP168, a User-Configurable Peripheral, which is ideal for DSP applications; the SAM448, a User-Configurable Microsequencer for control and interface applications, and the PAC1000, a User-Configurable Microcontroller.

The PSD301 is a second generation PSD. The PSD301 is ideal for microcontroller based applications where fast time-to-market, small form factor and low power consumption are essential. When combined together in an 8- or 16-bit system, virtually any microcontroller (8051, 8096, 16000, etc.) and the PSD301 work together to create a very powerful 2-piece chip-set. This implementation provides all the required control and peripheral elements of a microcontroller based system peripheral with no external "glue" logic required.

The PSD301 integrates high performance user-configurable blocks of EPROM, SRAM, and logic in a single circuit. The major functional blocks include a Programmable Address Decoder (PAD), 256K bits of high speed EPROM, 16K bits of high speed SRAM, input latches, and output ports. The PSD301 is ideal for applications requiring high performance, low power, and very small form factors. These include fixed disk control, modem, cellular telephone, instrumentation, computer peripherals, military and similar applications.

The PSD301 is an optimal solution for microcontrollers that need:

- I/O reconstruction (microcontrollers lose at least two I/O ports when accessing external resources).
- More EPROM and SRAM than the microcontroller's internal memory.
- Chip-select, control, or latched address lines that are otherwise implemented discretely.
- An interface to shared external resources.

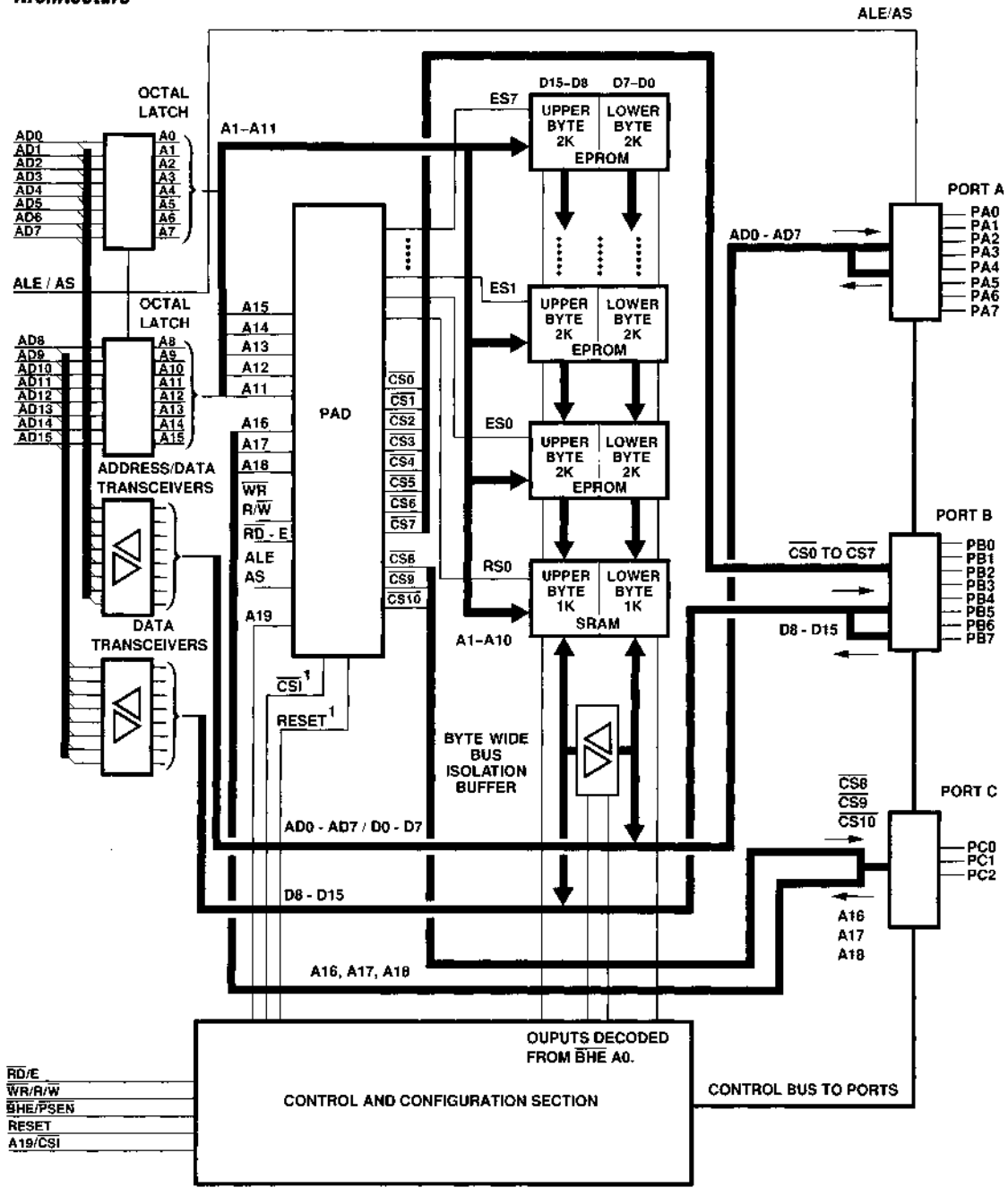
The PSD301 (shown in Figure 1) can efficiently interface with, and enhance, any 8- or 16-bit microcontroller system. No other solution provides microcontrollers with port expansion, latched addresses, a programmable address decoder (PAD), an interface to shared resources, 256 kbit EPROM, and 16 kbit SRAM on a single chip. The PSD301 does not require glue logic for interfacing to any 8- or 16-bit microcontrollers.

The 8051 microcontroller family can take full advantage of the PSD301's separate program and address spaces. Users of the 68HCXX family of microcontrollers can change the functionality of the control signals and directly connect the R/$\overline{W}$ and E signals. Users of 16-bit microcontrollers (including the 80186, 8096, 80196, 16XXX) can use the PSD301 in a 16-bit configuration. Address and data buses can be configured to be separated or multiplexed, whichever is required by the host processor.

The flexibility of the PSD301 I/O ports permit interfacing to shared resources. The user can assign the following functions to these ports: standard I/O pins, chip select outputs from the PAD, latched address or multiplexed low-order address/data byte. This enables users to design add-on systems such as disk drives, modems, etc., that easily interface to the host bus (e.g., IBM PC, SCSI).

The PSD301's on-chip programmable address decoder (PAD) enables the user to map the I/O ports, eight segments of EPROM (as 4K x 8, or as 2K x 16), SRAM (as 2K x 8 or as 1K x 16), and chip select outputs anywhere in the address space of the microcontroller. The PAD can implement up to 4 sum-of-product expressions based on address inputs and control signals. This further facilitates the interface to microcontrollers with different boot-up locations and I/O address mappings, e.g., the 8051 and 8096 microcontrollers have the boot-up addresses in the lower half of their memory maps; the 80186 and 68HCXX use high memory boot-up addresses.

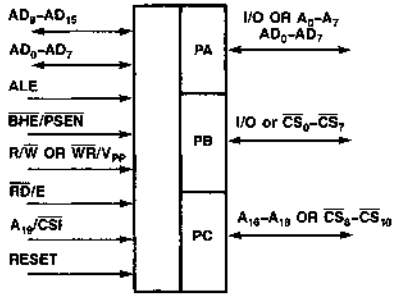
Figure 1. PSD301 Architecture



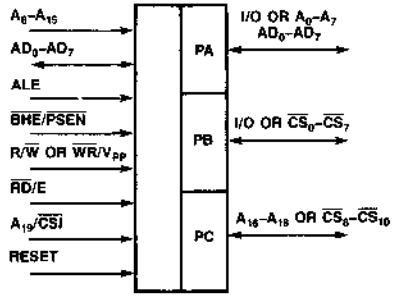
NOTES: 1. RESET and CSI are not available as programmable options in the PAD. An active RESET ensures that the PAD deselects all of its outputs, and a high level on CSI ensures that the PAD is in power-down mode.

Figure 2. PSD301 Port Configurations

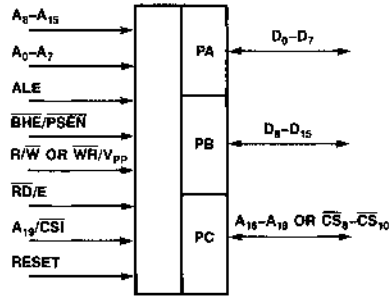
Figure 2 shows the PSD301's I/O port configurations.



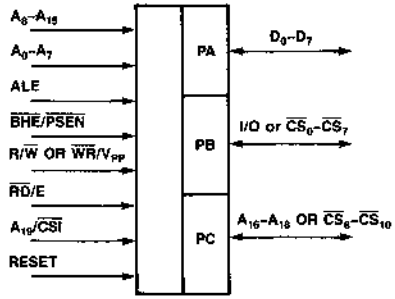
PSD301 configured for multiplexed 16-bit address/data bus



PSD301 configured for multiplexed 8-bit address/data bus.



PSD301 configured for non-multiplexed 16-bit address/data bus.



PSD301 configured for non-multiplexed 8-bit address/data bus.

Legend:

AD_0–AD_7 = addresses A_0–A_7 multiplexed with data lines D_0–D_7.
AD_8–AD_{15} = addresses A_8–A_{15} multiplexed with data lines D_8–D_{15}.

Programmable System™ Device

PAC1000 Introduction

User-Configurable Microcontroller

Overview

In 1988 WSI introduced a new concept in programmable VLSI: the Programmable System™ Devices (PSD). The PSD is defined as a family of *User-configurable system level building blocks on-a-chip enabling quick implementation of application specific controllers and peripherals.* The first generation PSD series includes the MAP168, a User-Configurable Peripheral with Memory; the SAM448, a User-Configurable Microsequencer; and the PAC1000, a User-Configurable Microcontroller.

The PAC1000 user-configurable high-performance microcontroller is the first of a generation of products intended for applications in high-end embedded control where high-speed data processing, interface or control is needed. The PAC1000 replaces a board full of discrete components such as standard logic, FIFO, EPROM for microcode store, ALU, SEQUENCER, register files and PAL/PLD/PGA. To shorten the time-to-market for the system designer, a high-level software development language is used. This contrasts with the myriad state-machine entry, schematic entry, and place and route tools that would be needed for a discrete design using PAL, PLD, PGA or gate arrays.

The PAC1000 architecture is flexible and enables the system designer to customize the PAC1000 to optimize application performance. The PAC1000 is composed of three basic sections: a CPU for data processing, a programmable instruction control unit that determines the next address to the microcode store through polling condition codes or responding to interrupts, and a host interface to asynchronously load data from the host. Registered input/outputs are used to synchronize with the system.

As a result of integrating logic and EPROM memory into the PAC1000 and defining a high-level language for programming both, time-to-market and board space is reduced and reliability increased. The PAC1000 is currently used in applications such as Intelligent DMA controller, FDDI buffer controller, Frame buffer controller, LAN communications controller, disk controller, and I/O controller. For further details on the PAC1000 see Application Note 10.

Contents

WAFERSCALE INTEGRATION, INC.

Programmable System™ Device

PAC1000

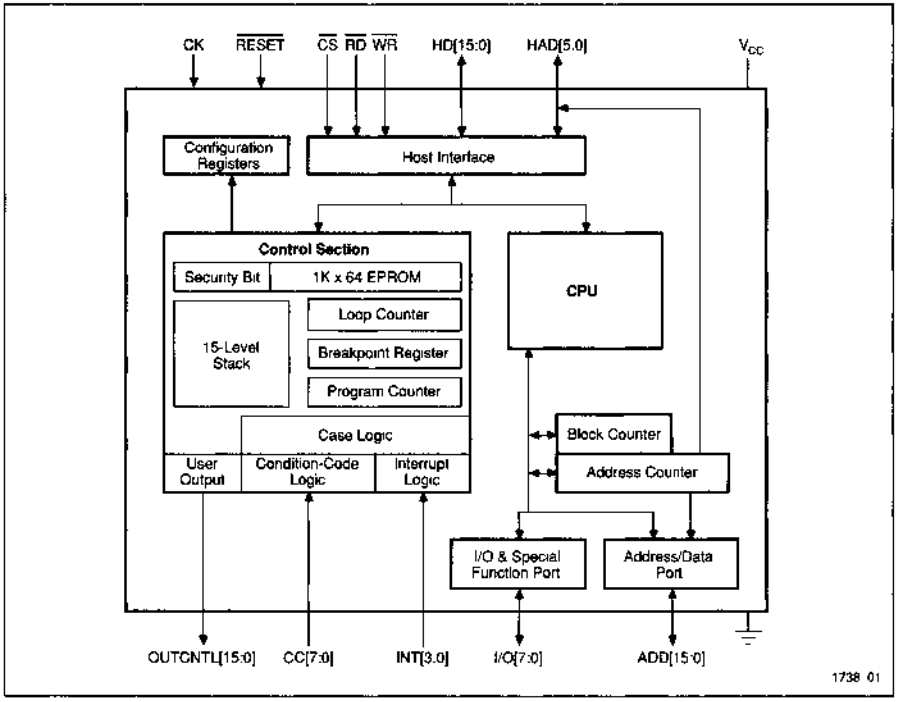
User-Configurable Microcontroller

Features

- First Generation Programmable System Device (PSD)
- High-Performance User-Configurable Microcontroller—20 MHz Instruction Execution, Output Port, and Address Bus
- Single-Cycle Control Architecture—One Cycle Per Instruction
- 16-bit CPU—Arithmetic Operations, Logic Operations, 33 General-Purpose Registers
- Address Generation—Up To 4 Mbytes Address Space
- High-Level Development Tools—System Entry Language, Functional Simulator, and Device Programmer
- Re-Programmable Program Store—On-Board 1Kx64-Bit EPROM
- Two Operating Modes—Host Processor Peripheral or Stand-alone Controller
- Security—For EPROM Program Memory

4

Figure 1. PAC1000 Block Diagram



General Description

In 1988 WSI introduced a new concept in programmable VLSI, Programmable System Devices (PSD). The PSD family consists of user-configurable system-level building blocks on-a-chip, enabling quick implementation of application-specific controllers and peripherals. The first generation PSD series includes the MAP168, a User-Configurable Peripheral with Memory; the SAM448, a User-Configurable Microsequencer; and the PAC1000, a User-Configurable Microcontroller.

The PAC1000 User-Configurable Microcontroller is based upon an architecture that enables it to execute complex instructions in a single clock cycle. Each PAC1000 instruction can perform three simultaneous operations: Program Control, CPU functions, and Output Control, as shown in Figure 2. The PAC1000 can also perform address generation or event counting simultaneously with instruction execution. The PAC1000 is also capable of performing a conditional test on up to four separate conditions and multi-way branching in a single cycle.

The PAC1000, with its System Development Tools, matches the development cycle and ease of use of any standard microcontroller. The high performance and flexibility of the PAC1000 were previously available only to designers who could afford the long development cycle, high cost, high power, and large board space requirements of a building-block solution (i.e., Sequencer, Microcode Memory, ALU, Register File, PALs, etc.)

The unique capabilities of PAC1000 are easily utilized with System development tools, which include a PACSEL C-like System Entry Language, a PACSIM Functional Simulator, and a MagicPro™ Device Programmer. All System Development Tools are PC-based and will operate on an IBM-XT, AT, PS2 or compatible machine. For more information, contact your nearest WSI sales office or representative.

Figure 2. Single-Cycle Control Architecture

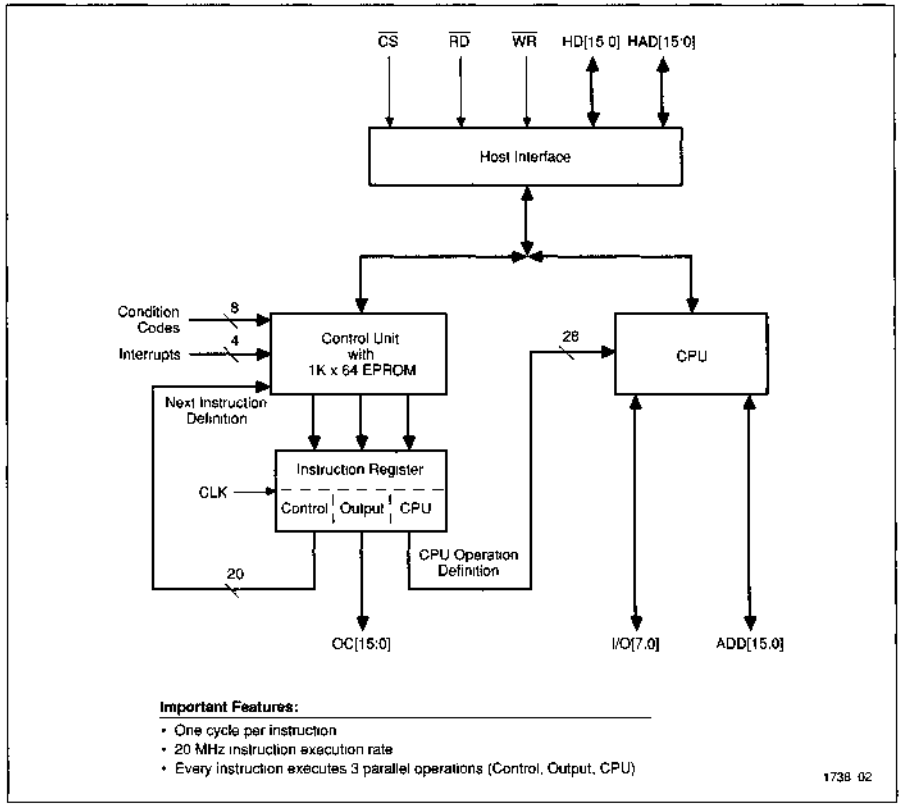


Table 1. Pin Description

Signal	I/O	Description
HD[15:0]	I/O	*Host Data.* PAC1000 Data I/O Port via the Host Interface. Can also be configured to generate 16-bit address or status. Can serve as a general-purpose Data I/O Port.
HAD[5:0]	I/O	*Host Address.* Can be configured to output the lower six bits of the 22-bit Address Counter; can be used as a Host Interface function address, or as a general-purpose 16-bit port.
$\overline{CS}$	I	*Chip Select (active low).* Used with $\overline{RD}$ and $\overline{WR}$ to access the device via the Host Interface.
$\overline{RD}$	I	*Read Enable (active low).* Used with $\overline{CS}$ to output Program Counter, Status Register, or Data Output Register to HD[15:0] bus lines.
$\overline{WR}$	I	*Write Enable (active low).* Used with $\overline{CS}$ to write HD Bus data via the Host Interface into the PAC1000 FIFO.
CK	I	*Clock.*
CC[7:0]	I	*Condition Codes.* Condition-code inputs for use with Call, Jump, and Case instructions.
INT[3:0]	I	*Interrupts.* General-purpose, positive-edge-triggered interrupt inputs.
$\overline{RESET}$	I	*Asynchronous Reset (active low).* Resets Input/Output registers and counters, tri-states all I/O, and sets the Program Counter to 0.
OUTCNTL[15:0]	O	*Output Control.* User-defined Output Port. May be programmed to change value every cycle.
ADD[15:0]	I/O	*Address Port.* Outputs data from Address Counter or Address Output Register when configured as an output. When configured as an input, reads data to Address Input Register.
I/O[7:0]	I/O	*Input or Output Port.* Individually configurable bidirectional bus. As simple I/O, outputs come from the I/O Output Register, and inputs appear in the I/O Input Register. As special I/O functions, provides status, handshaking, and serial I/O. Alternatively, these signals can be used to extend the OUTCNTL or ADD lines.

Architectural Overview

The PAC1000 is a user-configurable microcontroller optimized for high-performance control systems. The primary architectural elements, shown in Figure 3, are the Control Section, 16-bit CPU, Host Interface, 16-bit Address Port, 16-bit Output Control, 8-bit I/O Port, and Configuration Registers.

The PAC1000 can be used as a stand-alone microcontroller or as a peripheral to a host. In the latter case, the Host Data (HD) and Host Address (HAD) buses, together with the $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ pins allow for direct connection to a host bus. User-defined commands to the Control Section or data to the CPU can be loaded through the Host Interface.

In the stand-alone mode, the Host Interface ports can be used as additional address, data or I/O ports using the Data Output Register (DOR) and Data Input Register (DIR). The ADD port can be used to generate addresses through the Address Output Register (AOR) or the Address Counter. A DMA channel can be formed on the Host Interface using these and the Block Counter (BC) register. In addition, the ADD port can be used as a data bus or an I/O port, depending on how the chip is configured. Each pin in the I/O port can be configured individually as input, output, or special function. The special functions allow the control of internal PAC1000 elements (counters, I/O buffers) by other board elements.

The 16-bit CPU is highly parallel and can operate on operands from the 32x16-bit register file, miscellaneous register (AOR, AIR, DOR, DIR, Q, etc.), or constants loaded from the internal program-store EPROM.

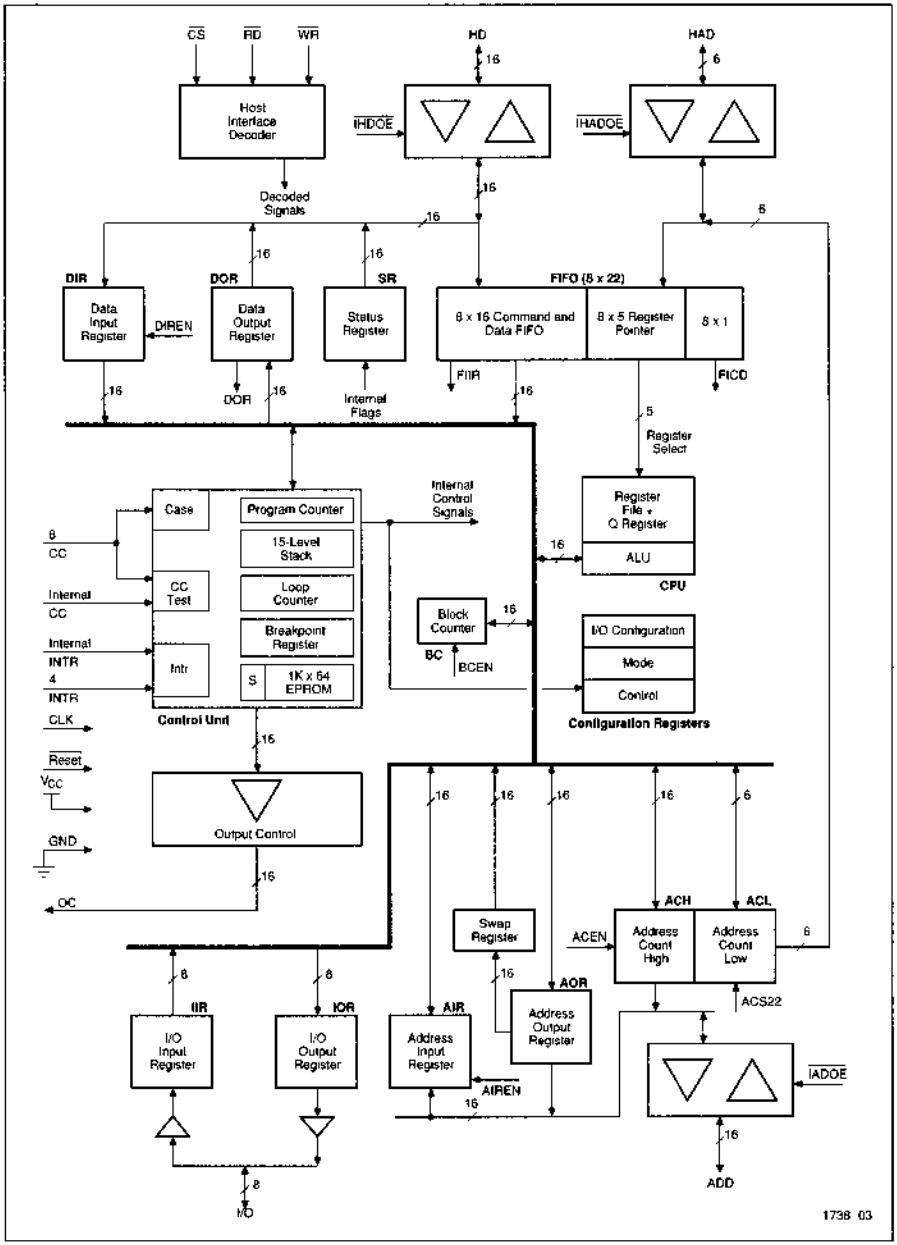
The internal and external operations of the PAC1000 are controlled by the Control Section. The 16 Output Control (OC) lines are general-purpose outputs. Each of them can be changed independently every clock cycle. They provide a very fast means to control various processes outside the chip.

In every clock cycle, one instruction is executed. Each instruction consists of up to three operations in parallel:

- Instruction Fetch—the next instruction is fetched from the 1Kx64 EPROM by the Program Control.
- Execution—the CPU executes an instruction.
- Output—placed on the Output Control (OC) lines.

Program flow can be changed through the condition-code inputs in one clock cycle or through the interrupt inputs after two clock cycles. Single-cycle 16-way branches can be done using the Case instruction, which samples four condition codes per cycle. Nested loops and subroutines can be carried out with the 15-level stack and the loop counter. The chip configuration can be changed in any cycle by loading the Configuration Register using the Program Control instruction portion.

Figure 3. Detailed Block Diagram



Operational Modes

The two basic modes of operation for the PAC1000 are either as a memory-mapped peripheral (Figure 4) or as a stand-alone controller (Figure 5).

In the peripheral mode, the host processor can asynchronously interface with the PAC1000.

Figure 4. Peripheral Mode

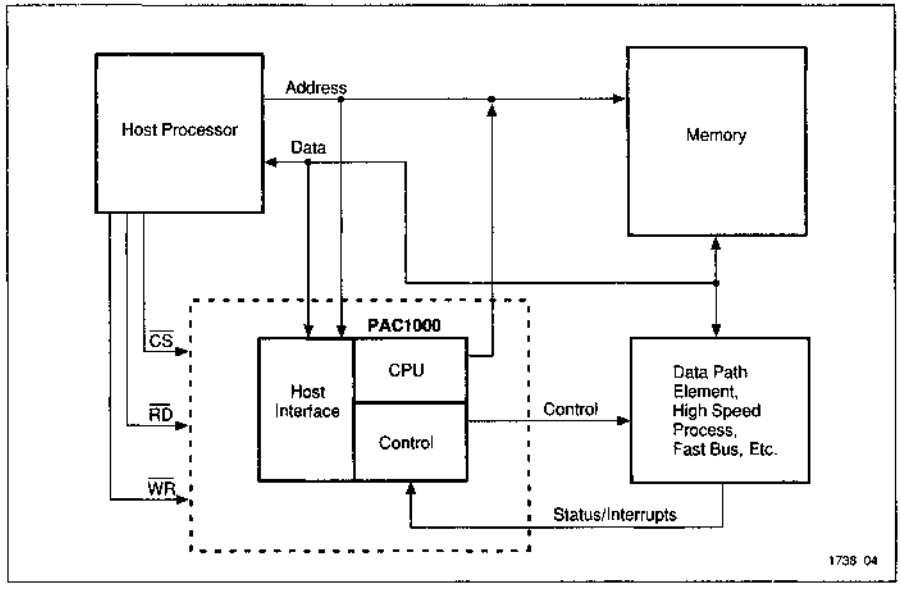
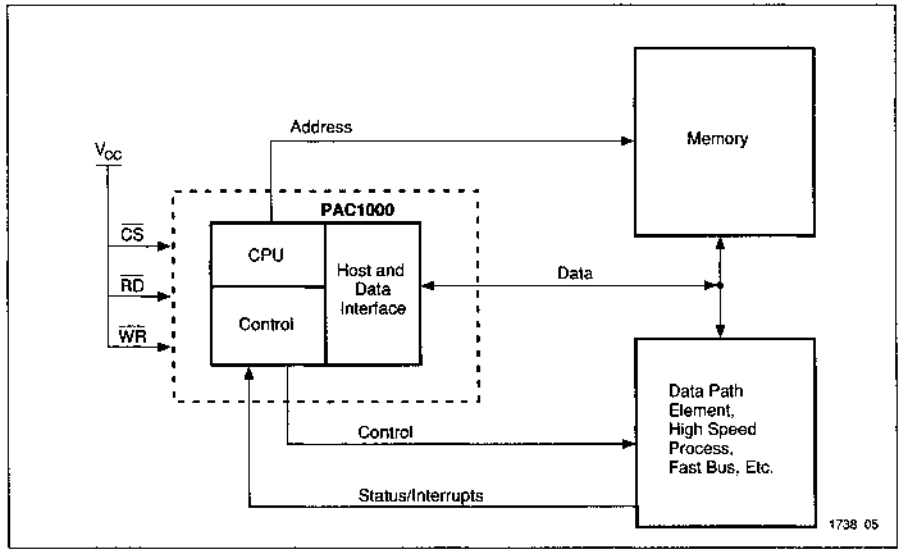


Figure 5. Stand-alone Mode



Host Interface

The Host Interface section of the PAC1000, shown in Figure 6, includes the Input Command/Data FIFO, Input/Output Data Registers, and the Status Register.

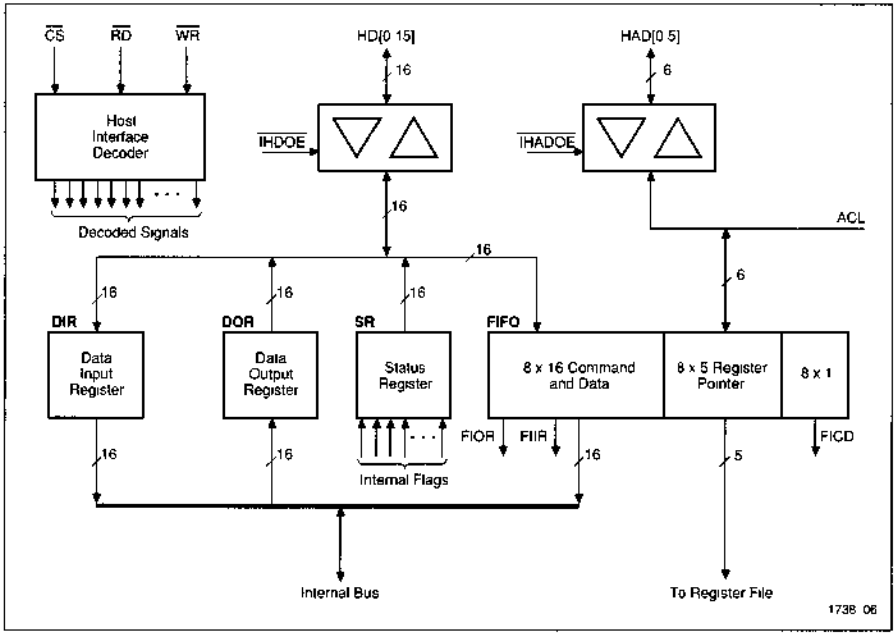
FIFO

When the PAC1000 serves as a peripheral to a host, the FIFO is used to asynchronously load commands or data into the PAC1000. In order to write into the FIFO, $\overline{CS}$ and $\overline{WR}$ must have low-to-high transitions. The information written into the FIFO is specified by the 16-bit Interface Data bus (HD) and the 6-bit Host Address bus (HAD). Since the FIFO is used only to buffer data and commands from a host, it is inoperative when the PAC1000 is in stand-alone mode.

Bit five of the HAD bus specifies whether the input to the FIFO is command (HAD5=1) or data (HAD5=0). HAD5 is connected to the FICD internal Condition Code that can be sampled by the Control Section. If a command is written, then the lower 10 bits of the HD bus are used as the branch address for one of the 1024 locations in the Program Memory EPROM. At that location a user defined command or subroutine should exist which executes the needed operation. If the information is data, then the lower 5 bits of the HAD bus specify which CPU register is to be loaded from the HD bus.

This method of operation allows the host to access the PAC1000 as a memory-mapped peripheral.

Figure 6. Host Interface Architecture



4

Host Interface (Con't)

An example of FIFO usage is shown in Figure 7. When command or data information is available in the FIFO, the FIFO Output Ready (FIOR) interrupt (interrupt 5) triggers. If the FIOR interrupt is masked, then the FIOR status may be polled under program control. If HAD5 equals 1, the branch address location specified by MOVE is the Program Memory Address which contains the user specified instruction or sub-routine which executes the command. A JUMP or CALL FIFO control instruction performs a jump or call to the location specified by MOVE. If HAD5 equals 0, an RDFIFO instruction can transfer the FIFO contents into the register specified by HAD[4:0].

For further explanation, refer to the diagram below. Beginning at the location specified by MOVE, a user defined program exists which is going to load data into CPU registers 0,1,2, and 3 in four consecutive cycles from the next four FIFO locations. If one of the four FIFO locations contains a command (FICD=1), interrupt level 7 occurs (highest level). Loading a command into a CPU or other data register is not allowed. If this occurs, FIXP (FIFO exception) will be generated.

Following the execution of this routine, the Control Section is ready for its next instruction.

The FIFO drives three internal flags which can also be programmed to interrupt the PAC1000. They are:

- $\overline{\text{FIIR}}$ (FIFO full) and FIXP (FIFO exception), which drive INT7.
- FIOR (FIFO output ready), which drives INT5.

Table 2. Host Interface Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	HAD5	HAD[4:0]	HD[15:0]	Function
0	1	0	0	Register Address	Data	Write data to FIFO
0	1	0	1	X	Command	Write command to FIFO
0	0	1	0	00100	X	Reset FIFO
0	0	1	0	00011	X	Reset status register
0	0	1	0	00010	Data	Read program counter
0	0	1	0	00001	Data	Read status register
0	0	1	0	00000	Data	Read data output register

Host Interface (Con't)

Data I/O Registers

Input and Output Data Registers are used to communicate with the Host Data (HD) bus. CPU Registers may be loaded directly from the Data Input Register (DIR) without passing through the FIFO. Similarly, the PAC1000 may be read via the Data Output Register (DOR).

Program Counter

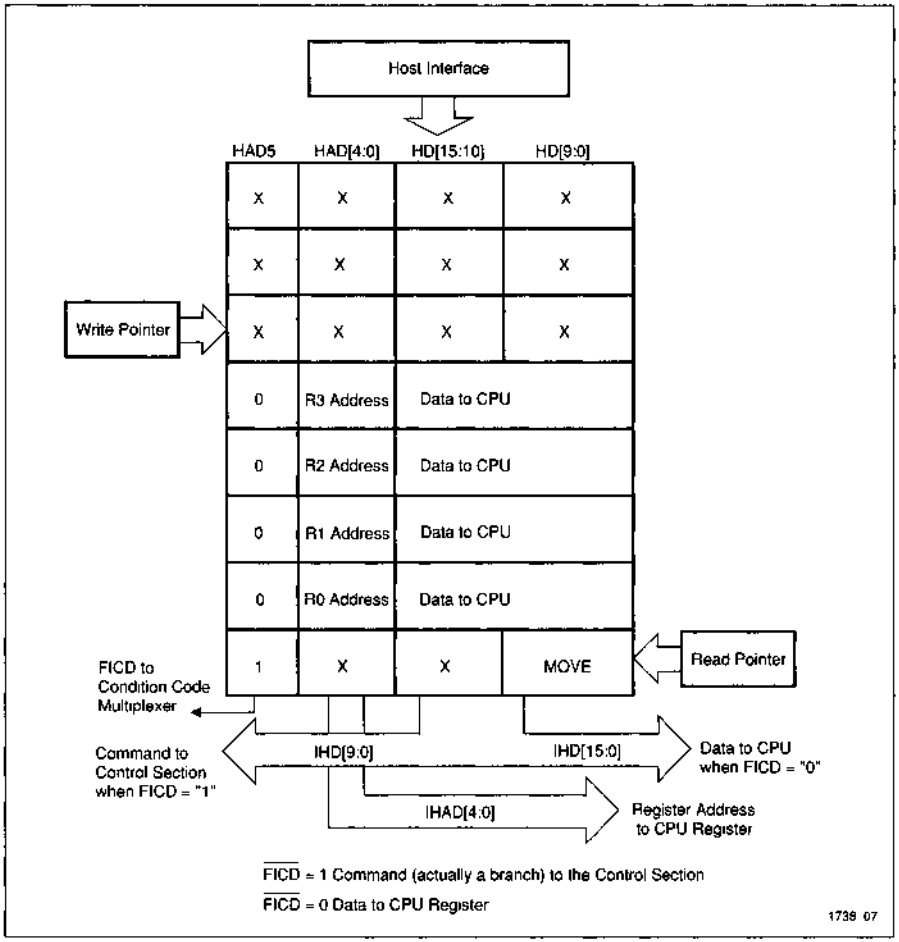
The Program Counter may be read via the Host Data bus. This allows a host to monitor the Program Memory address bus. It can also be used to drive external memory devices for expansion of the Control Port.

Status Register

The Status Register (SR), shown in Figure 8, monitors all internal status. Status bits can be set only by program execution. The SR can be read or cleared as specified in the Host Interface Functions table.

All SR flags are active high (1) and are latched at the rising edge of the clock.

Figure 7. Example of FIFO Block Diagram and Usage



Host Interface (Con't)

STAT11—(DBB) *Security Bit*, set when security is active:

1= Security active.

0= No security.

STAT10—*WSI Reserved.*

STAT9—(FIXP) *FIFO Exception*, set when the CPU receives a command or Control Section receives data:

1= Command or data received.

0= No exception occurred.

STAT8—(FIIR) *FIFO-Input Ready*, set when there is at least one vacant location in the FIFO:

1= FIFO ready for input.

0= FIFO not ready for input.

STAT7—(CY) *Carry Flag*, set when a carry (addition) or borrow (subtraction) occurs in CPU operations:

1= Carry occurred.

0= No carry occurred.

STAT6—(Z) *Zero Flag*, set when the result of a CPU operation is zero:

1= Zero occurred.

0= No zero occurred.

STAT5—(O) *Overflow Flag*, set when an overflow occurs during a two's complement operation:

1= Overflow occurred.

0= No overflow occurred.

STAT4—(S) *Sign Bit*, set when the most significant bit of the result of the previous CPU operation is negative:

1= Result is negative.

0= Result is positive.

STAT3—(STKF) *Stack Flag*, set when the stack is full:

1= Stack is full.

0= Stack is not full.

STAT2—(BRKPNT) *Breakpoint Flag*, set when the address in the breakpoint register is equal to the EPROM address:

1= Breakpoint occurred.

0= No breakpoint occurred.

STAT1—(BCZ) *Block Counter Zero*, set when the counter decrements to all 0s:

1= Block Counter reached zero.

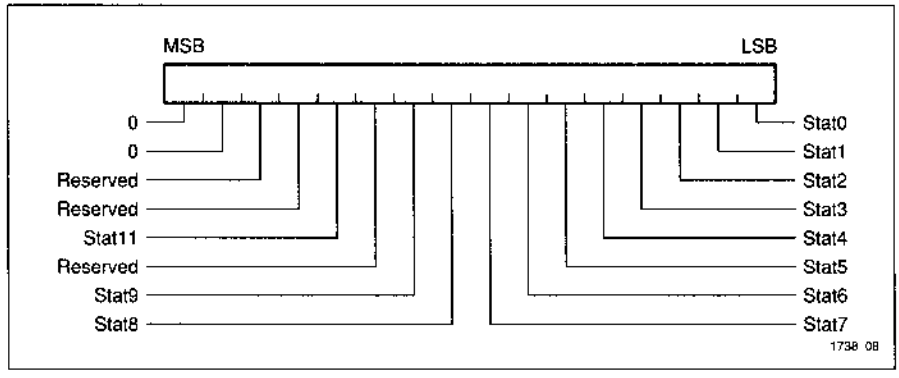
0= Block Counter is not zero.

STAT0—(ACO) *Address Counter Ones*, set when the counter increments to all 1s:

1= Address Counter reached all ones.

0= Address Counter is not all ones.

Figure 8. Status Register



Control Section

The control section, shown in Figure 9, consists of a number of blocks which are concerned with the sequencing of the control programs in the PAC1000. These are:

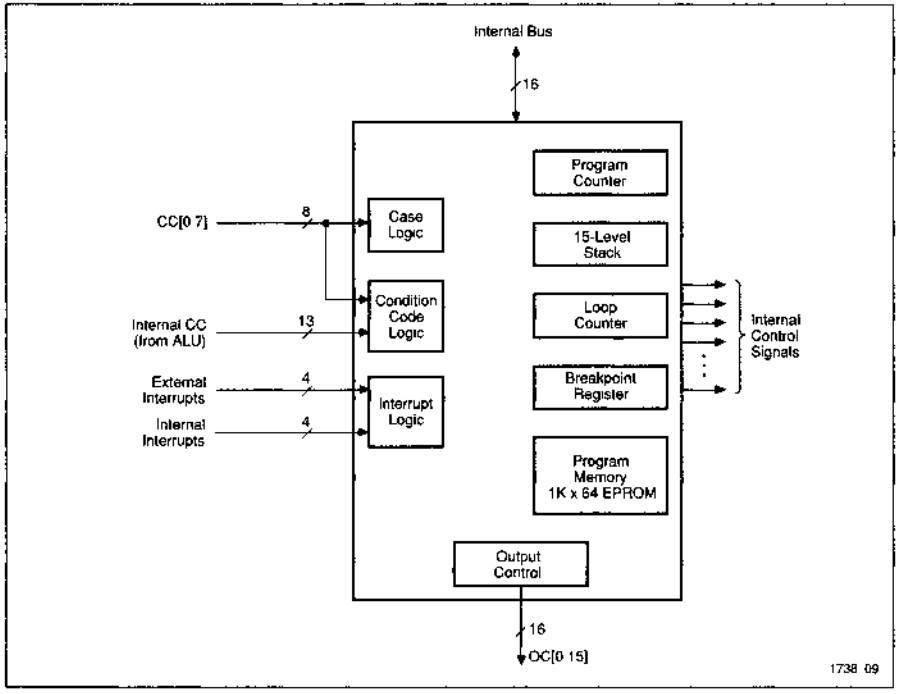
- Program Memory
- Security
- 15-Level Stack
- Program Counter
- Loop Counter
- Breakpoint Register
- Condition Codes
- Case Logic
- Interrupt Logic
- Output Control

Each block is described in detail below.

Parallel Operations

The PAC1000 can perform three simultaneous operations within a single instruction cycle, as shown in Figure 10. The ability to fetch an instruction from the Program Memory, execute it, and output a result within 50 nsec is due to a highly parallel structure.

Figure 9. Control Architecture



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Control Section (Con't)

Program Memory

The Program Memory is a 1Kx64 high-speed EPROM. This on-board-memory allows the PAC1000 to operate in embedded control applications and eliminates the need for external memory components. Using an erasable memory allows program code to be modified for debug and/or field upgrades. The Program Memory is easily programmed using the WSI MagicPro™ (Memory and PSD™ Programmer).

Only sixteen Program Memory locations are reserved. The rest of the 1024 locations are available for applications.

Program memory is segmented as follows:

Address	Function
000H	Reset pointer program to here
000H–007H	User Defined Initialization Routine
008H–00FH	Interrupt Vector Locations
010H–3FFH	User-Defined Application Programs

Upon receiving a reset, the Program Counter is forced to address 000H. This location may contain a jump or call which branches to an initialization routine. Alternatively, the first eight locations of memory may be used as an initialization/configuration routine.

Security

User programs may be protected by setting a security bit during EPROM programming. Thereafter, the EPROM contents cannot be read externally. When the EPROM is erased, the security bit is cleared.

15-Level Stack

The 15-level Stack stores the return address following subroutine calls, interrupt service routines and the contents of the Loop Counter inside nested loops. When the stack is full, the STKF condition becomes true, and an interrupt (INT7) will occur. The interrupt service routine will overwrite the top of the stack.

Popping from an empty stack produces the previous top of stack value; pushing on a full stack overwrites the top of the stack.

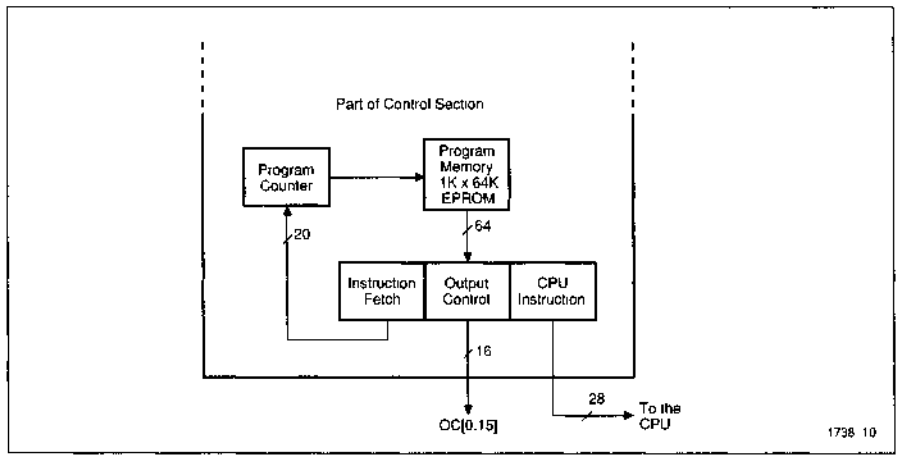
Program Counter

The 10-bit Program Counter (PC) generates sequential addressing to the 1K word Program Memory. Upon reset the PC is loaded with a 000H. From this point the value of the Program Counter is determined by program execution or interrupts.

Any JUMP or Case instruction that is executed loads the Program Counter with the destination address. CALL instructions or interrupts cause PC + 1 to be pushed onto the stack. The RETURN instruction loads the Program Counter from the stack with the value of the return address. This value may have previously been placed on the stack by a CALL or interrupt.

The PC can also be loaded from the Command/Data FIFO causing program execution to commence at an address provided by the host.

Figure 10. Parallel Operations



Control Section (Con't)

Loop Counter

The Loop Counter (LC) has two functions:

- 10-bit down counter that supports the LOOP instruction.
- Branch Register that can be loaded from the CPU Register File or Program Memory and used as an additional source of branching to Program Memory.

The LC can be loaded with values up to 1023. Loop initialization code places a value in LC. Loop termination code tests the counter for a zero value and then decrements LC. The loop count can be a constant, or it can be computed at execution time and loaded into LC from the CPU. The LC register can also be used as a CALL or JUMP execution vector. The content of the LC is automatically saved on (or retrieved from) the Stack when the program enters (or leaves) a nested loop.

A loop count will be loaded into the LC when a FOR instruction is encountered. This count can be a fixed value or it can be calculated and loaded from the CPU. The ENDFOR instruction will test the Loop Counter for a zero value. If this condition is not met, then the LC will be decremented by one. The program loop will continue until the count value equals zero. In a nested loop, the FOR instruction will load a new value to the LC and push the previous value to the stack.

Debug Capabilities

The PAC1000 provides breakpoint and single step capabilities for debugging application programs.

Breakpoint Register

The Breakpoint Register (BR) is a 10-bit register used for real time debug of the PAC1000 application program.

The Breakpoint Register can be loaded from one of two sources, either a constant value specified in the Program Memory or a calculated value loaded from the CPU. When the Program Memory address matches the contents of the Breakpoint Register an interrupt (INT 6) occurs. A service routine should exist in Program Memory which then performs the required procedure.

Single Step

Single step is a debugging mode in which the currently-executing program is interrupted by interrupt 6 after the execution of every instruction. The interrupt 6 service routine should reside in Program Memory.

Bit 8 in the Mask Register determines whether the PAC1000 is in a breakpoint mode (mask-bit 8 equals 0) or in a single step mode (mask-bit 8 equals 1).

Both breakpoint and single step use interrupt 6. The interrupt 6 service routine will typically dump the contents of the PAC1000 internal registers into external SRAM devices for examination by the user.

Condition Codes

The Condition Code (CC) logic operates on 21 individual program test conditions. Each condition can be tested for true or not true. The PAC1000 can also test up to four conditions simultaneously. For this feature refer to the section titled *Case Logic*.

Control Section (Con't)

User-Specified Conditions

User-Specified Conditions are treated in the same manner as internally generated test conditions. CC0—CC7 should be connected directly to the corresponding PAC1000 input pins. These signals must satisfy the required setup time to be serviced in the next cycle.

CPU Flags

CPU flags are internally generated. They reflect the status of the previous CPU arithmetic operation. These signals are internally latched and are valid only for one instruction (the instruction following their generation). The flags for arithmetic operations are defined as follows:

Zero (Z)—The result of the previous CPU operation is zero (Z=1).

Carry (CY)—The result of the previous CPU operation generated a carry (addition) or borrow (subtraction) (CY=1).

Overflow (O)—The previous two's complement CPU operation generated an overflow (O=1).

Sign (S)—The most significant bit of the result of the previous CPU operation is negative (S=1).

FIFO Flags

FIFO flags allow the user to synchronize and monitor the operations that are performed on the FIFO by the host or by user's program.

Upon reset the FIFO flags are cleared, signifying an empty state. The meaning of the flags are as follows:

FIFO Output Ready (FIOR)—There is at least one word in the FIFO (FIOR=1).

FIFO Input Ready (FIIR)—FIFO is not full (FIIR=1). This flag can also be connected to the host through I/07.

FIFO Command/Data (FICD)—This flag indicates if the contents of the FIFO is a command or a data. This flag is generated directly from HAD5 (FICD=1 command, FICD=0 data).

FIFO Exception (FIXP)—This flag indicates that one of two events occurred: (a) FIFO data has been read as a command, or (b) a command has been read as data.

Stack-Full Flag

STACK FULL flag (STKF=1) indicates that the stack is 15 levels full. This condition will also generate an interrupt (INT7) if not masked.

Interrupt Flag

INTERRUPT flag (INTR =1) indicates that there is a masked interrupt pending. This flag is cleared when the interrupt is cleared.

Data Register Read Flag

DATA REGISTER READ flag (DOR) is a handshake flag between the host and the PAC1000, accessible only to the PAC1000. The flag is reset (DOR=0) when the PAC1000 writes into the Data Output Register. The flag is set (DOR=1) after the host has performed a read on the Data Output Register.

Counter Flag

Counter flags reflect the status of their respective counters. The PAC1000 utilizes two counters; the Address (A) counter is a 16/22-bit auto-incrementing up counter; the

Table 3. Condition-Code Logic

Test Group	Source	Conditions and Flags
User-Specified	External	CC0–CC7
CPU	Internal	Carry (CY), Zero (Z), Overflow (O), Sign (S)
FIFO	Internal	FIFO Command/Data (FICD), FIFO Output Ready (FIOR), FIFO Input Ready (FIIR), FIFO Exception (FIXP)
Counters	Internal	Address Counter Ones (ACO), Block Counter Zero (BCZ)
Stack	Internal	Stack Full (STKF)
Interrupt	External/Internal	Interrupt (INTR) is pending
Data register read	Internal	Data Output Register(DOR) has been read

Control Section (Con't)

Block (B) counter is an auto-decrementing 16-bit down counter. The counters' clock input signal is the same as the PAC1000's clock signal. Each counter can be individually enabled or disabled. When disabled, the output retains the last count. The counter flags are defined as follows:

ACO—*A Counter Ones*, set when the A counter has reached the value FFFFH, in the 16-bit mode, or the value 3FFFFFH in the 22-bit mode.

BCZ—*B Counter Zero*, set when the B counter has reached the value 0000H.

Case Logic

THE PAC1000 hardware implements two basic types of Case instructions: Case and Priority Case.

Case Instructions

Case instructions operate on any one of four different Case groups. Each Case group consists of a combination of four test conditions which can be tested in a single cycle. In that same cycle the PAC1000 will branch to one of the addresses contained in the sixteen memory locations following the instruction, depending on the status of the four inputs to the Case group being tested.

There are four Case Groups (sets of Case Conditions):

Case Group 0 (CG0): CC0–CC3.

Case Group 1 (CG1): CC4–CC7.

Case Group 2 (CG2):

- Z—Zero
- O—Overflow
- S—Sign
- CY—Carry

Case Group 3 (CG3):

- INTR—Interrupt
- BCZ—B Counter Zero
- FIOR—FIFO output Ready
- FICD—FIFO Command/Data

(The FIXP, ACO, STKF, FIIR, and DOR condition codes do not fall into any of the four Case groups.)

Priority Case Instructions

Priority Case instructions operate on the four internal and the four external interrupt inputs. In this mode of operation, interrupts are treated as prioritized test conditions and the priority encoder is used to generate a branch to the highest priority condition. The branch address is located in one of the nine memory locations following the Priority Case instruction. Priorities in this mode of operation are the same as in the Interrupt mode of operation. Once a Priority Case instruction is executed, the occurrence of a higher priority condition will not affect program execution until another Priority Case instruction is executed. For a Priority Case instruction to be executed, MODE0 of the Mask Register must be equal to zero (MODE0=0).

Interrupt Logic

The Interrupt Logic accepts eight inputs, four of them are generated externally and four are dedicated for internal conditions. The four external, user defined, inputs (INT0–INT3) are connected to pins INT0, INT1, INT2, and INT3. These are positive, rising-edge-triggered signals that have a maximum latency of two cycles. Each interrupt has a reserved area in memory that should contain a branch to an interrupt service routine.

Table 4. Interrupt Assignments

Interrupt	Priority	Effect	Trigger Condition	Reserved Address
INT7	Highest	Internal	FIXP+ACO+STKF+$\overline{\text{FIIR}}$	00FH
INT6		Internal	BRKPT	00EH
INT5		Internal	FIOR	00DH
INT4		Internal	Software Interrupt (SWI)	00CH
INT3		External	INT3	00BH
INT2		External	INT2	00AH
INT1		External	INT1	009H
INT0	Lowest	External	INT0	008H

Control Section (Con't)

Clearing a serviced interrupt is performed automatically. When the interrupt is serviced, the internally generated vector is decoded to clear the serviced interrupt. In addition, the user can clear any pending interrupt by using the Clear Interrupt Instruction (CLI).

Interrupt Mask Register

The Interrupt Mask Register, shown in Figure 11, allows individual interrupts to be masked. Setting a Mask Register bit to a 1 masks the associated interrupt. To unmask an interrupt, the appropriate Mask Register bit must be reset to 0.

When the PAC1000 is reset,the Mask Register will mask all interrupts and the Mode Register will select the non-interrupt mode. To select the interrupt mode the MODE0 bit (see Configuration Register section in this document) should be set to 1 (MODE0=1).

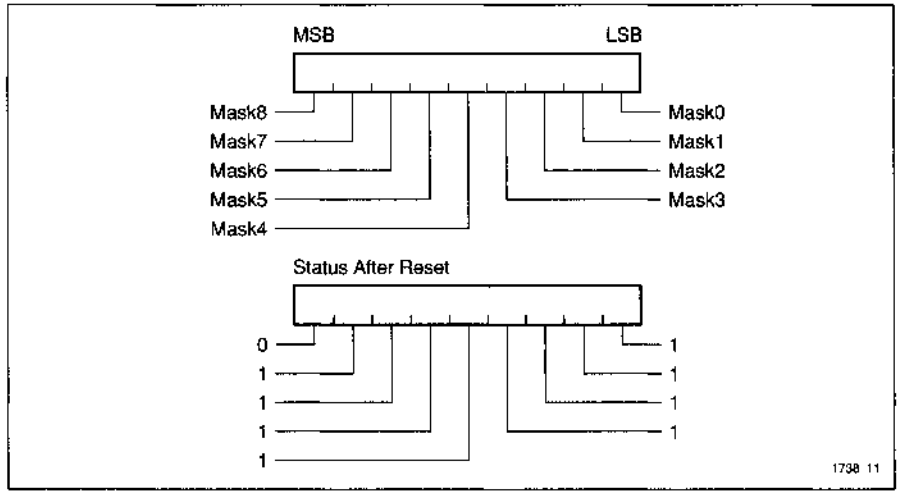
Mask8 is used to select INT6 to be either a single-step interrupt (when Mask8=1) or a breakpoint interrupt (when Mask8=0) .See the section on Debug Capabilities for further details.

Table 5. Interrupt Definitions

Interrupt	Triggered By
INT7[1]	FIFO Exception (FIXP)
	Address Counter contains all Ones (ACO)
	Stack Full (STKF)
	FIFO Full (Not FIFO Input Ready, $\overline{FIIR}$)
INT6[2]	Breakpoint or Single Step occurrence
INT5	FIFO Output Ready (FIOR)
INT4	Always pending; triggers when unmasked by program execution
INT3	User-defined
INT2	User-defined
INT1	User-defined
INT0	User-defined

Notes:
1. The INT7 interrupt handler checks the source of the interrupt by testing the condition code.
2. See Interrupt Mask Register, Mask8.

Figure 11. Interrupt Mask Register



Control Section (Con't)

Output Control

The Output Control bus (OUTCNTL) consists of 16 latched Output Control signals. These signals can be changed on a clock to clock basis. For every Program Memory location there is a dedicated field which specifies the value of the Output Control bus. The OUTCNTL Operation places this value on the Output Control bus. The OUTCNTL Operation can be performed in parallel with any other PAC1000 instructions.

The OUTCNTL bus can be used to control external events on a clock to clock basis.

Counters

The PAC1000 contains a 16 or 22-bit Address Counter and a 16-bit Block Counter. Each of these counters can change count on a clock to clock basis or can be internally or externally enabled or disabled on a clock to clock basis. These counters are in addition to the Loop and Program Counters of the Control Section.

Address Counter

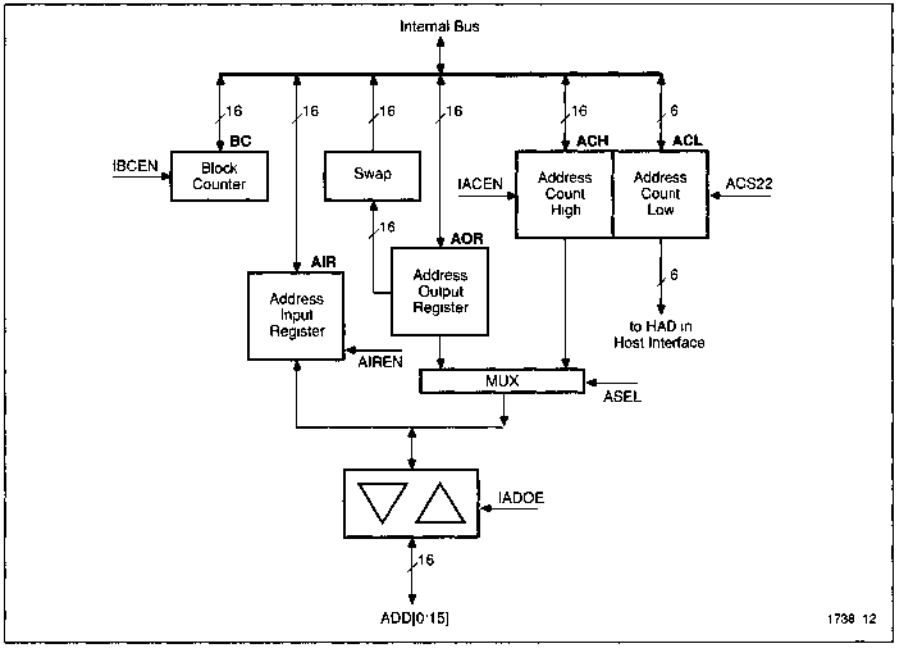
The Address Counter (AC), shown in Figure 12, is a 16- or 22-bit ascending counter that can be loaded or read by the CPU and enabled/disabled with the ACEN bit of the Control Register. (This control is also available externally through the I/01 pin; see I/O and Special Functions). While enabled, the counter will increment by one every rising edge of the clock.

The ACO flag indicates that the value of the counter is all ones. This flag stays latched until the counter is loaded with a new value. The counter will continue to count until disabled. ACO is a condition code and a member of a Case Group; see the Control Section description for more details. ACO can also generate an internal interrupt 7, if enabled.

In the 16-bit mode, the counter outputs (ACH) are available through the ADD bus. The count is gated to the ADD bus by setting the ASEL bit (CTRL9) of the Control Register.

In the 22-bit mode, the higher 16 bits (ACH) are available through the ADD bus and the six low order bits (ACL) are available through the Host Address (HAD) bus. These low order bits are multiplexed with the host address lines. The address lines from the host which drives the HAD bus must be placed in the high impedance state before the lower 6-bits (ACL) of the Address Counter can be read.

Figure 12. Address and Block Counter



Counters (Con't)

Selecting the 16- or 22-bit count mode is performed by setting or resetting the ACS22 bit in the I/O Configuration Register.

The address Output Register is an alternate source of address outputs; it is selected by resetting the ASEL bit of the Control Register. In this mode the CPU can be used to provide address generation and the Address Counter can be used as an event counter.

Block Counter

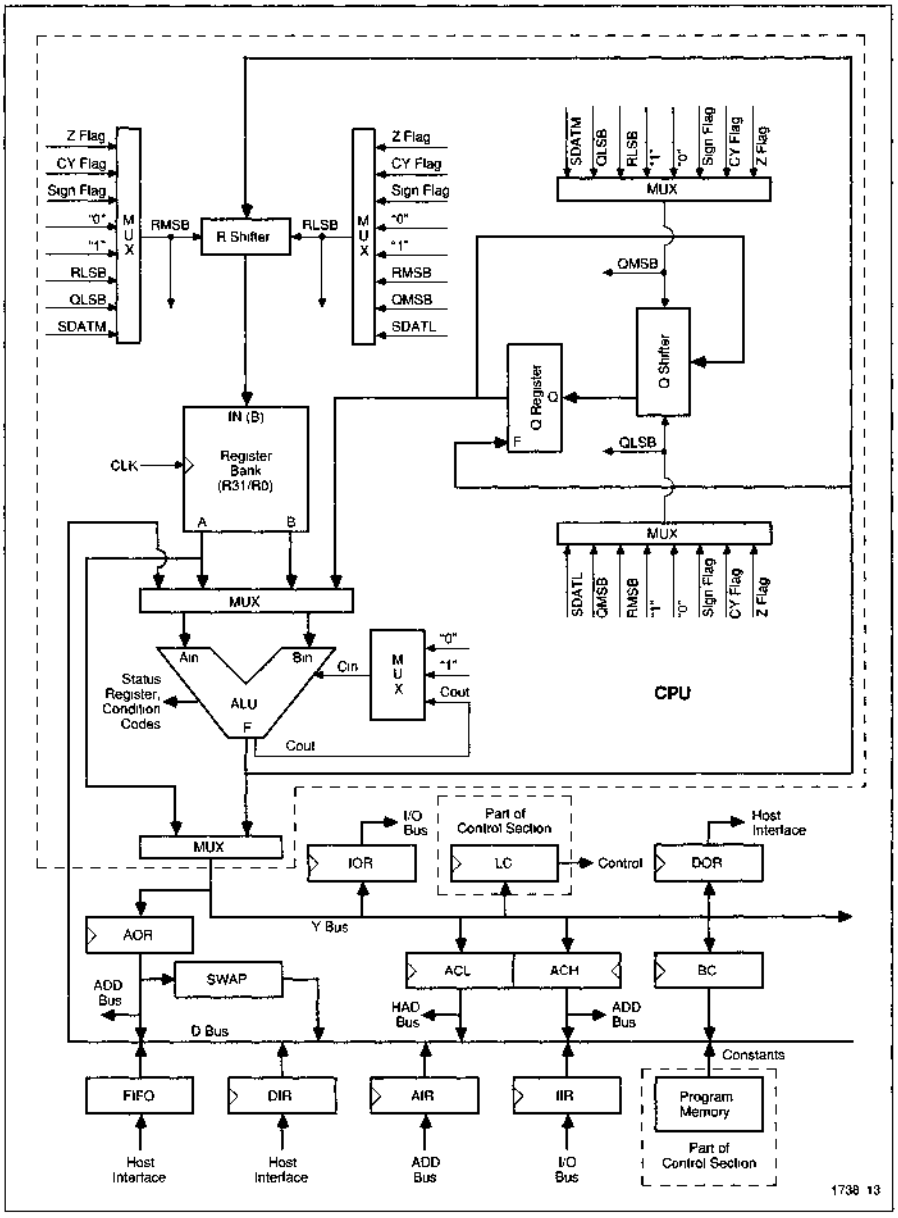
The Block Counter (BC) is a 16-bit down counter. It is enabled by the BCEN bit of the Control Register. It is useful as a counter for DMA transfers. The BCEN signal is (optionally) available externally through the I/O0 bit (see I/O and Special Functions). While enabled, the counter will decrement by one every rising edge of the clock. The BCZ flag indicates that the counter reached the zero value. After the occurrence of an all 0s condition the Block Counter will continue down counting until disabled. The flag is latched and can be cleared by loading a new value into the Block Counter. BCZ is a condition code and a member of a Case Group; see the Control Section description for more details.

Both counters may be read without disabling the count operation and loaded via the CPU.

Central Processing Unit

The CPU, shown in Figure 13, performs 16-bit operations in a single clock cycle. It contains 33 general purpose registers (R0...R31, and Q). The Q register can be used in conjunction with any of the R0...R31 registers to perform double precision shift operations. The main building blocks are the register bank (R0...R31), Q register, ALU, Y-bus devices, and D-bus devices. The register bank supplies up to two 16-bit registers, one of which is always the destination register.

Figure 13. CPU Block Diagram



Central Processing Unit (Con't)

The ALU operates on up to two external operands that are selected by its input MUX. In every instruction, 1 of the 10 D-bus devices (AOR, SWAP, ACL, ACH, BC, FIFO, DIR, AIR, IIR, and Program Store) or a member of the register bank or the Q register outputs, can be selected as an operand source to the ALU. The possibilities are shown in Figure 14. During ALU operations, three options can be selected to provide the carry-in (Cin) input: 0, 1, or the previous latched carry-out (adequate for multiple precision operations).

The ALU's output or a selected register can be loaded into one of the seven Y-bus devices (IOR, AOR, LC, DOR, ACL, ACH, or BC) every instruction cycle. This can happen in parallel with the feedback path from the ALU's output that is directed either to the Q register or to the destination register of the register bank.

Figure 14. CPU Sources and Destinations

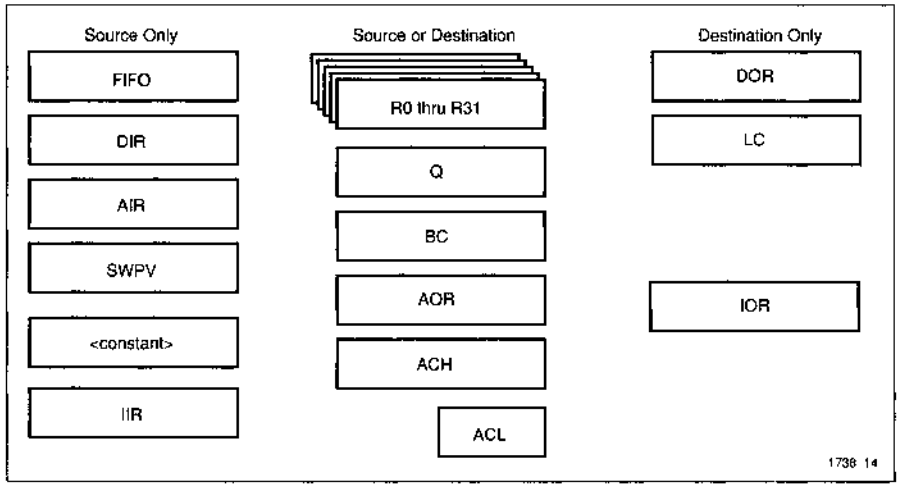


Table 6. CPU Operand Mnemonics

Mnemonic	Description
ACH or ACH/ACL	16- or 22-bit Auto-incrementing Counter, or General Purpose Registers
AIR	Address Input Register
AOR	Address Output Register
BC	Block Counter (16-bit auto-decrementing), or General Purpose Register
<constant>	Constant values in Program Storage
DIR	Data Input Register
DOR	Data Output Register
FIFO	Input Data from FIFO
IIR	I/O Input Register
IOR	I/O Output Register
LC	Program Loop Counter
Q	16-bit CPU Register
R0–R31	16-bit CPU Registers
SWPV	Byte Swap version of AOR

Central Processing Unit (Con't)

CPU operations can be performed on one, two or three operands. Each operation is performed in a single clock cycle. In two- or three-operand instructions, one of the operands must be a CPU internal register (R0...R31, or Q).

CPU operations are performed independently of operations in the counters, Host Interface, Output Control, and Program Control.

Arithmetic Operations

The CPU can perform the following arithmetic operations:

- Addition
- Subtraction
- Increment
- Decrement
- Compare

Logic Operations

The CPU can perform the following logic operations:

- AND
- OR
- Invert
- Exclusive OR
- Exclusive NOR

Shift Operations

Single shift operations, shown in Figure 15, can occur either to the left or to the right, with or without the Q register. Shift instructions specify the sources that are shifted into the corresponding registers.

All shift operations can be executed in the same clock cycle as an arithmetic or logic operation. The arithmetic or logic operation is executed first; the result is shifted and then stored in the register file. The shift can be either left or right.

The CPU can perform the following shift operations:

- Single-precision, left or right, within a general-purpose register (R0...R31, or Q).
- Double-precision, left or right, between an R0...R31 register and the Q register.

The LSB and MSB of the general-purpose registers are each fed by an eight-to-one multiplexer.

The sources and destinations for shift operation are given below:

Shift Right

Zero Flag (Z)

Carry Flag (CY)

Sign Flag (S)

Binary 0 (0)

Binary 1 (1)

Least-significant bit of this register (RLSB)

Least-significant bit of the Q register (QLSB)

Serial I/O port (SDATM)

Shift Left

Zero Flag (Z)

Carry Flag (CY)

Sign Flag (S)

Binary 0 (0)

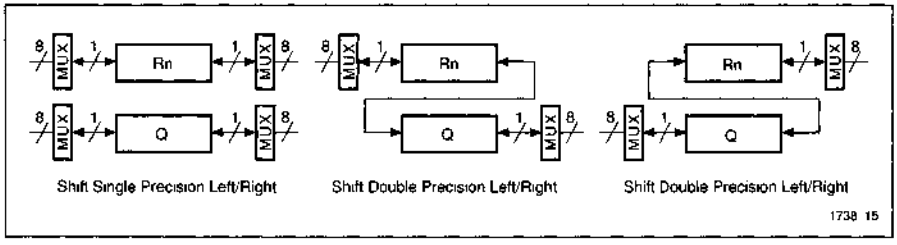
Binary 1 (1)

Most-significant bit of this register (RMSB)

Most-significant bit of the Q register (QMSB)

Serial I/O port (SDATL)

Figure 15. Shift Operations



Central Processing Unit (Con't)

Rotate Operations

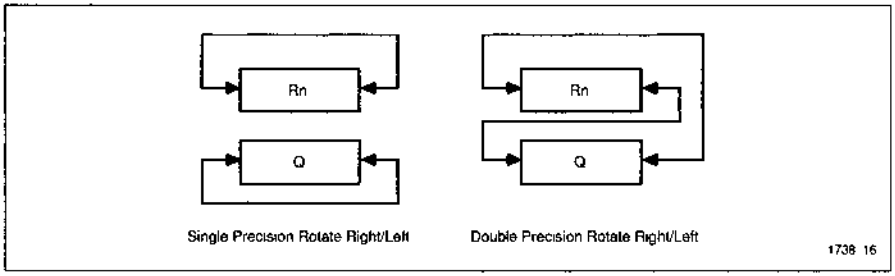
The CPU can perform the following rotate operations, as shown in Figure 16:

- Single-precision, left or right, within a general-purpose register (R0...R31, or Q).
- Double-precision, left or right, between an R0...R31 register and the Q register.

Multiple Precision Operations

The carry-out in each instruction can be used in the next instruction for multiple precision operations (e.g., ADDC). This feature enables the user to implement complex arithmetic operations such as division or multiplication in several clock cycles.

Figure 16. Rotate Operations

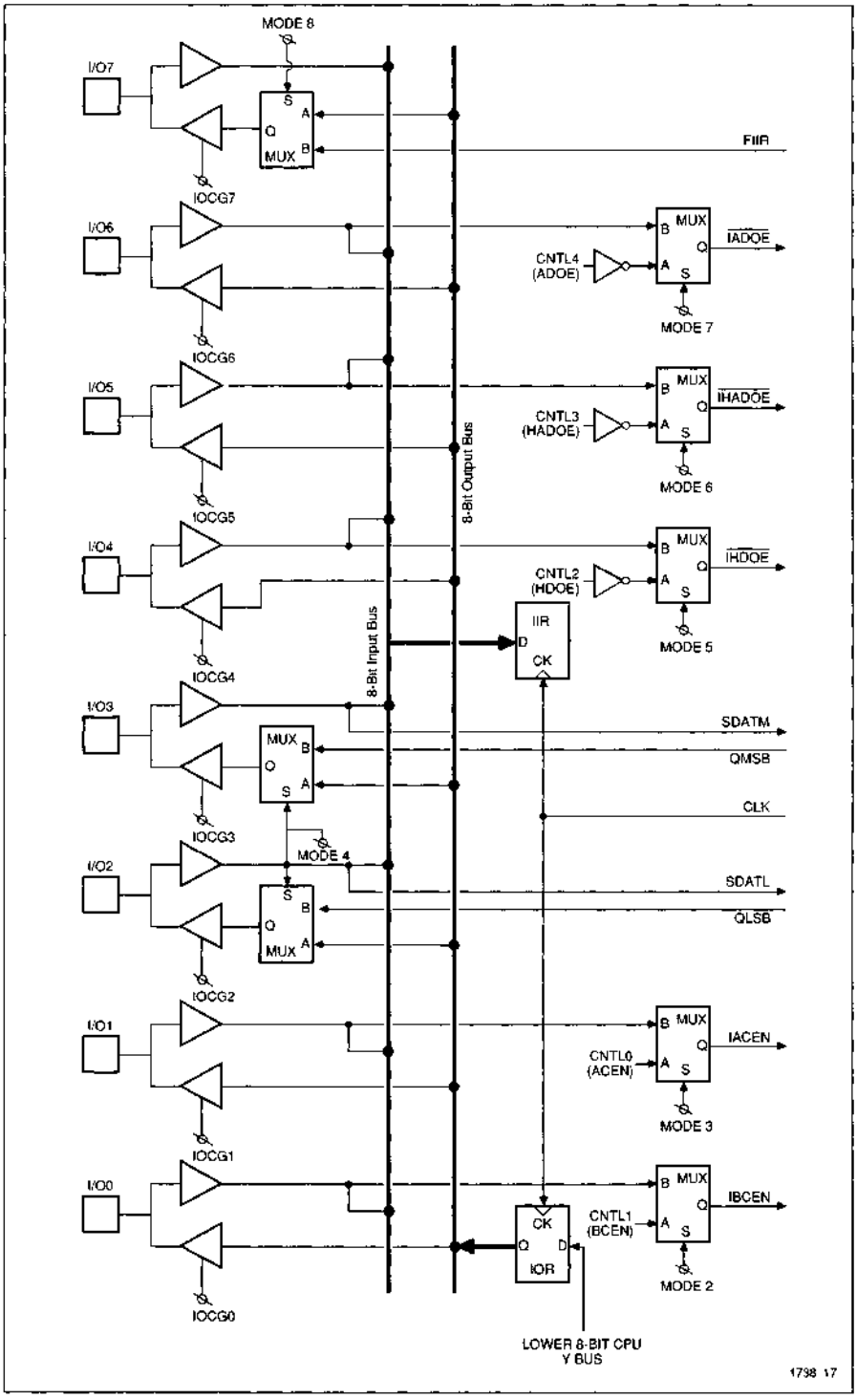


I/O and Special Functions

The I/O bus, shown in Figure 17, consists of eight lines which can be individually programmed as inputs or outputs. These lines can also be programmed to perform Special Functions. The functions of these pins are defined by the Mode Register and I/O Configuration Register (see Configuration Register Section). The I/O and Special Functions map according to the table. The I/O lines must first be configured as inputs or outputs via the I/O Configuration Register; the Special Function option can then be enabled via the Mode Register. Individual special function control is shown in the accompanying table.

Once a Special Function has been enabled, the corresponding internal control function is automatically disabled. Conversely, when a Special Function is disabled, control of the corresponding internal control function is returned to the Control Register (see Configuration Register). Because the Inputs in the I/O Register are clocked on each cycle, the status of the special function can also be read to the CPU.

Figure 17. I/O and Special Function Bus



Configuration Registers

The Configuration Registers allow the user to control and configure different operating modes of the PAC1000. The three 10-bit Configuration Registers are the Control Register, I/O Configuration Register, and Mode Register. Each register has an associated instruction which allows individual register bits to be modified.

Control Register

The Control Register, shown in Figure 18, provides for internal control of key functions within the PAC1000 . Several of these functions can alternatively be controlled externally through the I/O bus (see I/O and Special Functions). The Control Register is modified on the falling edge of the clock.

Table 7. I/O Pins and Special Functions

Pin	Special Function	Direction	Description
I/O7	FIIR	output	FIFO Input Ready. FIFO not full.
I/O6	ADOE	input	Address Output Enable
I/O5	HADOE	input	Host Address Output Enable
I/O4	HDOE	input	Host Data Output Enable
I/O3	QMSB	bidirectional	Q Register MSB
I/O2	QLSB	bidirectional	Q Register LSB
I/O1	ACEN	input	Address Counter Enable
I/O0	BCEN	input	Block Counter Enable

Table 8. Special-Function Control

Special Function	Pin Name	I/O Configuration	Mode
FIIR	I/O7	IOCG7=1 (output)	MODE8=1
ADOE	I/O6	IOCG6=0 (input)	MODE7=1
HADOE	I/O5	IOCG5=0 (input)	MODE6=1
HDOE	I/O4	IOCG4=0 (input)	MODE5=1
QMSB	I/O3	IOCG3=1 (output)	
		IOCG3=0 (input)	MODE4=1
QLSB	I/O2	IOCG2=1 (output)	
		IOCG2=0 (input)	MODE4=1
ACEN	I/O1	IOCG1=0 (input)	MODE3 =1
BCEN	I/O0	IOCG0=0 (input)	MODE2 =1

Configuration Registers (Con't)

ASEL (CTRL9)—*Address Select.* Selects the source that will write to the Address bus:

1= Address Counter.

0= Address Output Register (AOR).

AIREN (CTRL8)—*Address Input Register Enable.* Enables and disables writing to the Address Input Register from the ADD Port:

1= Enable writing to Address Input Register (AIR).

0= Disable writing to Address Input Register (AIR).

DIREN (CTRL7)—*Data Input Register Enable.* Enables and disables writing to the Data Input Register (DIR) from the HD Port:

1= Enable writing to Data Input Register (DIR).

0= Disable writing to Data Input Register (DIR).

HDSEL1 (CTRL6) and HDSEL0 (CTRL5)—*Host Data Select.* Select the source to be connected to Host Data (HD) bus:

HDSEL1 (CTRL6)	*HDSEL0 (CTRL5)*	*Selection*
0	0	FIFO—Peripheral Mode
0	1	Data Output Register
1	0	Status Register
1	1	Program Counter

ADOE (CTRL4)—*Address Output Enable.* Selects direction of Address bus (ADD) for next clock cycle:

1= Output (see ASEL).

0= Input (see AIREN).

HADOE (CTRL3)—*Host Address Output Enable.* Selects direction of Host Address (HAD) bus for next clock cycle:

1= Output (driven from ACL Register).

0= Input (into the FIFO).

HDOE (CTRL2)—*Host Data Output Enable.* Selects Direction of Host Data (HD) bus for next clock cycle:

1= Output (See HDSEL0 and HDSEL1).

0= Input (See DIREN).

BCEN (CTRL1)—*Block Counter Enable.* Enables and disables Block Counter:

1= Enable Counting on next rising clock edge.

0= Disable Counting on next rising edge.

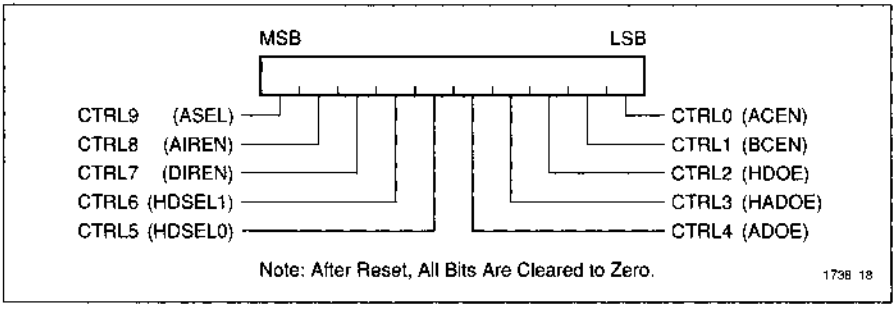
ACEN (CTRL0)—*Address Counter Enable.* Enables and disables Address Counter:

1= Enable Counting on next rising clock edge.

0= Disable Counting on next rising clock edge.

4

Figure 18. Control Register



Configuration Registers (Con't)

I/O Configuration Register

The I/O Configuration Register, shown in Figure 19, controls the direction of the individual lines of the I/O bus as well as configuring the Address Counter. Each I/O pin can be configured independently to be a general purpose input or output, or each can serve a special function (see I/O and Special Function). The I/O Configuration Register is also used to configure the Address Counter as a 16-bit counter with a maximum count of FFFFH or as a 22-bit counter with a maximum count of 3FFFFFH. The I/O Configuration Register is modified on the falling edge of the clock.

ACS22 (IOCG9)—Configures Address Counter as a 22- or 16-bit counter:

1= 22-bit counter.

0= 16-bit counter.

I/O7 (IOCG7)—Selects direction of I/O7 pin:

1= Output.

0= Input.

I/O6 (IOCG6)—Selects direction of I/O6 pin:

1= Output.

0= Input.

I/O5 (IOCG5)—Selects direction of I/O5 pin:

1= Output.

0= Input.

I/O4 (IOCG4)—Selects direction of I/O4 pin:

1= Output.

0= Input.

I/O3 (IOCG3)—Selects direction of I/O3 pin:

1= Output.

0= Input.

I/O2 (IOCG2)—Selects direction of I/O2 pin:

1= Output.

0= Input.

I/O1 (IOCG1)—Selects direction of I/O1 pin:

1= Output.

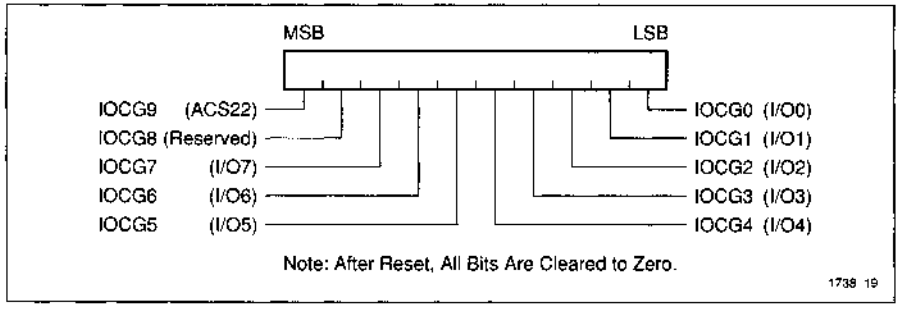
0= Input.

I/O0 (IOCG0)—Selects direction of I/O0 pin:

1= Output.

0= Input.

Figure 19. I/O Configuration Register



Configuration Registers (Con't)

Mode Register

The Mode Register, shown in Figure 20, allows the user to externally control and monitor key elements within the PAC1000 which would (alternatively) be controlled internally through the Control Register. Enabling a Special Function in the Mode Register disables the corresponding function in the Control Register. The Special Function input pins are shared with the general purpose I/O pins. The direction of the appropriate pin must be set in the I/O Configuration Register prior to programming the Mode Register.

The Mode Register can also be used to reset the FIFO as well as program the interrupt controller to generate either interrupts or Priority Test Conditions. See the discussion on "Priority Case" in the *Condition Code* section, above.

After Reset, all Mode Register bits equal zero. The Mode Register is modified on the falling edge of the clock.

The use of the Mode Register and I/O Configuration register for Special Functions is shown in the Special Function Settings table.

FIRST (MODE9)—*FIFO Reset.* (If held high, FIFO cannot receive information):

1= Initiate FIFO Reset (FIRST).

0= Complete FIFO Reset (FINRST).

FIIR (MODE8)—*FIFO Input Ready:*

1= I/O7 becomes output for the FIFO Input Ready (FIIR) flag.

0= I/O7 becomes general purpose I/O (IO7).

ADOE (MODE7)—*Address Output Enable:*

1= I/O6 becomes input for the Address Output Enable (AOE).

0= I/O6 becomes general purpose I/O (IO6).

HADOE (MODE6)—*Host Address Output Enable:*

1= I/O5 becomes input for Host Address Output Enable (HADOE).

0= I/O5 becomes general purpose I/O (IO6).

HDOE (MODE5)—*Host Data Output Enable:*

1= I/O4 becomes input for Host Data bus Output Enable HDOE).

0= I/O4 becomes general purpose I/O (IO4).

SIOEN (MODE4)—*Serial I/O Enable:*

1= I/O3 and I/O2 become MSB and LSB (respectively) of the CPU's Q register (SIO).

0= I/O3 and I/O2 become general purpose I/O ACEN(MODE3).

ACEN (MODE3)—*Address Counter Enable:*

1= I/O1 becomes input for Address Counter Enable (ACEN).

0= I/O1 becomes general purpose I/O.

BCEN (MODE2)—*Block Counter Enable:*

1= I/O0 becomes input for Block Counter Enable (BCEN).

0= I/O0 becomes general purpose I/O.

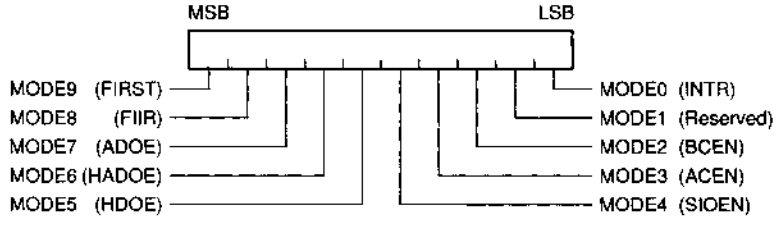
Reserved (MODE1)

INTR (MODE0)—*Interrupt/Priority-Case Mode:*

1= Select Interrupt mode (INTR).

0= Selects Priority Case mode (PCC).

Figure 20. Mode Register



Note: After Reset, All Bits Are Cleared to Zero.

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State Following Reset

Whenever the PAC1000 $\overline{\text{RESET}}$ input is driven low for at least two processor clocks, the chip goes through reset. The next two tables describe the PAC1000 signal and internal register states following reset.

Table 9. Special Function Settings

Mode Bit	I/O Configuration Bit	Function
MODE8=1	IOCG7=1	FIIR flag output on I/O7
MODE7=1	IOCG6=0	$\overline{\text{ADOE}}$ provided by I/O6
MODE6=1	IOCG5=0	$\overline{\text{HADOE}}$ provided by I/O5
MODE5=1	IOCG4=0	$\overline{\text{HDOE}}$ provided by I/O4
MODE4=1	IOCG3=1	MSB of Q register output on I/O3
MODE4=1	IOCG3=0	I/O3 can be shifted into MSB of Q register or destination register
MODE4=1	IOCG2=1	LSB of Q register output on I/O2
MODE4=1	IOCG2=0	I/O2 can be shifted into LSB of Q register or destination register
MODE3=1	IOCG1=0	ACEN provided by I/O1
MODE2=1	IOCG0=0	BCEN provided by I/O0

Table 10. Signal States Following Reset

Signal	Condition
HAD[5:0]	Input
HD[15:0]	Input
IO[7:0]	Input
ADD[15:0]	Input
OC[15:0]	0000H

Table 11. Internal States Following Reset

Component	Contents
ACH Register	0
ACL Register	0
AOR Register	0
AIR Register	0
DOR Register	0
DIR Register	0
IOR Register	0
IIR Register	0
STATUS Register	0
I/O Configuration Register	0
CONTROL Register	0
Breakpoint Register	0
Mode Register	0
PC Register (Program Counter)	0
MASK Register	011111111B
BC Register	FFFFH
R31–R0 Registers	Unknown
Q Register	Unknown
LC Register	Unknown
FIFO Locations	Unknown
FIFO Flags	Empty

Electrical and Timing Specifications

Table 12. Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Voltage to any pin with respect to GND	–0.6V to +7V
V_{PP} with respect to GND	–0.6 V to +14.0V
ESD Protection	>2000V

Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Table 13. Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	+5V ± 5%
Industrial	–40°C to +85°C	+5V ± 10%
Military	–55°C to +125°C	+5V ± 10%

Table 14. DC Characteristics

Over operating range with $V_{PP}=V_{CC}$

Parameter	Symbol	Test Conditions	Min	Max	Units
Output Low Voltage	V_{OL}	I_{OL}=8 mA		0.4	V
Output High Voltage	V_{OH}	I_{OH}=–4 mA	2.4		V
V_{CC} Standby Current CMOS	I_{SB1}	note 1		65	mA
V_{CC} Standby Current TTL	I_{SB2}	note 2		65	mA
Active Current (CMOS)	I_{CC1}	notes 1, 3			
—Commercial				80	mA
—Military				90	mA
Active Current	I_{CC2}	notes 2, 3			
—Commercial				110	mA
—Military				120	mA
V_{PP} Supply Current	I_{PP}	$V_{PP}=V_{CC}$		100	µA
V_{PP} Read Voltage	V_{PP}	notes 1, 2	V_{CC}–0.4	V_{CC}	V
Input Load Current	I_{LI}	V_{IN}=5.5V or GND	–10	10	µA
Output Leakage Current	I_{LO}	V_{OUT}=5.5V or GND	–10	10	µA

Notes:
1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3. Active current is an AC test and uses AC timing levels.

Table 15. AC Timing Levels

Inputs:	0 to 3V Reference 1.5V
Outputs:	0.4 to 2.4V

Table 16. AC Characteristics

Parameter	Symbol	12MHz[1] Min	12MHz[1] Max	16MHz[1] Min	16MHz[1] Max	20MHz[2] Min	20MHz[2] Max
CLOCK CYCLE							
Cycle Time	t_{CK}	84		62.5		50	
Clock Pulse Width High	t_{CKH}	26		24		21	
Clock Pulse Width Low	t_{CKL}	26		24		21	
HOST READ CYCLE							
Read Cycle Time	t_{RC}	50		40		30	
Address to Data Valid	t_{ACC}		45		35		30
$\overline{CS}$ to Data Valid	t_{CS}		45		35		30
$\overline{CS}$ to tristate	t_{CSZ}	0	45	0	35	0	30
HOST WRITE CYCLE							
Pulse width of $\overline{CS}$ and $\overline{WR}$ LOW	t_{PWL}	20		15		15	
Pulse width of $\overline{CS}$ and $\overline{WR}$ High	t_{PWH}	15		10		10	
Data setup to $\overline{WR}$	t_{SD}	10		10		5	
Data hold to $\overline{WR}$	t_{HD}	10		10		5	
RESET CYCLE							
$\overline{RESET}$ setup	t_{SR}	10		10		5	
$\overline{RESET}$ to tristate of ADD, HAD, HD, I/O	t_{RZ}	25		25		20	
$\overline{RESET}$ clocked to OUTCNTL low	t_{ROL}	30		30		25	
ADDRESS TIMING							
Address/Data setup	t_{SADD}	10		10		10	
Address/Data hold	t_{HADD}	8		8		5	
Clocked Counter to Address output	t_{CADD}		43		35		30
Clocked Address Register to Address	t_{RADD}		43		35		30
ADOE enable to data valid	t_{ADOE}		50		40		30
HADOE enable to data valid	t_{HADOE}		50		40		30
Address output disable	t_{CKZ}	0	25	20		0	16

Table 16. AC Characteristics (Con't)

Parameter	Symbol	12MHz[1] Min	12MHz[1] Max	16MHz[1] Min	16MHz[1] Max	20MHz[2] Min	20MHz[2] Max
DATA AND I/O TIMING							
Clock to I/O Output Valid	t_{CKIO}		35		30		30
Clock to HD Output	t_{CKHD}		35		30		30
IO data setup	t_{SIO}	10		10		10	
IO data hold	t_{HIO}	8		8		5	
HD data setup	t_{SHD}	10		10		10	
HD data hold	t_{HHD}	8		8		5	
HDOE enable to data valid	t_{HDOE}		50		40		30
Bus Output Disable	t_{CKZ}	0	25	0	20	0	16
TEST AND INTERRUPT TIMING							
Condition Code setup	t_{SCC}	60		50		40	
Condition Code hold	t_{HCC}	0		0		0	
Clock to OUTCNTL Valid	t_{COV}		33		33		25
Minimum interrupt pulse for acceptance	t_{IPWA}	15		10		10	
SPECIAL FUNCTION TIMING (I/O Bus)							
SQ15 setup	t_{SSQ15}	15		10		10	
SQ15 hold	t_{HSQ15}	0		0		0	
SQ0 setup	t_{SSQ0}	15		10		10	
SQ0 hold	t_{HSQ0}	0		0		0	
Clock to Q0 output	t_{CKQ0}		35		30		30
Clock to Q15 output	t_{CKQ15}		35		30		30
Address Counter enable setup	t_{SACEN}	20		15		10	
Address Counter enable hold	t_{HACEN}	10		5		5	
Block Counter enable setup	t_{SBCEN}	20		15		10	
Block Counter enable hold	t_{HBCEN}	10		5		5	
External output enable to data valid	t_{SFV}		30		25		20
External output enable to high impedance	t_{SFZ}		30		25		20

Notes:
1. Operating temperature range: Commercial, Industrial, Military
2. Operating temperature range: Commercial

Figure 21. Clock Cycle Timing

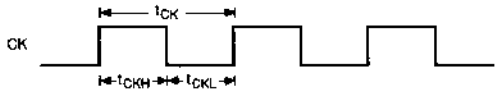


Figure 22. Host Read Cycle Timing

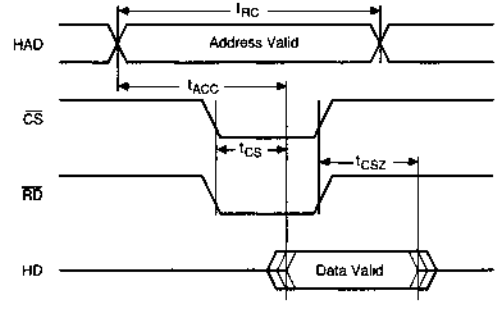


Figure 23. Host Write FIFO Cycle Timing

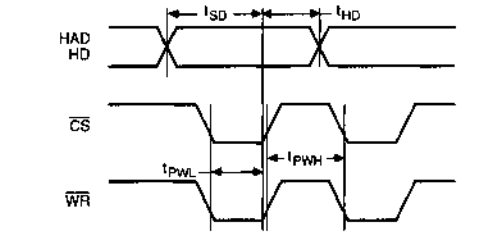


Figure 24. Reset Cycle Timing

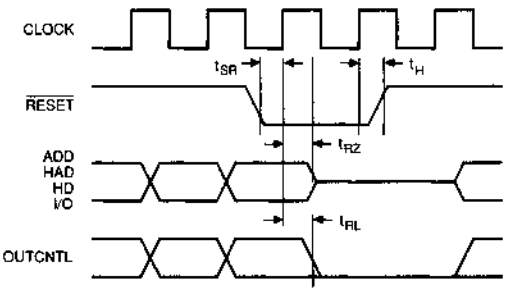
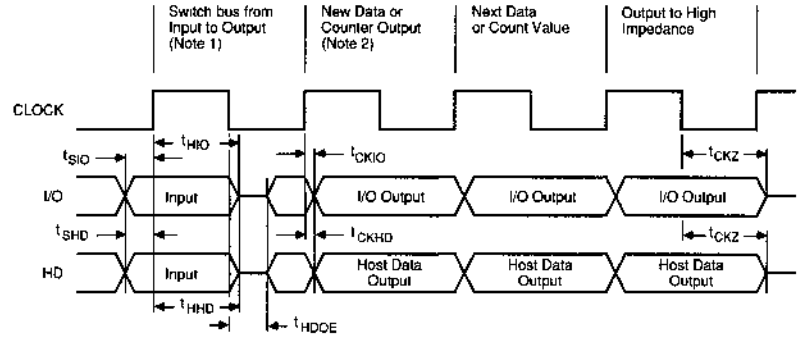


Figure 25. Data and I/O Timing



Notes: 1. A bus directional change (input-to-output or output-to-input) takes place on the falling edge of the clock
2. New data or count value is latched on the rising edge of the clock

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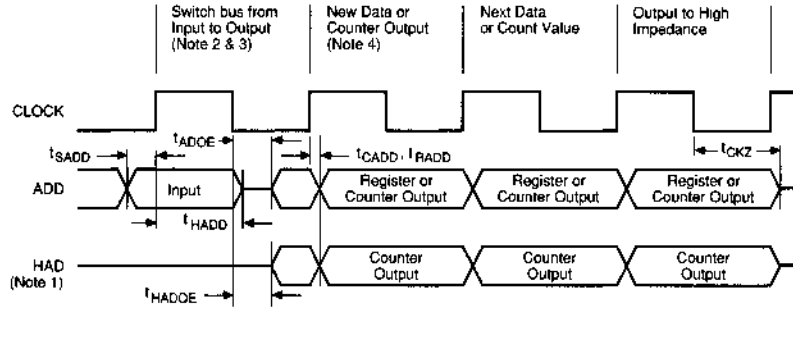
Figure 26. Address Timing



Notes: 1 The Host Address (HAD) bus is used to output the lower six bits of the 22-bit counter
2. A bus directional change takes place on the falling edge of the clock (input-to-output or output-to-input)
3. Selection of the source to be output on a bus occurs on the falling edge of the clock (i.e., counter or address register)
4. New data or count value is latched on the rising edge of the clock.

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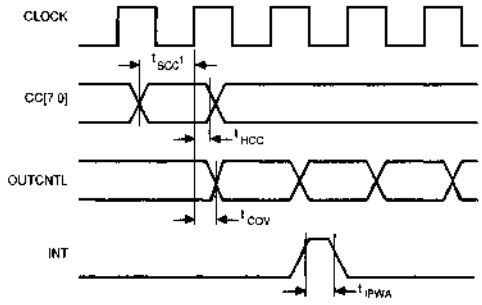
Figure 27. Test and Interrupt Timing



Note: 1. Since condition codes are not latched, they should be stable t_{SCC} prior to being tested.

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Figure 28. Special Function Timing

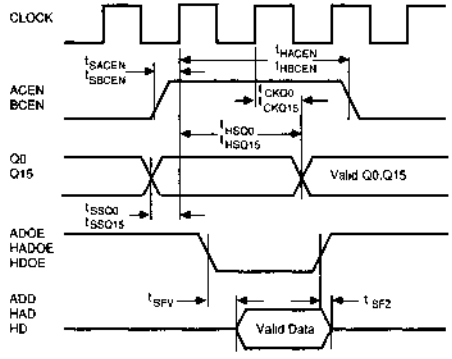

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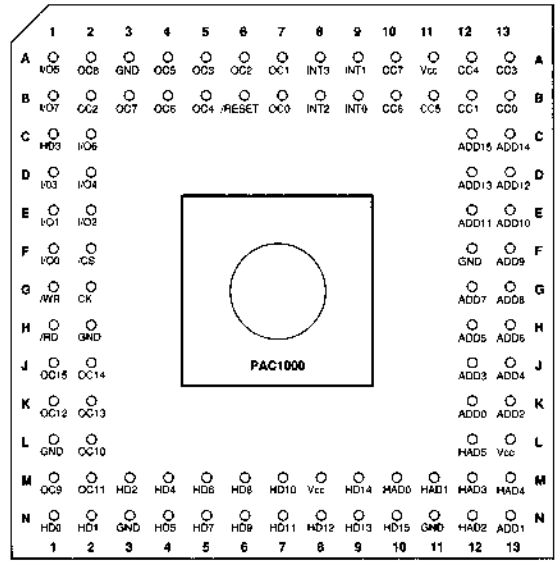
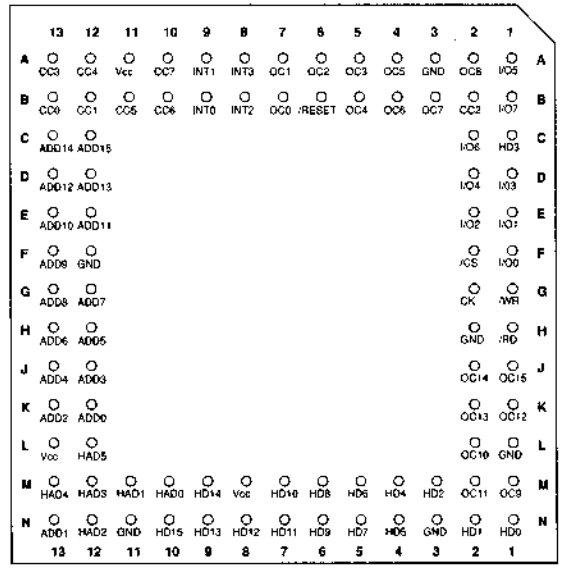
Figure 29. 88-Pin Ceramic PGA Pin Assignments



TOP (THROUGH PACKAGE) VIEW



BOTTOM VIEW

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Table 17. PGA Pin Assignments

Name	Pin	Name	Pin	Name	Pin
$\overline{CS}$	F2	GND	H2	I/O0	F1
$\overline{RD}$	H1	GND	L1	I/O1	E1
$\overline{RESET}$	B6	GND	A3	I/O2	E2
$\overline{WR}$	G1	GND	F12	I/O3	D1
ADD0	K12	GND	N3	I/O4	D2
ADD1	N13	GND	N11	I/O5	A1
ADD10	E13	HAD0	M10	I/O6	C2
ADD11	E12	HAD1	M11	I/O7	B1
ADD12	D13	HAD2	N12	INT0	B9
ADD13	D12	HAD3	M12	INT1	A9
ADD14	C13	HAD4	M13	INT2	B8
ADD15	C12	HAD5	L12	INT3	A8
ADD2	K13	HD0	N1	OC0	B7
ADD3	J12	HD1	N2	OC1	A7
ADD4	J13	HD10	M7	OC10	L2
ADD5	H12	HD11	N7	OC11	M2
ADD6	H13	HD12	N8	OC12	K1
ADD7	G12	HD13	N9	OC13	K2
ADD8	G13	HD14	M9	OC14	J2
ADD9	F13	HD15	N10	OC15	J1
CC0	B13	HD2	M3	OC2	A6
CC1	B12	HD3	C1	OC3	A5
CC2	B2	HD4	M4	OC4	B5
CC3	A13	HD5	N4	OC5	A4
CC4	A12	HD6	M5	OC6	B4
CC5	B11	HD7	N5	OC7	B3
CC6	B10	HD8	M6	OC8	A2
CC7	A10	HD9	N6	OC9	M1
CK	G2			VCC	A11
				VCC	L13
				VCC	M8

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Figure 30. 100-Pin Plastic or Ceramic Quad Flatpack (Gullwing) Pin Assignments

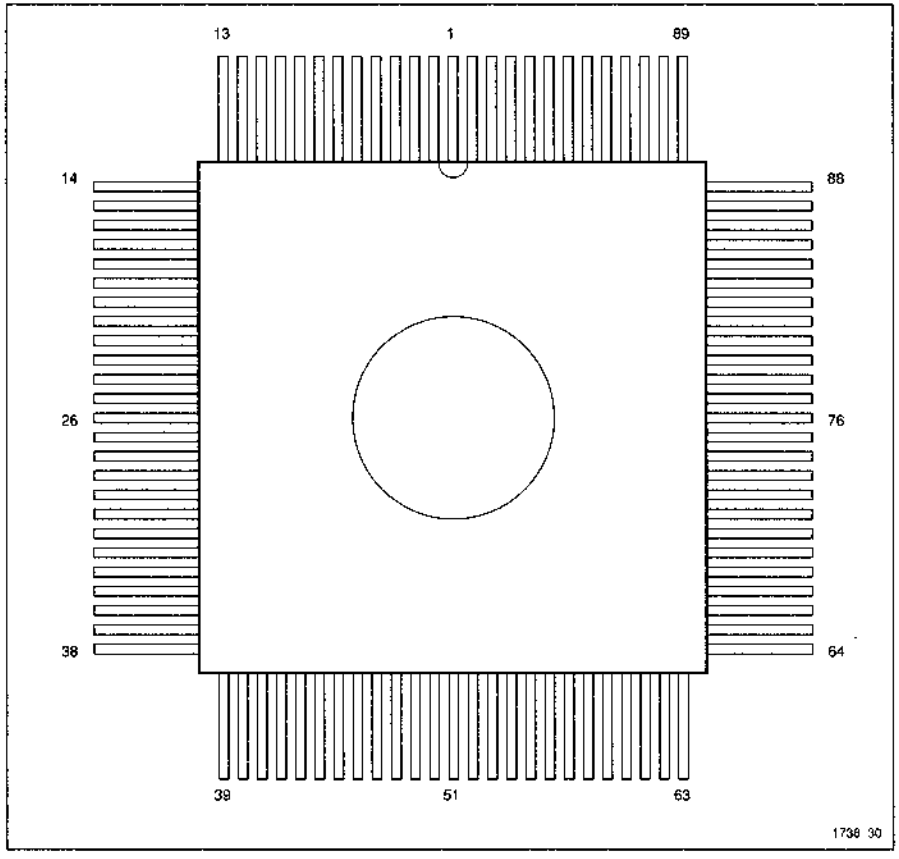


Table 18. Plastic or Ceramic Quad Flatpack (Gullwing) Pin Assignments

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	$\overline{RD}$	26	HD11	51	ADD7	76	OC1
2	GND	27	HD12	52	ADD8	77	OC2
3	GND	28	VCC	53	ADD9	78	$\overline{RESET}$
4	OC15	29	VCC	54	GND	79	N/C
5	OC14	30	HD13	55	GND	80	OC3
6	OC12	31	HD14	56	ADD10	81	OC4
7	OC13	32	HD15	57	ADD11	82	OC5
8	GND	33	HAD0	58	ADD12	83	OC6
9	GND	34	GND	59	ADD13	84	GND
10	OC10	35	GND	60	ADD14	85	GND
11	OC9	36	HAD1	61	ADD15	86	OC7
12	OC11	37	HAD2	62	CC0	87	OC8
13	N/C	38	N/C	63	CC1	88	CC2
14	HD0	39	HAD3	64	CC3	89	IO5
15	HD1	40	ADD1	65	CC4	90	IO7
16	HD2	41	HAD4	66	CC5	91	IO6
17	GND	42	HAD5	67	VCC	92	HD3
18	GND	43	VCC	68	VCC	93	IO4
19	HD4	44	VCC	69	CC6	94	IO3
20	HD5	45	ADD0	70	CC7	95	IO2
21	HD6	46	ADD2	71	INT0	96	IO1
22	HD7	47	ADD3	72	INT1	97	$\overline{CS}$
23	HD8	48	ADD4	73	INT2	98	IO0
24	HD9	49	ADD5	74	INT3	99	CK
25	HD10	50	ADD6	75	OC0	100	$\overline{WR}$

Instruction Set Overview

The PAC1000 architecture can perform three operations simultaneously in each instruction cycle. The operations are specified in the System Entry Language (PACSEL) using a single statement. PACSEL instructions can perform three operations:

- Program Control (PROGCNTL)
- CPU
- Output Control (OUTCNTL)

Each *instruction* is executed in a single cycle; the three *operations* are executed in parallel.

The syntax of a PACSEL statement has a label and three components:

```
[label:] PROGCNTL, CPU,
OUTCNTL;
```

The PROGCNTL component determines program flow and determines the next statement to be executed; the CPU component determines which operation is to be performed by the CPU; the OUTCNTL component determines the state of the control outputs.

A comma (,) is used to separate the instructions and a semi-colon marks the end of a statement. In general, each statement is executed in a single cycle.

In PACSEL statements, the PROGCNTL, CPU, OUTCNTL components can come in any order or any combination of Macro or Assembler operators. That is, you may mix Assembler operators among Macro operators. Tables at the end of this section summarize the Macro and Assembler operators.

In some cases, the same mnemonic is used to specify identical operations in both Macro and Assembler level.

You may:

- Specify all the components in the same statement in order to perform the operations in parallel:

  ```
  PROGCNTL, CPU, OUTCNTL;
  ```

- Specify components one at a time:

  ```
  CPU;
  PROGCNTL;
  OUTCNTL;
  ```

- Use components in any combination:

  ```
  PROGCNTL, CPU;
  PROGCNTL, OUTCNTL;
  CPU, OUTCNTL;
  ```

WSI recommends that, in general, you maintain a consistent ordering of these components and consistent groupings of Assembler-level and Macro operators, e.g. in separate files. This manual uses the PROGCNTL, CPU, OUTCNTL ordering.

When PROGCNTL is omitted, the implied instruction is CONTinue, that is, proceed to the next control instruction. When CPU is omitted, the implied instruction is NOP. When OUTCNTL is omitted, the implied instruction is MAINTain, that is, maintain the most recent OUTCTL, in Assembler order.

A summary of PACSEL Assembler and Macro statements follows.

Table 19. PACSEL Assembler Language Summary

Mnemonic	Arguments	Meaning
The PROGCNTL Operators		
ACSIZE	<16/22>	SET A COUNTER SIZE
CALL	<LABEL | LCPTR | FIFO>	UNCOND BRANCH SUBRTN
CALLC	<COND> <LABEL | FIFO>	COND BRANCH SUBRTN
CALLNC	<COND> <LABEL | FIFO>	INV COND BRANCH SUBRTN
CCASE	<CG> <VALUE>	BRANCH SUBRTN CASEBLK
CLI	<MASK>	CLEAR INTERRUPT
CONT(D)		CONTINUE
CPI	<VALUE>	PRIORITIZED SUB RTN
DI	<MASK>	DISABLE INTERRUPT
DSS		DISABLE SINGLE STEP MODE
EI	<MASK>	ENABLE INTERRUPT
ESS		ENABLE SINGLE STEP MODE
JCase	<CG> <VALUE>	UNCOND BRANCH CaseBLK
JMP	<LABEL | LCPTR | FIFO>	UNCONDITIONAL BRANCH
JMPC	<COND> <LABEL | FIFO>	CONDITIONAL BRANCH
JMPNC	<COND> <LABEL | FIFO>	INVERT COND BRANCH
JPI	<VALUE>	PRIORITIZED BRANCH
LDBP	<VALUE>	LOAD BP REG
LDBPD		LOAD BP COMP VALUE
LDLC	<VALUE>	LOAD COUNTER
LDLCD		LOAD CTR COMPUTED VAL
LOOPNZ	<LABEL>	REPEAT BRANCH,CNTRNZ
PLDLC	<VALUE>	PUSH VALUE & LDCTR
PLDLCD		PUSH VAL&LDCTR CM VL
POP		POP STACK
POPLC		POP STACK TO CNTR
PUSHLC		PUSH CNTR
RESTART		BRANCH TO 0
RET		RETURN
RC	<COND>	CONDITIONAL RETURN
RNC	<COND>	INV COND RETURN
RSTCON	<MASK>	RESET CONTROL REG
RSTIO	<MASK>	RESET I/O CONFIG REG
RSTMODE	<MASK>	RESET MODE REG
SETCON	<MASK>	SET CONTROL REG
SETIO	<MASK>	SET I/O CONFIG REG
SETMODE	<MASK>	SET MODE REG

Table 19. PACSEL Assembler Language Summary (Con't)

Mnemonic	Arguments	Meaning
The CPU Operators		
ADC	<ARG1> <ARG2> [<ARG3>]	ADD WITH CARRY
ADD	<ARG1> <ARG2> [<ARG3>]	ADD
AND	<ARG1> <ARG2> [<ARG3>]	BITWISE AND
CMP	<ARG1> <ARG2>	COMPARE
DEC	<ARG1> [<ARG2>]	DECREMENT
INC	<ARG1> [<ARG2>]	INCREMENT
INV	<ARG1> [<ARG2>]	INVERT
MOV	<DEST> <SRC>	MOVE SRC TODEST
NOP(D)		NO OPERATION
OR	<ARG1> <ARG2> [<ARG3>]	BITWISE OR
RDFIFO		READ FIFO DATA TO REG
SBC	<ARG1> <ARG2> [<ARG3>]	SUB WITH CARRY
SHLRQ	<REG> <RARG> <QARG>	SHIFT LEFT REG & Q
SHLR	<REG> <RARG>	SHIFT LEFT REG
SHRRQ	<REG> <RARG> <QARG>	SHIFT RIGHT REG & Q
SHRR	<REG> <RARG>	SHIFT RIGHT REG
SUB	<ARG1> <ARG2> [<ARG3>]	SUBTRACT
XOR	<ARG1> <ARG2> [<ARG3>]	EXCLUSIVE OR
XNOR	<ARG1> <ARG2> [<ARG3>]	EXCLUSIVE NOR
The MACRO Operators		
DIV	<ARG1> <ARG2> <ARG3>	DIVISION
MUL	<ARG1> <ARG2> <ARG3>	2'S COMP MULTIPLY
The OUTCNTL Operators		
MAINT(D)		MAINTAIN PREV VALUE
OUT	<VALUE>	OUTPUT

Table 20. PACSEL Macro Language Summary

The PROGCNTL Operators

```
ACSIZE <16/22>
CALL <label | LCPTR | FIFO> [ON] [NOT] [<cond>]
CASE n, PROGCNTL, CPU, OUTCNTL;
CLEAR <int level> [...<int level>]
CONFIGURE <pm1> [<pm2>...<pm10>]
CONT
DISABLE <int level> [<int level>...<int level>]
ELSE
ENABLE <int level> [<int level>...<int level>]
ENDFOR
ENDIF
ENDPSWITCH
ENDSWITCH
ENDWHILE
FOR <value>
GOTO <label | LCPTR | FIFO> [ON] [NOT] [<cond>]
IF [NOT] <cond>
INPUT <i/o pin> [<i/o pin>...<i/o pin>]
LOADBP <value>
OUTPUT <i/o pin> [<i/o pin>...<i/o pin>]
PRIORITY m, PROGCNTL, CPU, OUTCNTL;
PSWITCH
RESET <p1> [<p2>...<p10>]
RETURN [ON] [NOT] [<cond>]
SET <p1> [<p2>...<p10>]
SWITCH <case group>
WHILE [NOT] <cond>
```

4

Table 20. PACSEL Macro Language Summary (Con't)

The CPU-Operator Assignment

```
move
    <dest> := <src>
arithmetic expression
    <dest> := <arg1> <+/-> <arg2> <+/-> <arg3>
logical expression
    <dest> := <arg1> <logical operator> <arg3>
increment, decrement, invert, unary minus
    <dest> := <opr> <src>
macro expression
    <dest> := <arg1> [* | /] <arg2>
shift RAM
    <Rx> = Rx <shft opr> <shft arg>
shift RAM and q
    <QRx> = Q <shft opr> <shft arg> Rx <shft opr> <shft arg>
```

The OUTCNTL Operator

```
OUT <arg1> [<arg2>...<arg16>]
```

System Development Tools

PAC1000 System Development Tools are a complete set of PC-based development tools. They provide an integrated easy-to-use software and hardware environment to support PAC1000 development and programming.

The tools run on an IBM-XT, AT, PS2 or compatible computer running MS-DOS version 3.1 or later. The system must be equipped with 640 Kbytes of RAM and a hard disk.

Hardware

The PAC1000 System Programming Hardware consists of:

- WS6000 MagicPro Memory and PSD Programmer (XT, AT only)
- Package Adaptors (88-Pin Ceramic Pin-Grid Array and 100-Pin Ceramic Quad Flatpack—Gullwing) for the MagicPro Remote Socket Adaptor Unit

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of the IBM-PC plug-in Programmer Board and the Remote Socket Adaptor Unit.

Software

The PAC1000 System Development Software consists of the following:

- WISPER Software—PSD Software Interface
- IMPACT Software—Interface Manager for PAC1000
- PACSEL Software—System Entry Language
- PACSIM Software—Functional Simulator
- PACPRO Software—Device Programming Software

WISPER and IMPACT software provide a menu-driven user interface enabling other tools to be easily invoked by the user.

The system design is entered into PACSEL source program files using an editor chosen by the user. PACSEL supports assembly-level and high-level Macro programming.

The PACSEL Assembler produces object code format in single or multiple modules, which are then linked by the PACSEL Linker into a single load file with a format suitable for PACSIM and PACPRO.

The PACSIM functional simulator enables the user to test and debug programs by examining the state of PAC1000 internal registers before and during a complete functional simulation of the device.

PACPRO software programs PAC1000 devices by using the MagicPro hardware and the socket adapter.

The programmed PAC1000 is then ready to be used.

Support

WSI provides a complete set of quality support services to registered owners. These support services include the following:

- 12-month Software Updates.
- Hotline to WSI Application Experts—For direct design assistance.
- 24-Hour Electronic Bulletin Board—For design assistance via dial-up modem.

Training

WSI provides in-depth, hands-on workshops for the PAC1000 and the System Development Tools. Workshop participants will learn how to develop and program their own high-performance microcontrollers. Workshops are held at the WSI facility in Fremont, California.

Ordering Information—PAC1000

Part Number	Speed (MHz)	Package Type	Package Drawing	Operating Temperature	Manufacturing Procedure
PAC1000-12F*	12	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Commercial	Standard
PAC1000-12FI*	12	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Industrial	Standard
PAC1000-12FM*	12	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Military	Standard
PAC1000-12FMB*	12	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Military	MIL-STD-883C
PAC1000-12Q*	12	100-Pin Plastic Quad Flatpack, Gullwing	Q1	Commercial	Standard
PAC1000-12X	12	88-Pin Ceramic Pin-Grid Array	X1	Commercial	Standard
PAC1000-12XI	12	88-Pin Ceramic Pin-Grid Array	X1	Industrial	Standard
PAC1000-12XM	12	88-Pin Ceramic Pin-Grid Array	X1	Military	Standard
PAC1000-12XMB	12	88-Pin Ceramic Pin-Grid Array	X1	Military	MIL-STD-883C
PAC1000-16F*	16	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Commercial	Standard
PAC1000-16FI*	16	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Industrial	Standard
PAC1000-16FM*	16	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Military	Standard
PAC1000-16FMB*	16	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Military	MIL-STD-883C
PAC1000-16Q*	16	100-Pin Plastic Quad Flatpack, Gullwing	Q1	Commercial	Standard
PAC1000-16X	16	88-Pin Ceramic Pin-Grid Array	X1	Commercial	Standard
PAC1000-16XI*	16	88-Pin Ceramic Pin-Grid Array	X1	Industrial	Standard
PAC1000-16XM*	16	88-Pin Ceramic Pin-Grid Array	X1	Military	Standard
PAC1000-16XMB*	16	88-Pin Ceramic Pin-Grid Array	X1	Military	MIL-STD-883C
PAC1000-20F*	20	100-Pin Ceramic Quad Flatpack, Gullwing	F3	Commercial	Standard
PAC1000-20X*	20	88-Pin Ceramic Pin-Grid Array	X1	Commercial	Standard
PAC1000-20Q*	20	100-Pin Plastic Quad Flatpack, Gullwing	Q1	Commercial	Standard

*: These products are advanced information.

Ordering Information—System Development Tools

Part Number	Contents
PAC1000-GOLD	WISPER Software IMPACT Software PACSEL Software PACSIM Software PACPRO Software User's Manual WSI-Support WS6000 MagicPro Programmer
PAC1000-SILVER	WISPER Software IMPACT Software PACSEL Software PACSIM Software PACPRO Software User's Manual WSI-Support
WS6000	MagicPro Programmer IBM PC plug-in Adaptor Card Remote Socket Adaptor
WS6010	88-Pin CPGA Adaptor Used with the WS6000 MagicPro Programmer
WS6012	100-Pin Ceramic Quad Flatpack (Gullwing) Adaptor Used with the WS6000 MagicPro Programmer
WSI-Support	Support Services, including: ❑ 12-month Software Update Service ❑ Hotline to WSI Application Experts ❑ 24-hour access to WSI Electronic Bulletin Board
WSI-Training	Workshops at WSI, Fremont, CA For details and scheduling, call PSD Marketing, (415) 656-5400

User-Configurable Microsequencer

Overview

In 1988 WSI introduced a new concept in programmable VLSI: the Programmable System™ Device (PSD). The PSD is defined as a family of *User-configurable system level building blocks on-a-chip enabling quick implementation of application specific controllers and peripherals.* The first generation PSD series includes the MAP168, a User-Configurable Peripheral with Memory; the SAM448, a User-Configurable Microsequencer; and the PAC1000, a User-Configurable Microcontroller.

The SAM448 is a microsequencer intended for use in digital systems that require events to be controlled at high speed. A microsequencer is basically an instruction oriented device executing one internal instruction on each system cycle. This can be done in a linear flow or the sequencer can test the state of logic inputs or internal events and respond to program branching on a result. In addition, it has the capability of driving output signals on a cycle by cycle basis.

The SAM448 can operate at a high clock speed (30 MHz) so sequential operations can be performed much faster than with lower end microcontrollers. A classic application of the SAM448 would be in the generation of pulse waveforms for video line and frame synchronization with blanking output controls for both line and frame flyback. The device could also control the load and shift activity in the video output registers and supervise the video memory address counters. All these activities are sequential in nature so microcode could be developed for the SAM device and programmed into the device's on-chip EPROM.

Prior to the development of the SAM448 Microsequencer, a designer would most likely develop a system from discrete EPROM or ROM plus 74LS TTL logic with dedicated LIFO and registers. The actual development of such a design would escalate in chip count to eventually cover an entire printed circuit card. With the advent of Programmable Logic Devices (PLDs), the development of a microsequencing circuit became simpler. However, a typical system still required five to six PLDs. In addition, and EPROM was needed to hold the microcode. Because microcode is usually rather wide, a number of EPROMs were needed.

The SAM448 provides the optimum solution when implementing a microsequencer of medium complexity. It has been designed to be cascadable in width and depth so more complex microsequencer designs may be achieved.

Microcode EPROM Architecture

The core of the SAM448 is a microcode EPROM organized as a 448 locations deep and 36 bits wide. On each clock cycle, the current 32 bit wide instruction is clocked into the pipeline register. The 32 bit word is split into a number of fields. The F field consists of 16 bits and drives the output lines as user defined output pins. The remaining 20 bits are subdivided into one 8-bit Q field which generally directs processing to the next address of the EPROM. The 8-bit D field can be used to hold a constant or direct value but it can also be used for next address generation. The OP field is three bits in width and contains the current instruction to be executed. The remaining field is the

Microcode EPROM Architecture (Cont.)

E field and performs a 3-State control function on the pipeline register. When HIGH, the output pins are enabled and when LOW the outputs are in a high impedance state. This feature enables one SAM448 device to share the same outputs with a second for vertical cascading.

The EPROM locations are connected such that the first 192 locations (0 to 191) are in a linear sequence. The remaining locations are organized in four rows of 192 to 255. This permits a one of four branch control. The internal branch control logic will make the decision as to which branch to take depending on the state of the user defined inputs and the value of the next state address.

Branch Control Logic

The branch control logic determines the location from where the next instruction will be fetched. The next address can come from the Q or D field of the instruction currently in the pipeline register, the top of the stack or LIFO or the Branch Select EPLD. The Branch Select EPLD can be programmed to view inputs or the logical combination of inputs to invoke a branch when a logic state becomes true.

Stack

The stack or Last In First Out (LIFO) memory is 15 locations deep and 8 bits wide and can be used to hold the value of a return address so successful CALL to and RETURN from subroutines may be invoked. A loop counter is included in the SAM448 architecture and the stack can be used to hold the contents of this loop counter when nested loops are invoked. The eight input lines may also be pushed onto the stack to externally load the counter.

Loop Counter

To make provision for a number of operations to be repeated a defined number of times, a loop counter called CREG has been included in the design. This eight bit counter is loaded from the D field by a dedicated instruction LOADC or from the stack in the case of nested loops. The counter decrements to zero and then holds at zero. So repetitive routines may be achieved by a LOOPNZ instruction.

Instruction Set

The instruction set for the SAM448 consists of 12 instructions to handle multiway branching, subroutines, nested for-next loops and dispatch functions. With only 12 instructions a designer can become familiar with creating SAM448 designs very quickly. The WSI State Machine Input Language (ASMILE) support software enables designs to be generated quickly and efficiently.

WAFERSCALE INTEGRATION, INC.

Programmable System™ Device

SAM448

User-Configurable Microsequencer

Features

- First Generation Programmable System Device
- User-Programmable Microsequencer for Implementing High-Performance State Machines
- On-Chip Reprogrammable EPROM Microcode Memory Up to 448 Words Deep
- 15 × 8 Stack
- Loop Counter
- Prioritized, Multi-Way Control Branching
- 8 General-Purpose Branch Control Inputs
- 16 General-Purpose Control Outputs
- Cascadable to Expand Outputs or States
- Low-Power CMOS Technology
- Footprint Efficient 28 Pin 300 Mil Dip or 28 Lead CLDCC/PLDCC Package
- 30 MHz Minimum Clock Frequency
- High Level PC-XT/AT, PS2 or Compatible Design Support Software (SAM+PLUS):
  - WSI PSD Integrated Software Environment
  - State Machine Input Language
  - Microcode Assembler
  - Functional Simulator

4

Description

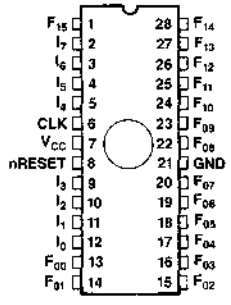
In 1988 WSI introduced a new concept in programmable VLSI, Programmable System™ Devices (PSD). The PSD is defined as a family of *User-configurable system level building blocks on-a-chip enabling quick implementation of application specific controllers and peripherals.* The first generation PSD series includes the MAP168, a User-Configurable Peripheral with Memory; the SAM448, a User-Configurable Microsequencer; and the PAC1000, a User-Configurable Microcontroller.

The SAM448 is a first generation PSD and is WSI's first user programmable microsequencer. On-chip EPROM (up to 448 words) is integrated with Branch Control Logic, Pipeline Register, Stack, and Loop Counter. This generic microcoded architecture provides an efficient vehicle for implementing a broad range of high performance controllers spanning the spectrum from basic state machines to traditional bit-slice controller applications.

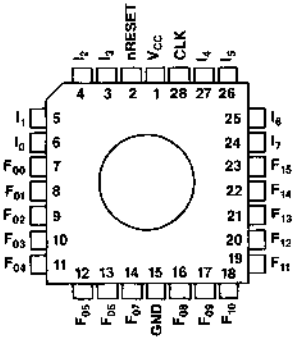
The SAM448 has eight general purpose input pins, a clock pin and a reset pin. It has 16 user-definable outputs packaged in a 28-pin 300 mil Dip or 28 Lead CLDCC/PLDCC package. One-Time-Programmable plastic versions are available to minimize volume production costs.

Pin Configuration (Top View)

Dual-In-Line



Leaded Chip Carrier



Description (Cont.)

Programming the SAM448 device is accomplished on a standard WSI PSD WISPER development system installed with the optional SAM+PLUS software package and device adapters. New users can purchase a separate WISPER-SAM development system with programming hardware included. SAM+PLUS allows designs to be entered in either state machine or microcoded formats. SAM+PLUS automatically performs logic minimization and design fitting for the device. The design may then be simulated or programmed directly to achieve customized working silicon within minutes.

Using WSI's proprietary high performance CMOS EPROM technology allows SAM448 to operate at a 25-MHz typical clock frequency while still enjoying the benefits of low CMOS power consumption. This technology also facilitates 100% generic testability which eliminates the need for post-programming testing.

Ideal application areas for SAM448 include programmable sequence generators (state machines), bus and memory control functions, graphics and DSP algorithm controllers, and other complex, high performance machines. The devices may be cascaded easily to obtain greater output requirements (horizontal cascade) or greater microcode memory depth (vertical cascade) or both.

SAM as a State Machine

The SAM448 architecture allows easy implementation of synchronous state machines. SAM's internal EPROM memory together with its Pipeline Register allows storage of up to 448 unique states. SAM's Branch Control Logic allows single clock, multi-way branching in response to the eight inputs, current device state, and user-defined transition conditions. Design entry is simplified with WSI's State Machine Input Language (ASMILE) supported by the SAM+PLUS development system. This high level language uses IF-THEN-ELSE statements to define state transitions and a truth table to define or tri-state the outputs on a state-by-state basis.

SAM as a Microcoded Sequencer

SAM's architecture has several advanced features that enable it to be used as a sophisticated microcoded sequencer. SAM's on-chip EPROM (448 words) is integrated with a microcoded sequencer consisting of Branch Control Logic, Stack, and Loop Counter. The eight general-purpose inputs, the Counter, the Stack, and the Pipeline Register feed the Branch Control Logic. The Branch Control Logic gives flexible multi-way microcode branch capability in a single clock, enhancing throughput beyond that of conventional controllers or sequencers.

SAM+PLUS development software offers high level microcode entry featuring a compact assortment of powerful instructions (OP-codes) allowing easy implementation of conditional branches, subroutine calls, multiple level for-next loops, and dispatch functions (branching to an externally specified address).

Functional Description

The SAM architecture is shown in Figure 1. The primary elements are the Microcode EPROM, 36-bit Pipeline Register, Branch Control Logic, 15 × 8-bit Stack, and 8-bit Loop Counter.

The Branch Control Logic generates the address of the next state and applies this address to the Microcode Memory. The outputs of the Microcode Memory represent the user-defined outputs and internal control values associated with the next state. On the leading edge of the clock these new values are clocked into the Pipeline Register and become the current state. The new values in the Pipeline Register—along with the Counter, Stack and Inputs—are used by the Branch Control Logic to generate the new next-state address.

Microcode EPROM and Pipeline Register

The Microcode EPROM is organized into 448, 36-bit words or locations, each of which can be viewed as a single state. 16 of these bits (the F-field) are available at device pins as user-defined outputs.

The other 20 bits are internal control signals that are divided into 4 fields: the 8-bit Q-field normally provides the next-state address; the 8-bit D-field is a general purpose field used either as a constant or as an alternative next-state address; the OP-field contains the instruction; and, the

Functional Description (Cont.)

E-field contains a single bit which enables or tri-states the device outputs.

As shown in Figure 2, the Microcode Memory is organized as 256 rows or addresses. Addresses 0 through 191 contain a single 36-bit word which is associated with the desired next-state. This state information will be clocked into the Pipeline Register on the next rising edge of the clock and the outputs will become valid one T_{CO} (clock to output delay) later.

Addresses 192–255, on the other hand, access four unique 36-bit words which correspond to four possible next states. (The extension .0, .1, .2, and .3 are used to distinguish those four states.) These 64 addresses are known as Multi-Way Branch locations and are used to perform single clock 4-way branches. Whenever the next-state address falls within the Multi-Way Branch locations, the Branch Control Logic will make the necessary 1-of-4 selection based on the next-state address and user-defined input conditions.

Figure 1. SAM448 Block Diagram

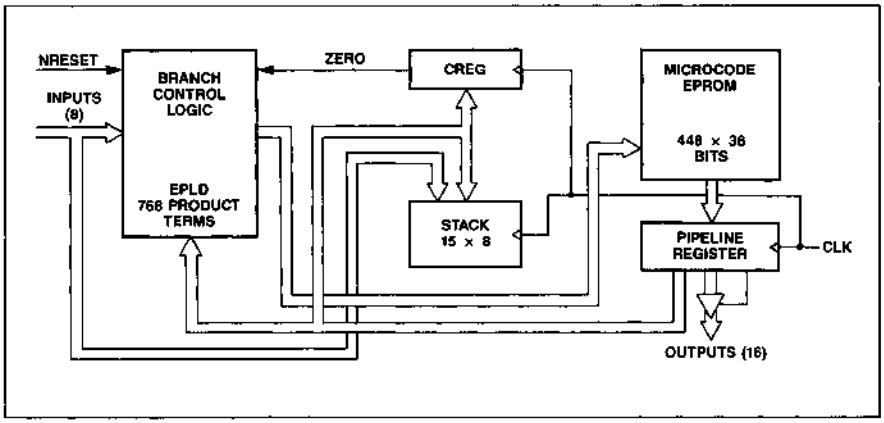


Figure 2. SAM Microcode Memory

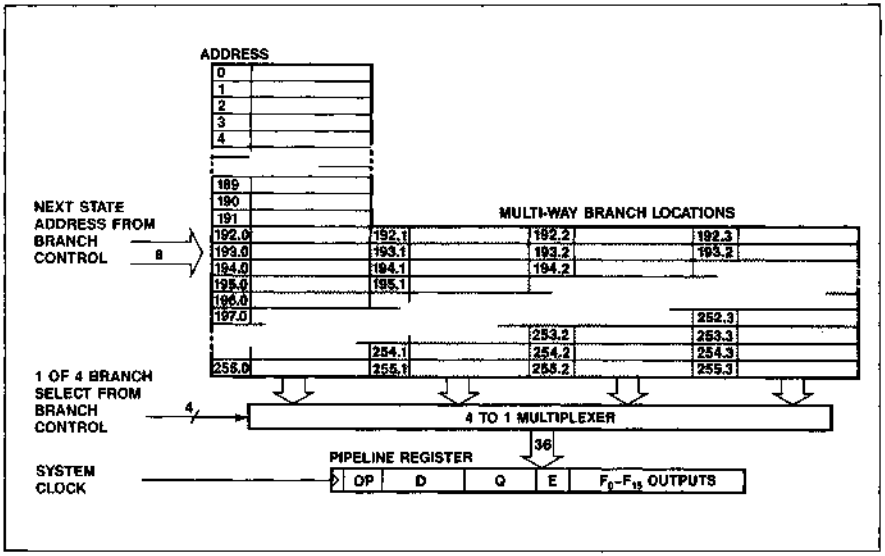
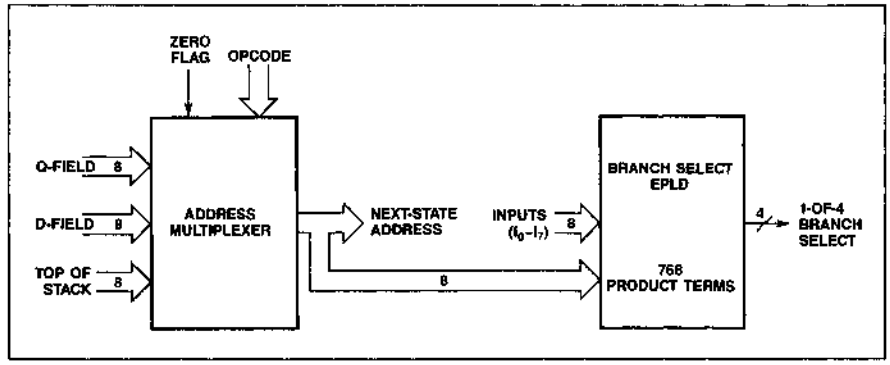


Figure 3. SAM Branch Control Logic



Branch Control Logic Block

At the heart of the high-performance sequencing ability of the SAM family is the Branch Control Logic. This block determines the next-state to be clocked into the Pipeline Register based on the current status of the Pipeline Register, the Counter, the Stack, and the eight input pins.

The Branch Control Logic is divided into two segments: the Address Multiplexer and the Branch Select EPLD.

The Address Multiplexer provides the next-state address to the Microcoded Memory. The next-state address can come from the Q-field, the D-field, or the Top-of-Stack. The selection between these three resources is based on the instruction in the Pipeline Register and the condition of the Zero Flag from the Counter.

The Branch Select EPLD is used to perform up to a 4-way branch based on user-defined input conditions. This block is a 768 product-term programmable logic device with 16 inputs and four outputs. When the next-state address falls within the multi-way branch block of memory (any address greater than 191) the Branch Select EPLD performs the necessary 1-of-4 selection. When the next-state address is less than 192, the Branch Select EPLD is turned off since no selection is required.

The conditions controlling the multi-way branch are defined by the user with a simple IF, THEN, ELSE format like the following:

```
      IF (cond3) THEN select 201.3
ELSEIF (cond2) THEN select 201.2
ELSEIF (cond1) THEN select 201.1
ELSE               select 201.0
```

The conditions are prioritized so that if the first condition is not met (cond3), then microword 201.3 will be selected and clocked into the Pipeline Register regardless of the results of cond2 and cond1. If none of the three conditions are met, then the microword 201.0 will be clocked into the Pipeline Register.

The three conditional expressions are user defined and may contain any logical equation based on the inputs that can be reduced to four product-terms. For example, the expression

```
  I1 * /I2 * /I4
+I3 * /I4 * /I5 * /I6 * /I7
+I0
+I2 * /I4 * /I5
```

contains four product-terms and is a valid condition. There is a unique set of 12 product-terms for each of the 64 multi-way branch locations for a total of 768 product-terms. (See Figure 4.)

The SAM448 has been designed so that the number of available product-terms should never be the limiting factor on a design. Prioritization provides an effective product-term count of more than 12 per location. A trade-off between number of product-terms and number of possible branches can be made by simply placing identical state information in two locations as shown in Figure 5.

Figure 4. SAM Branch Logic for Address 192 Through 255

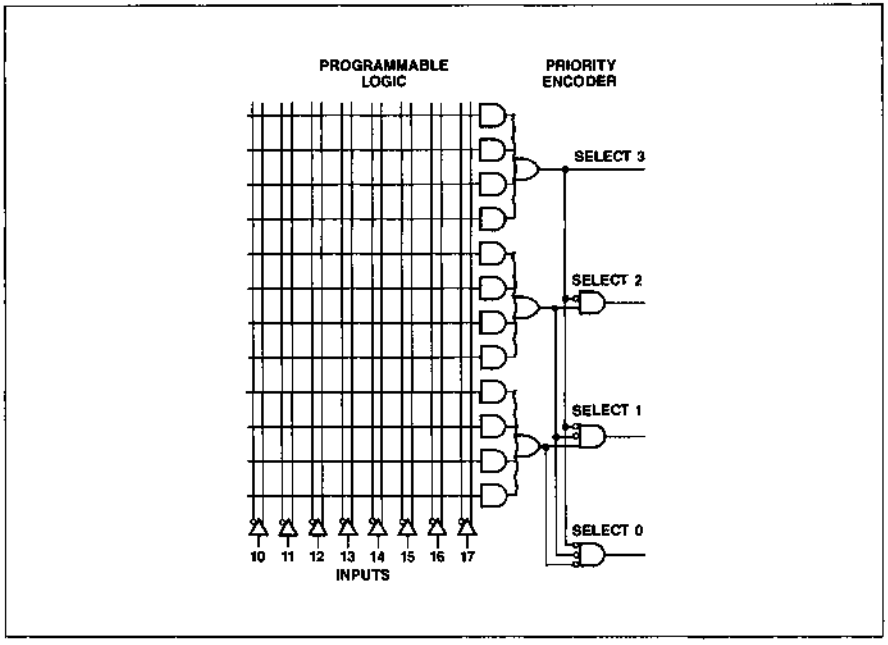
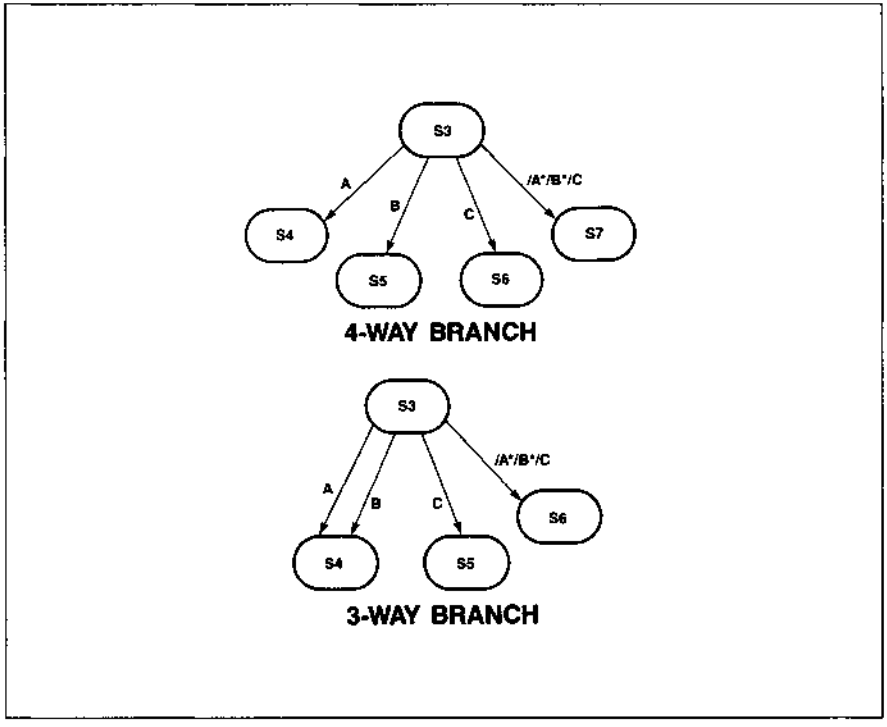


Figure 5. Multi-Way Branching



Functional Description (Cont.)

Stack

The Stack of the SAM448 is a Last In First Out (LIFO) arrangement consisting of 15 8-bit words. The Top-of-Stack may be used as the next-state address or popped into the Counter. Values may be pushed onto the stack either from the D-field in the Pipeline Register or from the Counter enabling efficient implementation of subroutines, nested loops, and other iterative structures. The eight input lines may also be pushed onto the stack to allow external address specification in a dispatch function or to externally load the counter.

The PUSHing or POPing of the stack occurs on the leading edge of the clock. The stack is "zero filled" so that a POP from an empty stack will return all eight bits set to zero. On the other hand, a push to an already full stack will write over the Top-of-Stack leaving the other 14 values unchanged.

Loop Counter

The SAM448 contains an 8-bit Loop Counter, referred to as the Count Register (CREG), which is useful for controlling timing loops and affecting a variety of branch operations. The CREG is a down counter and may be loaded directly from the D-field of the Pipeline Register or from the Top-of-Stack. The value of the CREG may be saved and restored by pushing and popping it to and from the Stack.

The CREG is loaded or decremented on the leading edge of the clock. It is designed so that it will not decrement once it reaches zero to prevent roll-over. A Zero Flag indicates when the counter has reached zero and is used with the LOOPNZ command to control program flow (see Instruction Set Description). Single instruction delay loops are easily constructed and, in combination with the Stack, nested loops or delays of arbitrary length may be generated.

Instruction Set

The instruction set of the SAM448 consists of a compact assortment of powerful commands. Assembly language constructs allow efficient implementation of multi-way branching, subroutines, nested for-next loops, and dispatch functions. The complete instruction set is described at the end of this data sheet. These instructions are only used with assembly language design entry and are automatically supplied when using the WSI State Machine Input Language (ASMILE).

Output Enable Control

Each microcode word contains an OE bit (the E-field) which enables the outputs when E = 1 and causes a high-impedance when E = 0. These bits are accessible through high-level constructs in the WSI Development Software. This capability allows the vertical cascading of SAM448 devices to increase the number of states.

nRESET Pin

The nRESET pin acts as a master reset for the SAM448 causing it to empty the Stack, clear the Counter, and load the microword found at address 0 into the Pipeline Register. The nRESET signal is useful for system reset or for synchronizing several SAMs that are cascaded vertically or horizontally.

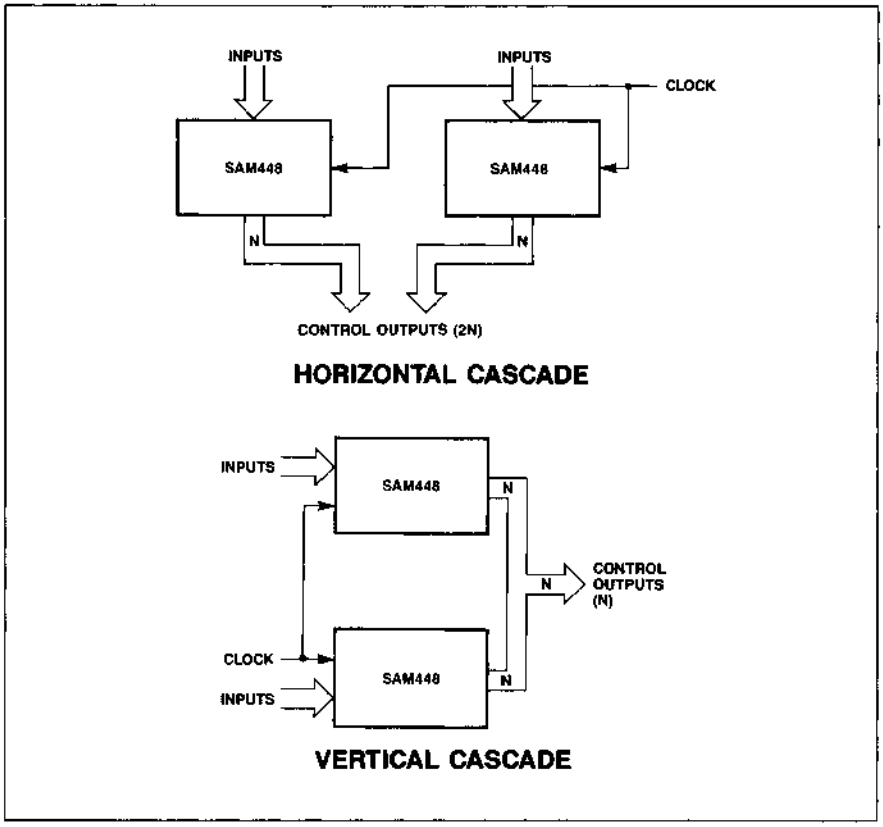
The nRESET signal must be held low for at least three clock rising edges to perform a valid clear. A nRESET of one clock rising edge causes the SAM448 to enter into a supervisor mode and a nRESET of two clock edges results in an undefined state.

The outputs of the boot address (00 Hex) will appear at the pins from the fourth clock edge after nRESET goes low, until the third clock edge after nRESET returns to high.

Horizontal and Vertical Cascading

Just as with memory and bit slice devices, the SAM devices can be cascaded to provide greater functionality. If an application requires more output lines, two or more SAMs can be cascaded horizontally. Likewise, if an application requires more states, two or more SAMs can be cascaded vertically. In either case, no speed penalty is incurred. Designs utilizing horizontal cascading are fully supported by the SAM+PLUS development software. Vertical cascading requires the designer to make certain tradeoffs to split the design.

Figure 6. SAM448 Cascading



Functional Testing

The SAM448 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of the SAM448 allows test programs to be used and then erased during early stages of production flow. This facility to use application-independent, general purpose tests is called generic testing and is unique among user-defined LSI logic devices. The devices also contain on board test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Note 6	4.75 (4.5)	5.25 (5.5)	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_R	Input Rise Time (Note 6)			500 (100)	ns
T_F	Input Fall Time (Note 6)			500 (100)	ns

DC Operating Characteristics

V_{CC} = 5V ± 5%, 0°C to +70°C for Commercial
V_{CC} = 5V ± 10%, −40°C to +85°C for Industrial
V_{CC} = 5V ± 10%, −55°C to +125°C for Military

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage		2.0		V_{CC}+0.3	V
V_{IL}	Low Level Input Voltage		−0.3		0.8	V
V_{OH}	High Level TTL Output Voltage	I_{OH} = −8 mA DC	2.4			V
V_{OH}	High Level CMOS Output Voltage	I_{OH} = −4 mA DC	3.84			V
V_{OL}	Low Level TTL Output Voltage	I_{OL} = 8 mA (4 mA) DC			0.45	V
I_I	Input Leakage Current	V_I = V_{CC} or GND			±10	µA
I_{OZ}	3-State Output Off-State Current	V_O = V_{CC} or GND			±10	µA
I_{CC1}	V_{CC} Supply Curent (Standby) (Note 6)	V_1 = V_{CC} or GND I_0 = 0 CLK = V_{CC}		30	65 (90)	mA
I_{CC2}	V_{CC} Supply Current (Active) (Note 6)	No Load 50% CLK f = 20 MHz		55	120 (170)	mA

Absolute Maximum Ratings

(See Design Recommendations)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	With Respect to GND (Note 2)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage		−2.0	14.0	V
V_I	DC Input Voltage		−2.0	7.0	V
I_{CCMAX}	DC V_{CC} or GND Current		−250	250	mA
I_{OUT}	DC Output Current, per Pin		−25	25	mA
P_D	Power Dissipation			1200	mW
T_{STG}	Storage Temperature	No Bias	−65	150	°C
T_{AMB}	Ambient Temperature	Under Bias	−10	85	°C

Capacitance

(Note 3)

Symbol	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz	15	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz	10	pF
C_{RST}	nRESET Pin Capacitance		75	pF

AC Characteristics

V_{CC} = 5V ± 5%, 0°C to +70°C for Commercial
V_{CC} = 5V ± 10%, −40°C to +85°C for Industrial
V_{CC} = 5V ± 10%, −55°C to +125°C for Military (Note 7)

Symbol	Parameter	Conditions	SAM448-30		SAM448-25		SAM448-20		Unit
			Min	Max	Min	Max	Min	Max	
f_{CYC}	Maximum Frequency	C_1 = 35 pF	30		25		20		MHz
t_{CYC}	Minimum Clock Cycle			33.3		40		50	ns
t_{SU}	Input Setup Time		16.5		20		22		ns
t_H	Input Hold Time		0		0		0		ns
t_{CO}	Clock to Output Delay	C_1 = 35 pF		16.5		20		22	ns
t_{CZ}	Clock to Output Disable or Enable			16.5		20		22	ns
t_{CL}	Minimum Clock Low Time		11		12		15		ns
t_{CH}	Minimum Clock High Time		11		12		15		ns
t_{SUR}	nRESET Setup Time		16.5		18		18		ns
t_{HR}	nRESET Hold Time		5		5		5		ns

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5V.
2. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
3. Capacitance measured at 25°C. Sample tested only.
4. If the nRESET is held low for more than 3 clock edges, then the outputs associated with the boot address (00 Hex) will remain at the pins until the third clock edge after nRESET goes high.
5. For 1.0 < V_1 < 3.8, the nRESET pin will source up to 200 µA.
6. Figures in ( ) pertain to military and industrial temperature versions.
7. The specifications noted above apply to military operating range devices. MIL-STD-883 compliant product specifications are provided in military product drawings available on request from WSI marketing at Tel. 415-656-5400. These military product drawings should be used for the preparation of source control drawings.

Figure 7. Timing Waveforms

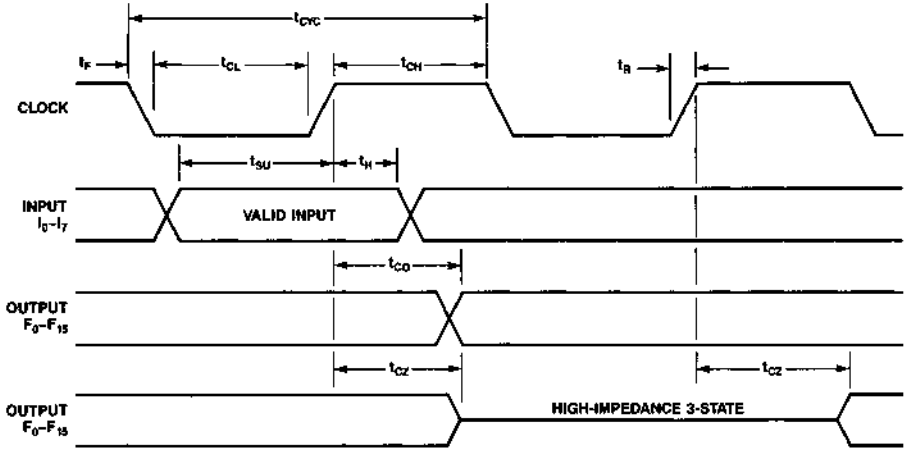
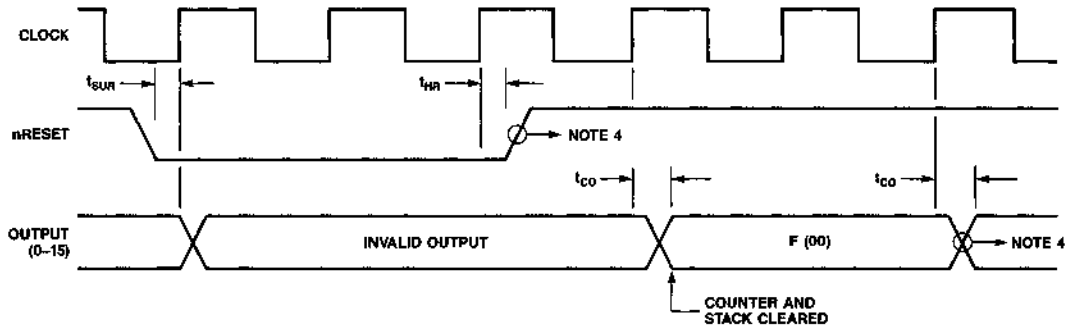


Figure 8. Reset Timing Waveforms



Design Security

The SAM448 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells in invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

Design Recommendations

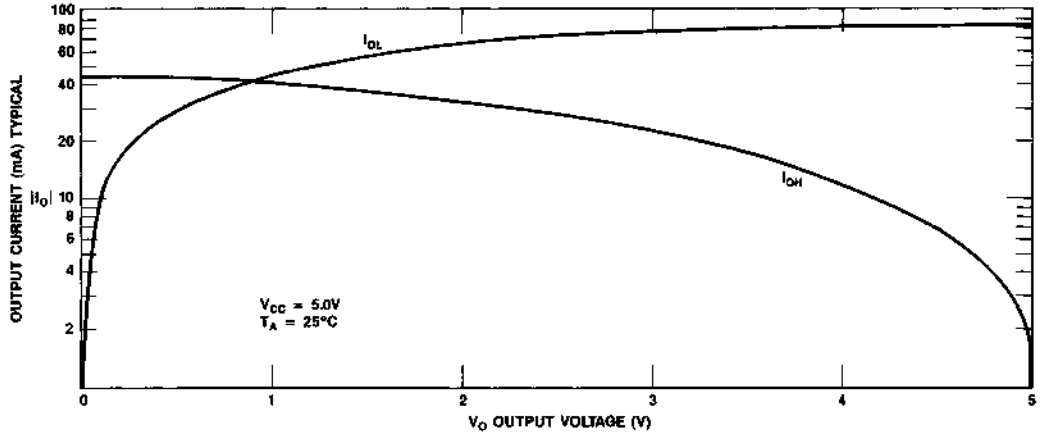
Operation of the SAM448 with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These devices contain circuitry to protect the input against damage to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

For proper operation, it is recommended that opaque labels be placed over the device window. Input and output pins must be constrained to the range GND $\leqslant$ (V_{IN} or V_{OUT}) $\leqslant$ V_{CC}. Unused inputs must always be tied to an appropriate logic level (e.g., either V_{CC} or GND). A power supply decoupling capacitor of at least 0.1 µF must be connected directly between the V_{CC} pin and GND.

When operating in noisy environments it is possible that a glitch on the nRESET pin one T_{SUR} before the clock edge could initiate a supervisor mode. To prevent this possibility, it is recommended to connect a capacitor of at least 0.1 µF from the nRESET input to ground.

All general purpose inputs to the SAM448 should be synchronized to be guaranteed to meet the setup time. Input transitions which occur less than one T_{SU} before the leading clock edge can cause the SAM448 to enter an undefined state.

Figure 9. Output Drive Current



Instruction Set Description

Following is a description of the instruction set available with the SAM448. These instructions can be used in conjunction with the Assembly Language entry to access the various features of the SAM448. They are automatically supplied when using the WSI State Machine Input Language (ASMILE).

In the following description label1 and label2 indicate arbitrary labels located in the assembly (.ASM) file. These labels will be converted by the software into the 8-bit address of that label. The parameter constant is any 8-bit number (0–255 Decimal, 0–FF Hex) representing an address, a mask, or a constant.

The instructions influence the control of the Stack, the Counter, and the Address Multiplexer. These effects are summarized in the Instruction Table. Throughout the examples it is assumed for simplicity that the destination labels do not lie within the Multi-Way Branch Block of memory so that branching based on inputs is not performed. It is valid, however, for any of these labels to lie within the Multi-Way Branch Block so that 4-way branching based on the inputs can be performed. See the MULTI-WAY BRANCH section at the end of this data sheet for more details.

The SAM+PLUS development system allows the designer to use the high level Assembly Language without worrying about the actual values that are placed in the various fields.

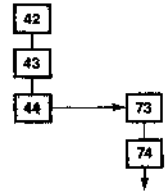
CONTINUE simply causes execution to continue with the next sequential instruction found in the Assembly Language file (.ASM).

CONTINUE

Instruction Set Description (Cont.)

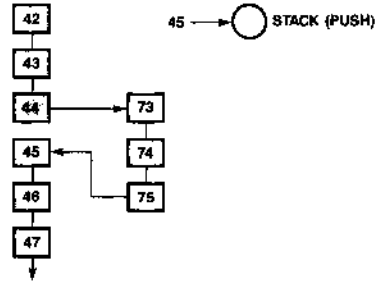
The JUMP instruction causes execution to branch to the indicated location. If address 44 contains the instruction 'JUMP label1,' then the next state will come from label1 which in this case is located at address 73.

JUMP label1



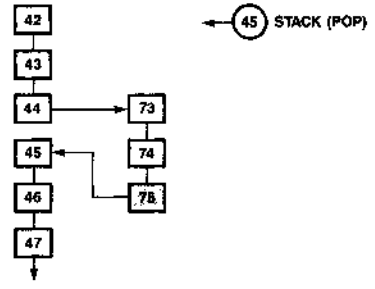
The CALL/RETURNTO instruction is typically used to call a subroutine. In general it will push the address of label2 onto the Stack and cause label1 to be the next-state address. Leaving the RETURNTO designation off will cause label2 to default to the next instruction in the .ASM file. In the example, address 44 contains the command 'CALL label1' where label1 is located at address 73. This causes the address of the following instruction, in this case 45, to be pushed onto the Stack, and the next state to come from address 73. The RETURN command at address 75 returns the execution to address 45.

CALL label1 RETURNTO label2



The RETURN command is used to return from a subroutine call or in general to cause the next-state address to come from the top of the Stack. In the example, the command at address 44 CALLed the subroutine at address 73 and PUSHed the value 45 onto the Stack. The RETURN command at address 75 will transfer execution to address 45 and POP that value off the Stack.

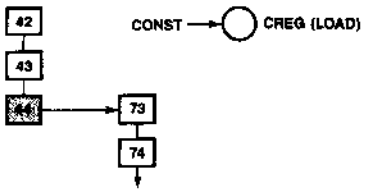
RETURN



Instruction Set Description (Cont.)

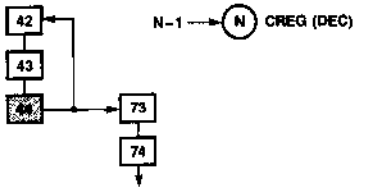
The LOAD Counter command loads the Counter with the value specified and transfers execution to label1. The LOADC command is typically used to initialize the Counter for a repetitive loop. In the example, address 44 has the command 'LOADC 73D GOTO label1' which causes the decimal value 73 to be loaded into the Counter and the next state to come from label1. In this case label1 is located at address 73. If the GOTO designation is left off label1 will default to the next instruction in the .ASM file.

LOADC constant GOTO label1



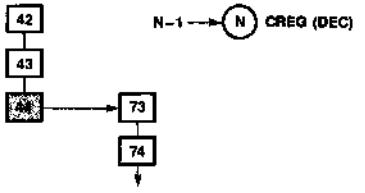
The LOOP on Non-Zero/ON ZERO goto command jumps to one of two addresses based on the value of the Zero Flag and decrements the Counter if not zero. This instruction is typically used to implement for-next loops. In the example, address 44 has the command 'LOOPNZ label1 ONZERO label2' where label1 is located at address 42 and label2 is located at address 73. If the Counter is not at zero then the next state will come from address 42 and the Counter will be decremented. If the Counter is already at zero then the instruction at address 73 will be executed and the Counter will stay at zero. If the ONZERO designation is left off, the default for label2 will be the next instruction in the .ASM file.

LOOPNZ label1 ONZERO label2



The DEcrement Counter on Non-Zero GOTO command will decrement the Counter if it is non-zero and jump to label1. In the example, address 44 has the command 'DECNZ GOTO label1' where label1 is located at address 73. The Counter is decremented and the next instruction comes from address 73. The default for label1 is the next instruction in the .ASM file.

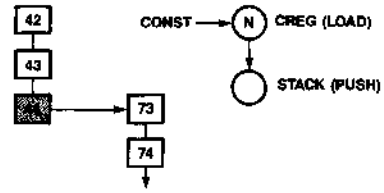
DECNZ GOTO label1



Instruction Set Description (Cont.)

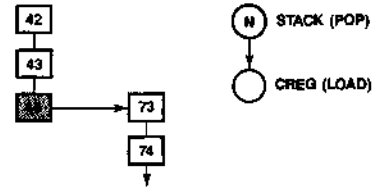
The PUSH Counter LOAD Counter command will push the current value of the Counter onto the Stack, load a constant into the Counter, and jump to label1. This instruction is useful for implementing nested for-next loops. In the example, the instruction at address 44 is 'PUSHLOADC 153D GOTO label1' where label1 is located at address 73. The value in the Counter will be pushed onto the Stack, the decimal value 153 will be loaded into the Counter, and the next instruction will come from address 73. The default for label1 is the next instruction in the .ASM file.

PUSHLOADC constant GOTO label1



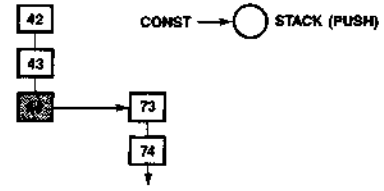
The POP Stack to Counter GOTO command will pop the top of Stack into the Counter and jump to label1. This command is typically used in conjunction with the PUSHLOADC to implement nested for-next loops. In the example, address 44 has the command 'POPC GOTO label1' where label1 is located at address 73. The default for label1 is the next instruction in the .ASM file.

POPC GOTO label1



The PUSH constant to Stack GOTO command will push the value constant onto the Stack and jump to label1. In the example, address 44 has the command 'PUSH 34D GOTO label1' where label1 is located at address 73. The decimal value 34 is pushed onto the Stack and the next state comes from address 73. The default for label1 is the next instruction in the .ASM file.

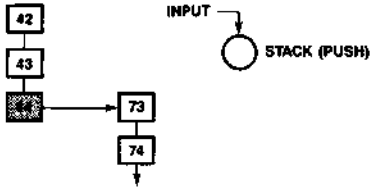
PUSH constant GOTO label1



Instruction Set Description (Cont.)

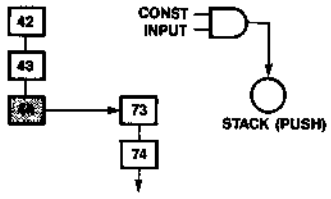
The PUSH Input GOTO command will push the eight inputs (I7–I0) onto the Stack. In the example address 44 has the instruction 'PUSHI GOTO label1' where label1 is located at address 73. At the leading edge of the clock the eight inputs are pushed onto the Stack. In a typical example, address 73 would have a RETURN instruction which would cause execution to jump to the address represented by the recently PUSHed input pins. This implements a dispatch function. The default for label1 will be the next instruction in the .ASM file. This instruction can also be used to load the Counter with an externally specified variable. In this case address 73 would have a POPC instruction.

PUSHI GOTO label1



The AND PUSH Input GOTO command is identical to the PUSHI command except the inputs are first bit-wise ANDed with a constant. This allows the masking of irrelevant inputs before PUSHing an address for a dispatch routine.

ANDPUSHI constant GOTO label1



The POP and XOR Stack to Counter GOTO command will pop the top of Stack, bitwise XOR it with a constant, load the result into the Counter, and jump to label1. In the example, address 44 has the command 'POPXORC 25D GOTO label1' where label1 is located at address 73. The top of Stack is POPed off the Stack, XORed with the decimal number 25, and loaded into the Counter. The next state comes from address 73. Since a XOR function does a comparison, this command can be used to compare the input to a constant and then branch based on the result with a LOOPNZ command. If the GOTO designation is left off the default for label1 will be the next instruction in the .ASM file.

POPXORC constant GOTO label1

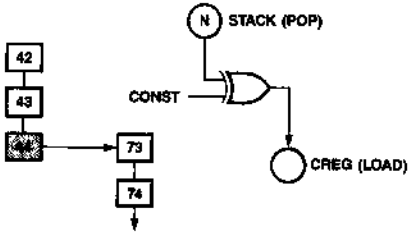


Figure 10. Instruction Set Summary

Instruction	Definition	Next-State Address	Stack	Counter
CONTINUE	Continue with Next Instruction	label1	None	HOLD
JUMP	Jump to a Label	label1	None	HOLD
CALL	Call Subroutine	label1	label2	HOLD
RETURN	Return From Subroutine	STACK	POP	HOLD
LOADC	Load CREG	label1	None	Constant
LOOPNZ	Loop/Dec. on Non-Zero	label 1 or 2	None	DECREMENT
DECNZ	Decrement CREG on Non-Zero	label1	None	DECREMENT
PUSHLOADC	Push CREG to Stack and Load CREG	label1	CREG	Constant
POPC	Pop Stack to CREG	label1	POP	STACK
PUSH	Push Constant to Stack	label1	Constant	HOLD
PUSHI	Push Inputs to Stack	label1	INPUTS	HOLD
ANDPUSHI	Push Masked Inputs to Stack	label1	INP * const	HOLD
POPXORC	XOR Stack with Constant and Send Result to CREG	label1	POP	STACK ⊕ Constant

NOTE: The value label1 is placed in the Q-field. The values label2 and constant are placed in the D-field.

Multi-Way Branching

The multi-way branching capability can be super imposed upon the instruction set providing another dimension of capability. Figure 11 shows how this translates into the flow diagrams. If location 44 had the instruction 'JUMP label1' where label1 is located at address 201, then the next-state would come from address 201. But address 201 is within the Multi-Way Branch Block so the Branch Select EPLD must decide which of the four words to send to the pipeline register. This selection is based on user-defined functions of the inputs.

Similarly, location 44 could contain any of the 13 available commands so that the multi-way branch capability can enhance each instruction. If location 44 was a CALL to a subroutine, then address 201 could contain the starting instruction for 4 unique subroutines. The actual routine executed would depend on the condition of the inputs as defined by the user.

The actual Assembly Language code required to implement this example is as follows:

44D: [Output Spec] CALL label1;

201D: IF cond1 THEN [out 1] JUMP 102D;
ELSEIF cond2 THEN [out 2] JUMP 73D;
ELSEIF cond3 THEN [out 3] JUMP 53D;
ELSE [out 4] JUMP 34D;

Figure 11. Jump to a Multi-Way Branch Address

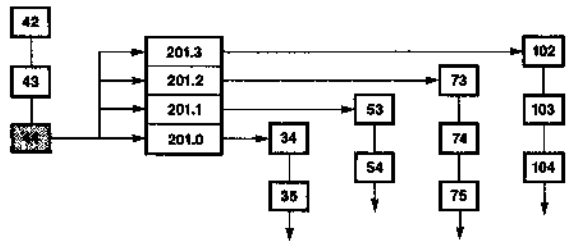
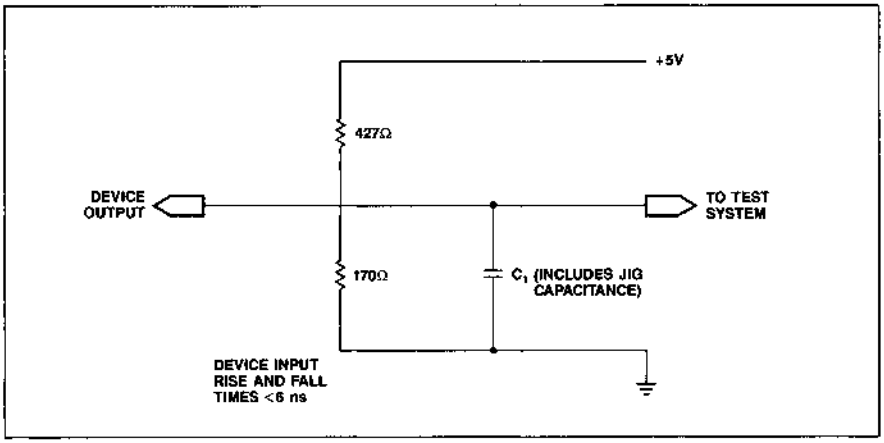


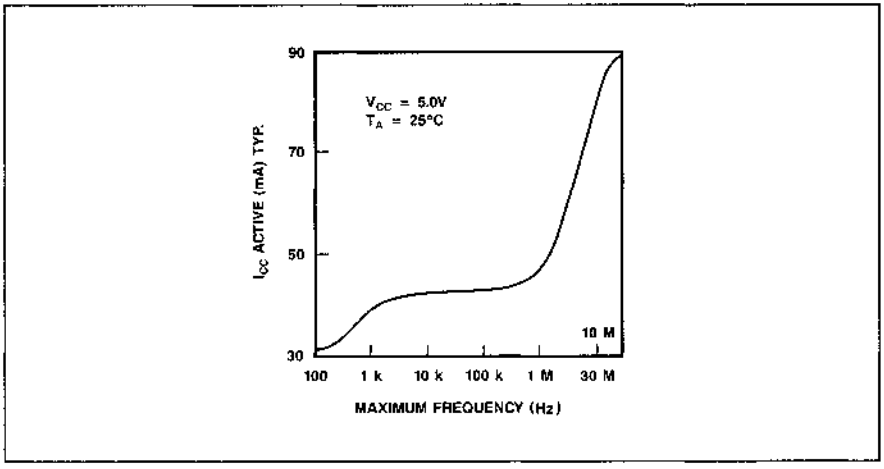
Figure 12. AC Test Conditions



Power supply transients can affect AC measurements; simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

4

Figure 13. I_{CC} vs. F_{MAX}



Product Grades

Application	Temperature Range	Marking Designator
Commercial	0°C to +70°C	
Industrial	−40°C to +85°C	I
Military	−55°C to +125°C	M
MIL-STD-883C, Class B	−55°C to +125°C	MB

SAM system development tools are a complete set of PC-based development tools for the SAM448. Installed on an IBM-XT, AT or compatible computer, these tools provide an integrated easy-to-use software and hardware environment to support SAM448 development. These tools may be purchased as a complete development system or as individual software and hardware products. SAM system development tools contain all necessary programming hardware and software required to build high-performance state machines.

Host Requirements

The host system requirements for installing and using the SAM448 system development tools are an IBM-XT, AT, or compatible computer running MS-DOS version 3.1 or later. The system must be equipped with 640 Kbytes of RAM and a hard disk.

Hardware

The SAM448 system programming hardware consists of the following:

- MagicPro — Memory and System Programmer
- WS6008 — 28 Pin Dip Socket Adaptor for MagicPro Remote Socket Adaptor Unit
- WS6009 — 28 Pin LCC Socket Adaptor for MagicPro Remote Socket Adaptor Unit

The MagicPro Programmer is the common hardware platform for programming all WSI programmable products. It consists of the IBM-PC® plug-in Programmer Board and the Remote Socket Adaptor Unit.

Software

The SAM448 System Development Software consists of the following:

- WISPER Software — WSI Integrated Software and Programming Environment
- SAMPLUS Software — Interface Manager for SAM Tools
- ASMILE Software — System Entry Language
- SAMSIM Software — Functional Simulator
- SAMPRO Software — Device Programming Software

The complete SAM448 development cycle is illustrated in Figure 1.

WISPER and SAMPLUS software provide a menu-driven user interface enabling other tools to be easily invoked by the user.

The system design is entered into ASMILE (WSI State Machine Input Language) source program files using an editor chosen by the user. ASMILE supports Microcode entry and State Machine entry.

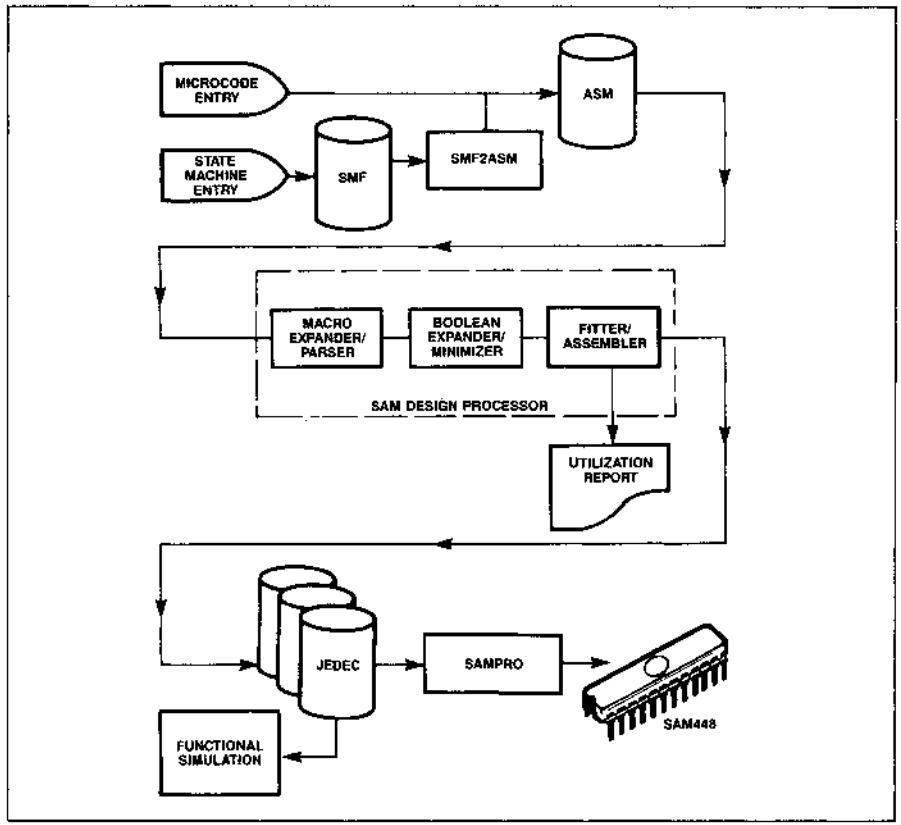
The ASMILE produces object code format which can be loaded to SAMSIM and SAMPRO

The SAMSIM functional simulator enables the user to test and debug programs by examining the state of SAM448 internal states before and during a complete functional simulation of the device.

SAMPRO software programs SAM448 devices by using the MagicPro hardware and the socket adaptor.

The programmed SAM448 is then ready to be used.

Figure 1. SAM Development Cycle



Documentation

SAM448 Software User's Manual.

WSI-Support

WSI provides a complete set of quality support services (WSI-Support) to registered system development tools owners. These services include the following:

- 12-Month Software update service — Up-to-date software maintenance, access to latest software and product information.
- Hotline to WSI Application Experts — Direct system development assistance
- 24-Hour Electronic Bulletin Board Service — Design assistance via our auto-answer dial-up modem service.

Training Workshops

WSI provides "Do-It-Yourself Systems" Technical Training Workshops that provide an in-depth tutorial on SAM448 and SAM system development tools.

Workshop participants will learn how to build their own high-performance state machine using the SAM448. SAM Development Training Workshops are held at the WSI Fremont facility.

Ordering Information — System Development Tools

SAM448-Gold package consists of the following:

- Software
  - — WISPER Software
  - — SAMPLUS Software
  - — ASMILE Software
  - — SAMSIM Software
  - — SAMPRO Software
  - — User's Manual
  - — WSI-Support
- Hardware
  - — WS6000 MagicPro Programmer

SAM448-Silver package consists of the following:

- Software
  - — WISPER Software
  - — SAMPLUS Software
  - — ASMILE Software
  - — SAMSIM Software
  - — SAMPRO Software
  - — User's Manual
  - — WSI-Support

WS6000 MagicPro™ Memory and PSD Programmer

- Includes IBM PC plug-in adaptor card and Remote Socket Adaptor

Adaptors

- WS6008 28 Pin Dip Socket Adaptor
- WS6009 28 Pin CLLCC/CLDCC/PLDCC Socket Adaptor

WSI-Support

- Includes 12-month Software Update Service to registered system owners
- Includes Hotline to WSI Application experts
- Includes 24-hour access to WSI's Electronic Bulletin Board Service

SAM Training Workshops

- Includes SAM448 Training Workshops at the WSI Fremont facility. For details and scheduling, contact PSD Marketing at (415) 656-5400.

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Ordering Information

Part Number	Speed (MHz)	Package Type	Package Drawing	Operating Temperature Range	WSI Manufacturing Procedure
SAM448-20J	20	28 Pin PLDCC	J3	Comm'l	Standard
SAM448-20L	20	28 Pin CLDCC	L2	Comm'l	Standard
SAM448-20LI	20	28 Pin CLDCC	L2	Industrial	Standard
SAM448-20LM	20	28 Pin CLDCC	L2	Military	Standard
SAM448-20LMB	20	28 Pin CLDCC	L2	Military	MIL-STD-883C
SAM448-20S	20	28 Pin Plastic Dip, 0.3"	S2	Comm'l	Standard
SAM448-20T	20	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
SAM448-20TI	20	28 Pin CERDIP, 0.3"	T2	Industrial	Standard
SAM448-20TM	20	28 Pin CERDIP, 0.3"	T2	Military	Standard
SAM448-20TMB	20	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
SAM448-25J	25	28 Pin PLDCC	J3	Comm'l	Standard
SAM448 25L	25	28 Pin CLDCC	L2	Comm'l	Standard
SAM448-25S	25	28 Pin Plastic Dip, 0.3"	S2	Comm'l	Standard
SAM448-25T	25	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
SAM448-30J	30	28 Pin PLDCC	J3	Comm'l	Standard
SAM448-30L	30	28 Pin CLDCC	L2	Comm'l	Standard
SAM448-30S	30	28 Pin Plastic Dip, 0.3"	S2	Comm'l	Standard
SAM448-30T	30	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard

Electronic Bulletin Board

Bulletin Board

WSI provides a 24-hour electronic bulletin board system that provides the user with the latest information on software updates, enhancements, and applications relating to WSI products. In addition, users developing applications software for WSI products can send portions of their code to WSI for application's consultation if desired.

The following hardware is required to use the WSI bulletin board:

- ❑ Computer Terminal
- ❑ 300, 1200, 2400 Baud Modem
- ❑ 8 Data Bits
- ❑ No Parity
- ❑ 1 Stop Bit

Access Line

To access the bulletin board, dial

(415) 498-1002

and wait for the modem tone. When your modem establishes a connection, enter <return> <return> to signal the bulletin board software. The board should respond:

WSI Customer Engineering Support
Electronic Bulletin Board Service

followed by some other messages, after which you will be asked for your name, and a password. Upon initial use, follow the on-screen prompts for establishing your password.

Now that you have entered the bulletin board service, you will be given a choice of "MAIN" commands:

Main Commands

M)sg-Section
Choose this option to leave messages.

F)ile-Section
Choose this option to download or upload data files and/or utility programs

B)ulletins
Choose this option to see the latest important news such as software versions and programming tips for WSI Memory and PSD products.

S)tatistics
This option describes the current bulletin board statistics

C)hange
Choose this option to change operational settings that the bulletin board maintains for your user name.

P)age-Operator
Choose this to page the operator for assistance. It is not likely that the operator will be available during West Coast U.S. non-business hours.

L)ist-Callers
Choose this option to see who else is using the board at this moment.

A)ns-Questionnaire
Choose this option to answer a user profile questionnaire.

V)ersion
Describes the board software version.

G)oodbye
Choose this to leave the bulletin board.

See the individual software manuals for more detailed explanation and usage of the bulletin board.

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

MEMORY PROGRAMMING AND PSD DEVELOPMENT SYSTEMS

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 800-562-6363.

WAFERSCALE INTEGRATION, INC.

Memory Programming and PSD Development Systems

Introduction

WSI is a company built upon user-programmable products. Customer success in programming our memory and Programmable System Devices is paramount to our continued growth and success. Consequently, WSI places a high priority on programming support and customer ease of programming of our products.

The WSI MagicPro™ Memory and PSD Programmer helps system designers as they develop end products that include WSI's memories or Programmable System Devices. MagicPro Programming software is immediately available for any new WSI memory or PSD product as soon as the product becomes available for sampling. The MagicPro enables newly developed software to be programmed into a WSI product and tried immediately in a prototype system. It is used with an IBM-PC or compatible computer and accepts a variety of socket adaptors for virtually any WSI package.

Several manufacturers of EPROM programmers support WSI products. For information on Data I/O, refer to Data I/O Programming Support in this section. Programmer manufacturers are listed below:

U.S.A.	Telephone
Data I/O	1-800-247-5400, Ext. 400
Logical Devices	1-800-EEI-PROM
Stag	408-988-1118
Bytek	407-994-3520
Digelec	818-887-3755
Link	201-994-6669
Elan	415-932-0882
Oliver Advanced Engineering	818-240-0080
Kontron	800-227-8834
BP Microsystems	800-225-2102
Europe	
Microprss (France)	(16) 20.47.90.40
Sprint/SMS (W. Germany)	32-2-687-4154
Kontron Messtechnik Gmbh (W. Germany)	(08165) 77-0
Asia	
Ando Electric Co., Ltd	03-733-1151
Advantest Corporation	03-342-7500
Minato Electronics Inc.	045-591-5611
Aval Data Corporation	03-344-2001
Data I/O Japan Co. Ltd.	03-432-6991
Japan Macnics Corporation	044-711-0330
Promac	

Please contact your local WSI sales office for information relating to commercially available programmers that support WSI products.

The PSD Development Systems are complete hardware/software or software development packages for any of the PSD products. The Gold package includes the MagicPro Memory and PSD Programmer, development and/or programming software and a comprehensive user manual. The Silver package contains the same items as the Gold package with the exception of the MagicPro Programmer.

Data I/O Programming Support

All WSI memory products program easily on standard commercially available EPROM programmers. Manufacturers of these EPROM programmers offer a broad range of products which cover prototyping through high volume production requirements. The table below covers that portion of Data I/O's product line which supports WSI's programmable products. For more information regarding programming support for WSI products call toll-free 800-TEAM WSI (800-832-6974) or 800-451-5970 (CA).

Product	Pkg Type	Family/Pinout Code	Unipak 2	Unipak 2B	Unipak 2B Cartridge	Series 22	S1000	S1000 Rail	UniSite	UniSite Module	SetSite	GangPak	288	288 Module	212	212 Module
WS57C191	DIP	7B/21	V12	V12	—	—	V12	SR 28	V2.0	SITE 40/48	V2.0	V07	—	—	V1.1	MOD-EPROM
WS57C191B	DIP	7B/21	V17	V17	—	—	—	—	V2.5	SITE 40/48	—	—	V2.0	MOD 32	—	—
WS57C191B	PLCC	7B/8B	—	V18	351B093	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS57C191C	DIP	12D/021	V18	V18	—	—	—	—	V2.5	SITE 40/48	—	—	—	—	—	—
WS57C291	DIP	7B/21	V12	V12	—	—	—	—	V2.5	SITE 40/48	—	V08	V2.0	MOD 32	V1.1	MOD-EPROM
WS57C291B	DIP	7B/21	V17	V17	—	—	—	—	V2.5	SITE 40/48	—	—	—	—	—	—
WS57C291C	DIP	12D/021	V18	V18	—	—	—	—	V2.5	SITE 40/48	—	—	—	—	—	—
WS57C45	DIP	122/0B0	V17	V17	—	—	—	—	—	—	—	—	—	—	—	—
WS57C43	DIP	7B/63	V12	V12	—	—	V12	SR 28	V2.0	SITE 40/48	V2.0	V07	—	—	—	—
WS57C43B	DIP	7B/63	V17	V17	—	—	—	—	V2.5	SITE 40/48	V2.0	—	V3.0	MOD 32	—	—
WS57C43B	PLCC	7B/8E	—	V18	351B093	—	—	—	V2.5	CHIPSITE	V2.5	—	—	—	—	—
WS57C43C	DIP	12D/063	V18	V18	—	—	—	—	V2.5	SITE 40/48	—	—	—	—	—	—
WS57C49	DIP	7B/67	—	—	—	—	—	—	V2.0	SITE 40/48	V2.0	—	—	—	—	—
WS27C64F	DIP	5C/33	—	—	—	—	—	—	—	—	—	V08	—	—	—	—
WS27C64F	DIP	3C/33	V12	V12	351B086	—	V07	SR 28	V2.0	SITE 40/48	V2.0	—	V2.0	MOD 32	V1.1	MOD-EPROM
WS57C65	DIP	2C/E7	—	—	—	—	—	—	V2.0	SITE 40/48	—	—	—	—	—	—
WS57C49	DIP	3C/67	V12	V12	—	V05	—	—	—	—	—	V07	—	—	—	—
WS57C49	DIP	F3C/067	—	—	—	—	V12	SR 28	—	—	—	—	—	—	—	—
WS57C49	DIP	7B/67	—	—	—	—	—	—	V2.0	SITE 40/48	V2.0	—	—	—	V1.1	MOD-EPROM
WS57C49	LCC	7B/9A	—	—	—	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS57C49B	DIP	3C/67	V17	V17	—	—	—	—	—	—	—	—	—	—	—	—
WS57C49B	DIP	7B/67	—	—	—	—	—	—	V2.5	SITE 40/48	—	—	V3.0	MOD 32	—	—
WS57C49B	LCC	7B/9A	—	—	—	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS57C49B	PLCC	3C/9A	—	V18	351B093	—	—	—	—	—	—	—	—	—	—	—
WS57C49B	PLCC	7B/9A	—	—	—	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS57C49B	DIP	7B/67	—	—	—	—	—	—	V2.5	SITE 40/48	—	—	—	—	—	—
WS57C49C	DIP	12D/067	V18	V18	—	—	—	—	V2.5	SITE 40/48	—	—	—	—	—	—
WS57C64F	DIP	3C/33	V12	V12	351B086	V05	V01	SR 28	V2.0	SITE 40/48	V2.0	V07	V2.0	MOD 32	V1.1	MOD-EPROM
WS57C64F	LCC	3C/C1	—	V17	351B099	—	—	—	V2.4	CHIPSITE	—	—	—	—	—	—
WS27C64L	DIP	11D/033*	—	V17	—	—	V12	—	V2.5	—	—	—	—	—	—	—
WS57C65	DIP	2C/E7	—	V12	351B095	—	V06	SR 40	V2.0	SITE 40/48	—	—	V2.0	MOD 40	V1.1	MOD-EPROM
WS57C65	LCC	02C/124	—	—	—	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS27C128F	DIP	3C/51	V12	V12	351B086	—	V07	SR 28	V2.0	SITE 40/48	V2.0	V07	V2.0	MOD 32	V1.1	MOD-EPROM
WS27C128F	LCC	3C/C2	—	V17	351B099	—	—	—	V2.4	CHIPSITE	—	—	—	—	—	—
WS57C128F	DIP	3C/51	V12	V12	351B086	V05	V01	SR 28	V2.5	SITE 40/48	—	—	V2.0	MOD 32	V1.1	MOD-EPROM

Data I/O Programming Support (Cont.)

Product	Pkg Type	Family/Pinout Code	Unipak 2	Unipak 2B	Unipak 2B Cartridge	Series 22	S1000	S1000 Rail	UniSite	UniSite Module	SetSite	GangPak	288	288 Module	212	212 Module
WS57C128F	LCC	3C/C2	—	V17	351B099	—	—	—	V2.4	CHIPSITE	—	—	—	—	—	—
WS27C128L	DIP	11D/051*	—	V17	—	—	V12	—	V2.5	—	—	—	—	—	—	—
WS27C128L	PLCC	11D/0C2	—	V19	—	—	—	—	—	—	—	—	—	—	—	—
WS57C51	DIP	7B/78	—	V13	351B101	—	—	—	V2.0	SITE 40/48	V2.0	—	—	—	V1.1	MOD-EPROM
WS57C51	DIP	F7B/078	—	—	—	—	V12	SR 28	—	—	—	—	—	—	—	
WS57C51B	DIP	7B/78	—	V17	351B101	—	—	—	V2.5	SITE 40/48	V2.5	—	V3.0	MOD 32	—	—
WS57C51B	LCC	07B/123	—	—	—	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS27C256F	DIP	124/032	V17	V17	351B086	—	—	—	V2.4	SITE 40/48	—	—	—	—	—	—
WS27C256F	DIP	3C/32	—	—	—	—	—	—	—	—	—	V08	V2.0	MOD 32	—	—
WS27C256F	LCC	124/0C3	—	V17	351B099	—	—	—	V2.4	CHIPSITE	—	—	—	—	—	—
WS27C256L	DIP	124/032	V17	V17	351B086	—	—	—	V2.4	SITE 40/48	—	—	—	—	—	—
WS27C256L	DIP	11D/F32*	—	—	—	—	V12	SR 28	—	—	—	—	—	—	—	—
WS27C256L	LCC	124/0C3	—	V17	351B099	—	—	—	V2.4	CHIPSITE	—	—	—	—	—	—
WS27C256L	PLCC	124/0C3	—	V18	351B099	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS57C256F	DIP	124/032	V17	V17	351B086	—	—	—	V2.4	SITE 40/48	—	—	—	—	—	—
WS57C256F	DIP	3C/32	—	—	—	—	—	—	—	—	—	—	V2.0	MOD 32	—	—
WS57C256F	LCC	124/0C3	—	V17	351B099	—	—	—	V2.4	CHIPSITE	—	—	—	—	—	—
WS57C257	DIP	1F/E1	—	V14	351B095	—	V09	SR 40	—	—	—	—	—	—	—	—
WS57C257	DIP	2C/E1	—	—	—	—	—	—	V2.4	SITE 40/48	—	—	V2.0	MOD 40	—	—
WS57C257	LCC	01F/113	—	V17	351B095P	—	—	—	V2.4	CHIPSITE	—	—	—	—	—	—
WS57C257	PLCC	01F/113	—	V18	351B095P	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS27C512F	DIP	125/0A4	V17	V17	351B086	—	—	—	V2.5	SITE 40/48	—	—	—	—	—	—
WS27C512L	DIP	125/0A4	V17	V17	351B086	—	V12	SR 28	V2.4	SITE 40/48	—	—	—	—	—	—
WS27C512L	PLCC	11E/0C4	—	V18	351B099	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS27C010L	DIP	109/0CB	—	V17	351B104	—	V12	SR 40	V2.4	SITE 40/48	—	—	—	—	—	—
WS27C010L	LCC	11B/0DE	—	V17	351B104P	—	—	—	V2.4	CHIPSITE	—	—	—	—	—	—
WS27C010L	PLCC	11B/0DE	—	—	—	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
WS27C010L	PLCC	11B/0DE	—	V18	351B104P	—	—	—	—	—	—	—	—	—	—	—
WS27C010R	DIP	11B/0CC	—	V18	351B104	—	—	—	V2.5	CHIPSITE	—	—	—	—	—	—
SAM448	DIP	F7/2F	—	—	—	—	—	—	V2.6	SITE 40/48	—	—	—	—	—	—
SAM448	LDCC	0F7/72F	—	—	—	—	—	—	V2.6	CHIPSITE	—	—	—	—	—	—

*AMD

Description

Memory-GOLD/Memory-SILVER is a complete set of IBM-PC-based development tools. They provide the integrated easy-to-use environment to support programming of all WSI Memory products.

WSI Memory devices include the following:

- ❑ RPROMs (2 Kbit–256 Kbit)
- ❑ Fast EPROMs (64 Kbit–256 Kbit)
- ❑ L-Family EPROMs (64 Kbit–4 Mbit)

The tools run on an IBM-PC XT, AT or compatible computer running MS-DOS version 3.1 or later.

Memory Programming Software

The Memory Programming Software is the interface software that enables the user to program a memory device on the WS6000 MagicPro™ programmer. The software enables the user to load the program into the programmer and to execute the following operations:

- ❑ Help
- ❑ Upload RAM from device
- ❑ Load RAM from disk
- ❑ Write RAM to FILE
- ❑ Display device data
- ❑ Blank test device
- ❑ Verify device
- ❑ Program device
- ❑ Configuration
- ❑ Quit

WS6000 MagicPro™ Programmer

The WS6000 MagicPro Programmer is an engineering development tool designed to program all WSI programmable products (EPROMs, RPROMs, PAC1000, MAP168, PSD301 and SAM448). It is used within the IBM-PC and compatible environment. The MagicPro consists of a short plug-in board and a Remote Socket Adaptor (RSA). It occupies a short expansion slot in the PC. The RSA has two ZIF-DIP sockets that will support WSI's 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil DIP packages without adaptors. Other packages are supported using adaptors.

WSI-Support

WSI provides on-going support for users of Memory-GOLD/Memory-SILVER. For the first year, software and programmer updates are included at no charge. After that, the user may purchase the WSI-Support agreement to continue to receive the latest software releases.

Ordering Information

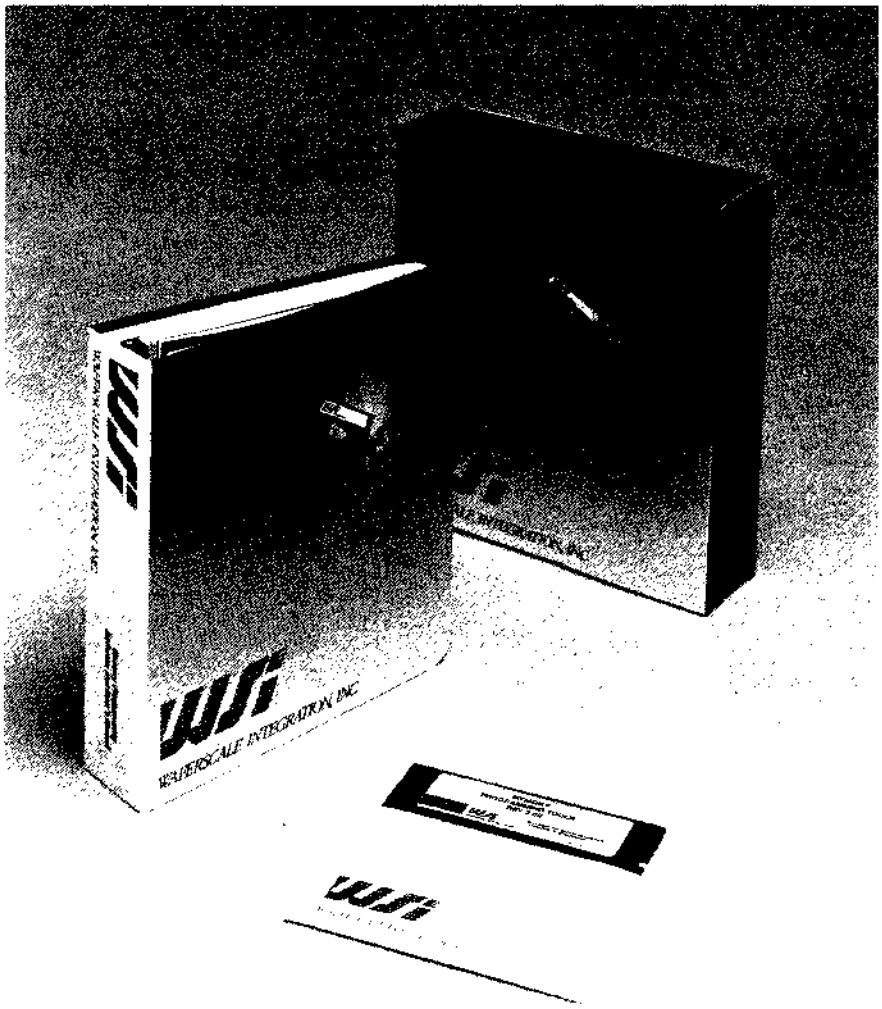
Product	Description
Memory-SILVER	WSI EPROM/RPROM Programming Software, User's Manual, WSI-Support.
Memory-GOLD	Contains Memory-SILVER, WS6000 MagicPro Programmer, WSI-Support.
WSI-Support	12-Month Software Update Service, Access to WSI's 24-Hour Electronic Bulletin Board, and Hotline to WSI System Application Experts.

Memory-GOLD

Contents

- ❑ Memory Programming Software
- ❑ Programmer user's manual
- ❑ WSI-SUPPORT agreement.
- ❑ WS6000 MagicPro™ Programmer.

Memory-SILVER



Contents

- ❑ Memory Programming Software
- ❑ Programmer user's manual
- ❑ WSI-SUPPORT agreement.

WAFERSCALE INTEGRATION, INC.

Programmable System™ Device

PAC1000

PSD Development System

Description

PAC1000-GOLD/PAC1000-SILVER is a complete set of IBM-PC-based development tools. They provide the integrated easy-to-use environment to support the PAC1000 program development and device programming.

The tools run on an IBM-PC XT, AT or compatible computer running MS-DOS version 3.1 or later.

PACSEL

PACSEL is the PAC1000 system entry language. It has the following features:

- ❑ Enables specification of up to three parallel operations:
  - — Program control operation
  - — CPU operation
  - — Out Control operation

  General Syntax:
  Label: Program Control, CPU, Out Control;
- ❑ Enables mixing of three source language types in one instruction:
  - — High Level Language
  - — Assembler
  - — Microcode
- ❑ Specific instructions support unique PAC1000 architecture features available in all three source language types.
- ❑ Links unlimited amounts of modules.

PACSIM

PACSIM is a functional simulator and software debugger. It has the following features:

- ❑ Clock driven functional simulator.
- ❑ Provides trace capabilities on internal states (Registers, Flags, Pins and more).
- ❑ Provides breakpoint capabilities on any internal state of the PAC1000.
- ❑ Supports batch mode simulation.
- ❑ Provides waveform analysis.
- ❑ On-line HELP available at any level.

PACPRO

PACPRO is the interface software that enables the user to program a PAC1000 microcontroller on the WS6000 MagicPro™ programmer. The PACPRO enables the user to load the program into the programmer and to execute the following operations:

- ❑ Help
- ❑ Upload RAM from PAC
- ❑ Load RAM from disk
- ❑ Write RAM to FILE
- ❑ Display PAC data
- ❑ Blank test PAC
- ❑ Verify PAC
- ❑ Program PAC
- ❑ Configuration
- ❑ Quit

IMPACT

IMPACT is the interface manager to the PAC1000 tools. IMPACT enables the user to access PACSEL, PACSIM, PACPRO, DOS and an editor with a menu driven interface. File specification can be done without extension enabling the user to use the same name throughout the design. A HELP window is available on-line giving information on all the needed steps at each level.

5

WS6000 MagicPro™ Programmer

MagicPro is an engineering development tool designed to program all WSI programmable products (EPROMs, RPROMs, PAC1000, MAP168, PSD301 and SAM448). It is used within the IBM-PC and compatible environment. The MagicPro consists of a short plug-in board and a Remote Socket Adaptor (RSA). It occupies a short expansion slot in the PC. The RSA has two ZIF-DIP sockets that will support WSI's 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil DIP packages without adaptors. Other packages are supported using adaptors.

WS6010 Socket Adaptor

The WS6010 is a socket adaptor that mounts on the MagicPro RSA and adapts the PAC1000 in an 88-pin CPGA package to the programmer.

WS6013 Socket Adaptor

The WS6013 is a socket adaptor that mounts on the MagicPro RSA and adapts the PAC1000 in a 100-pin QFP package to the programmer.

WSI-Support

WSI provides on-going support for users of PAC1000-GOLD/PAC1000-SILVER. For the first year, software and programmer updates are included at no charge. After that, the user may purchase the WSI-Support agreement to continue to receive the latest software releases.

Ordering Information

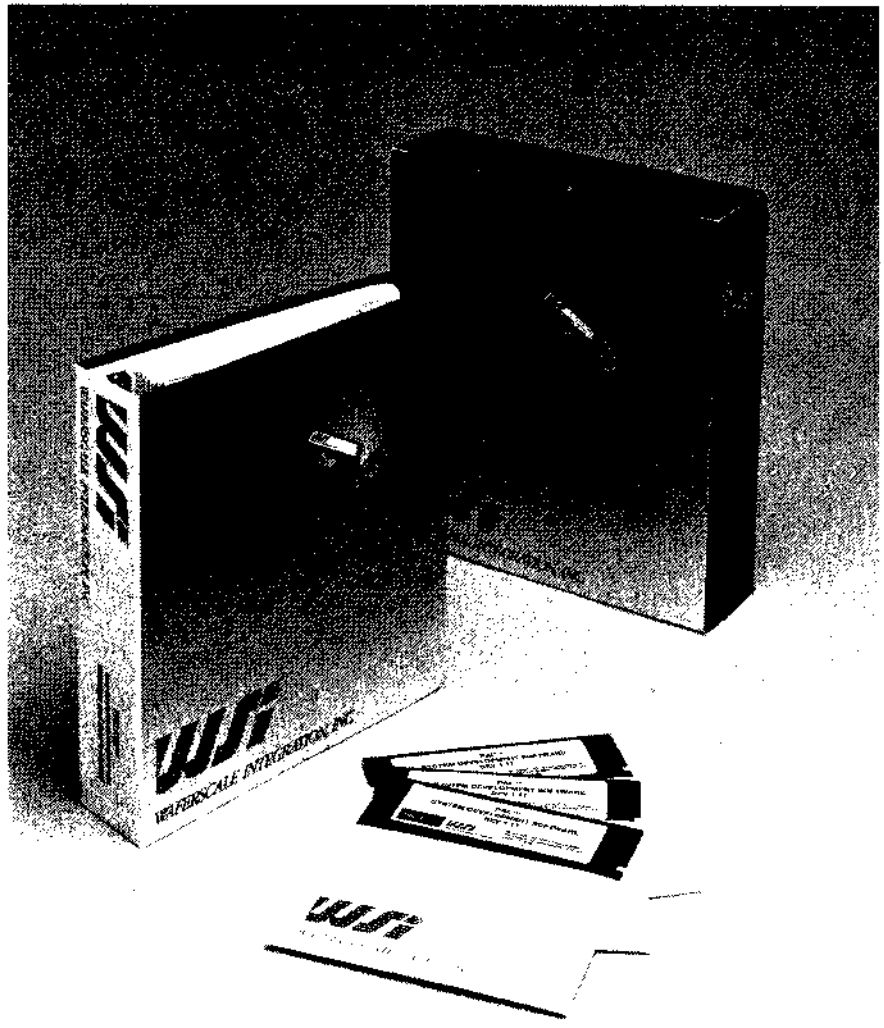
Product	Description
PAC1000-SILVER	Contains PAC1000 Software (PACSEL, PACSIM, PACPRO, and IMPACT), Software User's Manual, WSI-Support.
PAC1000-GOLD	Contains PAC1000-SILVER, WS6000 MagicPro Programmer, WSI-Support.
WSI-Support	12-Month Software Update Service, Access to WSI's 24-Hour Electronic Bulletin Board, and Hotline to WSI System Application Experts.

PAC1000-GOLD

Contents

- PACSEL
  System design entry language and program linker.
- PACSIM
  Functional simulator and software debugger.
- PACPRO
  Interface software to PAC1000 device programmer (MagicPro™).
- IMPACT
  Interface manager for PAC1000 microcontroller development tools.
- Software user's manual.
- WSI-SUPPORT agreement.
- WS6000 MagicPro Programmer.

PAC1000-SILVER



Contents

- ❑ PACSEL
  System design entry language and program linker.
- ❑ PACSIM
  Functional simulator and software debugger.
- ❑ PACPRO
  Interface software to PAC1000 device programmer (MagicPro™).
- ❑ IMPACT
  Interface manager for PAC1000 microcontroller development tools.
- ❑ Software user's manual.
- ❑ WSI-SUPPORT agreement.

Description

MAP168-GOLD/MAP168-SILVER is a complete set of IBM-PC-based development tools. They provide the integrated easy-to-use environment to support the MAP168 program development and device programming.

The tools run on an IBM-PC XT, AT or compatible computer running MS-DOS version 3.1 or later.

MAPLE

MAPLE is the MAP168 Locator Editor. It has the following features:

- ❑ Simple Menu Driven Commands for selecting different configurations of the MAP168:
  - — Byte wide or word wide operation.
  - — Address or Chip Select Input (CSI) Mode.
  - — PAD security option.
- ❑ Generating the PAD programming data that maps the 8 segments of EPROM, two segments of SRAM and eight Chip Selects Outputs to the user's address space.
- ❑ Combining all the different files to be programmed into the EPROM segments.

MAPPRO

MAPPRO is the interface software that enables the user to program a MAP168 device on the WS6000 MagicPro™ programmer. The MAPPRO enables the user to load the program into the programmer and to execute the following operations:

- ❑ Help
- ❑ Upload RAM from MAP
- ❑ Load RAM from disk
- ❑ Write RAM to FILE
- ❑ Display MAP data
- ❑ Blank test MAP
- ❑ Verify MAP
- ❑ Program MAP
- ❑ Configuration
- ❑ Quit

WS6000 MagicPro™ Programmer

The WS6000 MagicPro Programmer is an engineering development tool designed to program all WSI programmable products (EPROMs, RPROMs, PAC1000, MAP168, PSD301 and SAM448). It is used within the IBM-PC and compatible environment. The MagicPro consists of a short plug-in board and a Remote Socket Adaptor (RSA). It occupies a short expansion slot in the PC. The RSA has two ZIF-DIP sockets that will support WSI's 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil DIP packages without adaptors. Other packages are supported using adaptors.

WS6003 Socket Adaptor

The WS6003 is a socket adaptor that mounts on the MagicPro RSA and adapts the MAP168 in 44-pin CLDCC, PLDCC or CLLCC packages to the programmer.

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WS6011 Socket Adaptor

The WS6011 is a socket adaptor that mounts on the MagicPro RSA and adapts the MAP168 in a 44-pin PGA package to the programmer.

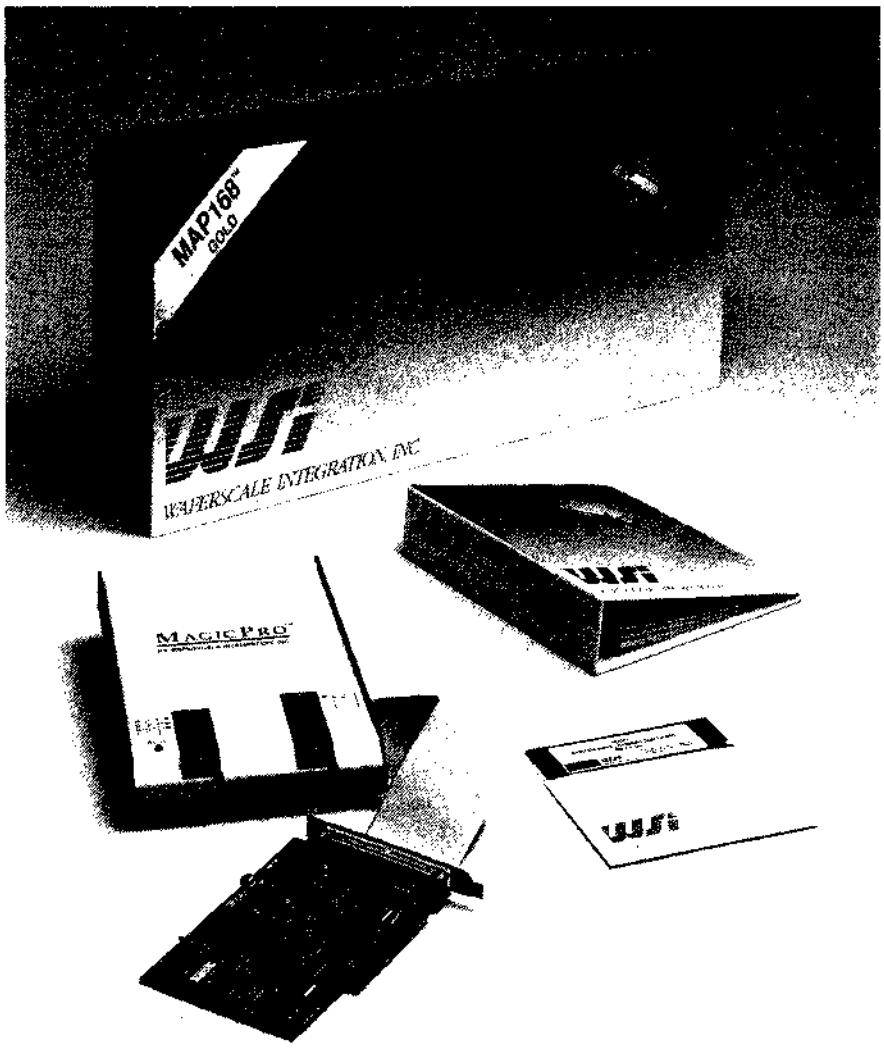
WSI-Support

WSI provides on-going support for users of MAP168-GOLD/MAP168-SILVER. For the first year, software and programmer updates are included at no charge. After that, the user may purchase the WSI-Support agreement to continue to receive the latest software releases.

Ordering Information

Product	Description
MAP168-SILVER	Contains MAP168 Software (MAPLE-MAP and MAPPRO), Software User's Manual, WSI-Support.
MAP168-GOLD	Contains MAP168-SILVER, WS6000 MagicPro Programmer, WSI-Support.
WSI-Support	12-Month Software Update Service, Access to WSI's 24-Hour Electronic Bulletin Board, and Hotline to WSI System Application Experts.

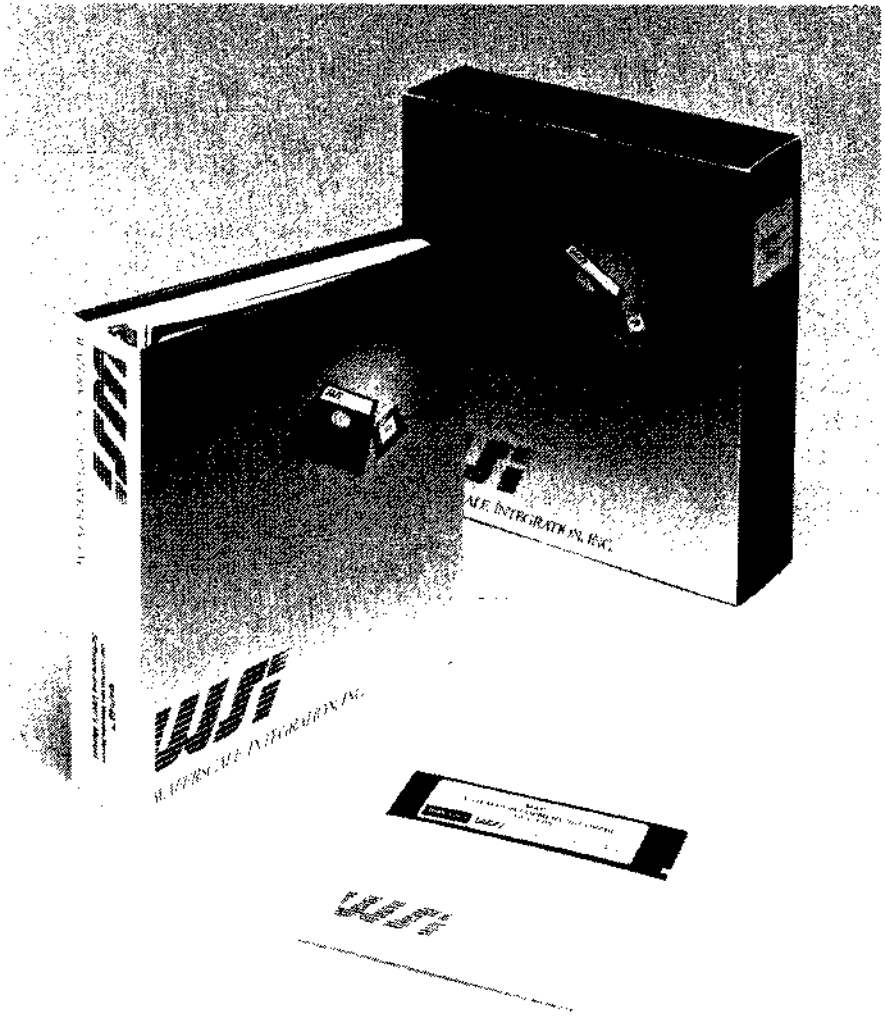
MAP168-GOLD



Contents

- ❑ MAPLE-MAP Locator editor.
- ❑ MAPPRO
  Interface software to MAP168 device programmer (MagicPro™).
- ❑ Software user's manual.
- ❑ WSI-SUPPORT agreement.
- ❑ WS6000 MagicPro Programmer.

MAP168-SILVER



Contents

- ❑ MAPLE-MAP Locator editor.
- ❑ MAPPRO
  Interface software to MAP168 device programmer (MagicPro™).
- ❑ Software user's manual.
- ❑ WSI-SUPPORT agreement.

WAFERSCALE INTEGRATION, INC.

Programmable System™ Device

SAM448

PSD Development System

Description

SAM448-GOLD/SAM448-SILVER is a complete set of IBM-PC-based development tools. They provide the integrated easy-to-use environment to support the SAM448 program development and device programming.

The tools run on an IBM-PC XT, AT or compatible computer running MS-DOS version 3.1 or later.

ASMILE

ASMILE is the SAM448 system entry language. It has the following features:

- ❑ State Machine Design Entry.
- ❑ Assembly Design Entry Language.
- ❑ User Definable Macros

SAMSIM

SAMSIM is an interactive functional simulator with Virtual Logic Analyzer Interface:

- ❑ Clock driven functional simulator.
- ❑ Provides trace capabilities on internal states (Registers, Flags, Pins and more).
- ❑ Displays input and output waveforms interactively providing such features as multiple zoom levels, split screens and differential time display.
- ❑ Line disassembler converts the actual code back into the original Assembly source code.
- ❑ On-line HELP available at any level.

SDP

The SAM Design Processor (SDP) takes an assembly file and creates an optimized JEDEC file for the SAM448. The SDP first expands macros that have been defined by the user. It then parses the design, listing any syntax or correction errors in an Error Log file. Next it minimizes the Boolean expressions that define the transition conditions. Finally, it fits the design into the SAM448, generating a JEDEC file.

SAMPRO

SAMPRO is the interface software that enables the user to program a SAM448 device on the WS6000 MagicPro™ programmer. The SAMPRO enables the user to load the program into the programmer and to execute the following operations:

- ❑ Help
- ❑ Upload RAM from SAM
- ❑ Load RAM from disk
- ❑ Write RAM to FILE
- ❑ Display SAM data
- ❑ Blank test SAM
- ❑ Verify SAM
- ❑ Program SAM
- ❑ Configuration
- ❑ Quit

SAMPLUS

SAMPLUS is the interface manager to the SAM448 software tools. SAMPLUS enables the user to access ASMILE, SAMSIM, SDP, SAMPRO, DOS and an editor with a menu driven interface. File specification can be done without extension enabling the user to use the same name throughout the design. A HELP window is available on-line giving information on all the needed steps at each level.

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WS6000 MagicPro™ Programmer

MagicPro is an engineering development tool designed to program all WSI programmable products (EPROMs, RPROMs, PAC1000, MAP168, PSD301 and SAM448). It is used within the IBM-PC and compatible environment. The MagicPro consists of a short plug-in board and a Remote Socket Adaptor (RSA). It occupies a short expansion slot in the PC. The RSA has two ZIF-DIP sockets that will support WSI's 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil DIP packages without adaptors. Other packages are supported using adaptors.

WS6008 Socket Adaptor

The WS6008 is a socket adaptor that mounts on the MagicPro RSA and adapts the SAM448 in a 28 pin DIP package to the programmer.

WS6009 Socket Adaptor

The WS6009 is a socket adaptor that mounts on the MagicPro RSA and adapts the SAM448 in a 28-pin PLDCC/CLDCC/CLLCC package to the programmer.

WSI-Support

WSI provides on-going support for users of SAM448-GOLD/SAM448-SILVER. For the first year, software and programmer updates are included at no charge. After that, the user may purchase the WSI-Support agreement to continue to receive the latest software releases.

Ordering Information

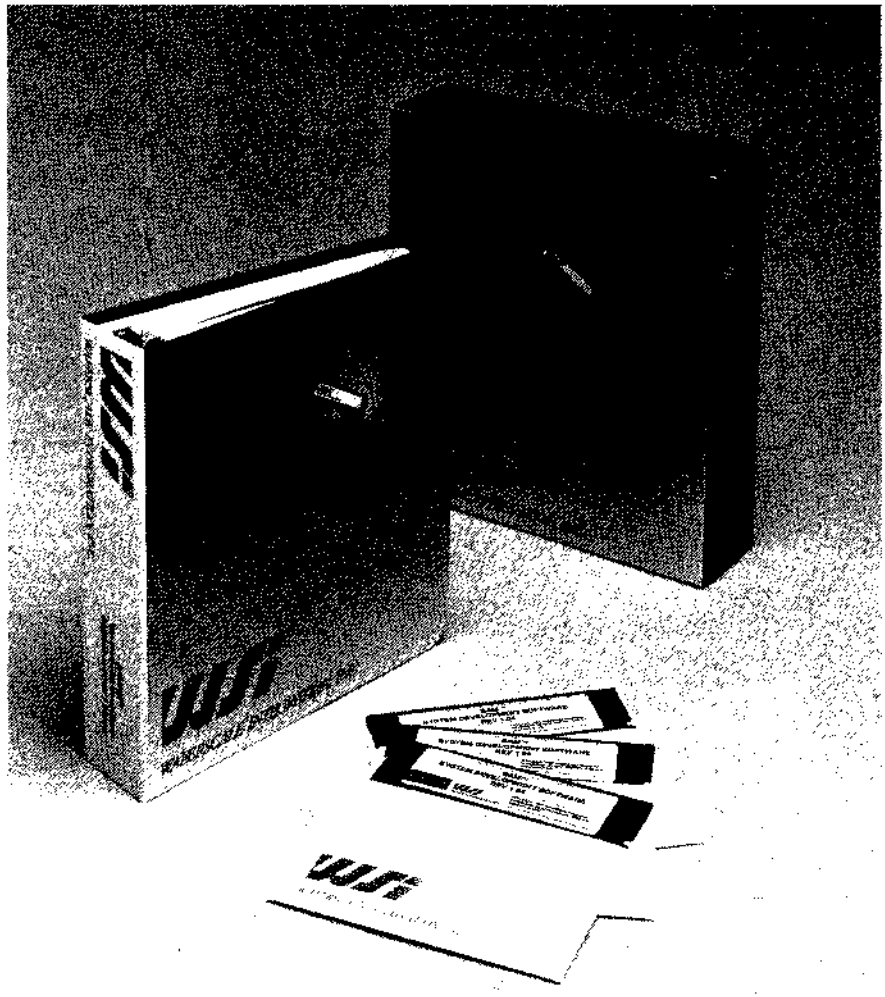
Product	Description
SAM448-SILVER	Contains SAM448 Software (ASMILE, SAMSIM, SDP, SAMPRO and SAMPLUS), Software User's Manual, WSI-Support.
SAM448-GOLD	Contains SAM448-SILVER, WS6000 MagicPro Programmer, WSI-Support.
WSI-Support	12-Month Software Update Service, Access to WSI's 24-Hour Electronic Bulletin Board, and Hotline to WSI System Application Experts.

SAM448-GOLD

Contents

- ASMILE
  SAM design entry language.
- SAMSIM
  Interactive Functional simulator with Virtual Logic Analyzer user interface.
- SDP
  SAM Design Processor Compiles the User's program to fit into the SAM448 Device.
- SAMPRO
  Interface software to SAM448 device programmer (MagicPro™).
- SAMPLUS
  Interface manager to SAM448 development tools.
- Software user's manual.
- WSI-SUPPORT agreement.
- WS6000 MagicPro Programmer.

SAM448-SILVER



Contents

- ASMILE
  SAM design entry language.
- SAMSIM
  Interactive Functional simulator with Virtual Logic Analyzer user interface.
- SDP
  SAM Design Processor Compiles the User's program to fit into the SAM448 Device.
- SAMPRO
  Interface software to SAM448 device programmer (MagicPro).
- SAMPLUS
  Interface manager to SAM448 development tools
- Software user's manual.
- WSI-SUPPORT agreement.

MAGICPRO™ MEMORY AND PSD PROGRAMMER

KEY FEATURES

- **Programs All WSI CMOS Memory and PSD Products and All Future Programmable Products**
- **Programs 24, 28, 32 and 40 Pin Standard 600 Mil or Slim 300 Mil Dip Packages Without Adaptors**
- **Programs LCC, PGA and QFP Packaged Product by Using Adaptors**
- **Easy-to-Use Menu-Driven Software**
- **Compatible with IBM PC/XT/AT Family of Computers (and True Plug-Compatible)**

GENERAL DESCRIPTION

MAGICPRO™ is an engineering development tool designed to program existing WSI EPROMs, RPROMs, Programmable System Devices, and future WSI programmable products. It is used within the IBM-PC® and compatible computers. The MAGICPRO™ is meant to bridge the gap between the introduction of a new WSI programmable product and the availability of programming support from programmer manufacturers (e.g., Data I/O, etc.). The MAGICPRO™ programmer and accompanying software enable quick programming of newly released WSI programmable products, thus accelerating the system design process.

The MAGICPRO™ plug-in board is integrated easily into the IBM-PC®. It occupies a short expansion slot and its software requires only 256K bytes of computer memory. The two external ZIF-Dip sockets in the Remote Socket Adaptor (RSA) support 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil Dip packages without adaptors. LCC, PGA and QFP packages are supported using adaptors.

Many features of the MAGICPRO™ Programmer show its capabilities in supporting WSI's future products. Some of these are:

— 24 to 40 pin JEDEC Dip pinouts
— 1 Meg. address space (20 address lines)
— 16 data I/O lines

The MAGICPRO™ menu driven software makes using different features of the MAGICPRO™ an easy task. Software updates are done via floppy disk which eliminates the need for adding a new memory device for system upgrading. Please call 800-TEAM-WSI for information regarding programming WSI products not listed herein. The MAGICPRO™ reads Intel Hex format for use with assemblers and compilers.

MAGICPRO™ COMMANDS

— Help
— Upload RAM from device
— Load RAM from disk
— Write RAM to disk
— Display RAM data
— Edit RAM
— Move/copy RAM
— Fill RAM
— Blank test device
— Verify device
— Program device
— Select device
— Configuration
— Quit MagicPro™

WSI PRODUCTS

WS57C191/191B/291/291B	2K × 8	RPROM
WS57C43/43B	4K × 8	RPROM
WS57C49/49B	8K × 8	RPROM
WS57C51/51B	16K × 8	RPROM
WS27C64F/L	8K × 8	EPROM
WS57C64F	8K × 8	EPROM
WS57C65	4K × 16	EPROM
WS57C66	4K × 16	EPROM
	(Mux I/O, 28 Pin DIP)	
WS27C128F/L	16K × 8	EPROM
WS57C128F	16K × 8	EPROM
WS27C256F/L	32K × 8	EPROM
WS57C256F	32K × 8	EPROM
WS57C257F	16K × 16	EPROM
WS27C512F/L	64K × 8	EPROM
WS27C010L	128K × 8	EPROM
MAP168		
PAC1000		
SAM448		
PSD301		

TECHNICAL INFORMATION

- Size: IBM-PC® short length card
- Port Address Location: 100H to 1FFH—default 140H (If a conflict exists with this address space, the address location can be changed in software and with the switches on the plug-in board.)
- System Memory Requirements: 256K bytes of RAM
- Power: +5 Volts, 0.03 Amp.; +12 Volts, 0.04 Amp.
- Remote Socket Adaptor (RSA): The RSA contains two ZIF-Dip sockets that are used to program and read WSI programmable products. The 32 pin ZIF-Dip socket supports 24, 28 and 32 pin standard 600 mil or slim 300 mil Dip packaged product. The 40 pin ZIF-Dip socket supports all 40 pin Dip packages. Adaptor sockets are available for LCC, PGA and QFP packages.

ORDERING INFORMATION

The WS6000 MAGICPRO™ System contains:

- MAGICPRO™ IBM-PC® plug-in programmer board
- MAGICPRO™ Remote Socket Adaptor and cable
- MAGICPRO™ Operating System Floppy Disk and Operating Manual

MAGICPRO™ Adaptors include:

- WS6001 28 Pin CLLCC Package adaptor for memory.
- WS6003 44 Pin PLDCC/CLDCC/CLLCC package adaptor for MAP168.
- WS6008 28 Pin 0.3" wide DIP adaptor for SAM448.
- WS6009 28 Pin PLDCC/CLDCC/CLLCC package adaptor for SAM448.
- WS6010 88 Pin PGA package adaptor for PAC1000.
- WS6011 44 Pin PGA package adaptor for MAP168.
- WS6012 32 Pin CLDCC package adaptor for memory.
- WS6013 100 Pin QFP package adaptor for PAC1000.
- WS6014 44 Pin CLDCC/PLDCC package adaptor for MAP168 and PSD301.
- WS6015 44 Pin PGA package adaptor for MAP168 and PSD301.

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IBM-PC® is a registered trademark of IBM Corporation.

MAGICPRO™ is a trademark of WaferScale Integration, Inc.

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

CMOS LOGIC PRODUCTS

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 800-562-6363.

WAFERSCALE INTEGRATION, INC.

CMOS 4-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **2901 Architecture in CMOS**
- **Drop-In Replacement for 2901C**
- **Expandable in 4-Bit Increments**
- **DESC SMD No. 5962-88535 01QA**
- **High Speed**
  — Maximum Clock Frequency of 43 MHz (23 ns)
- **Very Low Power**
  — 30 mA Maximum (Commercial Temperature)
- **EPI Processing**
  — Latch-Up Immunity Over 200 mA

GENERAL DESCRIPTION

The WS5901 is a 4-bit high-speed microprocessor which contains the logic of a Bipolar 2901 bit slice processor.

This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the 5901 is manufactured, provides significant performance improvements over its counterpart. While operating as fast as a 2901C based system, the WS5901C requires less than 8% of the power consumed by its Bipolar equivalent. The WS5901D is a 25% speed enhancement over the "C" speed.

The WS5901 is also a macro cell in the WaferScale cell library. As such it can be combined with other cells to build High Performance CMOS Application Specific Integrated Circuits.

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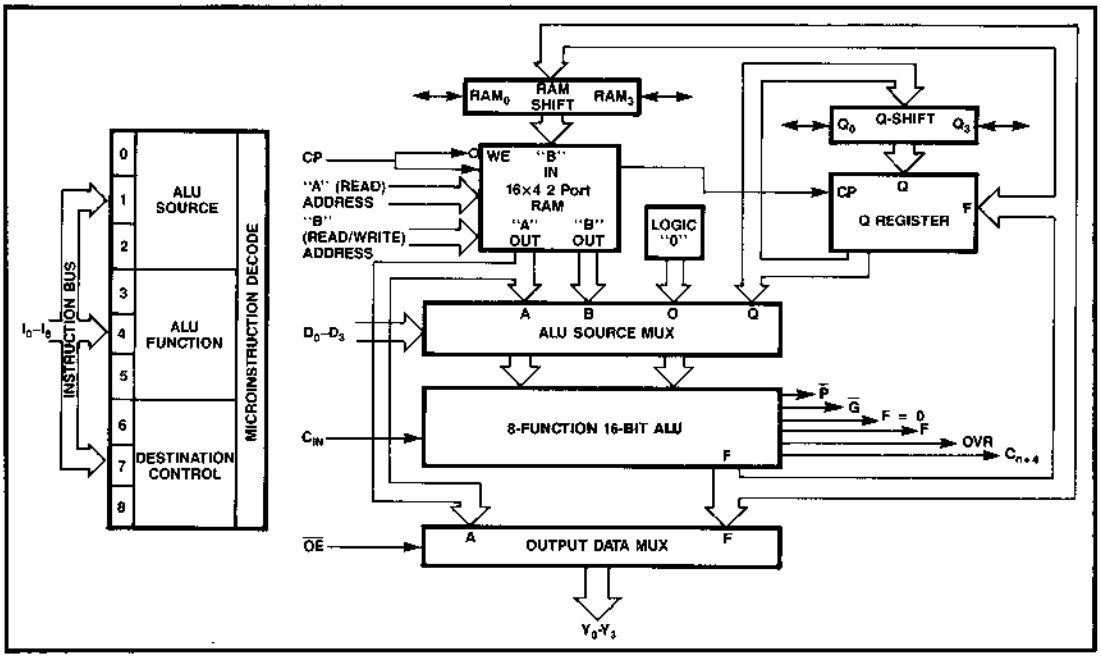
FUNCTIONAL BLOCK DIAGRAM

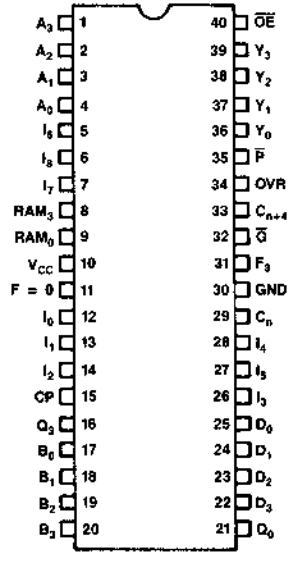


PIN DESCRIPTION

Signal Name	I/O	Description
A0-3	I	Addresses which select the word of on board RAM which is to be displayed through the A port.
B0-3	I	Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low.
I0-8	I	Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678).
Q3 , RAM3	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM 3 pin and the MSB of the Q-register is available on the Q3 pin. Otherwise, the pins appear as inputs When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4).
Qo, RAMo	I/O	Shift lines similar to Q3 and RAM3. However the description is applied to the LSB of RAM and the Q-register.
D0-D3	I	These four direct data inputs can be selected as a data source for the ALU. DO is the LSB.
Y0-Y3	O	These four three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678
$\overline{OE}$	I	When high, the Y outputs are in the high impedance state When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y3 , as determined by I678.
$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the ALU.
OVR	O	This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
F = 0	O	This output, when high, indicates the result of an ALU operation is zero.
F3	O	The most significant ALU output bit.
Cn	I	The carry-in to the ALU.
Cn + 4	O	The carry-out of the ALU.
CP	I	This clock signal is applied to the A and B-port latches, RAM, and Q-register. The clock low time is the write enable to the on-board 16 x 4 RAM, including set-up time for the A and B port registers. The A and B port and Q-register outputs change on the clock low-to-high transition.

PIN DESIGNATOR

Dual-In-Line Package



TOP

ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
Latch-Up Protection . . . . . >200 mA
ESD Protection . . . . . > ±2000V

*Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC READ CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OH} = −3.4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	Y_0–Y_3	I_{OL} = 20 mA Comm'l		0.4	
			All Others	I_{OL} = 16 mA Mil			
V_{IH}	Input High Voltage	Guaranteed Input High Voltage			2.0		
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = Gnd or V_{CC}			−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−40	40	
I_{CC}	Power Supply Current	V_{CC} = Max (Note 2)	Comm'l (0°C to +70°C)			30	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 2) 100 ns System Cycle

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR

The four signals, G, P, C_{n+4} and OVR are designed to indicate carry and overflow conditions when the WS5901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0}+C_n$	$\overline{P_3P_2P_1P_0}+C_n$
4	R ∧ S	LOW	$\overline{G_3+G_2+G_1+G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R}_i$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$ equations, but substitute $\overline{R}_i$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$P_3G_2+P_3P_2G_1+P_3P_2P_1G_0$	$\overline{G_3+P_3G_2+P_3P_2G_1 + P_3P_2P_1P_0(G_0+\overline{C_n})}$	See note 1

NOTES: 1) $(P_2 + G_2P_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n) \forall (\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n)$
2) + = OR

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 1: ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EXOR	$R \triangledown S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

Table 2. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care.
B = Register Addressed by B inputs.
DOWN is toward LSB. UP is toward MSB.

Table 3. ALU Destination Control.

		I_{210} (Octal Code)							
		0	1	2	3	4	5	6	7
I_{543} (Octal Code)	ALU Function	ALU Source (R, S)							
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \triangledown Q$	$A \triangledown B$	Q	B	A	$D \triangledown A$	$D \triangledown Q$	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; − = Minus, ∨ = OR; ∧ = AND, $\triangledown$ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1, and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4, and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS5901 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (Cn = 0) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \triangledown Q$
6 1		$A \triangledown B$
6 5		$D \triangledown A$
6 6		$D \triangledown Q$
7 0	EX-NOR	$\overline{A \triangledown Q}$
7 1		$\overline{A \triangledown B}$
7 5		$\overline{D \triangledown A}$
7 6		$\overline{D \triangledown Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Table 5. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6. ALU Arithmetic Mode Functions.

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WS5901C COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901C over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	31 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	32 MHz
Minimum Clock Low Time	15 ns
Minimum Clock High Time	15 ns
Minimum Clock Period	31 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	23 ns
From $\overline{OE}$ High to output disable	23 ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

FROM INPUT / TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	40	40	40	37	40	40	40	—	ns
D_0–D_3	30	30	30	30	38	30	30	—	
C_n	22	22	20	—	25	22	25	—	
I_{012}	35	35	35	37	37	35	35	—	
I_{345}	35	35	35	35	38	35	35	—	
I_{678}	25	—	—	—	—	—	26	26	
A BYPASS ALU (I = 2XX)	35	—	—	—	—	—	—	—	
CLOCK	35	35	35	35	35	35	35	28	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

CP / INPUT	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	15	1 (Note 3)	30 (Note 4)	1	ns
B Destination Address	15	DO NOT CHANGE (Note 2)		1	
D_0–D_3	—	—	25	0	
C_n	—	—	20	0	
I_{012}	—	—	30	0	
I_{345}	—	—	30	0	
I_{678}	10	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	—	—	12	0	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here.

WS5901CYM MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901C over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	32 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	31 MHz
Minimum Clock Low Time	17 ns
Minimum Clock High Time	15 ns
Minimum Clock Period	32 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	25 ns
From $\overline{OE}$ High to output disable	25 ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

FROM INPUT \ TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	48	48	48	44	48	48	48	—	ns
D_0–D_3	37	37	37	34	40	37	37	—	
C_n	25	25	21	—	28	25	28	—	
I_{012}	40	40	40	44	44	40	40	—	
I_{345}	40	40	40	40	40	40	40	—	
I_{678}	29	—	—	—	—	—	29	29	
A BYPASS ALU (I = 2XX)	40	—	—	—	—	—	—	—	
CLOCK	40	40	40	40	40	40	40	33	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	15	1 (Note 3)	32 (Note 4)	2	ns
B Destination Address	15	DO NOT CHANGE (Note 2)		2	
D_0–D_3	—	—	25	0	
C_n	—	—	20	0	
I_{012}	—	—	30	0	
I_{345}	—	—	30	0	
I_{678}	10	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	—	—	12	0	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here.

WS5901D COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901D over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	23 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	43 MHz
Minimum Clock Low Time	11 ns
Minimum Clock High Time	11 ns
Minimum Clock Period	23 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	14 ns
From $\overline{OE}$ High to output disable	16 ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

FROM INPUT / TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	30	30	30	28	30	30	30	—	ns
D_0–D_3	21	20	20	20	24	21	22	—	
C_n	17	17	14	—	19	16	18	—	
I_{012}	26	25	24	24	25	24	25	—	
I_{345}	26	24	24	24	26	24	26	—	
I_{678}	16	—	—	—	—	—	21	21	
A BYPASS ALU (I = 2XX)	24	—	—	—	—	—	—	—	
CLOCK	24	23	23	23	24	24	24	19	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

CP / INPUT	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	10	0 (Note 3)	21 (Note 4)	1	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		1	
D_0–D_3	—	—	16	0	
C_n	—	—	13	0	
I_{012}	—	—	19	0	
I_{345}	—	—	19	0	
I_{678}	7	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	—	—	9	1	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here.

WS5901DYM MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901D over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	27 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	37 MHz
Minimum Clock Low Time	15 ns
Minimum Clock High Time	12 ns
Minimum Clock Period	27 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	16 ns
From $\overline{OE}$ High to output disable	18 ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

FROM INPUT \ TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	33	33	33	33	33	33	33	—	ns
D_0–D_3	24	23	23	21	25	24	25	—	
C_n	18	17	14	—	19	17	19	—	
I_{012}	28	27	26	28	29	27	27	—	
I_{345}	27	27	26	26	27	26	27	—	
I_{678}	18	—	—	—	—	—	21	21	
A BYPASS ALU (I = 2XX)	26	—	—	—	—	—	—	—	
CLOCK	27	26	26	25	27	26	27	20	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

CP \ INPUT	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	12	0 (Note 3)	25 (Note 4)	2	ns
B Destination Address	12	DO NOT CHANGE (Note 2)		2	
D_0–D_3	—	—	16	0	
C_n	—	—	13	0	
I_{012}	—	—	19	0	
I_{345}	—	—	19	0	
I_{678}	9	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	—	—	9	0	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here.

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS5901CP	C	40 Pin Plastic DIP, 0.6"	P1	Comm'l	Standard
WS5901CYM	C	40 Pin CERDIP, 0.6"	Y1	Military	Standard
WS5901CYMB	C	40 Pin CERDIP, 0.6"	Y1	Military	MIL-STD-883C
WS5901DP	D	40 Pin Plastic DIP, 0.6"	P1	Comm'l	Standard
WS5901DYM	D	40 Pin CERDIP, 0.6"	Y1	Military	Standard
WS5901DYMB	D	40 Pin CERDIP, 0.6"	Y1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

CMOS 16-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **Four CMOS 2901 Type Devices in a Single Package**
- **On Board Look-Ahead Carry Generator**
- **Low CMOS Power**
  — 225 mW
- **High Speed Operation**
  — 31 ns Read-Modify-Write
- **Fully Firmware Compatible with the Bipolar Device Configuration of Four 2901s and One 2902A**

GENERAL DESCRIPTION

The WS59016 is a 16-bit high-speed microprocessor which combines the functions of four 2901 4-bit slice processors and distributed look-ahead carry generation on a single High Performance CMOS device.

This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the WS59016 is manufactured, provides significant performance improvements over an equivalent Bipolar device configuration. While operating faster than a 2901C based system, the WS59016 requires less than 3% of the power consumed by an equivalent Bipolar system.

The WS59016 is also available as a macro cell in the WaferScale cell library. As such it can be combined with other cells to build Application Specific Integrated Circuits.

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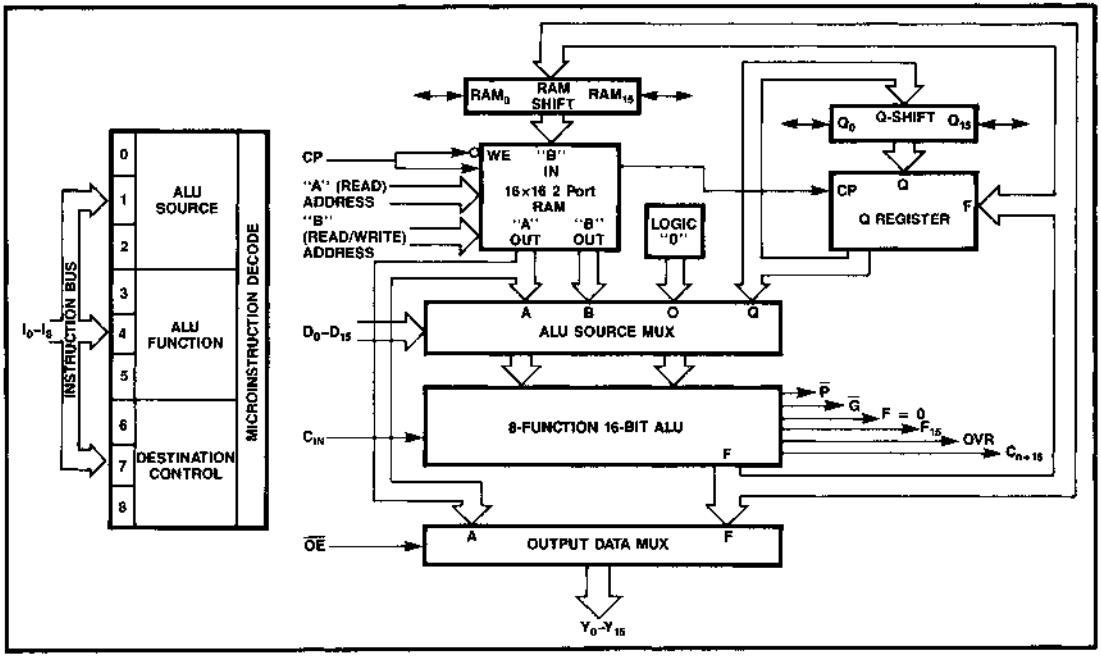
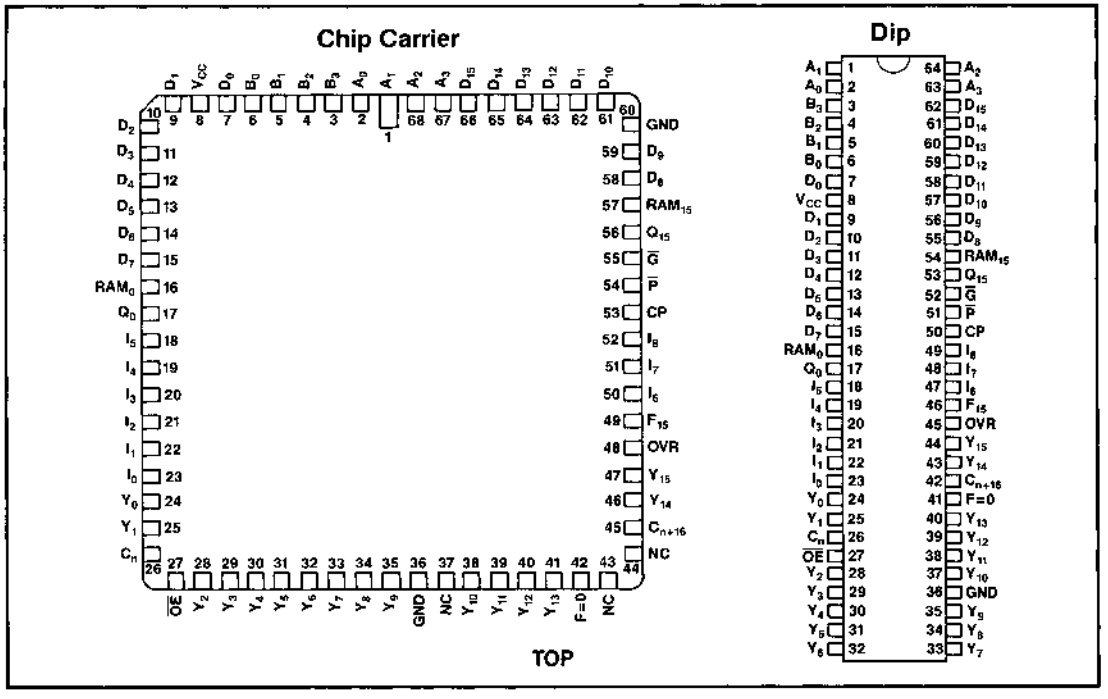
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Signal Name	I/O	Description
A0-3	I	Addresses which select the word of on board RAM which is to be displayed through the A port.
B0-3	I	Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low
I0-8	I	Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678)
Q15, RAM15	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM 15 pin and the MSB of the Q-register is available on the Q15 pin. Otherwise, the pins appear as inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4).
Q0, RAM0	I/O	Shift lines similar to Q15 and RAM15, however the description is applied to the LSB of RAM and the Q-register
D0-D15	I	These sixteen direct data inputs can be selected as a data source for the ALU. D0 is the LSB.
Y0-Y15	O	These sixteen three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678
$\overline{OE}$	I	When high, the Y outputs are in the high impedance state When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y15, as determined by I678.
$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the ALU.
OVR	O	This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
F = 0	O	This output, when high, indicates the result of an ALU operation is zero.
F15	O	The most significant ALU output bit
Cn	I	The carry-in to the ALU.
Cn + 16	O	The carry-out of the ALU
CP	I	This clock signal is applied to the A and B-port latches, RAM, and Q-register The clock low time is the write enable to the on-board dual port RAM, including set-up time for the A and B-port registers The A and B-port outputs change while the clock is high The Q-register is latched on the clock low-to-high transition.

PIN ORIENTATION



ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
Latch-Up Protection . . . . . >200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC READ CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OH} = −3.4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OL} = 12 mA Comm'l I_{OL} = 8 mA Mil		0.5	V
V_{IH}	Input High Voltage	Guaranteed Input High Voltage			2.0		
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = Gnd or V_{CC}			−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	Comm'l (0°C to +70°C)			45	mA
			Mil (−55°C to +125°C)			60	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+16}, and OVR

The four signals $\overline{G}$, $\overline{P}$, C_{n+16}, and OVR are designed to indicate carry and overflow conditions when the WS59016 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1

Definitions

$P_i = R_i + S_i$
$G_i = R_i \cdot S_i$
$P_{0-3} = P_0 \cdot P_1 \cdot P_2 \cdot P_3$ $\quad G_{0-3} = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0$
$P_{4-7} = P_4 \cdot P_5 \cdot P_6 \cdot P_7$ $\quad G_{4-7} = G_7 + P_7 \cdot G_6 + P_7 \cdot P_6 \cdot G_5 + P_7 \cdot P_6 \cdot P_5 \cdot G_4$
$P_{8-11} = P_8 \cdot P_9 \cdot P_{10} \cdot P_{11}$ $\quad G_{8-11} = G_{11} + P_{11} \cdot G_{10} + P_{11} \cdot P_{10} \cdot G_9 + P_{11} \cdot P_{10} \cdot P_9 \cdot G_8$
$P_{12-15} = P_{12} \cdot P_{13} \cdot P_{14} \cdot P_{15}$ $\quad G_{12-15} = G_{15} + P_{15} \cdot G_{14} + P_{15} \cdot P_{14} \cdot G_{13} + P_{15} \cdot P_{14} \cdot P_{13} \cdot G_{12}$
$C_{n+15} = G_{12-14} + P_{12-14} \cdot G_{8-11} + P_{12-14} \cdot P_{8-11} \cdot G_{4-7} + P_{12-14} \cdot P_{8-11} \cdot P_{4-7} \cdot G_{0-3}$
$P_{12-14} = P_{12} \cdot P_{13} \cdot P_{14}$ $\quad G_{12-14} = G_{14} + P_{14} \cdot G_{13} + P_{14} \cdot P_{13} \cdot G_{12}$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+16}	OVR
0	R + S	$\overline{P_{0-3} \cdot P_{4-7} \cdot P_{8-11} \cdot P_{12-15}}$	$\overline{G_{12-15} + P_{12-15} \cdot G_{8-11} + P_{12-15} \cdot P_{8-11} \cdot G_{4-7} + P_{12-15} \cdot P_{8-11} \cdot P_{4-7} \cdot G_{0-3}}$	$P \cdot C_n + G$	$C_{n+15} \oplus C_{n+16}$
1	S − R	← Same as R + S Equations except substitute $\overline{R}_i$ for R_i in definitions →			
2	R − S	← Same as R + S Equations except substitute $\overline{S}$ for S in definitions →			
3	R ∨ S	LOW	HIGH	LOW	LOW
4	R ∧ S	LOW	$\overline{G_{12-15} + G_{8-11} + G_{4-7} + G_{0-3}}$	HIGH	LOW
5	$\overline{R}$ ∧ S	LOW	Same as R ∧ S except substitute $\overline{R}$ for R in definition	HIGH	LOW
6	R ⊕ S	$\overline{P_{0-3} \cdot P_{4-7} \cdot P_{8-11} \cdot P_{12-15}}$	HIGH	LOW	LOW
7	$R \overline{\oplus} S$	Same as R⊕S except Substitute $\overline{R}$ for R in Definitions	HIGH	LOW	LOW

Note: 1) + = OR

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 1: ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EXOR S	$R \triangledown S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

Table 2. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}

X = Don't care.
B = Register Addressed by B inputs.
DOWN is toward LSB. UP is toward MSB.

Table 3. ALU Destination Control.

		I_{210} (Octal Code)							
		0	1	2	3	4	5	6	7
I_{543} (Octal Code)	ALU Function	ALU Source (R, S)							
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \triangledown Q$	$A \triangledown B$	Q	B	A	$D \triangledown A$	$D \triangledown Q$	D
7	REX-NORS	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; $\triangledown$ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1 and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4 and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS59016 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (CN = 0) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A ∧ Q
4 1		A ∧ B
4 5		D ∧ A
4 6		D ∧ Q
3 0	OR	A ∨ Q
3 1		A ∨ B
3 5		D ∨ A
3 6		D ∨ Q
6 0	EX-OR	A ▽ Q
6 1		A ▽ B
6 5		D ▽ A
6 6		D ▽ Q
7 0	EX-NOR	$\overline{A \triangledown Q}$
7 1		$\overline{A \triangledown B}$
7 5		$\overline{D \triangledown A}$
7 6		$\overline{D \triangledown Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$ ∧ Q
5 1		$\overline{A}$ ∧ B
5 5		$\overline{D}$ ∧ A
5 6		$\overline{D}$ ∧ Q

Table 5. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6. ALU Arithmetic Mode Functions.

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COMPETITIVE TIMING ANALYSIS

The following analysis compares the critical timing paths of a WS59016D vs. the equivalent Bipolar circuit implementation using four 2901C's and one 2902A.

As can be seen from this comparison, the WS59016 operates faster than even the theoretically achievable values of the Bipolar implementation. The actual values for the Bipolar circuit will be lengthened by the layout dependent interconnect delays between the individual devices. When these delays are taken into account, the WS59016 speed advantage becomes even greater.

TIMING COMPARISON
WS59016D vs 2901C w/2902A (Comm'l)

DATA PATH	CONTROL PATH
2901C w/ 2902A	2901C w/ 2902A
A, B Address → $\overline{P}$ or $\overline{G}$ = 37ns	I_{012} → $\overline{P}$ or $\overline{G}$ = 37ns
$\overline{P}$ or $\overline{G}$ → C = 9ns	$\overline{P}$ or $\overline{G}$ → C = 9ns
C → F = 0, $RAM_{0,15}$ = 25ns	C → F = 0, $RAM_{0,15}$ = 25ns
interconnect delay → = Xns	interconnect delay → = Xns
Total Delay → ≥ 71ns	Total Delay → ≥ 71ns
59016D	59016D
A, B Address → F = 0, $RAM_{0,15}$ = 46ns	I_{012} → F = 0, $RAM_{0,15}$ = 41ns
interconnect delay → = 0ns	interconnect delay → = 0ns
Total Delay → ≤ 46ns	Total Delay → ≤ 41ns

TIMING COMPARISON
WS59016D vs 2901C w/2902A (Military)

DATA PATH	CONTROL PATH
2901C w/ 2902A	2901C w/ 2902A
A, B Address → $\overline{P}$ or $\overline{G}$ = 44ns	I_{012} → $\overline{P}$ or $\overline{G}$ = 44ns
$\overline{P}$ or $\overline{G}$ → C = 11.5ns	$\overline{P}$ or $\overline{G}$ → C = 11.5ns
C → F = 0, $RAM_{0,15}$ = 28ns	C → F = 0, $RAM_{0,15}$ = 28ns
interconnect delay → = Xns	interconnect delay → = Xns
Total Delay → ≥ 83.5ns	Total Delay → ≥ 83.5ns
59016D	59016D
A, B Address → F15, $RAM_{0,15}$ = 56ns	I_{012} → F15, $RAM_{0,15}$ = 49ns
interconnect delay → = 0ns	interconnect delay → = 0ns
Total Delay → ≤ 56ns	Total Delay → ≤ 49ns

NOTE: This competitive analysis holds true for any 16 bit system which performs arithmetic operations. If arithmetic operations are not used, the Bipolar circuit can run faster than noted above.

COMMERCIAL RANGE AC CHARACTERISTICS (WS59016C)

The tables shown here specify the guaranteed performance of the WS59016C over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	67ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	15MHz
Minimum Clock Low Time	33ns
Minimum Clock High Time	33ns
Minimum Clock Period	67ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	25ns
From $\overline{OE}$ High to output disable	25ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM OUTPUT \ TO OUTPUT	Y	F15	C_{n+16}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM15	Q0, Q15	UNITS
A, B ADDRESS	69	69	60	68	71	69	71	–	ns
D0-D15	55	55	45	50	55	55	55	–	
Cn	38	38	27	–	42	38	42	–	
I_{012}	60	60	55	55	60	60	60	–	
I_{345}	60	60	55	55	60	60	60	–	
I_{678}	30	–	–	–	–	–	27	26	
A BYPASS ALU (I = 2XX)	45	–	–	–	–	–	–	–	
CLOCK	65	65	65	65	55	65	70	30	

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	15	2 (Note 3)	65 (Note 4)	1	ns
B Destination Address	15	DO NOT CHANGE (Note 2)		1	
D0-D15	–	–	50	0	
Cn	–	–	34	0	
I_{012}	–	–	55	0	
I_{345}	–	–	55	0	
I_{678}	15	DO NOT CHANGE (Note 2)		0	
RAM0, 15 and Q0, 15	–	–	20	4	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time Otherwise, erroneous operation may be the result.
3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H > L included here.

MILITARY RANGE AC CHARACTERISTICS (WS59016C)

The tables shown here specify the guaranteed performance of the WS59016C over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	80ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	12.5MHz
Minimum Clock Low Time	39ns
Minimum Clock High Time	39ns
Minimum Clock Period	80ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30ns
From $\overline{OE}$ High to output disable	30ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM OUTPUT \ TO OUTPUT	Y	F15	C_{n+16}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM15	Q0, Q15	UNITS
A, B ADDRESS	83	83	72	82	83	83	83	–	ns
D0-D15	66	66	54	60	66	66	66	–	
Cn	46	46	33	–	53	46	53	–	
I_{012}	72	72	66	66	72	72	72	–	
I_{345}	72	72	66	66	72	72	72	–	
I_{678}	36	–	–	–	–	–	31	31	
A BYPASS ALU (I = 2XX)	55	–	–	–	–	–	–	–	
CLOCK	78	78	78	78	66	78	78	36	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	20	2 (Note 3)	78 (Note 4)	2	ns
B Destination Address	20	DO NOT CHANGE (Note 2)		2	
D0-D15	–	–	60	0	
Cn	–	–	41	0	
I_{012}	–	–	66	0	
I_{345}	–	–	66	0	
I_{678}	20	DO NOT CHANGE (Note 2)		0	
RAM0, 15 and Q0, 15	–	–	25	5	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

COMMERCIAL RANGE AC CHARACTERISTICS (WS59016D)

The tables shown here specify the guaranteed performance of the WS59016D over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select) of A, B registers to end of cycle)	31 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	32 MHz
Minimum Clock Low Time	14 ns
Minimum Clock High Time	14 ns
Minimum Clock Period	40 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	24 ns
From $\overline{OE}$ High to output disable	22 ns

COMBINATION PROPAGATION DELAYS (C_L = 50PF)

FROM OUTPUT \ TO OUTPUT	Y	F15	C_{n+16}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0 RAM15	Q0 Q15	UNITS
A, B ADDRESS	46	46	44	43	46	46	44	—	ns
D0-D15	36	32	34	32	36	34	36	—	
C_n	32	29	24	—	32	28	32	—	
I_{012}	39	39	37	38	39	38	41	—	
I_{345}	39	38	37	37	39	38	41	—	
I_{678}	28	—	—	—	—	—	34	34	
A BYPASS ALU (I = 2XX)	34	—	—	—	—	—	—	—	
CLOCK	38	37	38	34	38	38	38	38	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B, Source Address	12	0 (Note 3)	23 (Note 4)	1	ns
B Destination Address	12	DO NOT CHANGE (Note 2)		1	
D0-D15	—	—	19	0	
C_n	—	—	16	0	
I_{012}	—	—	22	0	
I_{345}	—	—	22	0	
I_{678}	12	DO NOT CHANGE (Note 2)		0	
RAM0, 15 and Q0, 15	—	—	17	3	

NOTES:

1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H > L included here.

MILITARY RANGE AC CHARACTERISTICS (WS59016D)

The tables shown here specify the guaranteed performance of the WS59016D over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select) of A, B registers to end of cycle)	36 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	27 MHz
Minimum Clock Low Time	17 ns
Minimum Clock High Time	17 ns
Minimum Clock Period	47 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30 ns
From $\overline{OE}$ High to output disable	27 ns

COMBINATION PROPAGATION DELAYS (C_L = 50PF)

FROM OUTPUT \ TO OUTPUT	Y	F15	C_{n+16}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0 RAM15	Q0 Q15	UNITS
A, B ADDRESS	56	56	53	52	56	56	53	—	ns
D0-D15	43	39	42	39	43	42	43	—	
C_n	39	36	30	—	39	34	39	—	
I_{012}	48	48	46	47	48	47	49	—	
I_{345}	48	47	46	46	48	47	49	—	
I_{678}	34	—	—	—	—	—	42	42	
A BYPASS ALU (I = 2XX)	42	—	—	—	—	—	—	—	
CLOCK	47	46	47	42	47	47	47	47	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B, Source Address	16	0 (Note 3)	29 (Note 4)	2	ns
B Destination Address	16	DO NOT CHANGE (Note 2)		2	
D0-D15	—	—	23	0	
C_n	—	—	20	0	
I_{012}	—	—	27	0	
I_{345}	—	—	27	0	
I_{678}	16	DO NOT CHANGE (Note 2)		0	
RAM0, 15 and Q0, 15	—	—	21	4	

NOTES:

1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time Otherwise, erroneous operation may be the result
3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes After this transition the A address may be changed If it is not being used as a destination, the B address may also be changed If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H > L included here

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59016CB	C	64 Pin Ceramic Sidebrazed DIP, 0.9"	B1	Comm'l	Standard
WS59016CBMB	C	64 Pin Ceramic Sidebrazed DIP, 0.9"	B1	Military	MIL-STD-883C
WS59016CJ	C	68 Pin PLDCC	J1	Comm'l	Standard
WS59016CL	C	68 Pin CLDCC	N1	Comm'l	Standard
WS59016CLMB	C	68 Pin CLDCC	N1	Military	MIL-STD-883C
WS59016DB	D	64 Pin Ceramic Sidebrazed DIP, 0.9"	B1	Comm'l	Standard
WS59016DBMB	D	64 Pin Ceramic Sidebrazed DIP, 0.9"	B1	Military	MIL-STD-883C
WS59016DJ	D	68 Pin PLDCC	J1	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

CMOS 32-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **Eight CMOS 2901 Type Devices in a Single Package**
- **32 x 32 Dual Port RAM**
- **Low CMOS Power**
  — 350 mW
- **High Speed Operation**
  — 23 MHz Read-Modify-Write Cycle
- **Fully Firmware Compatible with the 2901**
- **On Board Carry Look-Ahead**

GENERAL DESCRIPTION

The WS59032 is a 32-bit High-Speed microprocessor which combines the functions of eight 2901 4-bit slice processors and distributed look-ahead carry generation on a single High Performance CMOS device. The WS59032 dual port RAM is 32-bits wide and 32 words deep. This architecture provides greater flexibility and eases the task of generating new microcode while maintaining 100% compatible with existing 2901 based microcode.

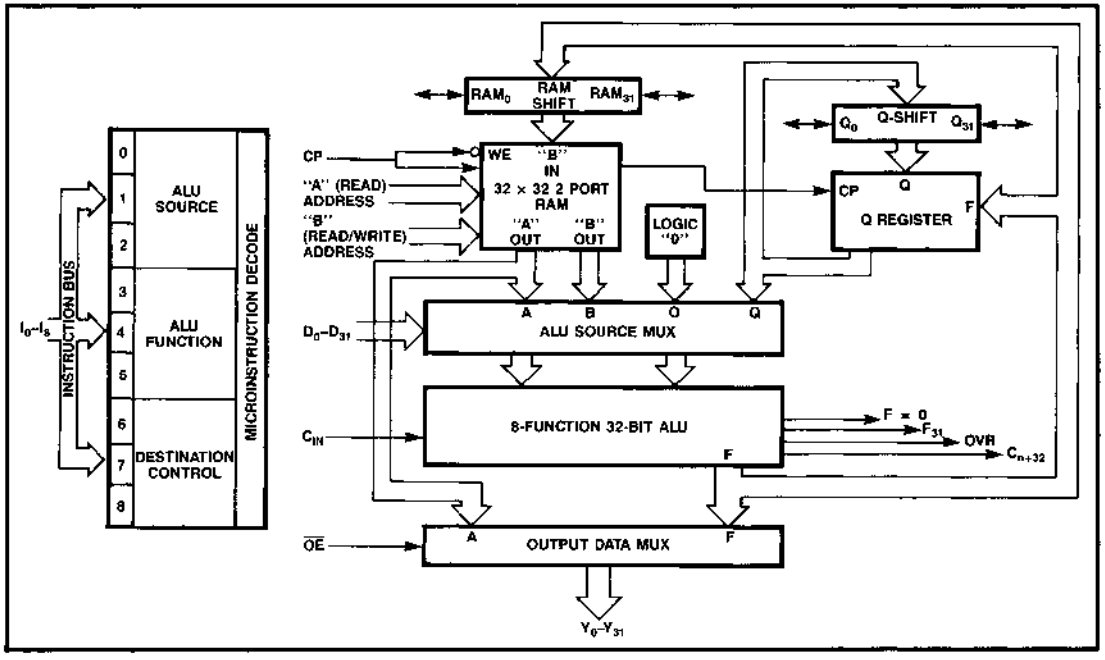
This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the WS59032 is manufactured, provides significant performance improvements over an equivalent Bipolar device configuration. While operating faster than a 2901C based system, the WS59032 requires less than 3% of the power consumed by an equivalent Bipolar system.

The WS59032 is also available as a macro cell in the WaferScale cell library. As such it can be combined with other cells to build Application Specific Integrated Circuits.

6

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Signal Name	I/O	Description
A0 – 4	I	Addresses which select the word of on board RAM which is to be displayed through the A port
B0 – 4	I	Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low
I0 – 8	I	Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678)
Q31, RAM31	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM 31 pin and the MSB of the Q-register is available on the Q 31 pin Otherwise, the pins appear as inputs When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4)
Q0, RAM0	I/O	Shift lines similar to Q31 and RAM31, however the description is applied to the LSB of RAM and the Q-register
D0 – D31	I	These thirty two direct data inputs can be selected as a data source for the ALU. D0 is the LSB
Y0 – Y31	O	These thirty two three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678
$\overline{OE}$	I	When high, the Y outputs are in the high impedance state When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y31, as determined by I678
OVR	O	This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
F=0	O	This output, when high, indicates the result of an ALU operation is zero
F31	O	The most significant ALU output bit
Cn	I	The carry-in to the ALU
Cn + 32	O	The carry-out of the ALU
CP	I	This clock signal is applied to the A and B-port latches, RAM, and Q-register The clock low time is the write enable to the on-board dual port RAM, including set-up time for the A and B-port registers The A and B-port outputs change while the clock is high The Q-register is latched on the clock low-to-high transition

PIN DESIGNATOR

PIN NAME	PGA GRID #	PIN NAME	PGA GRID #	PIN NAME	PGA GRID #	PIN NAME	PGA GRID #
VCC	N1	B3	N2	D23	B1	Y7	K12
VCC	A1	B4	M3	D24	B2	Y8	K13
GND	N7	D0	N6	D25	B3	Y9	J12
GND	G13	D1	M6	D26	A2	Y10	J13
GND	A12	D2	L6	D27	A3	Y11	H11
GND	C6	D3	N5	D28	B4	Y12	H12
RAM0	M7	D4	M5	D29	A4	Y13	H13
RAM31	B6	D5	N4	D30	B5	Y14	G12
Q0	L7	D6	M4	D31	A5	Y15	G11
Q31	A6	D7	N3	I0	N8	Y16	F13
CLK	A7	D8	H3	I1	M8	Y17	F12
CIN	N13	D9	H2	I2	L8	Y18	F11
CN+32	A9	D10	H1	I3	N9	Y19	E13
OVR	C8	D11	G1	I4	M9	Y20	E12
F=0	C13	D12	G3	I5	N10	Y21	D13
F31	B8	D13	G2	I6	A8	Y22	D12
OEN	M12	D14	F1	I7	B7	Y23	B13
A0	J1	D15	F2	I8	C7	Y24	C12
A1	J2	D16	F3	Y0	M10	Y25	A13
A2	K1	D17	E1	Y1	N11	Y26	B12
A3	K2	D18	E2	Y2	N12	Y27	B11
A4	L1	D19	D1	Y3	M11	Y28	A11
B0	M1	D20	D2	Y4	M13	Y29	B10
B1	L2	D21	C1	Y5	L12	Y30	A10
B2	M2	D22	C2	Y6	L13	Y31	B9

ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) ..... 0°C to +70°C
(Mil) ..... −55°C to +125°C
Storage Temp. (No bias) ... −65°C to +150°C
Voltage on any pin with
respect to GND ..... −0.6V to +7V
Latch Up Protection ..... >200 mA
ESD Protection ..... > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{oh}	Output High Voltage	V_{CC} = Min. V_{in} = V_{ih} or V_{il}	All outputs	I_{oh} = −1.6mA	2.4		V
V_{ol}	Output Low Voltage	V_{CC} = Min V_{in} = V_{ih} or V_{il}	Y0-Y31	I_{ol} = 12mA Com'l I_{ol} = 9mA Mil		0.5	V
			All others	I_{ol} = 8mA			
V_{ih}	Input High Voltage	Guaranteed Input High Voltage			2.0		
V_{il}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I_{ix}	Input Load Current	V_{CC} = Max, V_{in} = Gnd or V_{CC}			−10	10	µA
I_{oz}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−50	50	µA
I_{cc}	Power Supply Current	V_{CC} = Max	Comm'l (0°C to +70°C)			70	mA
			Mil (−55°C to +125°C)			85	

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C.
2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

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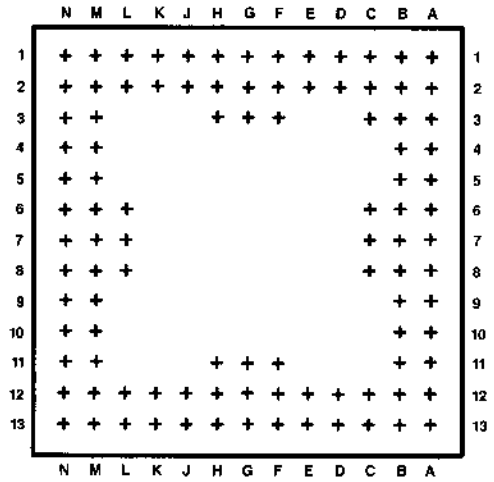
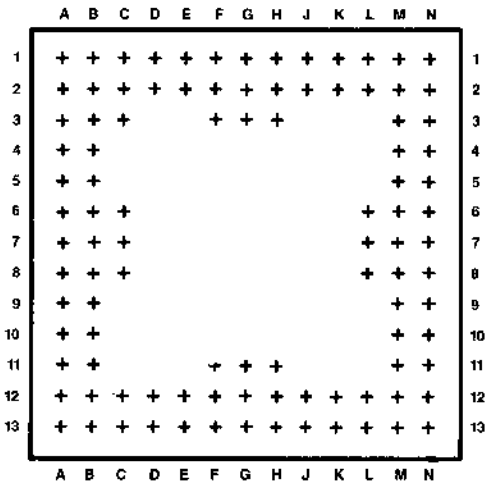
PACKAGE ORIENTATION

101 PIN PGA PACKAGE



TOP VIEW
(THROUGH PACKAGE VIEW)



BOTTOM VIEW

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 1: ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EXOR S	R ▽ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

Table 2. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}

X = Don't care.
B = Register Addressed by B inputs
DOWN is toward LSB UP is toward MSB

Table 3. ALU Destination Control.

		I_{210} (Octal Code)							
		0	1	2	3	4	5	6	7
I_{543} (Octal Code)	ALU Function	ALU Source (R, S)							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	A ▽ Q	A ▽ B	Q	B	A	D ▽ A	D ▽ Q	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus, − = Minus; ∨ = OR, ∧ = AND; ▽ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1, and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4, and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS59032 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (Cn = 0) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A ∧ Q
4 1		A ∧ B
4 5		D ∧ A
4 6		D ∧ Q
3 0	OR	A ∨ Q
3 1		A ∨ B
3 5		D ∨ A
3 6		D ∨ Q
6 0	EX-OR	A ∇ Q
6 1		A ∇ B
6 5		D ∇ A
6 6		D ∇ Q
7 0	EX-NOR	$\overline{A \nabla Q}$
7 1		$\overline{A \nabla B}$
7 5		$\overline{D \nabla A}$
7 6		$\overline{D \nabla Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$ ∧ Q
5 1		$\overline{A}$ ∧ B
5 5		$\overline{D}$ ∧ A
5 6		$\overline{D}$ ∧ Q

Table 5. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6. ALU Arithmetic Mode Functions.

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WS59032D COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032D over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	51ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	26.4 MHz
Minimum Clock Low Time	22ns
Minimum Clock High	26ns
Minimum Clock Period	48ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30ns
From $\overline{OE}$ High to output disable	25ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT / TO OUTPUT	Y	F31	C_{n+32}	F=0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	66	66	58	66	62	75	—	ns
D0-D31	45	45	35	45	35	48	—	
C_n	36	36	18	36	32	42	—	
I_{012}	46	46	35	46	41	58	—	
I_{345}	51	51	41	51	46	53	—	
I_{678}	22	—	—	—	—	22	20	
A BYPASS ALU (I = 2XX)	46	—	—	—	—	—	—	
CLOCK	51	51	42	51	46	59	22	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

CP / INPUT	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	20	1 (Note 3)	53 (Note 4)	0	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		0	
D0-D31	—	—	20	0	
C_n	—	—	22	0	
I_{012}	—	—	28	0	
I_{345}	—	—	30	0	
I_{678}	7	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	7	3	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS59032D MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032D over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	60ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	23.6 MHz
Minimum Clock Low Time	28ns
Minimum Clock High	30ns
Minimum Clock Period	60ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	36ns
From $\overline{OE}$ High to output disable	30ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F=0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	72	72	63	69	69	81	—	ns
D0-D31	51	51	40	52	42	52	—	
C_n	41	41	21	39	36	36	—	
I_{012}	48	48	40	48	44	63	—	
I_{345}	54	54	46	56	51	57	—	
I_{678}	27	—	—	—	—	21	20	
A BYPASS ALU (I = 2XX)	51	—	—	—	—	—	—	
CLOCK	58	58	50	58	53	66	29	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	25	1 (Note 3)	63 (Note 4)	1	ns
B Destination Address	25	DO NOT CHANGE (Note 2)		1	
D0-D31	—	—	30	0	
C_n	—	—	30	0	
I_{012}	—	—	36	0	
I_{345}	—	—	42	0	
I_{678}	13	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	10	5	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS59032E COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032E over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	42ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	33 MHz
Minimum Clock Low Time	18ns
Minimum Clock High	21ns
Minimum Clock Period	40ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	25ns
From $\overline{OE}$ High to output disable	20ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F=0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	55	55	48	55	51	62	—	ns
D0-D31	37	37	29	37	29	40	—	
C_n	30	30	15	30	26	35	—	
I_{012}	38	38	29	38	34	48	—	
I_{345}	42	42	34	42	38	44	—	
I_{678}	18	—	—	—	—	18	16	
A BYPASS ALU (I = 2XX)	38	—	—	—	—	—	—	
CLOCK	42	42	35	42	38	49	18	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	20	0 (Note 3)	44 (Note 4)	0	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		0	
D0-D31	—	—	18	0	
C_n	—	—	20	0	
I_{012}	—	—	26	0	
I_{345}	—	—	29	0	
I_{678}	5	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	5	3	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS59032E MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032E over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	50ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	29 MHz
Minimum Clock Low Time	23ns
Minimum Clock High	25ns
Minimum Clock Period	50ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30 ns
From $\overline{OE}$ High to output disable	30 ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F = 0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	60	60	52	57	57	67	—	ns
D0-D31	42	43	33	43	35	43	—	
C_n	34	34	17	32	30	30	—	
I_{012}	40	40	33	40	36	52	—	
I_{345}	45	45	38	46	42	47	—	
I_{678}	22	—	—	—	—	17	16	
A BYPASS ALU (I = 2XX)	42	—	—	—	—	—	—	
CLOCK	48	48	41	48	44	55	24	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	23	0 (Note 3)	52 (Note 4)	1	ns
B Destination Address	23	DO NOT CHANGE (Note 2)		1	
D0-D31	—	—	25	0	
C_n	—	—	25	0	
I_{012}	—	—	30	0	
I_{345}	—	—	35	0	
I_{678}	10	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	7	5	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here

COMPETITIVE TIMING ANALYSIS

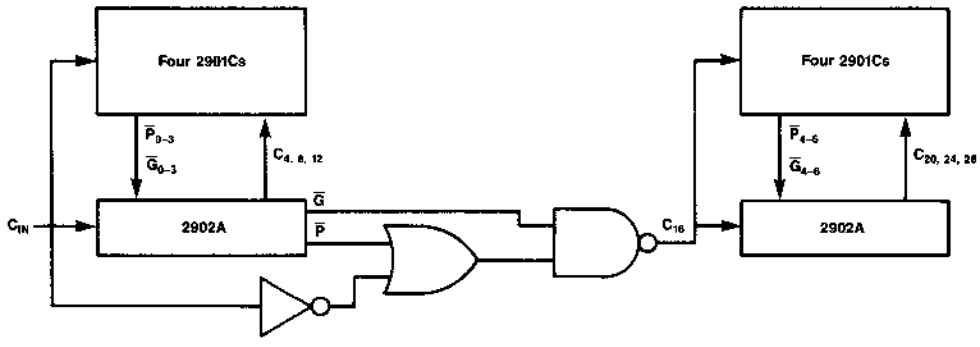
The following analysis compares the critical timing paths of a WS59032E vs. the equivalent Bipolar circuit implementation using eight 2901C's, two 2902A's and three high speed logic gates (See Figure).

As can be seen from the following comparison, the Data Path of the WS59032E is 44% faster than the Data Path of the Bipolar/ECL functional equivalent circuit. Additionally, the Control Path of the WS59032E is 50% faster than the Bipolar/ECL implementation. The actual values for the Bipolar/ECL circuit will be lengthened by the layout dependent interconnect delays between the individual devices. When these delays are taken into account, the WS59032E speed advantage becomes even greater.

TIMING COMPARISON
WS59032D vs Eight 2901C's, Two 2902A's Plus High Speed Logic

DATA PATH		CONTROL PATH	
WS59032E		**WS59032E**	
A,B Address → F = Ø	= 55ns	I 012 → F = Ø	= 48ns
interconnect delay	= Øns	interconnect delay	= Øns
Total Delay	≤ 55ns	Total Delay	≤ 48ns
DISCRETE IMPLEMENTATION (See Figure)		DISCRETE IMPLEMENTATION (See Figure)	
A,B → $\overline{P}_3, \overline{G}_3$	= 37ns	I 012 → F = Ø	= 37ns
$\overline{P}_3, \overline{G}_3$ → $\overline{P}, \overline{G}$	= 11ns	$\overline{P}_3, \overline{G}_3$ → $\overline{P}, \overline{G}$	= 11ns
$\overline{P}, \overline{G}$ → C_{16}	= 10ns	$\overline{P}, \overline{G}$ → C_{16}	= 10ns
C_{16} → C_{28}	= 14ns	C_{16} → C_{28}	= 14ns
C_{28} → F = Ø	= 25ns	C_{28} → F = Ø	= 25ns
interconnect delay	= Xns	interconnect delay	= Xns
Total Delay	> 97ns	Total Delay	> 97ns

Look-Ahead Carry Using Discrete Components



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59032DG	D	101 Pin Ceramic PGA	G2	Comm'l	Standard
WS59032DGMB	D	101 Pin Ceramic PGA	G2	Military	MIL-STD-883C
WS59032EG	E	101 Pin Ceramic PGA	G2	Comm'l	Standard
WS59032EGMB	E	101 Pin Ceramic PGA	G2	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

CMOS MICROPROGRAM CONTROLLER

KEY FEATURES

- **High Speed Operation**
  — 50% Faster Than Bipolar
- **Low Power**
  — 225 mW
- **On-Board Stack**
  — 9 Words Deep
- **DESC SMD No. 5962-87708**
- **Bipolar Replacement**
  — Fully Compatible with AM2910A
- **Immune to Latch-Up**
  — Over 200 mA
- **ESD Protection**
  — Exceeds 2000 Volts

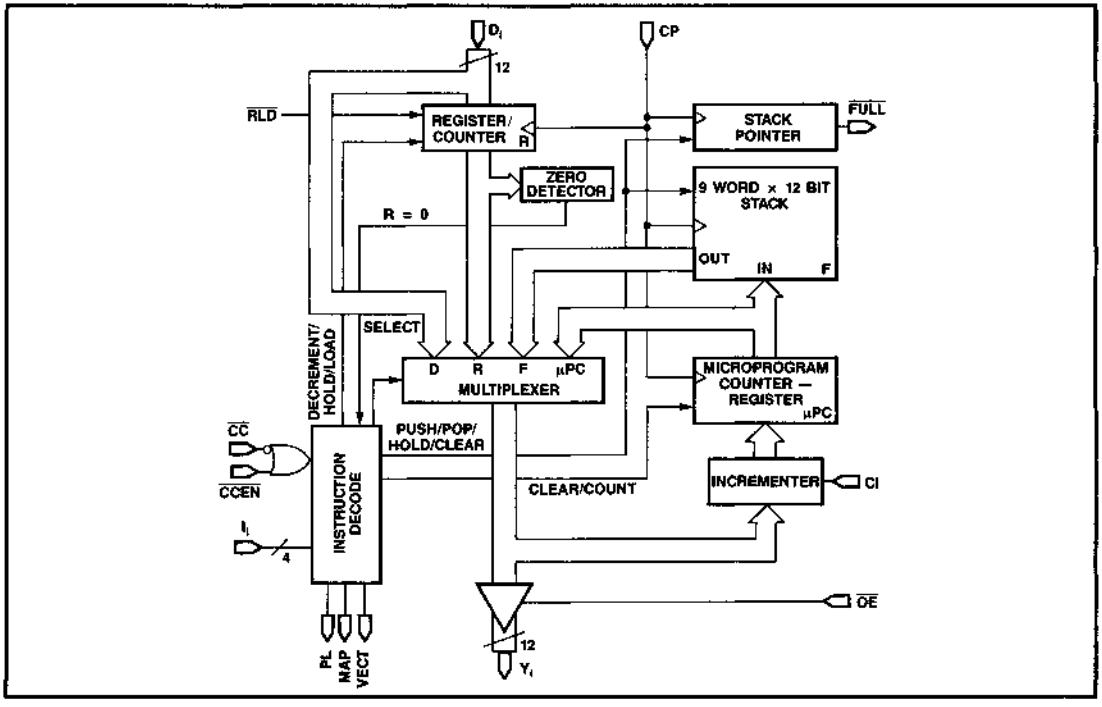
GENERAL DESCRIPTION

The WS5910A/B microprogram controller is an address sequencer which provides addresses to a control store memory. These addresses can come from one of four internal sources: 1) the Microprogram Counter, 2) the 9 word × 12 bit stack, 3) the 12-bit Register/Counter, or 4) the Direct Data Input. The address source selected is dependent upon the instruction applied to the WS5910A/B.

The device can sequentially address memory or it can provide a conditional branch address anywhere within its addressing range. In addition, the WS5910A/B also contains a last-in, first-out stack which provides capabilities for looping as well as providing the microsubroutine return linkage. The on-board register/counter provides loop count control with a count capacity of 4096.

The CMOS WS5910A/B is a form, fit and function replacement for the bipolar/ECL AM2910A. A.C. performance and output drive capability, meet or exceed the specifications of its bipolar counterpart. The WS5910A/B is also available as a macro cell in the WSI cell library.

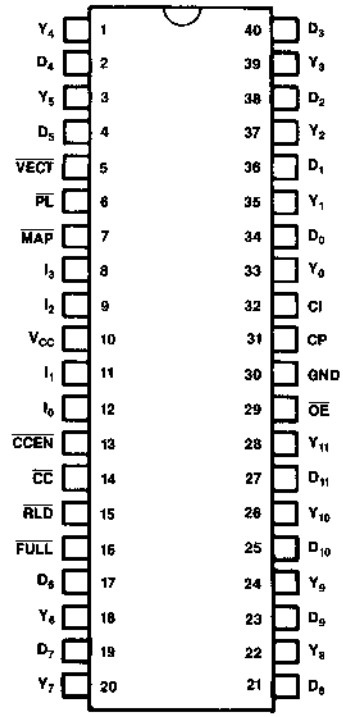
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SIGNAL NAME	I/O	DESCRIPTION
Di	I	Direct Input to Register/Counter and Multiplexer. D_0 is LSB.
Ii	I	Instruction Inputs to the WS5910A/B
$\overline{CC}$	I	Condition Code Input. Pass Test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	I	When HIGH, $\overline{CC}$ Input is Ignored and Internally Forced LOW
CI	I	Carry Input to the LSB of the Microprogram Counter
$\overline{RLD}$	I	When LOW, Register/Counter is Loaded Regardless of Instruction or Condition
$\overline{OE}$	I	Three State Control of Yi Outputs
Yi	O	Address to Microprogram Memory. Y_0 is LSB.
CP	I	All Internal States Change at LOW-to-HIGH Edge
$\overline{FULL}$	O	Stack Full Indicator. (Stack is Nine Levels Deep.)
$\overline{PL}$	O	Active LOW Signal Used to Select the Pipeline Register as the Direct Input Source
$\overline{MAP}$	O	Active LOW Signal Used to Select the Mapping PROM (or PLA) as the Direct Input Source
$\overline{VECT}$	O	Active LOW Signal Used to Select the Interrupt Vector as the Direct Input Source

PIN CONFIGURATION



TOP

INTRODUCTION

The WS5910A/B is a high performance CMOS microprogram controller that produces a sequence of addresses which control the execution of a microprogram. These 12-bit addresses are selected from one of the four sources which feed into a 12-bit 4 to 1 multiplexer. The source selected can be 1) the direct data inputs (D_0-D_{11}), 2) the Register/Counter, 3) the Microprogram Counter, or 4) the stack register. Selection is dependent upon which of the sixteen instructions is being executed as well as other external inputs. The selected source is used to drive the Y_0-Y_{11} three state output buffers.

External Inputs: D_0-D_{11}

The external inputs can be used to supply the jump address for conditional branch types of instructions. They can also be used to load the register counter.

Register Counter

The RC is an edge triggered 12-bit register which is clocked on the LOW-to-HIGH (positive) transition of the clock, CP. The RC is loaded synchronously from the D inputs when the load control input, RLD, is LOW. The output of RC is referred to as R in the table of instructions.

The RC operates as a 12-bit down counter and is decremented and tested for a zero result during instructions 8, 9, and 15. If the RC is loaded with a number N, the sequence will be executed N + 1 times. This allows microinstructions to be repeated up to 4096 times.

THE STACK AND STACK POINTER

The last-in-first-out stack, which is 9 levels deep by 12-bits wide, provides return addresses from micro-subroutine or from loops. Integral to it is the stack pointer which points to the last word written. This allows data on the top of the stack to be referenced without having to perform a POP operation.

There are five microinstructions during which a POP operation may occur (8, 10, 11, 13, 15). A POP decrements the stack pointer at the next rising clock edge following the microinstruction causing the POP. The stack pointer points to zero when the stack is empty. A POP from an empty stock may place unknown data on the Y outputs. The stack pointer remains at zero if a POP is attempted on an empty stack.

There are three operations during which a PUSH operation may occur (1, 3, and 5). A PUSH increments the stack pointer and the return linkage is then written into the stack at the location pointed to by the just incremented stack pointer. RESET (instruction 0) forces the stack pointer to zero, effectively emptying the stack. Each PUSH increments the stack pointer by one, each POP decrements the stack pointer by one. When the stack reaches the level of nine (stack pointer equals nine), the FULL flag goes low. This flag indicates that a POP should occur prior to the next PUSH. If a PUSH does occur on a full stack, the data is overwritten at the top of the stack (location nine) but the stack pointer remains unchanged. The operation will usually destroy useful information and is normally avoided.

TABLE OF INSTRUCTIONS

I_3-I_0	MNEMONIC	NAME	REG/ CNTR CONTENTS	RESULT					
				FAIL $\overline{CCEN}$=L and $\overline{CC}$=H		PASS $\overline{CCEN}$=H or $\overline{CC}$=L		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	Push/Cond LD CNTR	X	PC	Push	PC	Push	Note 1	PL
5	JSRP	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠ 0	F	Hold	F	Hold	Dec	PL
			= 0	PC	Pop	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠ 0	D	Hold	D	Hold	Dec	PL
			= 0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	≠ 0	F	Hold	PC	Pop	Dec	PL
			= 0	D	Pop	PC	Pop	Hold	PL

NOTE: 1) If $\overline{CCEN}$ = L and $\overline{CC}$ = H, hold; else load. H = HIGH L = LOW X = Don't Care

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
Latch Up Protection . . . . . >200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Temperature Range (See Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OH} = −3.4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OL} = 12 mA		0.5	
V_{IH}	Input High Voltage	Guaranteed Input High Voltage			2.0		
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I_{BC}	Input Load Current	V_{CC} = Max, V_{IN} = GND or V_{CC}			−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = GND or V_{CC}			−50	50	
I_{CC}	Power Supply Current	V_{CC} = Max	0°C to +70°C (Comm'l)			45	mA
			−55°C to +125°C (Mil)			70	

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

WS5910A
COMMERCIAL RANGE
AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5910A over the commercial operating range of 0°C to +70°C and a power supply range of 5V ± 5%.

Inputs are switching between 0 and 3V with rise and fall times of 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	20	
Minimum Clock Period	50	
Maximum Clock Frequency	20	MHz

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

INPUT	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	UNITS
D_0-D_{11}	20	—	—	ns
I_0-I_3	35	30	—	
CC	30	—	—	
CCEN	30	—	—	
CP	40	—	31	

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ LOW to Y Output Enable	25	ns
From $\overline{OE}$ HIGH to Y Output Disable	27	

SET UP AND HOLD TIMES

INPUT	t_S	t_H	UNITS
Di – R	16	0	ns
Di – PC	30	0	
I_0-I_3	35	0	
CC	24	0	
CCEN	24	0	
CI	18	0	
RLD	19	0	

WS5910A
MILITARY RANGE
AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5910A over the military operating range of −55°C to +125°C and a power supply range of 5V ± 10%.

Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

Minimum Clock LOW Time	25	ns
Minimum Clock HIGH Time	25	
Minimum Clock Period	51	
Maximum Clock Frequency	19.6	MHz

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

INPUT	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	UNITS
D_0-D_{11}	25	—	—	ns
I_0-I_3	40	35	—	
CC	36	—	—	
CCEN	36	—	—	
CP	46	—	35	

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ LOW to Y Output Enable	25	ns
From $\overline{OE}$ HIGH to Y Output Disable	30	

SET UP AND HOLD TIMES

INPUT	t_S	t_H	UNITS
Di → R	16	0	ns
Di → PC	30	0	
I_0-I_3	38	0	
CC	35	0	
CCEN	35	0	
CI	18	0	
RLD	20	0	

WS5910B
COMMERCIAL RANGE
AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5910B over the commercial operating range of 0°C to +70°C and a power supply range of 5V ± 5%.

Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

Minimum Clock LOW Time	13	ns
Minimum Clock HIGH Time	13	
Minimum Clock Period	33	
Maximum Clock Frequency	30	MHz

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

INPUT	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	UNITS
D_0-D_{11}	18	—	—	ns
I_0-I_3	24	—	—	
CC	21	—	—	
CCEN	21	—	—	
CP	27	—	20	

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ LOW to Y Output Enable	21	ns
From $\overline{OE}$ HIGH to Y Output Disable	22	

SET UP AND HOLD TIMES

INPUT	t_S	t_H	UNITS
Di – R	11	0	ns
Di – PC	20	0	
I_0-I_3	23	0	
CC	16	0	
CCEN	16	0	
CI	12	0	
RLD	12	0	

WS5910B
MILITARY RANGE
AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5910B over the military operating range of −55°C to +125°C and a power supply range of 5V ± 10%.

Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

Minimum Clock LOW Time	17	ns
Minimum Clock HIGH Time	17	
Minimum Clock Period	35	
Maximum Clock Frequency	29	MHz

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

INPUT	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	UNITS
D_0-D_{11}	22	—	—	ns
I_0-I_3	26	23	—	
CC	24	—	—	
CCEN	24	—	—	
CP	30	—	24	

OUTPUT ENABLE/DISABLE TIME

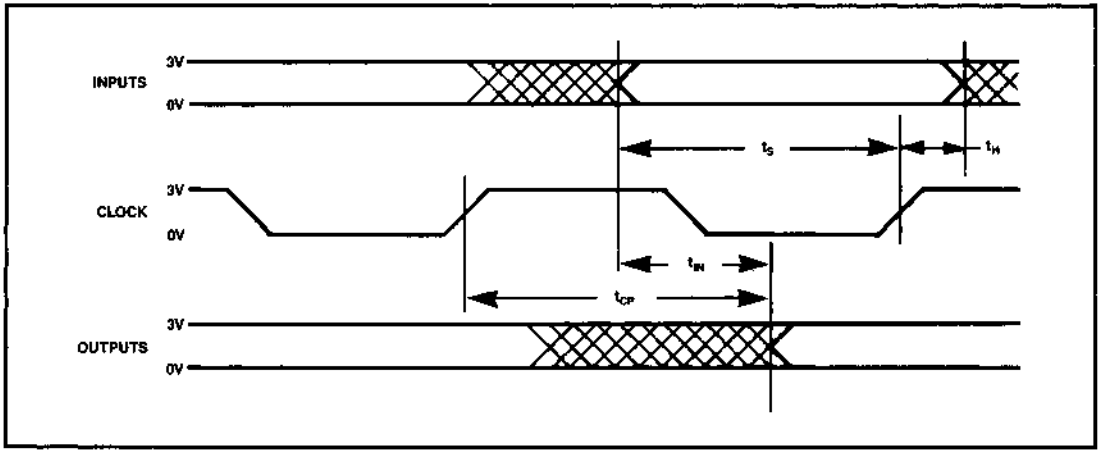
Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ LOW to Y Output Enable	24	ns
From $\overline{OE}$ HIGH to Y Output Disable	25	

SET UP AND HOLD TIMES

INPUT	t_S	t_H	UNITS
Di → R	11	0	ns
Di → PC	20	0	
I_0-I_3	25	0	
CC	23	0	
CCEN	23	0	
CI	12	0	
RLD	13	0	

SWITCHING WAVEFORMS



ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS5910AP	20 MHz	40 Pin Plastic DIP, 0.6"	P1	Comm'l	Standard
WS5910AYMB	20 MHz	40 Pin CERDIP, 0.6"	Y1	Military	MIL-STD-883C
WS5910BP	30 MHz	40 Pin Plastic DIP, 0.6"	P1	Comm'l	Standard
WS5910BYMB	30 MHz	40 Pin CERDIP, 0.6"	Y1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

CMOS 16 x 16 MULTIPLIER ACCUMULATOR

KEY FEATURES

- **16 x 16 Bit Parallel Multiplication with Accumulation to 35-Bit Result**
- **Fast**
  — 30 ns Multiply Accumulate Time
- **Low Power**
  — I_{CC} = 30 mA (10 MHz)
- **DESC SMD No. 5962-88733**
- **Two's Complement or Unsigned Magnitude Operation**
- **Immune to Latch-Up**
  — Over 200 mA
- **Pin Compatible and Functionally Equivalent to Am29510 and TDC1010**

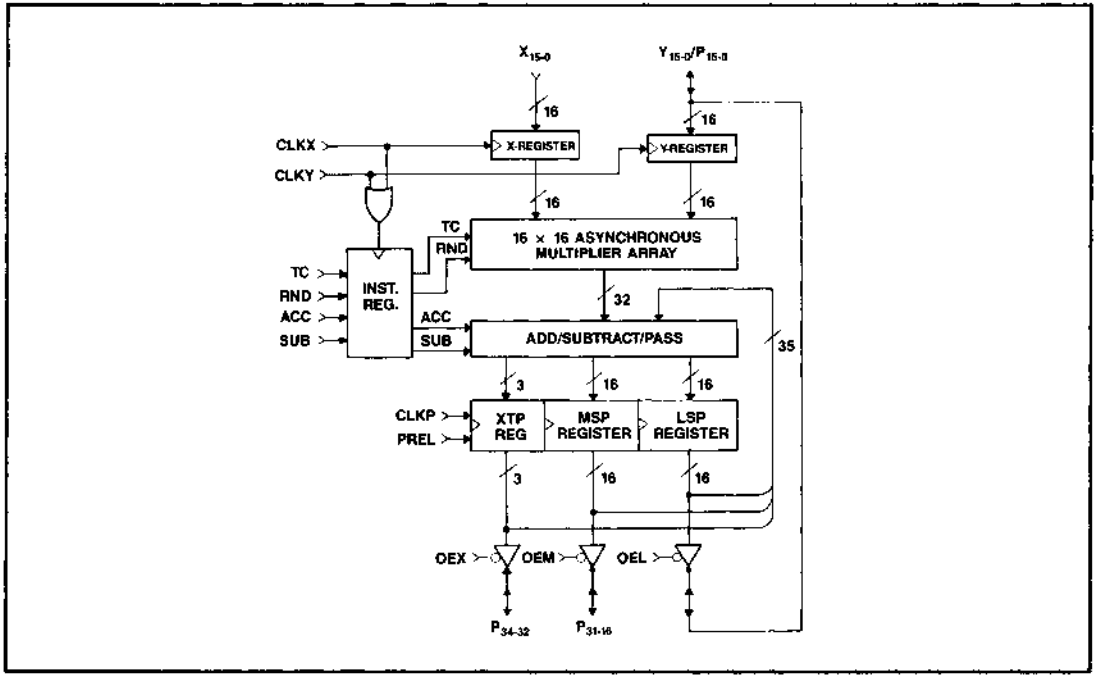
FUNCTIONAL DESCRIPTION

The WS59510 is a high-speed 16 x 16 parallel multiplier accumulator which operates at 30 ns clocked multiply accumulate (MAC) time (33 MHz multiply accumulate rate). The operands may be specified as either two's complement or unsigned magnitude 16-bit numbers. The accumulator functions include loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, or preloading the accumulator from the external world.

All inputs (data and instructions) and outputs are registered. These independently clocked registers are positive edge triggered D-type flip-flops. The 35-bit accumulator/output register is divided into a 3-bit extended product (XTP), a 16-bit most significant product (MSP), and a 16-bit least significant product (LSP). The XTP and MSP have dedicated ports for three-state output; the LSP is multiplexed with the Y-input. The 35-bit accumulator/output register may be preloaded through the bidirectional output ports.

6

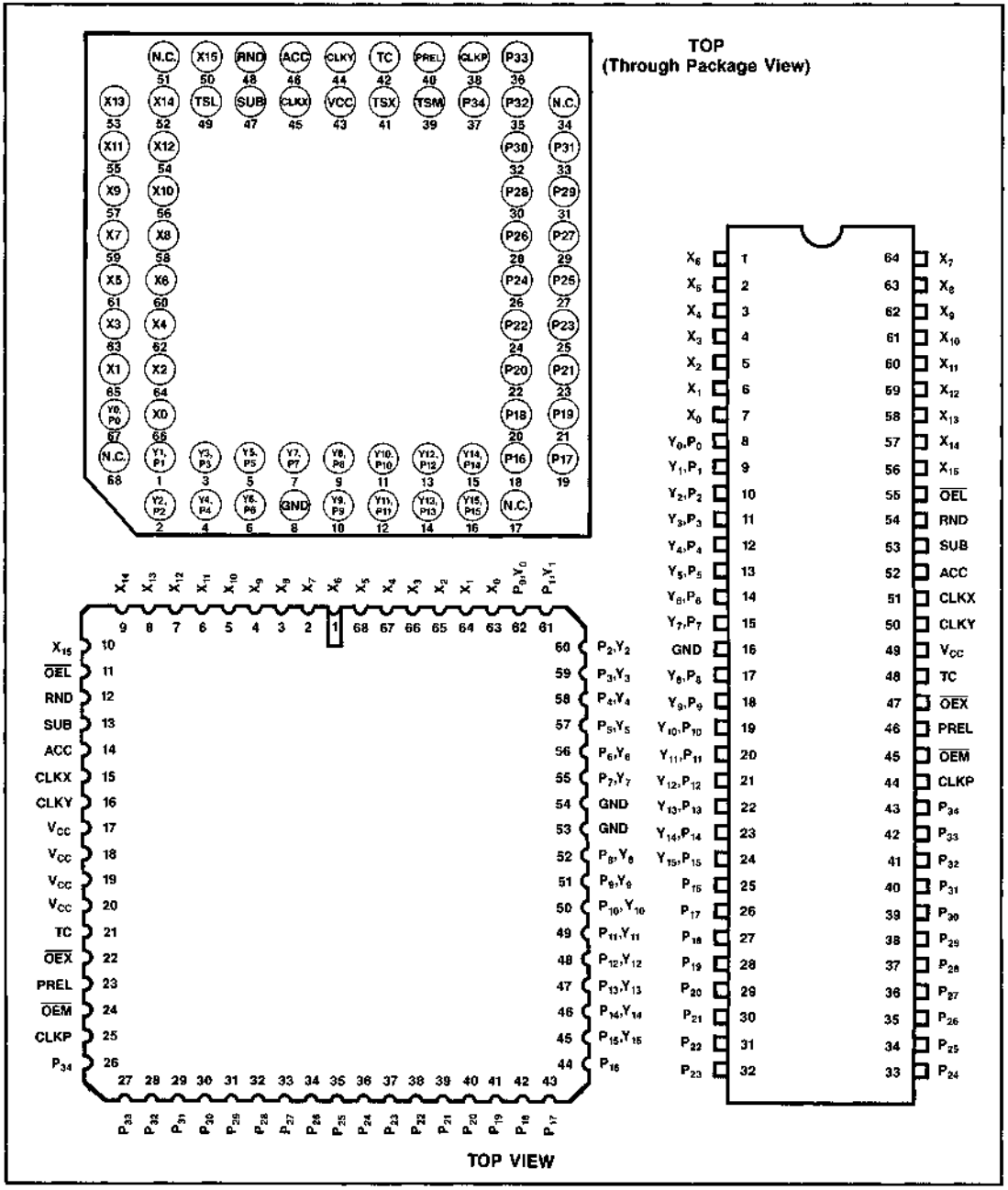
FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTION GUIDE

PARAMETER		59510-30	59510-35	59510-40	59510-50
Maximum Multiply-Accumulate Time (ns)	Commercial	30	35	40	—
	Military	—	—	40	50

PIN CONFIGURATIONS



PIN DESCRIPTION

*Pin No.	Name	I/O	Description
54	RND	I	Round When RND is High, a bit with a weight of P_{15} is added to the multiplier product RND is loaded on the rising edge of CLKx or CLKy
48	TC	I	Two's Complement When High, the X and Y inputs are defined as two's complement data, or as unsigned data when Low. The TC control is loaded on the rising edge of CLKx or CLKy
46	PREL	I	Preload When High, data is preloaded into the specific output register when its respective Load Enable is High When Low, the accumulator register is available at the P-port when the Output Enables are Low
47	LEx/$\overline{OE}$x	I	Load Enable Extended/Output Enable Extended Active High Load Enable for the XTP port during preloading. Active Low three-state control for the XTP port during normal operation (see Preload Function) (TSX)**
45	LEm/$\overline{OE}$m	I	Load Enable Most/Output Enable Most Active High Load Enable for the MSP port during preloading. Active Low three-state control for the MSP port during normal operation (see Preload Function) (TSM)**
55	LEL/$\overline{OE}$L	I	Load Enable Least/Output Enable Least Active High Load Enable for the LSP port during preloading. Active Low three-state control for the LSP port during normal operation (see Preload Function) (TSL)**
51, 50	CLKx, CLKy	I	CLOCKS Load X and Y data respectively and TC, RND, ACC and SUB/$\overline{ADD}$ on the rising edge
44	CLKp	I	CLOCK Loads data into the XTP, MSP and LSP registers on the rising edge
1-7, 56-64	X_{15}-X_0	I	Multiplier Data Input Data is loaded into the X register on the rising edge of CLKx
8-15, 17-24	Y_{15}-Y_0 P_{15}-P_0	I/O	Bidirectional Port Data is loaded into the Y register on the rising edge of CLKy. Product output for least Significant Product (LSP) and input to preload LSP register
41-43	P_{34}-P_{32}	I/O	Bidirectional Port Product output for extended Product (XTP) and input to preload XTP register
25-40	P_{31}-P_{16}	I/O	Bidirectional Port Product output for the Most Significant Product (MSP) and input to preload MSP register
52	ACC	I	Accumulate When High, the multiplier product is accumulated in the accumulator. When Low, the multiplier product is written into the accumulator (see Accumulator Function Table). The ACC control is loaded on the rising edge of CLKx or CLKy
53	SUB/$\overline{ADD}$	I	Subtraction/Addition When High, the accumulator contents are subtracted from the multiplier product and the result written back into the accumulator. When Low, the multiplier product is added into the accumulator (see Accumulator Function Table). The SUB/$\overline{ADD}$ control is loaded on the rising edge of CLKx or CLKy

*DIP Configuration
**TRW TDC1010 Pin Designation

ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) ..... 0°C to +70°C
(Mil) ..... -55°C to +125°C
Storage Temp. (No bias) ..... -65°C to +150°C
Voltage on any pin with
respect to GND ..... -0.6V to +7V
Latch Up Protection ..... > 200 mA
ESD Protection ..... > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OH} = −1.6 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	Y0–Y31 All Others	I_{OL} = 12 mA (Comm'l) I_{OL} = 9 mA (Military) I_{OL} = 8 mA		0.5	V
V_{IH}	Input High Voltage	Guaranteed Input High Voltage			2.0		V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	V
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = Gnd or V_{CC}			−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	0°C to +70°C (Comm'l)			30	mA
			−55°C to +125°C (Military)			50	mA

NOTES:
1. Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to +70°C.
2. Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

DETAILED DESCRIPTION

The WS59510 is a high-speed 16 x 16-bit multiplier accumulator (MAC). It comprises a 16-bit parallel multiplier followed by a 35-bit accumulator. All inputs (data and instructions) and outputs are registered. The WS59510 is divided into four sections: the input section, the 16 x 16 asynchronous multiplier array, the accumulator, and the output/preload section.

The input section has two 16-bit operand input registers for the X and Y operands, clocked by the rising edge of CLKX and CLKY, respectively. The four-bit instruction register (TC, RND, ACC, SUB) is clocked by the rising edge of the logical OR of CLKX, CLKY.

The 16 x 16 asynchronous multiplier array produces the 32-bit product of the input operands. Either two's complement or unsigned magnitude operation is selected, based on control TC. If rounding is selected, (RND = 1), a "1" is added to the MSB of the LSP (position P15). The 32-bit product is zero-filled or sign-extended as appropriate and passed as a 35-bit number to the accumulator section.

The accumulator function is controlled by ACC, SUB, and PREL. Four functions may be selected: the accumulator may be loaded with the current product; the product may be added to the accumulator contents; the accumulator contents may be subtracted from the current product; or the accumulator may be preloaded from the bidirectional ports.

The output/preload section contains the accumulator/output register and the bidirectional ports. This section is controlled by the signals PREL, $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$. When PREL is HIGH, the output buffers are in high impedance state. When the controls $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ are also high, data present at the output pins will be preloaded into the appropriate accumulator register at the rising edge of CLKP. When PREL is LOW, the signals $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ are enable controls for their respective three-state output ports.

WS59510
Input Formats

Fractional Two's Complement Input

XIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-20	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
(Sign)															

YIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-20	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
(Sign)															

Integer Two's Complement Input

XIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
(Sign)															

YIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
(Sign)															

Unsigned Fractional Input

XIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15	2-16

YIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15	2-16

Unsigned Integer Input

XIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

YIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

WS59510
Output Formats

Two's Complement Fractional Output

XTP	MSP																LSP														
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-24	23	22	21	20	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15	2-16	2-17	2-18	2-19	2-20	2-21	2-22	2-23	2-24	2-25	2-26	2-27	2-28	2-29	2-30
(Sign)																																		

Two's Complement Integer Output

XTP			MSP																LSP													
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-234	233	232	231	230	229	228	227	226	225	224	223	222	221	220	219	218	217	216	215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
(Sign)																																		

Unsigned Fractional Output

XTP			MSP																LSP													
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
22	21	20	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15	2-16	2-17	2-18	2-19	2-20	2-21	2-22	2-23	2-24	2-25	2-26	2-27	2-28	2-29	2-30	2-31	2-32

Unsigned Integer Output

XTP			MSP																LSP													
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-234	233	232	231	230	229	228	227	226	225	224	223	222	221	220	219	218	217	216	215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

SWITCHING CHARACTERISTICS Over Operating Range

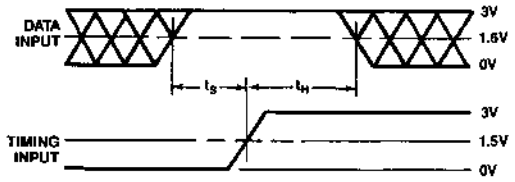
PARAMETER		SYMBOL	-30		-35		-40		-50		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Multiply Accumulate Time		t_{MA}		30		35		40		50	ns
Setup Time (X_{IN},Y_{IN},RND,TC,ACC,SUB)		t_{S1}	5		5		5		5		ns
Setup Time (PREL,$\overline{OEX}$,$\overline{OEM}$,$\overline{OEL}$)		t_{S2}	15		15		15		15		ns
Hold time		t_H	2		2		2		2		ns
Clock Pulse Width		t_{PW}	10		10		10		15		ns
Output Clock to P		t_{PDP}		20		20		25		30	ns
Output Clock to Y		t_{PDY}		20		20		25		30	ns
$\overline{OEX}$, $\overline{OEM}$ to P;	High to Z	t_{PHZ}		20		20		25		30	ns
$\overline{OEL}$ to Y (Disable Time)	Low to Z	t_{PLZ}		20		20		25		30	ns
$\overline{OEX}$, $\overline{OEM}$ to P;	Z to High	t_{PZH}		20		20		25		30	ns
$\overline{OEL}$ to Y (Enable Time)	Z to Low	t_{PZL}		20		20		25		30	ns
Relative Hold Time		t_{HCL}	0		0		0		0		ns

NOTE: Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All inputs have maximum DC load.

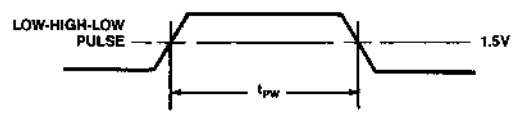
TEST WAVEFORMS

Test	V_X	OUTPUT WAVEFORM - MEASUREMENT LEVEL
All t_{PD}'s	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	2.6V	2.6V, 0.5V, V_{OL}
t_{PZH}	0.0V	V_{OH}, 1.5V, 0.0V
t_{PZL}	2.6V	2.6V, 1.5V, V_{OL}

Setup and Hold Time

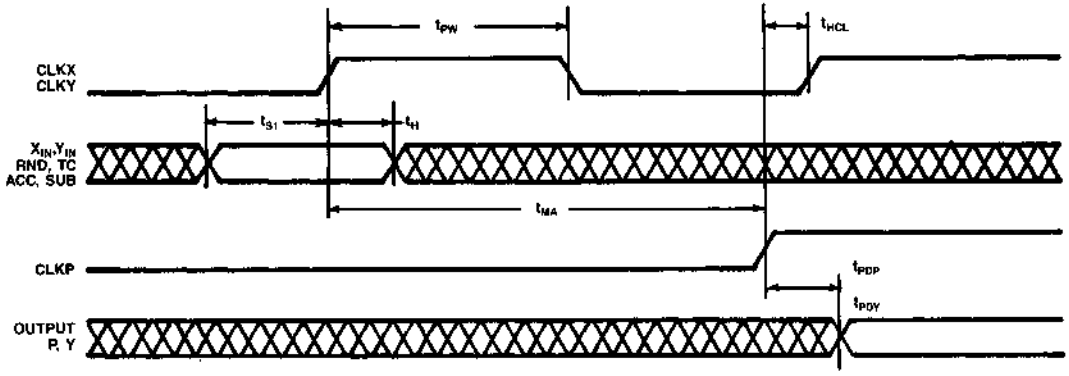


Pulse Width

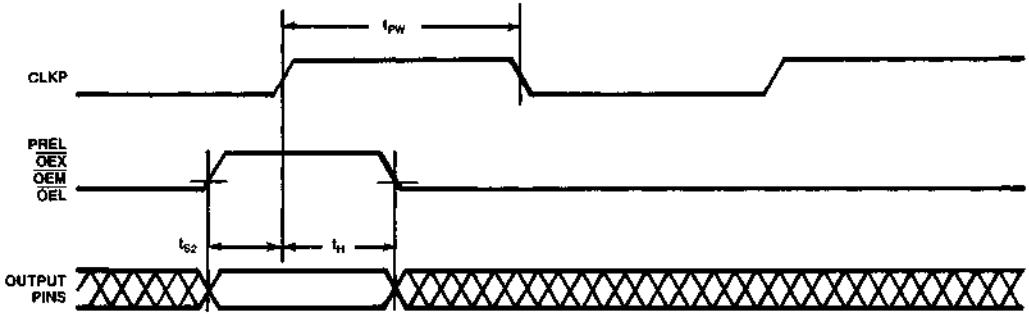


Notes:
1. Diagram shown for HIGH data only. Output transition may be opposite sense
2. Cross hatched area is don't care condition

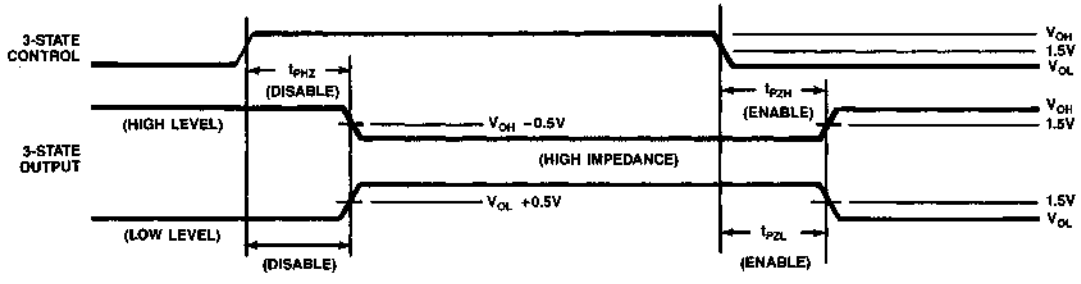
WS59510 TIMING DIAGRAM



PRELOAD TIMING DIAGRAM



THREE-STATE TIMING DIAGRAM



ACCUMULATOR FUNCTION TABLE

PREL	ACC	SUB/$\overline{\text{ADD}}$	P	OPERATION
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

PRELOAD FUNCTION

PREL	LEx/$\overline{\text{OEx}}$	LEM/$\overline{\text{OEM}}$	LEL/$\overline{\text{OEL}}$	Output Register XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = output buffers at High impedance (disabled).
Q = output buffers at Low impedance. Contents of output register available through output ports
PL = output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLKp.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59510-30J	30	68 Pin PLDCC	J1	Comm'l	Standard
WS59510-35G	35	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59510-40G	40	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59510-40GMB	40	68 Pin Ceramic PGA	G1	Military	MIL-STD-883C
WS59510-40J	40	68 Pin PLDCC	J1	Comm'l	Standard
WS59510-40P	40	64 Pin Plastic DIP, 0.9"	P4	Comm'l	Standard
WS59510-50G	50	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59510-50GMB	50	68 Pin Ceramic PGA	G1	Military	MIL-STD-883C
WS59510-50J	50	68 Pin PLDCC	J1	Comm'l	Standard
WS59510-50P	50	64 Pin Plastic DIP, 0.9"	P4	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

MULTILEVEL PIPELINE REGISTER

KEY FEATURES

- Four 8-Bit Registers
- Contents of Each Register Available at Output
- 24-Pin 300 Mil Package
- Dual Two Stage or Single Four Stage Push Only Stack Operation
- Hold, Transfer and Load Instructions
- High Performance CMOS
- TTL Compatible

GENERAL DESCRIPTION

The WS59520 and WS59521 are CMOS drop-in replacements for the bipolar AM29520 and AM29521 devices offered by Advanced Micro Devices. The high performance CMOS process with which these products are manufactured enables them to operate at bipolar speeds while consuming one tenth the power of the bipolar circuits.

The WS59520/521 consists of four 8-bit registers which can be configured as a single four level pipeline or two dual level pipelines. The architectural configuration is determined by the instruction inputs (I_0 and I_1).

Each of the four registers contents is available at the multiplexed output. The register to be used as the output register is determined by the control inputs (S_0 and S_1). The output is 8-bits wide and is enabled by the $\overline{OE}$ input.

The WS59520 and WS59521 differ only in the dual two level stack mode of operation.

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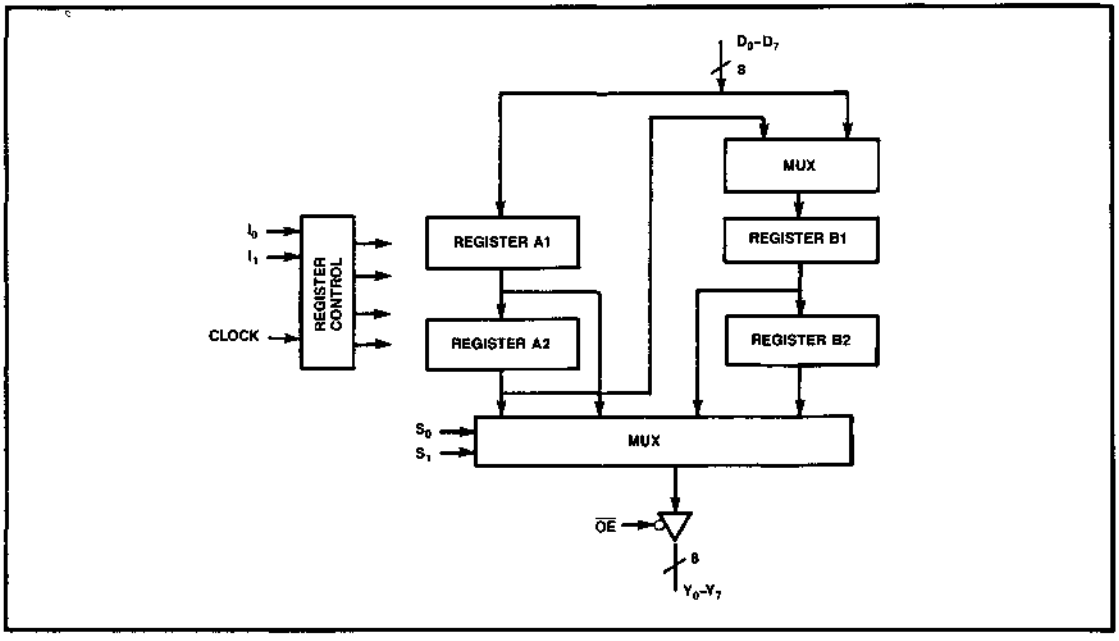
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

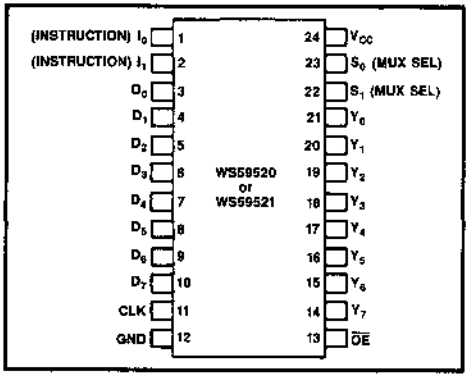
Operating Temp (Comm'l) ..... 0°C to +70°C
(Mil) ..... −55°C to +125°C
Storage Temp. (No bias) .... −65°C to +150°C
Voltage on any pin with
respect to GND ..... −0.6V to +7V
Latch Up Protection .....>200 mA
ESD Protection ..... > ±2000V

* **Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may effect device reliability.

PIN DESCRIPTION

SIGNAL NAME	I/O	DESCRIPTION
D_0–D_7	I	Data input port
Y_0–Y_7	O	Data output port
CLK	I	Data Latches on Low-to-High Transition
I_0–I_1	I	Instruction inputs. Refer to Instruction Control Tables.
S_0, S_1	I	Selects one of four registers to be read at the output port.
$\overline{OE}$	I	Active Low, output enable. A high signal disables the output port.

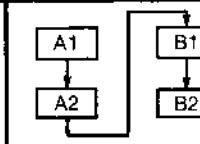
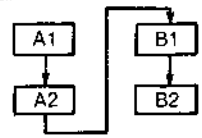
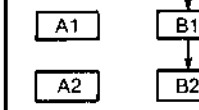
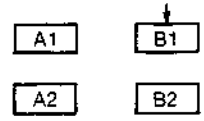
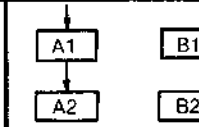
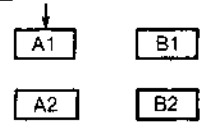
PIN CONFIGURATION



REGISTER SELECT

S1	S0	WS59520 or WS59521
0	0	B2
0	1	B1
1	0	A2
1	1	A1

INSTRUCTION CONTROL

I1	I0	WS59520	WS59521
0	0		
0	1		
1	0		
1	1	ALL REGISTERS HOLD	ALL REGISTERS HOLD

DC CHARACTERISTICS Over Operating Range (See Notes)

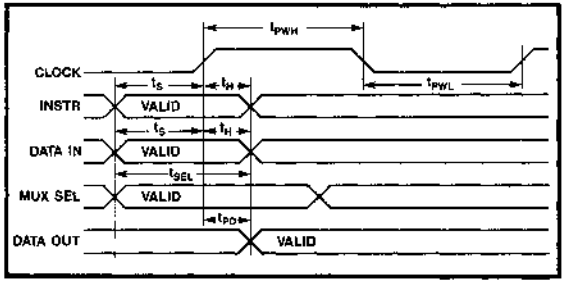
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6.5 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA (Comm'l)		0.5	V
			I_{OL} = 16 mA (Military)			
V_{IH}	Input High Voltage	Guaranteed Input High Voltage		2.0		V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage			0.8	V
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = Gnd or V_{CC}		−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}		−50	50	µA
I_{CC}	Dynamic Power Supply Current	V_{CC} = Max	0° to +70°C (Comm'l)		12	mA
			−55° to +125°C (Military)		15	mA
I_{CC}	Static Power Supply Current	V_{CC} = Max	0° to +70°C (Comm'l)		100	µA
			−55° to +125°C (Military)		200	µA

NOTES: 1. Commercial: V_{CC} = +5V ± 5%, T_A = 0° to +70°C.
2. Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.
3. C_L = 50 pF except for t_{DF} where C_L = 5 pF.

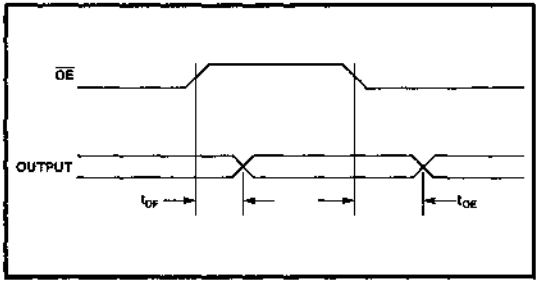
SWITCHING CHARACTERISTICS Over Operating Range (See Notes)

PARAMETER	DESCRIPTION	WS59520/WS59521				UNITS
		COMMERCIAL		MILITARY		
		MIN	MAX	MIN	MAX	
t_{PD}	Clock to Data Out		22		24	ns
t_{SEL}	Mux Select to Data Out		20		22	ns
t_S	Input (Data/Instr.) Set Up	10		10		ns
t_H	Input (Data/Instr.) Hold	3		3		ns
t_{DF}	Output Disable		15		16	ns
t_{OE}	Output Enable		21		22	ns
t_{PWH}	Clock Pulse Width High	10		10		ns
t_{PWL}	Clock Pulse Width Low	10		10		ns

TIMING DIAGRAM



OUTPUT TIMING DIAGRAM



Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59520S	22	24 Pin Plastic DIP, 0.3″	S1	Comm'l	Standard
WS59520K	22	24 Pin CERDIP, 0.3″	K1	Comm'l	Standard
WS59520KMB	24	24 Pin CERDIP, 0.3″	K1	Military	MIL-STD-883C
WS59521S	22	24 Pin Plastic DIP, 0.3″	S1	Comm'l	Standard
WS59521K	22	24 Pin CERDIP, 0.3″	K1	Comm'l	Standard
WS59521KMB	24	24 Pin CERDIP, 0.3″	K1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

CMOS/BI-DIRECTIONAL BUS INTERFACE REGISTERS

KEY FEATURES

- **Two Banks of 8 x 16 Registers**
- **Contents of Each Register Available at Output**
- **Provides Temporary Address or Data Storage Between Two Processor Ports or Buses**
- **Bi-Directional Buses Interface — Dual 4-Deep or 8-Deep Registers in Each Direction**
- **Separate Control for Each Register Bank**
- **Direct Processor Bus-to-Bus Interface**
- **TTL Compatible**
- **Replaces Eight WS59520's**

GENERAL DESCRIPTION

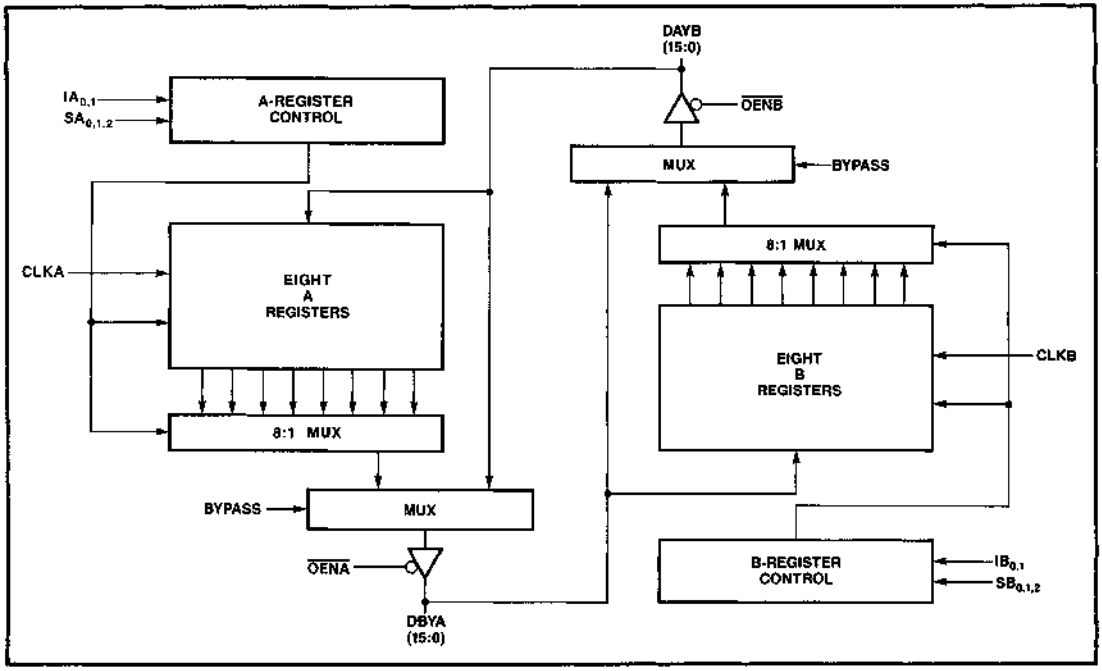
The WS59820/WS59820B consists of two banks of registers, eight registers in each bank, each register 16 bits wide. A single bank can be configured as an eight level pipeline or two each four level pipelines. The architectural configuration is determined by the instruction inputs (I0 and I1) for each register bank.

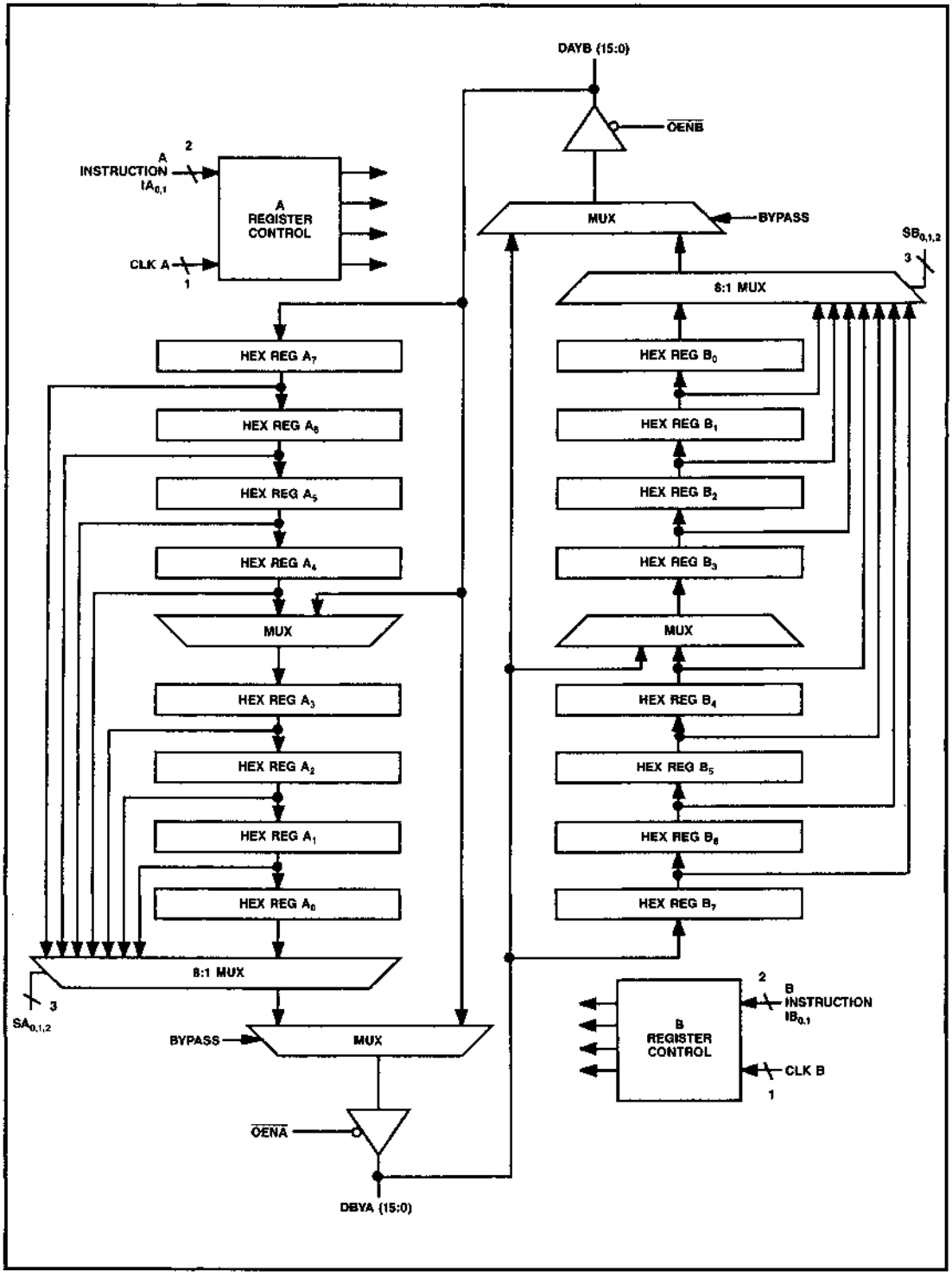
Each of the eight registers in each bank is available at the multiplex output. The output register is determined by the control inputs (S0, S1, and S2) for each register bank. The multiplexed output is 16 bits wide and is enabled by the $\overline{OEN}$ signal. Each bank of registers has its own clock (CLK), instruction inputs (I0-1) and multiplex controls.

The WS59820 and WS59820B differ only in pin assignments. The WS59820B has additional V_{CC} and ground pin assignments and is recommended for new designs.

6

BLOCK DIAGRAM



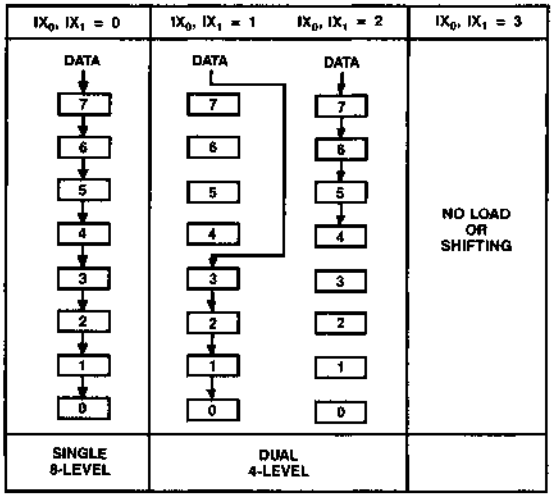

DAYB (15:0)
OENB
2
A
INSTRUCTION
IA0,1
A
REGISTER
CONTROL
CLK A
1
MUX
BYPASS
SB0,1,2
3
8:1 MUX
HEX REG A7
HEX REG A6
HEX REG A5
HEX REG A4
MUX
HEX REG A3
HEX REG A2
HEX REG A1
HEX REG A0
8:1 MUX
3
SA0,1,2
BYPASS
MUX
OENA
DBYA (15:0)
HEX REG B0
HEX REG B1
HEX REG B2
HEX REG B3
MUX
HEX REG B4
HEX REG B5
HEX REG B6
HEX REG B7
2
B
INSTRUCTION
IB0,1
B
REGISTER
CONTROL
CLK B
1

SELECTION TABLE FOR REGISTER A OR B

SX2	SX1	SX0	REGISTER SELECTED
0	0	0	REG 0
0	0	1	REG 1
0	1	0	REG 2
0	1	1	REG 3
1	0	0	REG 4
1	0	1	REG 5
1	1	0	REG 6
1	1	1	REG 7

X = Register A or B.

REGISTER SHIFT OPTIONS FOR REGISTERS A OR B



X = Register A or B.

MULTIPLEX CONTROL

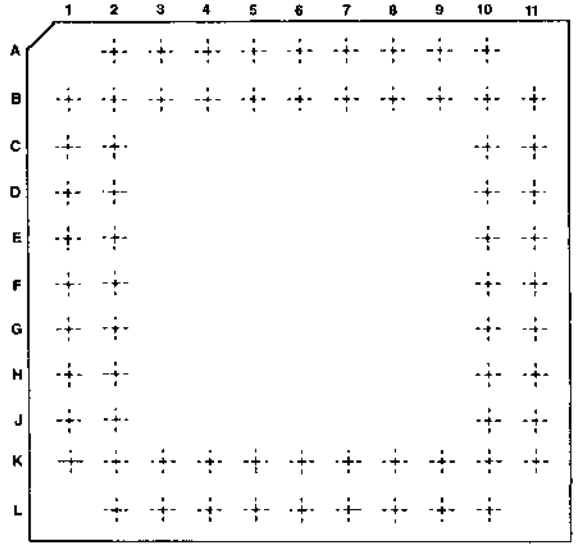
$\overline{OENA}$	$\overline{OENB}$	BYPASS	OPERATION
0	0	1	Pass Output of 8:1 Muxes to Outputs
0	0	0	Not Allowed (Input is Preferred)
0	1	0	Pass Input From DAYB (15:0) to Output DBYA (15:0)
0	1	1	Pass Output From 8:1 Mux to Outputs DBYA (15:0)
1	0	0	Pass Input From DBYA (15:0) to Output DAYB (15:0)
1	0	1	Pass Output From 8:1 Mux to Outputs DAYB (15:0)
1	1	X	Inhibit Outputs (High Impedance)

PIN DESCRIPTION

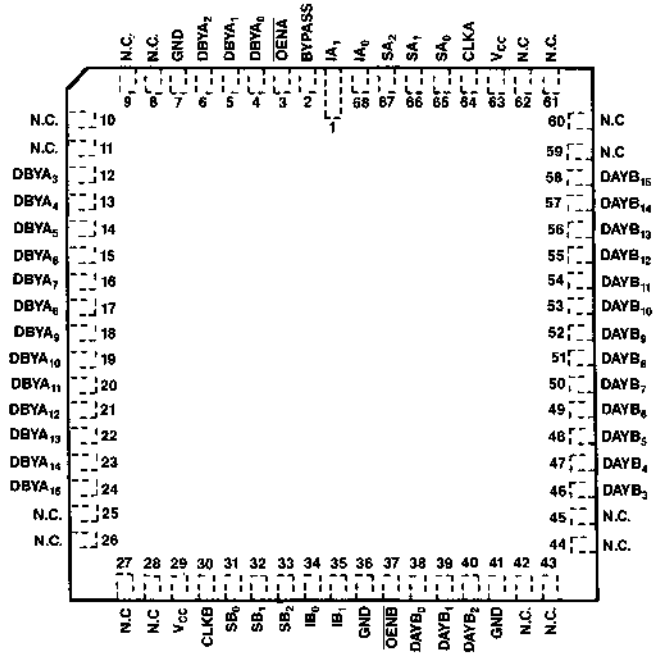
SIGNAL NAME	I/O	DESCRIPTION
IA_0, IA_1	I	Instruction Inputs for Register Bank A
IB_0, IB_1	I	Instruction Inputs for Register Bank B
SA_0-SA_2	I	Multiplex Select for Register Bank A
SB_0-SB_2	I	Multiplex Select for Register Bank B
$\overline{OENA}$	I	Output Enable for Output Port DBYA
$\overline{OENB}$	I	Output Enable for Output Port DAYB
CLKA	I	Clock Input for Register Bank A
CLKB	I	Clock Input for Register Bank B
DBYA 15:0	I/O	Register Bank B Input Port, Register Bank A Output Port
DAYB 15:0	I/O	Register Bank A Input Port, Register Bank B Output Port
BYPASS	I	BYPASS Control (Active Low). See Table on Output Control

PACKAGE ORIENTATION (WS59820)

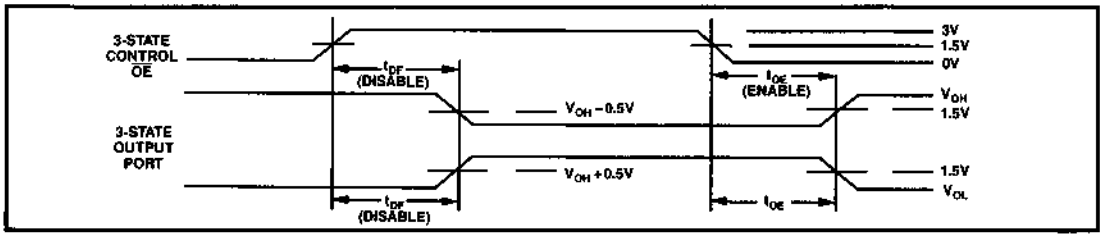
68 PIN CPGA
(Top Through Package View)



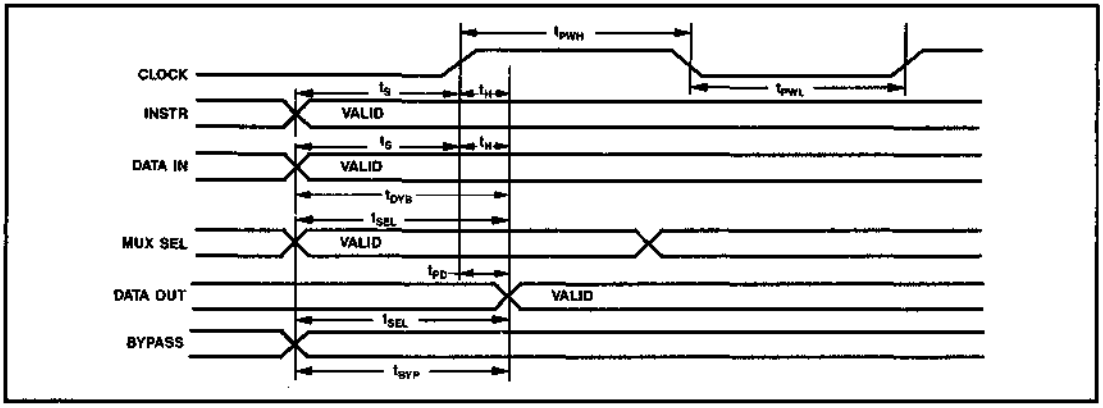
68 PIN PLDCC
(Top Through Package View)



WS59820/WS59820B THREE STATE TIMING



WS59820/WS59820B TIMING DIAGRAM



68 PIN CPGA PIN DESIGNATOR (WS59820)

PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME
A_6	IA_1	B_6	BYPASS	A_5	$\overline{OENA}$	B_5	$DBYA_0$
A_4	$DBYA_1$	B_4	$DBYA_2$	A_3	GND	B_3	Not Used
A_2	Not Used	B_1	Not Used	B_2	Not Used	C_1	$DBYA_3$
C_2	$DBYA_4$	D_1	$DBYA_5$	D_2	$DBYA_6$	E_1	$DBYA_7$
E_2	$DBYA_8$	F_1	$DBYA_9$	F_2	$DBYA_{10}$	G_1	$DBYA_{11}$
G_2	$DBYA_{12}$	H_1	$DBYA_{13}$	H_2	$DBYA_{14}$	J_1	$DBYA_{15}$
J_2	Not Used	K_1	Not Used	L_2	Not Used	K_2	Not Used
L_3	V_{CC}	K_3	CLKB	L_4	SB_0	K_4	SB_1
L_5	SB_2	K_5	IB_0	L_6	IB_1	K_6	GND
L_7	$\overline{OENB}$	K_7	$DAYB_0$	L_8	$DAYB_1$	K_8	$DAYB_2$
L_9	GND	K_9	Not Used	L_{10}	Not Used	K_{11}	Not Used
K_{10}	Not Used	J_{11}	$DAYB_3$	J_{10}	$DAYB_4$	H_{11}	$DAYB_5$
H_{10}	$DAYB_6$	G_{11}	$DAYB_7$	G_{10}	$DAYB_8$	F_{11}	$DAYB_9$
F_{10}	$DAYB_{10}$	E_{11}	$DAYB_{11}$	E_{10}	$DAYB_{12}$	D_{11}	$DAYB_{13}$
D_{10}	$DAYB_{14}$	C_{11}	$DAYB_{15}$	C_{10}	Not Used	B_{11}	Not Used
A_{10}	Not Used	B_{10}	Not Used	A_9	V_{CC}	B_9	CLKA
A_8	SA_0	B_8	SA_1	A_7	SA_2	B_7	IA_0

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
Latch Up Protection . . . . . > 200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Range (See Notes)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6.5 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA Comm'l I_{OL} = 16 mA Mil		0.5	V
V_{IH}	Input High Voltage	Guaranteed Input High Voltage		2.0		V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage			0.8	V
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = GND or V_{CC}		−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = GND or V_{CC}		−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	0°C to +70°C (Comm'l)		12	mA
			−55°C to +125°C (Mil)		15	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C.
2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.
3) C_L = 50 pF except for t_{DF} where C_L = 5 pF.

SWITCHING CHARACTERISTICS Over Operating Range (See Notes)

PARAMETER	DESCRIPTION	WS59820/WS59820B				UNITS
		COMMERCIAL		MILITARY		
		MIN	MAX	MIN	MAX	
t_{PD}	Clock to Data Out		20		22	ns
t_{SEL}	Mux Select to Data Out		20		22	
t_S	Input (Data/Instr.) Set Up	6		6		
t_H	Input (Data/Instr.) Hold	5		5		
t_{DF}	Output Disable	7	15		16	
t_{OE}	Output Enable	7	18		22	
t_{PWH}	Clock Pulse Width High	10		12		
t_{PWL}	Clock Pulse Width Low	11		12		
t_{BYP}	Bypass to Data Out		17		20	
t_{DYB}	Data Via BYPASS (Data In to Data Out When BYPASS is Active Low)		13		16	

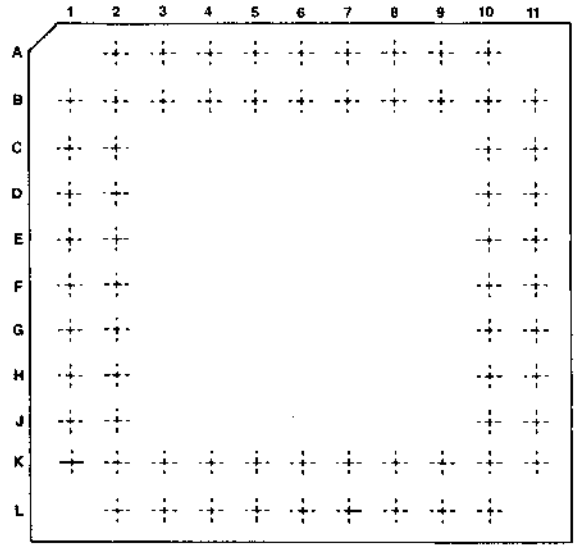
NOTE: Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

68 PIN CPGA PIN DESIGNATOR (WS59820B)

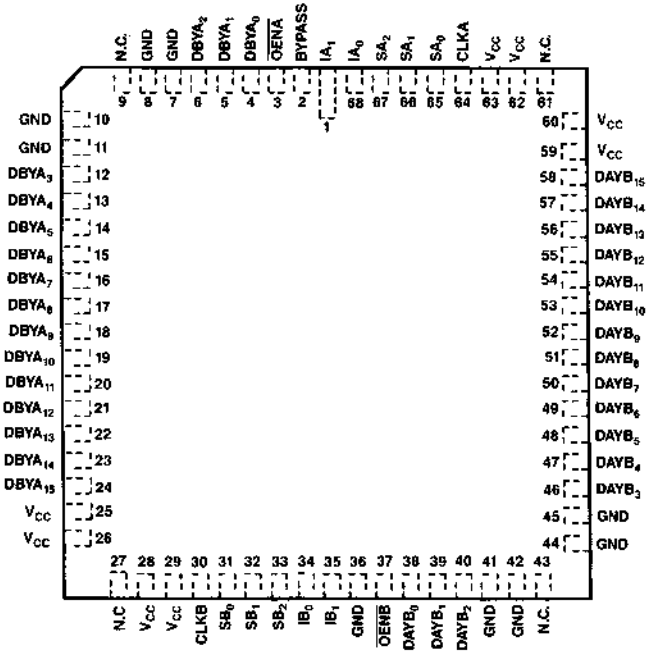
PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME
A_6	IA_1	B_6	BYPASS	A_5	$\overline{OENA}$	B_5	$DBYA_0$
A_4	$DBYA_1$	B_4	$DBYA_2$	A_3	GND	B_3	GND
A_2	Not Used	B_1	GND	B_2	GND	C_1	$DBYA_3$
C_2	$DBYA_4$	D_1	$DBYA_5$	D_2	$DBYA_6$	E_1	$DBYA_7$
E_2	$DBYA_8$	F_1	$DBYA_9$	F_2	$DBYA_{10}$	G_1	$DBYA_{11}$
G_2	$DBYA_{12}$	H_1	$DBYA_{13}$	H_2	$DBYA_{14}$	J_1	$DBYA_{15}$
J_2	V_{CC}	K_1	V_{CC}	L_2	Not Used	K_2	V_{CC}
L_3	V_{CC}	K_3	CLKB	L_4	SB_0	K_4	SB_1
L_5	SB_2	K_5	IB_0	L_6	IB_1	K_6	GND
L_7	$\overline{OENB}$	K_7	$DAYB_0$	L_8	$DAYB_1$	K_8	$DAYB_2$
L_9	GND	K_9	GND	L_{10}	Not Used	K_{11}	GND
K_{10}	GND	J_{11}	$DAYB_3$	J_{10}	$DAYB_4$	H_{11}	$DAYB_5$
H_{10}	$DAYB_6$	G_{11}	$DAYB_7$	G_{10}	$DAYB_8$	F_{11}	$DAYB_9$
F_{10}	$DAYB_{10}$	E_{11}	$DAYB_{11}$	E_{10}	$DAYB_{12}$	D_{11}	$DAYB_{13}$
D_{10}	$DAYB_{14}$	C_{11}	$DAYB_{15}$	C_{10}	V_{CC}	B_{11}	V_{CC}
A_{10}	Not Used	B_{10}	V_{CC}	A_9	V_{CC}	B_9	CLKA
A_8	SA_0	B_8	SA_1	A_7	SA_2	B_7	IA_0

PACKAGE ORIENTATION (WS59820B)

68 PIN CPGA
(Top Through Package View)



68 PIN PLDCC
(Top Through Package View)



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59820J	23	68 Pin PLDCC	J1	Comm'l	Standard
WS59820G	23	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59820GMB	25	68 Pin Ceramic PGA	G1	Military	MIL-STD-883C
WS59820BJ	23	68 Pin PLDCC	J1	Comm'l	Standard
WS59820BG	23	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59820GMB	25	68 Pin Ceramic PGA	G1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 800-562-6363.

Waferscale Integration, Inc. (WSI) is committed to supplying products that meet the demands of the Military/Hi-Reliability marketplace. WSI's very high performance CMOS EPROM (with its patented Split-Gate design) and Logic technology offers an intrinsic reliability that, when coupled with Military screening and testing, produces an extremely enhanced and reliable product. All WSI products can be procured fully compliant to Paragraph 1.2.1 of MIL-STD-883C.

The WSI Quality Assurance Program has been designed and implemented to maintain the high standards needed to repeatedly produce these products. The cohesiveness of the Program is accomplished through a comprehensive Document Control system that assures the repeatability of the process.

State-of-the-art equipment and techniques are being used extensively throughout Design, Wafer Fabrication, Assembly, Screening and Testing (Method 5004), and Quality Conformance Inspections (Method 5005) to produce the highest yields possible with their associated reliability enhancement.

The tables below describe the program in detail. Worthy of notation is the fact that WSI UV EPROMs are subjected to a 100% data retention test in wafer form (72 hours at 225°C). This wafer data retention test, with its high activation temperature, assures that data retention problems are reduced and virtually eliminated.

TABLE I. 100% SCREENING TO METHOD 5004

All product is subjected to the following 100% screening flow. Screening test methods are in accordance with MIL-STD-883, Method 5004. (Latest issues in effect.)

SCREEN	TEST METHOD/CONDITION	QUALITY LEVEL
Data Retention (EPROMs Only)	72 Hours at 225°C	100%
Visual and Mechanical	**5004**	
Internal Visual	2010/Condition B	100%
Temperature Cycle	1010/Condition C	100%
Constant Acceleration	2001/Condition D or E (Y_1 Axis)	100%
Hermeticity	1014	
Fine	Condition A or B	100%
Gross	Condition C	100%
External Visual	2009	100%
Burn-In	**5004**	
Pre-Burn-In Electrical	Per Applicable WSI Device Specifications or Military Drawing. T_A = +25°C.	100%
Burn-In	1015/Condition D, T_A = +125°C Minimum	100%
Final Electrical Tests (See Note 1)	**5004**	
Static (DC)	a) T_A = +25°C, +125°C, and −55°C	100%
Functional	b) Power Supply Extremes	100%
Switching (AC)		
Percent Defective Allowable (PDA)	**5004** Paragraph 3.5.1	5%
Quality Conformance Inspection	**5005**	
Sample Selection	See Tables II Through V	Sample
External Visual	2009	**100%**

NOTE: 1. Per applicable WSI device specification or Military Drawing.

TABLE II. GROUP A QUALITY CONFORMANCE INSPECTION

Group A Inspection is performed on each inspection lot per MIL-STD-883, Method 5005, Table I.

TEST (See Note 1)	LTPD	MAXIMUM	
		SAMPLE SIZE	ACCEPT NUMBER
Subgroup 1 Static Tests at T_A = +25°C	2	116	0
Subgroup 2 Static Tests at Maximum Rated Operating Temperature	2	116	0
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	2	116	0
Subgroup 4 (See Note 2) Dynamic Tests at T_A = +25°C	2	116	0
Subgroup 5 (See Note 2) Dynamic Tests at Maximum Rated Operating Temperature	2	116	0
Subgroup 6 (See Note 2) Dynamic Tests at Minimum Rated Operating Temperature	2	116	0
Subgroup 7 Functional Tests at T_A = +25°C	2	116	0
Subgroup 8 Functional Tests at Maximum and Minimum Rated Operating Temperatures	2	116	0
Subgroup 9 Switching Tests at T_A = +25°C	2	116	0
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature	2	116	0
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature	2	116	0

NOTES: 1. Per applicable WSI device specification or Military Drawing.
2. Subgroups 4, 5, and 6 are not applicable to WSI products.

TABLE III. GROUP B QUALITY CONFORMANCE INSPECTION

Group B quality conformance tests are performed on each inspection lot in accordance with MIL-STD-883, Method 5005, Table IIb.

TEST	TEST METHOD	TEST CONDITIONS	QUALITY LEVEL/ MAXIMUM ACCEPT NUMBER
Subgroup 2 Resistance to Solvents	2015	4 Chemical Solutions	4 Devices (No Failures)
Subgroup 3 Solderability	2403	Soldering Temperature of +245°C ± 5°C	LTPD 10/Accept = 2 38 Leads From 3 Devices Minimum
Subgroup 5 Bond Strength Ultrasonic or Wedge	2011	Condition C or D	LTPD 15/Accept = 1 34 Bonds From 4 Devices Minimum
Subgroup 8 Electrostatic Discharge Sensitivity Classification	3015	Unless Otherwise Specified, This Test Will be Performed for Initial Qualification of New Product or Redesign.	LTPD 15/Accept = 0

TABLE IV. GROUP C QUALITY CONFORMANCE INSPECTION

Group C quality conformance tests are performed on inspection lots every 52 weeks in accordance with MIL-STD-883, Method 5005, Table III.

TEST	TEST METHOD	TEST CONDITIONS	QUALITY LEVEL/ MAXIMUM ACCEPT NUMBER
Subgroup 1 Steady-State Life Test End-Point Electrical	1005	Condition D, 1000 Hours at T_A = 125°C or Equivalent Per WSI Specification or Military Drawing	LTPD 5/Accept = 2

7

TABLE V. GROUP D QUALITY CONFORMANCE INSPECTION

Group D quality conformance tests are performed on inspection lots every 52 weeks in accordance with MIL-STD-883, Method 5005, Table IV.

TEST	TEST METHOD	TEST CONDITIONS	QUALITY LEVEL/ MAXIMUM ACCEPT NUMBER
Subgroup 1			
Physical Dimensions	2016	Per WSI Outline Drawing and Appendix C of MIL-M-38510	LTPD 15/Accept = 2
Subgroup 2			
Lead Integrity	2004 or 2028	Test Condition B2 (Lead Fatigue) or D	LTPD 15/Accept = 2
Hermeticity, Fine and Gross	1014	Condition A or B and C	
Subgroup 3			
Thermal Shock	1011	Condition B Minimum	
Temperature Cycling	1010	Condition C Minimum	
Moisture Resistance	1004		LTPD 15/Accept = 2
Hermeticity, Fine and Gross	1014	Condition A or B and C	
Visual Examination	1004, 1010		
End-Point Electrical Parameters		Per WSI Specification or Military Drawing	
Subgroup 4			
Mechanical Shock	2002	Condition B Minimum	
Vibration, Variable Frequency	2007	Condition A Minimum	
Constant Acceleration	2001	Condition D or E	LTPD 15/Accept = 2
Hermeticity, Fine and Gross	1014	Condition A or B and C	
Visual Examination	2009		
End-Point Electrical Parameters		Per WSI Specification or Military Drawing	
Subgroup 5			
Salt Atmosphere	1009	Condition A Minimum	
Hermeticity, Fine and Gross	1014	Condition A or B and C	LTPD 15/Accept = 2
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor	1018	5,000 ppm Maximum Water Content at 100°C	3 Devices, 0 Failures or 5 Devices, 1 Failure
Subgroup 7			
Adhesion of Lead Finish	2025		LTPD 15/Accept = 2
Subgroup 8			
Lid Torque	2024	As Applicable to Glass-Frit Packages	LTPD 15/Accept = 0

WSI'S SMD PRODUCTS

WSI supports the Standardized Military Drawings (SMD) program sponsored by the Defense Electronics Supply Center (DESC), Dayton, Ohio 45444-5277, and has submitted Certificates of Compliance for the following products:

SMD NO.	WSI PART NO.	ESTIMATED DESC PUBLICATION DATE
85102	WS27C64F/WS27C64L/WS57C64F	Available Now
5962-86063	WS27C256F/WS27C256L/WS57C256F	Available Now
5962-87515	WS57C49B	Available Now
5962-87529	WS57C45	Available Now
5962-87614	WS27C010L	Available Now
5962-87648	WS27C512L	Available Now
5962-87650	WS57C191B/WS57C291B	Available Now
5962-87661	WS27C128F/WS27C128L/WS57C128F	Available Now
5962-87708	WS5910	Available Now
5962-88733	WS59510	Available Now
5962-88734	WS57C191B/WS57C291B OTP	Available Now
5962-87735	WS57C45 OTP	Available Now
5962-88736	WS59520	Q4, 1989
5962-88535	WS5901	Available Now
5962-89538	WS57C51B	Q4, 1989
5962-86805	WS27C210L	Q4, 1989

Copies of the SMD may be obtained by calling DESC at Tel. 513-296-6095. Any of the above products can also be obtained compliant to MIL-STD-883C.

WSI'S MIL-STD-883C COMPLIANT PRODUCTS

When Standardized Military Drawings are not yet available for new products offered by WSI, military versions of these products may be obtained compliant to MIL-STD-883C:

		FASTEST MILITARY SPEED
WS27C010L	128K x 8 CMOS EPROM	150 ns
WS27C040L	512K x 8 CMOS EPROM	150 ns
WS27C210L	64K x 16 CMOS EPROM	120 ns
WS27C512F	64K x 8 CMOS EPROM	90 ns
WS57C43B	4K x 8 CMOS PROM/RPROM	30 ns
WS57C51B	16K x 8 CMOS PROM/RPROM	35 ns
WS57C65	4K x 16 CMOS EPROM	70 ns
WS57C256F	32K x 8 CMOS EPROM	55 ns
WS57C257	16K x 16 CMOS EPROM	55 ns
WS59016	16-Bit CMOS Bit Slice Processor	27 MHz
WS59032	32-Bit CMOS Bit Slice Processor	29 MHz
WS59520/21	CMOS Pipeline Register	24 ns
WS59820	CMOS Bi-Directional Register	22 ns
MAP168	User-Configurable Peripheral with Memory	45 ns
PAC1000	User-Configurable 16-Bit Microcontroller	16 MHz
SAM448	User-Configurable Microsequencer	20 MHz

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

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QUALITY STATEMENT

WaferScale Integration, Inc. is committed to producing and delivering defect-free products and services that meet or exceed the specified requirements. We are dedicated to a system of defect prevention and an attitude of zero defects through management example.

The management of WaferScale Integration, Inc. pledges this to you . . . our CUSTOMER.

QUALITY & RELIABILITY PROGRAM

INTRODUCTION

The Quality & Reliability (Q & R) Program at WSI is intended to comply with the latest requirements of: MIL-I-45208, "Inspection System Requirements;" MIL-Q-9858, "Quality Program Requirements;" and Appendix A of MIL-M-38510, "Quality Assurance Program."

The task of the Q & R Program is to assure that all delivered products conform to the requirements of each order placed with the company and to drive the quality and reliability improvement process to optimize product performance and market acceptance.

In order to support the above, WSI has organized its Q & R Department into four main sections:

1.0 Quality Control (QC) — The main functions of QC are:

1.1 QC Engineering — To provide the Quality Control function and the manufacturing function with technical support.

1.2 Materials Quality Control — Assures that all raw materials used in the manufacture of the final product meet WSI specified requirements.

1.3 Process Quality Control — Assures that all WSI manufacturing processes are within their specified control limits and that in-process product maintains the highest quality level.

2.0 Quality Assurance (QA) — The main functions of QA are:

2.1 QA Engineering — To provide a factory interface for customers on all field returns and corrective action requests; to provide technical assistance to other QA functions and engineering functions in matters of product quality.

2.2 QA Inspection — To assure that the final product meets the internal product specifications, applicable customer specifications, and/or other contractual requirements.

2.3 Calibration — To provide a function that assures all equipment used to test or accept product is properly calibrated at set intervals to assure product quality.

3.0 Reliability — The main functions of Reliability are:

3.1 Reliability Engineering (RE) — To assure that all manufactured products reflect the highest reliability standards and to measure this with in-house programs to compare against these standards; to provide technical assistance to other engineering functions in matters of product reliability; to prepare and execute Qualification plans for new or revised designs, packages and processes.

3.2 Reliability Test Lab — To provide suitable step/stress facilities in-house, or at an appropriate vendor, for the purpose of conducting qualifications or quality conformance inspections.

3.3 Failure Analysis Lab — To provide and maintain a Failure Analysis function in-house, or at an appropriate vendor, for the purpose of investigating the cause(s) of failure(s) and for their systematic elimination from the product.

4.0 Configuration Control — The main functions are:

4.1 Document Control — To provide an organized, systematic function for originating, changing and distributing internal specifications and drawings; to provide for the prompt notification of changes to customers with Change Notification Requirements.

4.2 Audits — To provide a system for periodically checking WSI's and vendor's quality programs for compliance with stated policies, procedures and contractual requirements.

4.3 Specification Review and Writing — To provide a function for reviewing customer documentation and converting those requirements to in-house requirements.

5.0 For detailed coverage of WSI's total Q & R System, write or call for our "Quality & Reliability Policy Manual."

QUALITY

What Is Quality?

Quality is something we all strive for, but seem at a loss to define simply. At WSI we have chosen to adopt Phil Crosby's definition because it is the simplest and to-the-point.

Quality is: "Conformance to the requirements."

Quality is not relegated only to the state of the product. It encompasses all administrative areas also. At WSI we strive for *zero defects* and our programs are geared to attain this.

Product Flows

WSI offers five standard product flows which are shown below:

1.0	Flows	883 Class B	Mil-Temp	Standard	Standard	Standard
2.0	Packages	Hermetic	Hermetic	Hermetic	Hermetic	Plastic
3.0	Operating Temperature Range	Military −55°C to +125°C		Industrial −40°C to +85°C	Commercial 0°C to +70°C	

	SCREENS & INSPECTIONS	MIL-STD-883 METHOD/CONDITION OR WSI REQUIREMENT	883	MIL-TEMP	STANDARD	STANDARD	STANDARD
4.0	Preseal Inspection	M2010/Condition B	100%	N/A	N/A	N/A	N/A
		WSI Requirement	N/A	100%	100%	100%	100%
6.0	Temperature Cycle	M1010/Condition C 10 Cycles, −65°C to +150°C	100%	N/A	N/A	N/A	N/A
7.0	Constant Acceleration	M2001/Condition D or E Y1:20K Gs or 30K Gs	100%	N/A	N/A	N/A	N/A
8.0	Hermeticity						
8.1	Fine Leak	M1014/Condition A or B	100%	100%	100%	100%	N/A
8.2	Gross Leak	M1014/Condition C	100%	100%	100%	100%	N/A
9.0	Data Retention (EPROMs only)	Wafers — 72 Hours at 225°C	100%	100%	100%	100%	100%
10.0	Pre Burn-In Electricals	Per Applicable Data Sheet	100%	100%	100%	100%	N/A
11.0	Burn-In	M1015/Condition A or D 160 Hours at +125°C or Equivalent	100%	Note 1	Note 1	Note 1	N/A
12.0	Post Burn-In Electricals	Per Applicable Data Sheet	100%	100%	100%	100%	N/A
13.0	% Defective Allowable	M5004, Paragraph 3.5.1	5%	N/A	N/A	N/A	N/A
14.0	Final Electricals	Per Applicable Data Sheet	100%	100%	100%	100%	100%
15.0	Quality Conformance	QCI per M5005/Group A	Sample	Sample	Sample	Sample	Sample
16.0	External * Visual	M2009	100%	N/A	N/A	N/A	N/A
		WSI Requirement	N/A	100%	100%	100%	100%
17.0	Quality Conformance	QCI per M5005/ Group B, C and D	Sample	N/A	N/A	N/A	N/A
18.0	Shipping Inspection	Every Shipment	100%	100%	100%	100%	100%

* WSI ships visual and mechanical criteria to a 0.1% AQL.

Note: 1. 6–21 hours at 150°C depending on product family. Consult factory for details.

RELIABILITY

INTRODUCTION

WSI is committed to serving its customers with the most reliable products available. From the onset, products are designed, manufactured and tested to rigorous WSI standards which culminate in devices that are better in both performance and reliability.

RELIABILITY GOALS

The failure rate for any integrated circuit has been classically described as having a "bathtub" curve (see Figure 1). The "bathtub" curve shows three main stages of a product's life: 1) A very high failure rate in the beginning, known as the infant mortality period, which normally represent the first 300 hours in a system. 2) A constant failure rate period, with relatively few failures, known as the intrinsic failure rate or useful life. This period represents the next 20 years or more of operation. 3) Eventually, the devices enter the wearout region where failures begin to occur very rapidly again. The mean time to failure for wearout is >20 years.

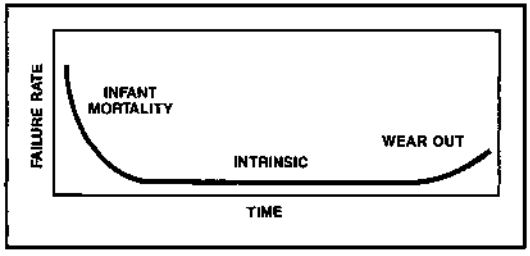


Figure 1 — Bathtub Curve

WSI has established the following Reliability Goals at T_A = 55°C:

• Infant Mortality	0–300 Hours	≤0.1%
• Intrinsic Failure Rate	300 Hours–20 Years	≤100 FITs
• Wear Out		MTTF >20 Years

In order to meet the infant mortality goal of 0.1%, an appropriate burn-in screen may be implemented. Data collected on 10,000 EPROMs, from various wafer fab runs, showed the failure rate to be 0.23% during the first six hours of burn-in which then dropped to 0.02% over the next 21 hours. This demonstrated that a proper burn-in (150°C, 6.5V) for six hours was sufficient to lower the failure rate to less than 0.1%. This screen is revisited on a periodic basis to determine whether or not it is continuing to meet the stated goal. Similar data is collected when a new process is released to production.

RELIABILITY PREDICTION

The life expectancy of an integrated circuit can be accelerated by both temperature and voltage. At WSI, both are used extensively in assessing product reliability.

Temperature

For many years, temperature had been known to be an accelerator of various types of failure mechanisms. By increasing the temperature, it was observed that the devices took less time to fail. By elevating the temperature, long term reliability data can be collected in a relatively short time. Failure rate calculations are based upon data collected from accelerated life testing.

The temperature dependence on accelerating failures has been shown to be exponential. The acceleration factor between two temperatures can be calculated by using the Arrhenius equation:

$$A = \text{Exp}\ \frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

T_1 = Application Junction Temperature
T_2 = Accelerated Stress Junction Temperature
k = 8.62×10^{-5} eV/°K
E_a = Thermal Activation Energy

Each failure mechanism is accelerated differently by temperature. The thermal activation energy is a constant which adjusts for the temperature dependence for the various failure mechanisms. The following activation energies are used for each failure mechanism:

Failure Mechanism	Activation Energy (E_a)
Oxide Defects	0.3 eV
Masking Defects	0.5 eV
Assembly Defects	0.5 eV
Bulk Silicon Defects	0.5 eV
Electromigration	0.5–0.9 eV
Charge Loss	0.6 eV
Contamination	1.0 eV

Voltage

Oxide defects are more highly accelerated by voltage than by temperature (note the low activation energy for oxide defects). To obtain a higher acceleration for oxide defects during a lifetest, the supply voltage is increased by 6.5 volts when possible. By increasing the supply voltage, an additional acceleration of 55× is obtained for oxide defects.

FAILURE RATE CALCULATIONS

Failure rate calculations are based on a summary of the life test results. Typically, the failure rate is calculated for a family of devices manufactured on a given process. To calculate a failure rate, the acceleration factor for each activation energy must be calculated between the accelerated stress temperature and the application temperature. Junction temperatures are used rather than ambient temperatures. The junction temperature is the temperature at the die surface due to the heat generated by the device itself. The junction temperature is the product of the power dissipation multiplied by the thermal resistance of the package and is then added to the ambient temperature.

$$T_J = T_A + (\theta_{JA})(P); \text{ where } P = (I_{CC})(V_{CC})$$

The next step is to calculate the number of accelerated device hours from the lifetest data. The number of device hours is the product of the sample size multiplied by the hours of the lifetest. The equivalent device hours for each activation energy is calculated by multiplying the device hours by the acceleration factor. The failure rate for each activation energy is computed by dividing the total number of failures with the same activation energy by the equivalent device hours. Typically a 60% confidence level is used for calculating failure rates. The total failure rate is the summation of all the failure rates for each activation energy. The failure rate is expressed in FITs which is the number of failures per 10^9 device hours:

$$\text{Failure Rate} = \sum \frac{F(E_a, 60\%\ UCL)}{A(E_a, T_1, T_2) \times D} \times 10^9 \text{ FITs}$$

$F(E_a, 60\%\ UCL) = 1.049$ (Failures with same E_a) + 1.0305
$A(E_a, T_1, T_2)$ = Acceleration Factor
D = Device Hours

RELIABILITY DATA SUMMARY

The Reliability Data Summary is a quarterly publication which presents all WSI reliability data and is available to WSI customers. The data is presented with the test results at each timepoint with accompanying failure analysis where applicable. In this manner, the customer can compute the failure rate for his own application. For convenience, the failure rates have been computed to 55°C using the previous method discussed.

Current life test results show a failure rate of 63 FITs at 55°C on EPROMs with a density of 64K and higher. This data was computed from approximately 9 million device hours. The failure rate for Bit Slice products was approximately 106 FITs after 2 million device hours.

PRODUCT RELIABILITY

ElectroStatic Discharge Sensitivity (ESDS)

WSI products are tested for ESDS in accordance with Method 3015 of MIL-STD-883. Typical inputs fail around 5,000 volts and outputs fail in the range of 3,000 to 5,000 volts. Testing is performed on new products or when changes occur that can influence the ESDS of a device (i.e., redesign, new process, etc.).

Latch-Up

Latch-up is a condition that occurs due to excessive current (spikes) in the circuit periphery and creates a large potential that triggers a parasitic SCR inherent to all CMOS processes. Latch-up can be destructive to the device. To reduce latch-up, WSI employs an epitaxial layer above a low resistivity substrate. This diverts the current to the substrate, away from the active circuitry, reducing the lateral potential which triggers the latch-up. WSI products are tested for latch-up between −1.0 and +7.0 volts with currents up to 200 mA forced on any one pin.

Qualifications

All new processes, major process changes, or new design rules must pass a reliability qualification. One to three lots are used depending on the reliability risk involved. Qualification requires a minimum 1000-hour life test at 125°C. EPROMs are stressed dynamically at 150°C with an overvoltage condition of 6.5 volts. (The overvoltage accelerates oxide defects an additional 55×.) Qualifications place heavy emphasis on the first 48 hours (infant mortality) of the life test. Larger sample sizes are used initially with the number decreasing as the qualification progresses. If other reliability stresses are to be used in the qualification, those units will receive a 48-hour burn-in prior to starting those stresses in order to eliminate any unrelated failures.

Logic and EPROM products run on the same fab process with the Logic products lacking the steps for the EPROM products. The peripheral circuitry of the EPROM, decoders, I/Os, etc., have the identical design rules as the Logic products. Every reliability evaluation on an EPROM product also evaluates the Logic product line. Testing and failure analysis is easier on an EPROM. Because of the large availability of EPROM burn-in boards, larger sample sizes can be used. Also, the straightforward operation of an EPROM allows 100% dynamic stressing during burn-in at a higher temperature and voltage.

EPROMs are subjected to special qualification requirements to study the data retention characteristics of the EPROM cell. These devices are programmed with a 100% zero pattern and then baked at 150°C, 200°C, and 250°C for 1000 hours. These tests are performed to insure that WSI reliability goals have been met.

Other tests include Temperature Cycle from −65°C to +150°C for 1000 cycles. In addition, plastic packaged products must pass 1000 hours of Temperature Humidity Bias at 85°C and 85% relative humidity or 100 hours of HAST (High Accelerated Stress Test) at 120°C and 85% relative humidity, and 168 hours of Pressure Pot at 15 PSIG.

EPROMs

Because of the floating gate storage cell, EPROMs have unique reliability considerations. Data retention is related to the ability to store a charge on the floating gate of the EPROM cell. Charge loss can shift the threshold of the EPROM cell from a programmed state to an unprogrammed state, i.e., from a logical 0 to a 1. Charge loss is the result of defects in the oxide surrounding the floating gate. These defects occur during wafer processing and generally affect a single bit in the array. It has been shown that defective bits of this type lose their charge very rapidly with high temperature. For this reason, they can be effectively screened out with a high temperature bake.

EPROM Screening

Data retention screening is performed on all EPROM products. Screening is at the wafer level so that higher temperatures can be used without the fear of affecting the solderability of a packaged unit. The screen consists of programming each device 100% and then baking the wafers for 72 hours at 225°C. After the bake, the 100% pattern is verified. This screen is equivalent to 11.5 years of continuous operation at 55°C.

Charge can also flow electrically to the floating gate. Charge gain is charge transfer from either the word line or the bit line to the floating gate such that an unprogrammed device becomes programmed. To date, charge gain has not been observed on any WSI EPROM.

EPROM Programming

Electrical charge loss is the major cause for programming failure. Program Disturb is charge transfer from the floating gate to the bit line. This charge loss mechanism occurs during programming due to the high electrical fields present. Failure occurs when an already programmed cell loses charge as other cells, with the same bit line, are being programmed. This failure mechanism is the result of oxide defects at the edge of the floating gate.

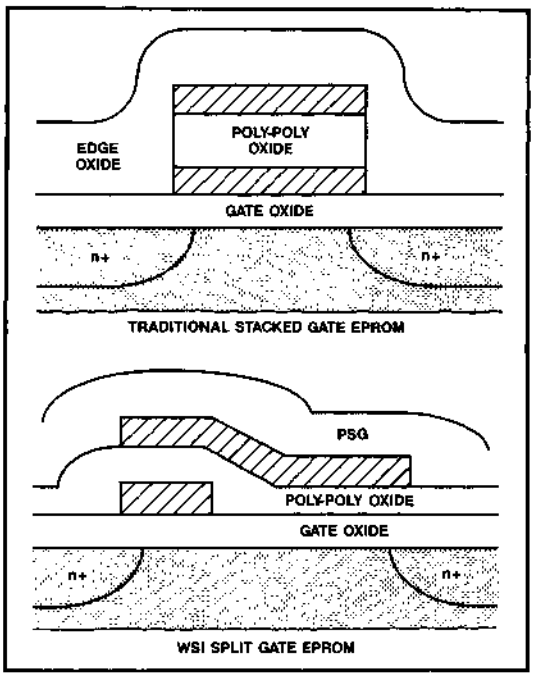
DC Erase is electrical charge loss to the word line. DC Erase is the result of defects in the oxide between the floating gate and the word line above. Like Program Disturb, DC Erase occurs during programming when an already programmed cell losses charge as adjacent cells on the same word line are programmed.

The WSI split gate EPROM has matured to the point that programmability by the customer can be >99.9%. Product Assurance data collected on over 5000 units showed programmability to be 99.98%. The most recent Program/Erase cycling data had no fails out to 100 cycles. By focusing on eliminating Program Disturb and DC Erase, the threshold of a programmed EPROM cell is consistently well above 7.0 volts and typically above 8.0 volts. This provides additional operating margin and reliability.

Split Gate vs. Traditional EPROMs

The patented WSI split gate EPROM (Patent Numbers 4,328,565; 4,361,847; 4,409,723; 4,639,893; 4,795,719; 4,649,520; 4,758,869) has several inherent advantages over the traditional stacked gate EPROM. One major advantage is better control over the etching of the floating gate during wafer processing. With the traditional stacked gate EPROM, a self-aligning process is used to define the floating gate. That is, a layer of poly is first deposited for the floating gate, followed by an oxide layer, and finally another poly layer for the control gate. To define and etch the floating gate, the control gate poly and poly-poly oxide are first etched and are used as the mask to define the floating gate. This means that the etching of the control gate and the poly-poly oxide must be very well controlled in order to achieve good definition of the floating gate. For the WSI split gate EPROM, the floating gate is etched using conventional methods in the step following the poly deposition of the floating gate. This way the floating gate etch is very well controlled and is not dependent upon both a poly and an oxide etch.

This leads to another advantage for the WSI split gate EPROM. Because of the critical etching involved with the traditional stacked gate EPROM, it is difficult to use a silicide on the control gate to reduce the poly resistance and speed up the device. The conventional processing steps used to make the WSI split gate EPROM does allow for the successful use of silicide and is used on many products.



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Another advantage lies in the quality of the oxide surrounding the floating gate. Following the floating gate etch on the stacked gate EPROM, a third oxide is grown which contacts the edge of the floating gate as well as the poly-poly oxide. The floating gate is now surrounded by three separate oxides (gate oxide, poly-poly oxide and edge oxide), all of which contribute to defects. On the other hand, the WSI split gate EPROM has a homogeneous poly-poly oxide which contacts the floating gate at the top as well as the edges. Because the floating gate of the split gate EPROM is surrounded by only two oxides, neither of which are etched, better oxide integrity is obtained. Oxide integrity is the key in reducing reliability problems such as: Data Retention, Program Disturb and DC Erase.

PROCESS RELIABILITY

WSI utilizes a Class 10 wafer fab facility for all its wafer processing. Most processing is performed by robotics which reduces the human factors such as contamination and handling from contributing to reliability failures. Photolithography is performed using state-of-the-art steppers which eliminates marginal mask defects from becoming reliability hazards. Passivation cracks and metal shifting on double layer metal devices are minimized on even large die through a planarization process. When processing is completed, the back of the wafer is polished to remove oxides and other processing artifacts. This results in better eutectic die attach at assembly and reduces the chances of die cracking.

The CMOS Advantage

The low power characteristics of CMOS greatly enhance the reliability of any system. This can be demonstrated by comparing the thermal characteristics of WSI's RPROM vs a Bipolar PROM and applying it to reliability.

For instance, if we assume a 24-pin CERDIP package with a thermal resistance of 63°C in an ambient temperature of 55°C, the following junction temperatures are obtained:

WS57C49 CMOS RPROM (Standby)	WS57C49 CMOS RPROM (18 MHz)	64K Bipolar PROM
I_{CC} = 15 mA	I_{CC} = 50 mA	I_{CC} = 150 mA
P = 75 mW	P = 250 mW	P = 750 mW
T_R = 5°C	T_R = 16°C	T_R = 47°C
T_J = 60°C	T_J = 71°C	T_J = 102°C

Calculating the acceleration factor of the Bipolar PROM over the WSI EPROM, using an activation energy of 0.5 eV, we find that the acceleration is 7× in the standby mode and 4× at 18 MHz. This means that by running cooler, the WSI RPROM will have a life expectancy of 4 to 7 times greater than its Bipolar PROM equivalent.

The following tables show reliability results obtained on various WSI products.

TABLE 1. EPROM RELIABILITY DATA

DYNAMIC HIGH TEMPERATURE LIFE TEST

CONDITIONS	48 HOURS	168 HOURS	500 HOURS	1000 HOURS	1500 HOURS	2000 HOURS
125°C/6.5V	0/450	0/450	0/450	0/450		
150°C/6.5V	13/15,479	5/9385	13/8344	18/7923	0/486	0/486

Total Device Hours: 9,088,228 @ 150°C
450,000 @ 125°C

Junction Temperature Above Ambient: +5°C

Ea	Accelerated Device Hours	# Failures	Failure Rate
0.3 eV × 55	5.11 × 10 E9	1	0.4 FITs
0.5 eV	4.43 × 10 E8	7	19 FITs
0.6 eV	9.58 × 10 E8	39	43 FITs
1.0 eV	2.09 × 10 E10	2	0.2 FITs

Total Failure Rate: 62.6 FITs (55°C; 60% Confidence Level)

TABLE 1. EPROM RELIABILITY DATA (Cont.)

HIGH TEMPERATURE STORAGE LIFE TEST

CONDITIONS	48 HOURS	72 HOURS	168 HOURS	500 HOURS	1000 HOURS
150°C	0/375		0/375	0/375	0/375
170°C	0/144		0/144	1/144	1/143
200°C	1/1630		9/1629	11/1620	12/1609
225°C		0/416	5/416	9/411	9/402

Product Types: WS27C64F, WS57C64F, WS57C49, WS27C128F, WS27C256F, WS27C256L, WS57C43B, WS57C49B, WS57C256F.

TABLE 2. OTP EPROM RELIABILITY DATA

DYNAMIC HIGH TEMPERATURE LIFE TEST

DHTL 150°C 6.5 Volts	48 Hours	168 Hours	500 Hours	1000 Hours
	4/3495	0/1252	0/1183	6/1175

TEMPERATURE/HUMIDITY WITH BIAS

THB 85°C/85% RH 5.0 Volts	168 Hours	500 Hours	1000 Hours
	0/287	0/287	0/287

HIGHLY ACCELERATED STRESS TEST (HAST)

CONDITIONS	100 HOURS	200 HOURS
120°C/85% RH	0/351	0/39

PRESSURE POT

PPOT 15 PSIG/121°C	96 Hours	168 Hours	240 Hours
	1/734	1/733	8/732

TEMPERATURE CYCLE

TC −55°C/+150°C	100 Cycles	500 Cycles	1000 Cycles
	0/572	3/572	12/569

Products: WS57C64F, WS27C256L, WS57C49B, WS27C64F, WS27C256F, WS57C49, WS57C256F

TABLE 3. BIT SLICE RELIABILITY DATA

DYNAMIC HIGH TEMPERATURE LIFE TEST

CONDITIONS	48 HOURS	168 HOURS	500 HOURS	1000 HOURS	1500 HOURS	2000 HOURS
125°C/6.5V	1/1550	0/1382	1/1246	0/848	0/120	0/120
150°C/6.5V	1/1842	1/1170	2/642	0/639		

Product Hours	Failures	Act. Eng.	Failure Rate 60% Conf at 55°C
1,197,912 at 125°C	1	1.0 eV	0.9 FITs
761,460 at 150°C	5	0.5 eV	105 FITs

Combined Failure Rate: 105.9 FITs

HIGH TEMPERATURE STORAGE LIFE

CONDITIONS	168 HOURS	336 HOURS	500 HOURS	1000 HOURS
150°C	0/145	0/145	0/145	0/145
200°C	1/180	0/179	1/179	

TEMPERATURE HUMIDITY BIAS

CONDITIONS	PACKAGE	168 HOURS	500 HOURS	1000 HOURS
85°C/85% RH	PLASTIC	1/473	0/473	4/473

PRESSURE POT

CONDITIONS	PACKAGE	96 HOURS	168 HOURS	240 HOURS
121°C/15 PSIG	PLASTIC	2/609	0/607	0/182
121°C/15 PSIG	PPGA	0/52	0/52	

TEMPERATURE CYCLE (AIR TO AIR)

CONDITIONS	PACKAGE	100 CYCL	500 CYCL	1000 CYCL
−65°C/+150°C	CERDIP	0/78	0/78	0/78
−65°C/+150°C	PLASTIC	0/572	2/572	3/570

Products: WS5901, WS59016, WS5910A, WS59520, ASIC1004

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 800-562-6363.

PACKAGE INTRODUCTION

WSI offers its integrated circuit products in a wide variety of package styles. Hermetic, plastic, through-board, surface mount, windowed and windowless package types are all available.

Hermetic:	Side Brazed Ceramic DIP, 0.6"/0.9" CERDIP, 0.3"/0.6" Ceramic Flatpack Ceramic Quad Flatpack, Gullwing Ceramic PGA Ceramic Leaded Chip Carrier Ceramic Leadless Chip Carrier
Plastic:	Plastic Leaded Chip Carrier Plastic DIP, 0.3"/0.6"/0.9" Plastic Quad Flatpack, Gullwing
Surface Mount:	Ceramic Leadless Chip Carrier Ceramic Leaded Chip Carrier Ceramic Quad Flatpack, Gullwing Plastic Quad Flatpack, Gullwing Plastic Leaded Chip Carrier Ceramic Flatpack

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For information concerning packages available for a particular product, please consult the Ordering Information chart included on each Preliminary and Final product data sheet.

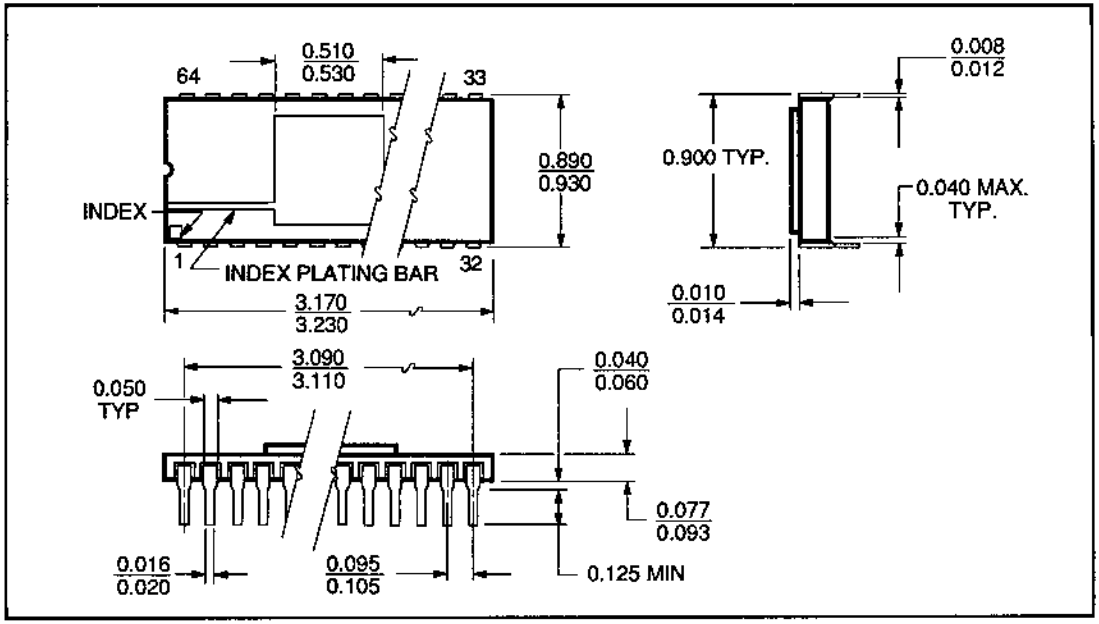
PACKAGE INFORMATION
(By Drawing Number)

Pins	Package	Window	Package Type	Drawing
64	Side Brazed Ceramic DIP, 0.9"	No	B	B1
(28)	Ceramic Leadless Chip Carrier	Yes	C	C1
(32)	Ceramic Leadless Chip Carrier	Yes	C	C2
(44)	Ceramic Leadless Chip Carrier	Yes	C	C3
24	CERDIP, 0.6"	Yes	D	D1
28	CERDIP, 0.6"	Yes	D	D2
40	CERDIP, 0.6"	Yes	D	D3
32	CERDIP, 0.6"	Yes	D	D4
24	Ceramic Flatpack	Yes	F	F1
28	Ceramic Flatpack	Yes	F	F2
100	Ceramic Quad Flatpack, Gullwing	Yes	F	F3
68	Ceramic PGA	No	G	G1
101	Ceramic PGA	No	G	G2
24	Ceramic Flatpack	No	H	H1
28	Ceramic Flatpack	No	H	H2
100	Ceramic Quad Flatpack, Gullwing	No	H	H3
68	Plastic Leaded Chip Carrier	No	J	J1
44	Plastic Leaded Chip Carrier	No	J	J2
28	Plastic Leaded Chip Carrier	No	J	J3
32	Plastic Leaded Chip Carrier	No	J	J4
24	CERDIP, 0.3"	No	K	K1
28	Ceramic Leaded Chip Carrier	Yes	L	L2
32	Ceramic Leaded Chip Carrier	Yes	L	L3
44	Ceramic Leaded Chip Carrier	Yes	L	L4
68	Ceramic Leaded Chip Carrier	No	N	N1
32	Ceramic Leaded Chip Carrier	No	N	N2
40	Plastic DIP, 0.6"	No	P	P1
24	Plastic DIP, 0.6"	No	P	P2
28	Plastic DIP, 0.6"	No	P	P3
64	Plastic DIP, 0.9"	No	P	P4
32	Plastic DIP, 0.6"	No	P	P5
100	Plastic Quad Flatpack, Gullwing	No	Q	Q1
40	Side Brazed Ceramic DIP, 0.6"	Yes (2)	R	R1 (Module)
32	Side Brazed Ceramic DIP, 0.6"	Yes (2)	R	R2 (Module)
24	Plastic DIP, 0.3"	No	S	S1
28	Plastic DIP, 0.3"	No	S	S2
24	CERDIP, 0.3"	Yes	T	T1
28	CERDIP, 0.3"	Yes	T	T2
88	Ceramic PGA	Yes	X	X1
44	Ceramic PGA	Yes	X	X2
40	CERDIP, 0.6"	No	Y	Y1
32	CERDIP, 0.6"	No	Y	Y2
24	CERDIP, 0.6"	No	Y	Y3
(68)	Ceramic Leadless Chip Carrier	No	Z	Z1
(28)	Ceramic Leadless Chip Carrier	No	Z	Z2

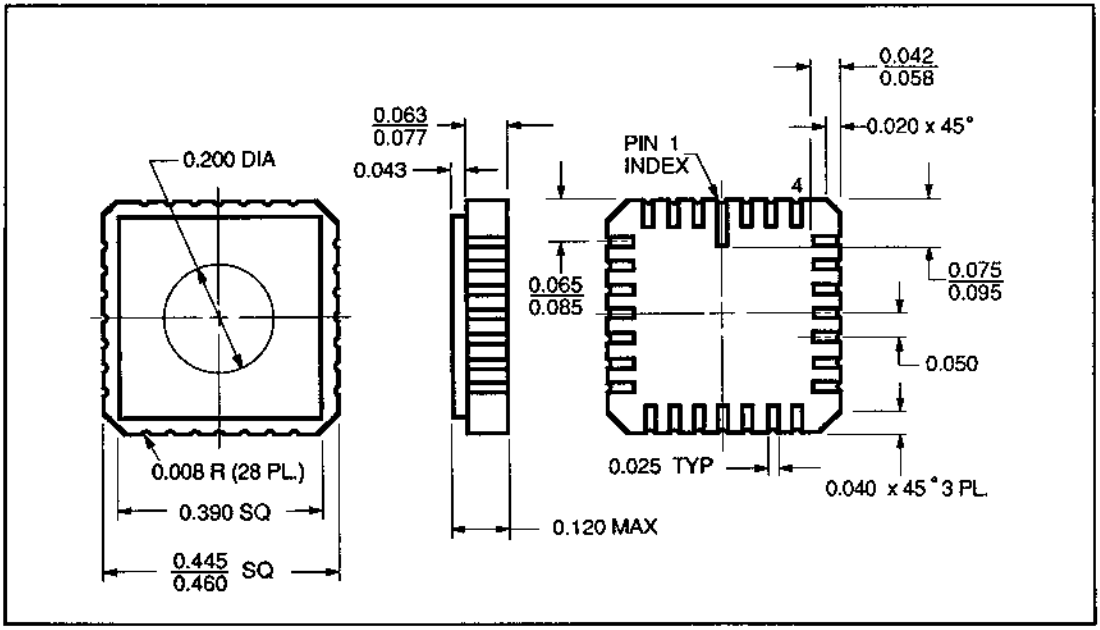
PACKAGE INFORMATION
(By Pin Count)

Pins	Package	Window	Package Type	Drawing
24	CERDIP, 0.3"	No	K	K1
24	Plastic DIP, 0.3"	No	S	S1
24	CERDIP, 0.6"	Yes	D	D1
24	CERDIP, 0.6"	No	Y	Y3
24	Ceramic Flatpack	Yes	F	F1
24	Ceramic Flatpack	No	H	H1
24	CERDIP, 0.3"	Yes	T	T1
24	Plastic DIP, 0.6"	No	P	P2
28	Plastic DIP, 0.3"	No	S	S2
28	Plastic DIP, 0.6"	No	P	P3
(28)	Ceramic Leadless Chip Carrier	Yes	C	C1
(28)	Ceramic Leadless Chip Carrier	No	Z	Z2
28	CERDIP, 0.6"	Yes	D	D2
28	Plastic Leaded Chip Carrier	No	J	J3
28	Ceramic Leaded Chip Carrier	Yes	L	L2
28	CERDIP, 0.3"	Yes	T	T2
28	Ceramic Flatpack	Yes	F	F2
28	Ceramic Flatpack	No	H	H2
(32)	Ceramic Leadless Chip Carrier	Yes	C	C2
32	CERDIP, 0.6"	Yes	D	D4
32	CERDIP, 0.6"	No	Y	Y2
32	Plastic Leaded Chip Carrier	No	J	J4
32	Ceramic Leaded Chip Carrier	Yes	L	L3
32	Ceramic Leaded Chip Carrier	No	N	N2
32	Plastic DIP, 0.6"	No	P	P5
32	Side Brazed Ceramic DIP, 0.6"	Yes (2)	R	R2 (Module)
40	CERDIP, 0.6"	No	Y	Y1
40	Plastic DIP, 0.6"	No	P	P1
40	CERDIP, 0.6"	Yes	D	D3
40	Side Brazed Ceramic DIP, 0.6"	Yes (2)	R	R1 (Module)
44	Ceramic PGA	Yes	X	X2
(44)	Ceramic Leadless Chip Carrier	Yes	C	C3
44	Plastic Leaded Chip Carrier	No	J	J2
44	Ceramic Leaded Chip Carrier	Yes	L	L4
64	Side Brazed Ceramic DIP, 0.9"	No	B	B1
64	Plastic DIP, 0.9"	No	P	P4
68	Ceramic PGA	No	G	G1
(68)	Ceramic Leadless Chip Carrier	No	Z	Z1
68	Plastic Leaded Chip Carrier	No	J	J1
68	Ceramic Leaded Chip Carrier	No	N	N1
88	Ceramic PGA	Yes	X	X1
100	Ceramic Quad Flatpack, Gullwing	Yes	F	F3
100	Ceramic Quad Flatpack, Gullwing	No	H	H3
100	Plastic Quad Flatpack, Gullwing	No	Q	Q1
101	Ceramic PGA	No	G	G2

DRAWING B1 64 Pin Side Brazed Ceramic Dip (Package Type B)



DRAWING C1 28 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



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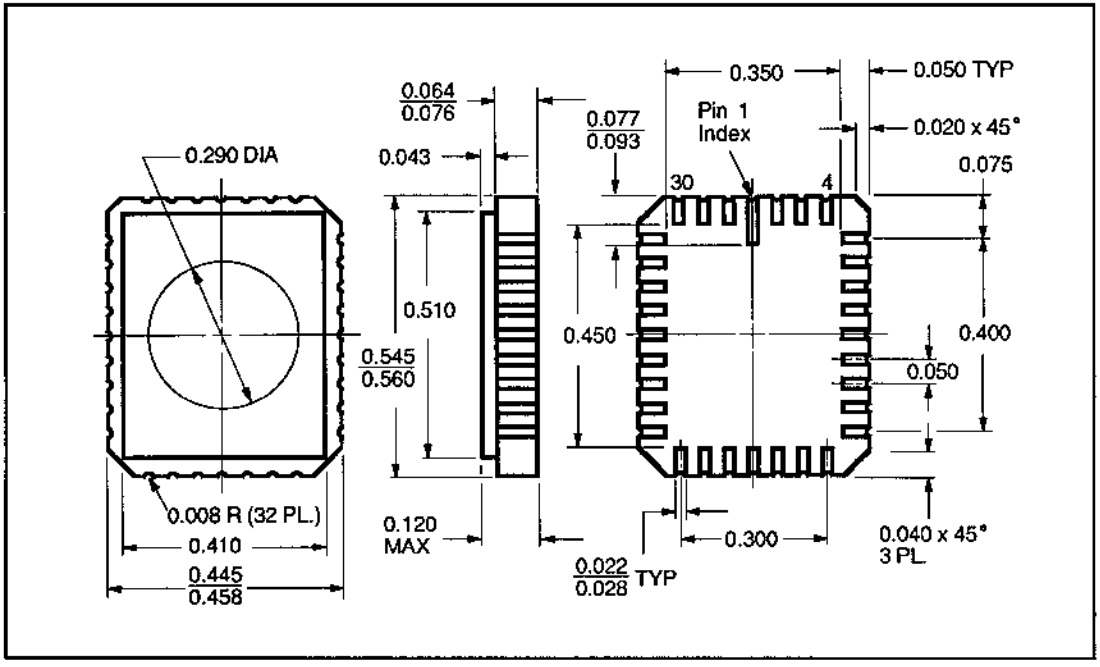
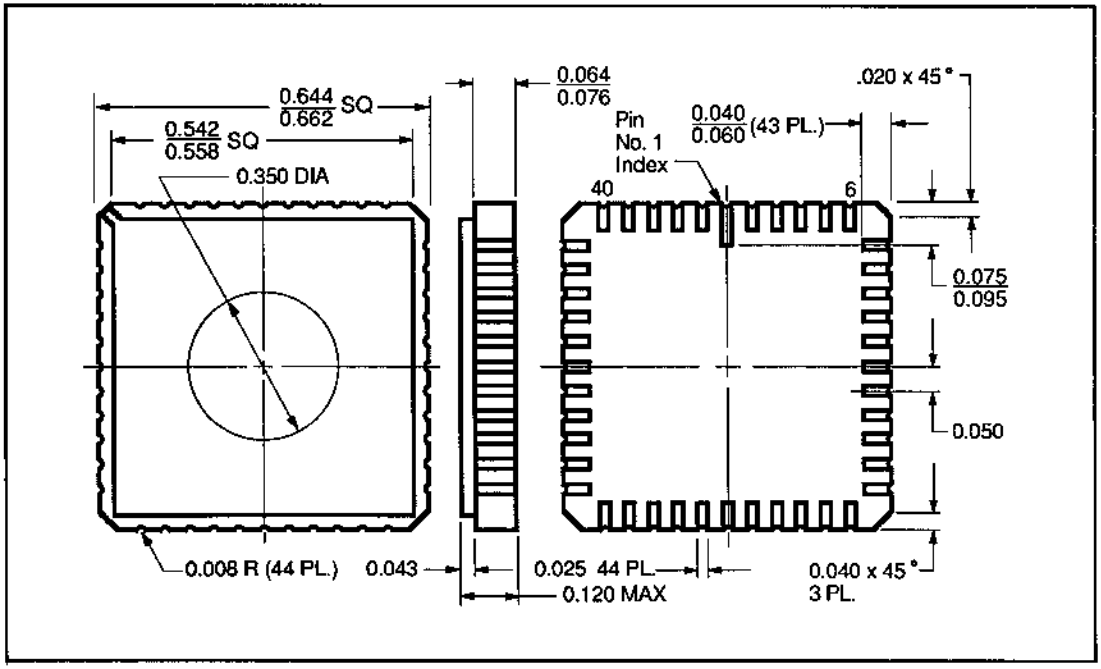
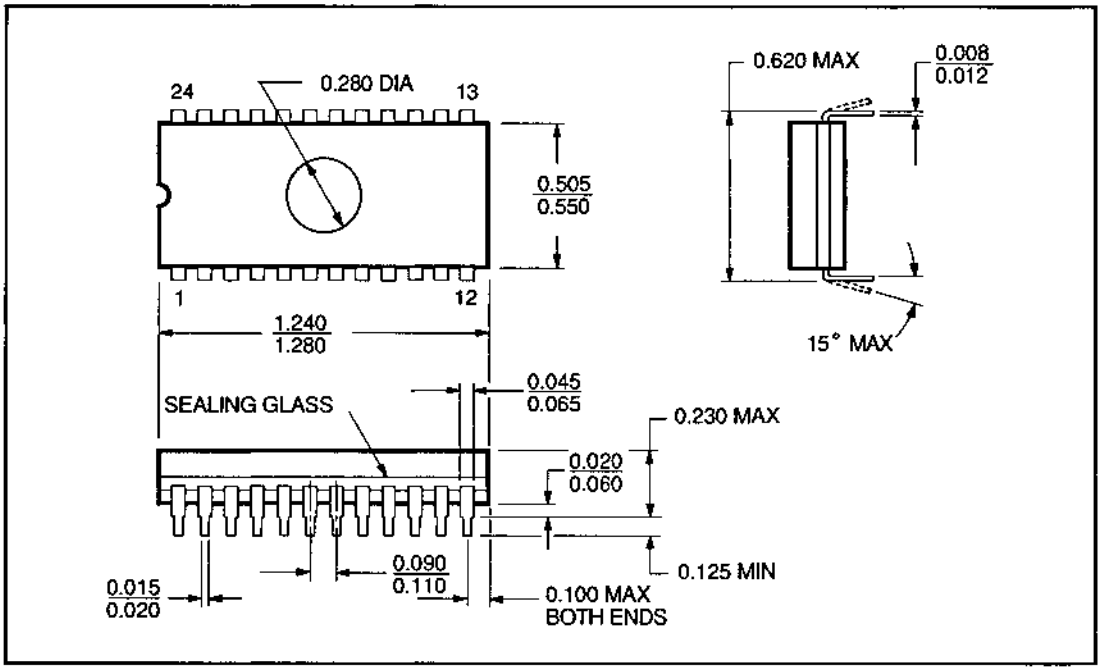
DRAWING C2 32 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



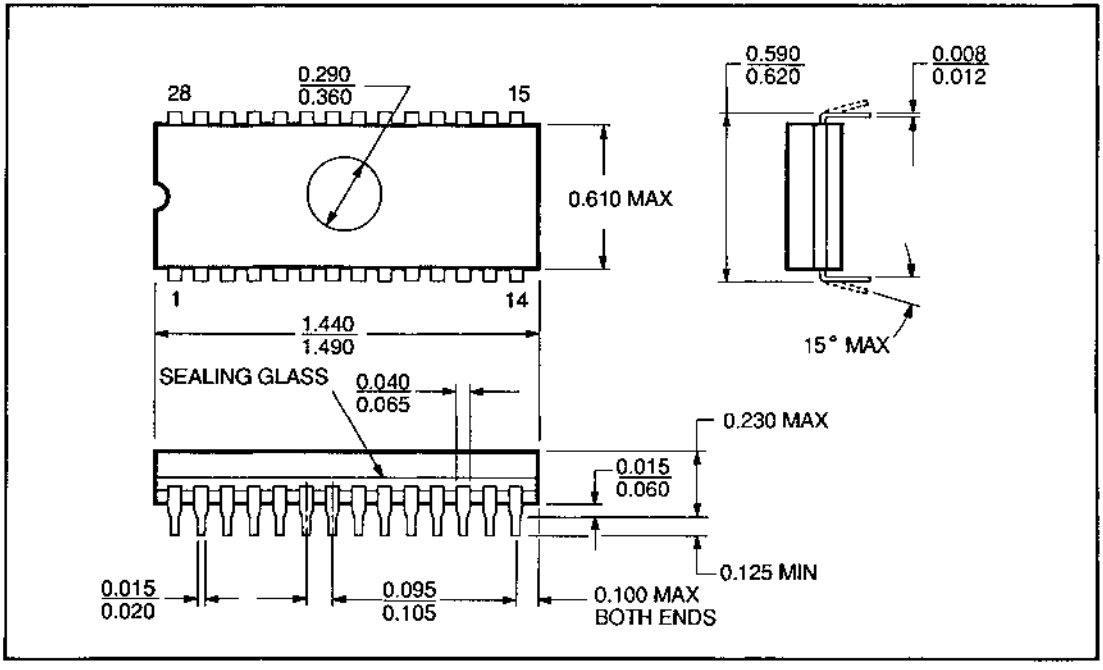
DRAWING C3 44 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



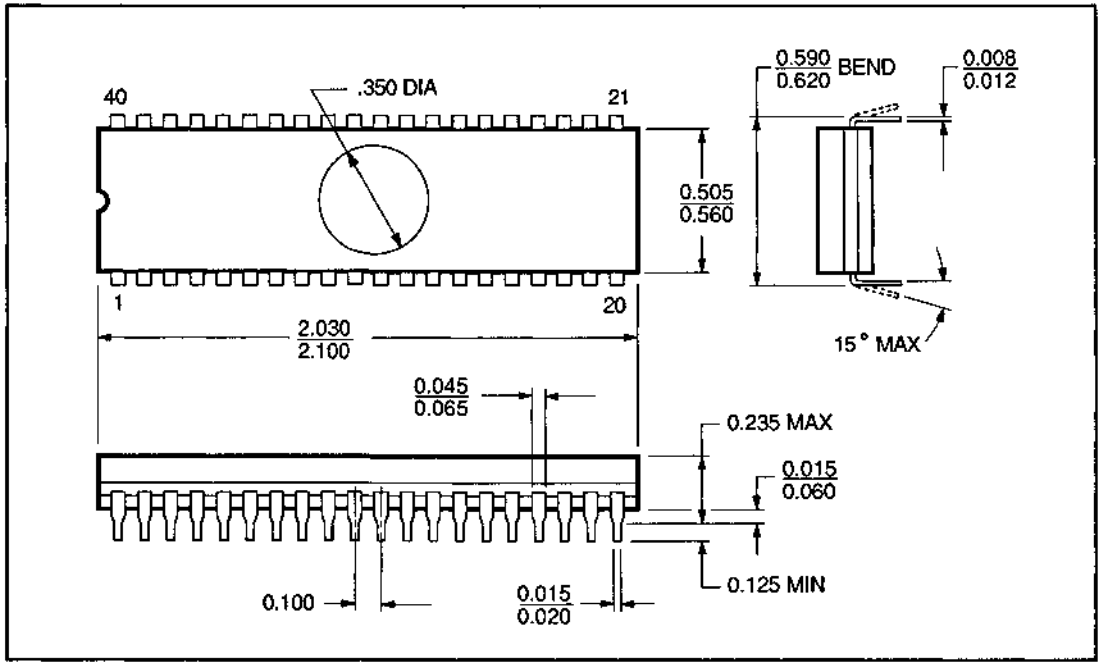
DRAWING D1 24 Pin CERDIP (Package Type D)



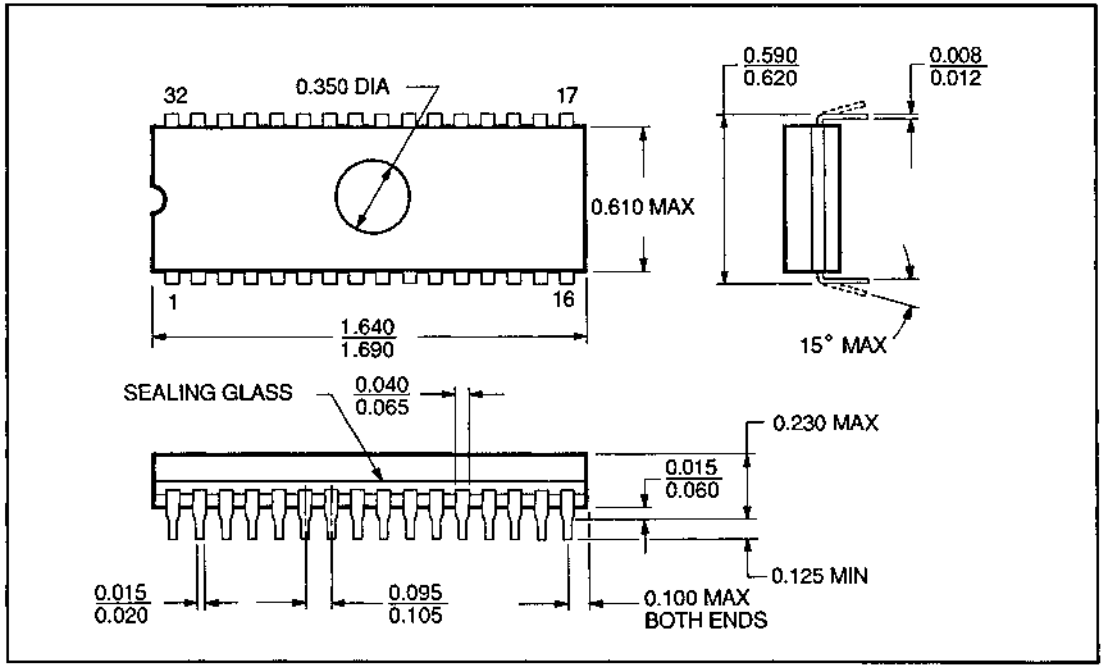
DRAWING D2 28 Pin CERDIP (Package Type D)



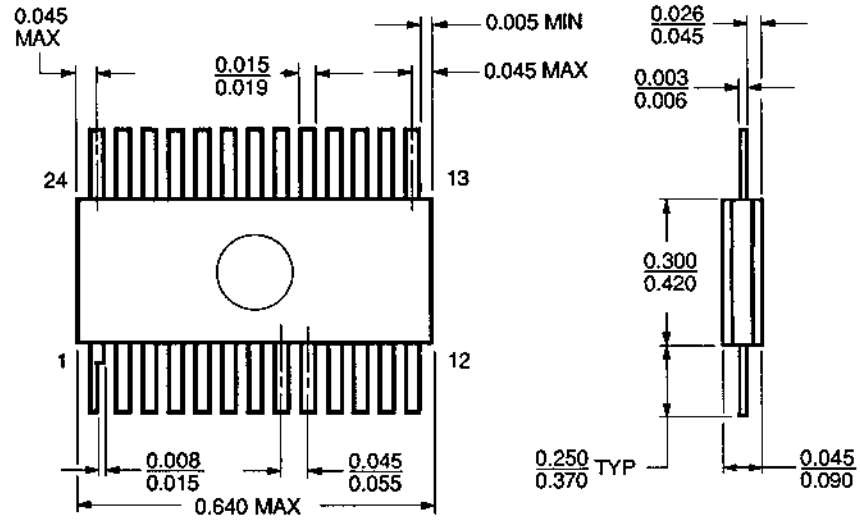
DRAWING D3 40 Pin CERDIP (Package Type D)



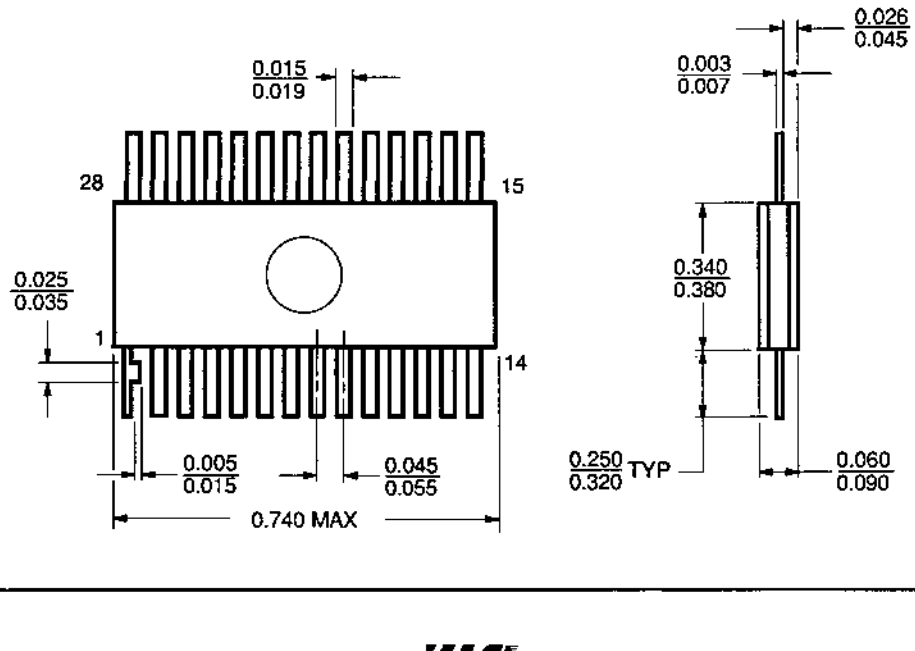
DRAWING D4 32 Pin CERDIP (Package Type D)



DRAWING F1 24 Pin Ceramic Flatpack (Package Type F)

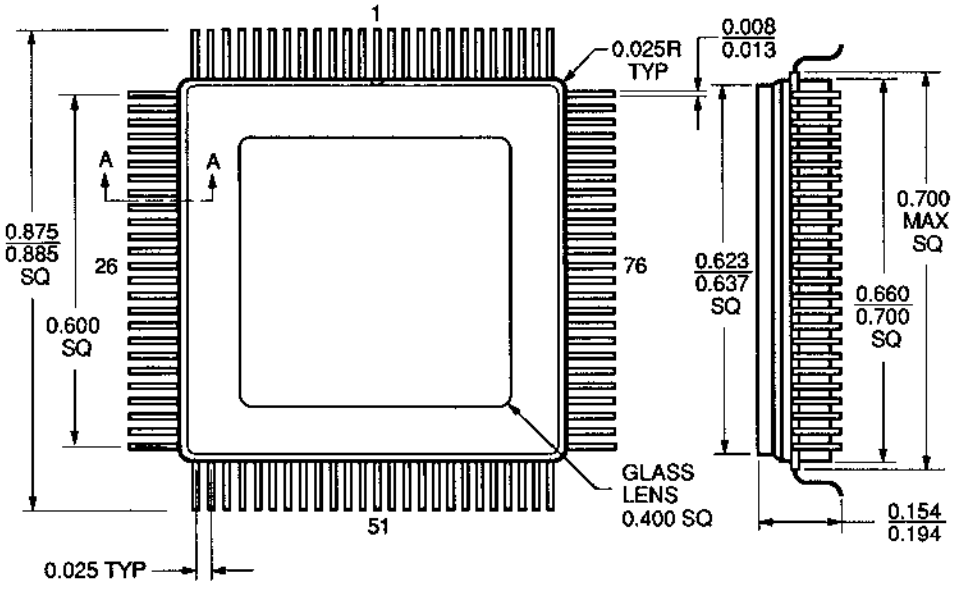


DRAWING F2 28 Pin Ceramic Flatpack (Package Type F)

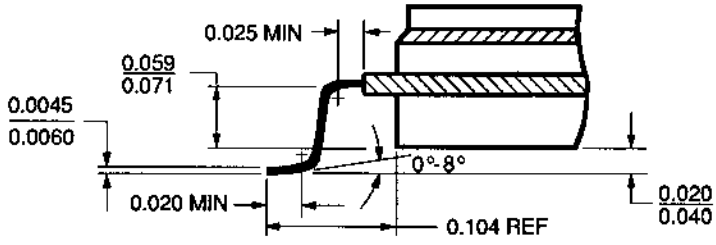


9

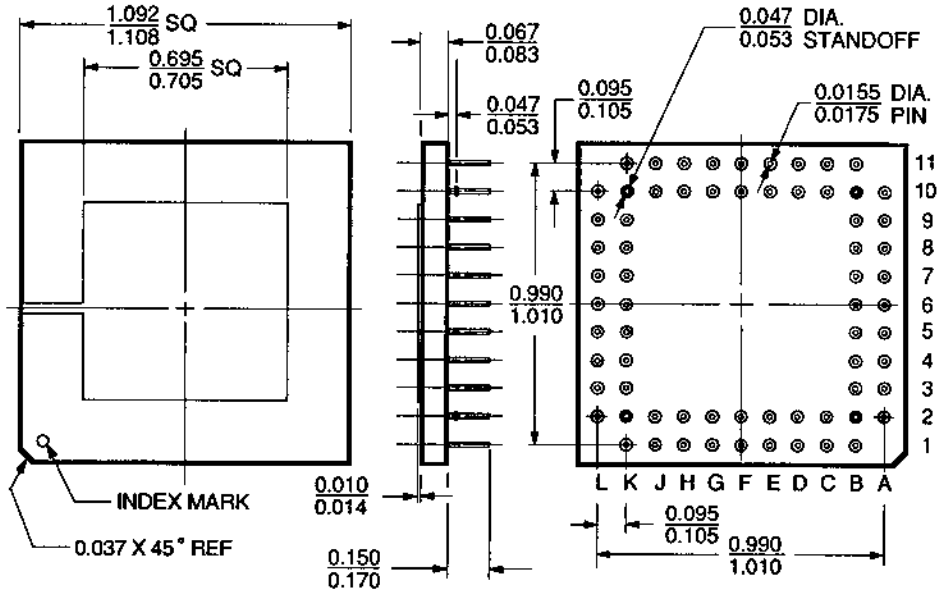
DRAWING F3 100 Pin Ceramic Quad Flatpack (with window), Gullwing, Fine Pitch (Package Type F)



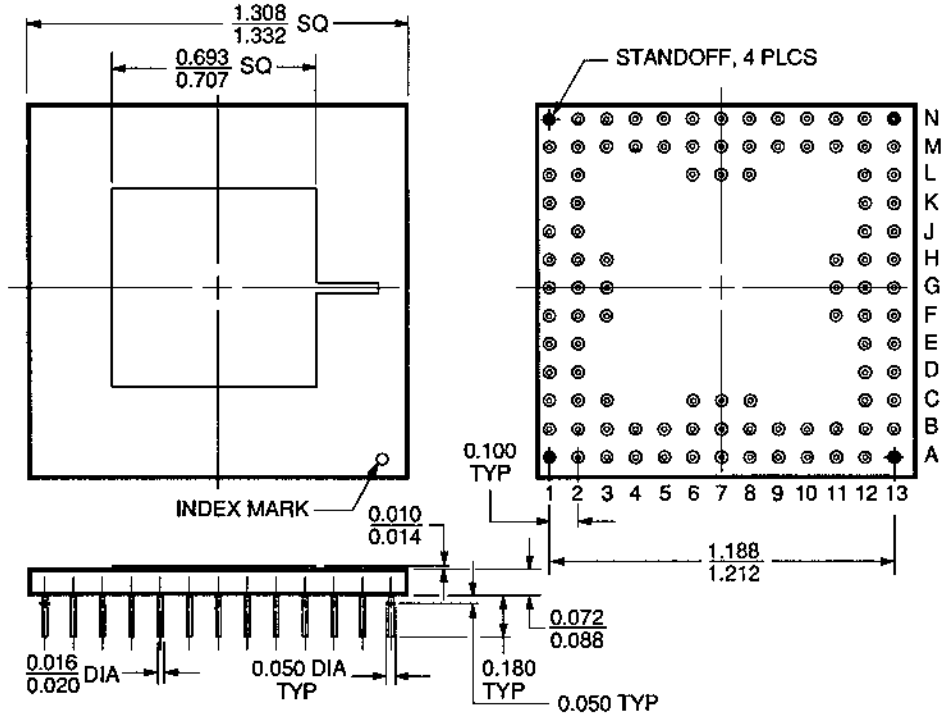
SECTION A-A



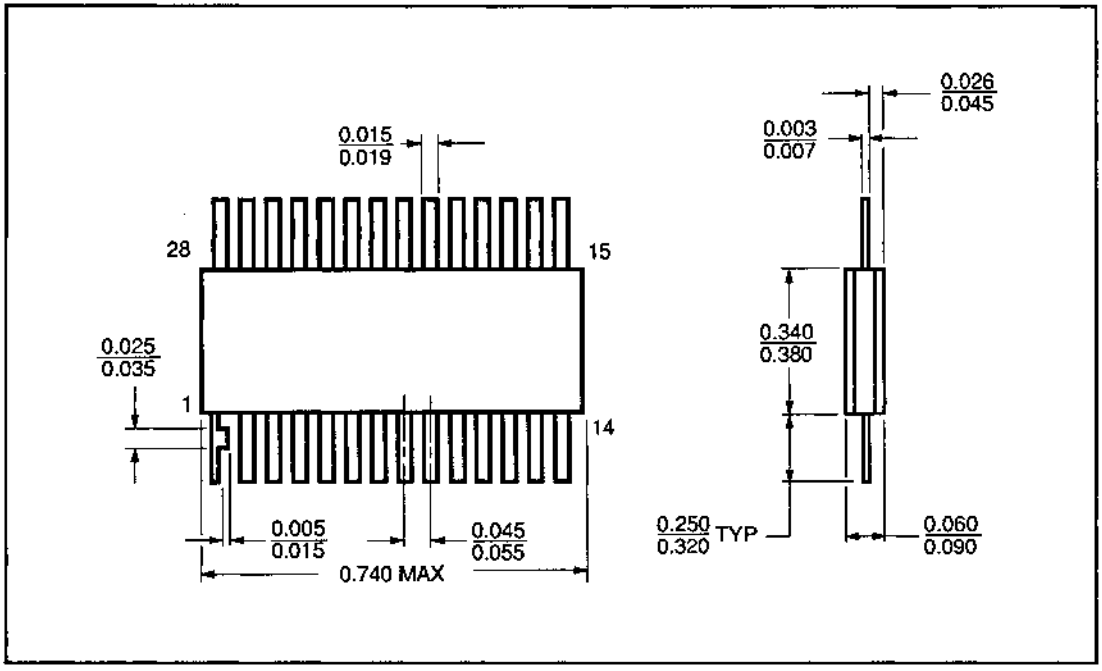
DRAWING G1 68 Pin Ceramic PGA (Package Type G)



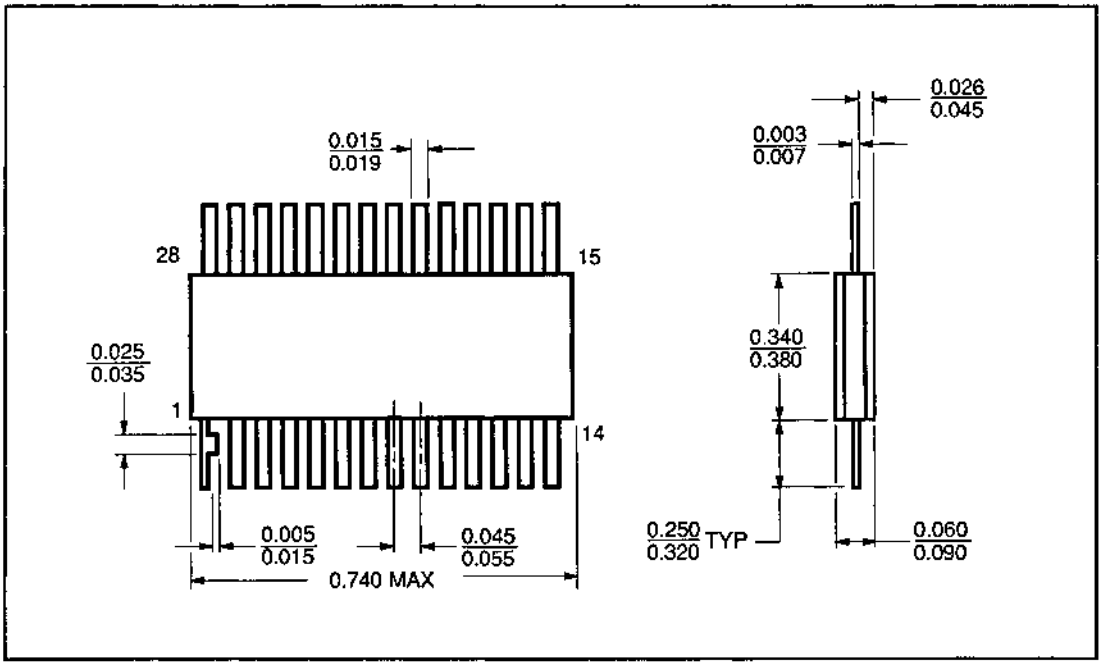
DRAWING G2 101 Pin Ceramic PGA (Package Type G)



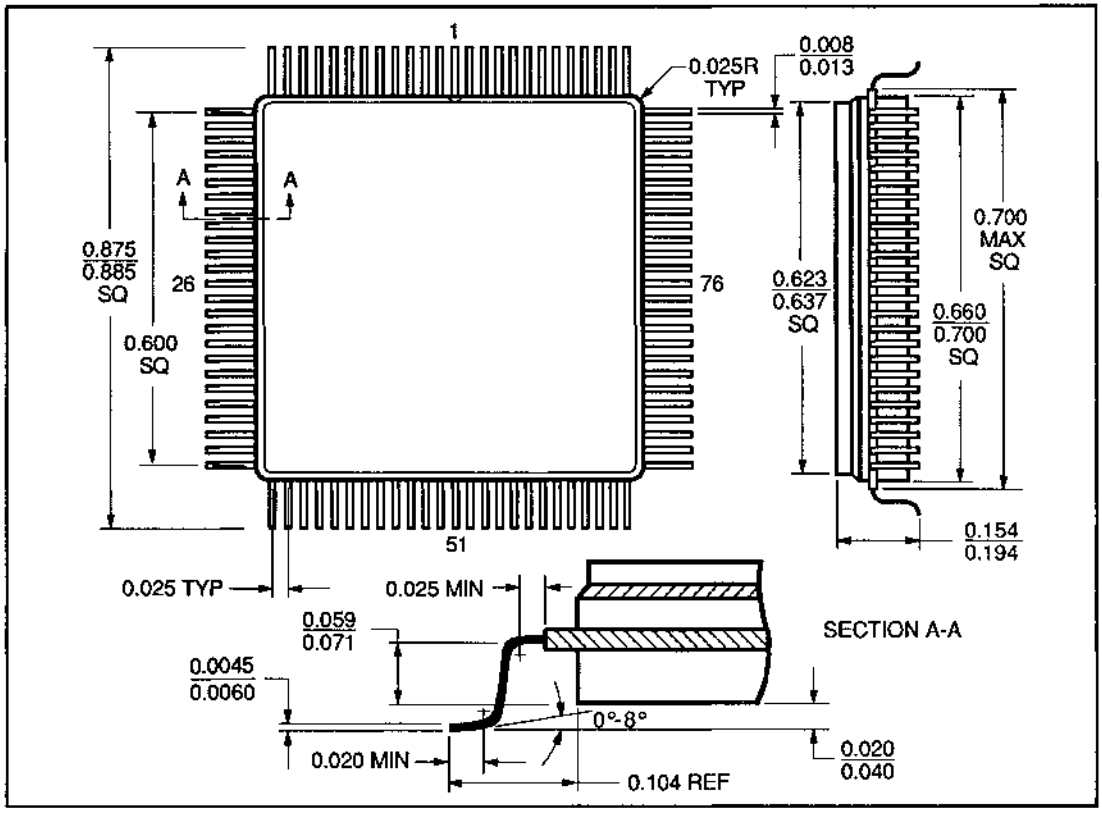
DRAWING H1 28 Pin Ceramic Flatpack (Package Type H)



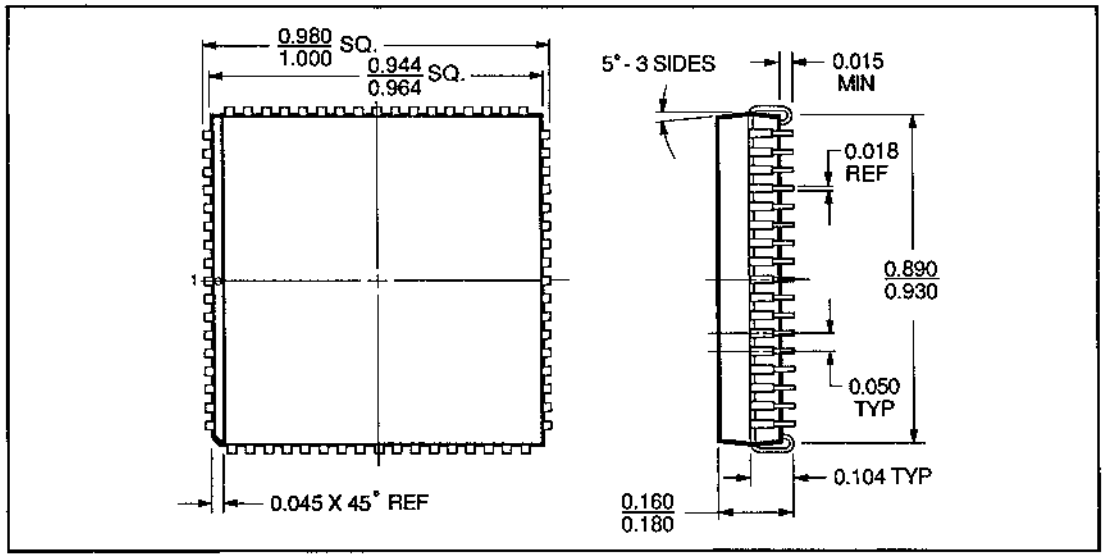
DRAWING H2 28 Pin Ceramic Flatpack (Package Type H)



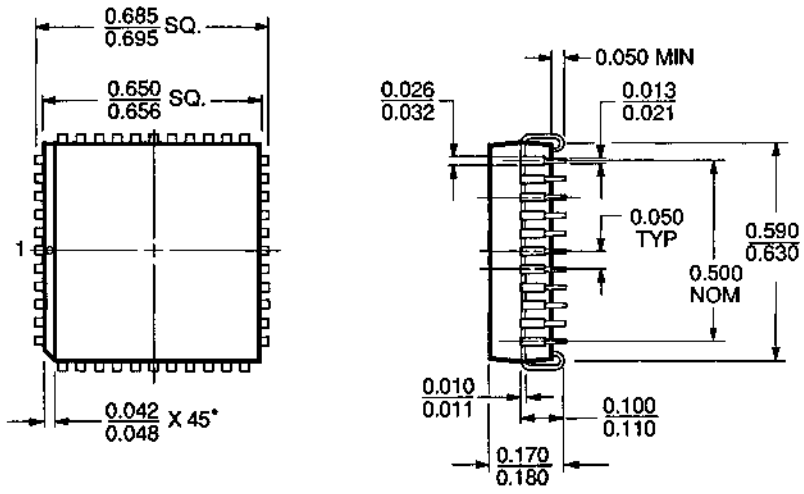
DRAWING H3 100 Pin Ceramic Quad Flatpack, Gullwing, Fine Pitch (Package Type H)



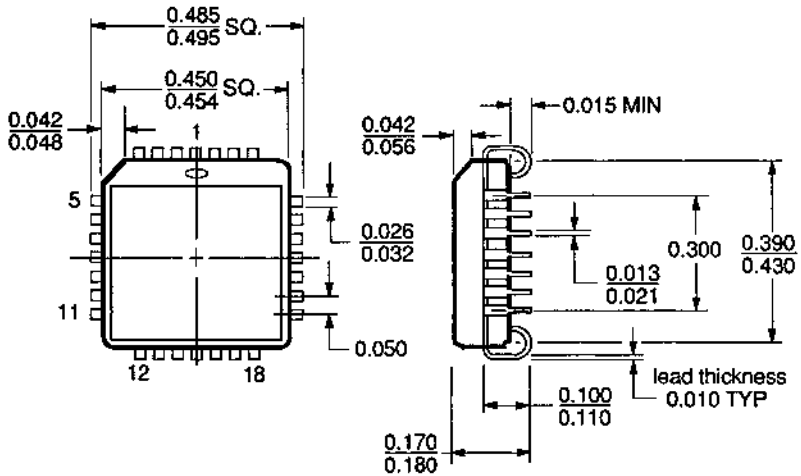
DRAWING J1 68 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



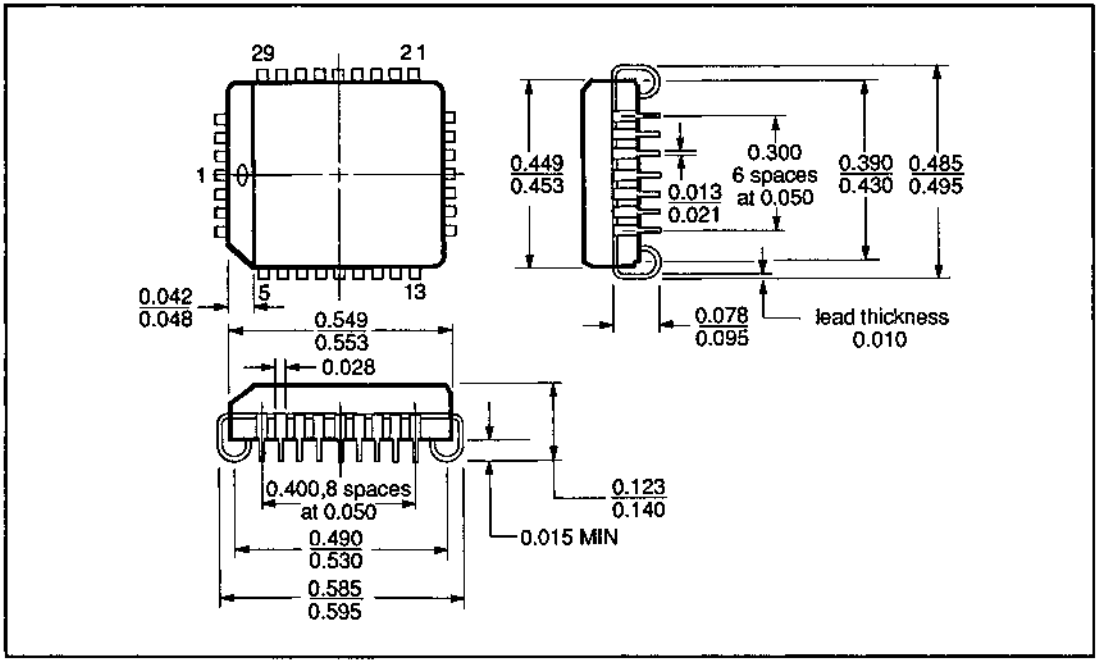
DRAWING J2 44 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



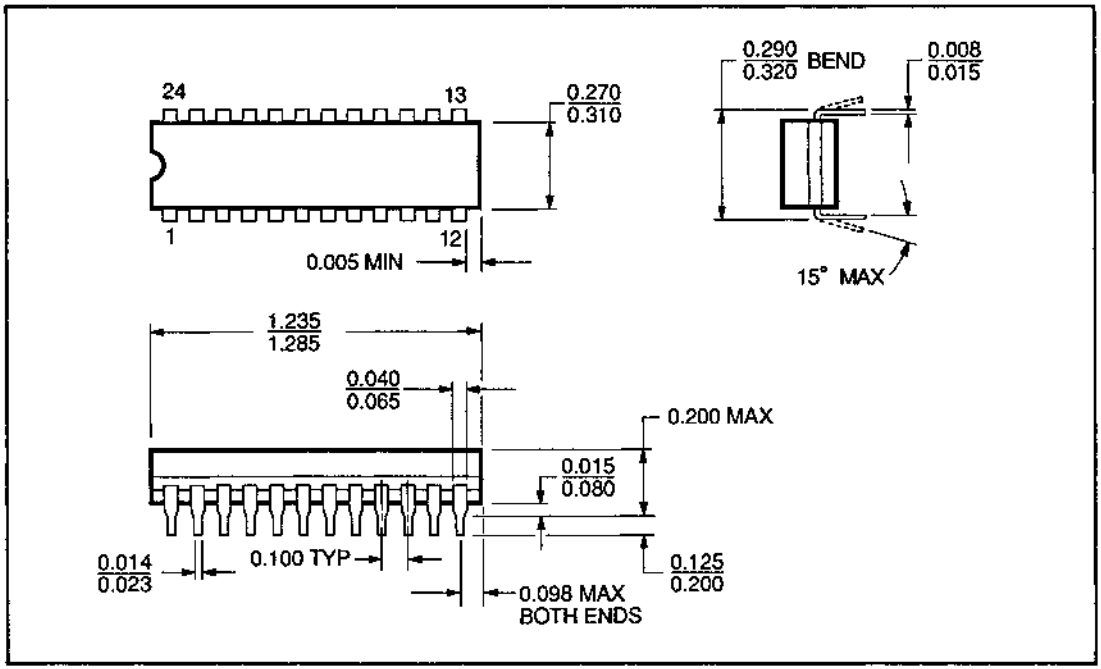
DRAWING J3 28 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



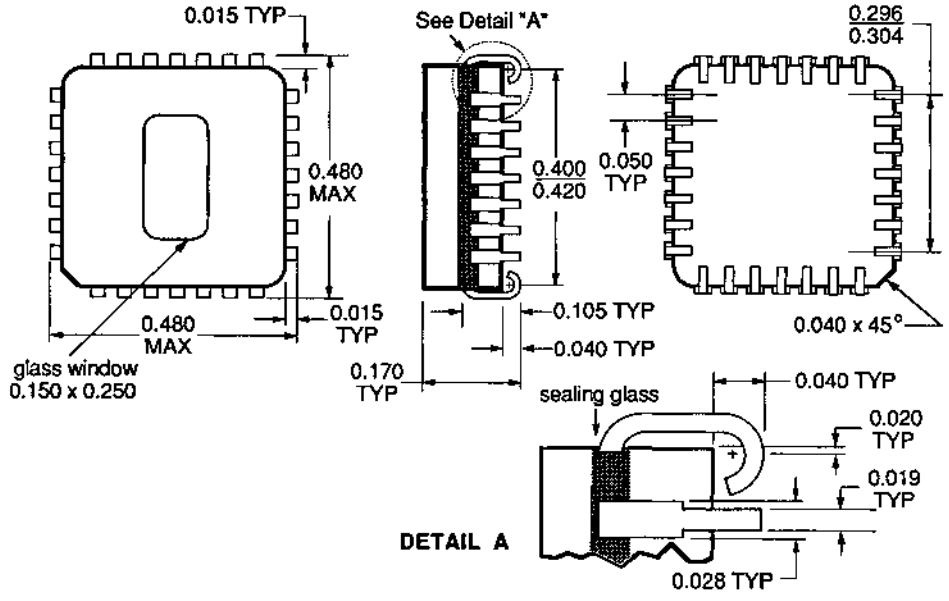
DRAWING J4 32 Pin Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



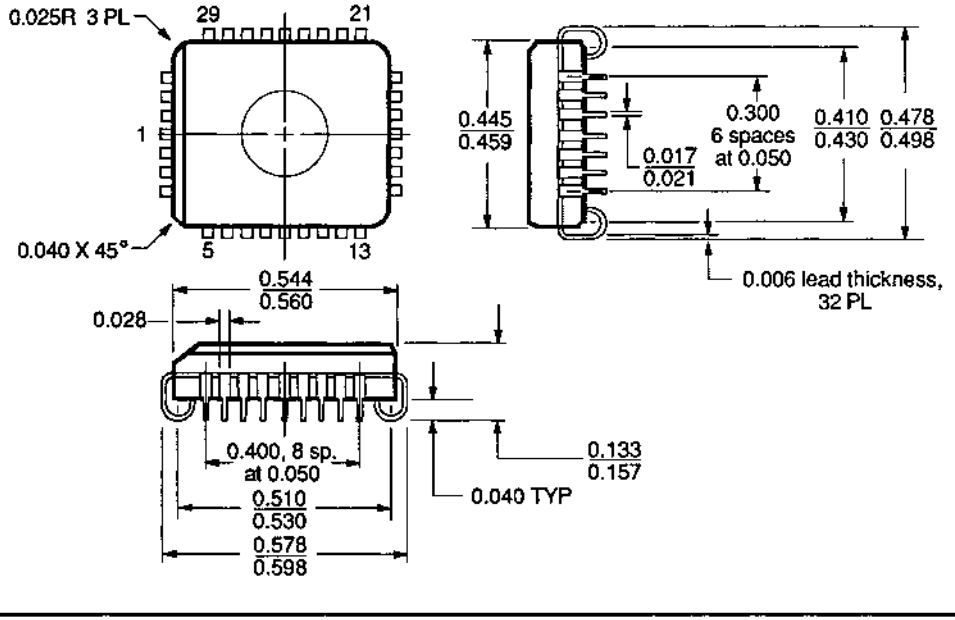
DRAWING K1 24 Pin CERDIP (Package Type K)



DRAWING L2 28 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

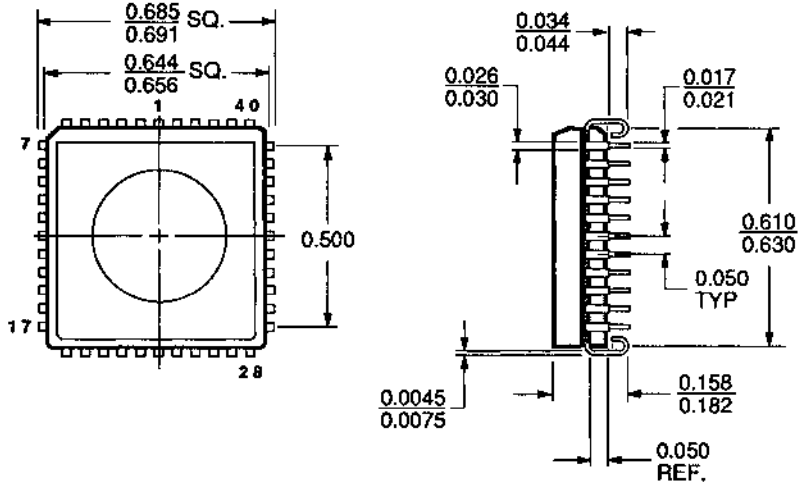


DRAWING L3 32 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)

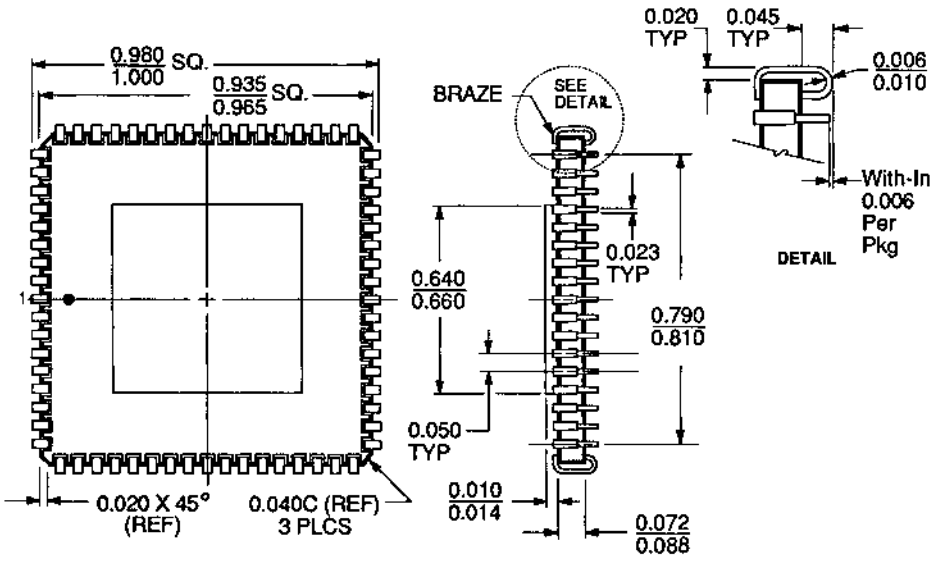


9

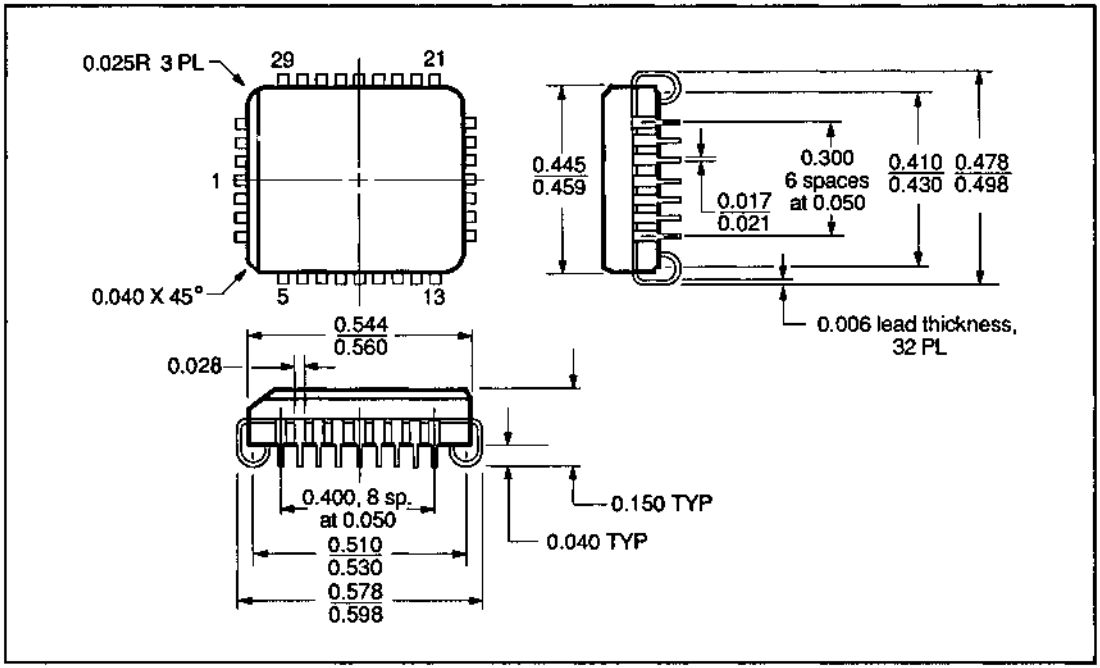
DRAWING L4 44 Pin Ceramic Leaded Chip Carrier (CLDCC) with Window (Package Type L)



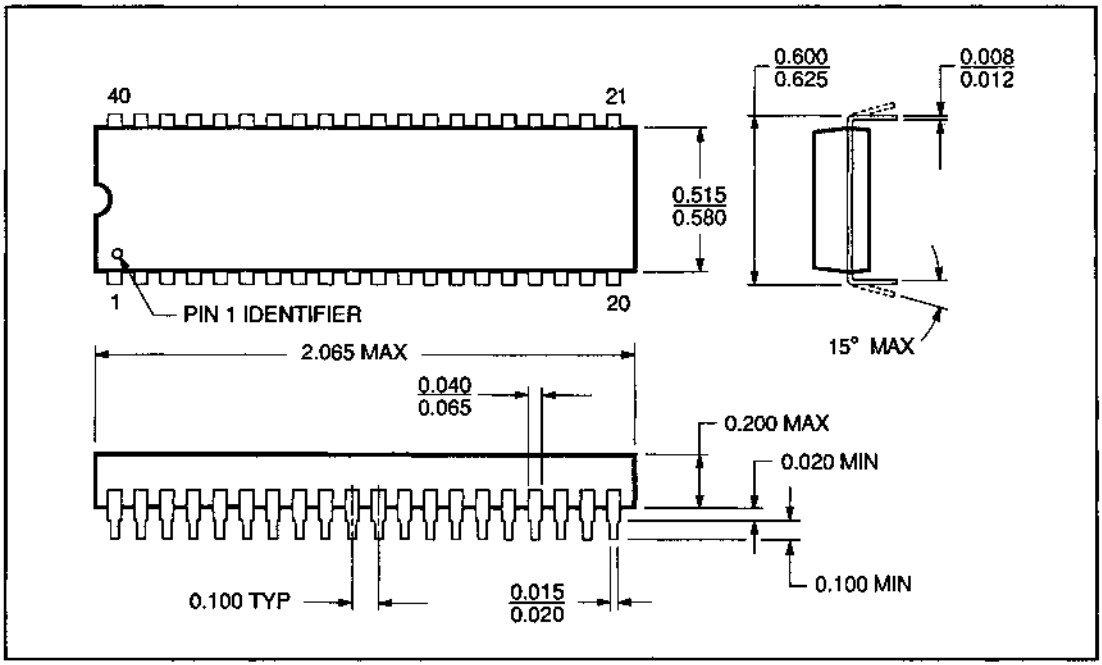
DRAWING N1 68 Pin Ceramic Leaded Chip Carrier (CLDCC) (Package Type N)



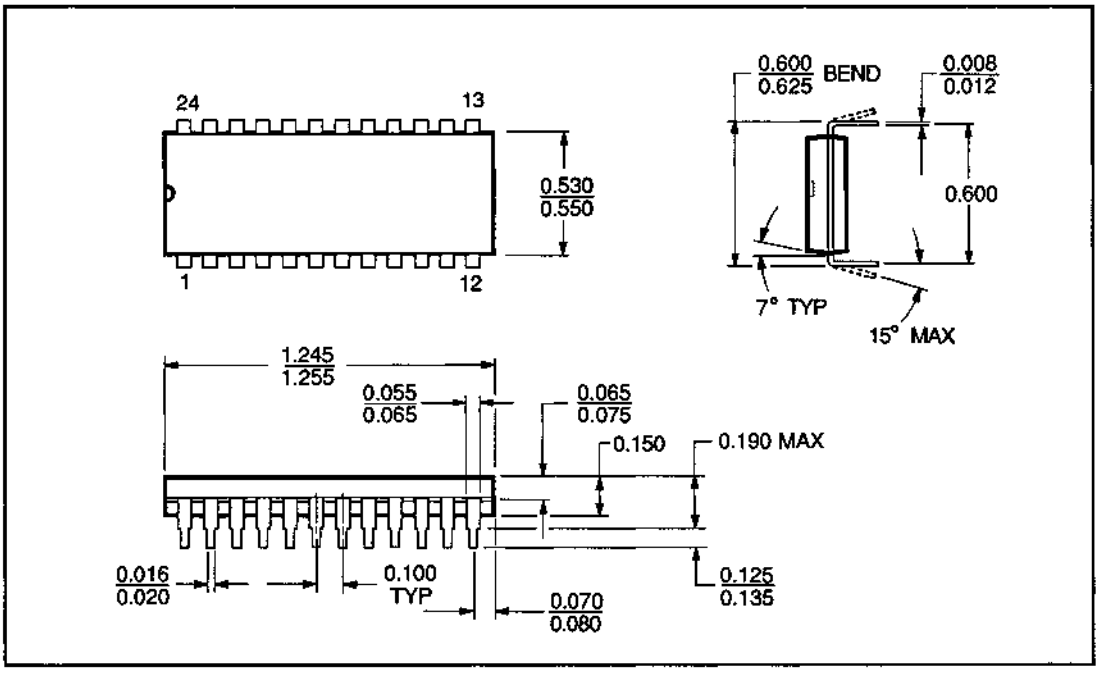
DRAWING N2 32 Pin Ceramic Leaded Chip Carrier (CLDCC) (Package Type N)



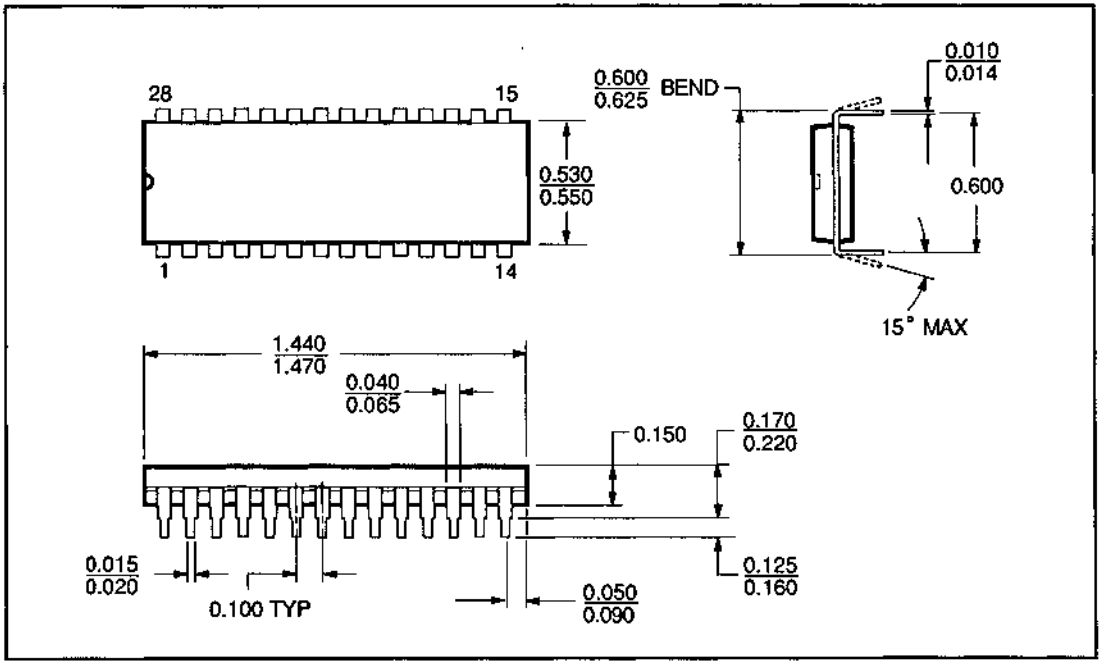
DRAWING P1 40 Pin Plastic DIP (Package Type P)



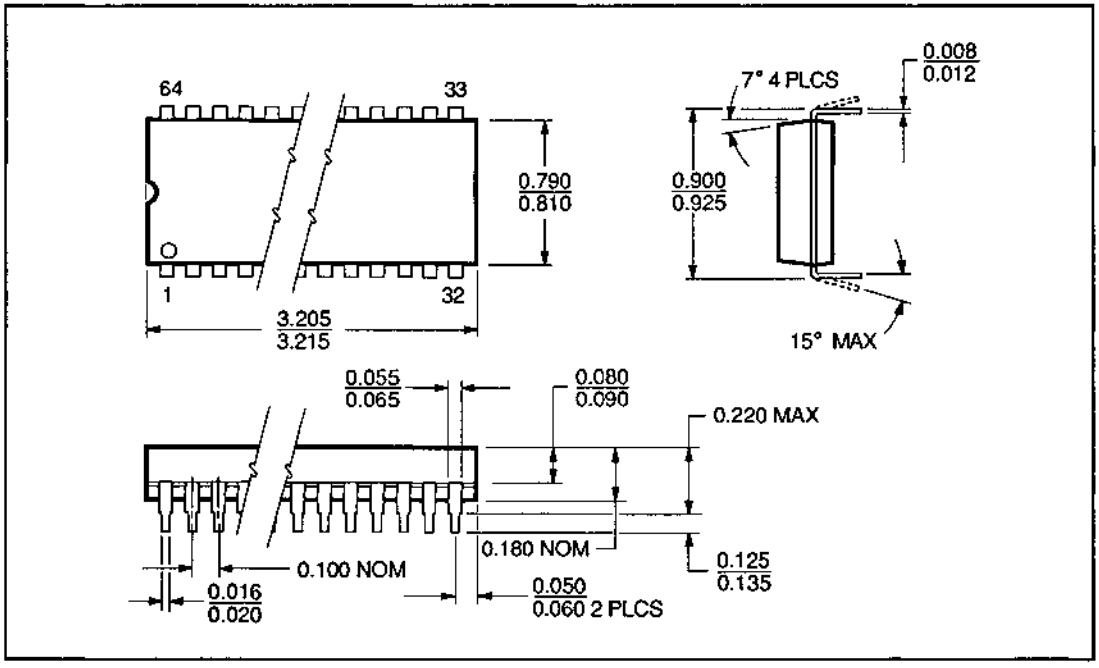
DRAWING P2 24 Pin Plastic DIP (Package Type P)



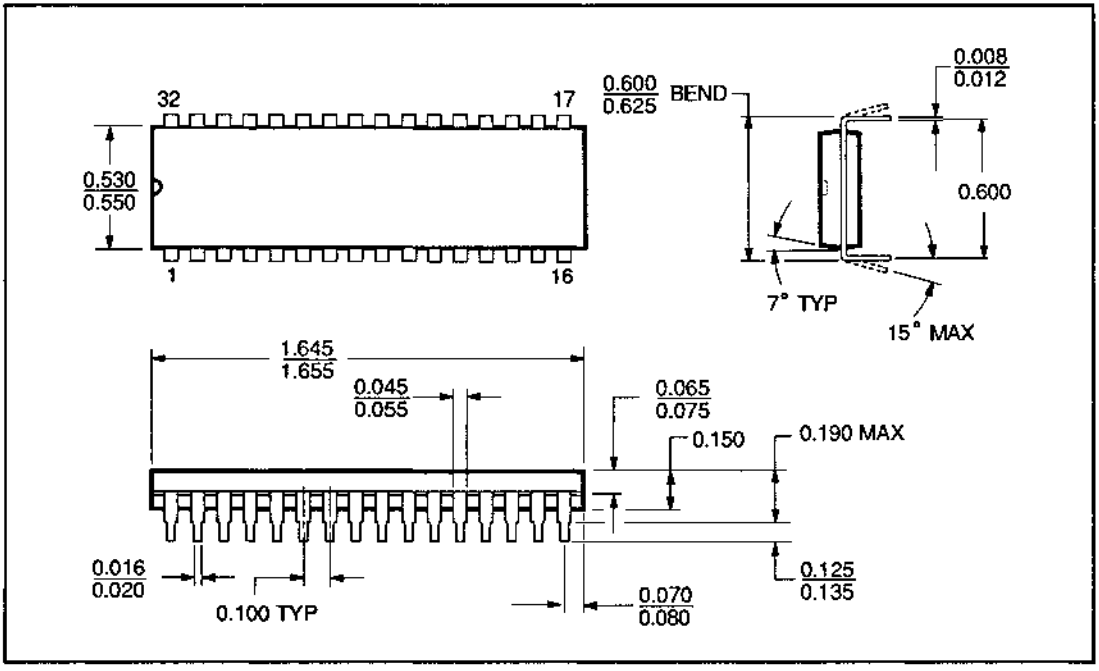
DRAWING P3 28 Pin Plastic DIP (Package Type P)



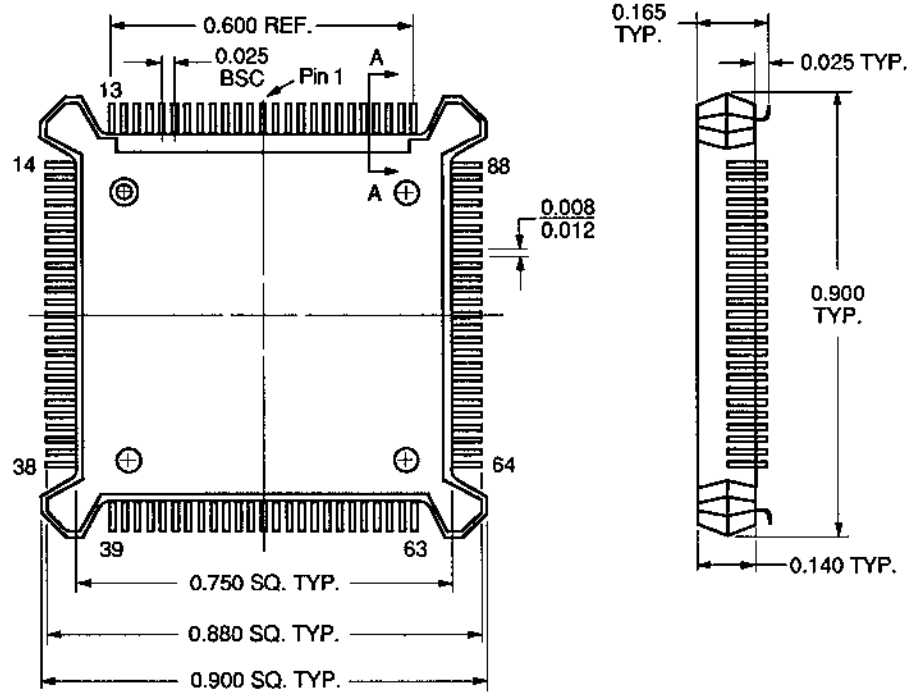
DRAWING P4 64 Pin Plastic DIP (Package Type P)



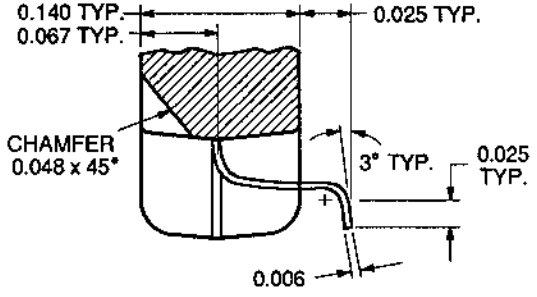
DRAWING P5 32 Pin Plastic DIP (Package Type P)



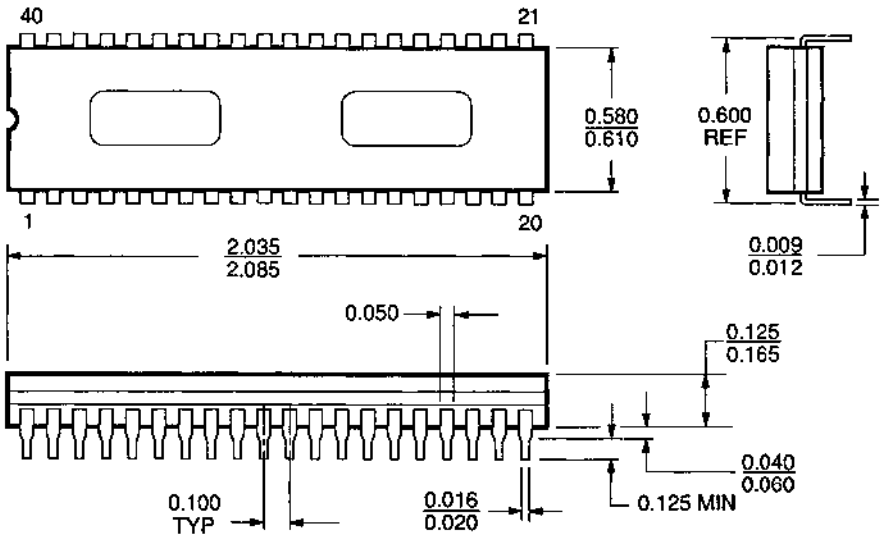
DRAWING Q1 100 Pin Plastic Quad Flatpack (PQFP), Gullwing, Fine Pitch (Package Type Q)



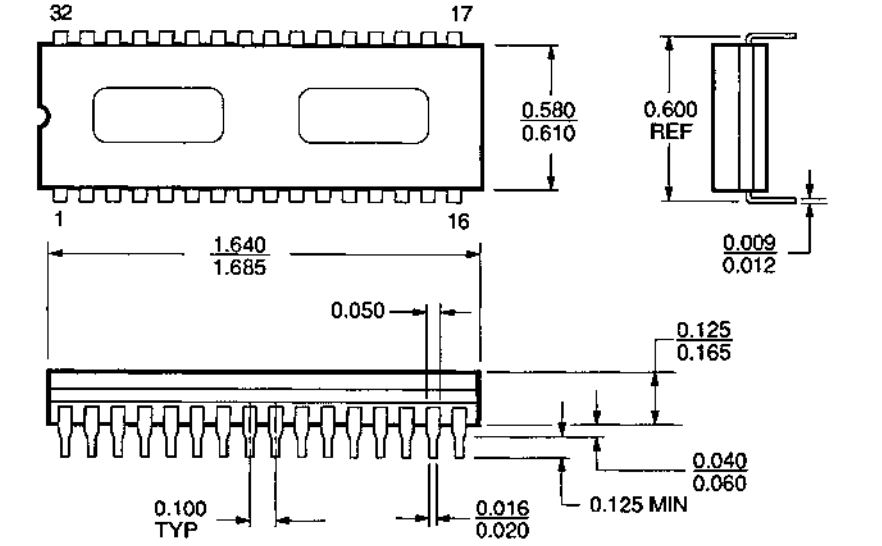
SECTION A–A



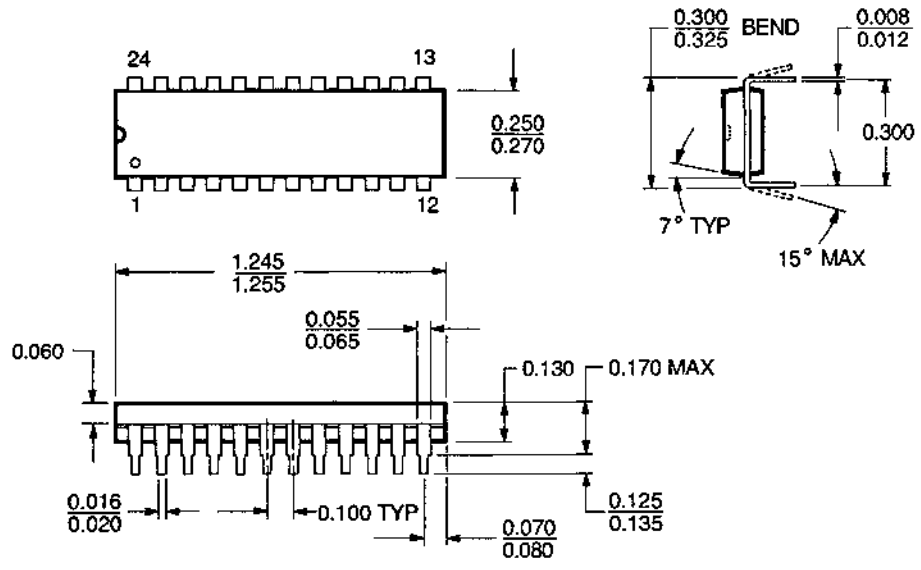
DRAWING R1 40 Pin Side Brazed Ceramic DIP (Package Type R)



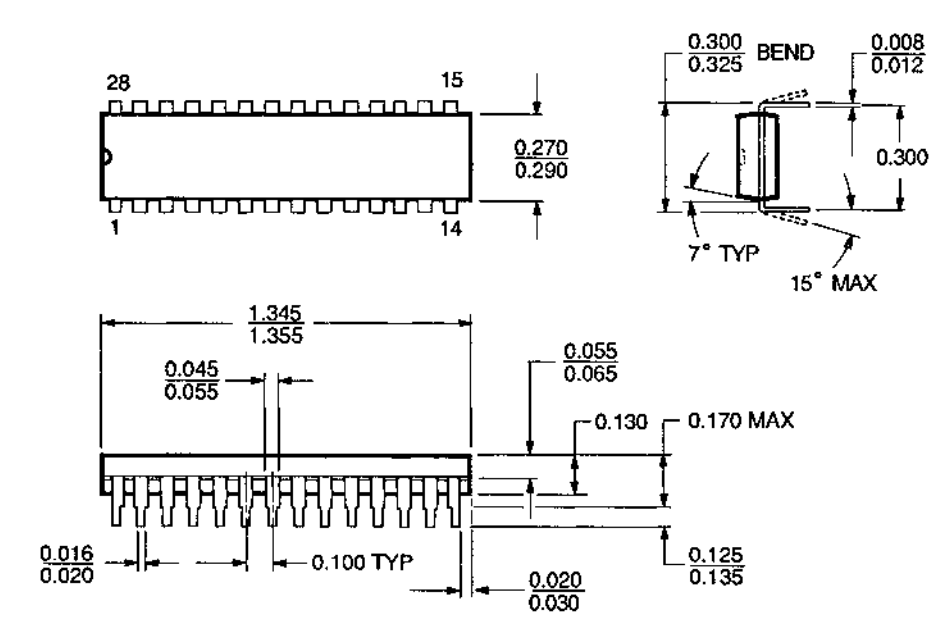
DRAWING R2 32 Pin Side Brazed Ceramic DIP (Package Type R)



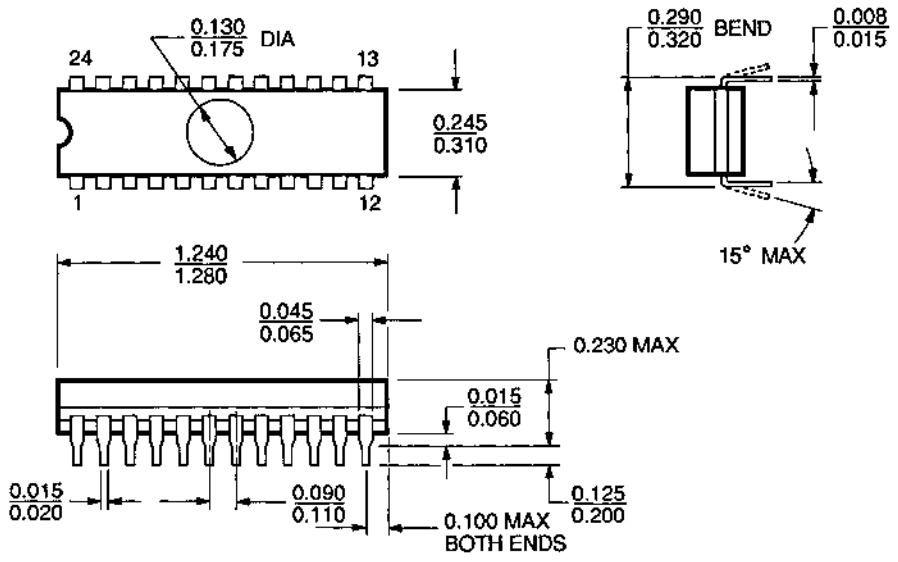
DRAWING S1 24 Pin Plastic .300 DIP (Package Type S)



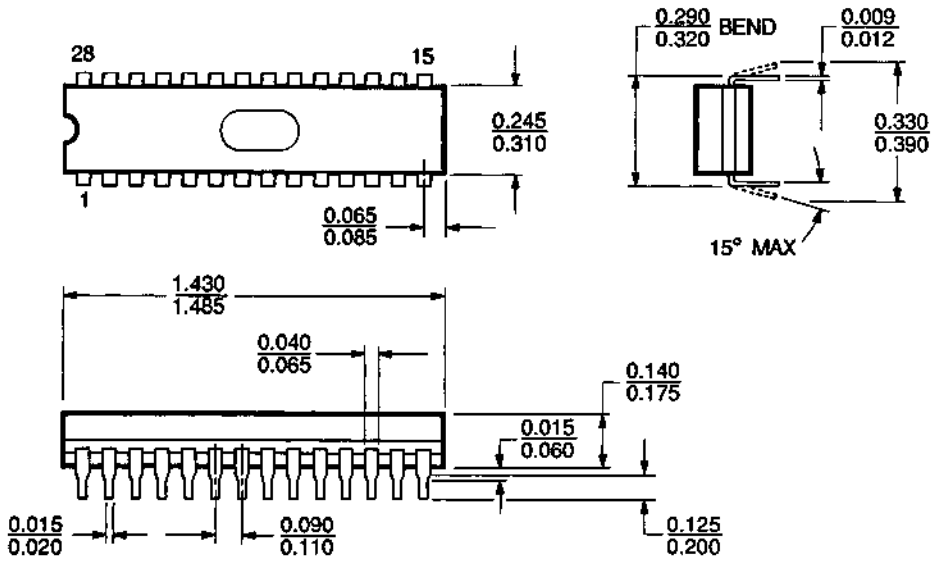
DRAWING S2 28 Pin Plastic .300 DIP (Package Type S)



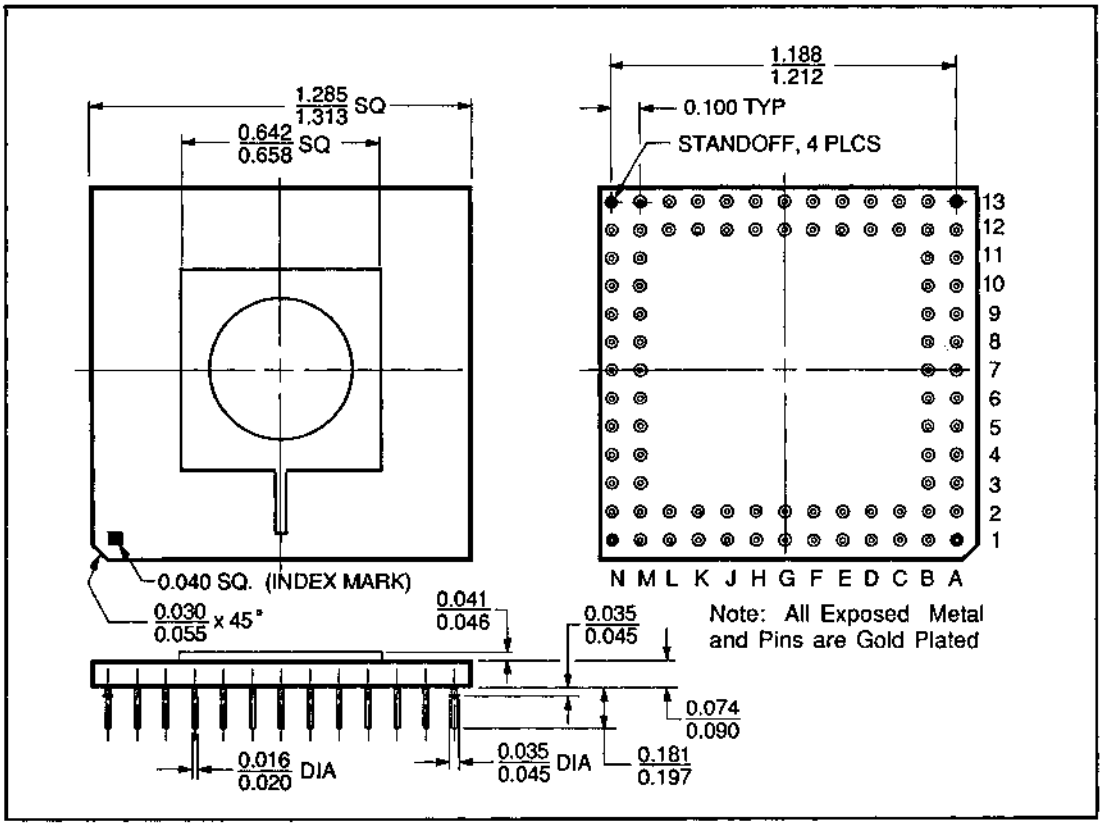
DRAWING T1 24 Pin CERDIP (Package Type T)



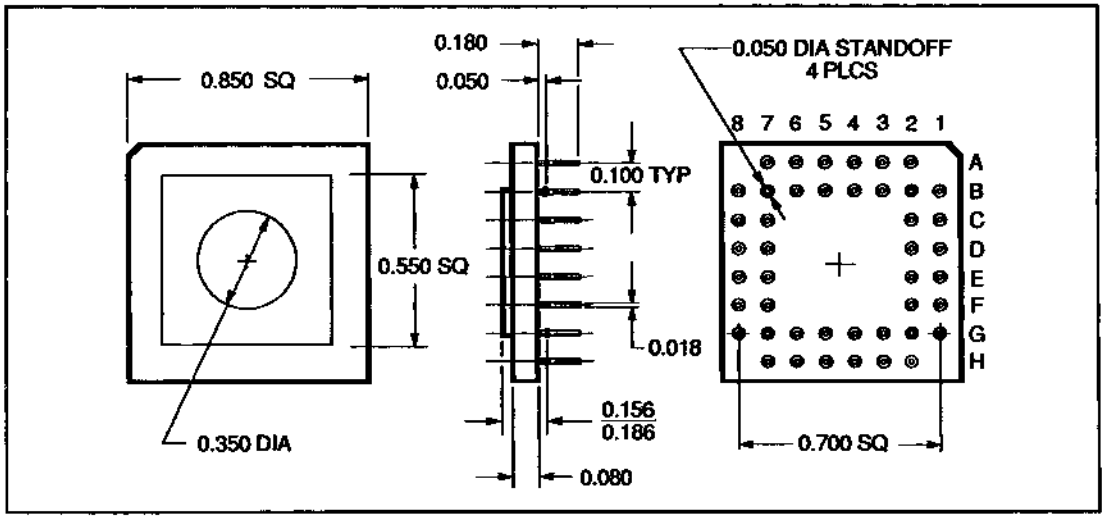
DRAWING T2 28 Pin CERDIP (Package Type T)



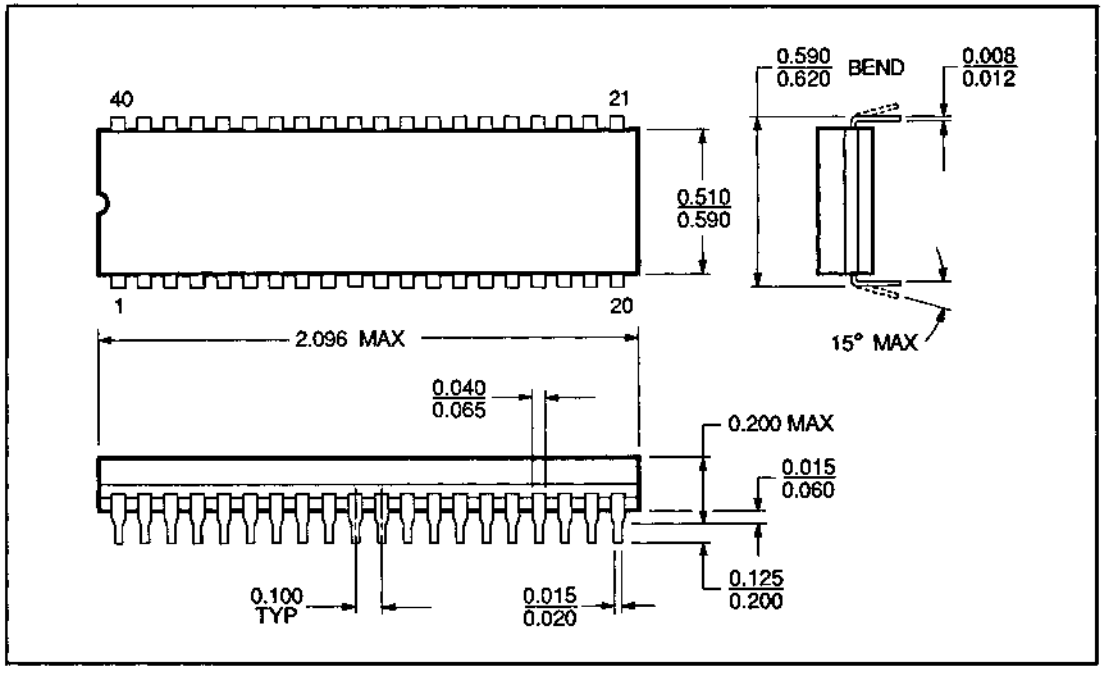
DRAWING X1 88 Pin Ceramic PGA (Package Type X)



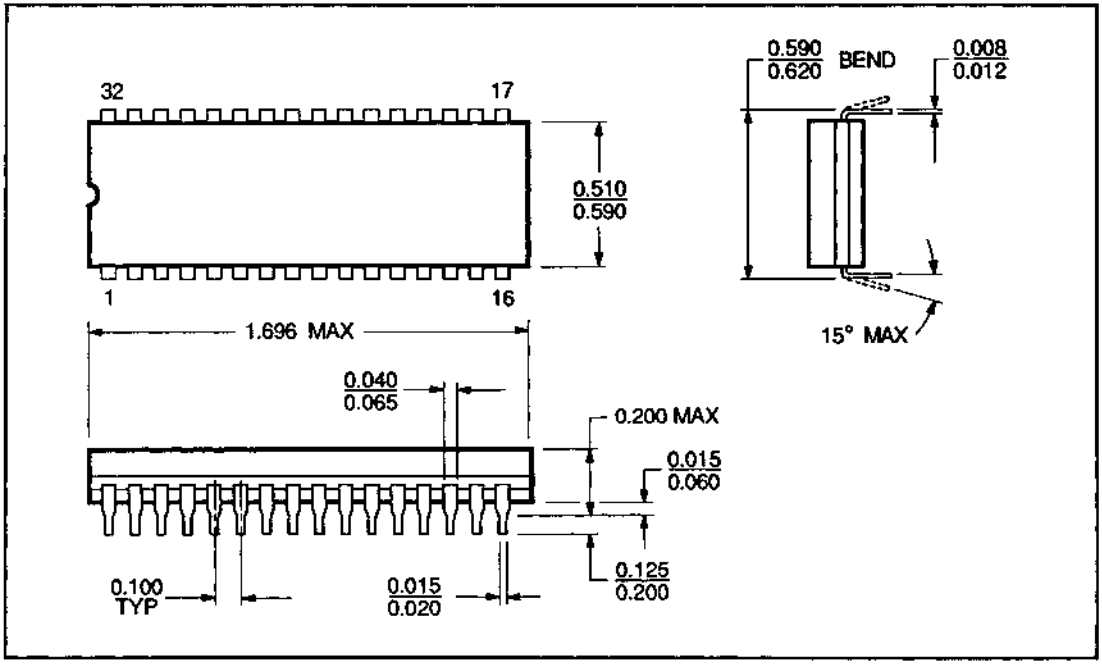
DRAWING X2 44 Pin Ceramic PGA (Package Type X)



DRAWING Y1 40 Pin CERDIP (Package Type Y)

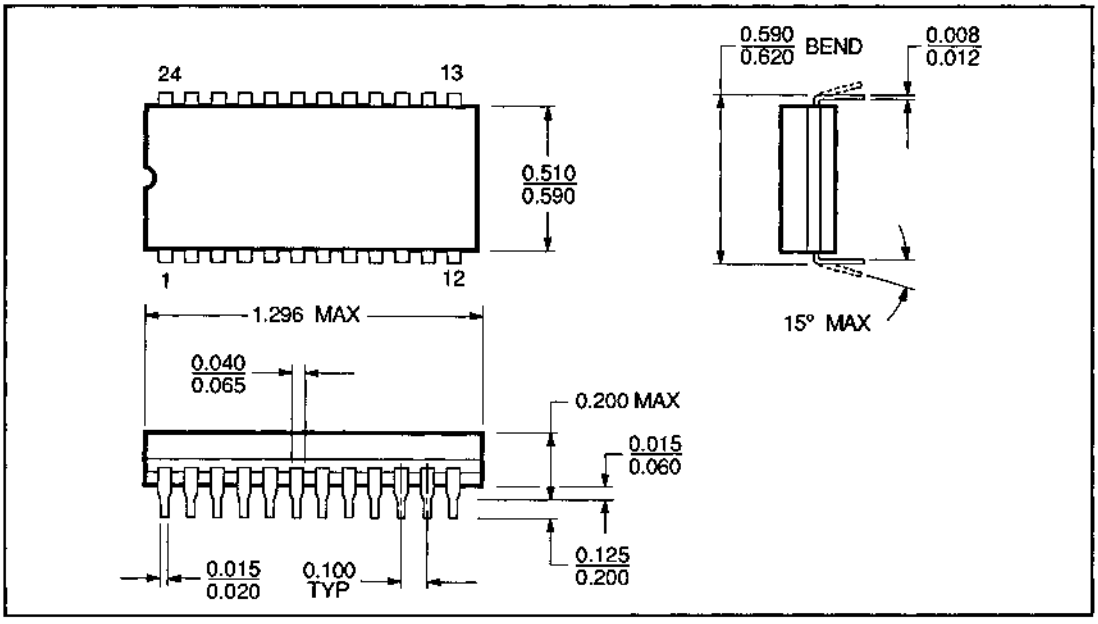


DRAWING Y2 32 Pin CERDIP (Package Type Y)

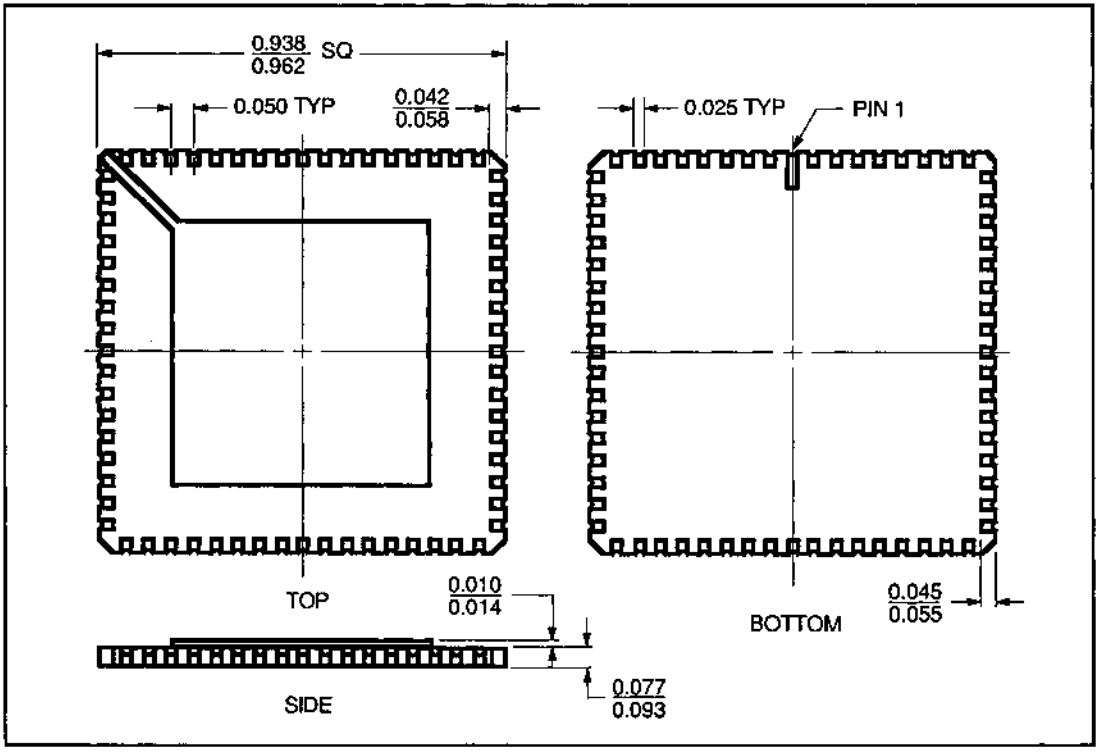


9

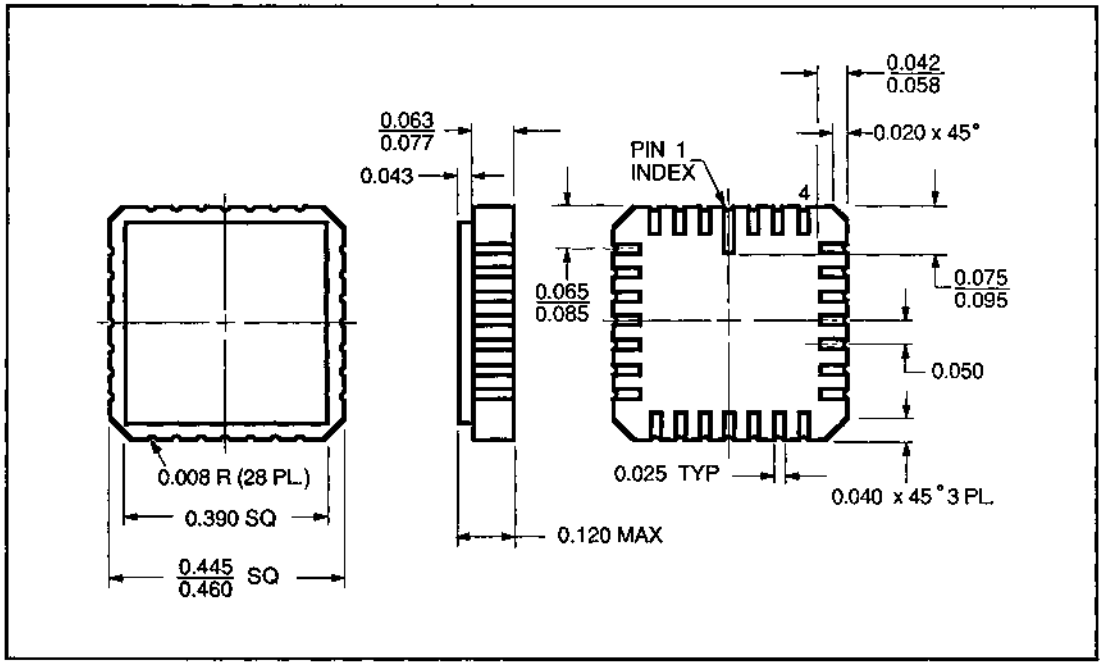
DRAWING Y3 24 Pin CERDIP (Package Type Y)



DRAWING Z1 68 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type Z)



DRAWING Z2 28 Pad Ceramic Leadless Chip Carrier (CLLCC) (Package Type Z)



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Patents Pending Rev. 1.3

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