

SILICON STACKED GATE CMOS

65,536 WORD x 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

Description

The TC57512AD is a 65,536 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. It operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time. The standby mode is activated by applying a TTL-high level signal to the \overline{CE} input. Advanced CMOS technology reduces the maximum active current to 30mA/6.7MHz and the standby current to 100 μ A. Programming is achieved by using a high speed programming mode. The TC57512AD is fabricated using CMOS technology and N-channel silicon double layer gate MOS technology.

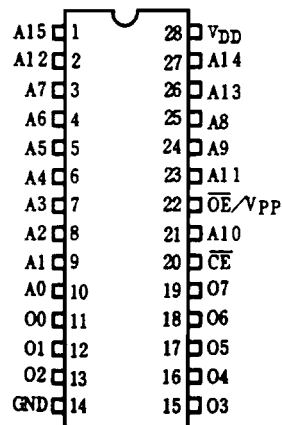
Features

- Peripheral circuit : CMOS
Memory cell : NMOS
- Fast access time : TC57512AD-15 150ns
TC57512AD-20 200ns
- Low power dissipation
 - Active : 30mA/6.7MHz
 - Standby : 100 μ A
- Single 5V power supply
- Fully static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Standard 28-pin DIP cerdip package : WDIP28-G-600

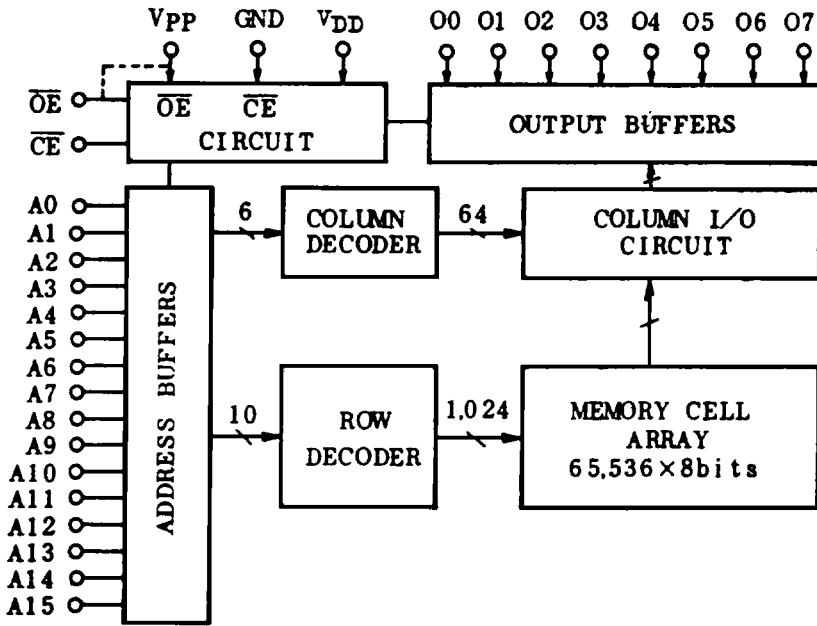
Pin Names

A0 ~ A15	Address Inputs
O0 ~ O7	Outputs (Inputs)
\overline{CE}	Chip Enable Input
\overline{OE}/V_{PP}	Output Enable Input/ Program Supply Voltage
V_{DD}	Power Supply Voltage (+5V)
GND	Ground

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	CE (20)	OE / V _{PP} (22)	V _{DD} (28)	00 - 07 (11 - 13, 15 - 19)	POWER
Read		L	L	5V	Data Out	Active
Output Deselect		*	H		High Impedance	
Standby		H	*		High Impedance	Standby
Program		L	V _{PP}	6V ¹⁾	Data In	Active
Program Inhibit		H	V _{PP}		High Impedance	
Program Verify		L	L	6.25V ²⁾	Data Out	

* H or L 1) High Speed Programming Mode I
 2) High Speed Programming Mode II

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.6 ~ 7.0	V
V _{PP}	Program Supply Voltage	-0.6 ~ 14.0	
V _{IN}	Input Voltage	-0.6 ~ 7.0	
V _{I/O}	Input/Output Voltage	-0.6 ~ V _{DD} + 0.5	
P _D	Power Dissipation	1.5	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 125	°C
T _{OPR}	Operating Temperature	-40 ~ 85	

Read Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	–	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	–	0.8	
V _{DD}	Power Supply Voltage	4.75	5.0	5.25	
V _{PP}	Program Supply Voltage	0	–	V _{DD} + 0.6	

DC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	–	–	±10	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0.4 ~ V _{DD}	–	–	±10	
I _{DDO1}	Operating Current	$\overline{CE} = 0V$ $I_{OUT} = 0mA$	f = 6.7MHz	–	–	30
I _{DDO2}						
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	–	–	1	mA
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2V$	–	–	100	μA
V _{OH}	Output High Voltage	I _{OH} = -400μA	2.4	–	–	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	–	–	0.4	
I _{PP1}	V _{PP} Current	V _{PP} = 0 ~ V _{DD} + 0.6	–	–	±10	μA

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±5%)

SYMBOL	PARAMETER	TEST CONDITION	TC57512AD-15		TC57512AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t _{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	–	150	–	200	ns
t _{CE}	\overline{CE} to Output Valid	$\overline{OE} = V_{IL}$	–	150	–	200	
t _{OE}	\overline{OE} to Output Valid	$\overline{CE} = V_{IL}$	–	70	–	70	
t _{DF1}	\overline{CE} to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	0	60	
t _{DF2}	\overline{OE} to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	0	60	
t _{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	–	0	–	

AC Test Conditions

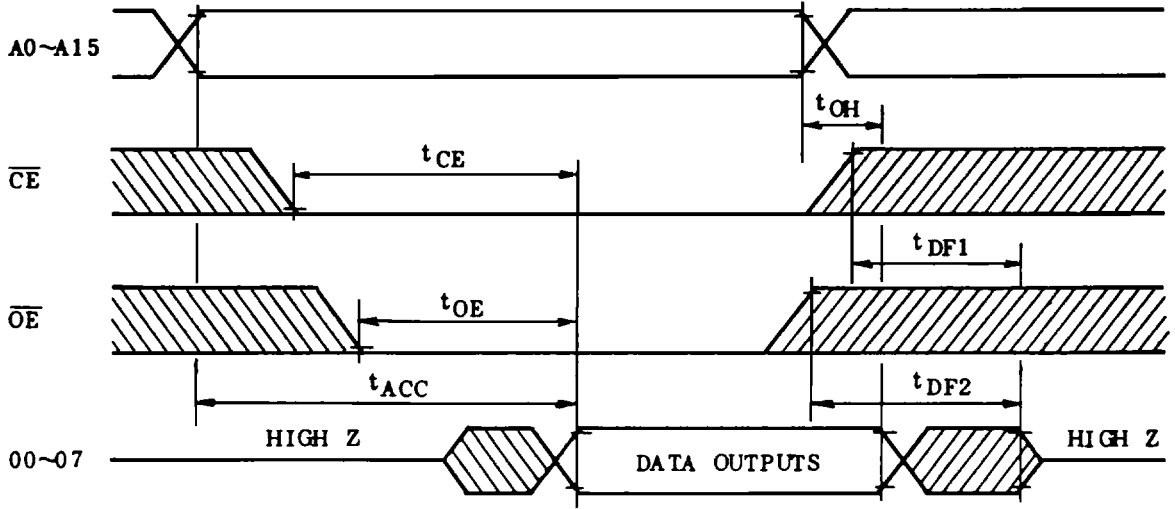
Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C _L = 100 pF

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C _{IN1}	Input Capacitance	V _{IN} = 0V	–	4	6	pF
C _{IN2}	\overline{OE}/V_{PP} Input Capacitance	V _{IN} = 0V	–	50	60	
C _{OUT}	Output Capacitance	V _{OUT} = 0V	–	8	12	

*This parameter is periodically sampled and is not 100% tested.

Timing Waveforms (Read)



High Speed Programming Mode I

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 1.0$	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	
V_{DD}	Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	Program Supply Voltage	12.0	12.5	13.0	

DC Characteristics ($T_a = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	± 10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\text{mA}$	–	–	0.4	
I_{DD}	V_{DD} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0V$	–	–	50	

AC Programming Characteristics ($T_a = 25 \pm 5^\circ\text{C}$, $V_{DD} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	
t_{OES}	$\overline{\text{OE}}/V_{PP}$ Setup Time	–	2	–	–	
t_{OEH}	$\overline{\text{OE}}/V_{PP}$ Hold Time	–	2	–	–	
t_{PRT}	$\overline{\text{OE}}/V_{PP}$ Pulse Rise Time	–	50	–	–	ns
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	
t_{VR}	$\overline{\text{OE}}/V_{PP}$ Recovery Time	–	2	–	–	
t_{VDS}	V_{DD} Setup Time	–	2	–	–	
t_{PW}	Initial Program Pulse Width	$\overline{\text{CE}} = V_{IL}$, $\overline{\text{OE}}/V_{PP} = V_{PP}$	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	
t_{DV}	Data Valid from $\overline{\text{CE}}$	$\overline{\text{OE}}/V_{PP} = V_{IL}$	–	–	1	μs
t_{DF}	$\overline{\text{CE}}$ to Output in High-Z	$\overline{\text{OE}}/V_{PP} = V_{IL}$	–	–	130	ns

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and $C_L = 100\text{ pF}$

High Speed Programming Mode II

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{IH}	Input High Voltage	2.2	–	V _{DD} + 1.0	V
V _{IL}	Input Low Voltage	-0.3	–	0.8	
V _{DD}	Power Supply Voltage	6.0	6.25	6.5	
V _{PP}	Program Supply Voltage	12.5	12.75	13.0	

DC Characteristics (T_a = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	–	–	±10	μA
V _{OH}	Output High Voltage	I _{OH} = -400μA	2.4	–	–	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA	–	–	0.4	
I _{DD}	V _{DD} Supply Current	–	–	–	30	mA
I _{PP2}	V _{PP} Supply Current	V _{PP} = 13.0V	–	–	50	

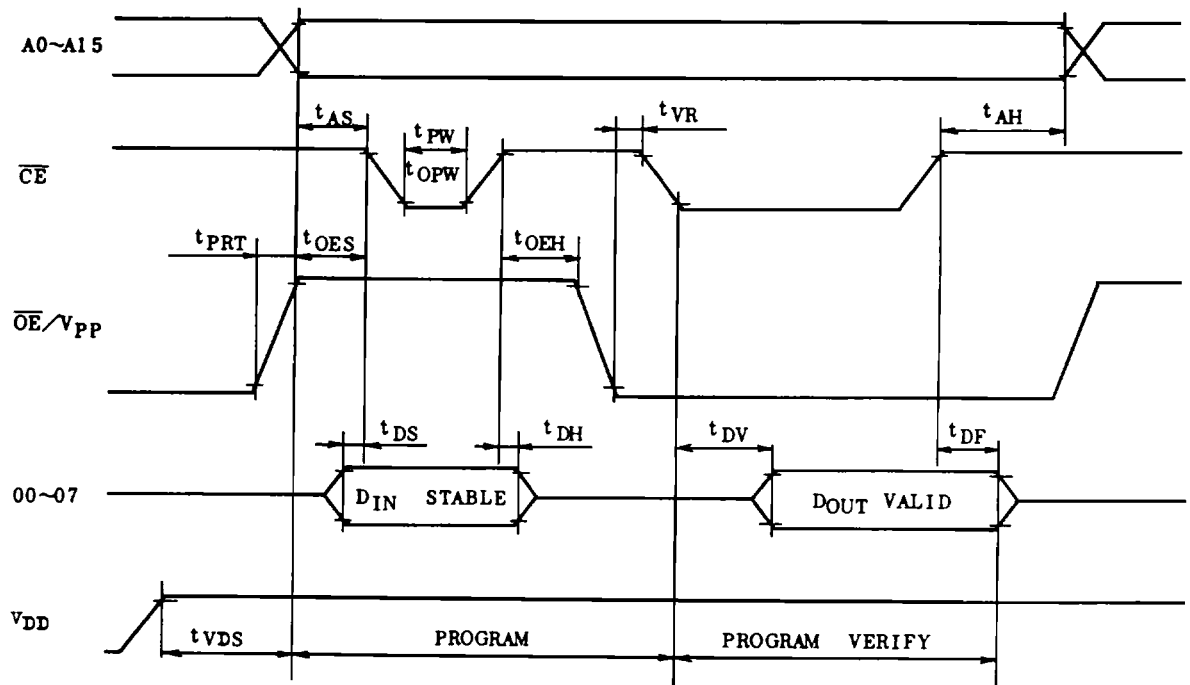
AC Programming Characteristics (T_a = 25±5°C, V_{DD} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t _{AS}	Address Setup Time	–	2	–	–	μs
t _{AH}	Address Hold Time	–	2	–	–	
t _{OES}	\overline{OE}/V_{PP} Setup Time	–	2	–	–	
t _{OEH}	\overline{OE}/V_{PP} Hold Time	–	2	–	–	
t _{PRT}	\overline{OE}/V_{PP} Pulse Rise Time	–	50	–	–	ns
t _{DS}	Data Setup Time	–	2	–	–	μs
t _{DH}	Data Hold Time	–	2	–	–	
t _{VR}	\overline{OE}/V_{PP} Recovery Time	–	2	–	–	
t _{VDS}	V _{DD} Setup Time	–	2	–	–	
t _{PW}	Program Pulse Width	$\overline{CE} = V_{IL}, \overline{OE}/V_{PP} = V_{PP}$	0.095	0.1	0.105	ms
t _{DV}	Data Valid from \overline{CE}	$\overline{OE}/V_{PP} = V_{IL}$	–	–	1	μs
t _{DF}	\overline{CE} to Output in High-Z	$\overline{OE}/V_{PP} = V_{IL}$	–	–	130	ns

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C _L = 100 pF

Timing Waveforms (Program)

High Speed Program Mode I ($V_{DD} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.5V$)High Speed Program Mode II ($V_{DD} = 6.25V \pm 0.25V$, $V_{PP} = 12.75V \pm 0.25V$)

Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP} .
2. Removing the device from a programming socket and replacing the device in the socket while $V_{PP} = 12.5V$ (12.75V) may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted to be up to 14V for programming. Voltages over 14V should not be applied to the V_{PP} terminal. When the programming voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Erasure Characteristics

Erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (ultraviolet light intensity [W/cm^2] x exposure time [sec.]) necessary for erasure should be a minimum of 15 [$W \cdot sec/cm^2$].

When the Toshiba sterilizing lamp (GL-15) is used and the device is exposed at a distance of 1 cm from the lamp surface, erasure will be achieved within 60 minutes. Using commercial lamps whose ultraviolet light intensity is 12000 [$\mu W/cm^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [$\mu W/cm^2$] x (20 x 60) [sec] \cong 15 [$W \cdot sec/cm^2$].)

Erasure begins to occur when exposed to light with a wavelength shorter than 4000Å. Sunlight and fluorescent lights have 3000 ~ 4000Å wavelength components. Therefore, when used under these lighting conditions for extended periods of time, opaque seals should be used (Toshiba EPROM Protect Seal AC901).

Operation Information

The TC57512AD's six operating modes are listed in the following table.

Mode selection is achieved by applying TTL level signals to appropriate inputs.

MODE	PIN NAMES (NUMBER)	CE (20)	OE/V _{PP} (22)	V _{DD} (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read Operation (Ta = -40 ~ 85°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	
	Standby	H	*		High Impedance	Standby
Program Operation (Ta = 25±5°C)	Program	L	V _{PP}	6V ¹⁾	Data In	Active
	Program Inhibit	H	V _{PP}		High Impedance	
	Program Verify	L	L	6.25V ²⁾	Data Output	

Notes: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}.
 1) High Speed Programming Mode I, V_{PP} = 12.5
 2) High Speed Programming Mode II, V_{PP} = 12.75

Read Mode

The TC57512AD has two control inputs. The chip enable (\overline{CE}) input controls the operating power and should be used for device selection while the output enable (\overline{OE}) input controls the output buffers. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, once the address has stabilized, output data will be valid after the address access time has elapsed.

The \overline{CE} to output valid time (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and that the address has been stable for at least t_{ACC} , then output data will be valid after t_{OE} from the falling edge of \overline{OE} .

Output Deselect Mode

If $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state.

Therefore, two or more devices can be connected together on a common bus if the output of only one device is enabled. When \overline{CE} is used for device selection, all deselected devices are in the low power standby mode.

Standby Mode

The TC57512AD has a low power standby mode controlled by the \overline{CE} signal.

By applying a MOS high level voltage (V_{DD}) to the \overline{CE} input, the TC57512AD is placed in the standby mode which reduces the operating current to 100μA and puts the outputs in a high impedance state, independent of the \overline{OE} input.

Program Mode

When the TC57512AD is initially received by customers, all bits of the device are in the "1" state, which is the erased state.

Therefore, the object of the program operation is to introduce "0" data into the desired bit locations.

The TC57512AD is in the programming mode when $\overline{OE}/V_{PP} = 12.5V(12.75V)$, and $\overline{CE} = V_{IL}$.

The TC57512AD can be programmed at any address location at any time - either individually, sequentially, or at random.

Program Verify Mode

The verify mode is used to check that the desired data has been correctly programmed. The verify mode is activated when $\overline{OE}/V_{PP} = V_{IL}$ and $\overline{CE} = V_{IL}$.

Program Inhibit Mode

When the programming voltage (+12.5V or +12.75V) is applied to the V_{PP} terminal, a high level \overline{CE} input inhibits the TC57512AD from being programmed.

The programming of two or more TC57512ADs in parallel with different data is easily accomplished. All inputs except for \overline{CE} may be commonly connected, then a TTL low level program pulse is applied to the \overline{CE} of the desired device only while a TTL high level signal is applied to the \overline{CE} of the other devices.

High Speed Programming Mode I

The device is set up in high speed programming mode I when the programming voltage (+12.5V) is applied to the \overline{OE}/V_{PP} terminal with $V_{DD} = 6V$.

Programming is achieved by applying a single 1ms TTL low level pulse to the \overline{CE} input after addresses and data are stable. Then the programmed data is verified by using the program verify mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

After correctly programming the selected address, an additional program pulse with a width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with $V_{DD} = 5V$.

High Speed Programming Mode II

Programming time can be greatly decreased by using high speed programming mode II. The device is set up in high speed programming mode II when the programming voltage (+12.75V) is applied to the \overline{OE}/V_{PP} terminal with $V_{DD} = 6.25V$.

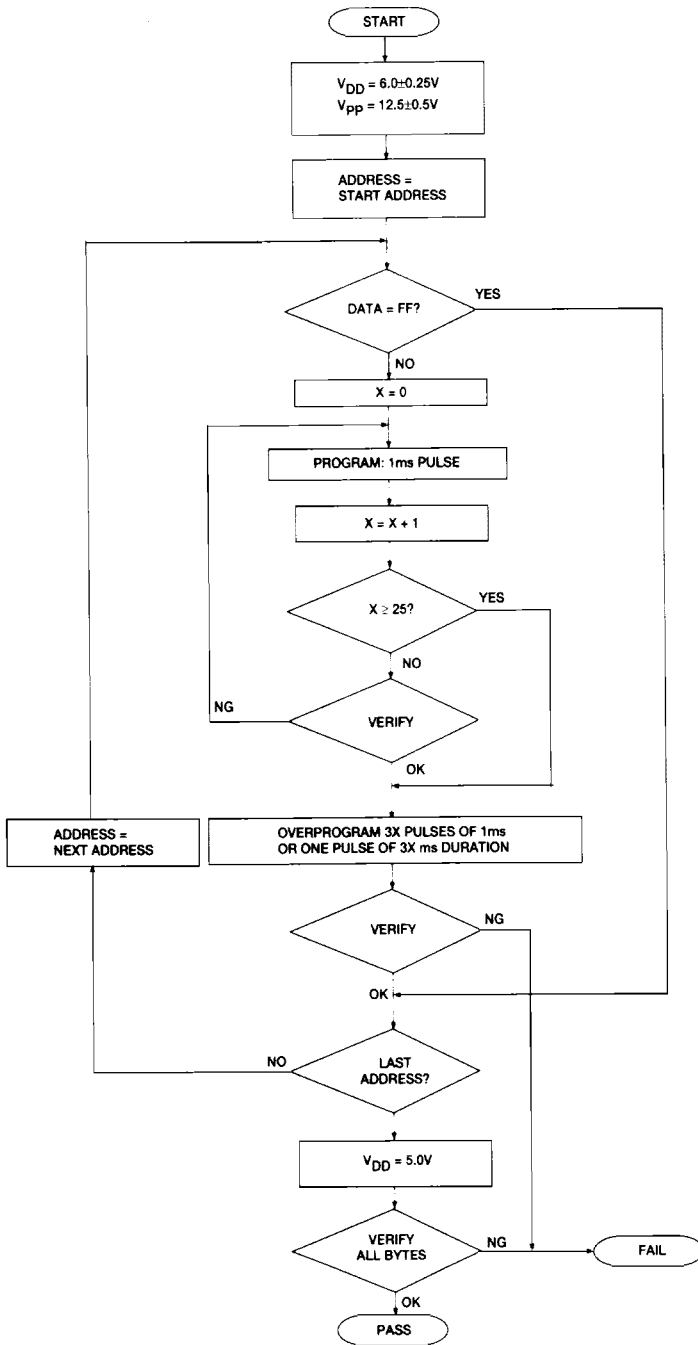
Programming is achieved by applying a single 0.1ms TTL low level pulse to the \overline{CE} input after addresses and data are stable. Then the programmed data is verified by using the program verify mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with $V_{DD} = 5V$.

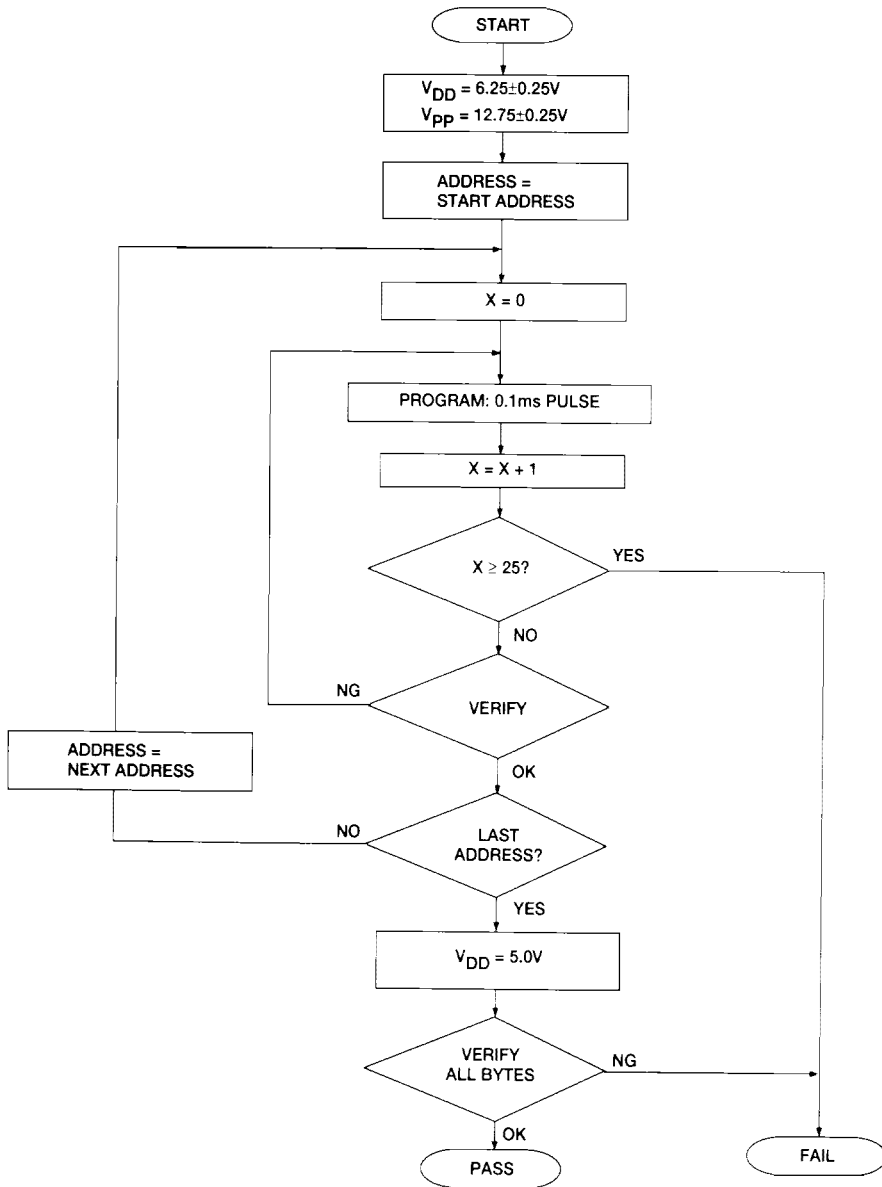
High Speed Programming Mode I

Flow Chart



High Speed Programming Mode II

Flow Chart



Electric Signature Mode

The electric signature mode allows one to read out a code from the TC57512AD which identifies its manufacturer and device type.

The programming equipment may read out the manufacturer code and device code from the TC57512AD by using this mode before programming and automatically set the programming voltage (V_{PP}) and algorithm.

The electric signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} during a read operation. Data output under these conditions is the manufacturer code. The device code is output when address A0 is set to V_{IH} . These two codes possess an odd parity with the parity bit being the MSB (O7). The following table shows the electric signature of the TC57512AD.

SIGNATURE	PINS	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacturer Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code		V_{IH}	1	0	0	0	0	1	0	1	85

Notes: A9 = 12V±0.5V

A1 ~ A8, A10 ~ A15, \overline{CE} , \overline{OE} = V_{L}