TOSHIBA MOS MEMORY PRODUCT

32,768 WORD X 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABEL READ ONLY MEMORY

TC57256D-20
TC57256D-25

SILICON STACKED GATE MOS

DESCRIPTION

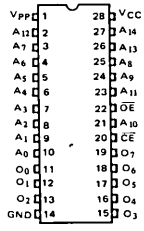
The TC57256D is a 32,768 word ×8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256D's access time is 200ns, and the TC57256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30 mA/5MHz and standby current to 100μA.

For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V. The programming of the TC57256D is accomplished within one and a half minutes (typ.) TC57256D is fabricated using CMOS technology and N-channel silicon double layer gate MOS technology.

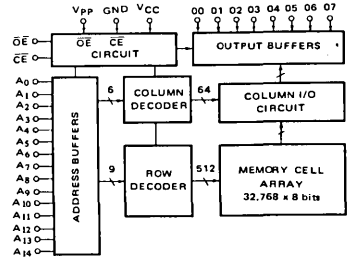
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  30mA/5MHZ (active)
  100μA (standby)
- Fast access time TC57256D-20 200 ns
  TC57256D-25 250 ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROMS TC53257P, TMM23256P and EPROM i27256
- Standard 28 pin DIP cerdip Package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H		5V	High Impedance	
Standby	H	*		5V	High Impedance	Standby
Program	L	H	21V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	L	L			Data Out	

* * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	−0.6 ~ 22.0	V
V_{IN}	Input Voltage	−0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	−65 ~ 125	°C
T_{OPR}	Operating Temperature	−40 ~ 85	°C

READ OPERATION
D.C. RECOMMENDED OPERATING CONDITONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	−	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC} + 0.3	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input current	V_{IN} = 0 ~ V_{CC}		−	−	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$ = 0	f = 5MHz	−	−	30	mA
I_{CC02}			f = 1MHz	−	−	10	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}		−	−	1	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} −0.2V		−	−	100	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA		2.4	−	−	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		−	−	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = 0 ~ V_{CC} + 0.3V		−	−	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{CC}		−	−	±10	μA

A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{CC} = 5V ±5%, V_{PP} = 2.0V ~ V_{CC} + 0.3V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256D-20		TC57256D-25		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	−	200	−	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}	−	200	−	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}	−	70	−	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	0	60	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	−	0	−	ns

A.C. TEST CONDITONS

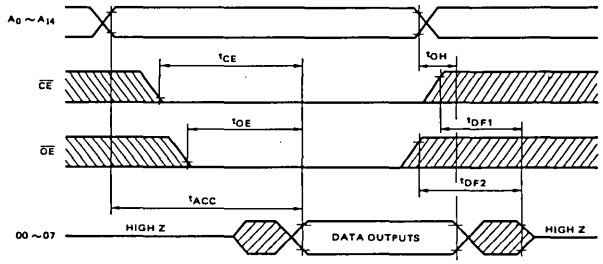
Output Load : 1 TTL Gate and C_L = 100pF
Input Pulse Rise and Fall Times : 10 ns Max.
Input Pulse Levels : 0.45 ~ 2.4V
Timing Mesurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	–	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	–	8	12	pF

*This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION
D.C. RECOMMENDED OPERATING CONDITONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 25 ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 21V ±0.5)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0 ~ V_{CC}	–	–	±10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 21.5V	–	–	30	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta = 25 ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 21V ±0.5)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs
t_{OEH}	$\overline{OE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	0.95	1	21	ms
t_{DV}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}	–	–	1	μs
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	–	–	150	ns

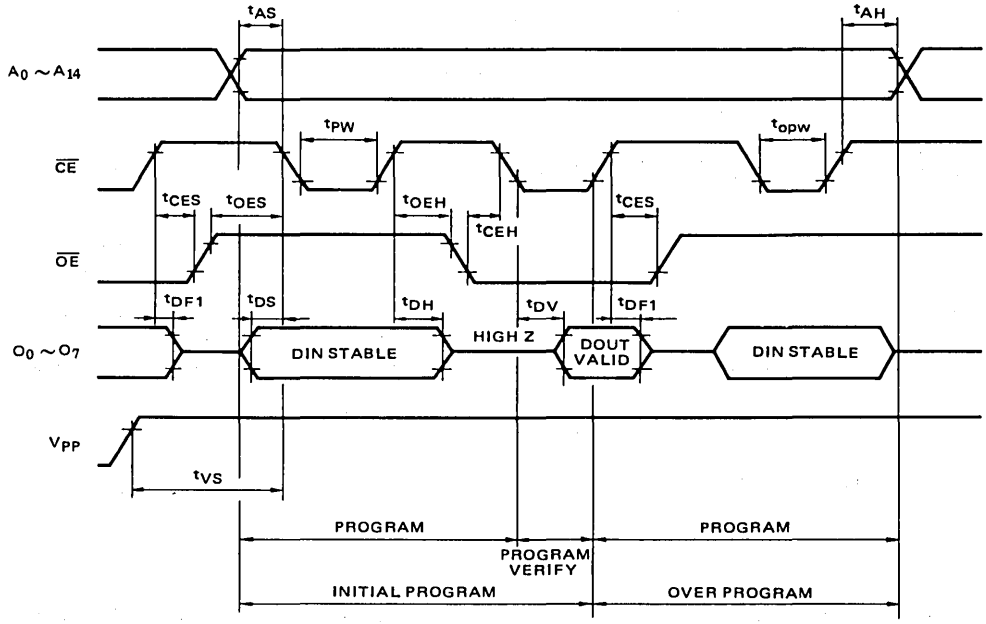
A.C. TEST CONDITIONS

Output Load	:	1 TTL Gate and C_L (100pF)
Input Pulse Rise and Fall Times	:	10 ns Max.
Input Pulse Levels	:	0.45 ~ 2.4V
Timing Measurement Reference Level	:	Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC} = 6V ±0.25V, V_{PP} = 21V ± 0.5V)



Note: (1) V_{CC} must be applied simultaneously with or before V_{PP} and cut off simultaneously with or after V_{PP}.
(2) Removing the device from socket and setting the device in socket with V_{PP}=21V may cause permanent damage to the device.
(3) The V_{PP} supply voltage is permitted up to 22V for program operation; voltages over 22V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 22V.

ERASURE CHARACTERISTICS

The TC57256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps with an ultraviolet light intensity of 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TC57256D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Both sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TC57256D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read Operation (Ta = −40 ~ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta = 25 ±5°C)	Program	L	H	21V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	L	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after the address access time from stabilizing of all addressess.

The $\overline{CE}$ to output valid (t_{CE}) time is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{CE}$.

OUTPUT DESELECT MODE

With $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in high impedance state.
Therefore two or more TC57256D's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TC57256D is placed in the standby mode which reduces the operating current to 100μA. The outputs will be in a high impedence state, independent of the $\overline{OE}$inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256D are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TC57256D is in the programming mode when the V_{PP} input is at 21V and $\overline{CE}$ is at TTL-Low $\overline{OE}=V_{IH}$.

The TC57256D can be programmed at any location, anytime — either individually, sequentially or at randomly.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC57256D from being programmed.

Programming two or more TC57256D's in parallel with different data is easily accomplished: All inputs except for $\overline{CE}$ may be commonly connected, a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only, and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using a high speed programming mode. The device is set up in the high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

Programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified in the Program Verify Mode.

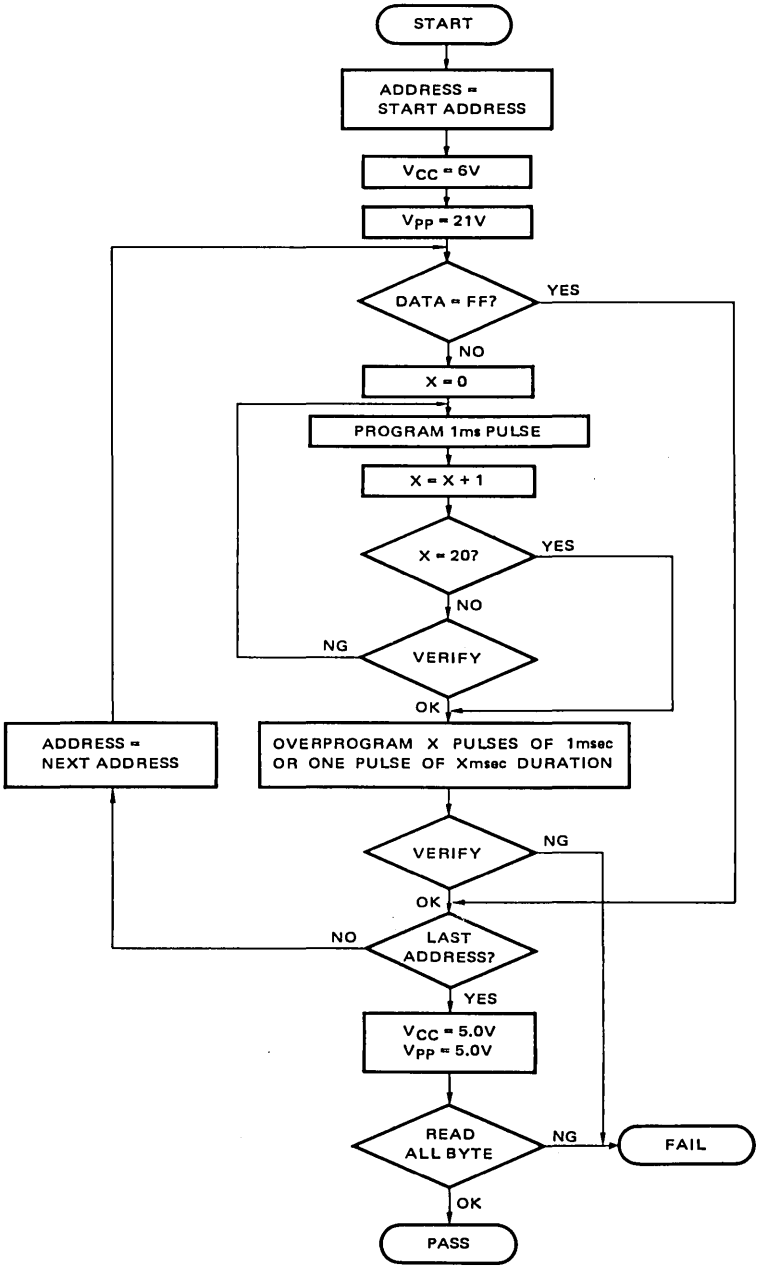
If the programmed data is not correct, another program pulse of 1ms is applied and the programmed data is verified. This should be repeated until the program operates correctly (max. 20 times).

After correctly programming the selected address, an additional program pulse with a width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

This high speed program algorithm allows the programming of the TC57256D to be accomplished within one and a half minutes (typ.)

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TC57256D which identifies its manufacture and device type.

The programming equipment may be used to read the manufacturer code and device code from the TC57256D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

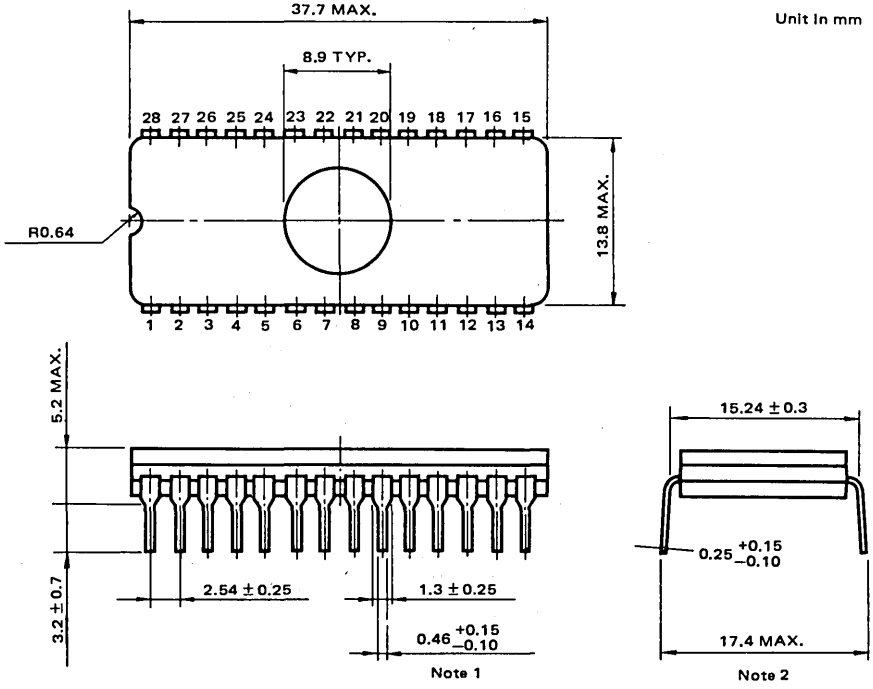
Electric Signature mode is set up when 12V is applied to address line A_9 and the rest of address lines are set to V_{IL} in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address A_0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O_7).

The following table shows electric signature of TC57256D.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

Notes: $A_9 = 12V \pm 0.5V$
$A_1 - A_8$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS



Note: (1) Each lead pitch 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.
(2) This value is measured at the end of leads.
(3) The dimensions are in millimeters.