TOSHIBA AMERICA, INC.

MOS
MEMORY

TOSHIBA

MOS MEMORY PRODUCTS

DATA BOOK

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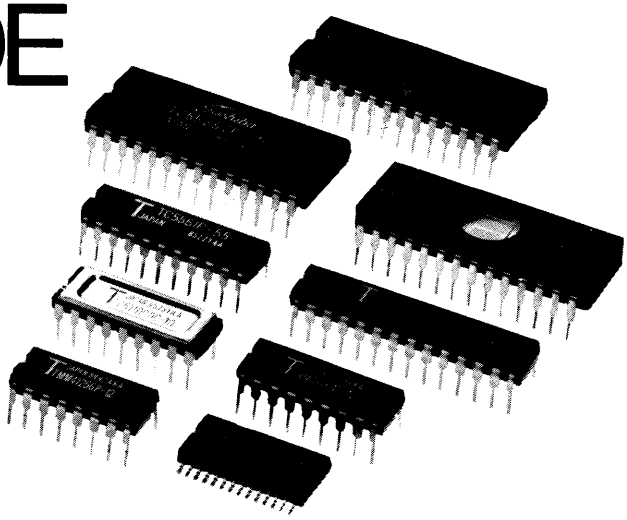
MEMORY PRODUCT GUIDE



1. NMOS Dynamic RAM

Capacity	Type No.	Organi-zation	Access Time, Max(ns)		Cycle Time	Power Supply	Power Dissipation Max (mW)		Pins	Alternate Source
			t_{RAC}	t_{CAC}	Min. (ns)	(V)	Active	Standby		
64K Bit	TMM4164AP-15	65,536×1	150	75	260	+5	275	22	16	—
	TMM4164AP-20		200	100	330					
256K Bit	TMM41256P/T-12	262,144×1	120	60	220	+5	330	28	P-16 T-16	UPD41256
	TMM41256P/T-15		150	75	260		275			
	□TMM41257P/T-12	262,144×1	120	60	220	+5	385	28	P-16 T-16	UPD41257
	□TMM41257P/T-15		150	75	260		330			
	TMM41464P-12	65,536×4	120	60	220	+5	385	28	18	UPD41464
	TMM41464P-15		150	75	260		330			

Note: Package material P: Plastic C: Ceramic, □: Nibble mode parts
*: Preliminary····· These are target specifications and are subject to change without notice.

2. CMOS Dynamic RAM

Capacity	Type No.	Organi-zation	Access Time, Max(ns)		Cycle Time	Power Supply	Power Dissipation Max (mW)		Pins	Alternate Source
			t_{RAC}	t_{CAC}	Min. (ns)	(V)	Active	Standby		
1M Bit	△TC511000P/J-10	1,048,576×1	100	50	190	+5	330	5.5	P-18 J-20	HM51100
	△TC511000P/J-12		120	60	220		275			
	□TC511001P/J-10	1,048,576×1	100	50	190	+5	330	5.5	P-18 J-20	HM51101
	□TC511001P/J-12		120	60	220		275			
	*○TC511002P/J-10	1,048,576×1	100	45	190	+5	330	5.5	P-18 J-20	HM51102
	*○TC511002P/J-12		120	55	220		275			

Note: Package material P: Plastic C: Ceramic, △: Fast page mode parts
○: Static Column parts □: Nibble mode parts
*: Preliminary····· These are target specifications and are subject to change without notice.

3. STANDARD APPLICATION NMOS STATIC RAMS

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Package Width (inch)	Alternate Source
						Active	Standby			
16K Bit	TMM2015AP-90	2,048×8	90	90	+5	440	38.5	24	0.3	(HM6116AS)
	TMM2015AP-10		100	100		358				
	TMM2015AP-12		120	120						
	TMM2015AP-15		150	150						
	TMM2015BP-90	2,048×8	90	90	+5	275	27.5	24	0.3	(HM6116AS)
	TMM2015BP-10		100	100						
	TMM2015BP-12		120	120						
	TMM2015BP-15		150	150						
	TMM2016AP-90	2,048×8	90	90	+5	440	38.5	24	0.6	(HM6116)
	TMM2016AP-10		100	100		358				
	TMM2016AP-12		120	120						
	TMM2016AP-15		150	150						
	TMM2016BP-90	2,048×8	90	90	+5	275	27.5	24	0.6	(HM6116)
	TMM2016BP-10		100	100						
	TMM2016BP-12		120	120						
	TMM2016BP-15		150	150						
64K Bit	TMM2063P-10	8,192×8	100	100	+5	440	55	28	0.3	(HM6264AS)
	TMM2063P-12		120	120						
	TMM2063P-15		150	150						
	TMM2064P-70	8,192×8	70	70	+5	440	55	28	0.6	(HM6264)
	TMM2064P-10		100	100						
	TMM2064P-12		120	120						
	TMM2064P-15		150	150						

Note: Package material P: Plastic

4. STANDARD APPLICATION CMOS STATIC RAM

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Alternate Source
						Active	Standby		
4K Bit	TC5514AP-2	1,024×4	200	200	+5	27.5	0.11	18	HM6514
	TC5514AP-3		300	300					
	TC5514APL-2		200	200			0.005		
	TC5514APL-3		300	300					
16K Bit	TC5516AP/AF-2	2,048×8	200	200	+5	302.5	0.165	24	—
	TC5516AP/AF		250	250					
	TC5516APL/AFL-2		200	200			0.005		
	TC5516APL/AFL		250	250					
	TC5517AP/AF-2	2,048×8	200	200	+5	302.5	0.165	24	(HM6116L)
	TC5517AP/AF		250	250					
	TC5517APL/AFL-2		200	200			0.005		
	TC5517APL/AFL		250	250					
	TC5517BP/BF-20	2,048×8	200	200	+5	27.5	0.165	24	(HM6116L)
	TC5517BP/BF-25		250	250					
	TC5517BPL/BFL-20		200	200			0.005		
	TC5517BPL/BFL-25		250	250					
	TC5518BP/BF-20	2,048×8	200	200	+5	27.5	0.165	24	(HM6117L)
	TC5518BP/BF-25		250	250					
	TC5518BPL/BFL-20		200	200			0.005		
	TC5518BPL/BFL-25		250	250					
	TC5517CP/CF-15	2,048×8	150	150	+5	27.5	0.165	24	(HM6116L)
	TC5517CP/CF-20		200	200					
	TC5517CPL/CFL-15		150	150			0.005		
	TC5517CPL/CFL-20		200	200					
	TC5518CP/CF-15	2,048×8	150	150	+5	27.5	0.165	24	(HM6117L)
	TC5518CP/CF-20		200	200					
	TC5517CPL/CFL-15		150	150			0.005		
	TC5518CPL/CFL-20		200	200					
64K Bit	TC5564PL-15	8,192×8	150	150	+5	27.5	0.005	28	μPD4464C
	TC5564PL-20		200	200					
	TC5564APL-12		120	120					
	TC5564APL-15		150	150					
	TC5565PL/FL-12	8,192×8	120	120	+5	27.5	0.55	28	HM6264L
	TC5565PL/FL-15		150	150					
	TC5565PL/FL-12L		120	120			0.165		
	TC5565PL/FL-15L		150	150					
256K Bit	*TC55257P-10	32,768×8	100	100	+5	27.5	5.5	28	—
	*TC55257P-12		120	120					
	*TC55257PL-10	32,768×8	100	100	+5	27.5	0.55	28	—
	*TC55257PL-12		120	120					

Note: Package material P: Plastic F: Flat package

*: Preliminary ····· These are target specifications and are subject to change without notice.

5. HIGH SPEED NMOS STATIC RAMS

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW) Active	Power Dissipation Max (mW) Standby	Pins	Package Width (inch)	Alternate Source
16K Bit	TMM2068D-35	4,096×4	35	35	+5	825	110	20	0.3	IMS1420
	TMM2068D-45		45	45		660				
	TMM2068D-55		55	55						
	TMM2078D-35	4,096×4	35	35	+5	825	110	22	0.3	—
	TMM2078D-45		45	45		660				
	TMM2078D-55		55	55						
	TMM2018D-35	2,048×8	35	35	+5	825	110	24	0.3	—
	TMM2018D-45		45	45						
	TMM2018D-55		55	55						

6. HIGH SPEED CMOS STATIC RAMS

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW) Active	Power Dissipation Max (mW) Standby	Pins	Alternate Source
64K Bit	TC5561P-55	65,536×1	55	55	+5	550	0.55	22	—
	TC5561P-70		70	70					
	TC5562P-45	65,536×1	45	45	+5	550	11	22	HM6287
	TC5562P-55		55	55					

7. NMOS EPROM

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Alternate Source
						Active	Standby		
64K Bit	TMM2764AD-15	8,192×8	150	150	+5	525	131	28	i2764
	TMM2764AD-20		200	200					
	TMM2764AD-150		150	150					
	TMM2764AD-200		200	200					
128K Bit	TMM27128AD-15	16,384×8	150	150	+5	525	131	28	i27128
	TMM27128AD-20		200	200					
	TMM27128AD-150		150	150					
	TMM27128AD-200		200	200					
256K Bit	TMM27256AD-15	32,768×8	150	150	+5	525	131	28	i27256
	TMM27256AD-20		200	200					
	TMM27256AD-150		150	150					
	TMM27256AD-200		200	200					
512K Bit	TMM27512D-20	65,536×8	200	200	+5	525	131	28	i27512
	TMM27512D-25		250	250					
	TMM27512D-200		200	200					
	TMM27512D-250		250	250					

Note: Package material D: Cerdip DI type; Operating temperature range=−40°C~85°C

8. CMOS EPROM

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Alternate Source
						Active	Standby		
256K Bit	TC57256D-20	32,768×8	200	200	+5	158	0.525	28	MBM27C256
	TC57256D-25		250	250					

Note: Package material D: Cerdip

9. NMOS OTP

64K Bit	TMM2464AP/F	8192×8	200	200	+5	525	131	28	P2764
128K Bit	TMM24128AP/F	16,384×8	200	200	+5	525	131	28	P27128
256K Bit	TMM24256AP/F	32,768×8	200	200	+5	525	131	28	P27256

Note: Package Material P: Plastic F: Flat Package

10. CMOS OTP

256K Bit	TC54256P/F	32,768×8	200	200	+5	158	0.525	28	—

Note: Package Material P: Plastic F: Flat Package

11. NMOS Mask ROM

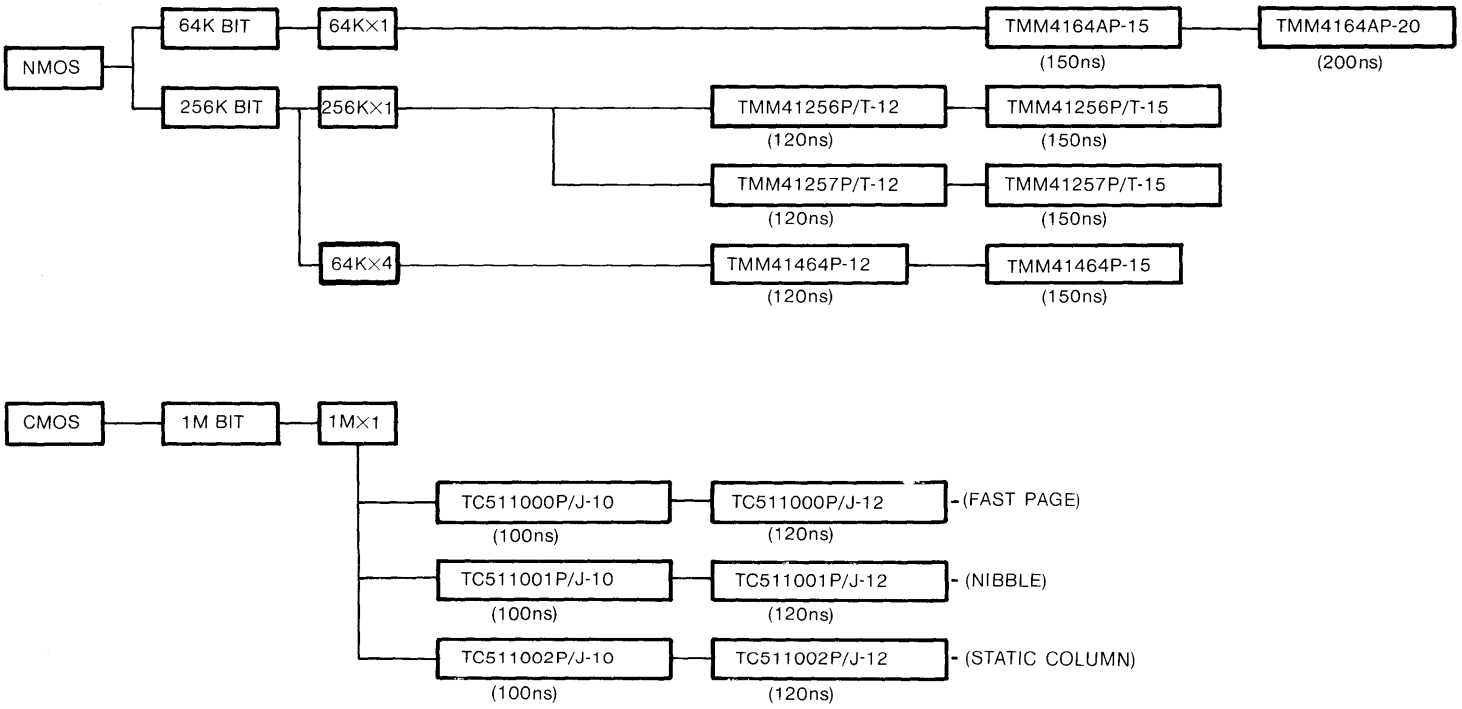
Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Alternate Source
						Active	Standby		
64K Bit	TMM2365P	8,192×8	200	200	+5	550	138	28	(i2764)
	TMM2366P		200	200		550	138	24	(TMS4764)
128K Bit	TMM23128P	16,384×8	200	200	+5	440	110	28	(i27128)
256K Bit	TMM23256P	32,768×8	150	230	+5	220	55	28	(i27256)

Note: Package Material P: Plastic

12. CMOS Mask ROM

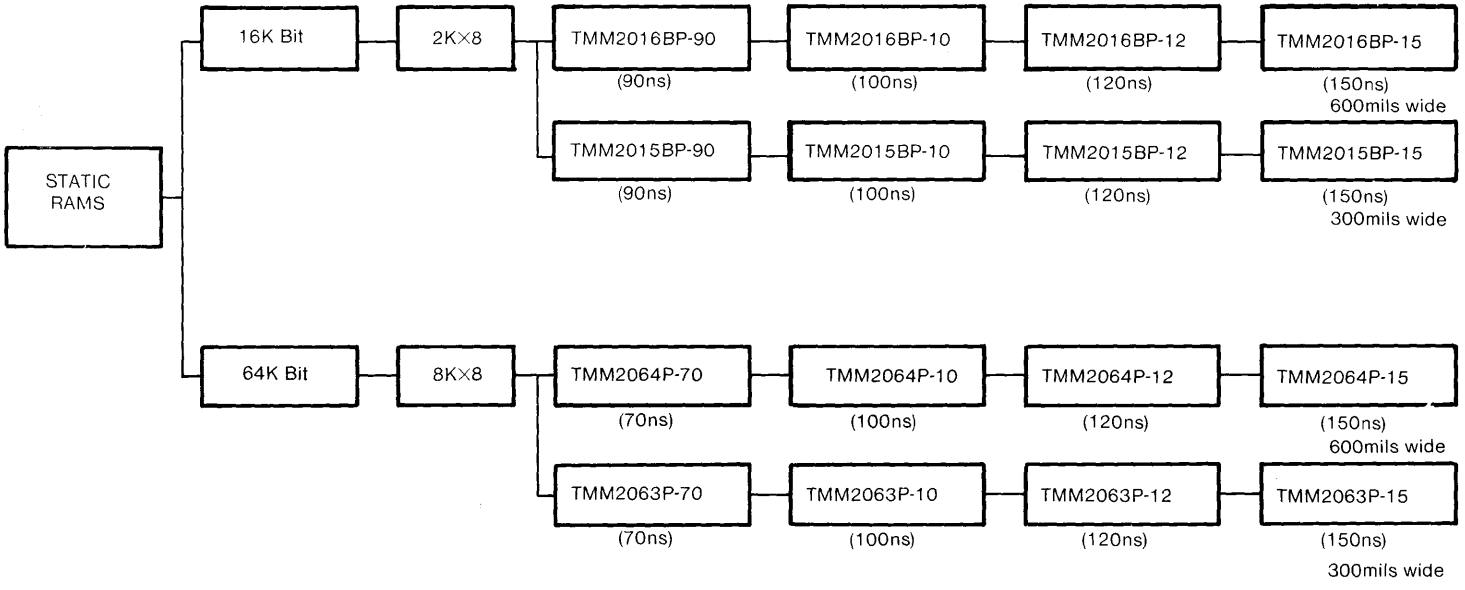
Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Alternate Source
						Active	Standby		
64K Bit	TC5364P	8,192×8	250	350	+5	39	0.11	28	(MK37000)
	TC5365P/F			250					(i2764)
	TC5366P							24	(TMS4764)
256K Bit	TC53257P/F	32,768×8	200	200	+5	39	0.11	28	(i27256)
1M Bit	TC531000P	131,072×8	200	200	+5	39	0.11	28	—

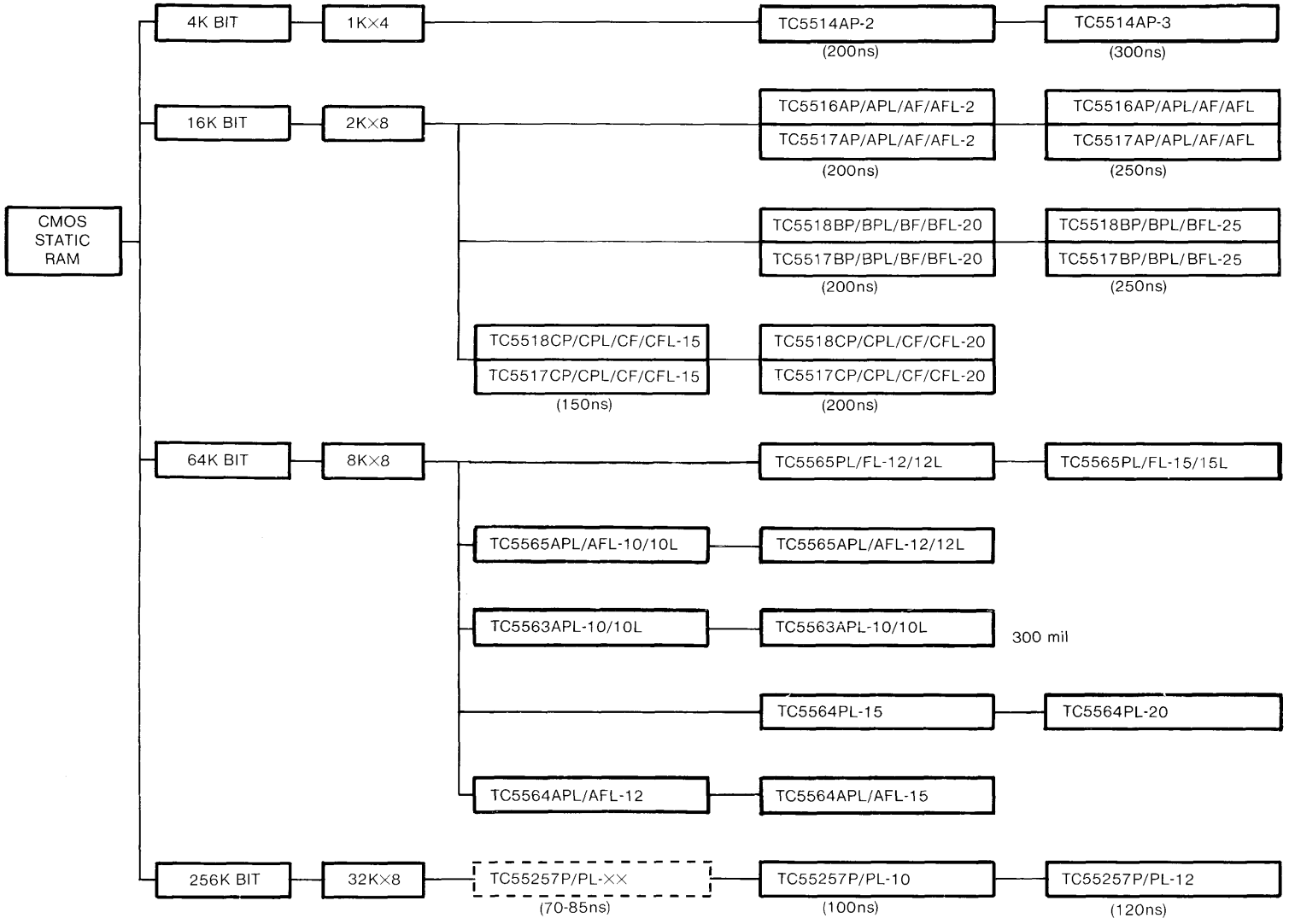
Note: Package material P: Plastic



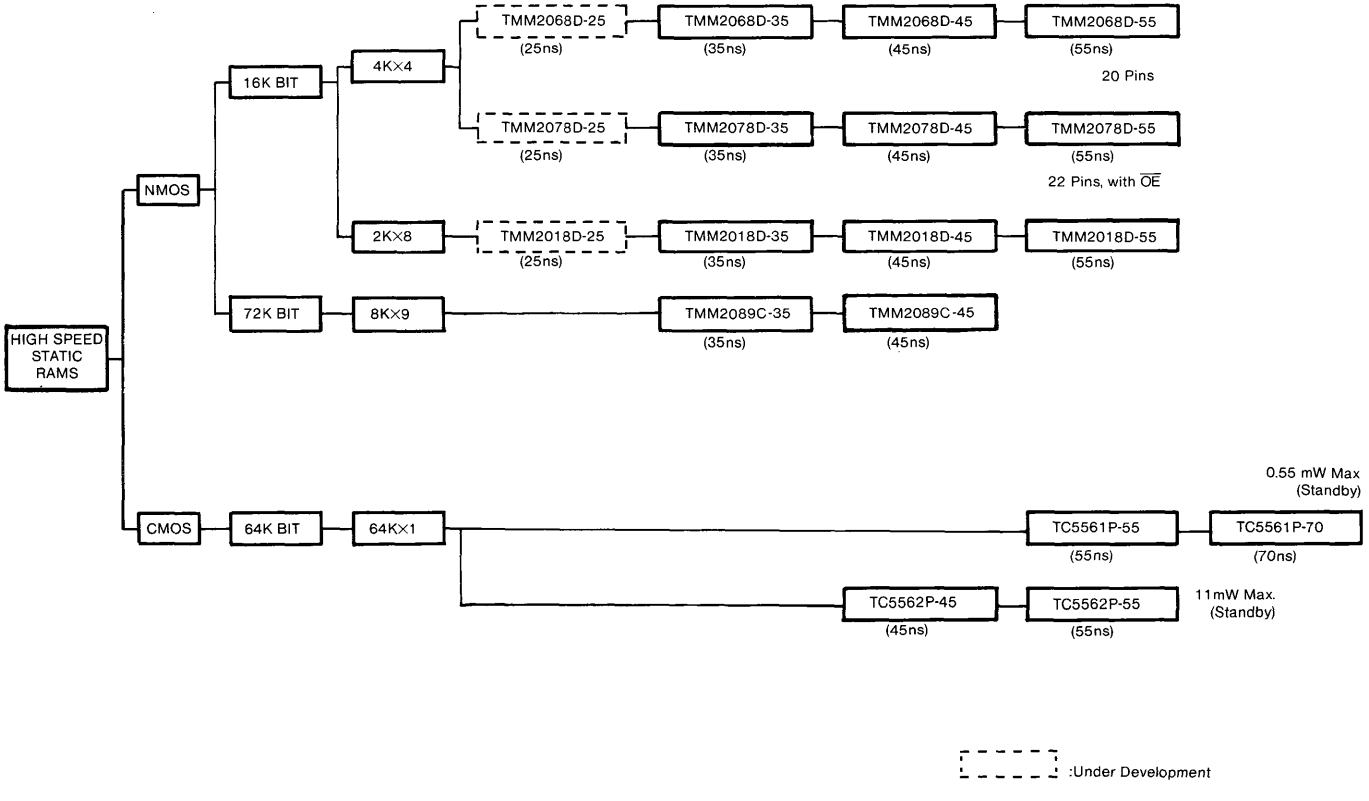
C: CERAMIC P: PLASTIC T: PLCC J: SOJ

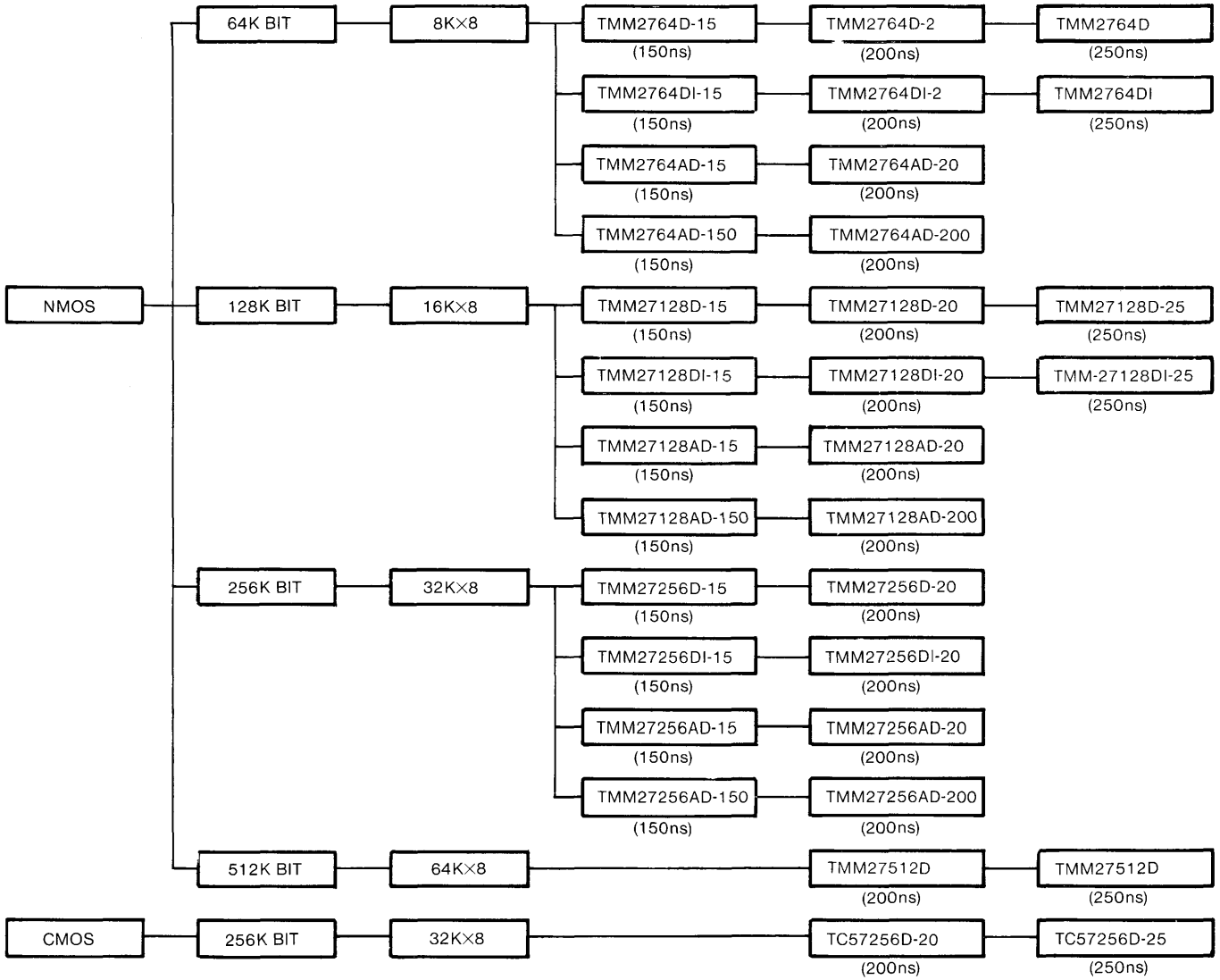
*Preliminary

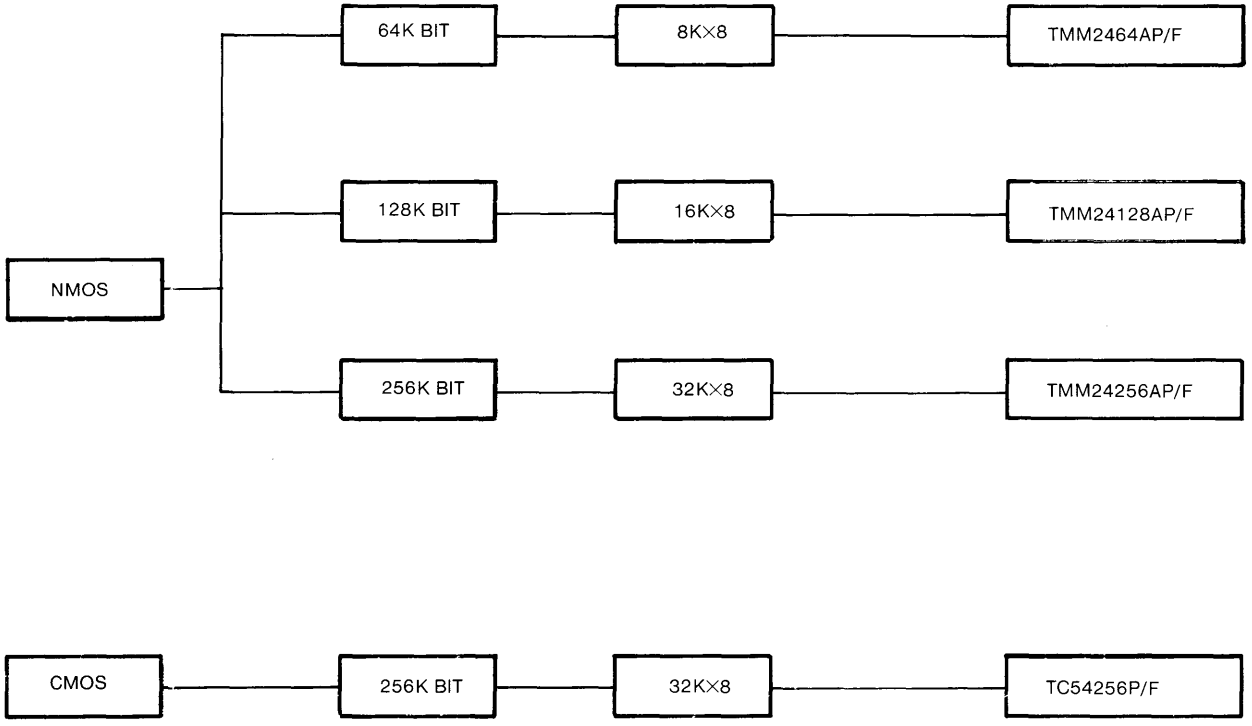

STATIC RAMS
16K Bit
2K×8
TMM2016BP-90
(90ns)
TMM2016BP-10
(100ns)
TMM2016BP-12
(120ns)
TMM2016BP-15
(150ns)
600mils wide
TMM2015BP-90
(90ns)
TMM2015BP-10
(100ns)
TMM2015BP-12
(120ns)
TMM2015BP-15
(150ns)
300mils wide
64K Bit
8K×8
TMM2064P-70
(70ns)
TMM2064P-10
(100ns)
TMM2064P-12
(120ns)
TMM2064P-15
(150ns)
600mils wide
TMM2063P-70
(70ns)
TMM2063P-10
(100ns)
TMM2063P-12
(120ns)
TMM2063P-15
(150ns)
300mils wide


CMOS STATIC RAM
4K BIT
1K×4
TC5514AP-2
(200ns)
TC5514AP-3
(300ns)
16K BIT
2K×8
TC5516AP/APL/AF/AFL-2
TC5517AP/APL/AF/AFL-2
(200ns)
TC5516AP/APL/AF/AFL
TC5517AP/APL/AF/AFL
(250ns)
TC5518BP/BPL/BF/BFL-20
TC5517BP/BPL/BF/BFL-20
(200ns)
TC5518BP/BPL/BFL-25
TC5517BP/BPL/BFL-25
(250ns)
TC5518CP/CPL/CF/CFL-15
TC5517CP/CPL/CF/CFL-15
(150ns)
TC5518CP/CPL/CF/CFL-20
TC5517CP/CPL/CF/CFL-20
(200ns)
64K BIT
8K×8
TC5565PL/FL-12/12L
TC5565PL/FL-15/15L
TC5565APL/AFL-10/10L
TC5565APL/AFL-12/12L
TC5563APL-10/10L
TC5563APL-10/10L
300 mil
TC5564PL-15
TC5564PL-20
TC5564APL/AFL-12
TC5564APL/AFL-15
256K BIT
32K×8
TC55257P/PL-××
(70-85ns)
TC55257P/PL-10
(100ns)
TC55257P/PL-12
(120ns)

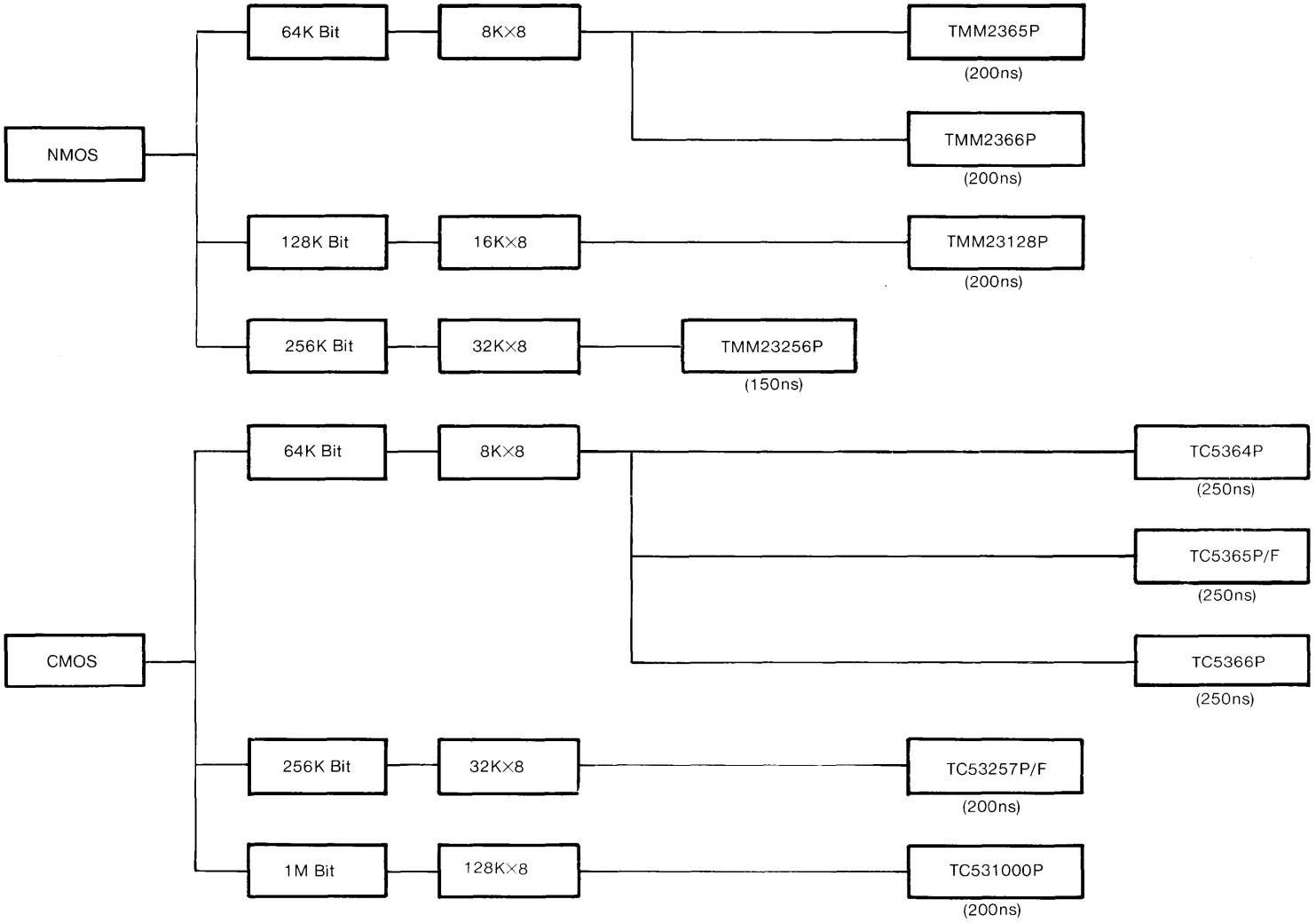
TOSHIBA HIGH SPEED STATIC RAM (25ns-70ns)




NMOS
64K BIT
8K×8
TMM2764D-15 (150ns)
TMM2764D-2 (200ns)
TMM2764D (250ns)
TMM2764DI-15 (150ns)
TMM2764DI-2 (200ns)
TMM2764DI (250ns)
TMM2764AD-15 (150ns)
TMM2764AD-20 (200ns)
TMM2764AD-150 (150ns)
TMM2764AD-200 (200ns)
128K BIT
16K×8
TMM27128D-15 (150ns)
TMM27128D-20 (200ns)
TMM27128D-25 (250ns)
TMM27128DI-15 (150ns)
TMM27128DI-20 (200ns)
TMM-27128DI-25 (250ns)
TMM27128AD-15 (150ns)
TMM27128AD-20 (200ns)
TMM27128AD-150 (150ns)
TMM27128AD-200 (200ns)
256K BIT
32K×8
TMM27256D-15 (150ns)
TMM27256D-20 (200ns)
TMM27256DI-15 (150ns)
TMM27256DI-20 (200ns)
TMM27256AD-15 (150ns)
TMM27256AD-20 (200ns)
TMM27256AD-150 (150ns)
TMM27256AD-200 (200ns)
512K BIT
64K×8
TMM27512D (200ns)
TMM27512D (250ns)
CMOS
256K BIT
32K×8
TC57256D-20 (200ns)
TC57256D-25 (250ns)


NMOS
64K BIT
8K×8
TMM2464AP/F
128K BIT
16K×8
TMM24128AP/F
256K BIT
32K×8
TMM24256AP/F
CMOS
256K BIT
32K×8
TC54256P/F

TOSHIBA MASK ROM



MEMORY SELECTION GUIDE (1)

* Preliminary

Access Time (ns)	4K Bit	16K Bit	64K Bit	72K Bit	128K Bit	256K Bit	512K Bit	1M Bit
300	TC5514AP-3							
		TC5516AP TC5517AP TC5517BP-25 TC5518BP-25	TMM2764D TC5364P TC5365P TC5366P		TMM27128D-25	TC57256D-25 *TC57256AD-25	TMM27512D-25 TMM27512D-250	
200	TC5514AP-20	TC5516AP-2 TC5517AP-2 TC5517BP-20 TC5518BP-20 TC5517CP-20 TC5518CP-20	TMM2764AD-20 TMM2764AD-200 TMM4164AP-20 TC5564PL-20 TMM2764D-2 TMM2365P TMM2366P TMM2464AP		TMM27128D-20 TMM23128P TMM24128AP TMM27128AD-20 TMM27128AD-200	*TC57256AD-20 TMM27256AD-20 TMM41256C-20 TMM27256D-20 TC57256D-20 TC53257P TMM27256AD-200 *TC57256AD-200 TMM24256AP TC54256P	TMM27512D-20 TMM27512D-200	TC531000P
		TMM2015AP-12/15 TMM2015BP-12/15 TMM2016AP-12/15 TMM2016BP-12/15 TC5517CP-15 TC5518CP-15	TMM4164AP-15 TMM2063P-12/15 TMM2064P-12/15 TC5564PL-15 TC5564APL-12/15 TC5565PL-12/15 TMM2764D-15 TMM2764AD-15 TMM2764AD-150		TMM27128D-15 TMM27128AD-15 TMM27128AD-150	TMM41256P/T-12/15 TMM41257P/T-12/15 TMM41464P-12/15 TC55257P-12 TMM27256D-15 TMM23256P TMM27256AD-15 TMM27256AD-150		TC511000P/J-12 TC51001P/J-12 TC511001P/J-12 TC511001P/J
100		TMM2015AP-90/10 TMM2015BP-90/10 TMM2016AP-90/10 TMM2016BP-90/10	TMM2063P-10 TMM2064P-10 TMM2064P-70 TC5561P-55/70			TC55257P-10		TC511000P/J-10 TC511001P/J-10 TC511002P/J-10
		TMM2018D-35/45/55 TMM2068D-35/45/55 TMM2078D-35/45/55	TC5562P-45/55	TMM2089C-35/45/55				

MEMORY SELECTION GUIDE (2)

• Preliminary

Memory	Type	Memory Capacity							
		4K Bit	16K Bit	64K Bit	72K Bit	128K Bit	256K Bit	512K Bit	1M Bit
RAM	NMOS Dynamic RAM			TMM4164AP			TMM41256C/P TMM41257P/T TMM41464P/T		
	CMOS Dynamic RAM								TC511000P/J TC511001P/J TC511002P/J
	NMOS Static RAM		TMM2015AP TMM2015BP TMM2016AP TMM2016BP TMM2018D TMM2068D TMM2078D	TMM2063P TMM2064	TMM2089C		TC55257P		
	CMOS Static RAM		TC5516AP/AF TC5517AP/AF TC5517BP/BF TC5518BP/BF TC5517CP/CF TC5518CP/CF	TC5564PL TC5564APL/FL TC5563APL TC5565PLFL TC5565APL/AFL TC5561P TC5562P			TC55257P		
ROM	NMOS EPROM			TMM2764AD TMM2764D TMM2764DI		TMM27128AD TMM27128D TMM27128DI	TMM27256AD TMM27256D TMM27256DI	TMM27512D	
	CMOS EPROM						TC57256D		
	NMOS Mask ROM			TMM2365P TMM2366P		TMM23128P	TMM23256P		
	CMOS Mask ROM			TC5364P TC5365P/F TC5366P			TC53257P/F		TC531000P
	NMOS OTP			TMM2464AP		TMM24128AP	TMM24256AP		
	CMOS OTP						TC54256P		

MEMORY SELECTION GUIDE (3)

Word \ Bit	1	4	8	9
1K		TC5514AP		
2K			TMM2015AP TC5516AP/AF TMM2015BP TC5517AP/AF TMM2016AP TC5517BP/BF TMM2016BP TC5518BP/BF TMM2018D *TC5517CP/CF *TC5518CP/CF	
4K		TMM2068D TMM2078D		
8K			TMM2063P TMM2365P TMM2064P TMM2366P TMM2464P TMM2764AD TC5564PL TC5364P TC5565PL/FL TC5365P/F TMM2764D TC5366P	TMM2089C
16K			TMM27128D TMM24128P TMM23128P TMM27128AD	
32K			TC55257P TMM23256P TC54256P TMM27256AD TMM27256D TC53257P TC57256D T57256AD TMM24256P	
64K	TMM4164AP TC5561P TC5562P	TMM41464P	TMM27512D	
128K			TC531000P	
256K	TMM41256C/P/T TMM41257P/T			
1M	*TC511000P/J *TC511001P/J *TC511002P/J			

TOSHIBA BYTE-WIDE MEMORY PIN OUT (CURRENT AND FUTURE DEVICES)

1M BIT	MROM	TC531000
512K BIT	EPROM	TMM27512D
256K BIT	MROM	TMM23256/TC53257
	OTP	TC54256/TMM24256
	EPROM	TC57256/TMM27256
	CRAM	*TC55257
128K BIT	MROM	TMM23128
	OTP	TMM24128
	EPROM	TMM27128
72K BIT	H.S. SRAM	TMM2089
64K BIT	CRAM	TC5564/65
	SRAM	TMM2063/64
	MROM	TMM2365/TC5365
	OTP	TMM2464
	EPROM	TMM2764
16K BIT	CRAM	TC5517
		TC5516/18
	H.S. SRAM	TMM2018
	SRAM	TMM2015/16

16K BIT	SRAM	TMM2015/16
	H.S. SRAM	TMM2018
	CRAM	TC5516/18
		TC5517
64K BIT	EPROM	TMM2764
	OTP	TMM2464
	MROM	TMM2365/TC5365
	SRAM	TMM2063/64
	CRAM	TC5564/65
72K BIT	H.S. SRAM	TMM2089C
128K BIT	EPROM	TMM27128
	OTP	TMM24128
	MROM	TMM23128
256K BIT	CRAM	*TC55257
	EPROM	TC57256/TMM27256
	OTP	TC54256/TMM24256
	MROM	TMM23256/TC53257
512K BIT	EPROM	TMM27512D
1M BIT	MROM	TC531000

4. 16K Bit Static RAM

1) NMOS

Organization	2K × 8			4K × 4
Package Width	0.6 inch	0.3 inch		
TOSHIBA	TMM2016AP/BP	TMM2015AP/BP	TMM2018D	TMM2068D
Fujitsu	MB8128			MB8168
Hitachi	HM6116	HM6116AS		HM6168
Inmos				IMS1420/1421
Mitsubishi	M58725			M5M2168
Motorola	MCM2128		MCM2016/18H	MCM6168/78
NEC	μPD4016	μPD4016CX		
Oki	MSM2128			

2) CMOS

Organization	2K × 8		
TOSHIBA	TC5516AP	TC5517AP/BP/CP	TC5518BP/CP
Fujitsu	MB8417	MB8416	MB8418
Hitachi		(HM6116)	(HM6117)
NEC	μPD447	μPD446	μPD449
Mitsubishi	M5M5116	M5M5117	M5M5118
Oki	MSM5127	MSM5128	MSM5129

5. 64K Bit Static RAM

NMOS/CMOS	NMOS		CMOS		
Package Width	0.3 inch	0.6 inch			0.3 inch
TOSHIBA	TMM2063P	TMM2064P	TC5564P	TC5565P	TC5562P
Fujitsu		MB8464		MB8464	HB81C71
Hitachi	HM6264AS	HM6264		HM6264	HM6287
Mitsubishi		M5M5165	M5M5164	M5M5165	
NEC		μPD4364	μPD4464	μPD4364	μPD4361
Oki		MSM5165	MSM5164	MSM5165	
Inmos					IMS1600

CROSS REFERENCE

1. 64K Bit Dynamic RAM

TOSHIBA	TMM4164AP
Fujitsu	MB8264A
Hitachi	HM4864A
Mitsubishi	M5K4164AN
Motorola	MCM6665A
NEC	μPD4164
Oki	MSM3764A
TI	TMS4164

2. 256K Bit Dynamic RAM

Organization	256K × 1 (page mode)	256K × 1 (nibble mode)	64K × 4 (page mode)
TOSHIBA	TMM41256P/T	TMM41257P/T	TMM41464P
Fujitsu	MB81256	MB81257	MB81464
Hitachi	HM50256	HM50257	HM50464
Mitsubishi	M5M4256	M5M4257	M5M4464
NEC	μPD41256	μPD41257	μPD41464
Oki	MSM37256	MSM37257	
TI	TMS4256	TMS4257	TMS4464

3. IMBIT DYNAMIC RAM

Organizatiom	IMB × 1 (Fast page mode)		IMB × 1 (Static column mode)		IMB × 1 (Nibble mode)	
SUPPLIER	PART #	PROCESS	PART #	PROCESS	PART #	PROCESS
TOSHIBA	TC511000	CMOS	TC511002	CMOS	TC511001	CMOS
AT & T	M411024XP	CMOS	—		M411024XN	CMOS
FUJITSU	MB811000	NMOS	?		MB811001	NMOS
HITACHI	HM51100	CMOS	HM51102	CMOS	HM511C1	CMOS
MITSUBISHI	?	NMOS	—		?	
NEC	μPD411000	NMOS	—		?	
PANASONIC	MN411000	NMOS	—		—	
SIEMENS	?	CMOS	—		—	
TI	?	CMOS	?		?	

Note: ( ): Vpp=12.5V

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right at any time without notice, to change said circuitry.

6. 64K/128K Bit EPROM/OTP/Mask ROM

Organization	8K×8				16K×8		
EPROM/OTP/MROM	EPROM	OTP	MROM		EPROM	OTP	MROM
Pins	28	28	28	24	28	28	28
TOSHIBA	(TMM2764AD)	(TMM2464AP)	TMM2365P TC5364/65P	TMM2366P TC5366P	(TMM27128AD)	(TMM24128AP)	TMM23128P
AMD	Am2764				Am27128		
Fujitsu	MBM2764			MB8364	MBM27128		—
Hitachi	HN482764	HN482764	HN61364	HN48364	HN4827128	HN4827128	HN43128
Intel	i2764	(P2764A)	i2364		i27128	(P27128A)	—
Mitsubishi	M5L2764		M5M2364	M58334	M5L27128		
Mostek			MK37000	MK36000			
Motorola	—			MCM68364			
NEC	μPD2764	μPD2764C		μPD2364	μPD27128	μPD27218C	μPD23128
Oki	MSM2764		MSM3864	MSM2965	MSM27218		MSM38218
TI	—			TMS4764	—		

7. 256K/512K/IMBIT EPROM/OTP/MROM

Organization	32K×8						64K×8	128K×8
EPROM/OTP/MROM	EPROM		OTP		MROM		EPROM	MROM
	NMOS	CMOS	NMOS	CMOS	NMOS	CMOS	NMOS	CMOS
TOSHIBA	(TMM27256AD)	TC57256D	(TMM24256AP)	(TMM54256P)	TMM23256P	TC53257P	(TMM27512D)	TC531000P
AMD	(Am27256)							
Fujitsu	(MBM27256)	MBM27C256				MB83256		MB831124
Hitachi	(HN27256)	(HN27C256)	HN4827256			HN613256P	(AM27512)	HN62301
Intel	(i27256)	(i27C256)	(P27256A)		—	—	(i27512)	—
Mitsubishi	—	—						M5M231000
NEC	μPD27256	μPD27C256	μPD27256C	μPD27C256C	μPD23256	μPD23C256		μPD231000
Oki	—	—			MSM38256	MSM53256		MSM531000
RCA	—	—				CDM53256		

NMOS Dynamic Random Access Memories

65,536 WORD × 1 BIT DYNAMIC RAM
N-CHANNEL SILICON GATE MOS

TMM4164AP-12, TMM4164AP-15 TMM4164AP-20

DESCRIPTION

The TMM4164AP is the high speed, low power dynamic RAM organized 65,536 words by 1 bit, it is successor to the industry standard TMM4164P.

The TMM4164AP utilizes TOSHIBA's double poly N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM4164AP to be packaged in a standard 16 pin plastic DIP. This package size provides high system bit density and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

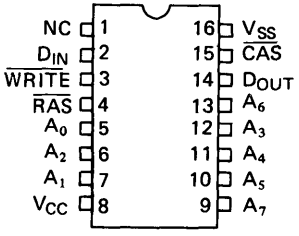
FEATURES

- 65,536 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{CAC}	t_{RC}
TMM4164AP-12	120 ns	60 ns	220 ns
TMM4164AP-15	150 ns	75 ns	260 ns
TMM4164AP-20	200 ns	100 ns	330 ns

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low power; 275mW operating (MAX.)
  22mW standby (MAX.)
- Industry standard 16 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh and Page Mode capability
- All inputs and output TTL compatible
- 128 refresh cycles/2ms

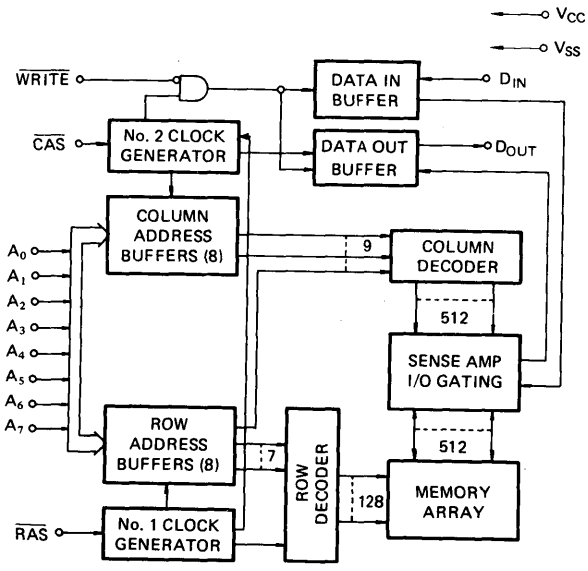
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
NC	No – Connection
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	—	—	50	mA	3,4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)	—	—	4	mA	
I_{CC3}	REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	—	—	40	mA	3
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN.)	—	—	40	mA	3, 4
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)	−10	—	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ +5.5V)	−10	—	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)	2.4	—		V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)	—	—	0.4	V	

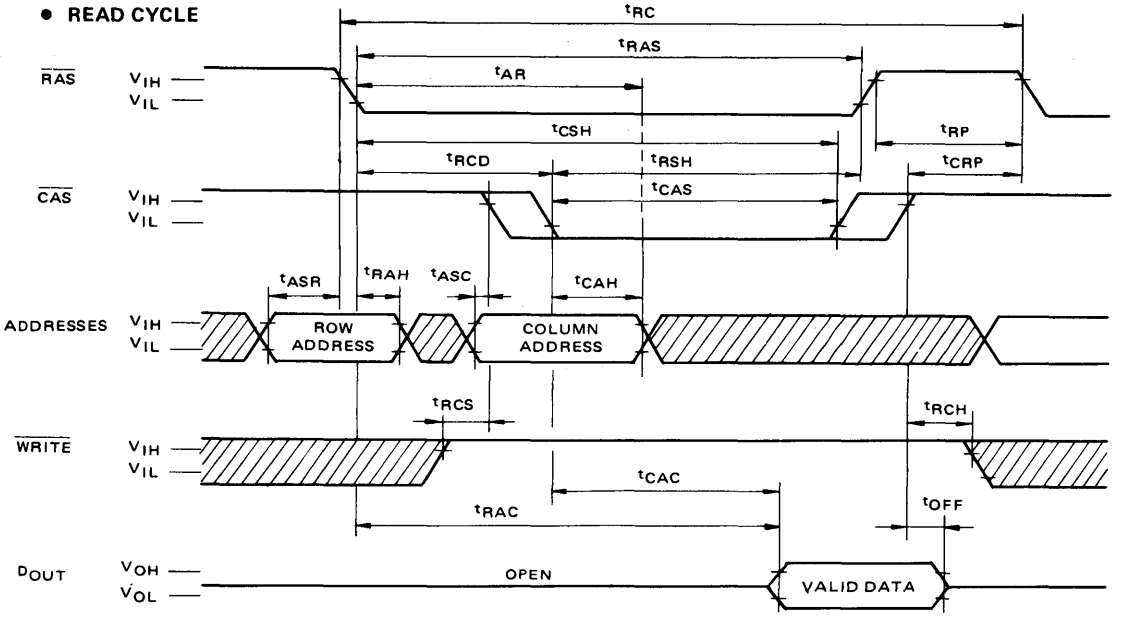
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

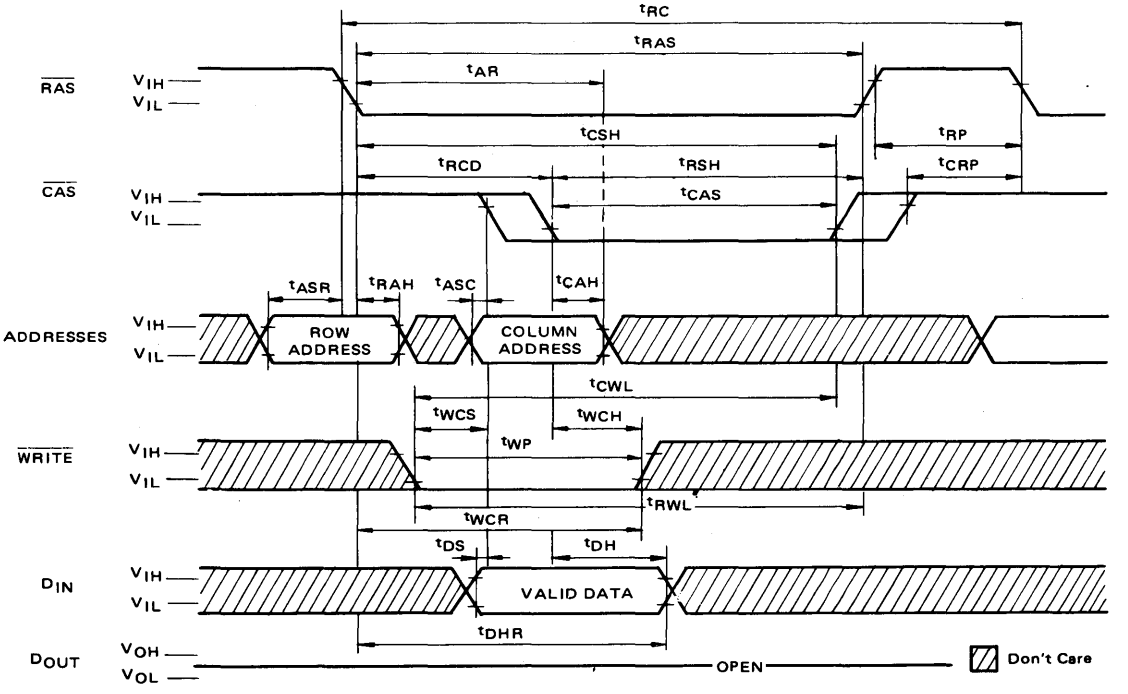
SYMBOL	PARAMETER	TMM4164AP-12		TMM4164AP-15		TMM4164AP-20		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	—	260	—	330	—	ns	
t_{RWC}	Read-Write Cycle Time	240	—	285	—	350	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	260	—	310	—	390	—	ns	
t_{PC}	Page Mode Cycle Time	120	—	145	—	190	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	120	—	150	—	200	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$	—	60	—	75	—	100	ns	9, 10
t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	0	50	ns	11
t_T	Transition Time (Rise and Fall)	3	35	3	35	3	50	ns	6
t_{RP}	$\overline{RAS}$ Precharge Time	90	—	100	—	120	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	200	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	—	75	—	100	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	—	150	—	200	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	100	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	30	100	ns	12
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0	—	0	—	0	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	20	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	35	—	45	—	55	—	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95	—	120	—	155	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	35	—	45	—	55	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95	—	120	—	155	—	ns	
t_{WP}	Write Command Pulse Width	35	—	45	—	55	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	—	45	—	55	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	—	45	—	55	—	ns	
t_{DS}	Data-In Set-Up Time	0	—	0	—	0	—	ns	13
t_{DH}	Data-In Hold Time	35	—	45	—	55	—	ns	13
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95	—	120	—	155	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	50	—	60	—	80	—	ns	
t_{REF}	Refresh Period	—	2	—	2	—	2	ms	
t_{WCS}	Write Command Set-Up Time	−10	—	−10	—	−10	—	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	40	—	50	—	60	—	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100	—	125	—	160	—	ns	14

TIMING WAVEFORMS

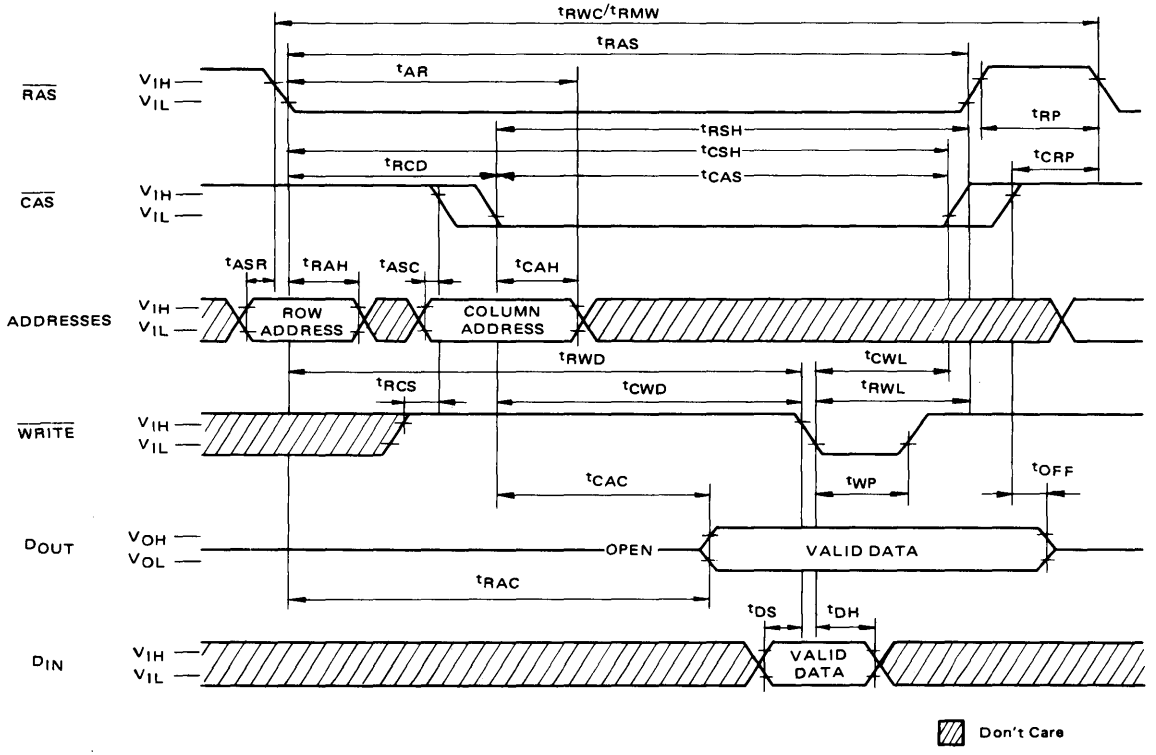
- READ CYCLE



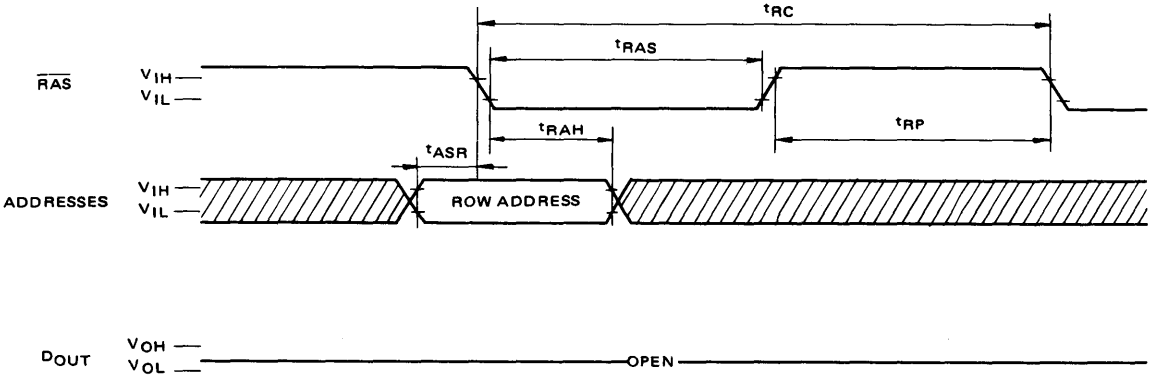
- WRITE CYCLE (EARLY WRITE)



- **READ-WRITE/READ-MODIFY-WRITE CYCLE**

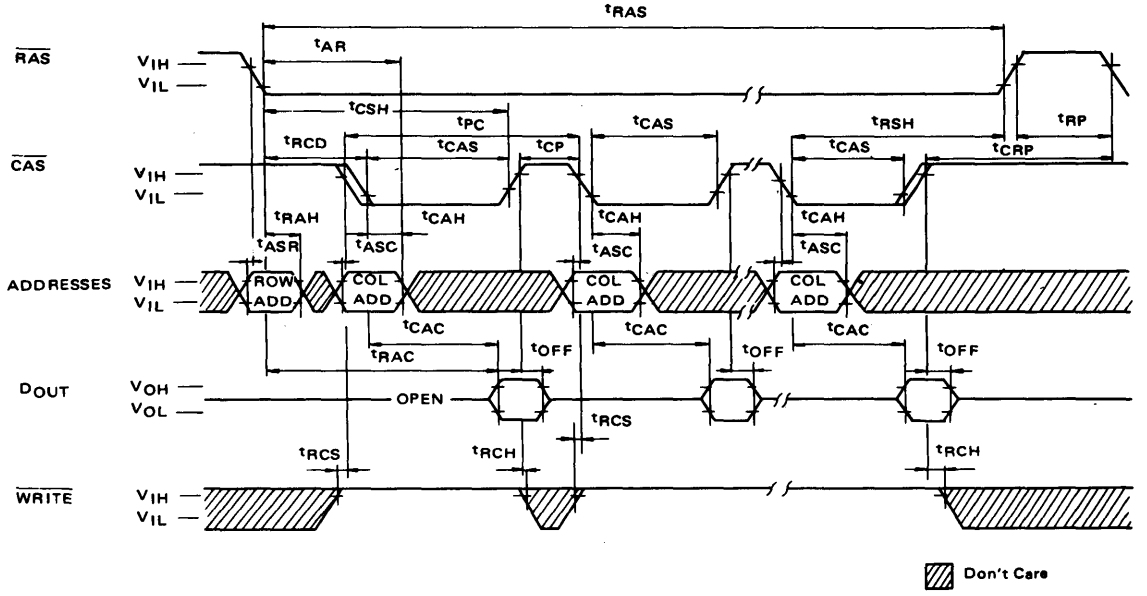


- **"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE**

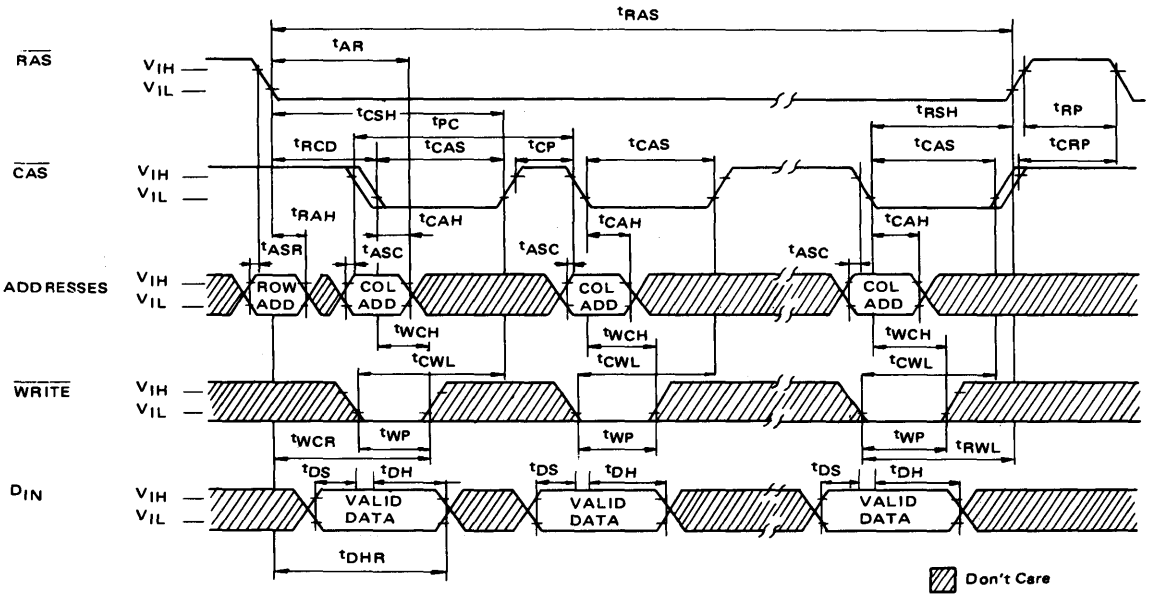


Note: $\overline{\text{CAS}} = V_{IH}$, $\overline{\text{WRITE}}$ = Don't Care, A_7 = Don't Care Don't Care

- **PAGE MODE READ CYCLE**



- **PAGE MODE WRITE CYCLE**



CAPACITANCE

(V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_7$, D_{IN})	—	4	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	—	8	10	pF
C_O	Output Capacitance (D_{OUT})	—	5	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
14. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle:
    If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$ (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM4164AP are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM4164AP is the high impedance (open circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

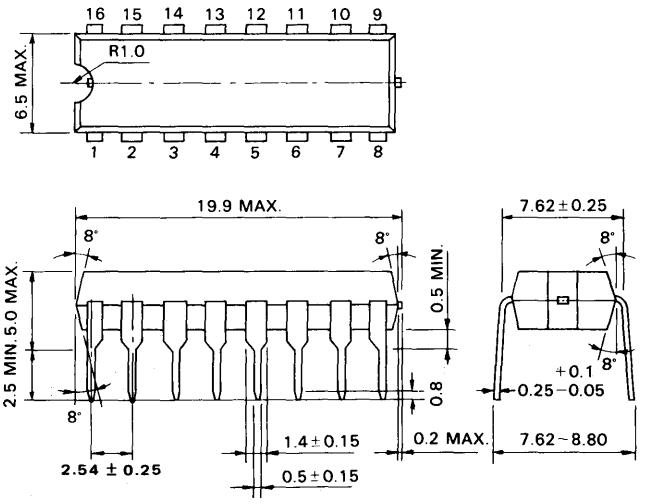
PAGE MODE

The "Page-Mode" feature of the TMM4164AP allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row address ($A_0 \sim A_6$) within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

262,144 WORD × 1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41256P/T-12
TMM41256P/T-15

DESCRIPTION

The TMM41256P/T is the new generation dynamic RAM organized 262,144 words by 1 bit, it is successor to the industry standard TMM4164AP. The TMM41256P/T utilizes TOSHIBA's N-channel Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TMM41256P/T to be packaged in a standard 16 pin plastic DIP and 18 pin plastic leaded chip carrier. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

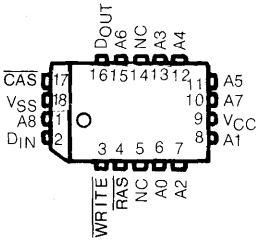
- 262,144 words by 1 bit organization
- Fast access time and cycle time

DEVICE	t_{RAC}	t_{CAC}	t_{RC}
TMM41256P/T-12	120ns	60ns	220ns
TMM41256P/T-15	150ns	75ns	260ns

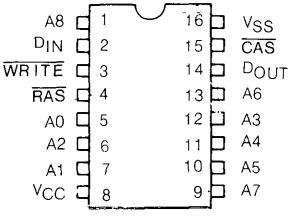
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  330mW MAX. Operating (TMM41256P/T-12)
  275mW MAX. Operating (TMM41256P/T-15)
  28mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh, and Page Mode capability.
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP :TMM41256P
  Plastic Leaded Chip Carrier :TMM41256T

PIN CONNECTION (TOP VIEW)

- Plastic LCC



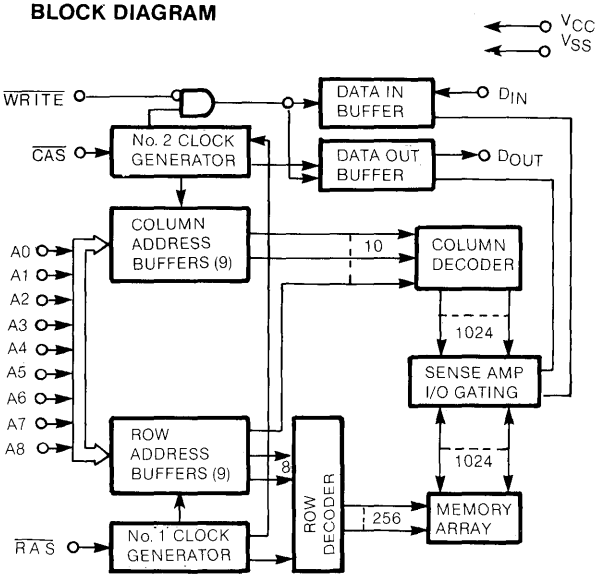
- Plastic DIP



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	1	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	−1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TMM41256P/T-12		60	mA	3,4
		TMM41256P/T-15		50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ =$\overline{CAS}$=V_{IH})			5	mA	
I_{CC3}	REFRESH CURRENT Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC} =t_{RC} MIN.)	TMM41256P/T-12		45	mA	3
		TMM41256P/T-15		40		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=t_{PC} MIN.)	TMM41256P/T-12		45	mA	3,4
		TMM41256P/T-15		40		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≦V_{IN}≦6.5V, All other pins not under test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV≦V_{OUT}≦+5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4		V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41256P/T-12		TMM41256P/T-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	-	260	-	ns	
t_{RWC}	Read-Write Cycle Time	240	-	285	-	ns	
t_{RMW}	Read-Modity-Write Cycle Time	260	-	310	-	ns	
t_{PC}	Page Mode Cycle Time	120	-	145	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	120	-	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	-	60	-	75	ns	9,10
t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6
t_{RP}	$\overline{RAS}$ Precharge Time	90	-	100	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	-	75	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	-	150	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0	-	0	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20	-	25	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	50	-	60	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	35	-	45	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95	-	120	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	15	-	20	-	ns	12
t_{WCH}	Write Command Hold Time	35	-	45	-	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95	-	120	-	ns	
t_{WP}	Write Command Pulse Width	35	-	45	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	-	45	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	-	45	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	ns	14
t_{DH}	Data-In Hold Time	35	-	45	-	ns	14
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95	-	120	-	ns	
t_{REF}	Refresh Period	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	-10	-	-10	-	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	40	-	50	-	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100	-	125	-	ns	15

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

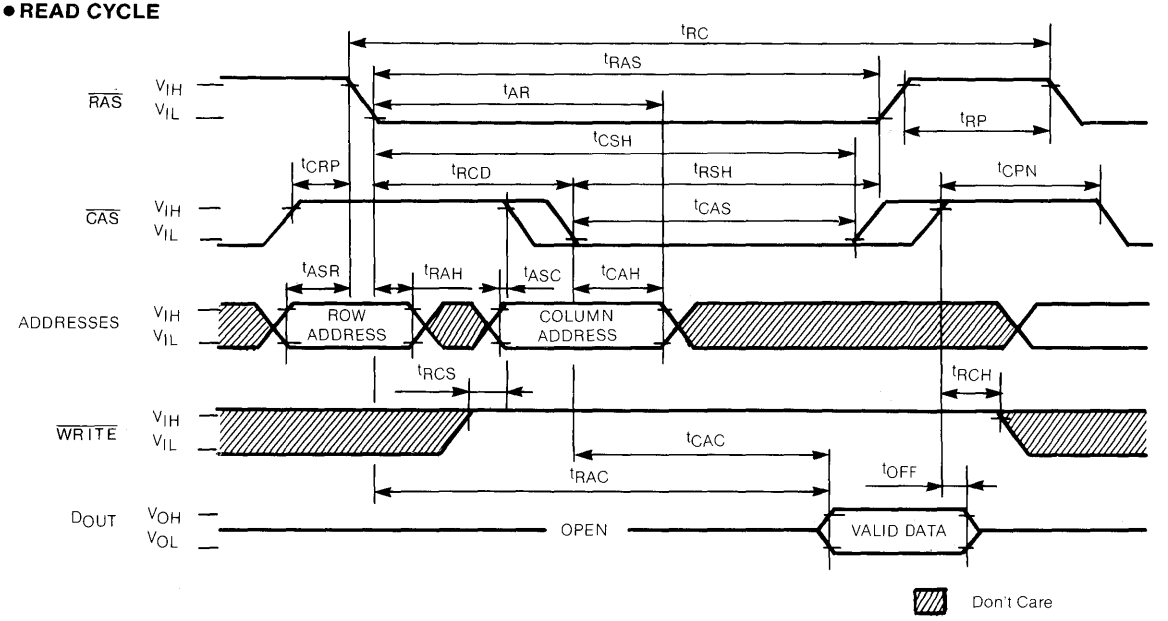
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A0~A8, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

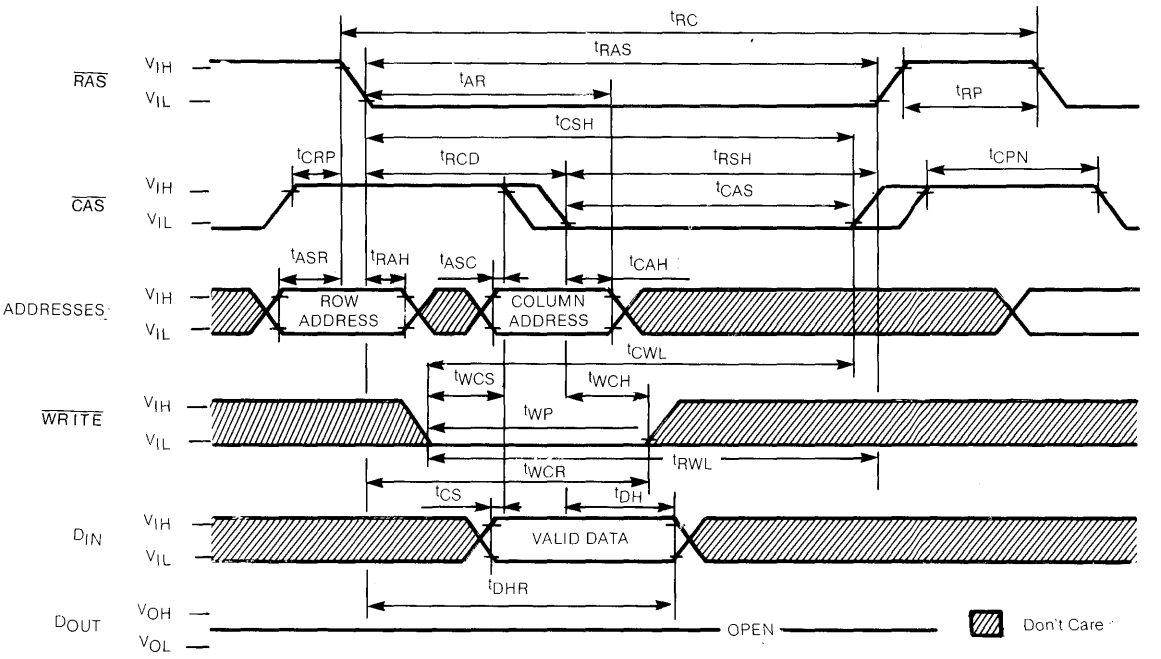
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$(min.) and $t_{RWD} \geqq t_{RWD}$(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

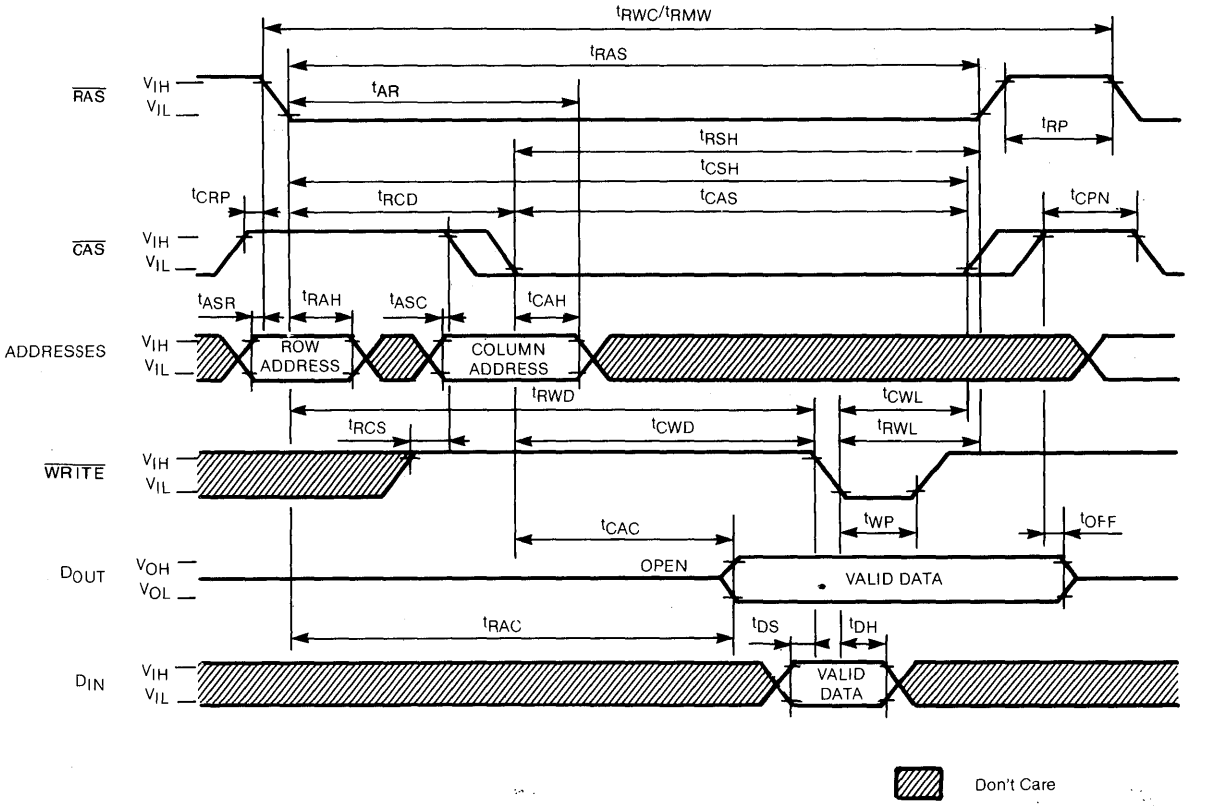
• READ CYCLE



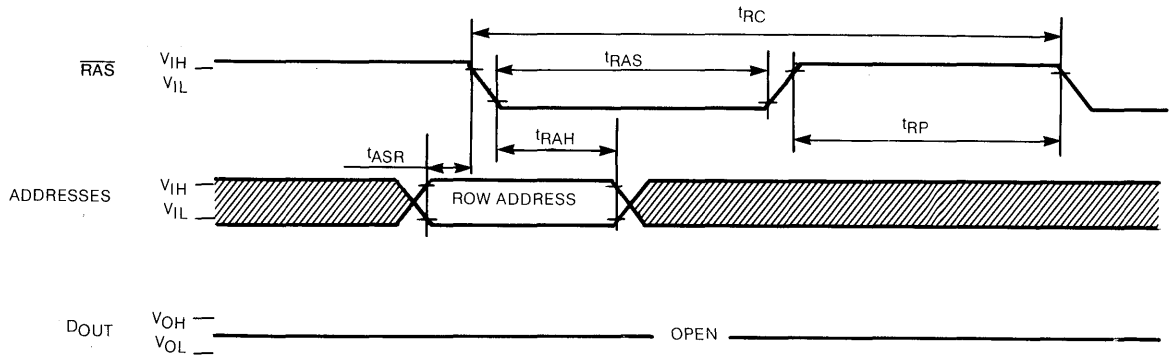
• WRITE CYCLE (EARLY WRITE)



• READ-WRITE/READ-MODIFY-WRITE CYCLE



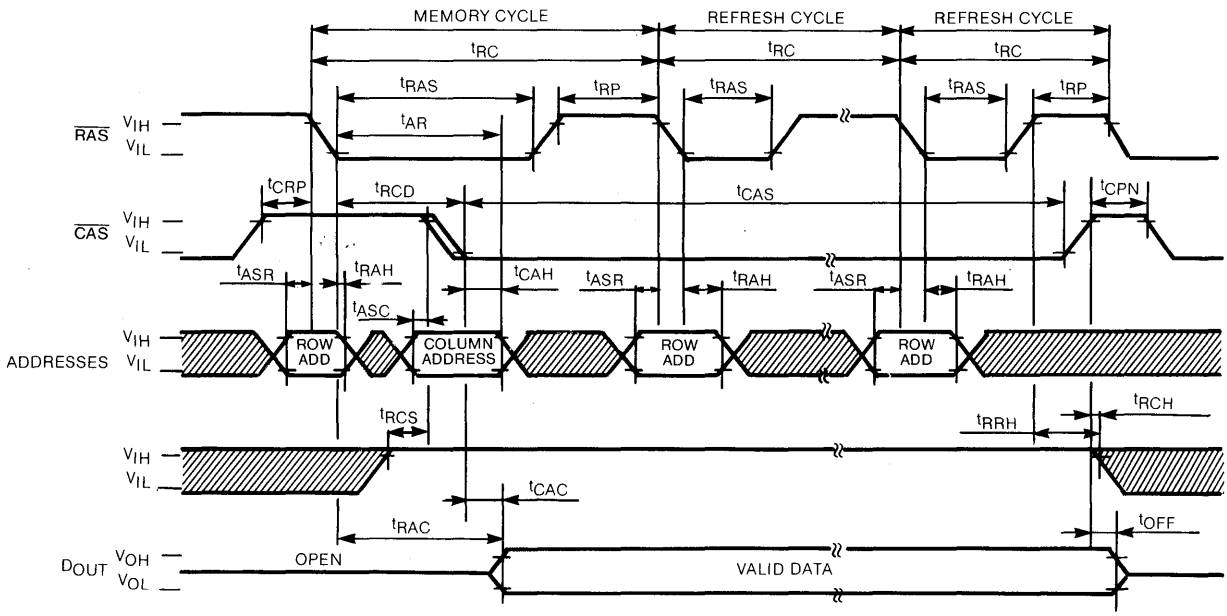
• "$\overline{RAS}$-ONLY" REFRESH CYCLE



Note: $\overline{CAS}$ =V_{IH}, $\overline{WRITE}$ =Don't Care, A_8=Don't Care

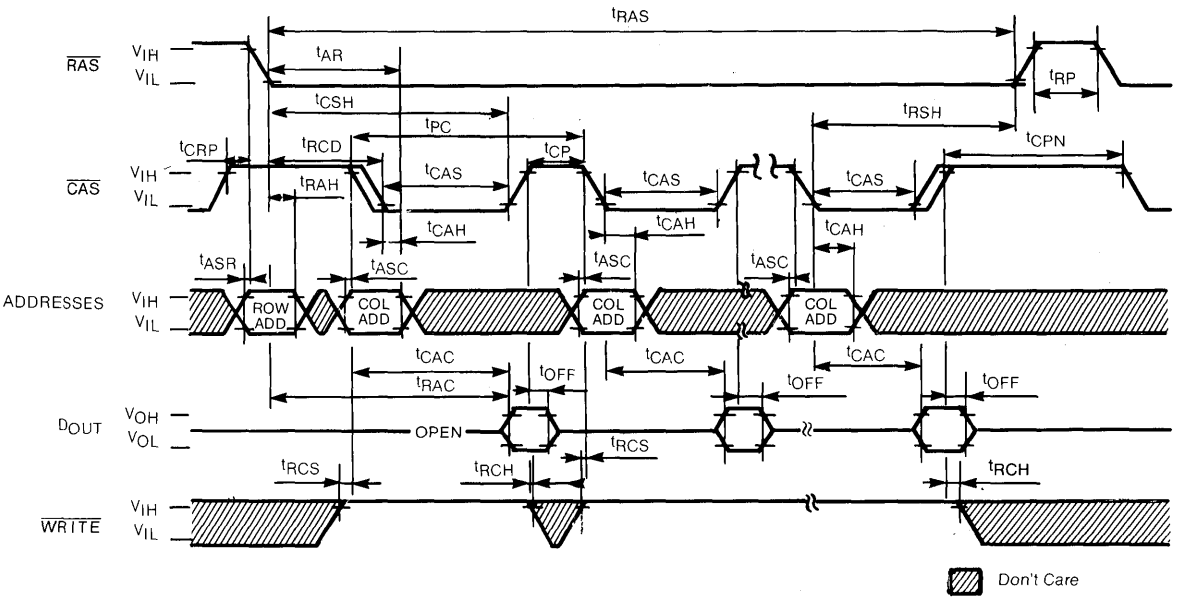
Don't Care

• HIDDEN REFRESH CYCLE

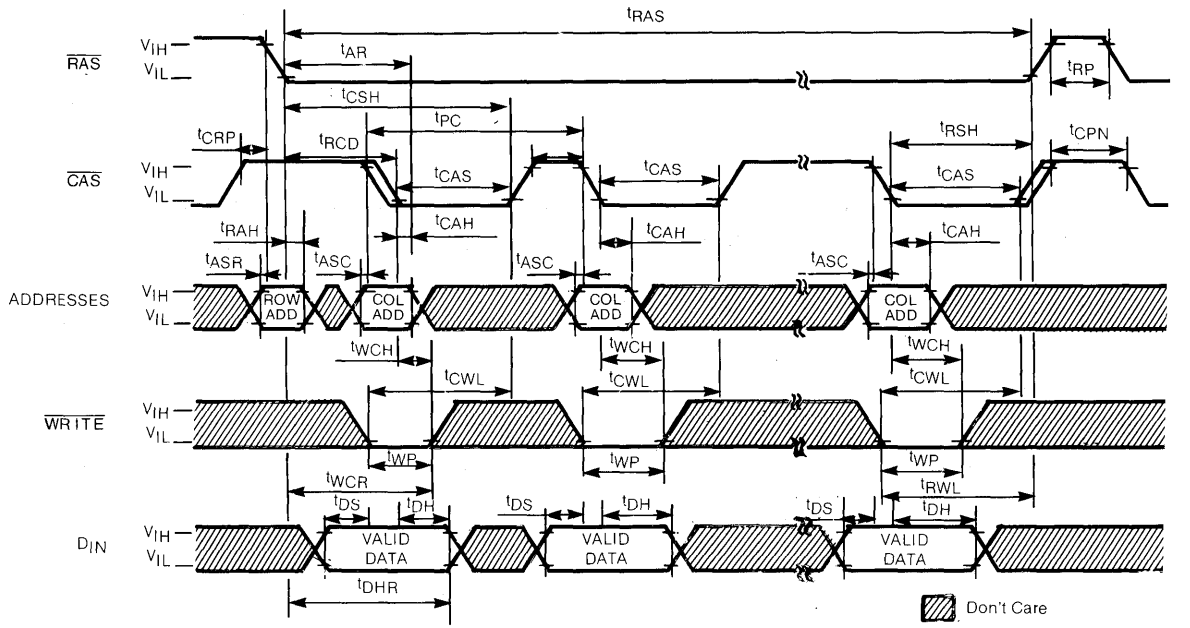


Don't Care

• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256P/T are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256P/T is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

PAGE MODE

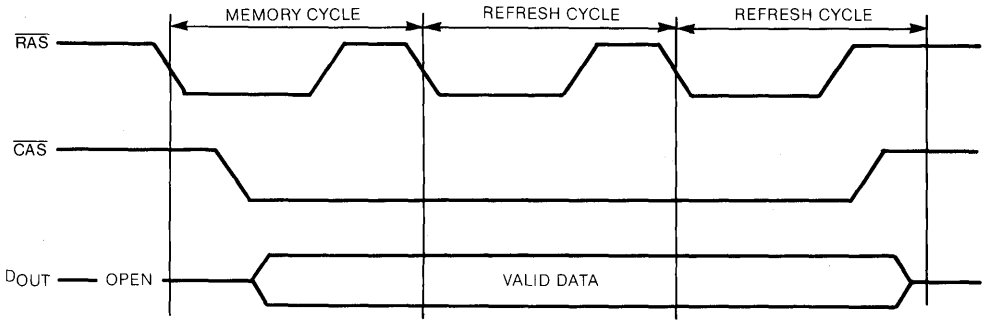
The "Page-Mode" feature of the TMM41256P/T allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. The "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

HIDDEN REFRESH

An optional feature of the TMM41256P/T is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a "$\overline{RAS}$-only" refresh cycle, but with $\overline{CAS}$ held low (see Figure below).

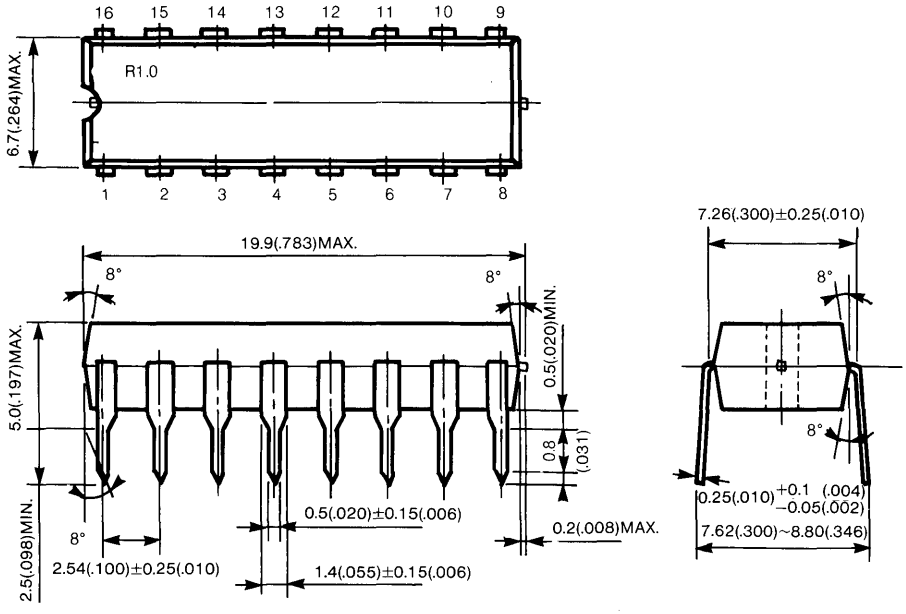


This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

OUTLINE DRAWINGS

- **Plastic Dip**

Unit in mm (inches)



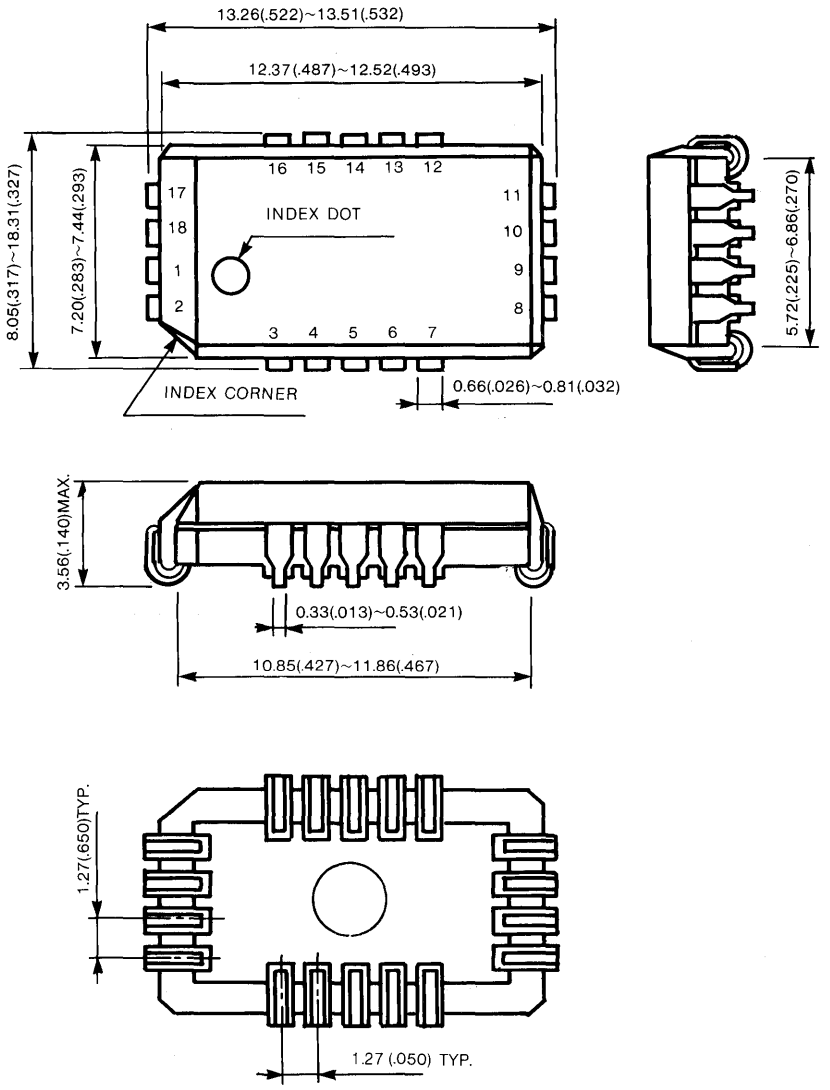
Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.16 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TMM41256P/T-12
TMM41256P/T-15

- **Plastic LCC**

Unit in mm (inches)



262,144 WORD × 1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41257P/T-12
TMM41257P/T-15

DESCRIPTION

The TMM41257P/T is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41257P/T to be packaged in a standard 16 pin plastic DIP and 18 pin plastic leaded chip carrier. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41257P/T high speed operation. Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the $\overline{RAS}$ only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of TMM41257P/T is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

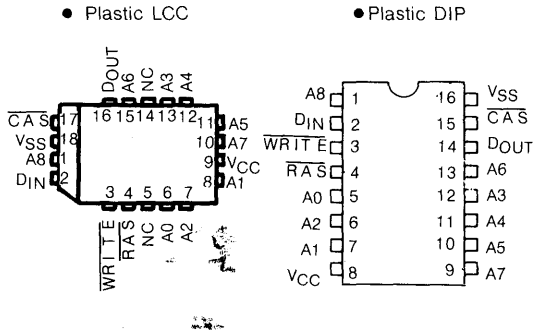
FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41257P/T-12	TMM41257P/T-15
$\overline{RAS}$ Access Time	120ns	150ns
$\overline{CAS}$ Access Time	60ns	75ns
Cycle Time	220ns	260ns
Nibble Mode Access Time	30ns	40ns
Nibble Mode Cycle Time	55ns	70ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  385mW MAX. Operating (TMM41257P/T-12)
  330mW MAX. Operating (TMM41257P/T-15)
  28mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Nibble Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP :TMM41257P
  Plastic Leaded Chip Carrier :TMM41257T

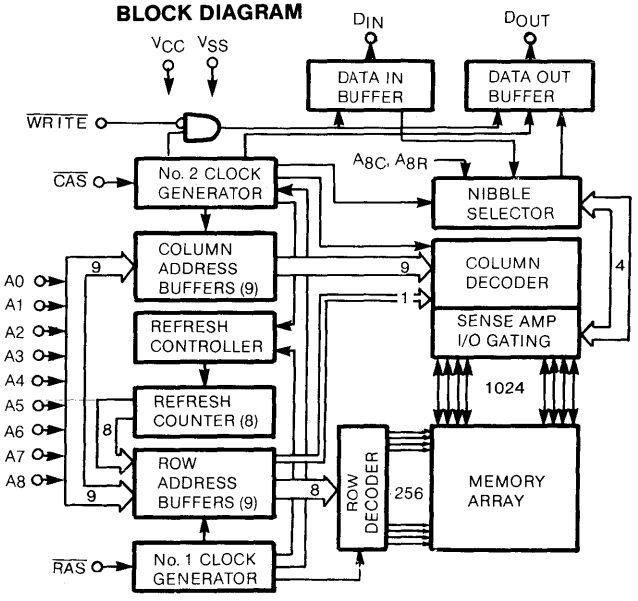
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	−1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TMM41257P/T-12	-	70	mA	3,4
		TMM41257P/T-15	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TMM41257P/T-12	-	60	mA	3
		TMM41257P/T-15	-	50		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	TMM41257P/T-12	-	40	mA	3,4
		TMM41257P/T-15	-	30		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC}=t_{RC} MIN.)	TMM41257P/T-12	-	60	mA	3
		TMM41257P/T-15	-	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≦V_{IN}≦6.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV≦V_{OUT}≦+5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4		V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41257P/T-12		TMM41257P/T-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	-	260	-	ns	
t_{RWC}	Read-Write Cycle Time	240	-	285	-	ns	
t_{RMW}	Read-Modity-Write Cycle Time	260	-	310	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	120	-	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	-	60	-	75	ns	9,10
t_{OFF}	Output Buffer Turn-Off Delay	5	30	5	35	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	90	-	100	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	-	75	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	-	150	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20	-	25	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	25	-	30	-	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	85	-	105	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	15	-	20	-	ns	12
t_{WCH}	Write Command Hold Time	25	-	30	-	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	85	-	105	-	ns	
t_{WP}	Write Command Pulse Width	25	-	30	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	-	45	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	-	45	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	ns	14
t_{DH}	Data-In Hold Time	25	-	30	-	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	85	-	105	-	ns	
t_{REF}	Refresh Period	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	40	-	50	-	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100	-	125	-	ns	15
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	-	60	-	ns	
t_{NC}	Nibble Mode Cycle Time	55	-	70	-	ns	
t_{NCAC}	Nibble Mode Access Time	-	30	-	40	ns	10
t_{NCAS}	Nibble Mode Pulse Width	30	-	40	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	15	-	20	-	ns	
t_{NRRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Read)	25	-	30	-	ns	
t_{NWRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Write)	45	-	50	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to WRITE Delay Time	30	-	40	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Read Time	25	-	30	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

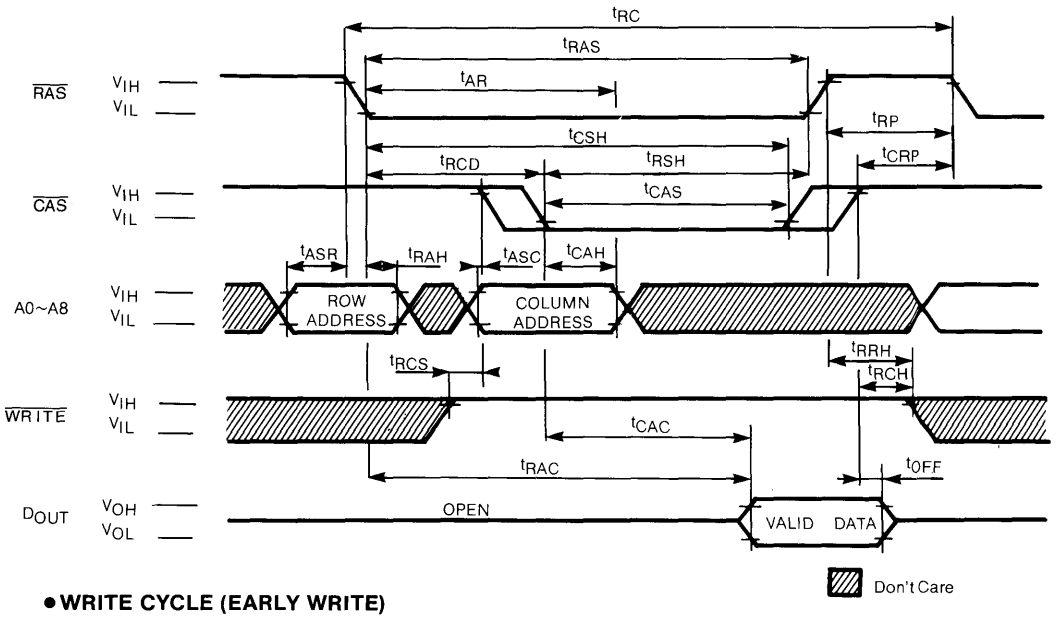
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A_0~A_8, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

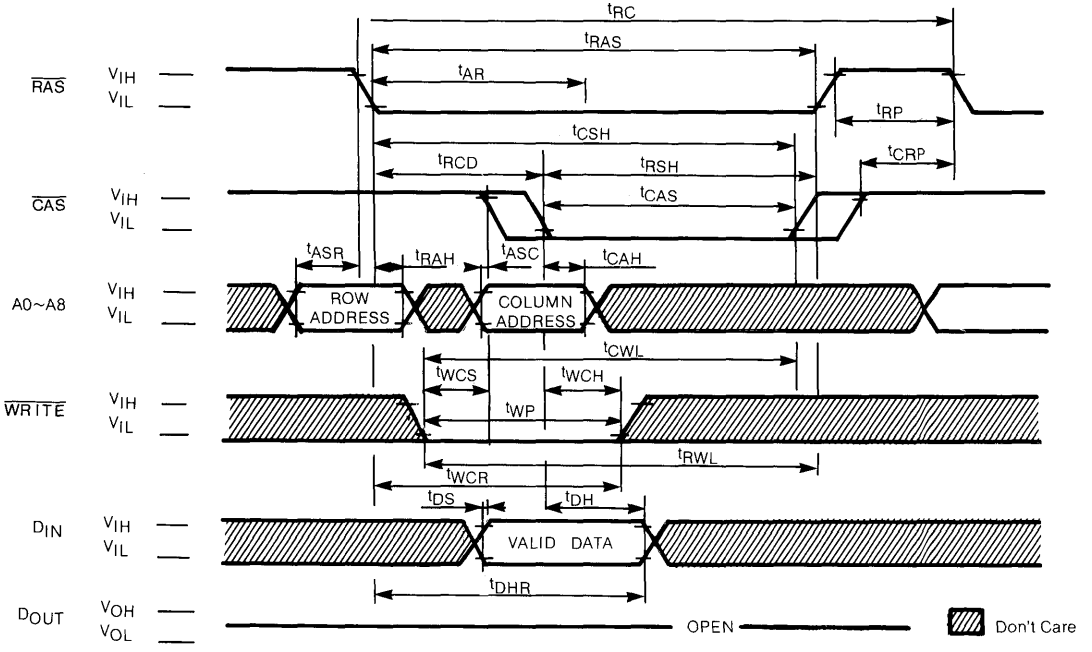
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$(min.) and $t_{RWD} \geqq t_{RWD}$(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

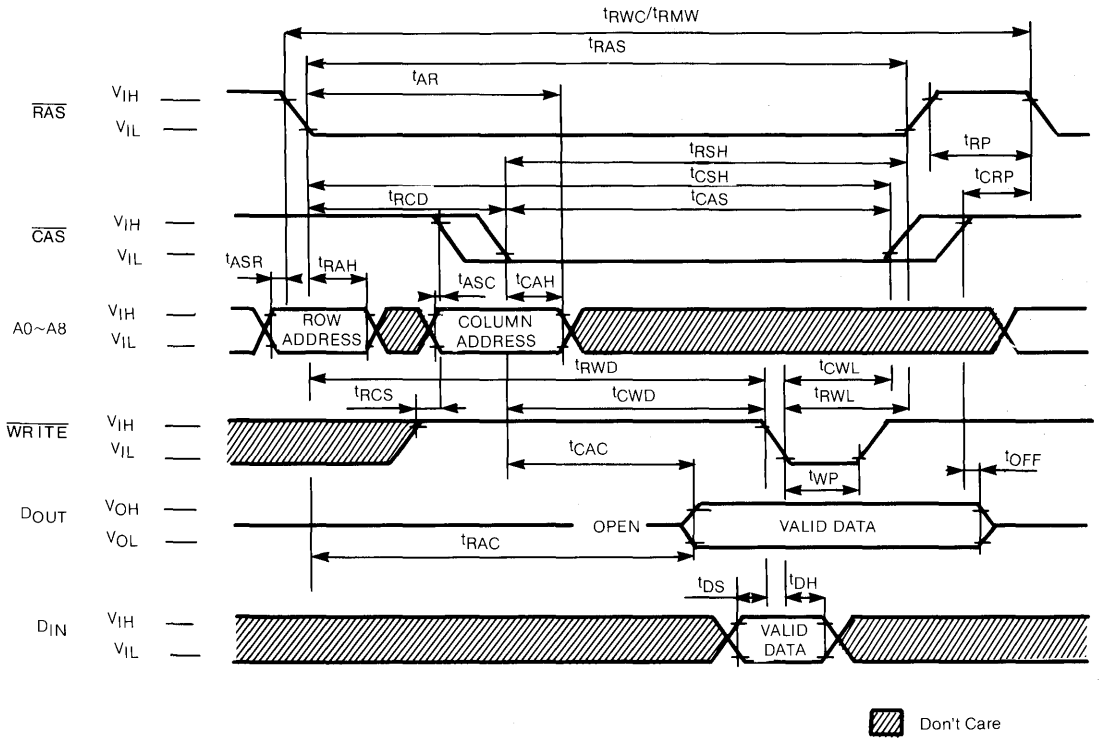
• READ CYCLE



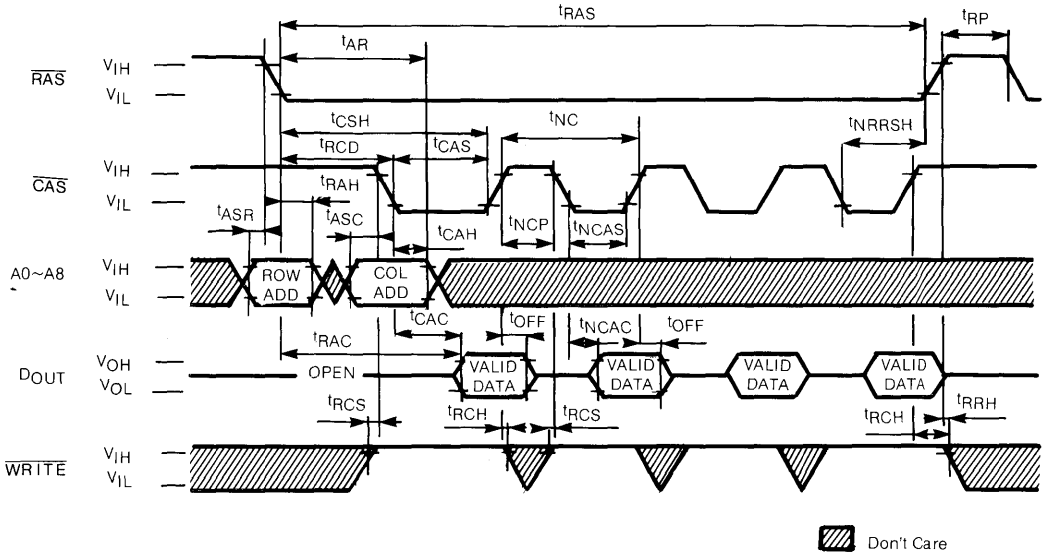
• WRITE CYCLE (EARLY WRITE)



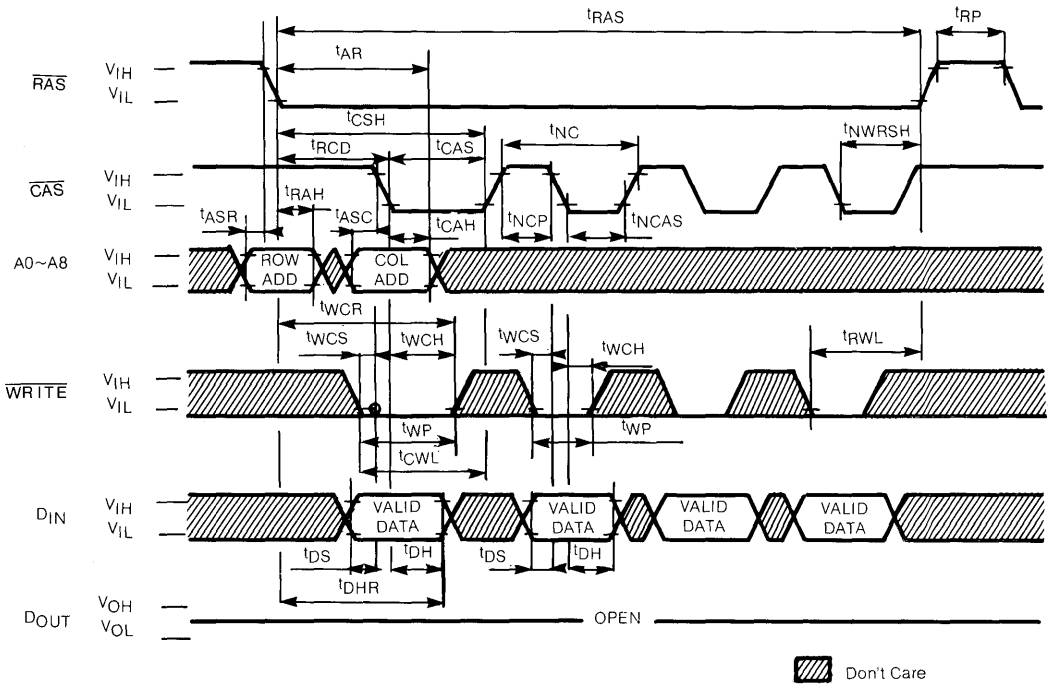
• READ-WRITE/READ-MODIFY-WRITE CYCLE



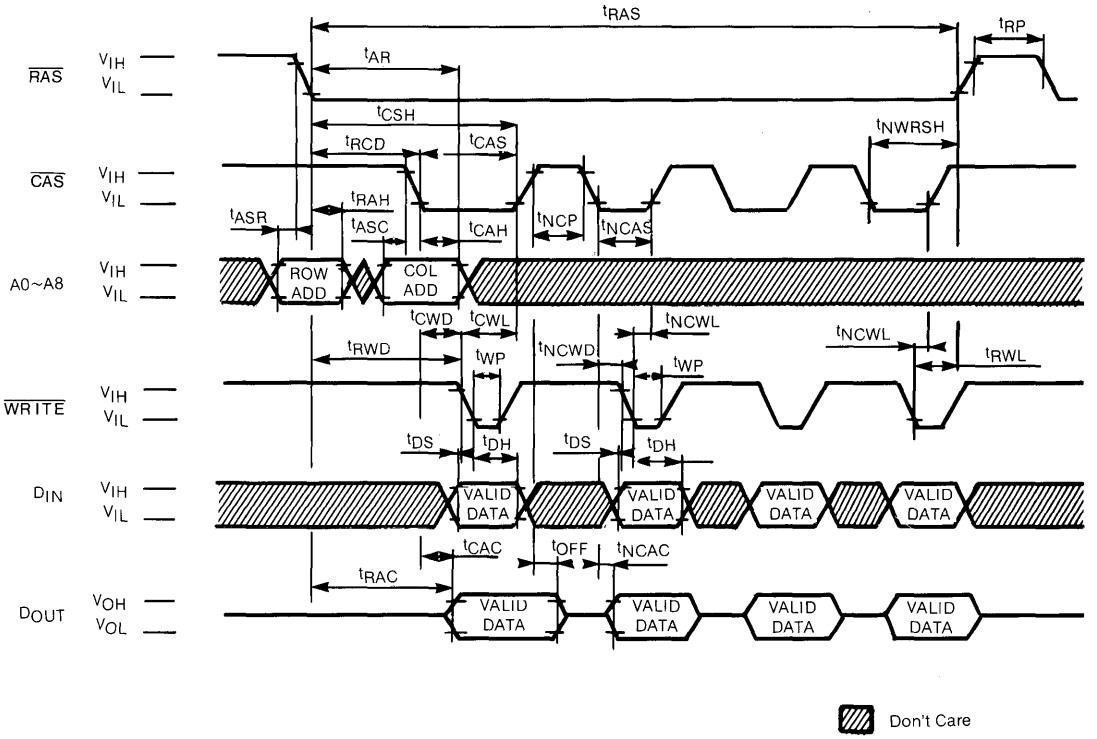
• NIBBLE MODE READ CYCLE



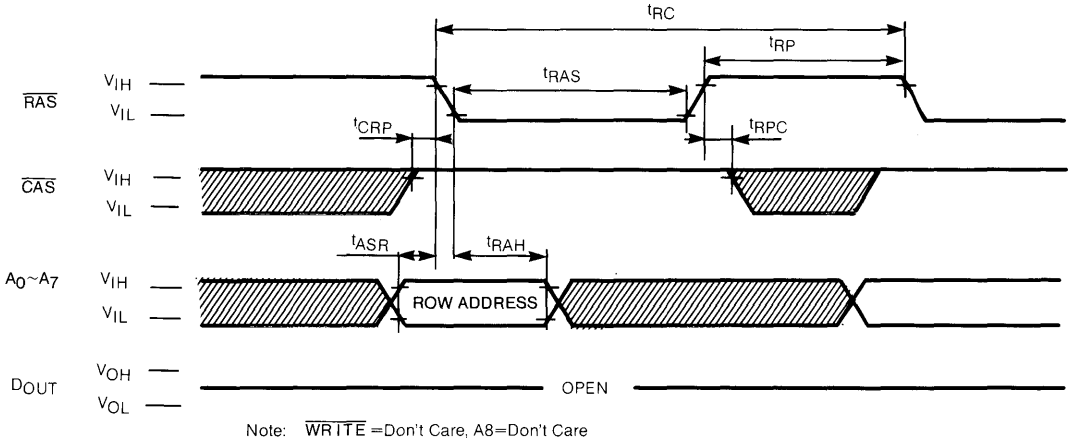
• NIBBLE MODE WRITE CYCLE



• NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



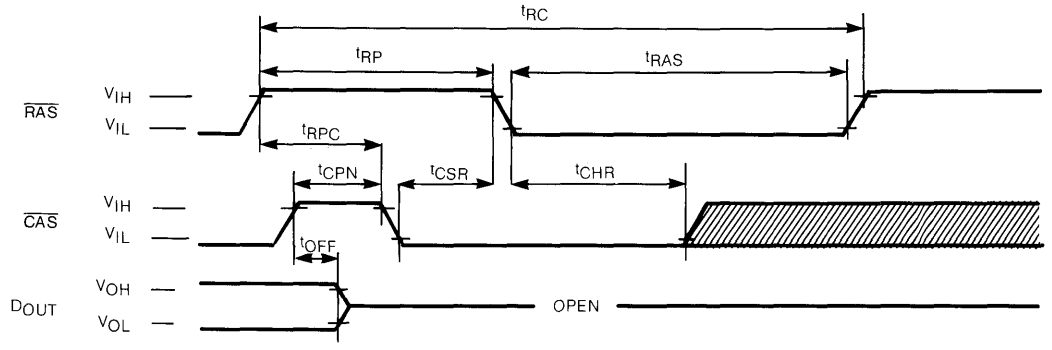
• $\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ =Don't Care, A8=Don't Care

Don't Care

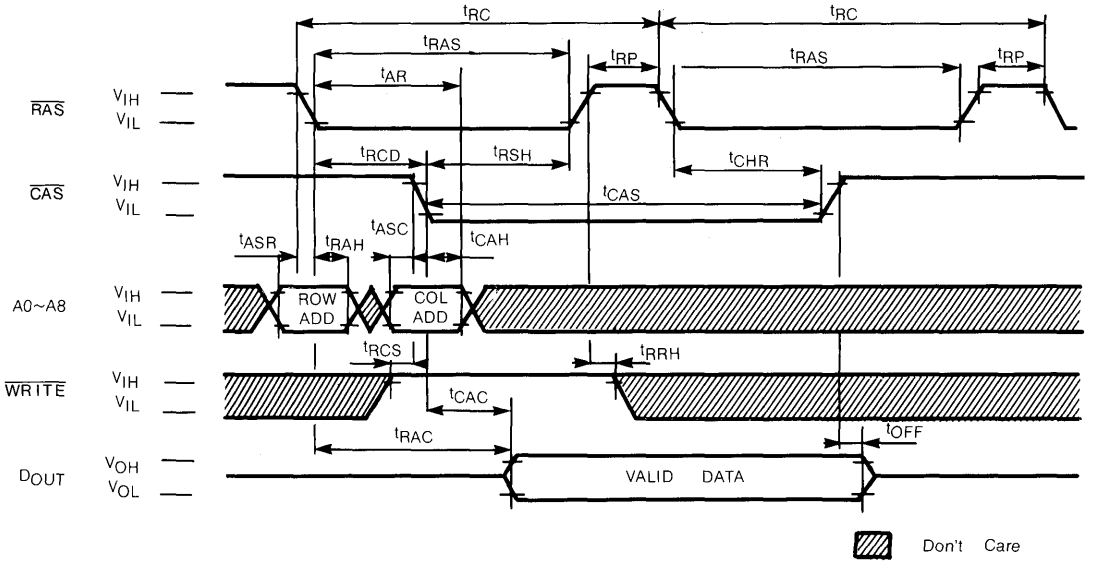
• $\overline{CAS}$ BEFORE $\overline{RAS}$ CYCLE



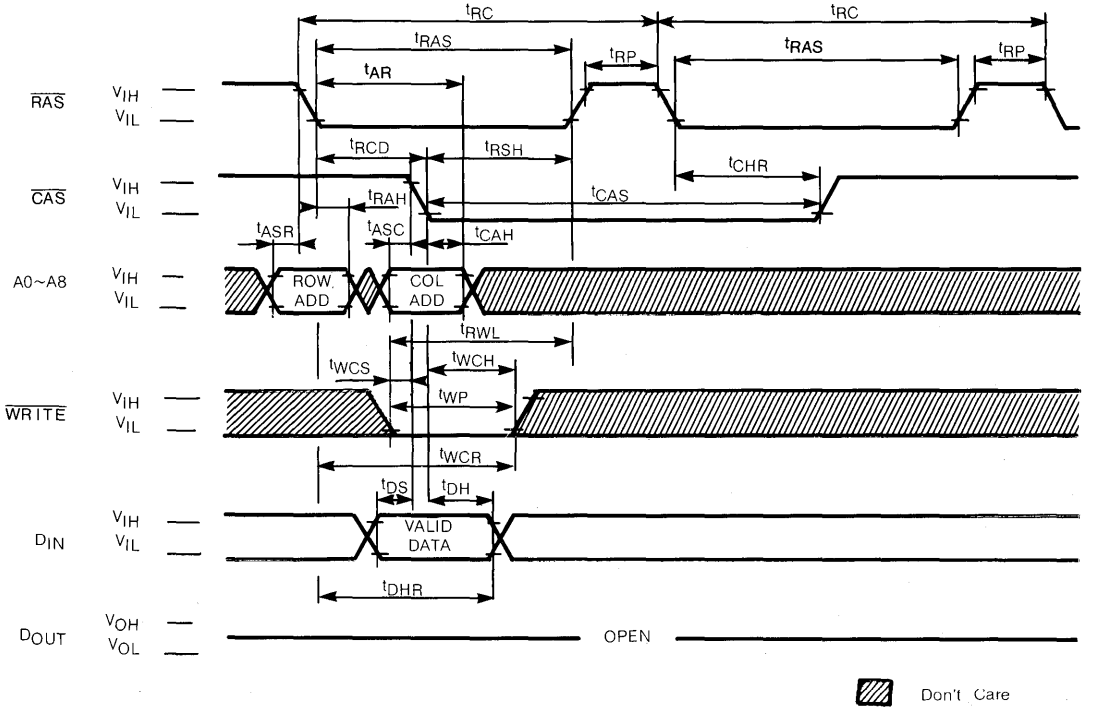
Note: $\overline{WRITE}$ =Don't Care, A0~A8=Don't Care

Don't Care

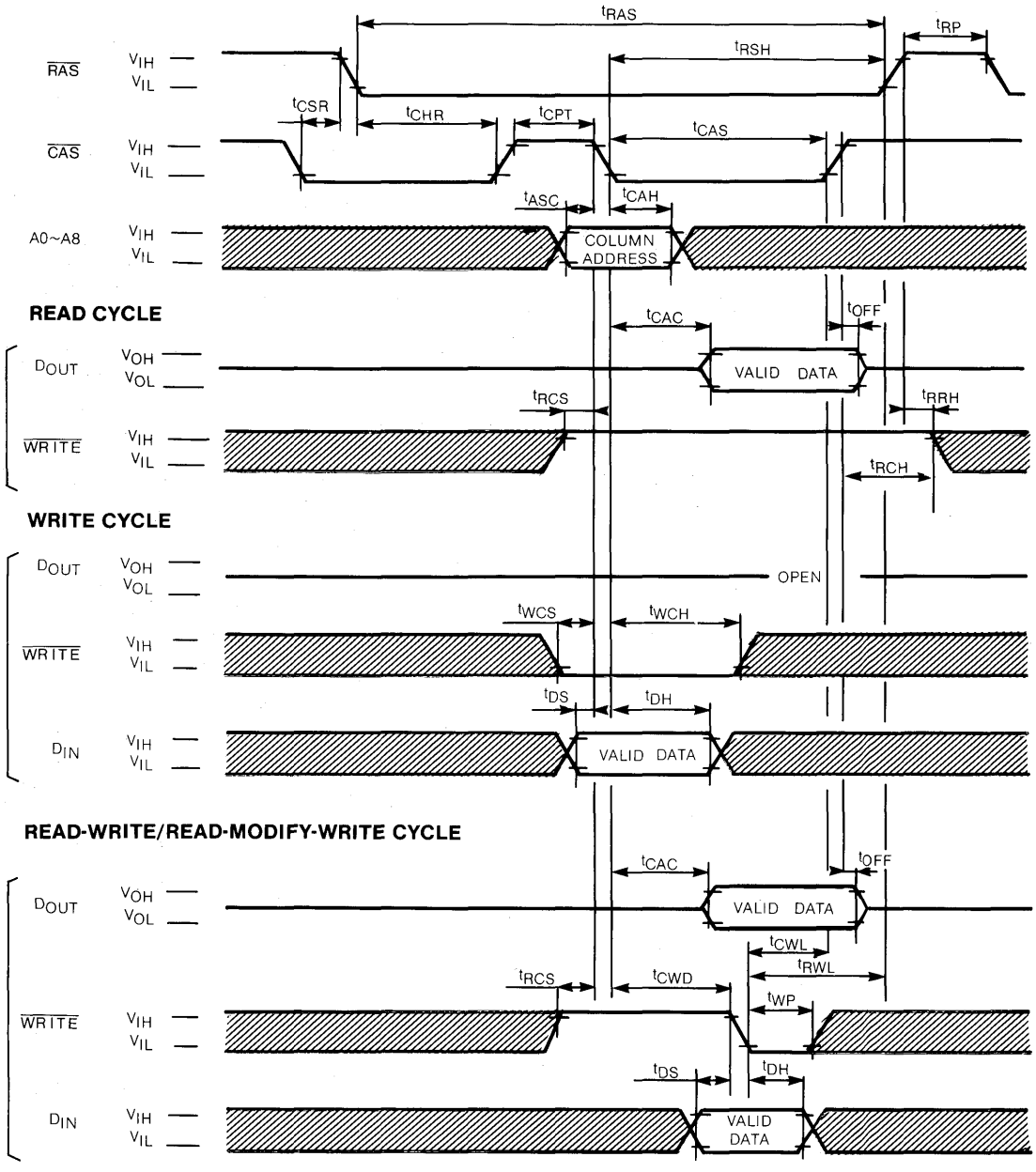
• HIDDEN REFRESH CYCLE (READ)



• HIDDEN REFRESH CYCLE (WRITE)



• $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41257P/T are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$ " feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

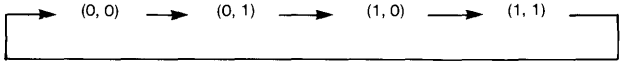
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41257P/T is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at a high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A_8) determines the starting point of the circular 4 bits nibble. Row A_8 and column A_8 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A_8 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

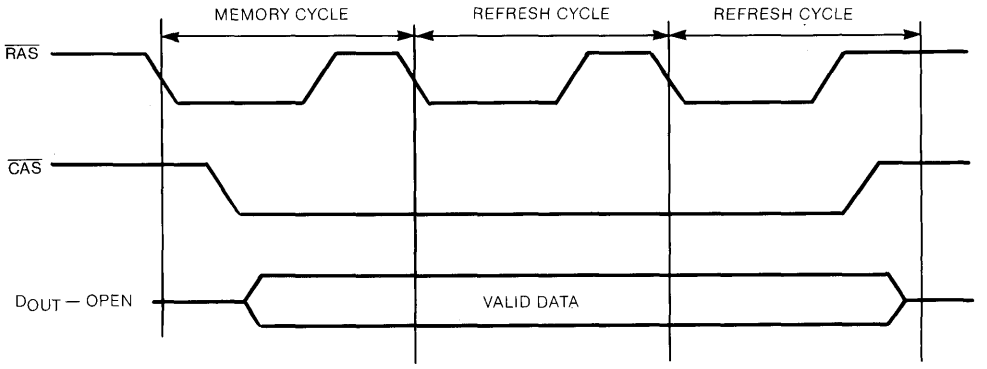
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A_0~A_7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results is a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on the TMM41257P/T offers an alternate refresh method. If $\overline{\text{CAS}}$ is held on low for the specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41257P/T is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41257P/T can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as intialization cycles. The test procedure is as follows.

(1) Write "0" into all the memory cells at normal write mode.

(2) Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.

(3) Check "1" out of 256 bits at normal read mode, which was written at (2).

(4) Using the same column as (2), read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. Repeat this operation 256 times.

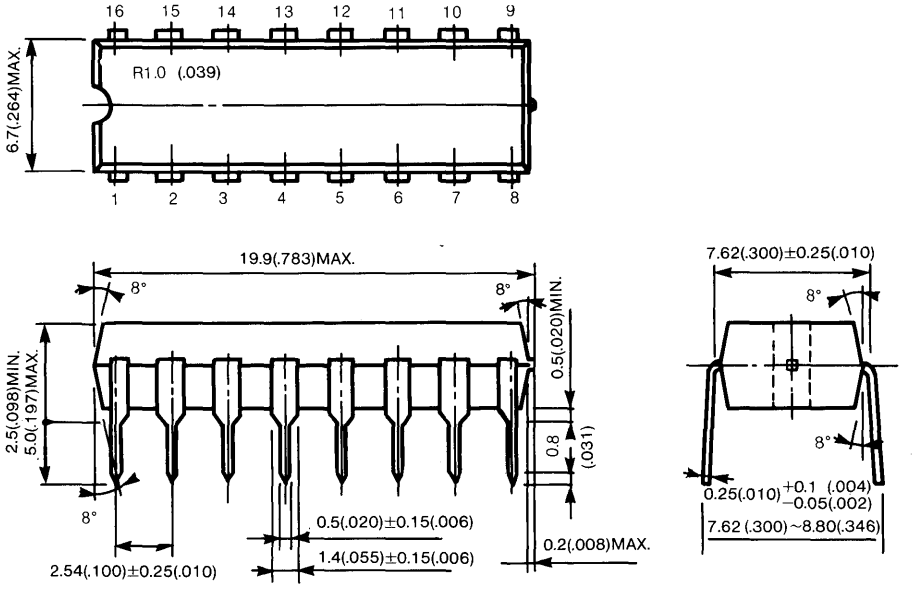
(5) Check "0" out of 256 bits at normal read mode, which was written at (4).

(6) Perform the above (1) to (5) with the complement data.

OUTLINE DRAWINGS

- **Plastic Dip**

Unit in mm (inches)

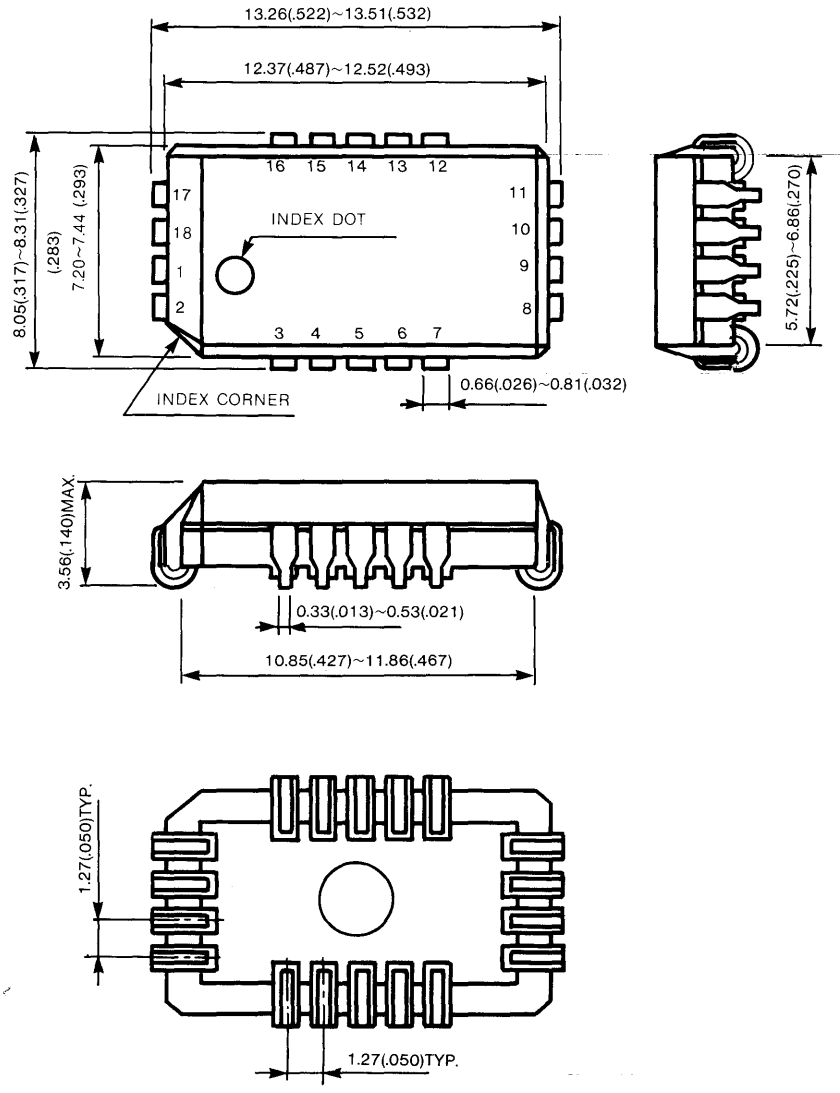


Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.16 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

- **Plastic LCC**

Unit in mm (inches)



TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 4 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41464P-12
TMM41464P-15

DESCRIPTION

The TMM41464P is the new generation dynamic RAM organized 65,536 word by 4 bit, it is successor to the industry standard TMM4164AP.

The TMM41464P utilizes TOSHIBA's N-channel/ Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM 41464P to be packaged in a standard 18 pin plastic DIP. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as schottky TTL.

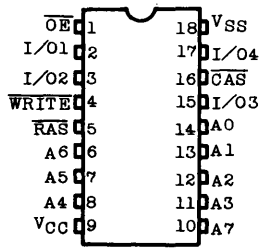
FEATURES

- 65,536 words by 4 bit organization
- Fast access Time and cycle time

DEVICE	t_{RAC}	t_{CAC}	t_{RC}
TMM41464P-12	120ns	60ns	220ns
TMM41464P-15	150ns	75ns	260ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low power:
  385mW Operating (MAX.) (TMM41464-12)
  330mW Operating (MAX.) (TMM41464-15)
  28mW Standby (MAX.)
- Industory standard 18 pin plastic DIP
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{RAS}$ only refresh, Hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and Page Mode capability.
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms

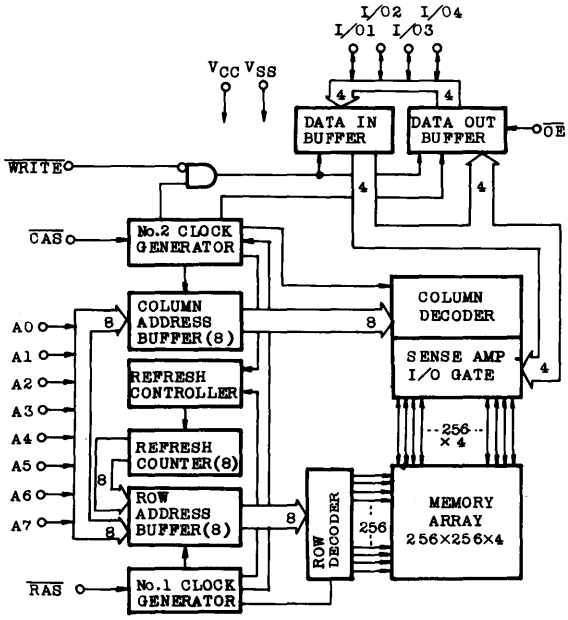
PIN CONNECTION



PIN NAMES

A_0~A_7	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O_1~I/O_4	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling : t_{RC}=t_{RC} MIN.)	TMM41464P-12	—	70	mA	3,4
		TMM41464P-15	—	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		—	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH} : t_{RC}=t_{RC} MIN.)	TMM41464P-12	—	60	mA	3
		TMM41464P-15	—	50		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling : t_{PC}=t_{PC} MIN.)	TMM41464P-12	—	60	mA	3,4
		TMM41464P-15	—	50		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC}=t_{RC} MIN.)	TMM41464P-12	—	60	mA	3
		TMM41464P-15	—	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test =0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦+5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4		V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41464P-12		TMM41464P-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	220	—	260	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	295	—	355	—	ns	
t_{PC}	Page Mode Cycle Time	120	—	145	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	120	—	150	ns	8,10
t_{CAC}	Access Time from $\overline{CAS}$	—	60	—	75	ns	9,10
t_{OFF}	Output Buffer Turn-Off Delay	0	35	0	40	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	90	—	100	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	60	—	75	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120	—	150	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20	—	25	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	50	—	60	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	25	—	35	—	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	85	—	110	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	—	0	—	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	15	—	20	—	ns	12
t_{WCH}	Write Command Hold Time	35	—	45	—	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{WP}	Write Command Pulse Width	35	—	45	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	35	—	45	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	35	—	45	—	ns	
t_{DS}	Data-In Set-Up Time	0	—	0	—	ns	14
t_{DH}	Data-In Hold Time	35	—	45	—	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	95	—	120	—	ns	
t_{REF}	Refresh Period	—	4	—	4	ms	
t_{WCS}	Write Command Set-Up Time	0	—	0	—	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	100	—	120	—	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	160	—	195	—	ns	15
t_{OEA}	$\overline{OE}$ Access time	—	30	—	40	ns	
t_{OED}	$\overline{OE}$ to Data Delay	30	—	40	—	ns	
t_{OEZ}	Output Buffer Turn-Off Delay Time from $\overline{OE}$	0	30	0	40	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	30	—	40	—	ns	

SYMBOL	PARAMETER	TMM41464P-12		TMM41464P-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	30	—	30	—	ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	10	—	10	—	ns	
t_{RPC}	$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	0	—	0	—	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	50	—	60	—	ns	

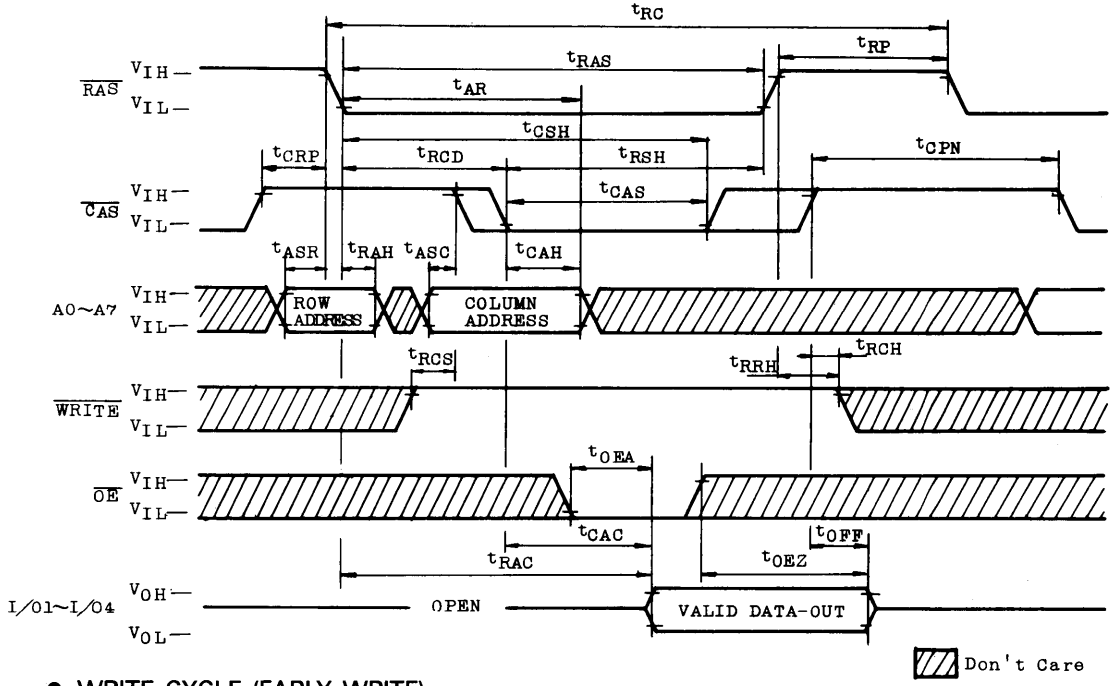
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A_0~A_7)	—	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	—	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	—	7	pF

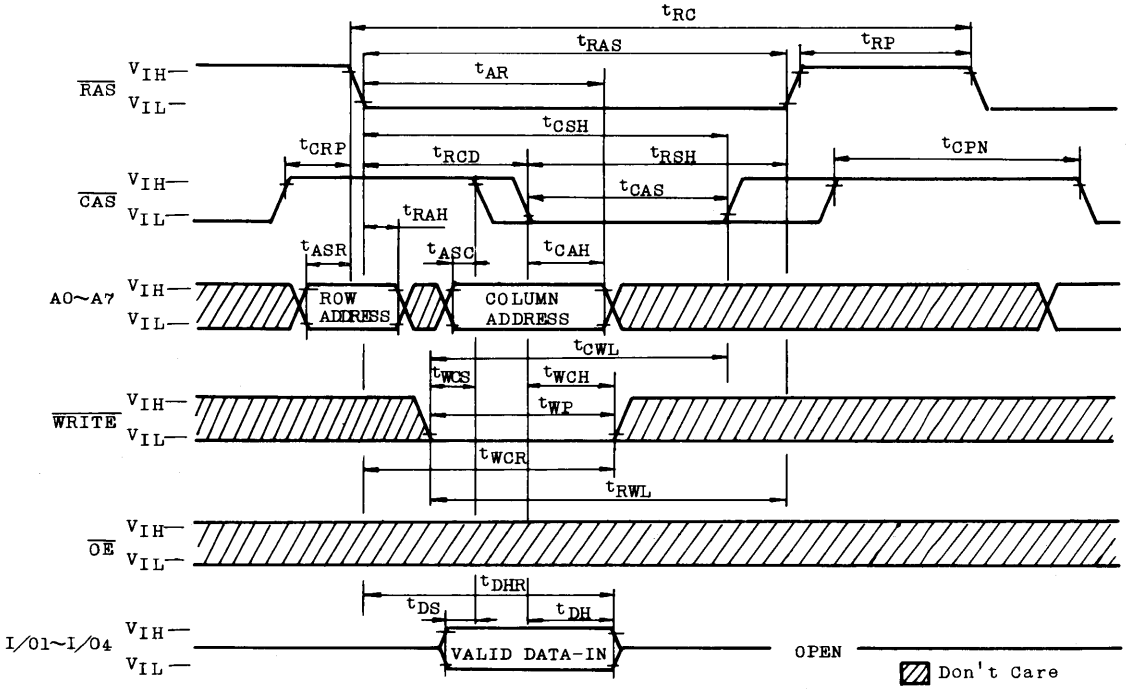
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are refrenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{CAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimun of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycle are required.
6. AC measurements assume t_T =5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TLL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These paramenters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the input/output pin will remain open circuits (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{RWD} \geqq t_{RWD}$(min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell.

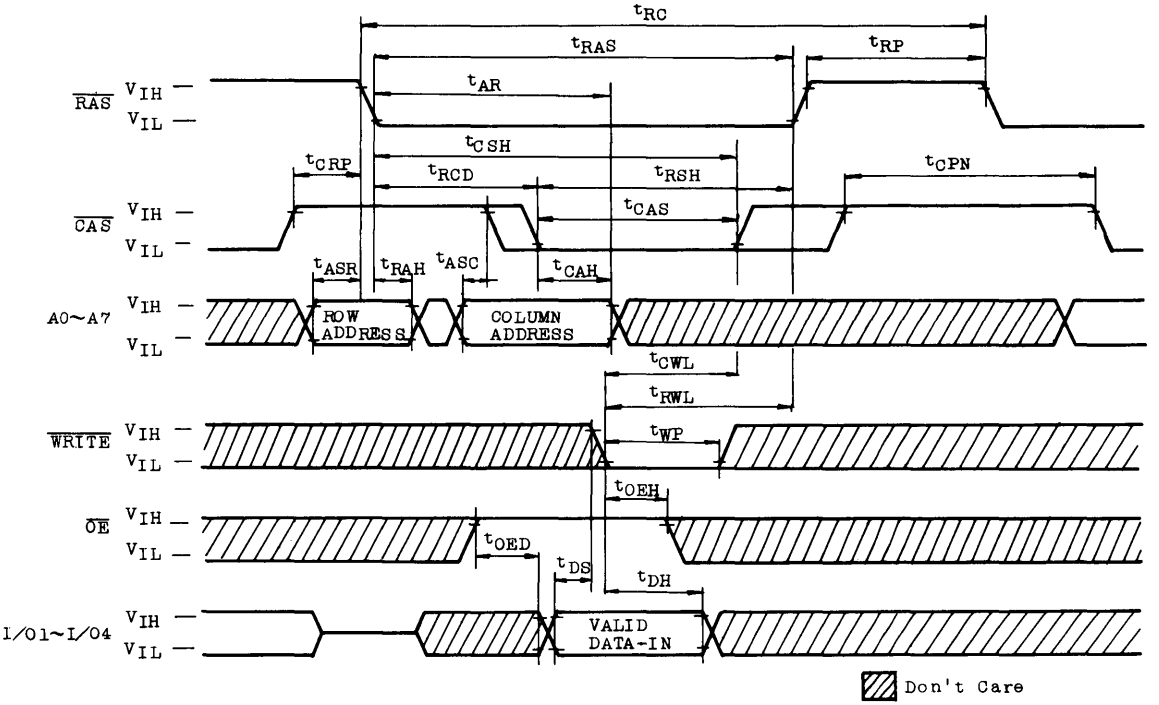
● READ CYCLE



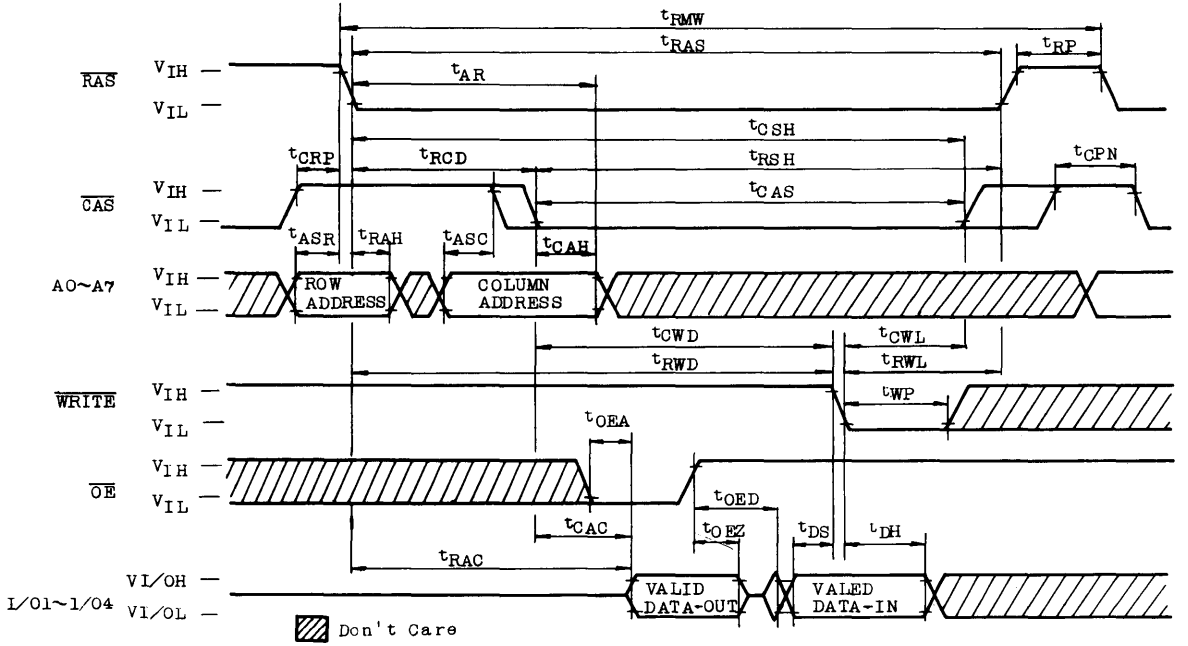
● WRITE CYCLE (EARLY WRITE)



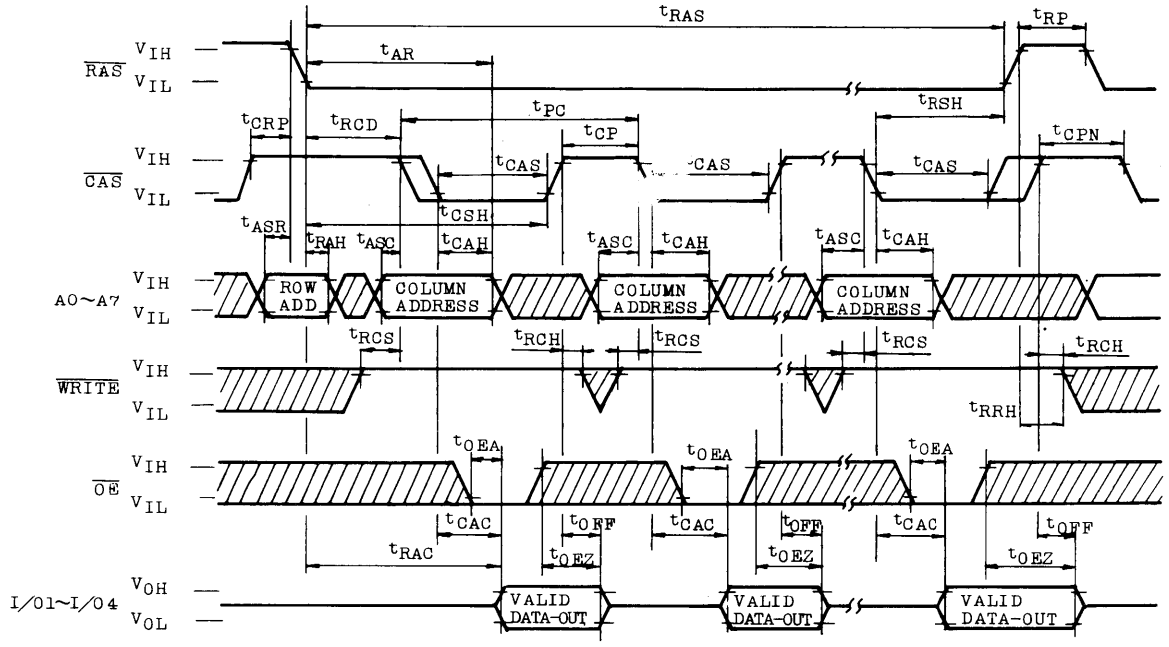
● WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



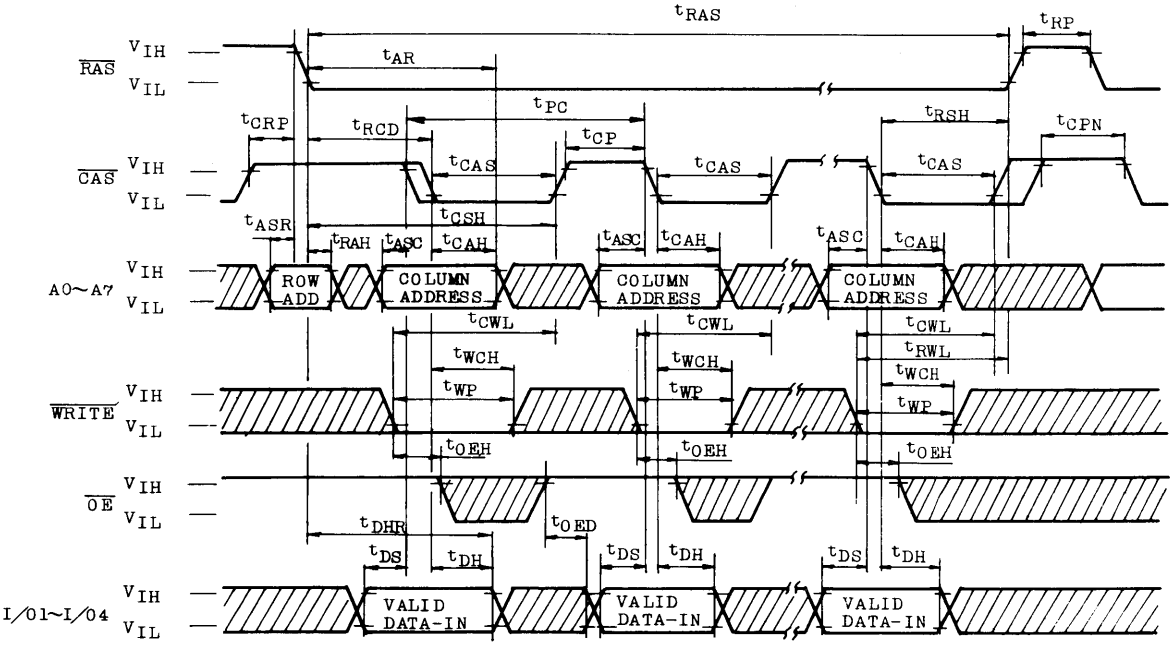
● READ-WRITE/READ-MODIFY-WRITE CYCLE



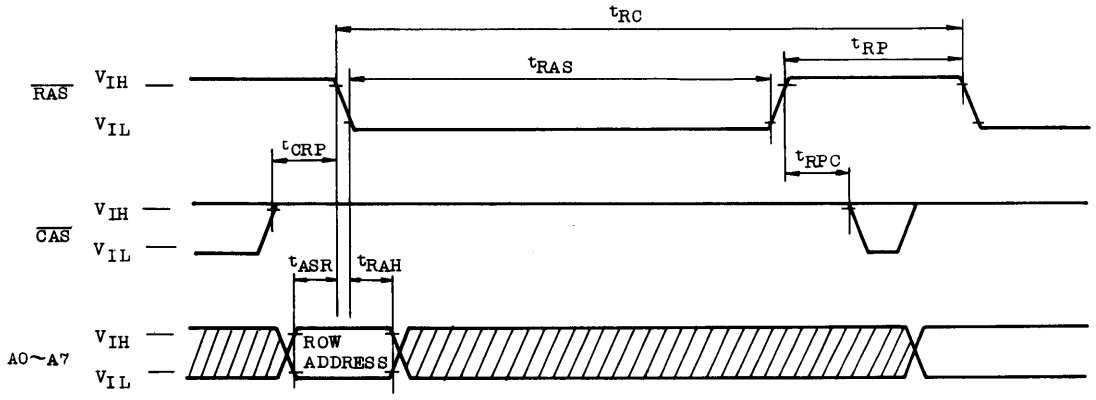
● PAGE MODE READ CYCLE



● PAGE MODE WRITE CYCLE



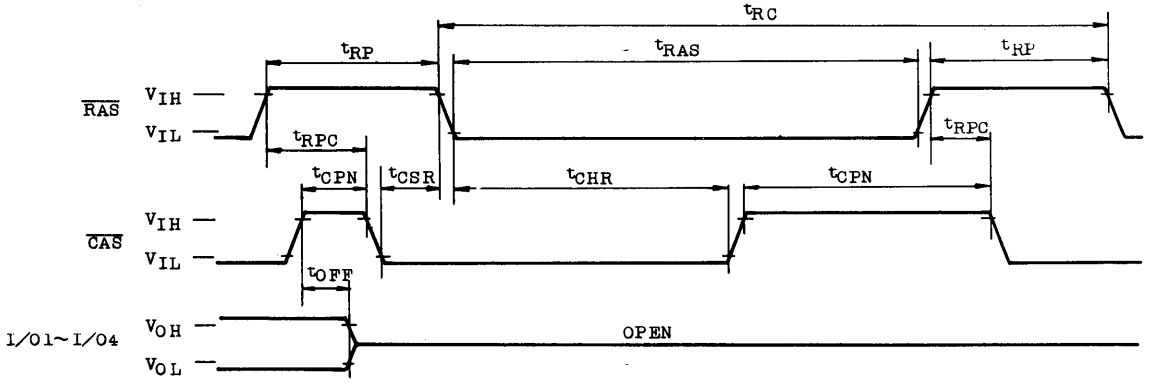
- $\overline{RAS}$ ONLY REFRESH CYCLE



Notes: $\overline{WRITE}$, $\overline{OE}$=Don't Care

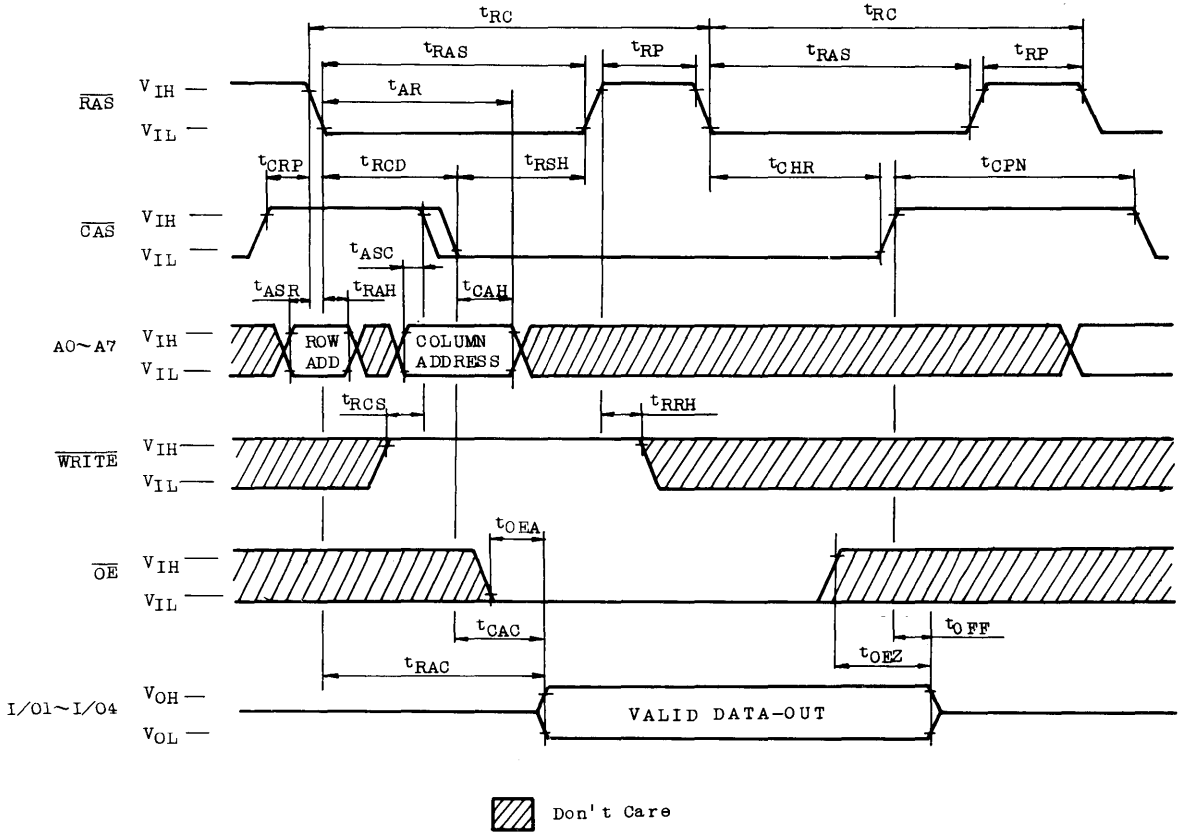
Don't Care

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

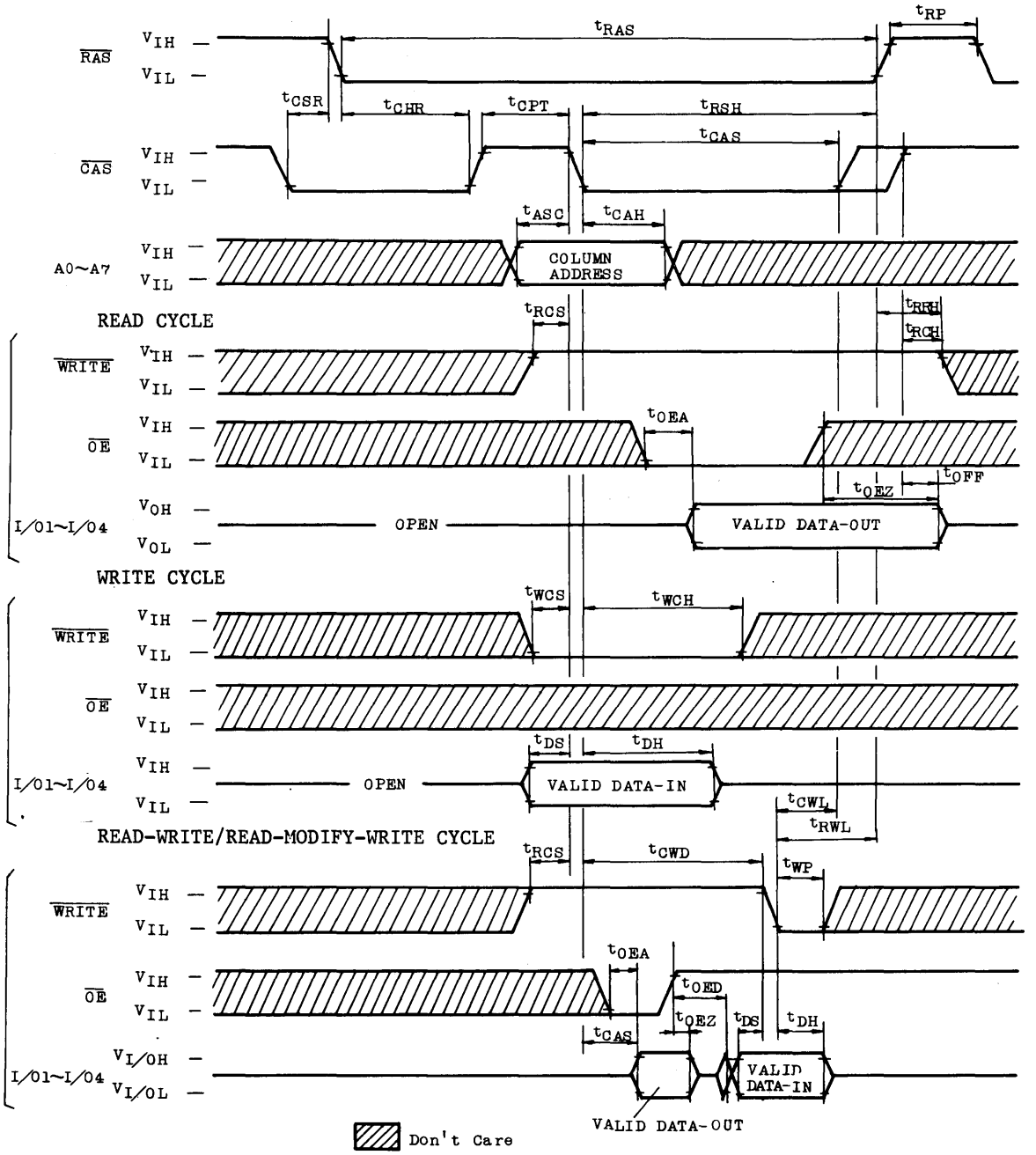


Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A7=Don't Care

● HIDDEN REFRESH CYCLE



• $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM41464P are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

Data is written during write or read-modify-write cycle.

The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ strobes data into the on-chip data latches.

In an early-write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold time referenced to this signal.

In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed -write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state

When the $\overline{OE}$ input is brought to a logic low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A_0-A_7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41464P offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation .

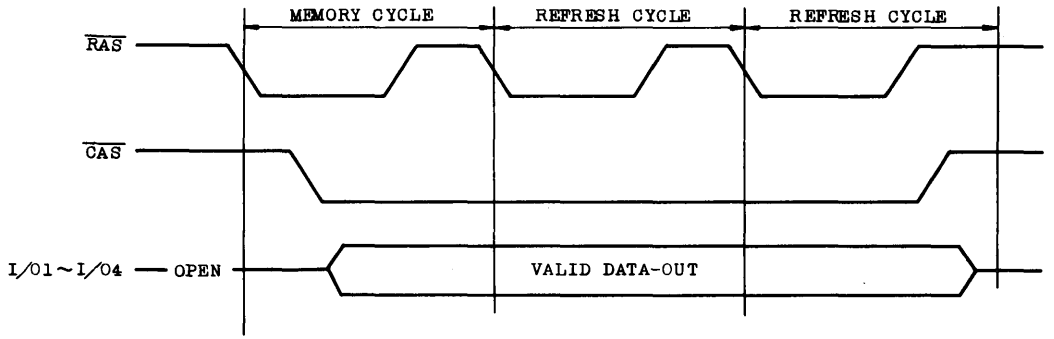
PAGE MODE

The "Page-Mode" feature of the TMM41464P allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative

going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TMM41464P is that refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

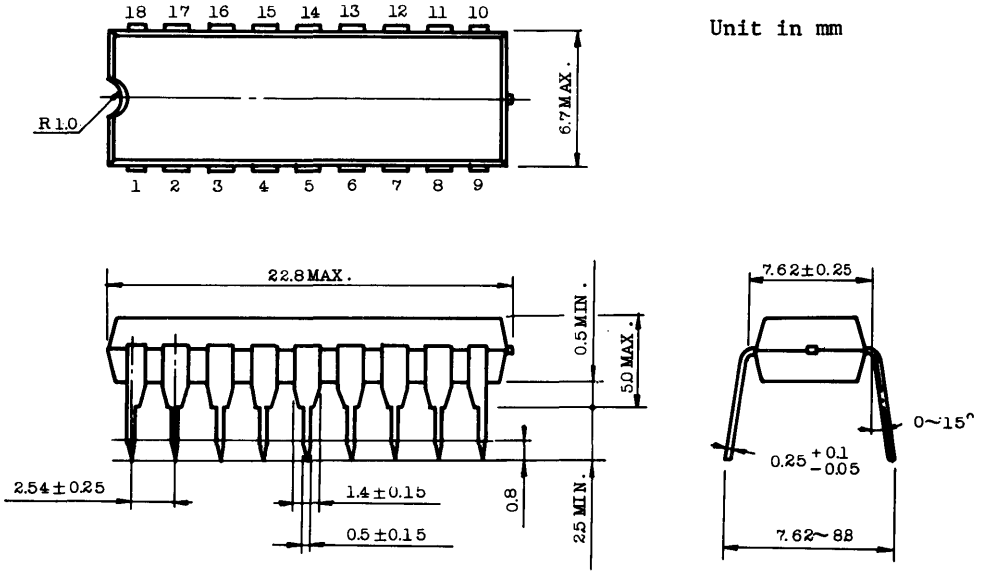
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41464P can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).
Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. Repeat this operation 256 times.
⑤ Check"0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ to the complement data.

OUTLINE DRAWINGS



Unit in mm

NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. Alldimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

CMOS Dynamic Random Access Memories

TOSHIBA MOS MEMORY PRODUCTS

1,048,576 WORDS × 1 BIT DYNAMIC RAM
SILICON GATE CMOS

* This is advanced information and specifications are subject to change without notice.

TC511000P/J-10
TC511000P/J-12

DESCRIPTION

The TC511000P/J is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000P/J utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000P/J to be packaged in a standard 18 pin plastic DIP and 20 pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

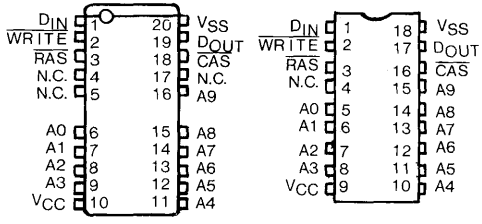
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511000P/J-10	TC511000P/J-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	45ns
t_{RC}	Cycle Time	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	55ns	70ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  330mW MAX. Operating (TC511000P/J-10)
  275mW MAX. Operating (TC511000P/J-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511000P
  Plastic SOJ: TC511000J

PIN CONNECTION (TOP VIEW)

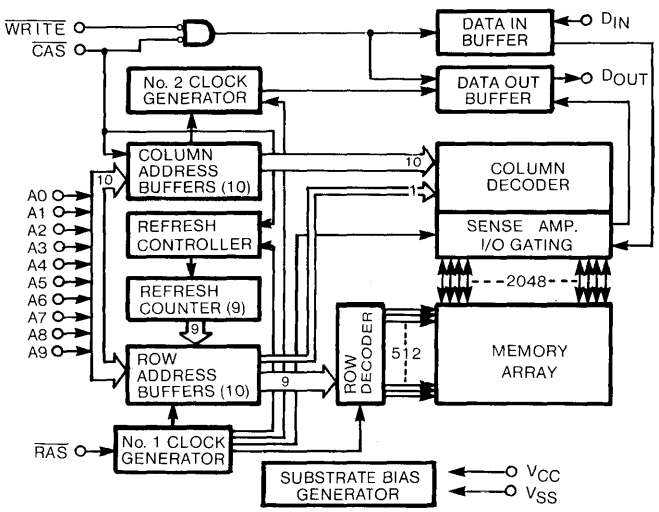
- Plastic SOJ
- Plastic DIP



PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	−1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511000P/J-10	-	60	mA	3,4
		TC511000P/J-12	-	50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511000P/J-10	-	60	mA	3
		TC511000P/J-12	-	50		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC511000P/J-10	-	40	mA	3,4
		TC511000P/J-12	-	30		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511000P/J-10	-	60	mA	3
		TC511000P/J-12	-	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV ≦ V_{OUT} ≦ V_{CC})		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} =4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511000P/J-10		TC511000P/J-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190		220		ns	
t_{RWC}	Read-Write Cycle Time	220		255		ns	
t_{PC}	Fast Page Mode Cycle Time	55		70		ns	
t_{PRWC}	Fast Page Mode Read-Write Cycle Time	85		105			
t_{RAC}	Access Time from $\overline{RAS}$		100		120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$		35		45	ns	8,13
t_{AA}	Access Time from Column Address		50		60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		50		65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5		5		ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80		90		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast page mode)	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35		45		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100		120		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35		45		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		15		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	20		25		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	50		60		ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511000P/J-10		TC511000P/J-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	20		25		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{WP}	Write Command Pulse Width	20		25		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		30		ns	
t_{DS}	Data Set-Up Time	0		0		ns	11
t_{DH}	Data Hold Time	20		25		ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	75		90		ns	
t_{REF}	Refresh Period		8		8	ms	
t_{WCS}	Write Command Set-Up Time	0		0		ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	35		45		ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100		120		ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	50		60		ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30		30		ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50		60		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15		20		ns	

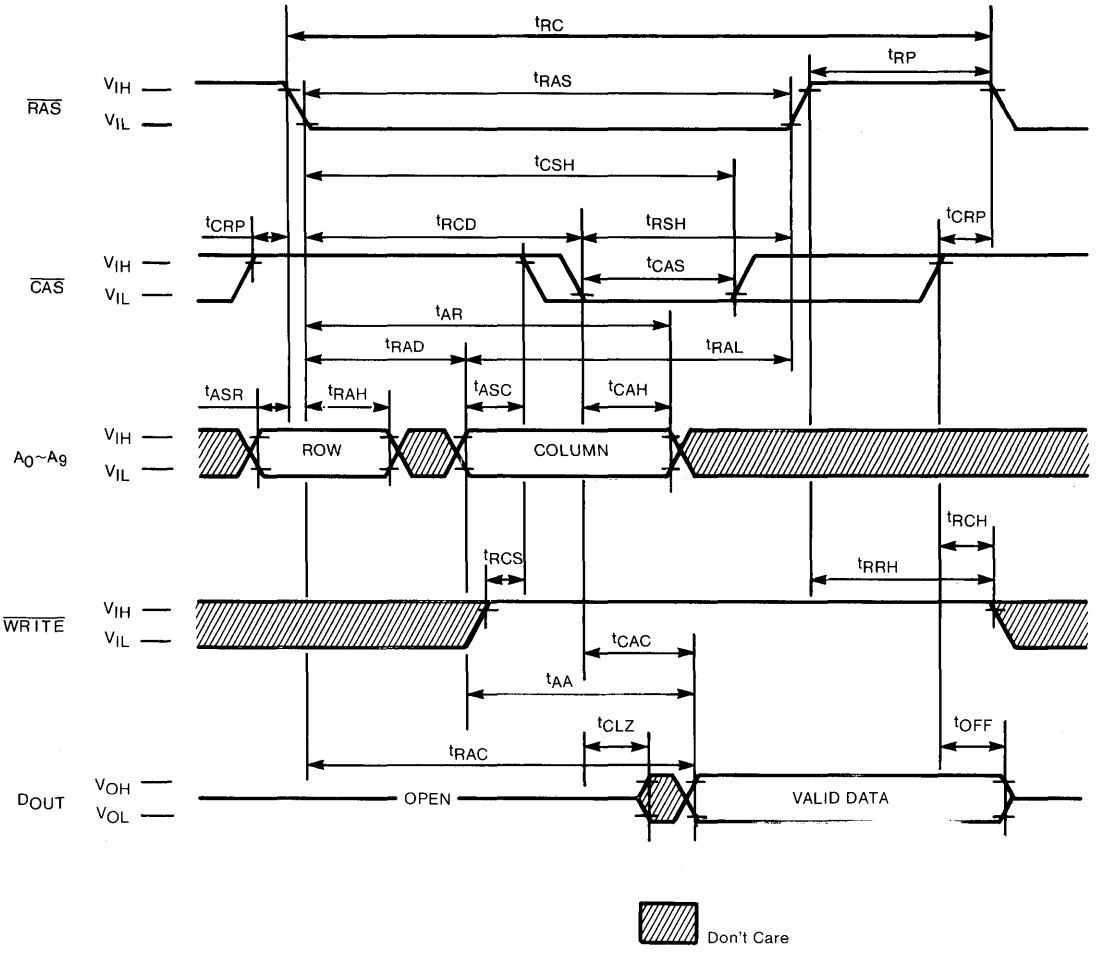
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A_0~A_9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

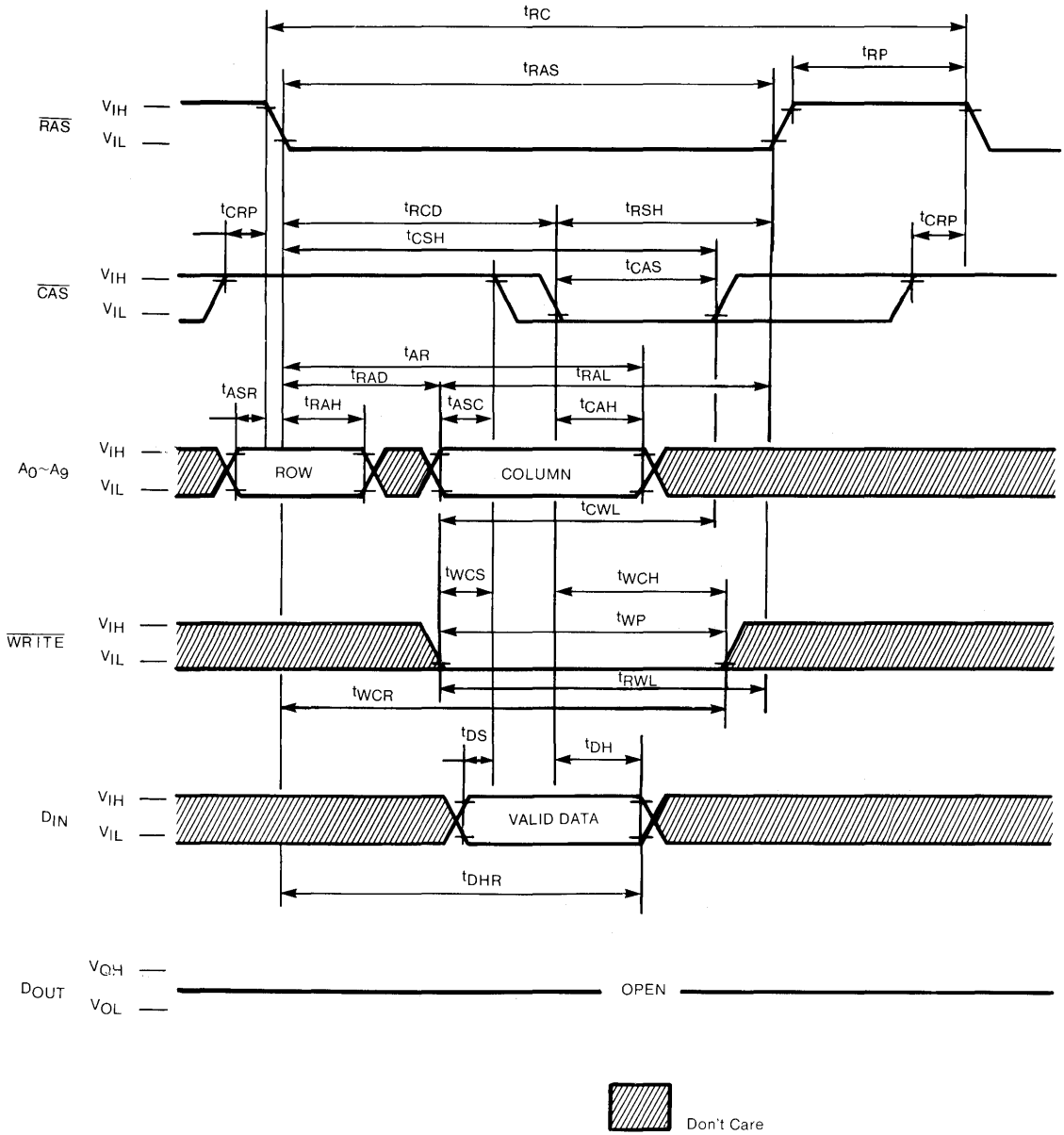
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycle.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RCD}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

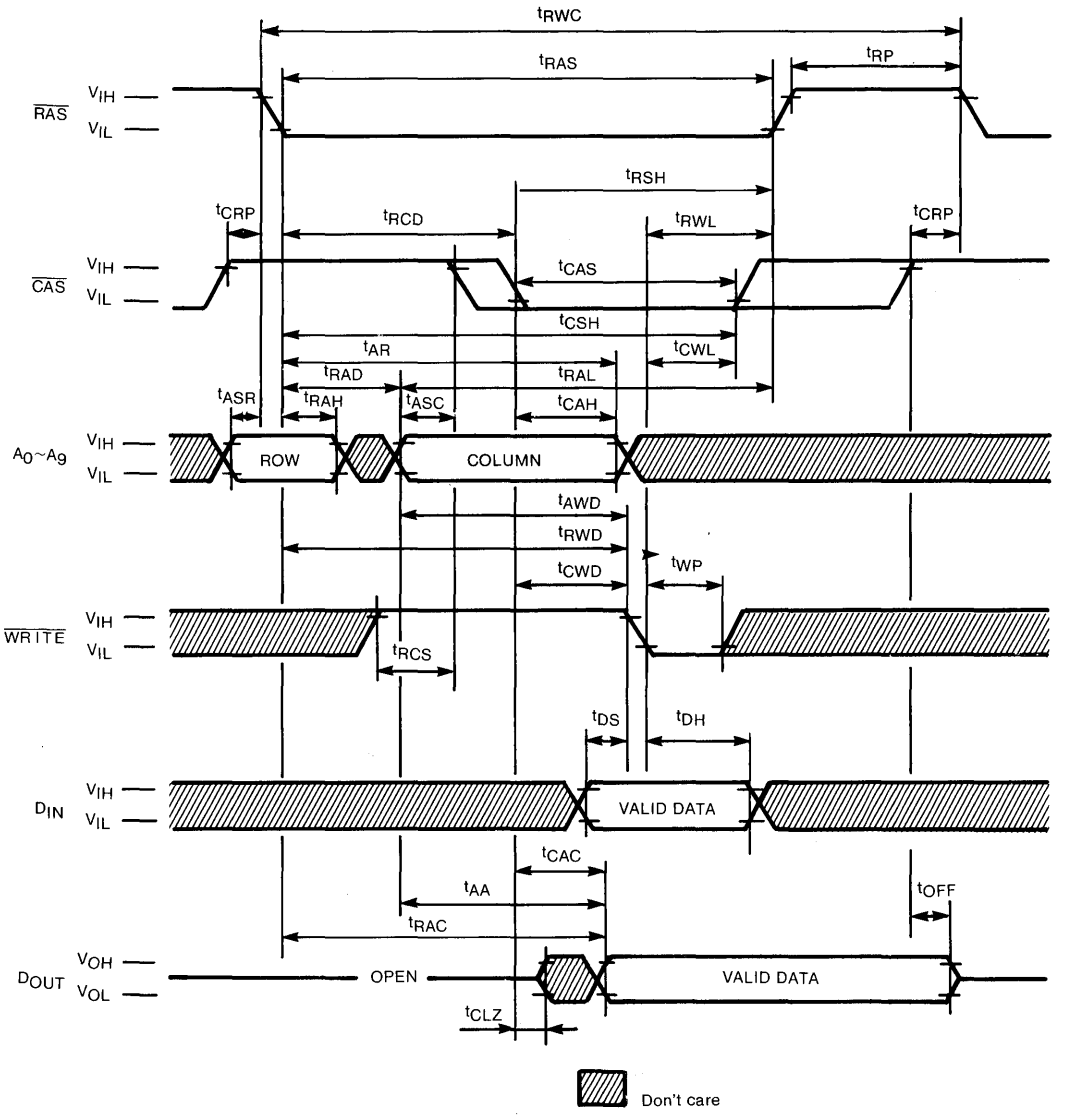
READ CYCLE


tRC
tRP
RAS
VIH
VIL
tRAS
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
VIH
VIL
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
Don't Care

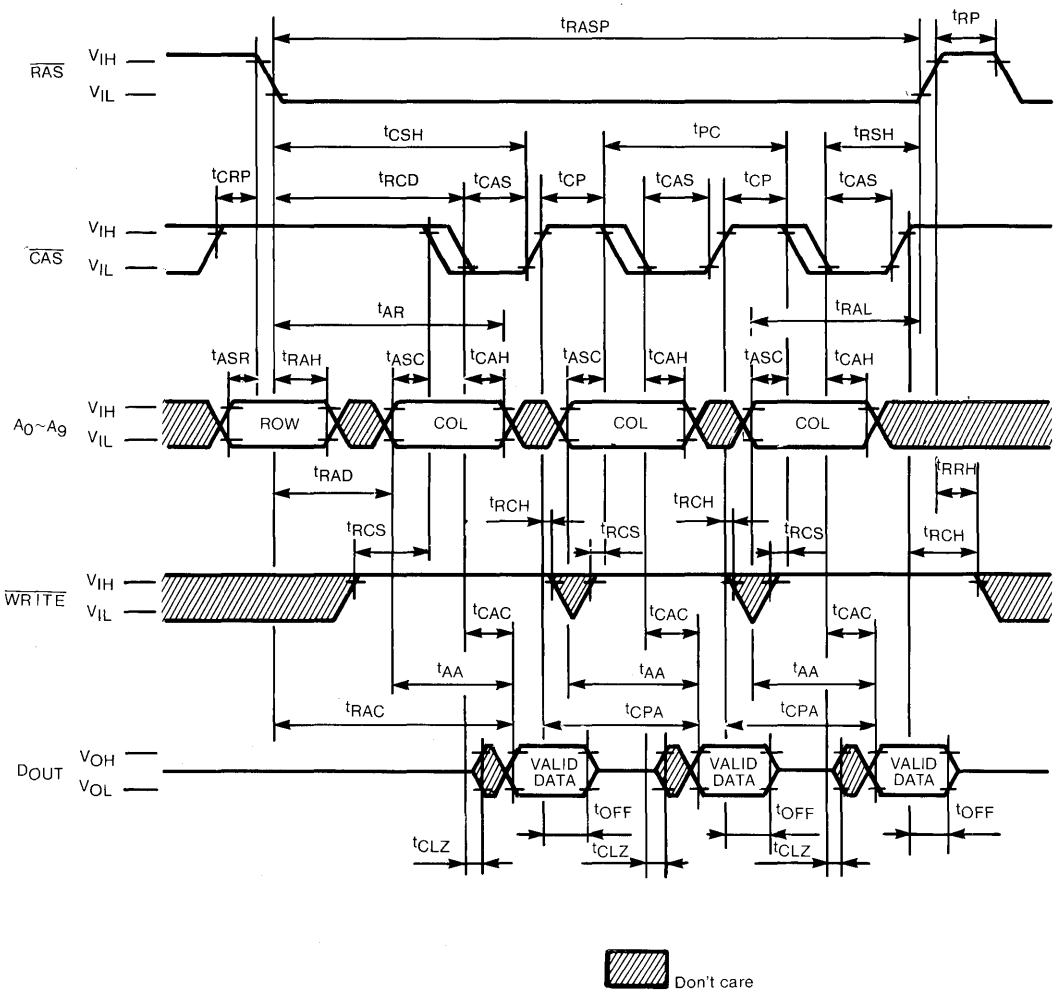
• EARLY WRITE CYCLE



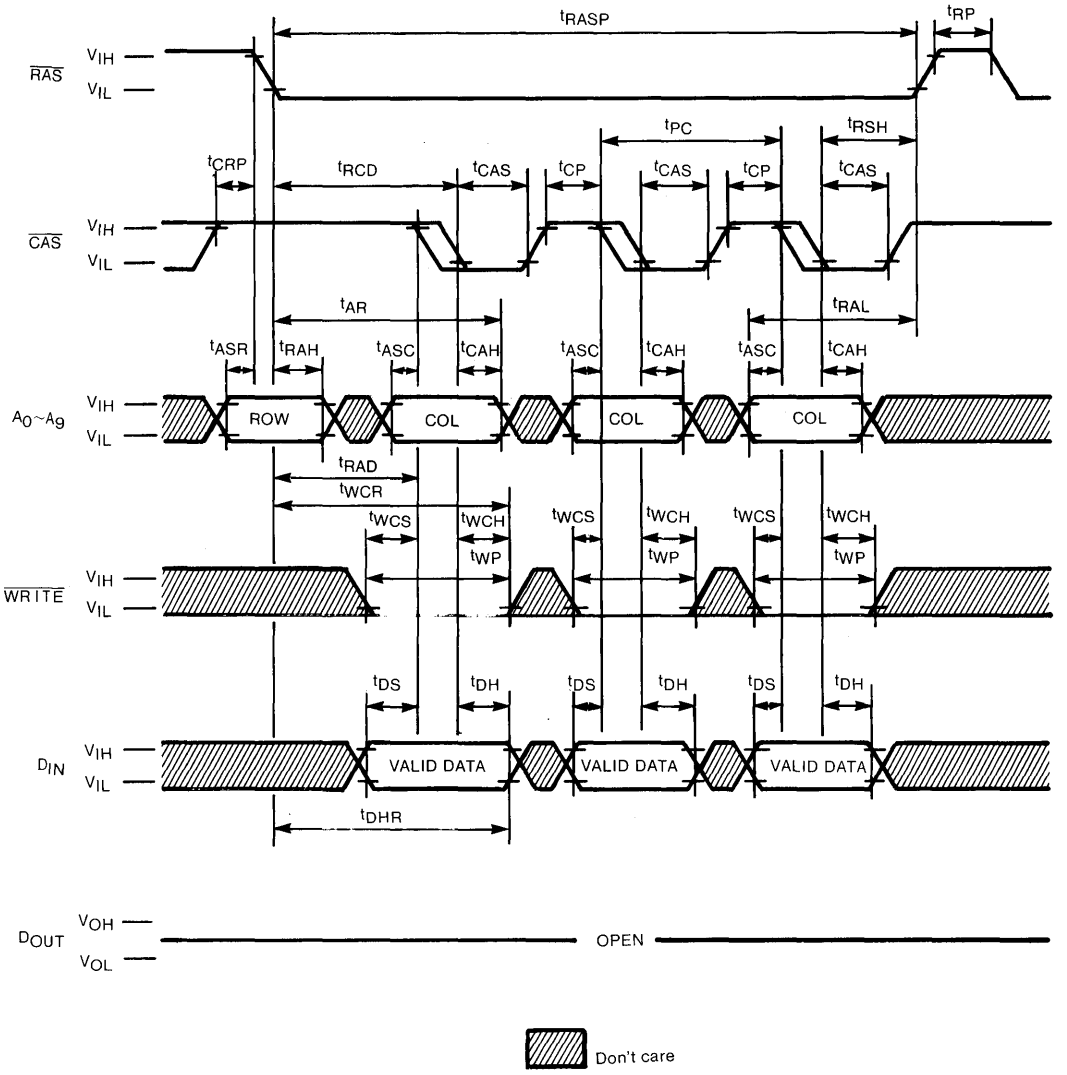
READ-WRITE CYCLE



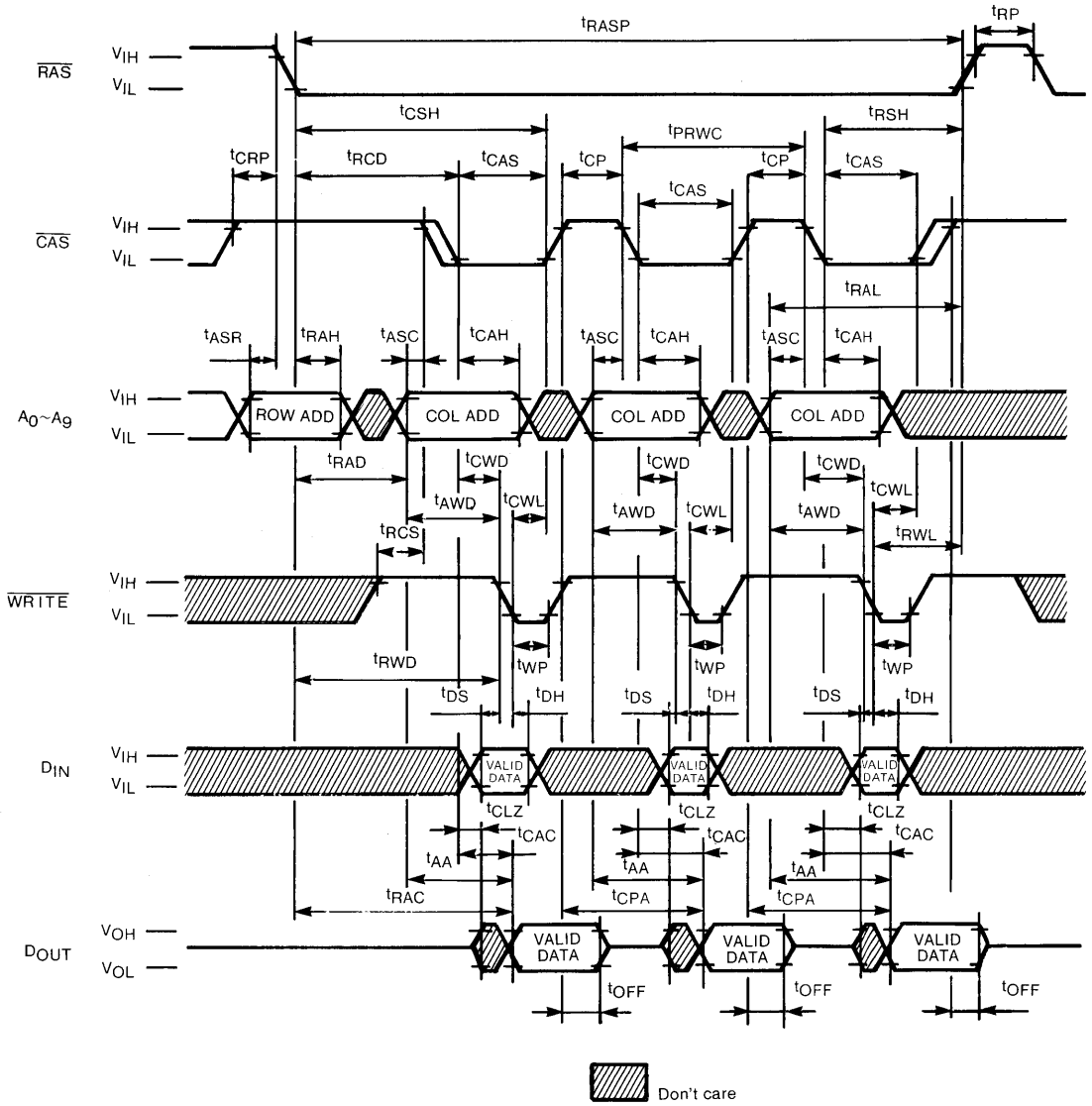
FAST PAGE MODE READ CYCLE



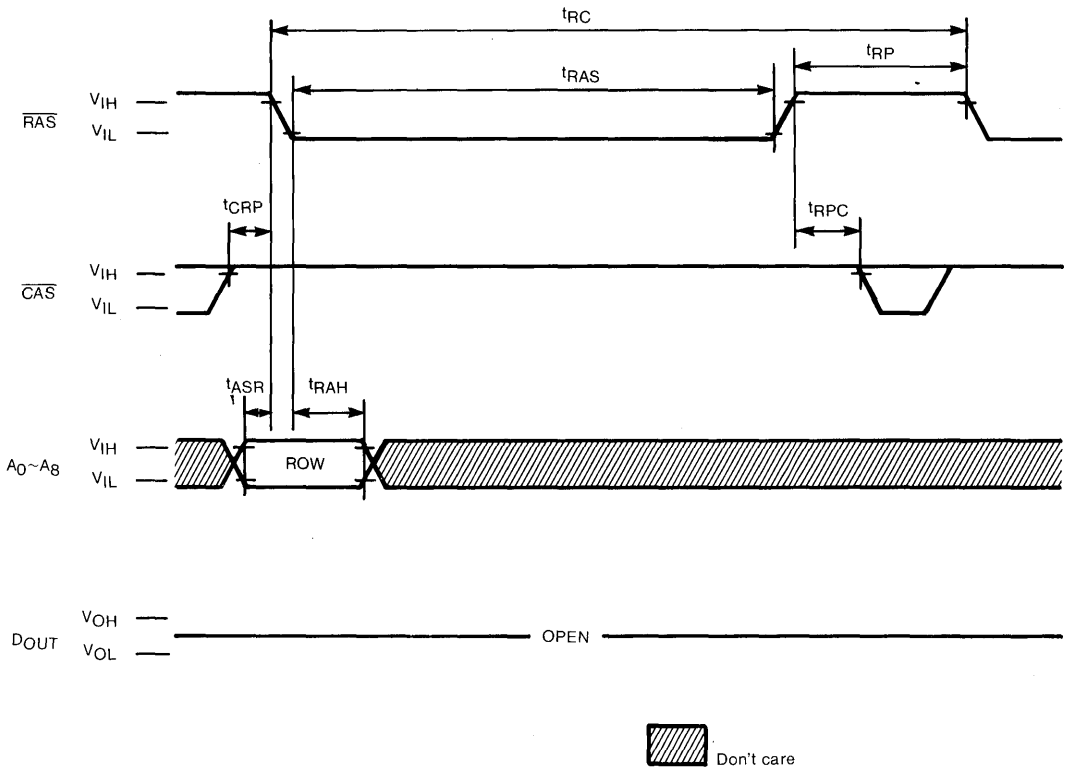
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-WRITE CYCLE

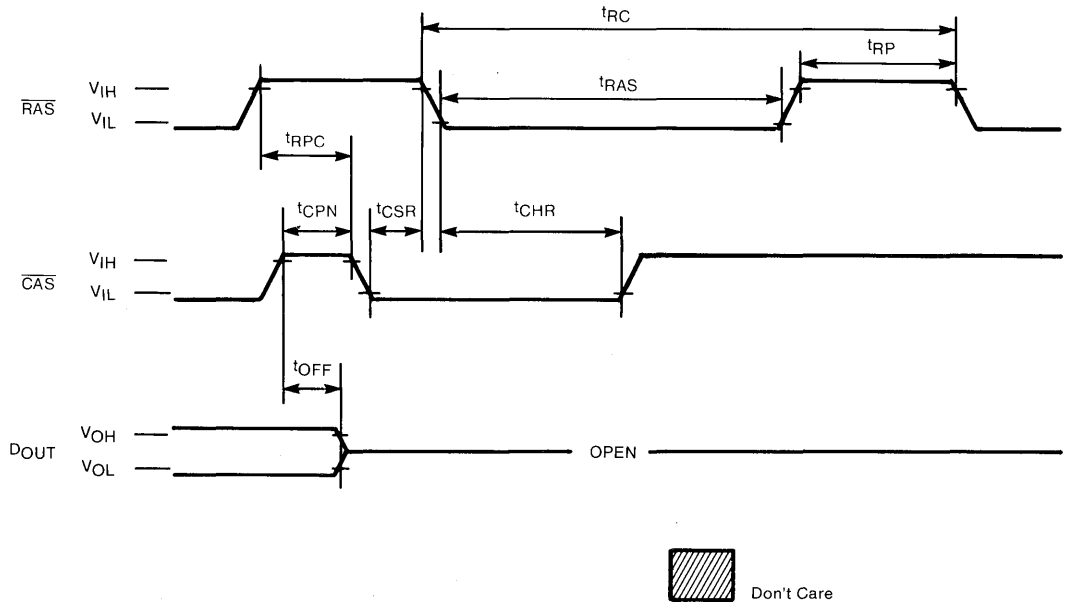


$\overline{RAS}$ ONLY REFRESH CYCLE



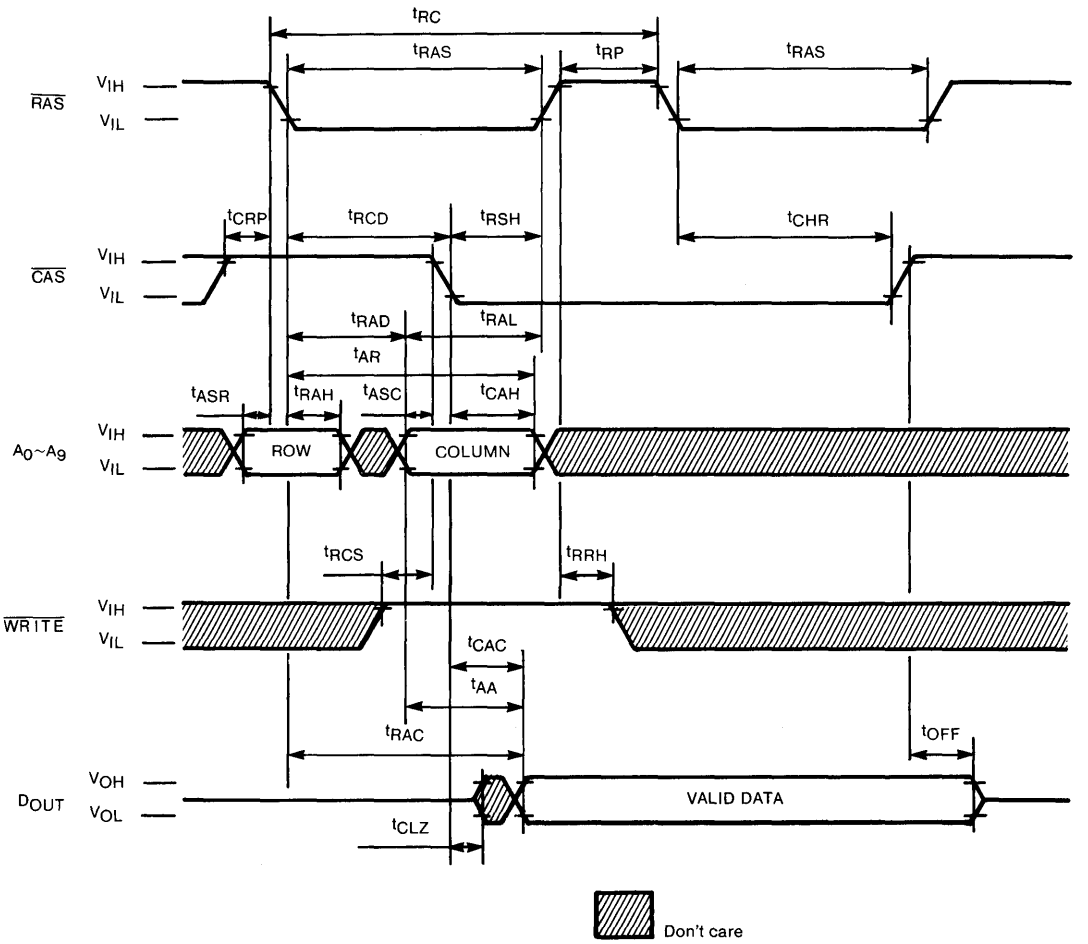
NOTE: $\overline{WRITE}$=Don't care, A9=Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

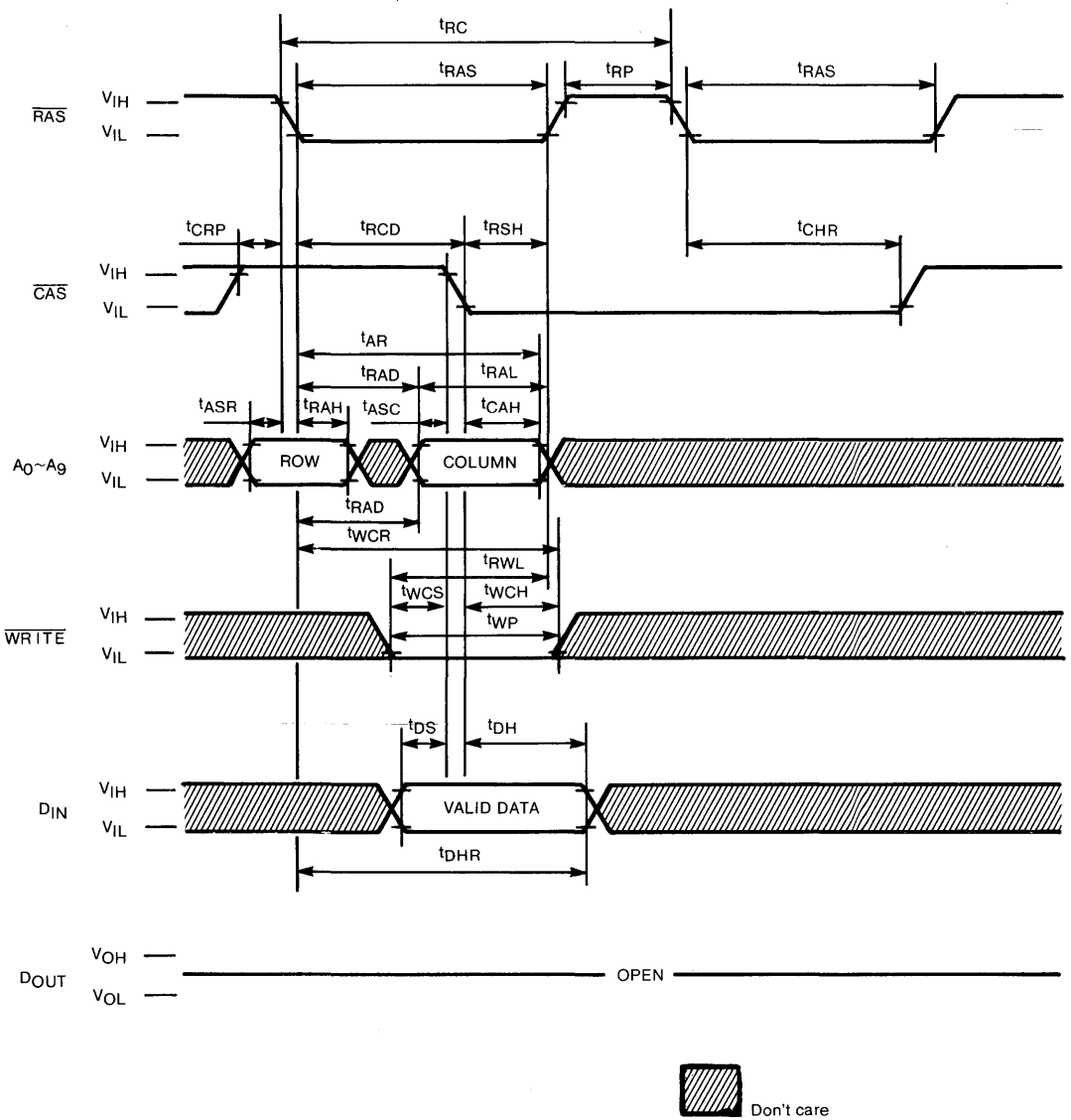


NOTE: $\overline{WRITE}$=Don't care, A0~A9=Don't care

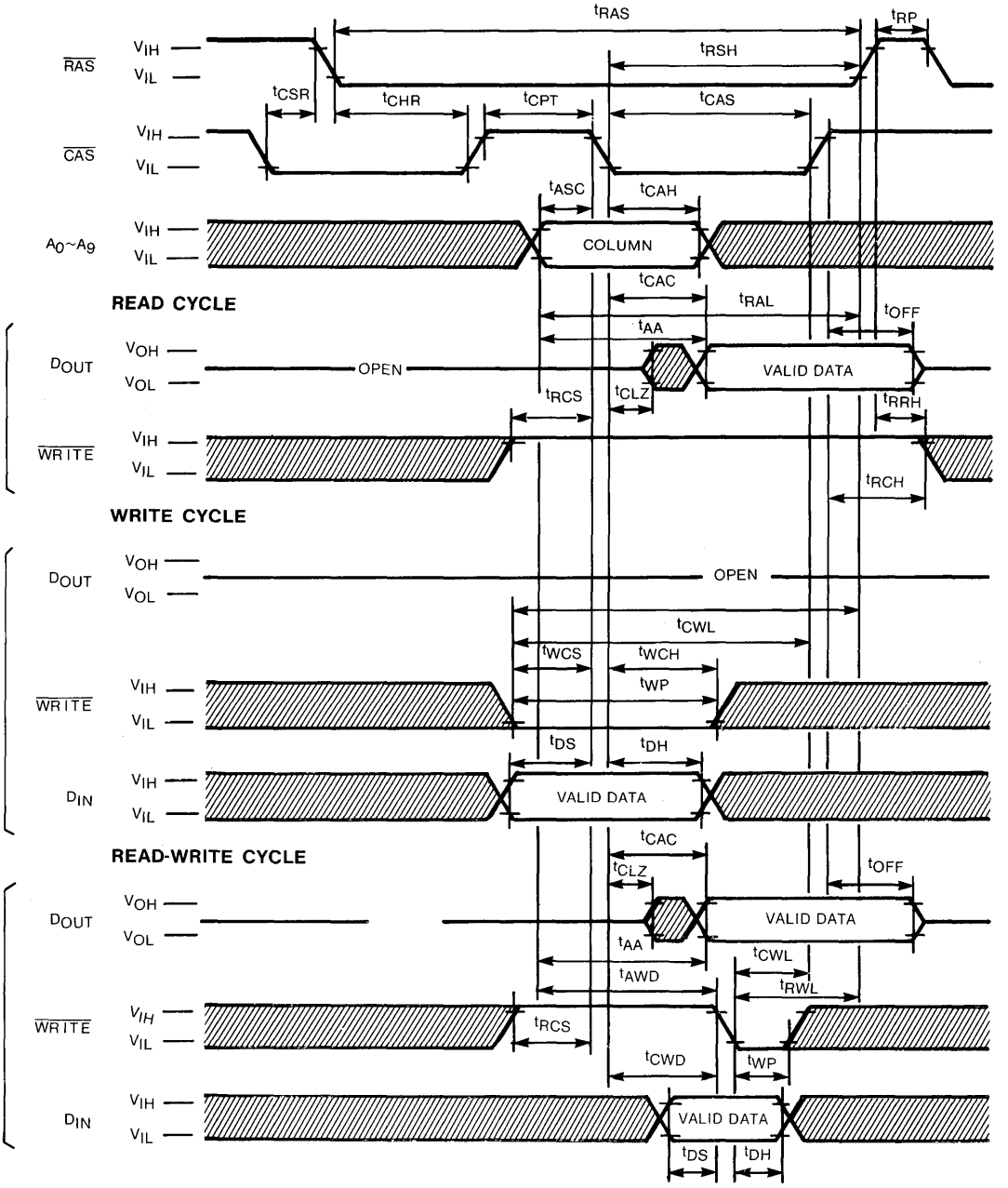
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



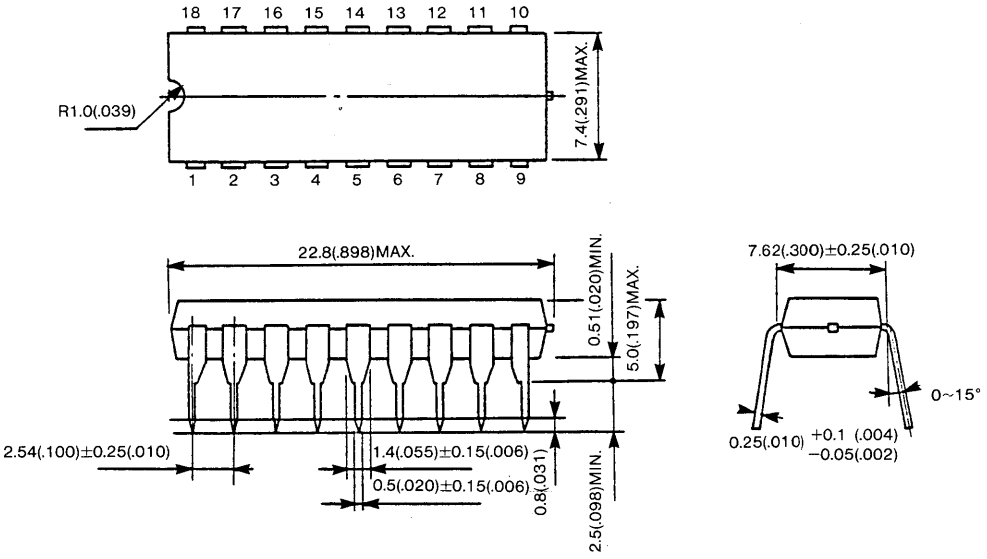
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

Unit in mm(inches)

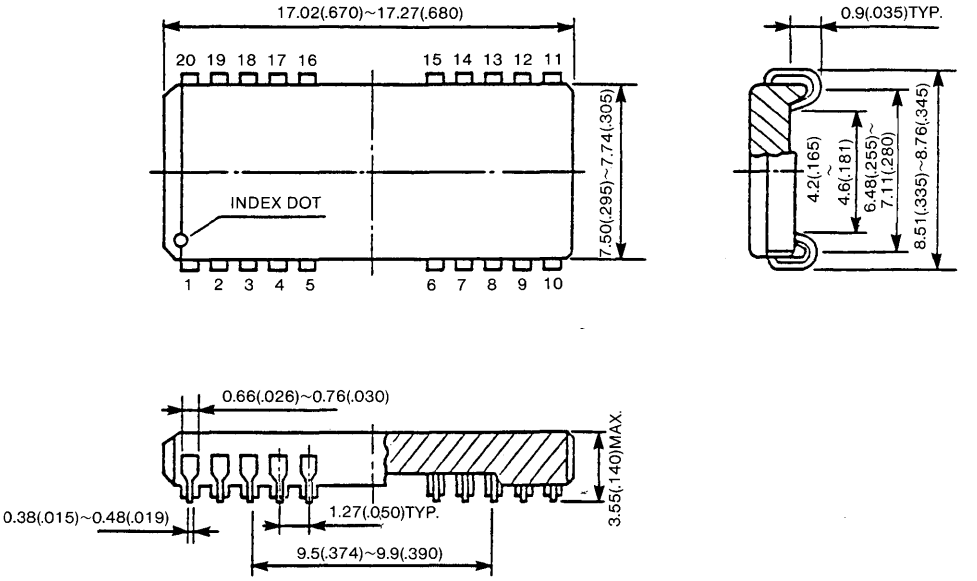
- Plastic DIP



Note: Each lead pitch is 2.54(.100) mm. All leads are located within 0.25(.010)mm of their true longitudinal position with respect to No. 1 and No. 18 leads.

Unit in mm(inches)

- Plastic SOJ



Note: Each lead pitch 1.27(.050)mm.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

1,048,576 WORD × 1 BIT DYNAMIC RAM
SILICON GATE CMOS

* This is advanced information and specifications are subject to change without notice.

TC511001P/J-10
TC511001P/J-12

DESCRIPTION

The TC511001P/J is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001P/J utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511001P/J to be packaged in a standard 18 pin plastic DIP and 20 pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001P/J is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

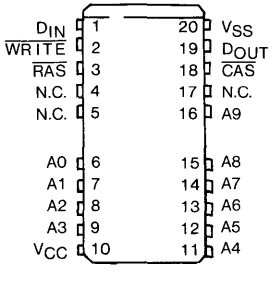
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511001P/J-10	TC511001P/J-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	45ns
t_{RC}	Cycle Time	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	50ns

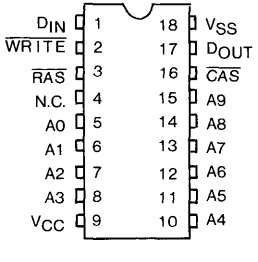
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  330mW MAX. Operating (TC511001P/J-10)
  275mW MAX. Operating (TC511001P/J-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Nibble Mode capability
- All inputs and output TTL compatible
- 512 refresh cycle/8ms
- Package Plastic DIP: TC511001P
  Plastic SOJ: TC511001J

PIN CONNECTION (TOP VIEW)

- Plastic SOJ



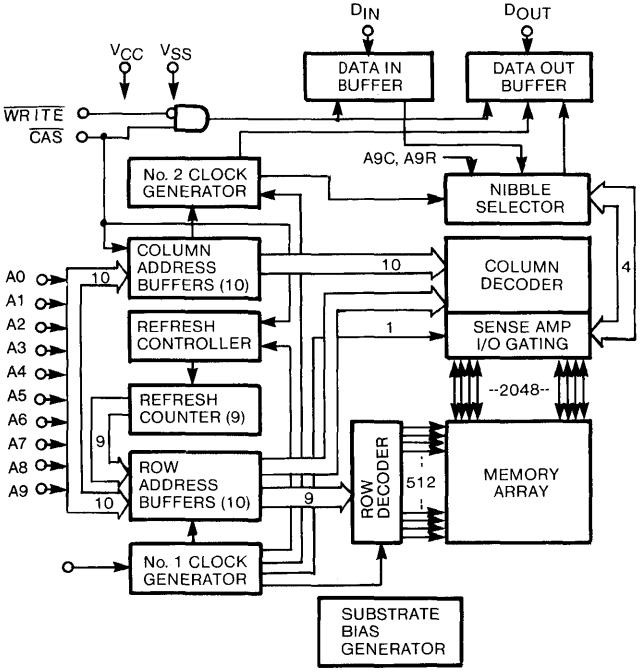
- Plastic DIP



PIN NAMES

A0~A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	−0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511001P/J-10	-	60	mA	3,4
		TC511001P/J-12	-	50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511001P/J-10	-	60	mA	3
		TC511001P/J-12	-	50		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	TC511001P/J-10	-	40	mA	3,4
		TC511001P/J-12	-	30		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}−0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode) $\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511001P/J-10	-	60	mA	3
		TC511001P/J-12	-	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV ≦ V_{OUT} ≦ +5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4		V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} =4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511001P/J-10		TC511001P/J-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	-	220	-	ns	
t_{RWC}	Read-Write Cycle Time	220	-	255	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	50	-	ns	
t_{NRMW}	Nibble Mode Read-Write Cycle Time	65	-	80	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	35	-	45	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	55	ns	8,14
t_{NCAC}	Nibble Mode Access Time	-	20	-	25	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	ns	
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35	10,000	45	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	65	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	55	20	65	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20	-	25	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	25	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	80	-	95	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	55	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511001P/J-10		TC511001P/J-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	80	-	95	-	ns	
t_{WP}	Write Command Pulse Width	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	80	-	95	-	ns	
t_{REF}	Refresh Period	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	35	-	45	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	100	-	120	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	-	55	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	-	60	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	15	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	25	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	

CAPACITANCE (V_{CC}~5V±10%, f~1MHz, Ta~0~70°C)

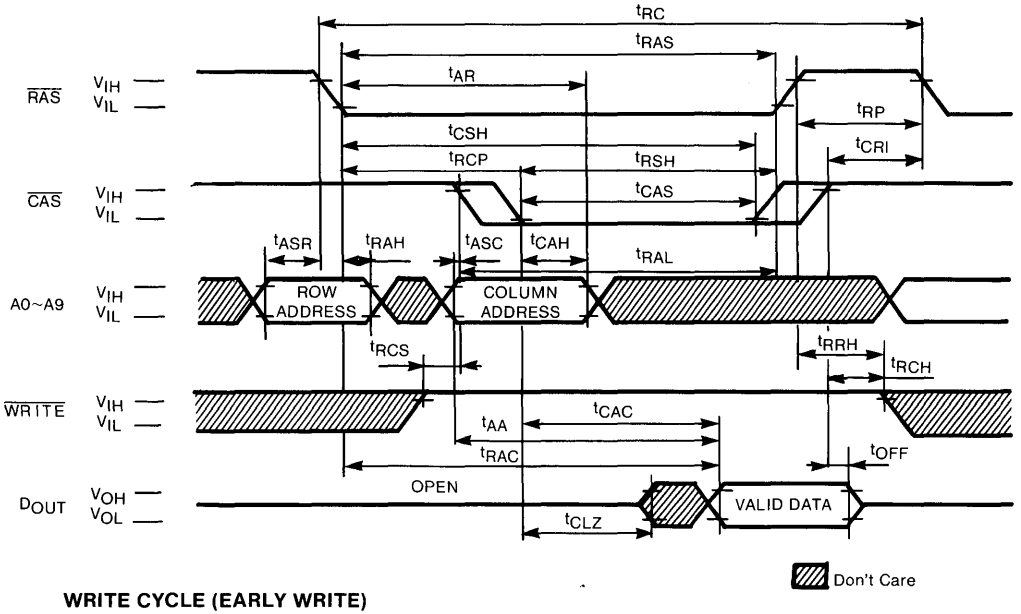
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A_0~A_9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

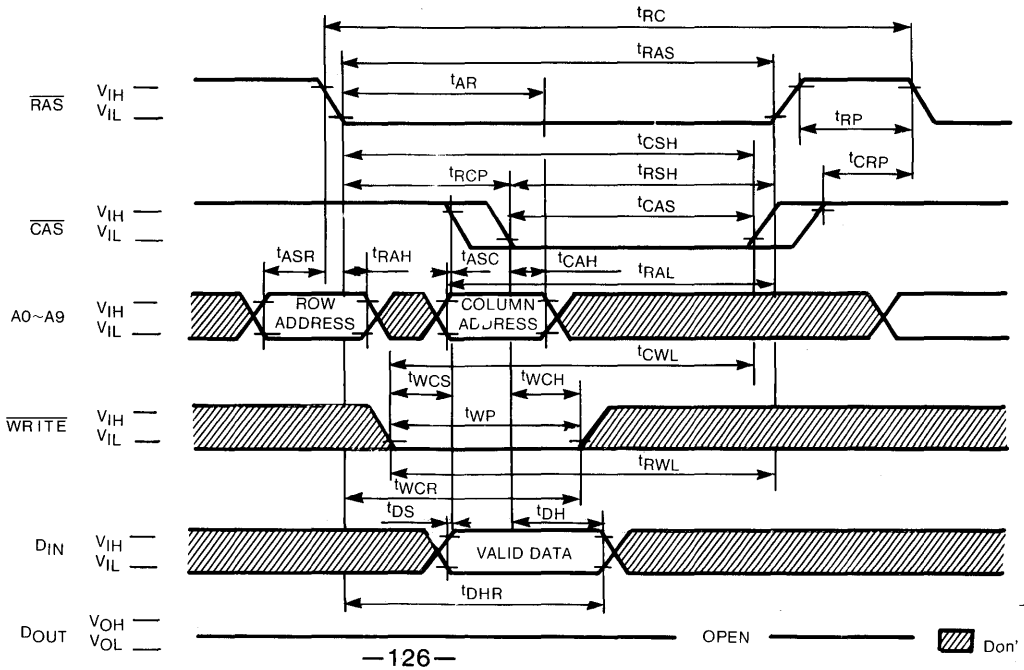
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycle.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RCD}(max.) can be met. t_{RAD}(Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

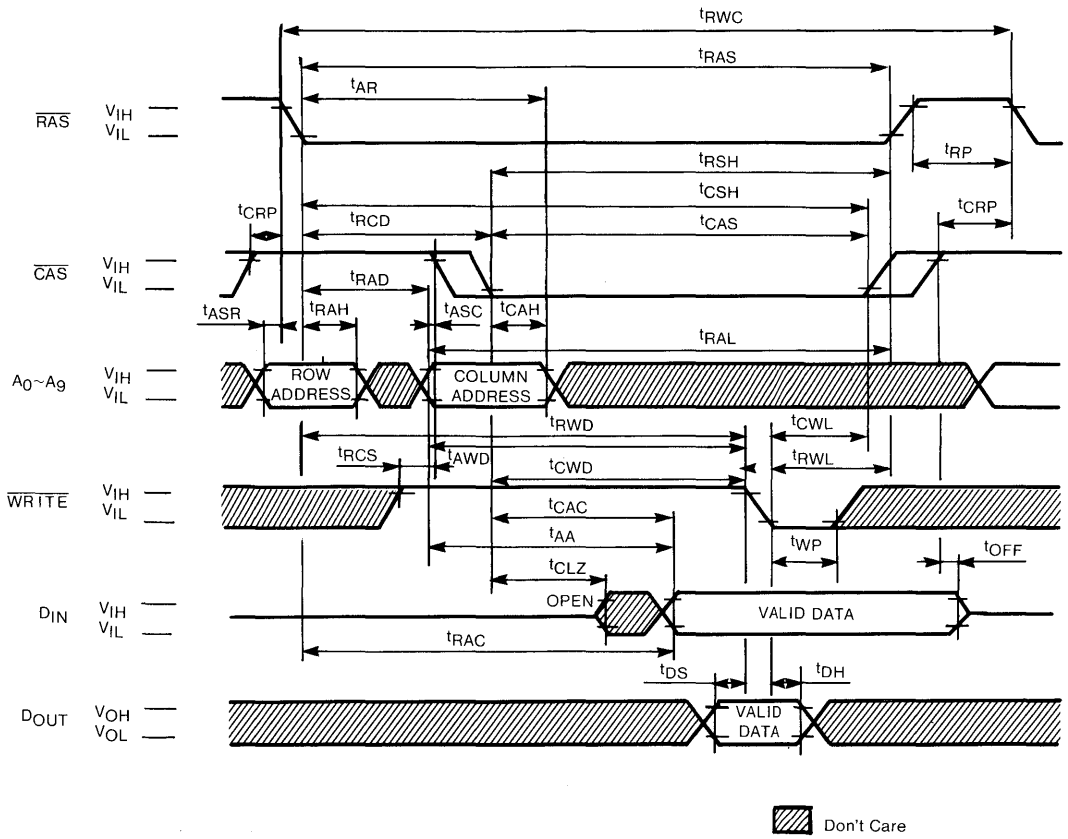
READ CYCLE



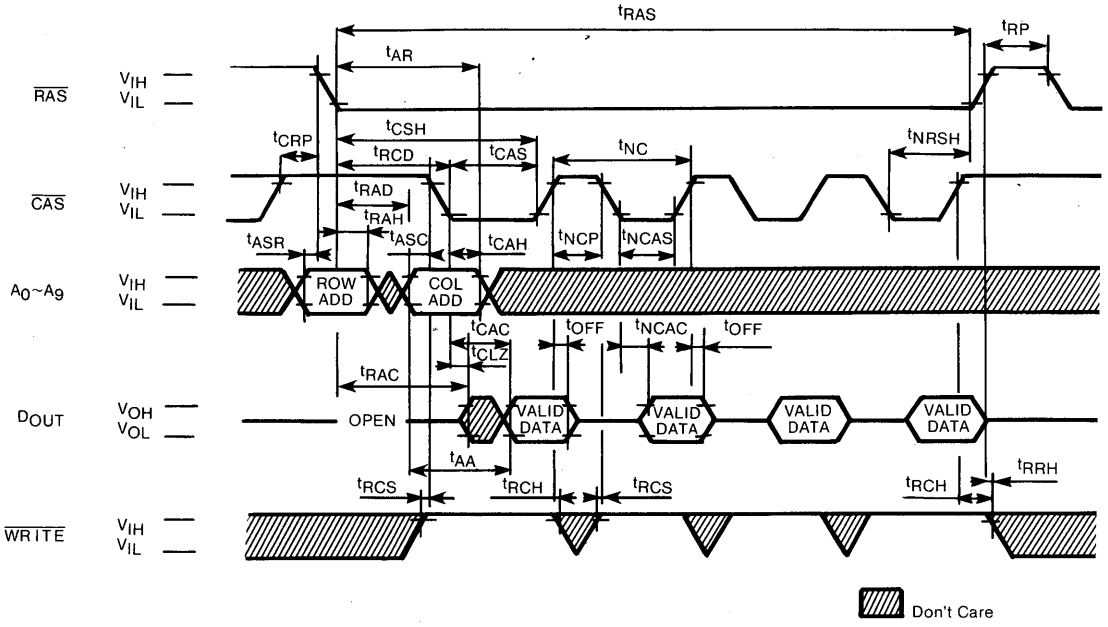
WRITE CYCLE (EARLY WRITE)



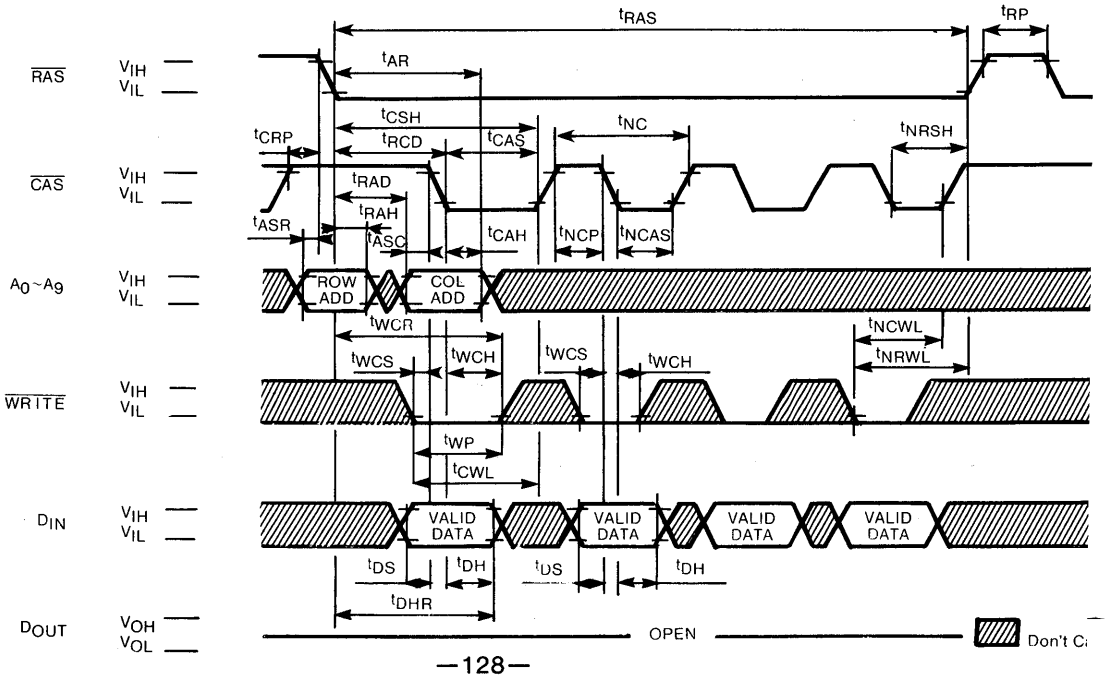
READ-WRITE CYCLE



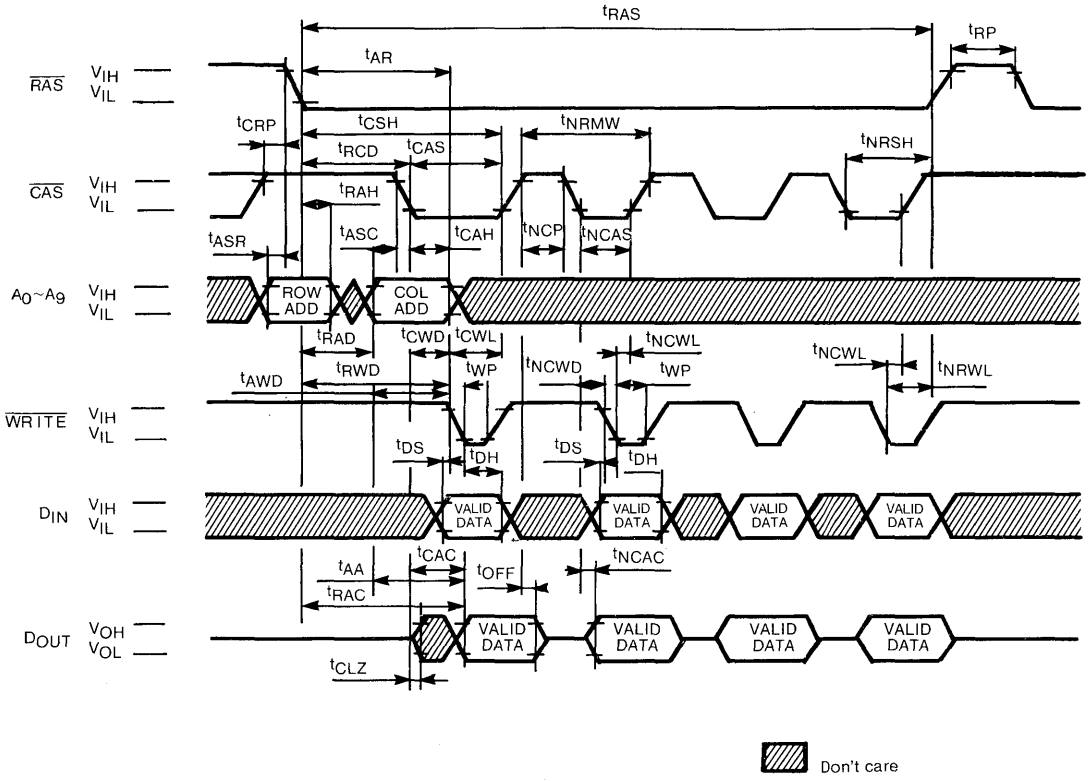
NIBBLE MODE READ CYCLE



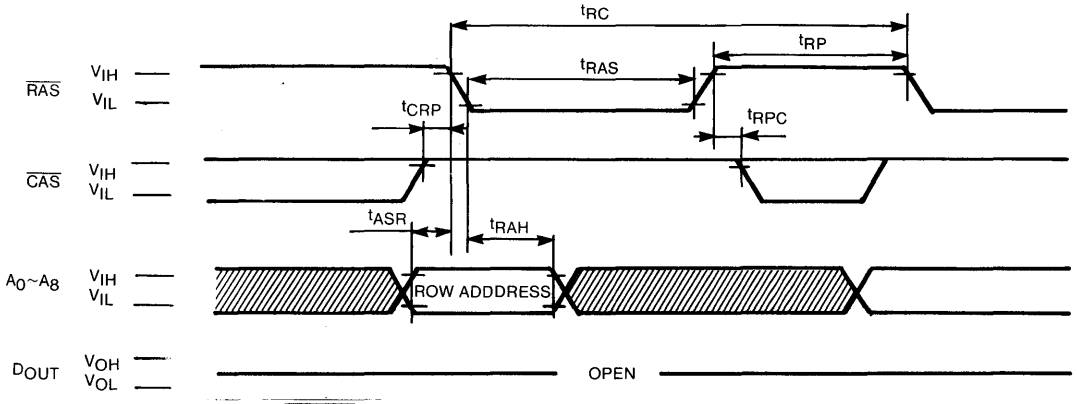
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



NIBBLE MODE READ-WRITE CYCLE



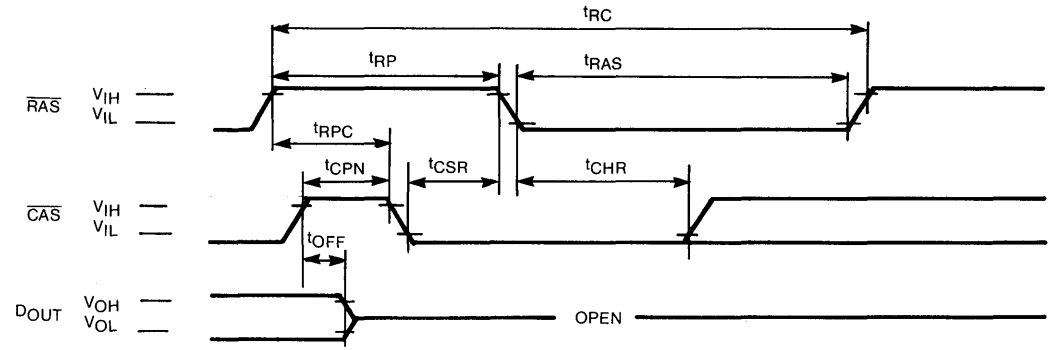
$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$=Don't care, A9=Don't care

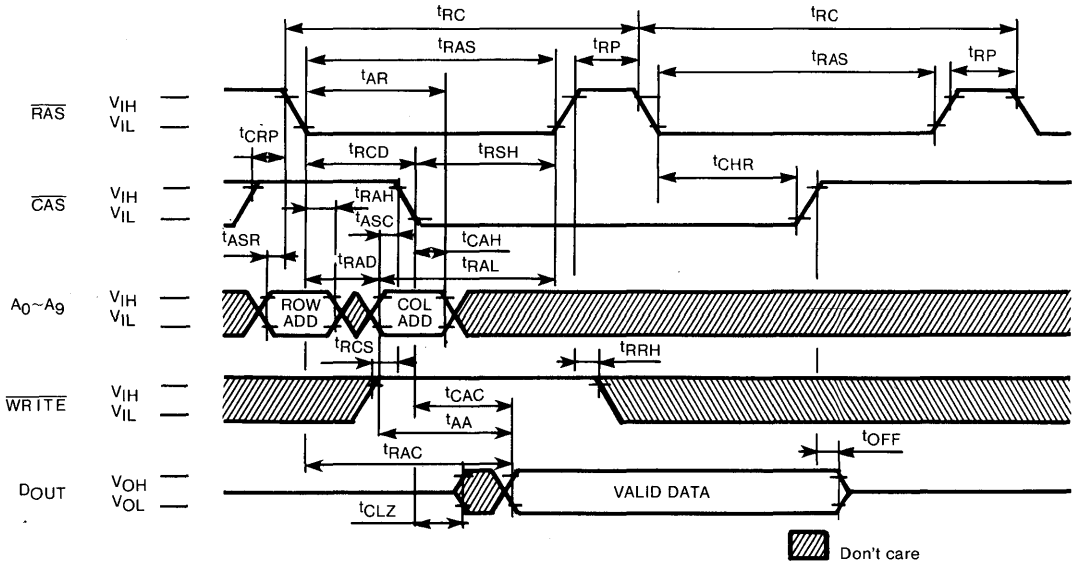
Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

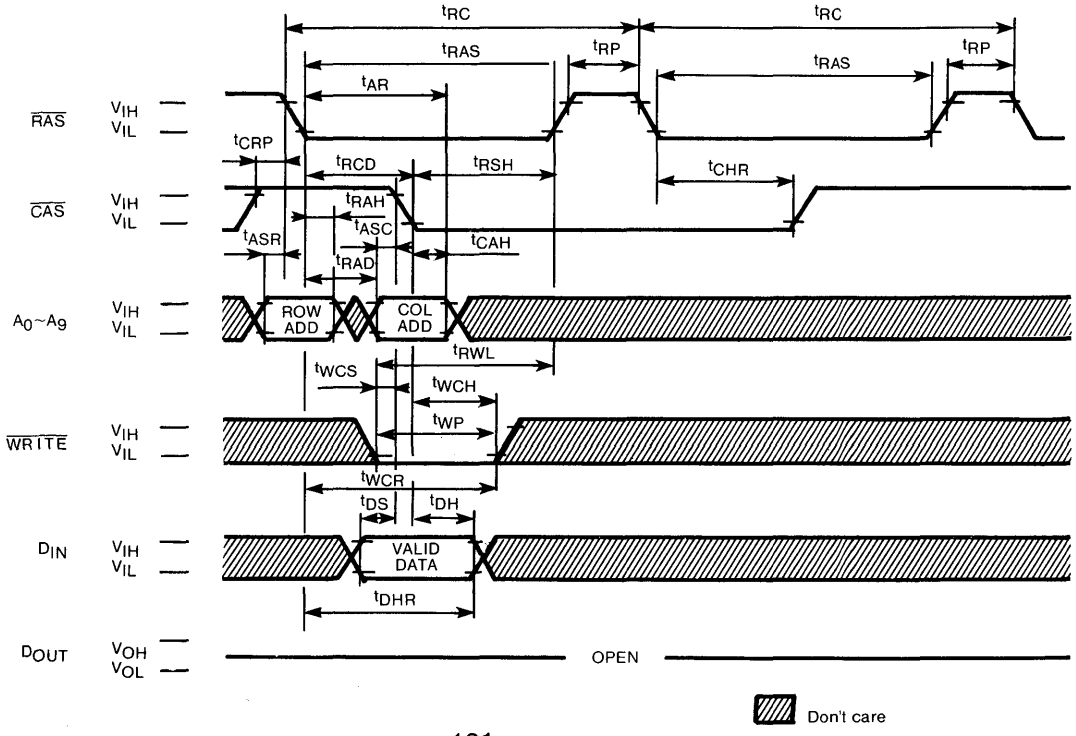


NOTE: $\overline{WRITE}$=Don't care, A0 ~ A9=Don't care

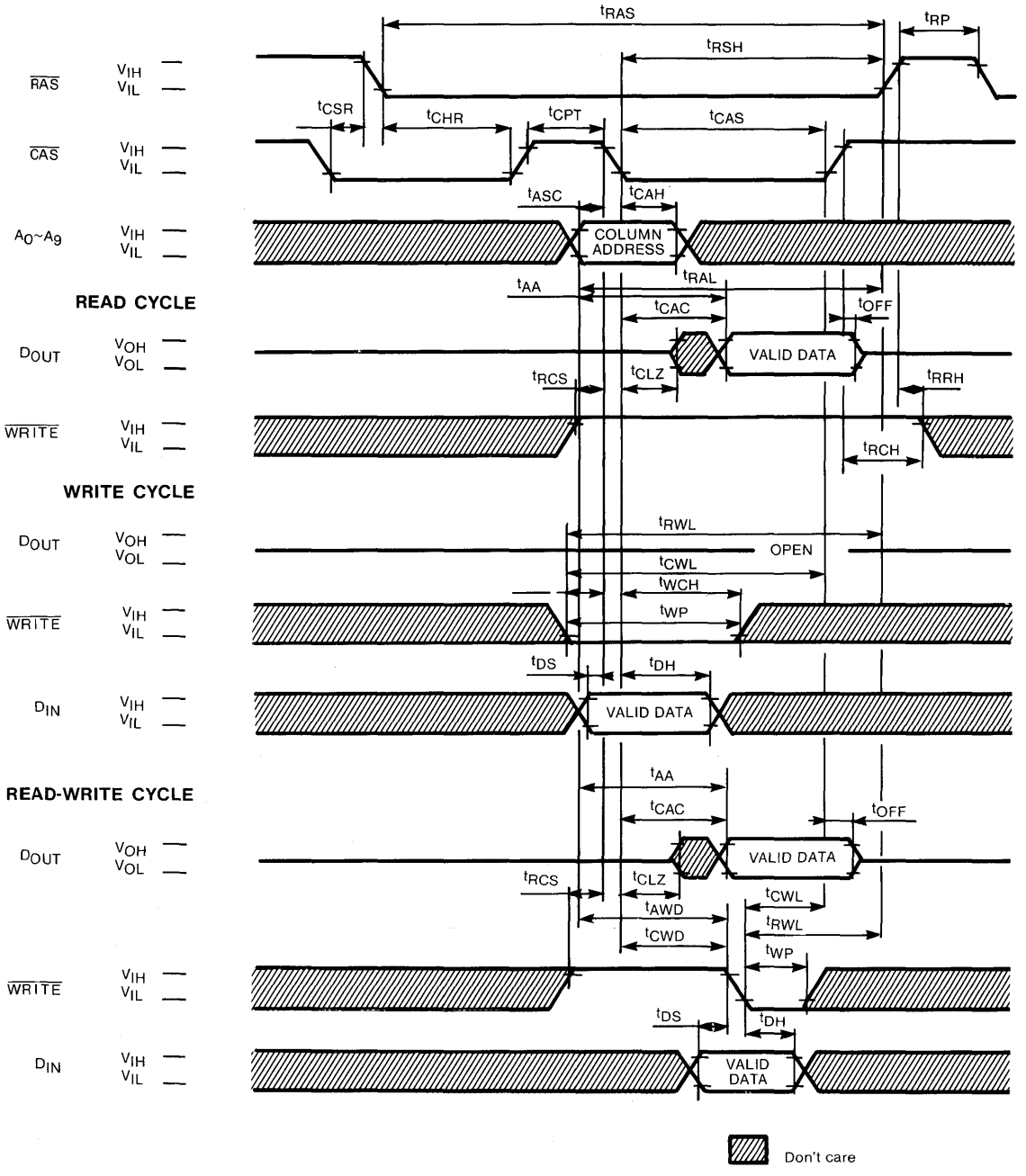
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC511001P/J are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

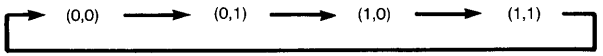
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC511001P/J is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin 15 (A9) determines the starting point of the circular 4 bits nibble. Row A9 and column A9 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A9 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

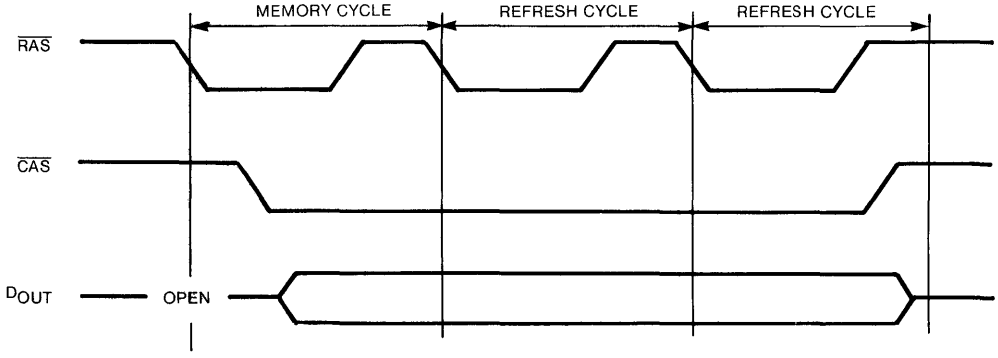
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0 ~ A8) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511001P/J offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC511001P/J is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holdng $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511001P/J can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as colun address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ WRITE CYCLE).
Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST.
Repeat this operation 512 times.

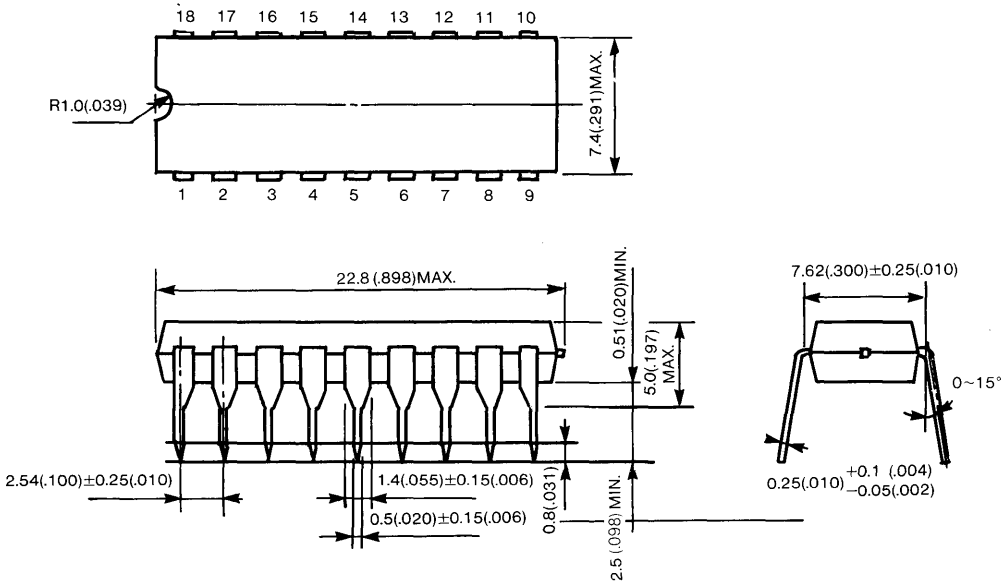
⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS

- **Plastic DIP**

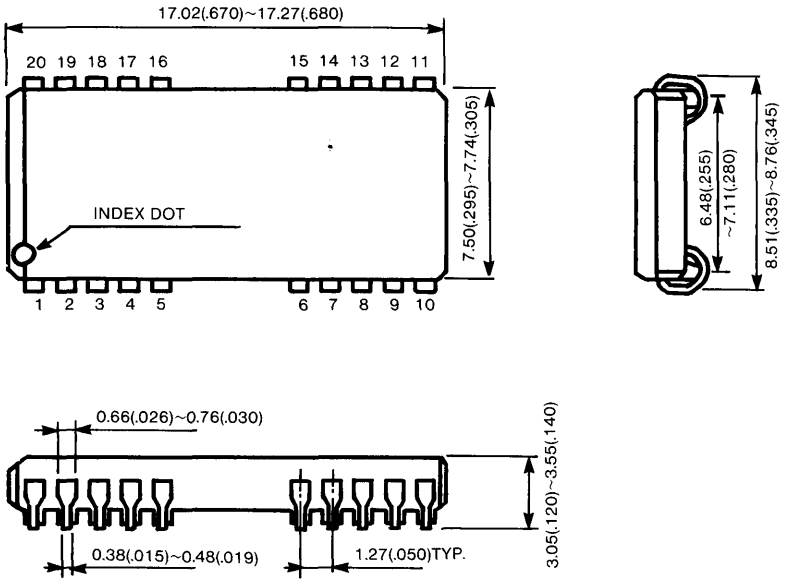
Unit in mm (inches)



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.

- **Plastic SOJ**

Unit in mm (inches)



Note: Each lead pitch 1.27mm. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

1,048,576 WORDS × 1 BIT STATIC COLUMN DYNAMIC RAM
SILICON GATE CMOS
* This is advanced information and specifications are subject to change without notice.

TC511002P/J-10
TC511002P/J-12

DESCRIPTION

The TC511002P/J is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002P/J utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511002P/J to be packaged in a standard 18 pin plastic DIP and 20 pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

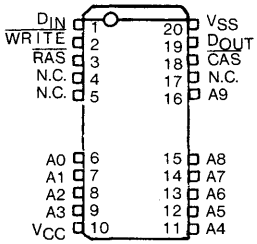
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511002P/J-10	TC511002P/J-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	35ns	45ns
t_{RC}	Cycle Time	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	55ns	70ns

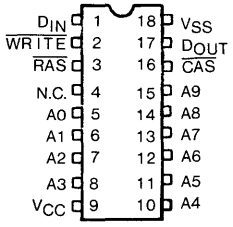
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  330mW MAX. Operating (TC511002P/J-10)
  275mW MAX. Operating (TC511002P/J-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Static Column Mode Capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP : TC511002P
  Plastic SOJ : TC511002J

PIN CONNECTION

- Plastic SOJ



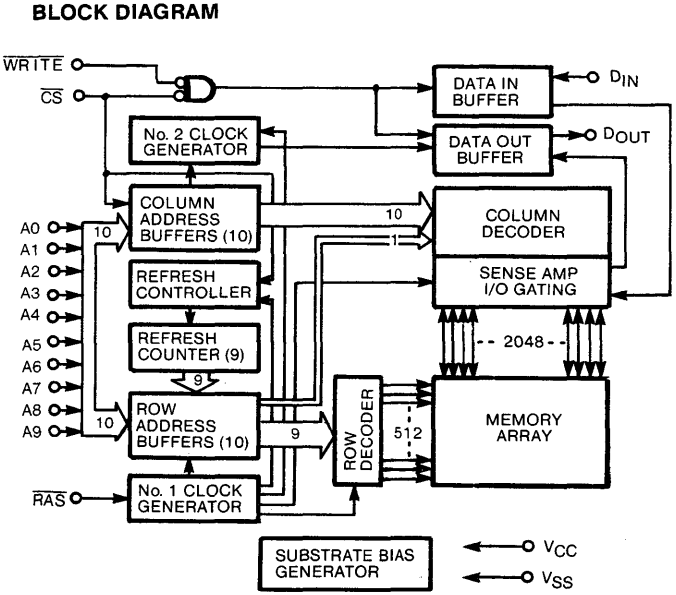
- Plastic DIP



PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	W · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	−1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511002P/J-10	-	60	mA	3,4
		TC511002P/J-12	-	50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}; t_{RC}=t_{RC} MIN.)	TC511002P/J-10	-	60	mA	3
		TC511002P/J-12	-	50		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$ =V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC511002P/J-10	-	40	mA	3,4
		TC511002P/J-12	-	30		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}−0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511002P/J-10	-	60	mA	3
		TC511002P/J-12	-	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=OV)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, OV ≦ V_{OUT} ≦ V_{CC})		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511002P/J-10		TC511002P/J-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190		220		ns	
t_{RWC}	Read-Write Cycle Time	220		255		ns	
t_{SC}	Static Column Mode Cycle Time	55		65		ns	
t_{SRWC}	Static Column Mode Read Write Cycle Time	100		120		ns	
t_{RAC}	Access Time from $\overline{RAS}$		100		120	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$		35		45	ns	8,13
t_{AA}	Access Time from Column Address		50		60	ns	8,14
t_{ALW}	Access Time from Last Write		90		110	ns	8,15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5		5		ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5		5		ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$		30		35	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0		0		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80		90		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25		30		ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	100		120		ns	
t_{CS}	$\overline{CS}$ Pulse Width	35		45		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	65	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10		15		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	20		25		ns	
t_{AWR}	Write Address Hold Time Referenced to $\overline{RAS}$	75		90		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	115		140		ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	50		60		ns	
t_{AH}	Column Address Hold Time Referenced to $\overline{RAS}$ Rise	10		15		ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	25		30		ns	
t_{LWAD}	Last Write to Column Address Delay Time	25	45	30	55	ns	17
t_{AHLW}	Last Write to Column Address Hold Time	95		115		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511002P/J-10		TC511002P/J-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RCS}	Read Command Set-up Time Referenced to $\overline{CS}$	0		0		ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CS}$	0		0		ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0		0		ns	12
t_{WCR}	Write Command Hold Time Referenced $\overline{RAS}$	75		90		ns	
t_{WP}	Write Command Pulse Width	20		25		ns	
t_{WI}	Write Command Inactive Time	10		15		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		ns	
t_{DS}	Data-In Set-Up Time	0		0		ns	11
t_{DH}	Data-In Hold Time	20		25		ns	11
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	75		90		ns	
t_{REF}	Refresh Period		8		8	ms	
t_{WS}	Write Command Set-Up Time (Output Data Disable)	0		0		ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	35		45		ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	100		120		ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	50		60		ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10		10		ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30		30		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0		0		ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	50		60		ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15		20		ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0~70°C)

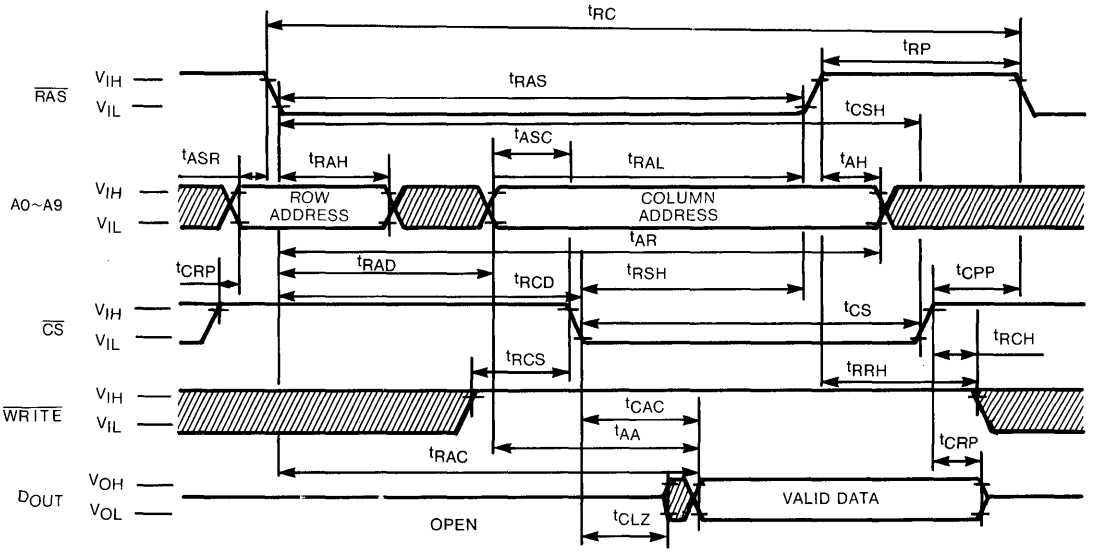
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})		5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$)		7	pF
C_O	Output Capacitance (D_{OUT})		7	pF

NOTES:

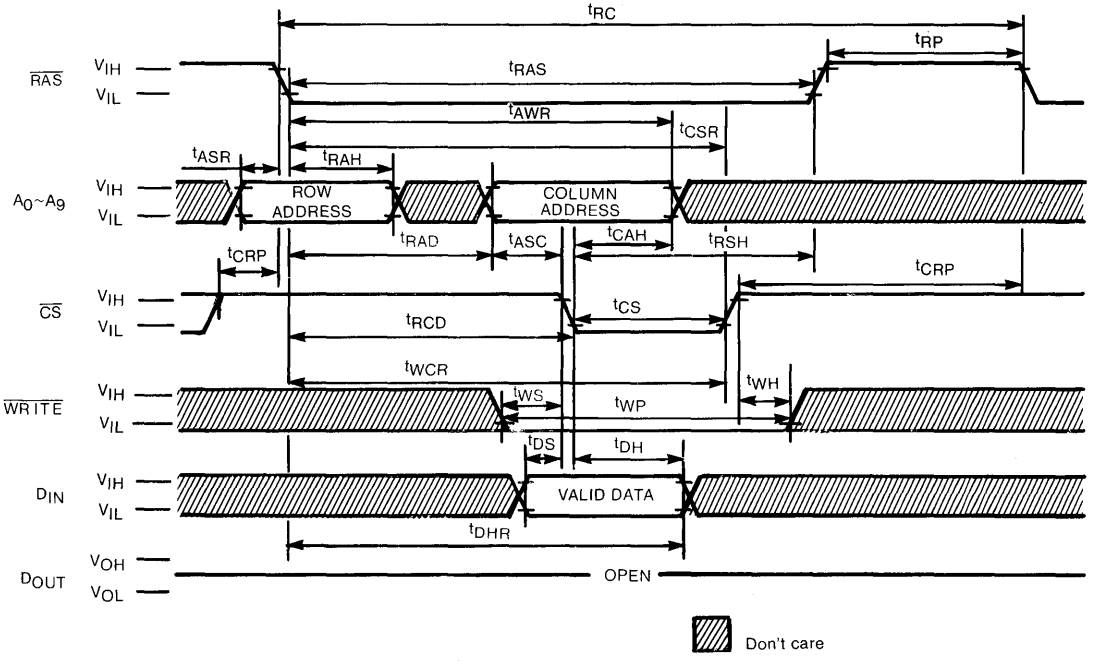
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycle.
12. t_{WS}, t_{WH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WS} \geqq t_{WS}$(min.) and $t_{WH} \geqq t_{WH}$(min.), the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

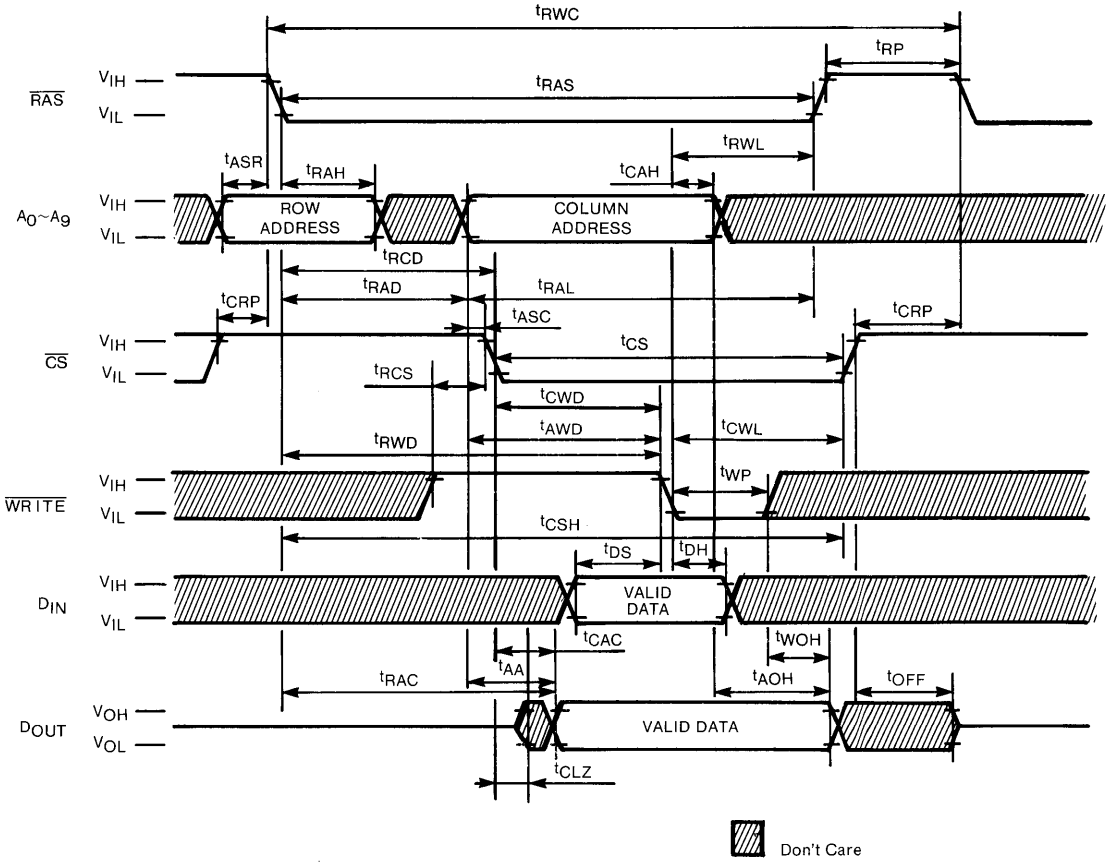
READ CYCLE



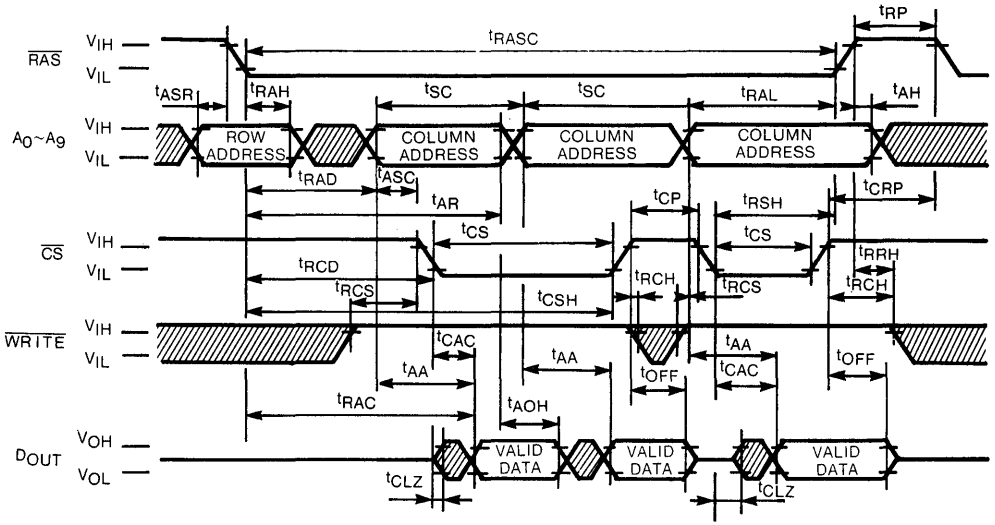
WRITE CYCLE (EARLY WRITE)



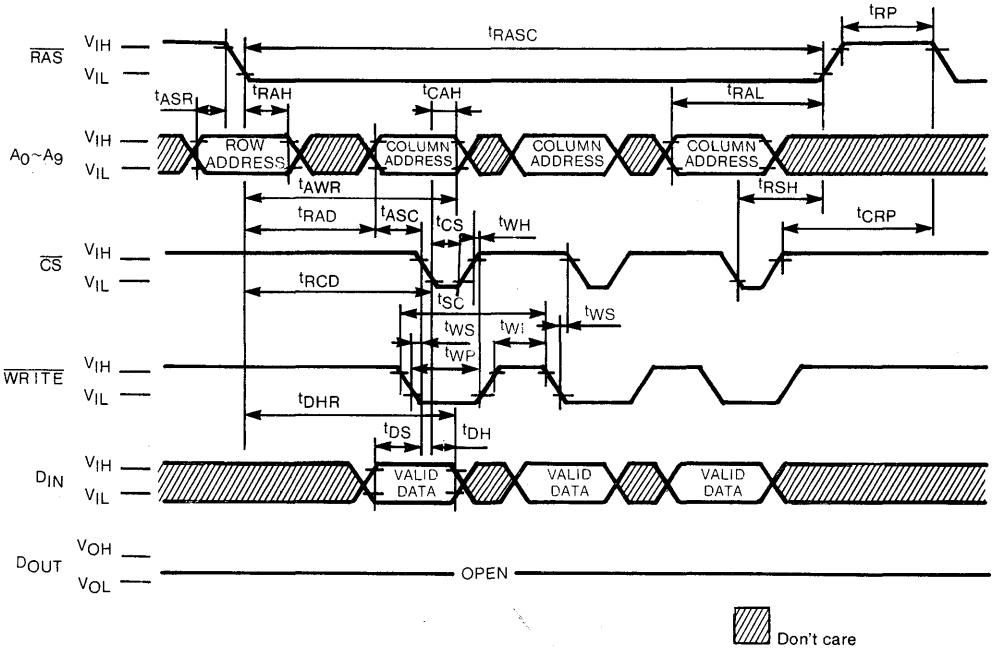
READ-WRITE CYCLE



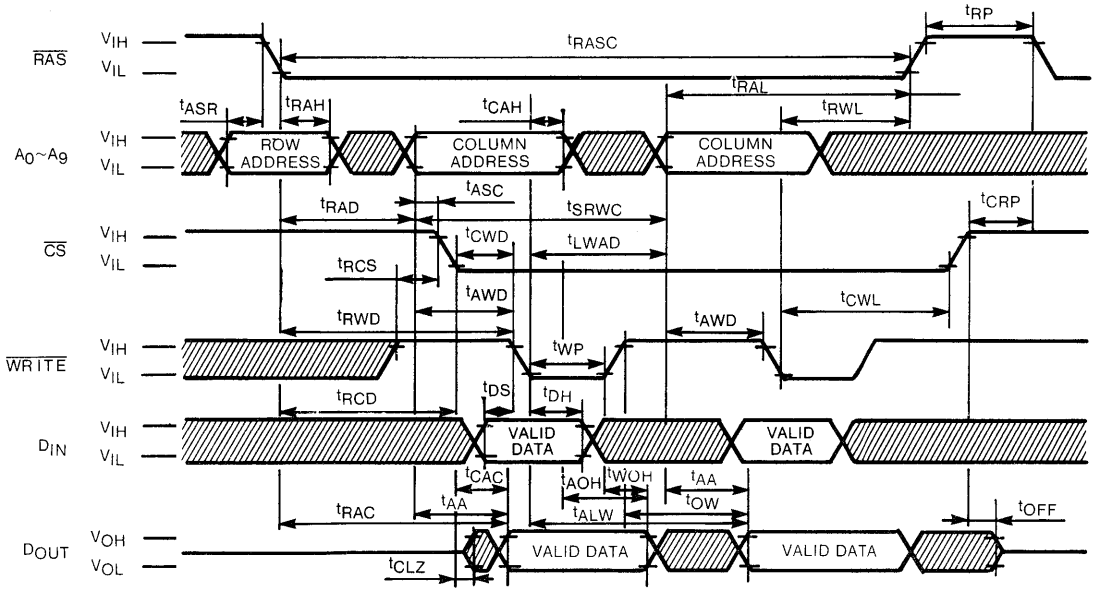
STATIC COLUMN MODE READ CYCLE



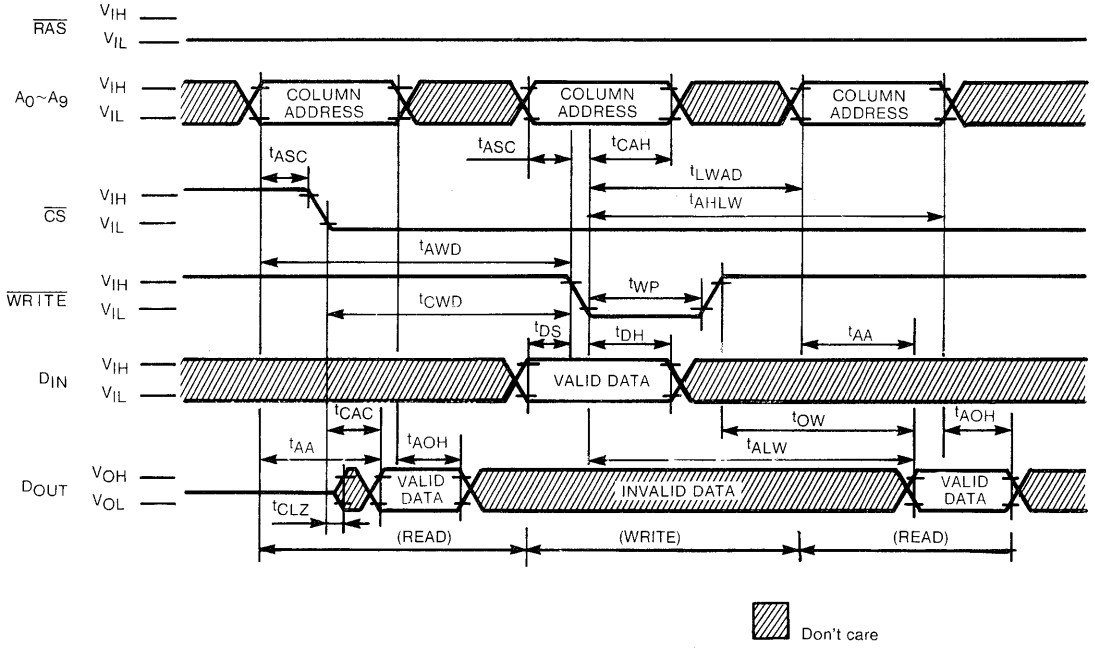
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



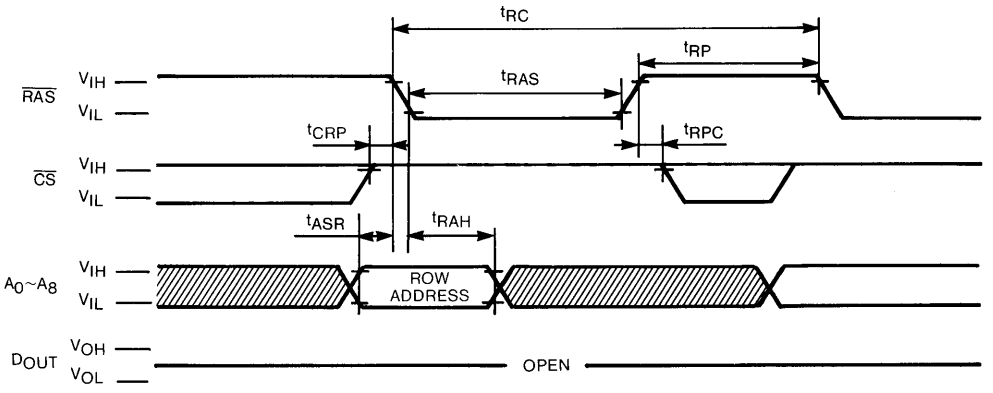
STATIC COLUMN MODE READ-WRITE CYLCE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE



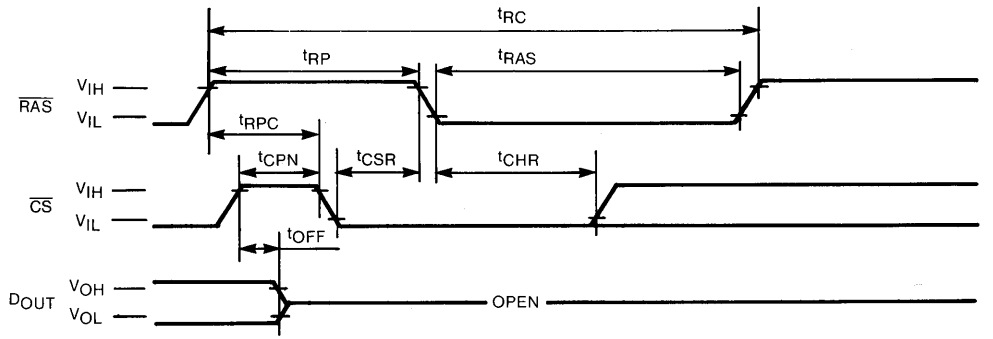
$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$=Don't care, A9=Don't care

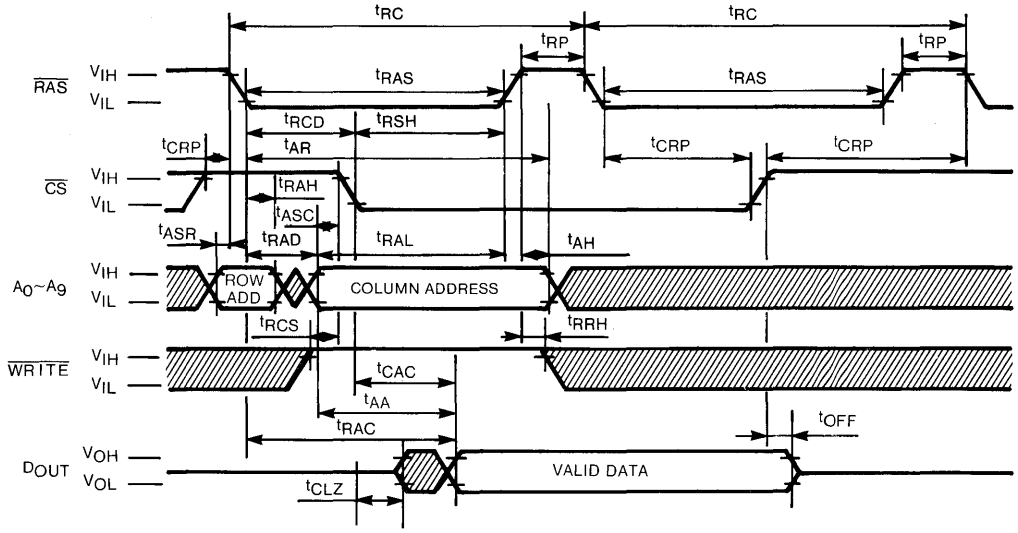
Don't Care

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

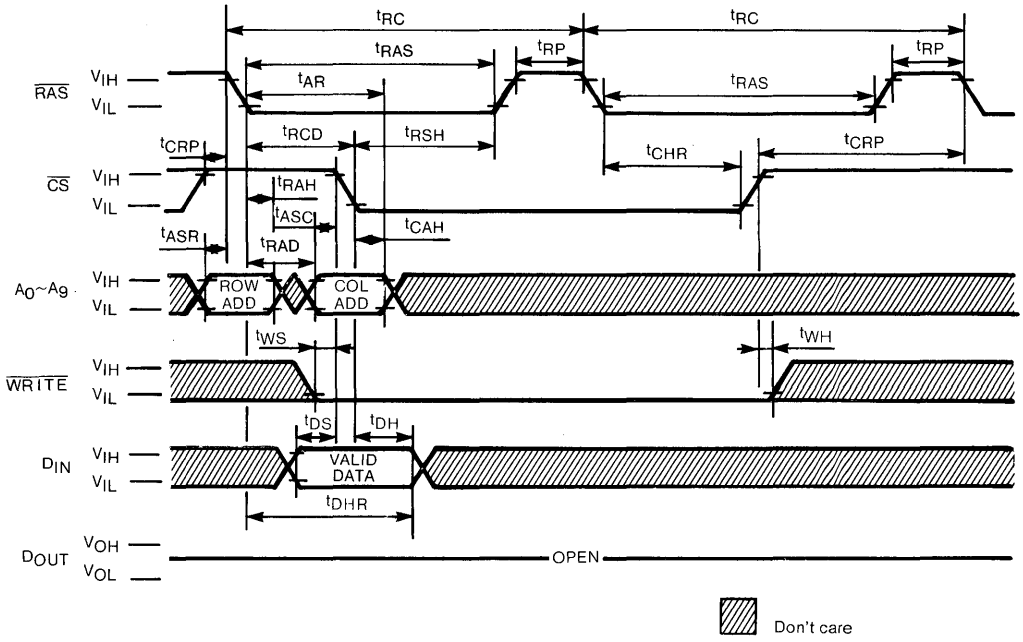


NOTE: $\overline{WRITE}$=Don't care, A0~A9=Don't care

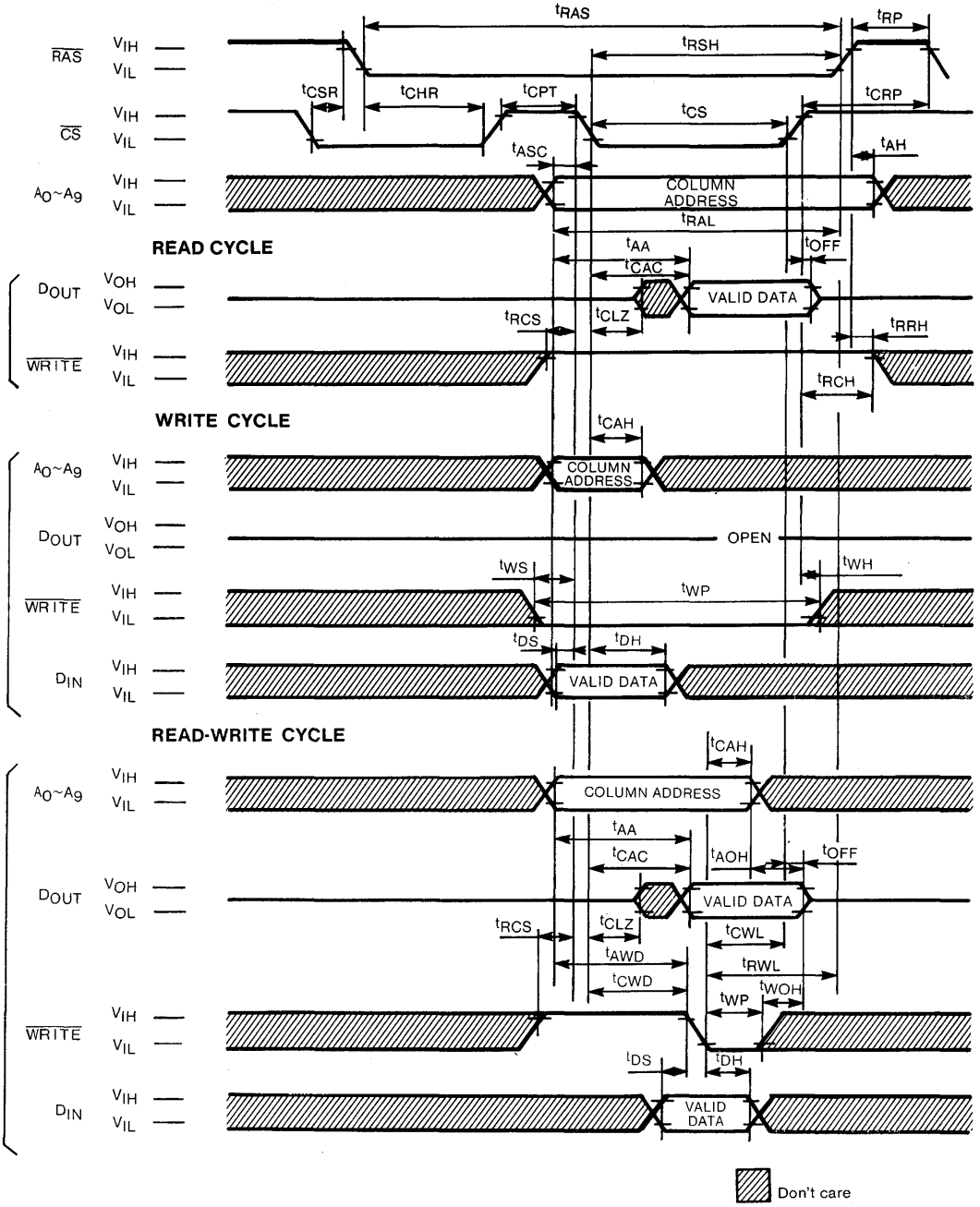
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



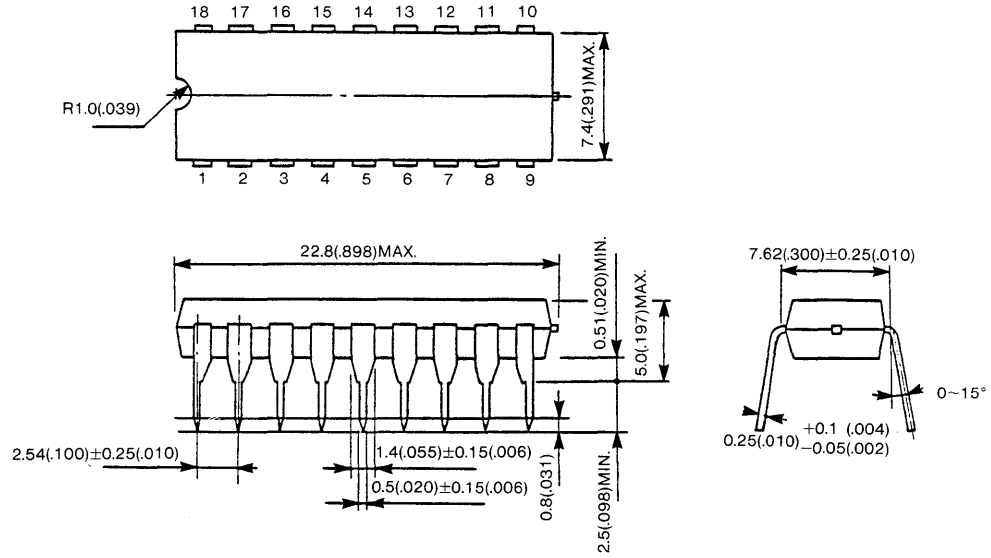
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

Unit in mm(inches)

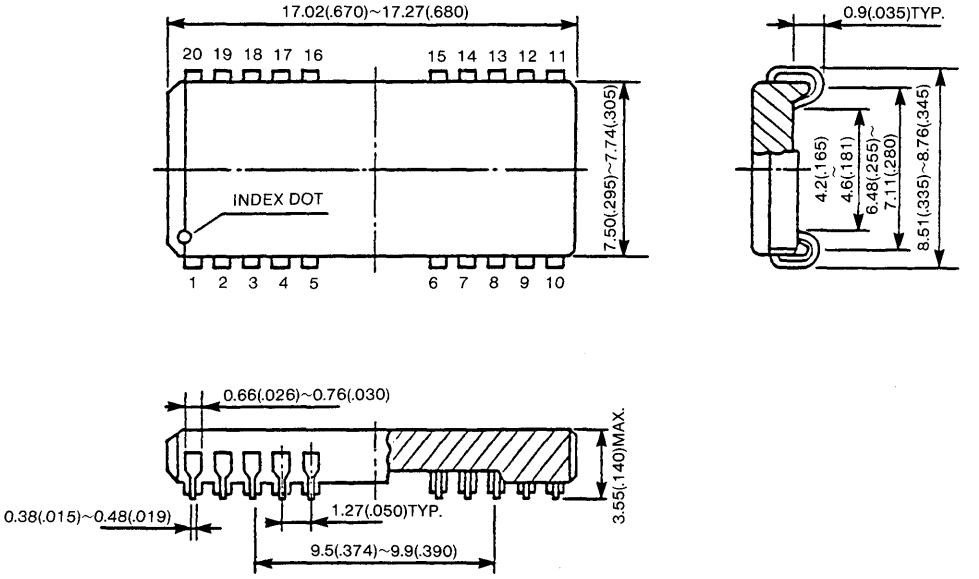
- **Plastic DIP**



Note: Each lead pitch is 2.54(.100) mm. All leads are located within 0.25(.010)mm of their true longitudinal position with respect to No. 1 and No. 18 leads.

Unit in mm(inches)

- **Plastic SOJ**



Note : Each lead pitch 1.27(.050)mm.

Note : Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

NMOS Standard Application Static Memories

TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM

TMM2015AP-90, TMM2015AP-12
TMM2015AP-10, TMM2015AP-15

DESCRIPTION

The TMM2015AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 80mA/65mA/65mA/65mA. When $\overline{CS}$ is a logical high, the device is placed in a low power standby mode in which maximum standby current is 7mA. Thus the TMM2015AP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

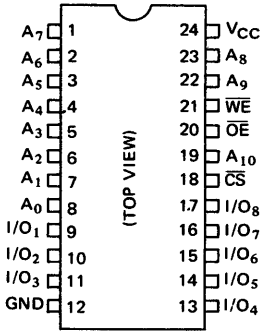
FEATURES

- Access Time and Current

Parameter / Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2015AP-90	90ns	80mA	7mA
TMM2015AP-10	100ns	65mA	7mA
TMM2015AP-12	120ns	65mA	7mA
TMM2015AP-15	150ns	65mA	7mA

- High Density Assembly Capability:
  0.3 inch package
  (24 pins plastic DIP)
- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS}$
- Output Buffer Control: $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

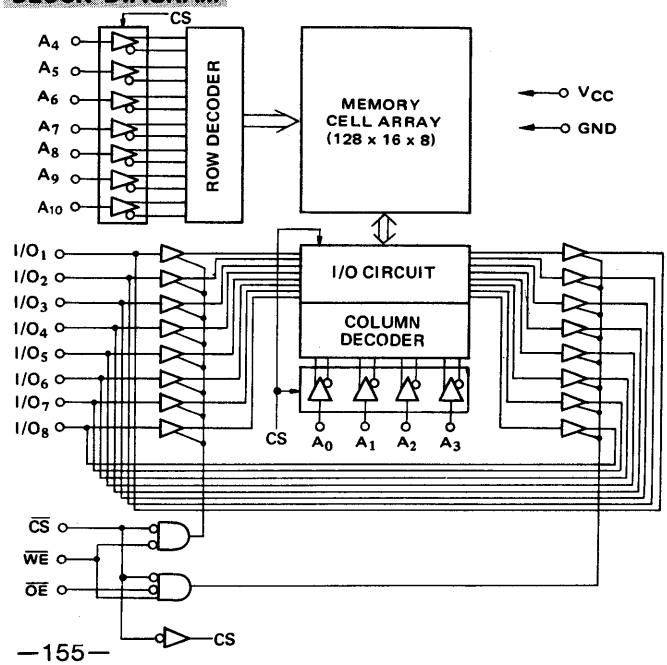
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_{10}$	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5 ~ 7.0	V
$T_{OPR.}$	Operating Temperature	0 ~ 70	°C
$T_{STG.}$	Storage Temperature	−55 ~ 150	°C
$T_{SOLDER.}$	Soldering Temperature • Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	0.7	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

D.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V ~ 5.5V	−10	–	10	μA
V_{OH}	Output High Voltage	I_{OUT} = −1.0mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA	–	–	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V ~ 5.5V	−10	–	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$ = V_{CC}, I_{OUT} = 0mA	–	–	30	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH}, I_{OUT} = 0mA	–	–	7	mA
I_{CC1}	Operating Current TMM2015AP-10/-12/-15	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	65	mA
I_{CC2}	Operating Current TMM2015AP-90	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	80	mA

CAPACITANCE* (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0v	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0v	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TMM2015AP-90		TMM2015AP-10		TMM2015AP-12		TMM2015AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	–	100	–	120	–	150	–	ns
t_{ACC}	Address Access Time	–	90	–	100	–	120	–	150	ns
t_{CO}	Chip Select Access Time	–	90	–	100	–	120	–	150	ns
t_{OE}	Output Enable Time	–	35	–	35	–	50	–	55	ns
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	10	–	10	–	ns
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	10	–	10	–	10	–	10	–	ns
t_{CHZ}	$\overline{CS}$ to Output in High-Z	–	40	–	40	–	40	–	55	ns
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{OHZ}	$\overline{OE}$ to Output in High-Z	–	35	–	35	–	35	–	50	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	50	–	50	–	60	–	60	ns

WRITE CYCLE

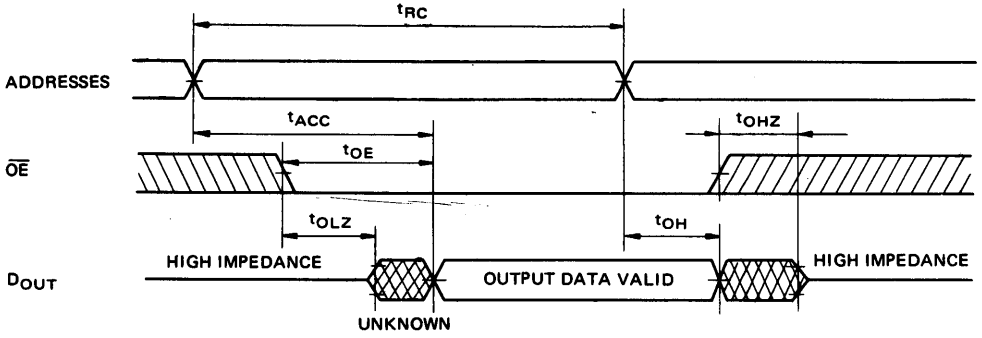
SYMBOL	PARAMETER	TMM2015AP-90		TMM2015AP-10		TMM2015AP-12		TMM2015AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	–	100	–	120	–	150	–	ns
t_{CW}	Chip Selection to End of Write	70	–	80	–	100	–	120	–	ns
t_{AS}	Address Set up Time	20	–	20	–	20	–	20	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	85	–	100	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DS}	Data Set up Time	35	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{WHZ}	$\overline{WE}$ to Output in High-Z	–	25	–	30	–	35	–	50	ns

A.C. TEST CONDITIONS

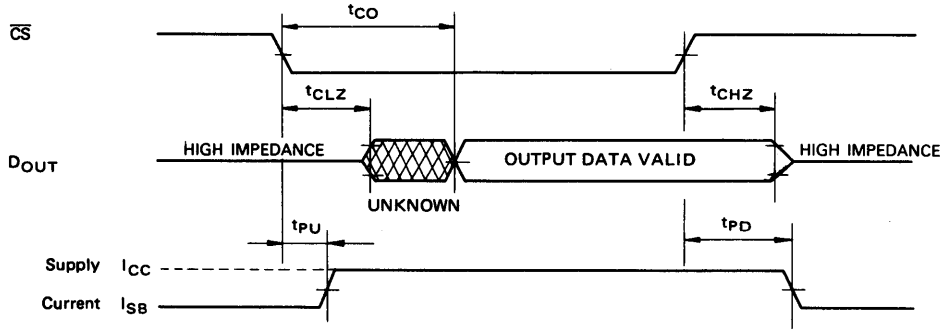
Input Pulse Levels	$0 \sim 3.5V$
Input Rise and Fall Time	10 ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100pF$

TIMING WAVEFORMS

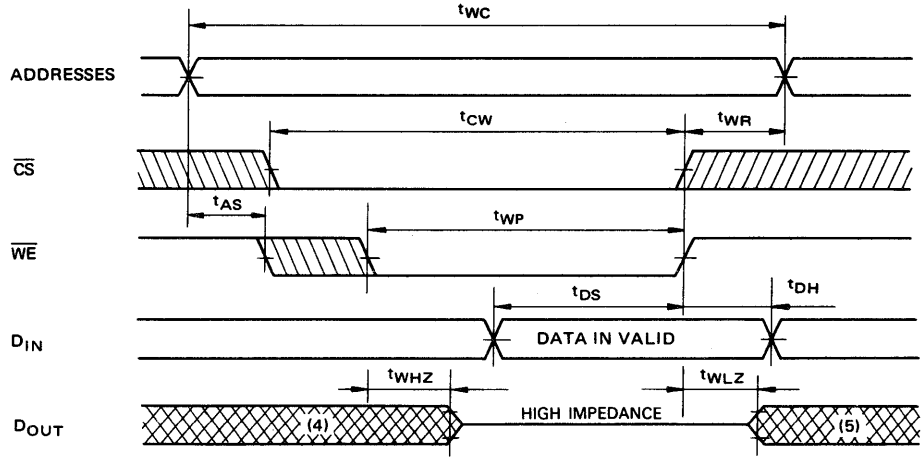
(A) READ CYCLE [1] (1)

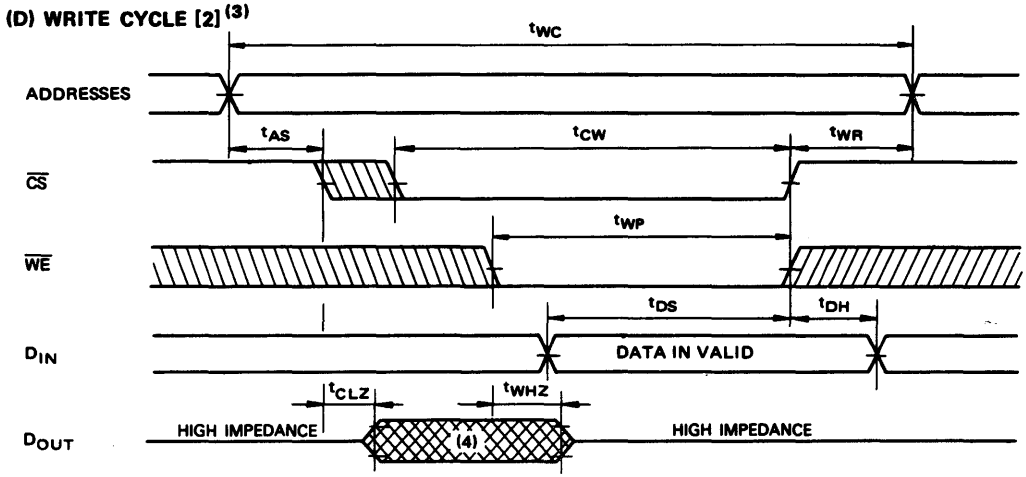


(B) READ CYCLE [2] (1)(2)



(C) WRITE CYCLE [1] (3)





Note: (1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS}$ = V_{IL} in read cycle [1].

(2) All addresses are valid prior to or simultaneously with $\overline{CS}$ transitions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{CW} is specified as the time from the chip selection to end of write in write cycle, and the t_{WP} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high, the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transition occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaneously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time
(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

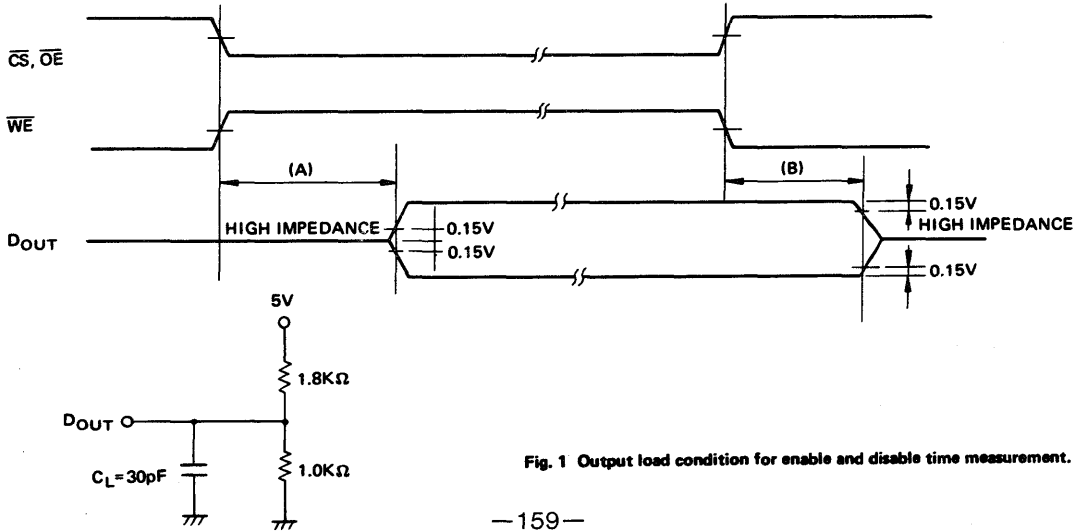
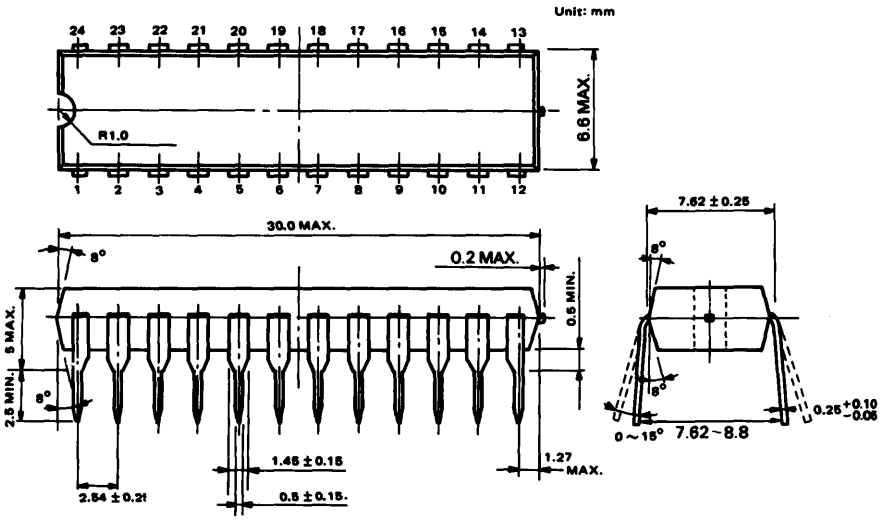


Fig. 1 Output load condition for enable and disable time measurement.

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

2,048 WORD × 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2015BP-90, TMM2015BP-12
TMM2015BP-10, TMM2015BP-15

DESCRIPTION

The TMM2015BP is a 16, 384 bits high speed and low power static random access memory organized as 2, 048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 50mA. When $\overline{CS}$ is a logical high, the device is placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2015BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2015BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

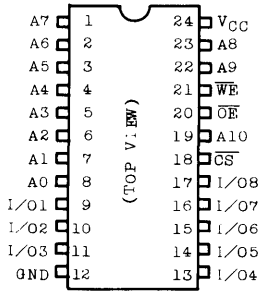
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2015BP-90	90ns	50mA	5mA
TMM2015BP-10	100ns	50mA	5mA
TMM2015BP-12	120ns	50mA	5mA
TMM2015BP-15	150ns	50mA	5mA

- High Density Assembly Capability:
  0.3 inch width package (24pin plastic DIP)
- Single 5V power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS}$
- Output Buffer Control: $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

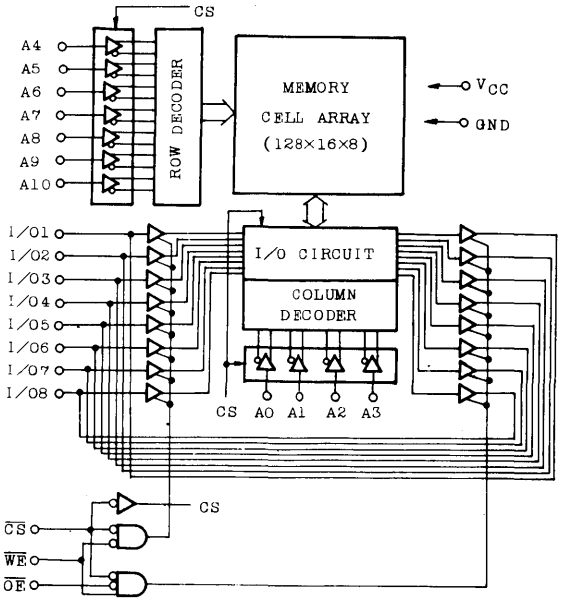
PIN CONNENCTION



PIN NAMES

$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_{10}$	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Terperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation(Ta=70°C)	0.7	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Vovtage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=4.0mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0v~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, I_{OUT}=0mA	—	—	10	mA
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}, I_{OUT}=0mA	—	—	5	mA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}, I_{OUT}=0mA	—	—	50	mA

CAPACITANCE*** (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

*** Note : This paramenter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	—	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	90	—	100	—	120	—	150	
t_{CO}	Chip Select Access Time	—	90	—	100	—	120	—	150	
t_{OE}	Output Enable Time	—	35	—	35	—	50	—	55	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	15	—	15	—	15	—	15	—	
t_{CHZ}	$\overline{CS}$ to Output in High-Z	—	40	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	35	—	50	
t_{PU}	Chip Selection to power Up Time	0	—	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	

Write Cycle

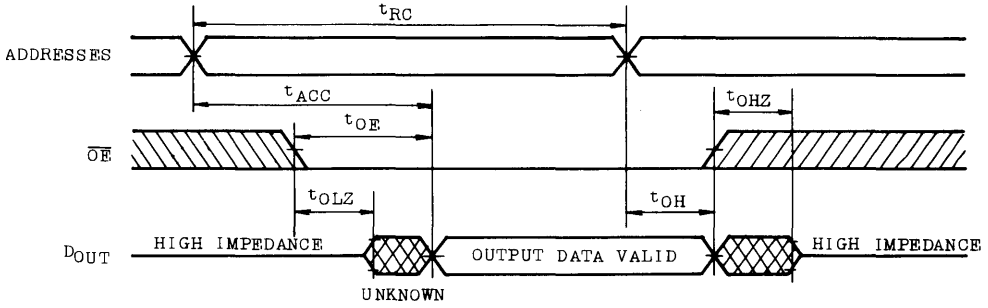
SYMBOL	PARAMETER	TMM2015BP-90		TMM2015BP-10		TMM2015BP-12		TMM2015BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	—	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	60	—	70	—	85	—	100	—	
t_{AS}	Address Set Up Time	20	—	20	—	20	—	20	—	
t_{WP}	Write Pulse Width	55	—	65	—	80	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	30	—	35	—	45	—	50	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	25	—	30	—	35	—	50	

A. C. TEST CONDITIONS

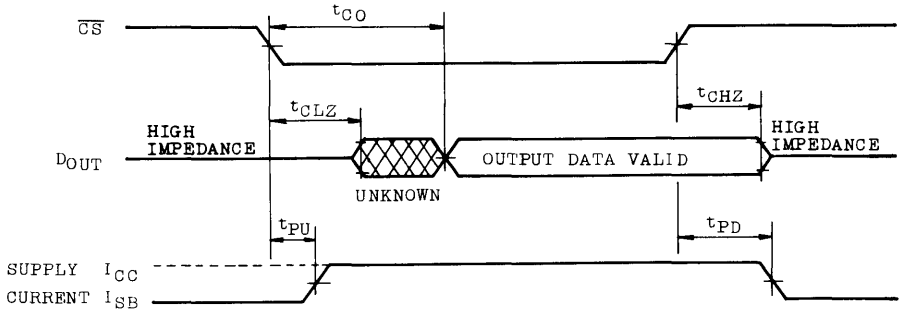
Input Pulse Levels	0~3.5V
Input Rise and Fall Time	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100pF$

TIMING WAVEFORMS

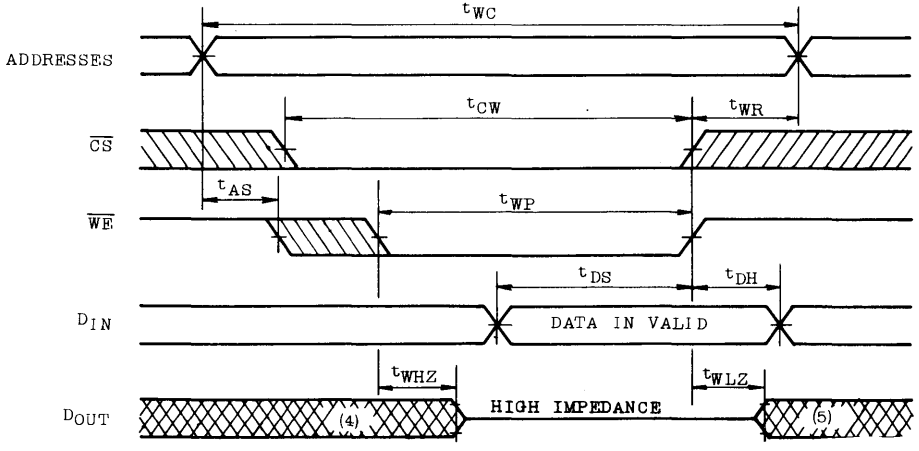
- (A) READ CYCLE [1] (1)



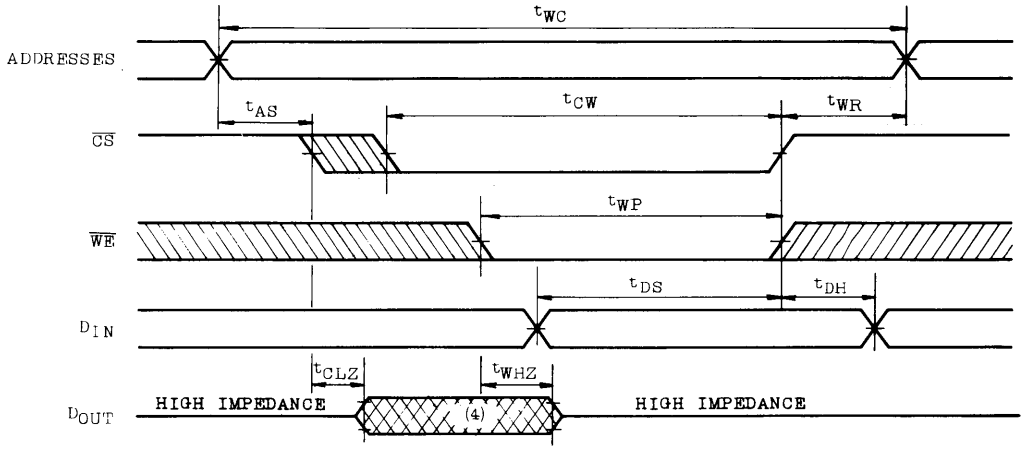
- (B) READ CYCLE [2] (1), (2)



- (C) WRITE CYCLE [1] (3)



• (D) WRITE CYCLE (2) (3)



NOTES:

(1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS}$ = V_{IL} in read cycle (1)

(2) All addresses are valid perior to or simultaneously with $\overline{CS}$ transitions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{cw} is specified as the time from the chip selection to end of write in write cycle, and the t_{wp} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high, the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transition occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaneously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ····· Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ····· Output Disable Time

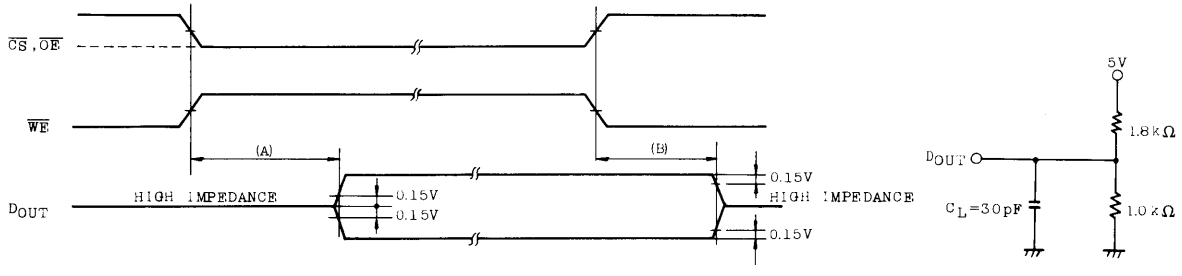
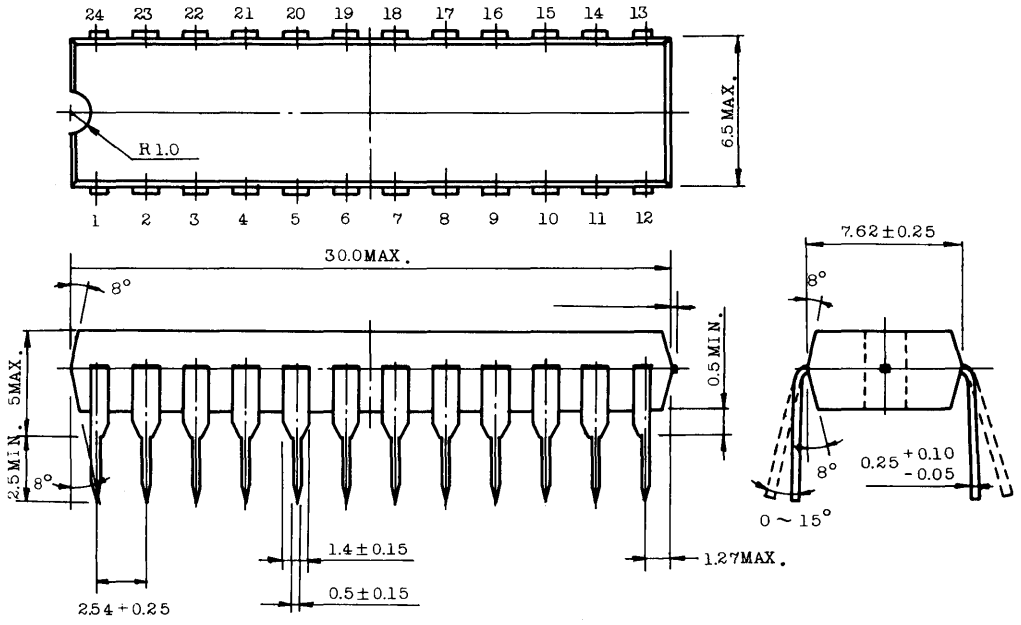


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT STATIC RAM

TMM2016AP-90, TMM2016AP-12
TMM2016AP-10, TMM2016AP-15

DESCRIPTION

The TMM2016AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 80mA/65mA/65mA/65mA. When $\overline{CS}$ is a logical high, the device is placed in a low power standby mode in which maximum standby current is 7mA. Thus the TMM2016AP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2016AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

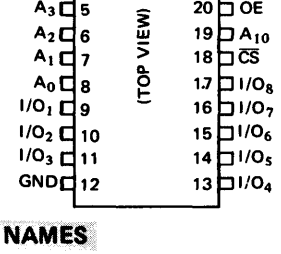
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2016AP-90	90ns	80mA	7mA
TMM2016AP-10	100ns	65mA	7mA
TMM2016AP-12	120ns	65mA	7mA
TMM2016AP-15	150ns	65mA	7mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS}$
- Output Buffer Control: $\overline{OE}$
- Three Stage Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have prtoection against static charge.

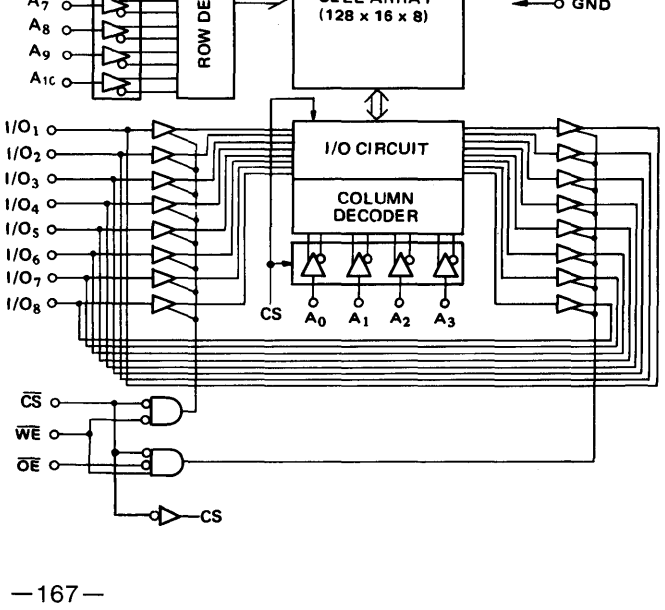
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_{10}$	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5 ~ 7.0	V
$T_{OPR.}$	Operating Temperature	0 ~ 70	°C
$T_{STG.}$	Storage Temperature	−55 ~ 150	°C
$T_{SOLDER.}$	Soldering Temperature • Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

D.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V ~ 5.5V	−10	–	10	μA
V_{OH}	Output High Voltage	I_{OUT} = −1.0mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA	–	–	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0V ~ 5.5V	−10	–	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$ = V_{CC}, I_{OUT} = 0mA	–	–	30	mA
I_{SB}	Standby Current	$\overline{CS}$ = V_{IH}, I_{OUT} = 0mA	–	–	7	mA
I_{CC1}	Operating Current TMM2016AP-10/-12/-15	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	65	mA
I_{CC2}	Operating Current TMM2016AP-90	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	–	–	80	mA

CAPACITANCE* (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TMM2016AP-90		TMM2016AP-10		TMM2016AP-12		TMM2016AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	–	100	–	120	–	150	–	ns
t_{ACC}	Address Access Time	–	90	–	100	–	120	–	150	ns
t_{CO}	Chip Select Access Time	–	90	–	100	–	120	–	150	ns
t_{OE}	Output Enable Time	–	35	–	35	–	50	–	55	ns
t_{OH}	Output Data Hold Time from Address Change	10	–	10	–	10	–	10	–	ns
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	10	–	10	–	10	–	10	–	ns
t_{CHZ}	$\overline{CS}$ to Output in High-Z	–	40	–	40	–	40	–	55	ns
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{OHZ}	$\overline{OE}$ to Output in High-Z	–	35	–	35	–	35	–	50	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	50	–	50	–	60	–	60	ns

WRITE CYCLE

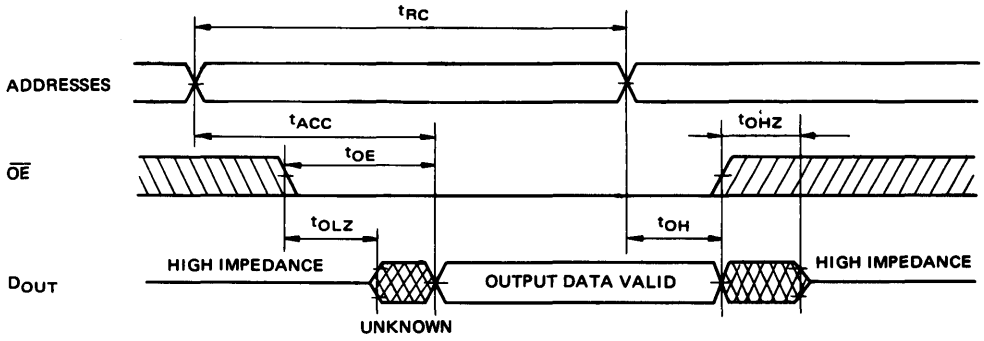
SYMBOL	PARAMETER	TMM2016AP-90		TMM2016AP-10		TMM2016AP-12		TMM2016AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	–	100	–	120	–	150	–	ns
t_{CW}	Chip Selection to End of Write	70	–	80	–	100	–	120	–	ns
t_{AS}	Address Set up Time	20	–	20	–	20	–	20	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	85	–	100	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DS}	Data Set up Time	35	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{WHZ}	$\overline{WE}$ to Output in High-Z	–	25	–	30	–	35	–	50	ns

A.C. TEST CONDITIONS

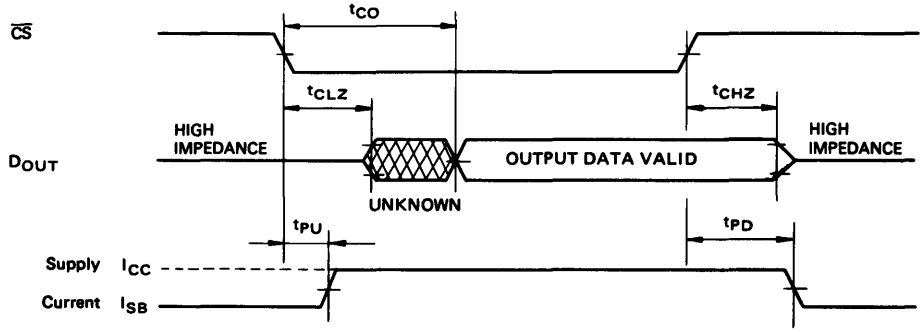
Input Pulse Levels	$0 \sim 3.5V$
Input Rise and Fall Time	10 ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100pF$

TIMING WAVEFORMS

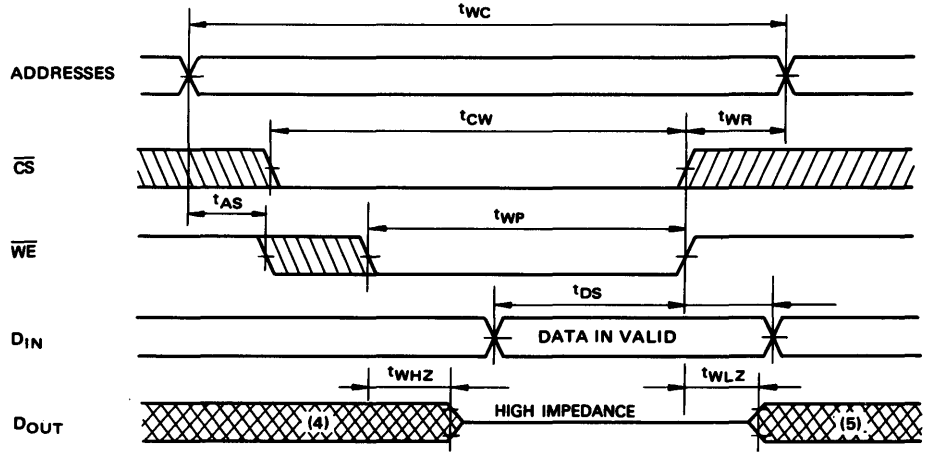
(A) READ CYCLE [1] (1)

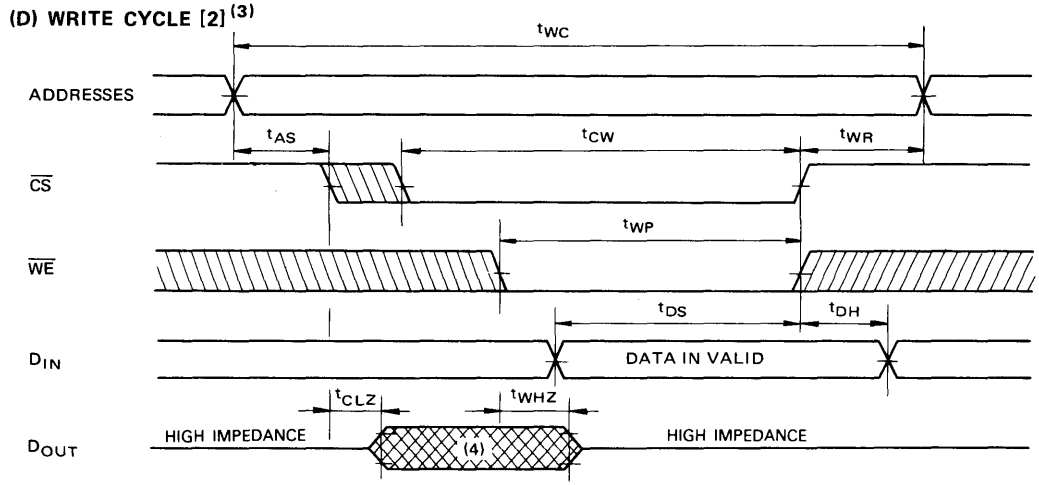


(B) READ CYCLE [2] (1)(2)



(C) WRITE CYCLE [1] (3)





Note: (1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS}$ = V_{IL} in read cycle [1].

(2) All addresses are valid perior to or simultaneously with $\overline{CS}$ transistions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{CW} is specified as the time from the chip selection to end of write in write cycle, and the t_{WP} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high, the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transistion occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaneously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time
(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

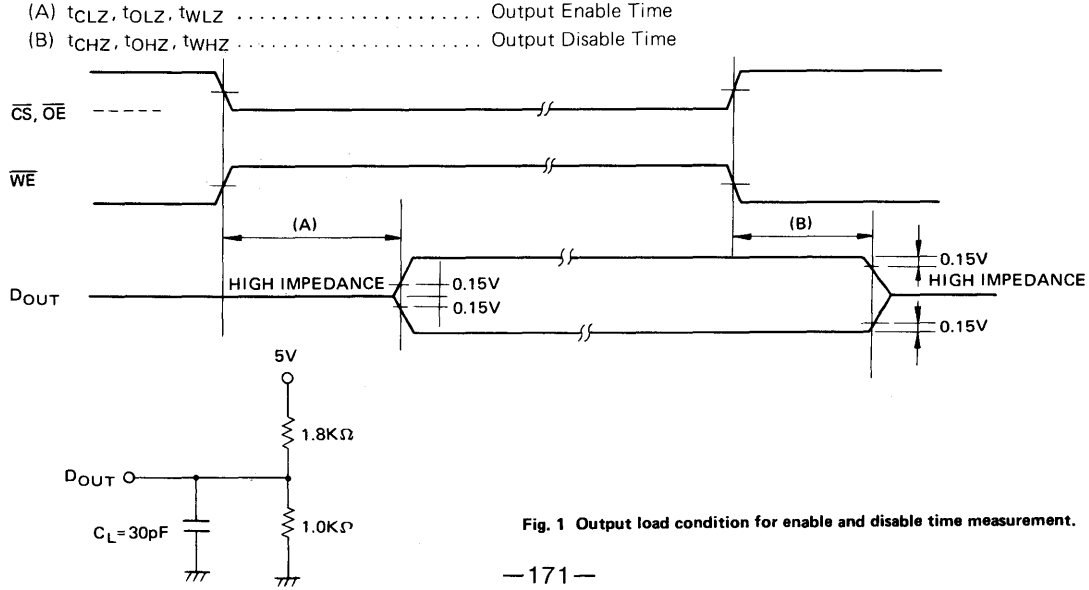
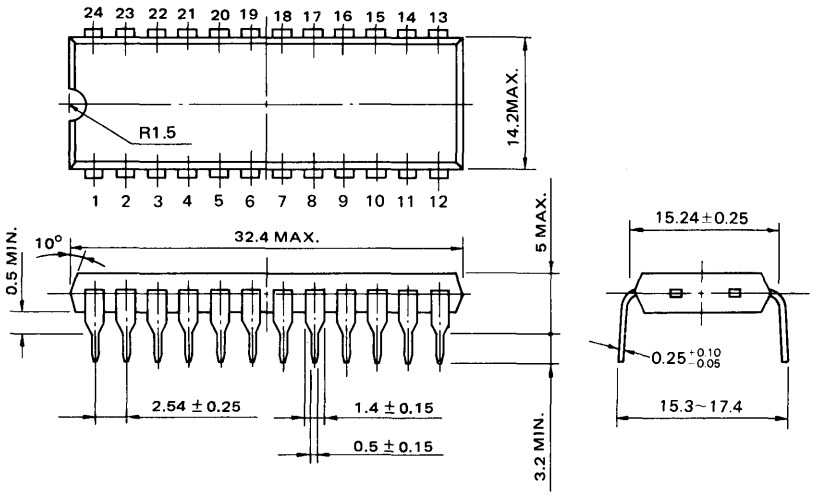


Fig. 1 Output load condition for enable and disable time measurement.

OUTLINE DRAWINGS

Unit: mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

2,048 WORD × 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2016BP-90, TMM2016BP-12
TMM2016BP-10, TMM2016BP-15

DESCRIPTION

The TMM2016BP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns /120ns/150ns and maximum operating current of 50mA. When $\overline{CS}$ is logical high, the device is placed in a low power standby mode in which maximum standby current is 5mA. Thus the TMM2016BP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2016BP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

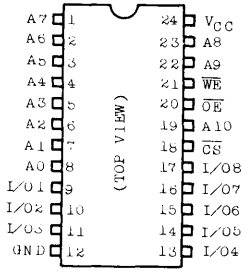
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2016BP-90	90ns	50mA	5mA
TMM2016BP-10	100ns	50mA	5mA
TMM2016BP-12	120ns	50mA	5mA
TMM2016BP-15	150ns	50mA	5mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS}$
- Output Buffer Control: $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

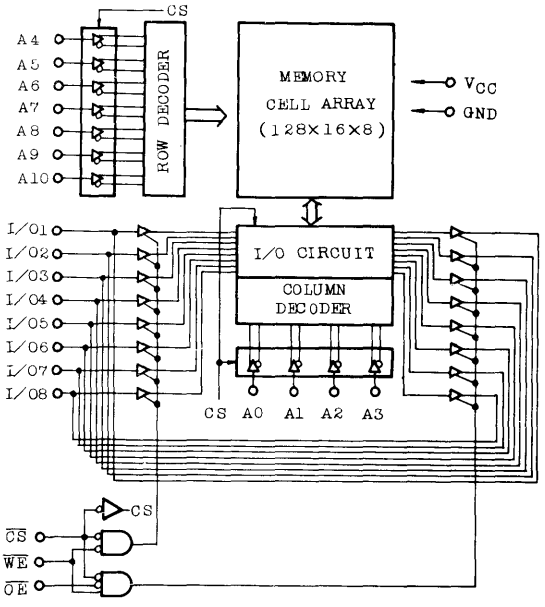
PIN CONNECTION



PIN NAMES

A_0~A_3	Column Address Inputs
A_4~A_{10}	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
I/O_1~I/O_8	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Terperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation(Ta=70°C)	1.0	W

* −3.0V at Pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Vovtage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=4.0mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, I_{OUT}=0mA	—	—	10	mA
I_{SB}	Standby Current	$\overline{CS}$=V_{IH} , I_{OUT}=0mA	—	—	5	mA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}, I_{OUT}=0mA	—	—	50	mA

CAPACITANCE*** (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

*** Note : This paramenter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2016BP-90		TMM2016BP-10		TMM2016BP-12		TMM2016BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	90	—	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	90	—	100	—	120	—	150	
t_{CO}	Chip Select Access Time	—	90	—	100	—	120	—	150	
t_{OE}	Output Enable Time	—	35	—	35	—	50	—	55	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	15	—	15	—	15	—	15	—	
t_{CHZ}	$\overline{CS}$ to Output in High-Z	—	40	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	35	—	50	
t_{PU}	Chip Selection to power Up Time	0	—	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	

Write Cycle

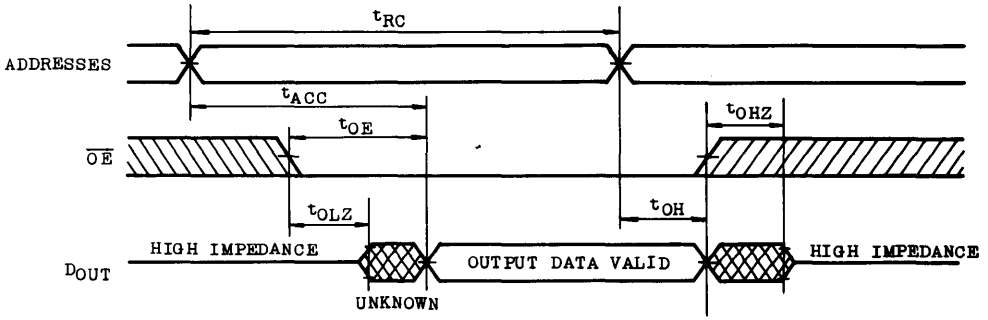
SYMBOL	PARAMETER	TMM2016BP-90		TMM2016BP-10		TMM2016BP-12		TMM2016BP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	90	—	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	60	—	70	—	85	—	100	—	
t_{AS}	Address Set Up Time	20	—	20	—	20	—	20	—	
t_{WP}	Write Pulse Width	55	—	65	—	80	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	30	—	35	—	45	—	50	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	25	—	30	—	35	—	50	

A. C. TEST CONDITIONS

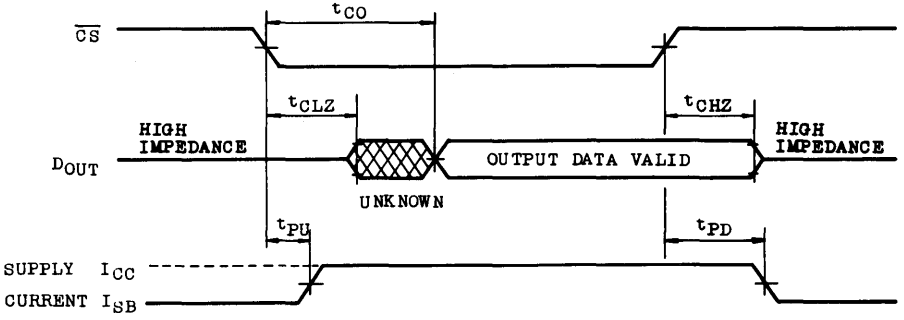
Input Pulse Levels	0~3.5V
Input Rise and Fall Time	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate & C_L=100pF

TIMING WAVEFORMS

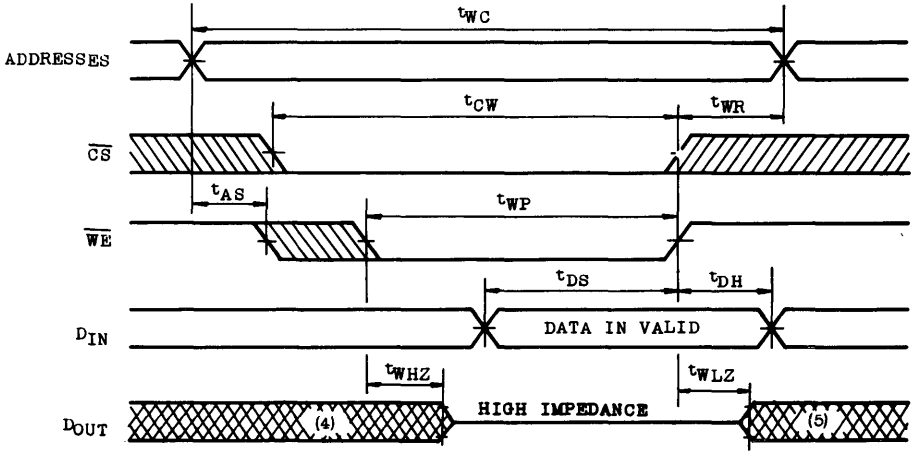
- (A) READ CYCLE [1] (1)



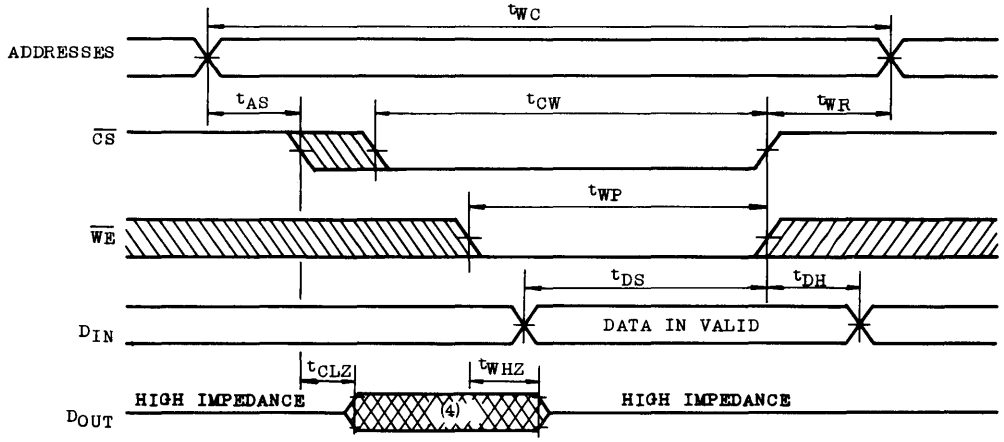
- (B) READ CYCLE [2] (1), (2)



- (C) WRITE CYCLE [1] (3)



• (D) WRITE CYCLE (2) (3)



NOTES:

(1) The $\overline{WE}$ is high for read cycle.
Device is continuously selected, $\overline{CS}=V_{IL}$ in read cycle (1)

(2) All adresses are valid perior to or simultaneously with $\overline{CS}$ transitions.

(3) A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.
The t_{cw} is specified as the time from the chip selection to end of write in write cycle , and the t_{wp} is specified as the overlap time of low $\overline{CS}$ and low $\overline{WE}$.
$\overline{OE}$ is allowed to be low or high level in write cycle.
If the $\overline{OE}$ is high , the output buffers remain in a high impedance state in this period.

(4) If the $\overline{CS}$ low transition occurs simultaneously with or latter to the $\overline{WE}$ low transition, the output buuffers remain in a high impedance state in this period.

(5) If the $\overline{CS}$ high transition occurs simultaeously with $\overline{WE}$ high transition, the output buffers remain in a high impedance state in this period.

Thease parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

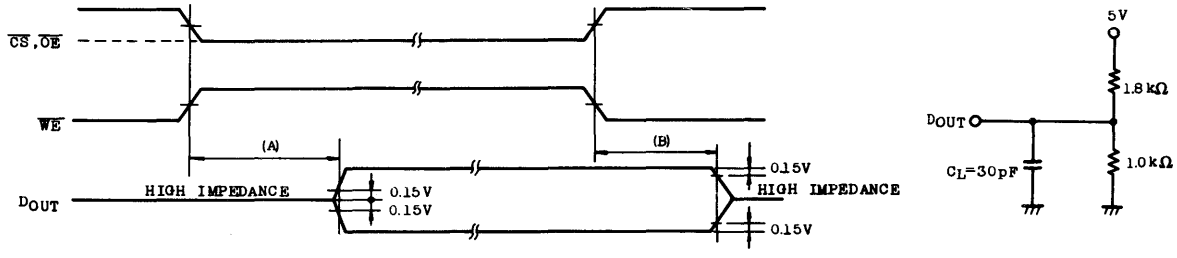
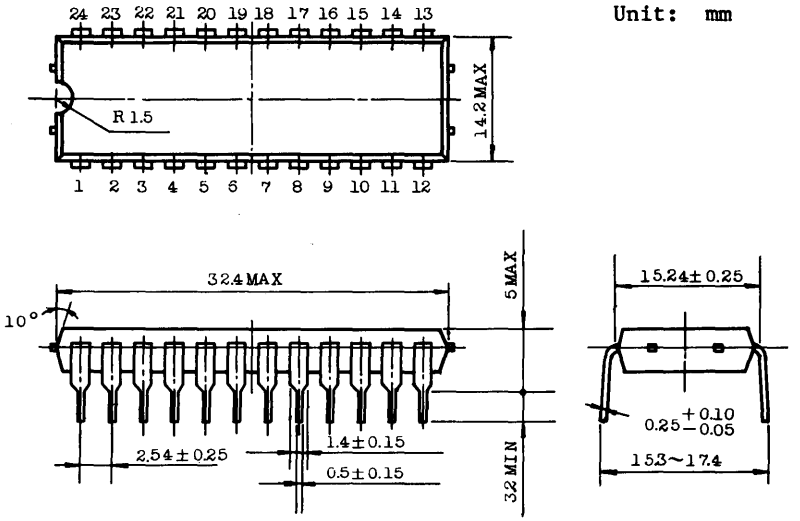


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2063P-10, TMM2063P-12 TMM2063P-15

DESCRIPTION

The TMM2063P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When $\overline{CS_1}$ is a logical high or CS_2 is a logical low, the device is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2063P is most suitable for use in microcomputer peripheral memory where the low power applications are required, moreover, suitable for use in high density assembly as 0.3 inch width package is use for. The TMM2063P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

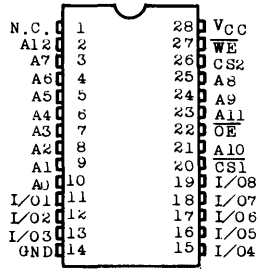
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2063P-10	100ns	80mA	10mA
TMM2063P-12	120ns	80mA	10mA
TMM2063P-15	150ns	80mA	10mA

- High Density Assembly Capability : 0.3 inch width package (28 pin plastic DIP)
- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : $\overline{CS_1}$, CS_2
- Output Buffer Control : $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge.

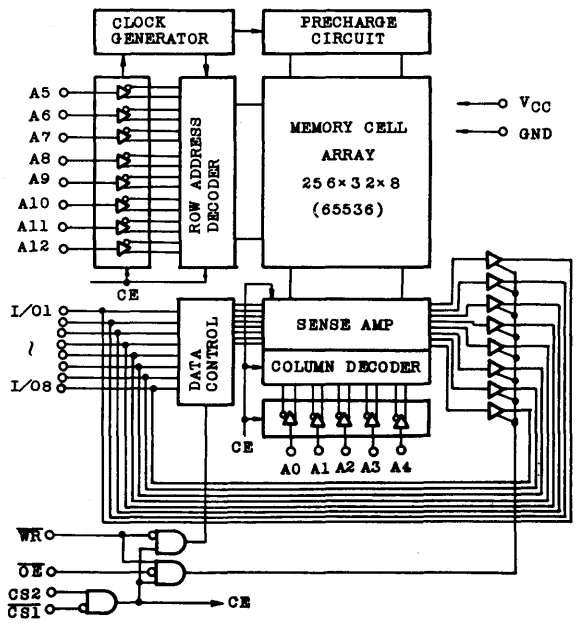
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_4$	Column Address Inputs
$A_5 \sim A_{12}$	Row Address Inputs
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	0.8	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=2.1mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS_1}$=V_{CC}, CS_2=0V I_{OUT}=0mA	—	—	20	mA
I_{SB}	Standby Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, I_{OUT}=0mA	—	—	10	mA
I_{CC}	Operating Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{OUT}=0mA	—	—	80	mA

CAPACITANCE*** (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CS_1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CS_2 Access Time	—	100	—	120	—	150	
t_{OE}	$\overline{OE}$ Access Time	—	40	—	50	—	60	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS_1}$ or CS_2 to Output in Low-Z	10	—	10	—	10	—	
t_{CHZ}	$\overline{CS_1}$ or CS_2 to Output in High-Z	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	50	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	60	—	60	

Write Cycle

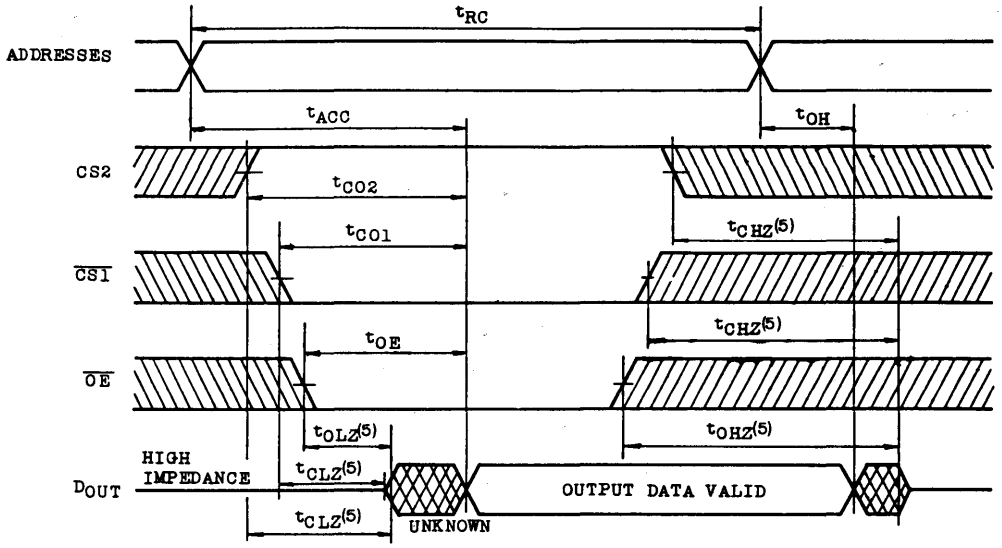
SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	80	—	100	—	120	—	
t_{AS}	Address Set Up Time	10	—	10	—	10	—	
t_{WP}	Write Pulse Width	70	—	85	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	30	—	35	—	40	

A. C. TEST CONDITIONS

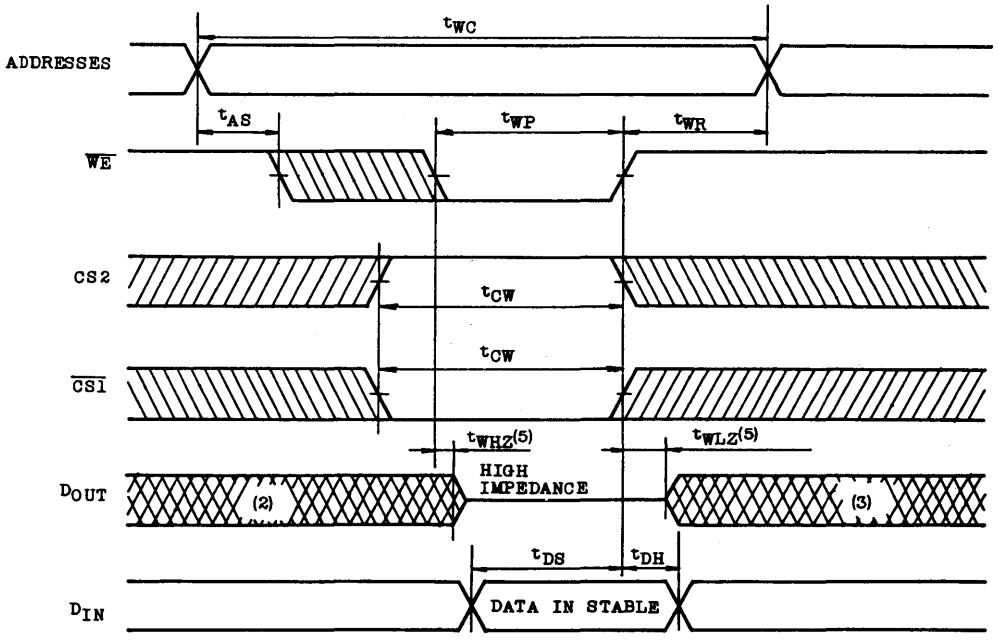
Input Pulse Levels	$V_{IH} = 2.2V$, $V_{IL} = 0.6V$
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100pF$

TIMING WAVEFORMS

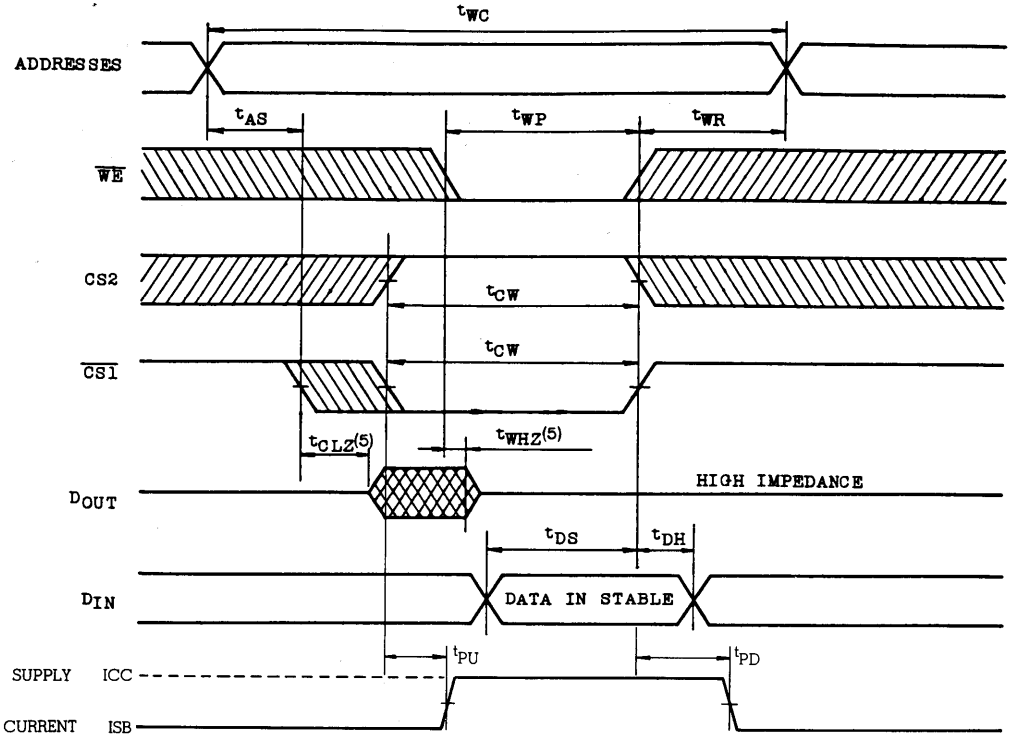
- READ CYCLE (1)



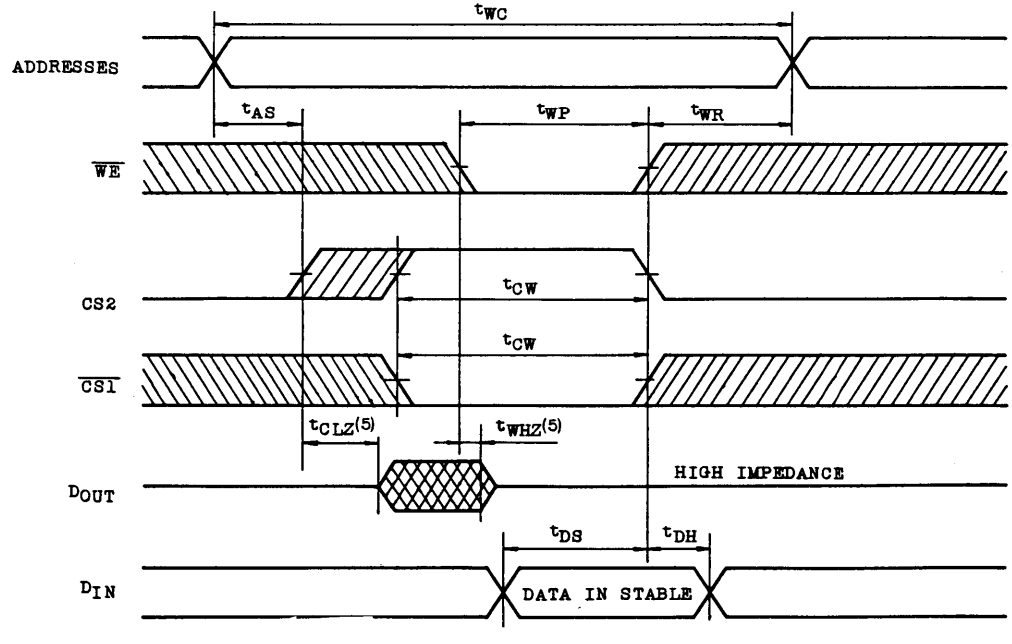
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



- WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS_1}$ Low transition or CS_2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS_1}$ High transition or CS_2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ}·····Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ}·····Output Disable Time

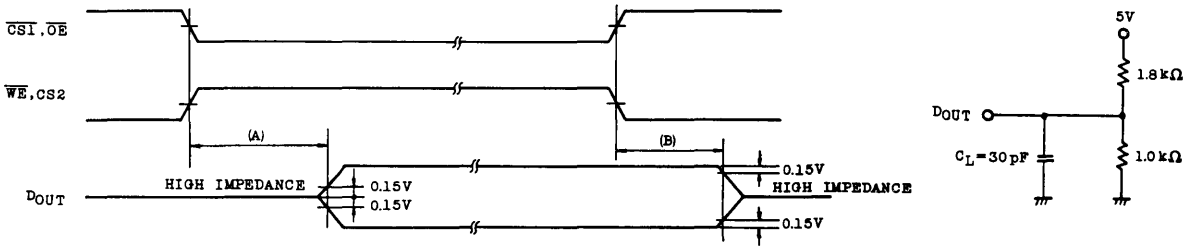
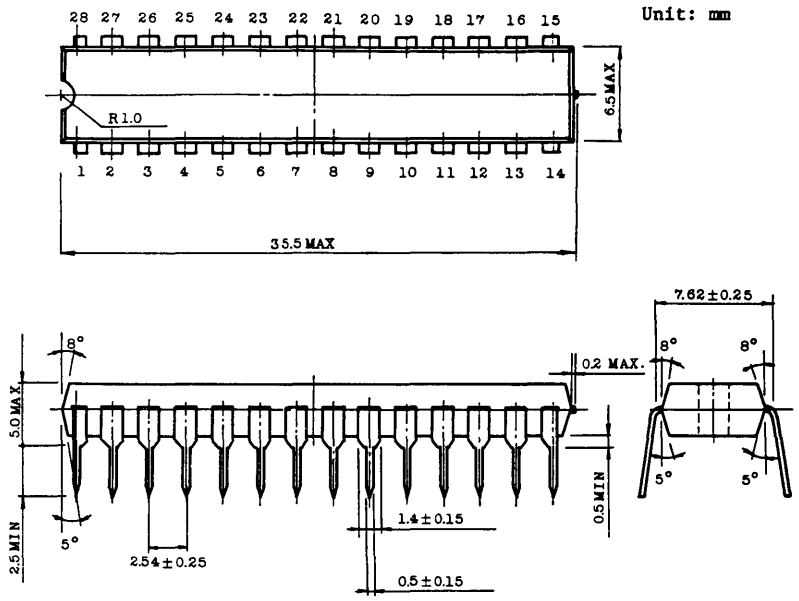


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2064P-10, TMM2064P-12 TMM2064P-15

DESCRIPTION

The TMM2064P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When $\overline{CS_1}$ is a logical high or CS_2 is a logical low, the deivce is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2064P is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2064P is fabricated with ion implanted N channel silicon gate MOS technology for high perfomance and high reliability.

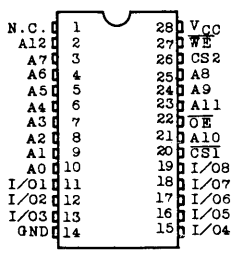
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2064P-10	100ns	80mA	10mA
TMM2064P-12	120ns	80mA	10mA
TMM2064P-15	150ns	80mA	10mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : $\overline{CS_1}$ CS_2
- Output Buffer Control : $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge.

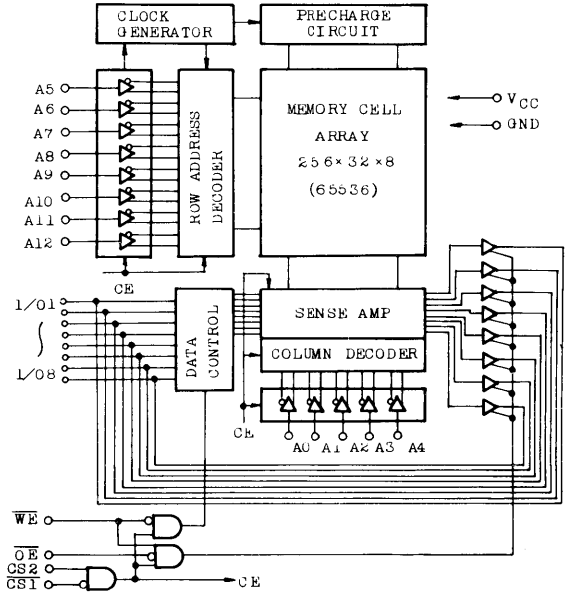
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
A_0~A_4	Column Address Inputs
A_5~A_{12}	Row Address Inputs
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/O_1~I/O_8	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=2.1mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS_1}$=V_{CC}, CS_2=0V I_{OUT}=0mA	—	—	20	mA
I_{SB}	Standby Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, I_{OUT}=0mA	—	—	10	mA
I_{CC}	Operating Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{OUT}=0mA	—	—	80	mA

CAPACITANCE*** (Ta=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2064P-10		TMM2064P-12		TMM2064P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CS_1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CS_2 Access Time	—	100	—	120	—	150	
t_{OE}	$\overline{OE}$ Access Time	—	40	—	50	—	60	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS_1}$ or CS_2 to Output in Low-Z	10	—	10	—	10	—	
t_{CHZ}	$\overline{CS_1}$ or CS_2 to Output in High-Z	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	50	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	60	—	60	

Write Cycle

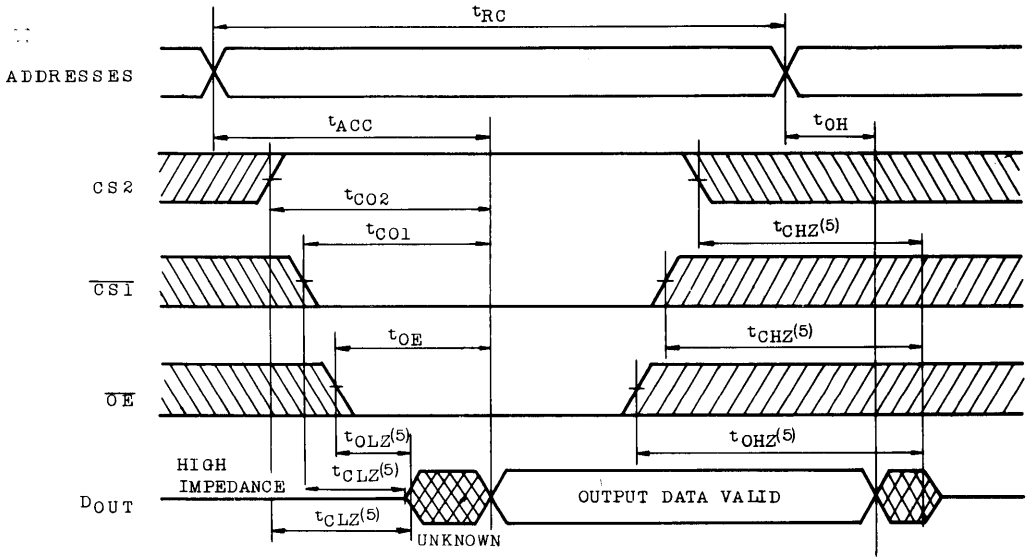
SYMBOL	PARAMETER	TMM2064P-10		TMM2064P-12		TMM2064P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	80	—	100	—	120	—	
t_{AS}	Address Set Up Time	10	—	10	—	10	—	
t_{WP}	Write Pulse Width	70	—	85	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	30	—	35	—	40	

A. C. TEST CONDITIONS

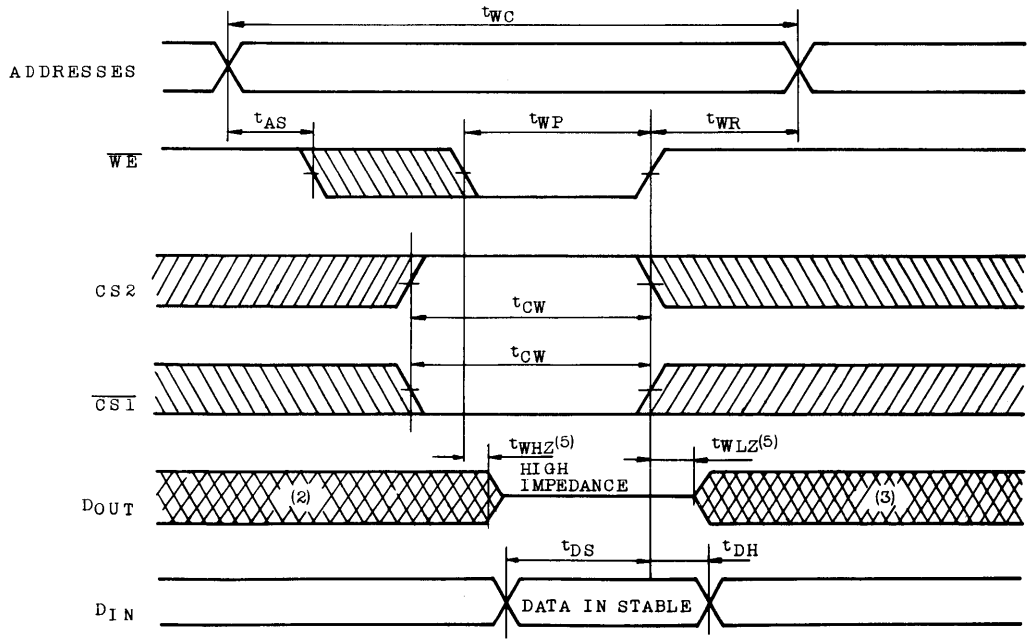
Input Pulse Levels	$V_{IH} = 2.2V$, $V_{IL} = 0.6V$
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100pF$

TIMING WAVEFORMS

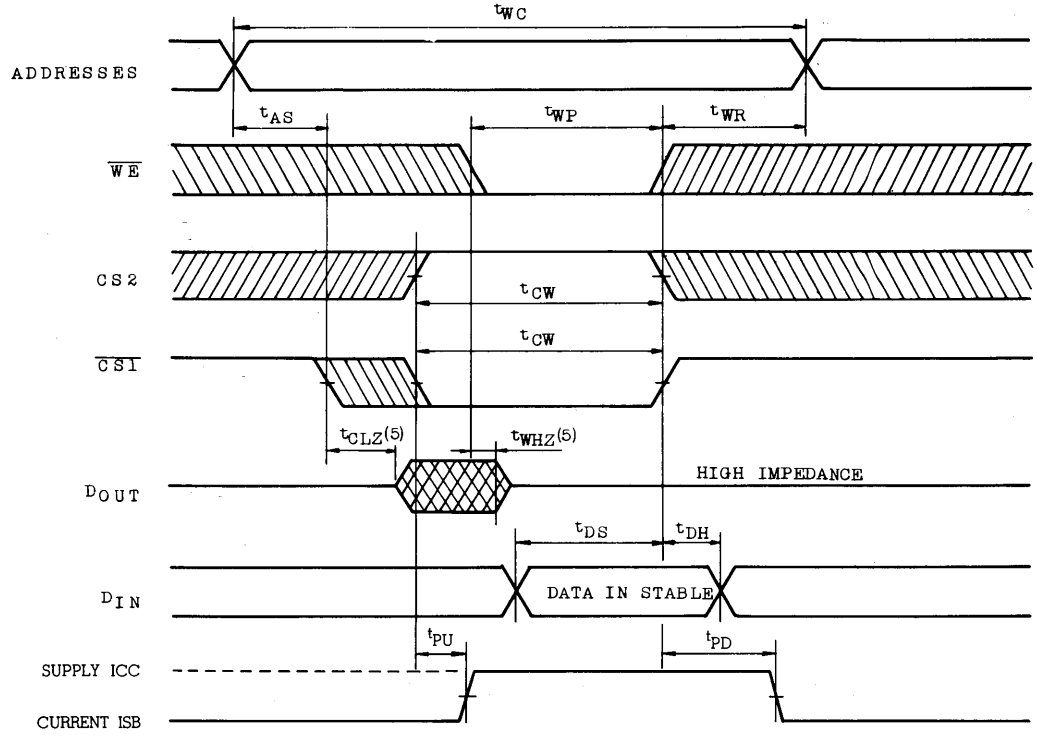
- READ CYCLE (1)



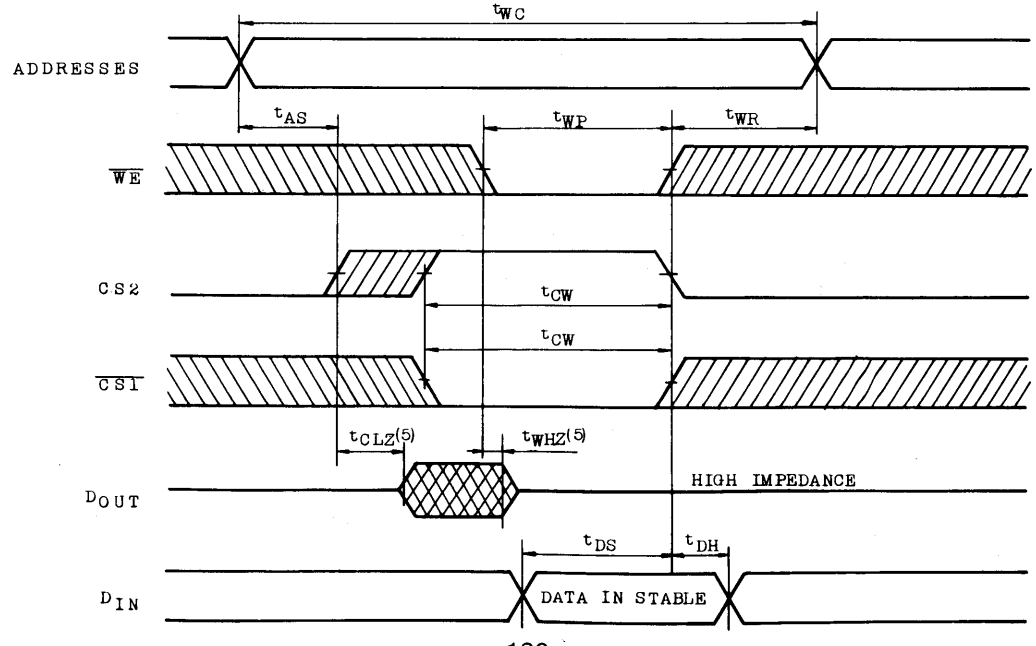
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



● WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS_1}$ Low transition or CS_2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS_1}$ High transition or CS_2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

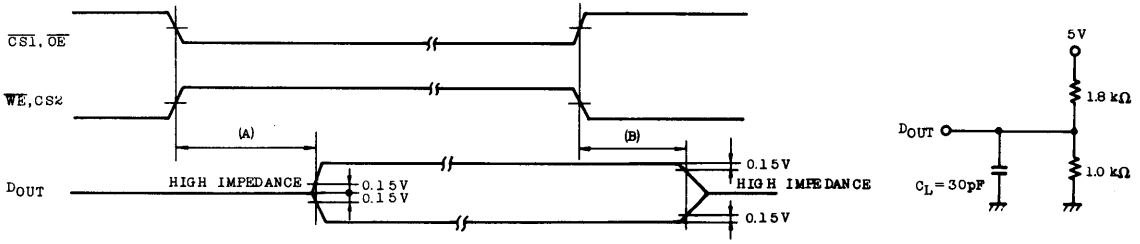
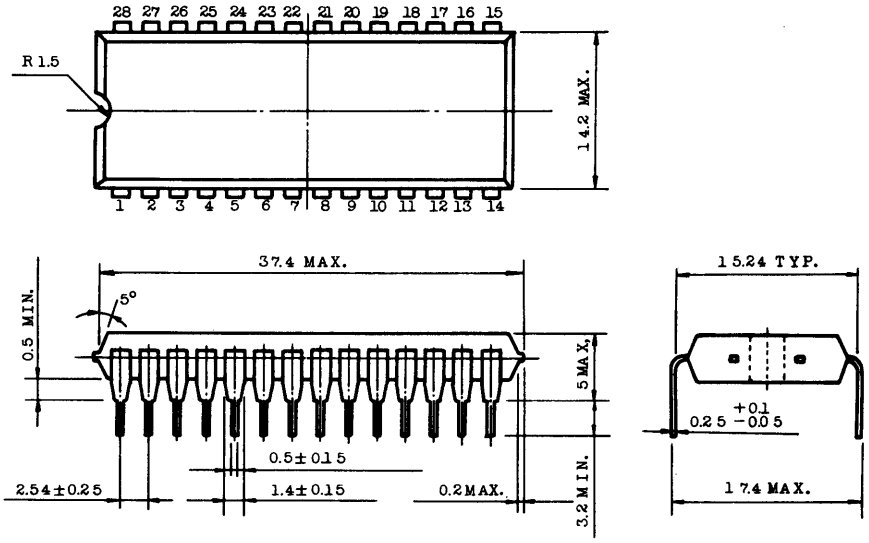


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS
PRELIMINARY

TMM2064P-70

DESCRIPTION

The TMM2064P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 70ns and maximum operating current of 80mA. When $\overline{CS1}$ is a logical high or CS2 is a logical low, the device is placed in a low power stanby mode in which maximum standby current is 10mA. Thus the TMM2064P is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2064P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

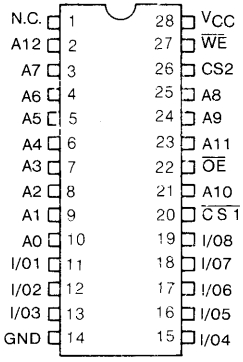
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2064P-70	70ns	100mA	10mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS1}$, CS2
- Output Buffer Control: $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

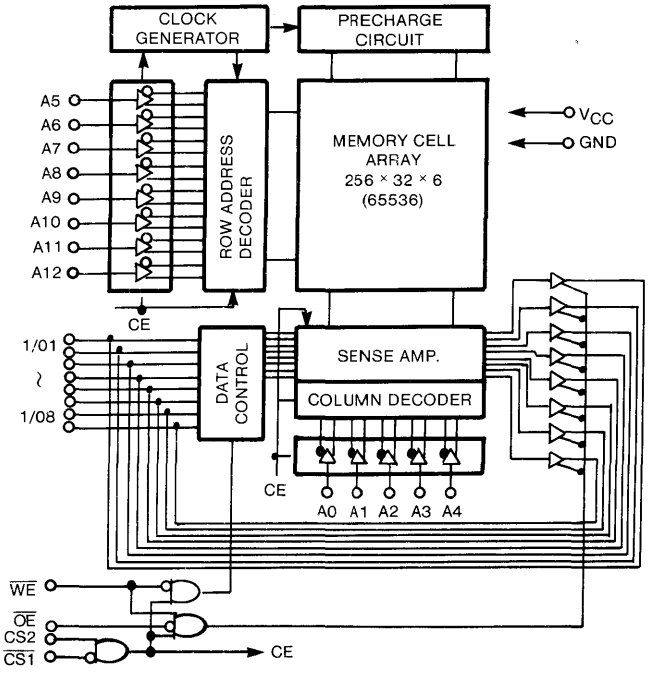
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
A0 ~ A4	Column Address Inputs
A5 ~ A12	Row Address Inputs
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/01 ~ I/08	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	−0.5*~7.0	V
T_{opr}	Operating Temperature	0~70	°C
T_{stg}	Storage Temperature	−55~150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

* −3.0V at Pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.5**	-	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

** −3.0V Pulse width 50ns

D.C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	V_{IN}=0V~5.5V	-10	-	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OUT}=2.1mA	-	-	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IH} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	-10	-	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	-	-	20	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL}, I_{OUT}=0mA	-	-	10	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, I_{OUT}=0mA	-	-	100	mA

CAPACITANCE *** (Ta=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

***Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2064P-70		UNIT
		MIN.	MAX.	
t_{RC}	Read Cycle Time	70	-	ns
t_{ACC}	Address Access Time	-	70	
t_{CO1}	CS1 Access Time	-	70	
t_{CO2}	CS2 Access Time	-	70	
t_{OE}	OE Access Time	-	40	
t_{OH}	Output Data Hold Time from Address Change	5	-	
t_{CLZ}	CS1 or CS2 to Output Low-Z	10	-	
t_{CHZ}	CS1 or CS2 to Output in High-Z	-	35	
t_{OLZ}	OE to Output in Low-Z	5	-	
t_{OHZ}	OE to Output in High-Z	-	30	
t_{PU}	Chip Selection to Power Up Time	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	50	

WRITE CYCLE

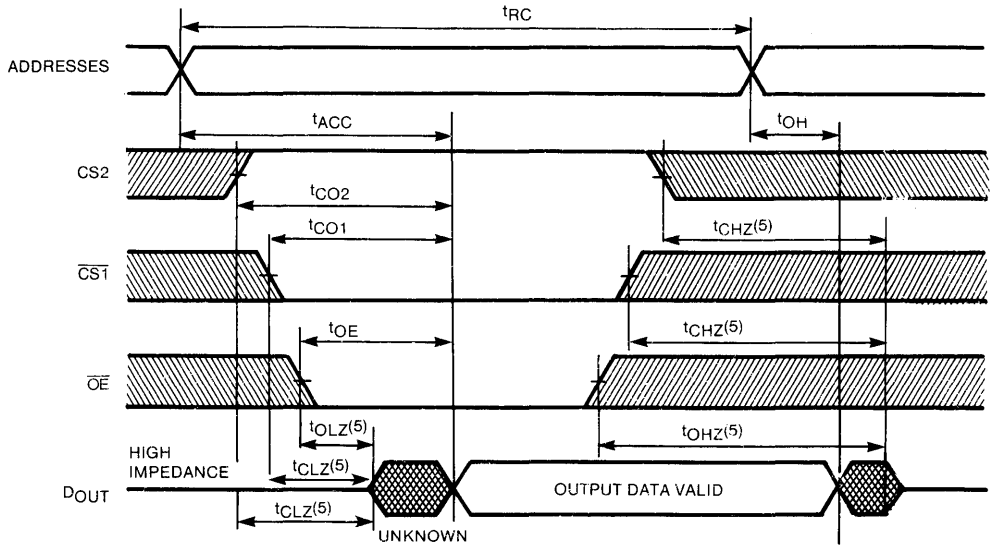
SYMBOL	PARAMETER	TMM2064P-70		UNIT
		MIN.	MAX.	
t_{WC}	Write Cycle Time	70	-	ns
t_{CW}	Chip Selection to End of Write	60	-	
t_{AS}	Address Set Up Time	5	-	
t_{WP}	Write Pulse Width	55	-	
t_{WR}	Write Recovery Time	0	-	
t_{DS}	Data Set Up Time	30	-	
t_{DH}	Data Hold Time	0	-	
t_{WLZ}	WE to Output in Low-Z	5	-	
t_{WHZ}	WE to Output in High-Z	-	30	

A.C. TEST CONDITIONS

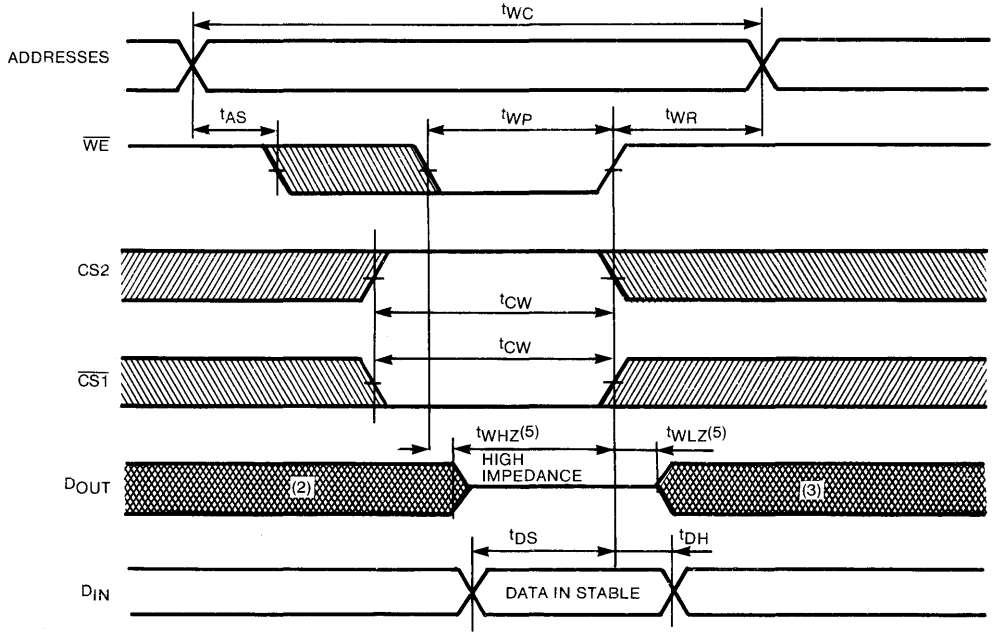
Input Pulse Levels	V_{IH}=2.2V, V_{IL}=0.6V
Input Rise and Fall Time	10 ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & C_L=100pF

TIMING WAVEFORMS

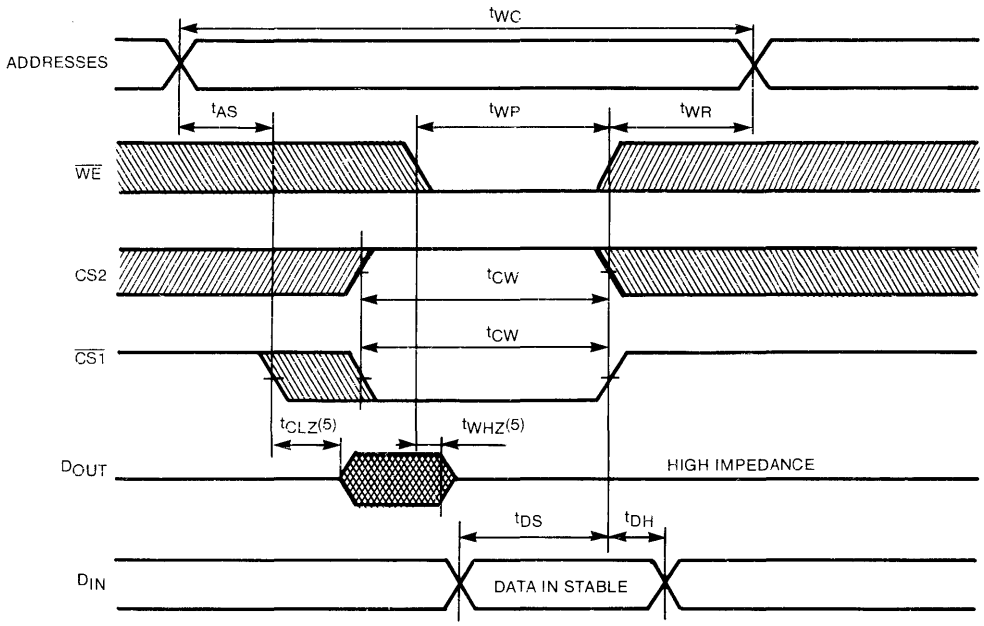
READ CYCLE (1)



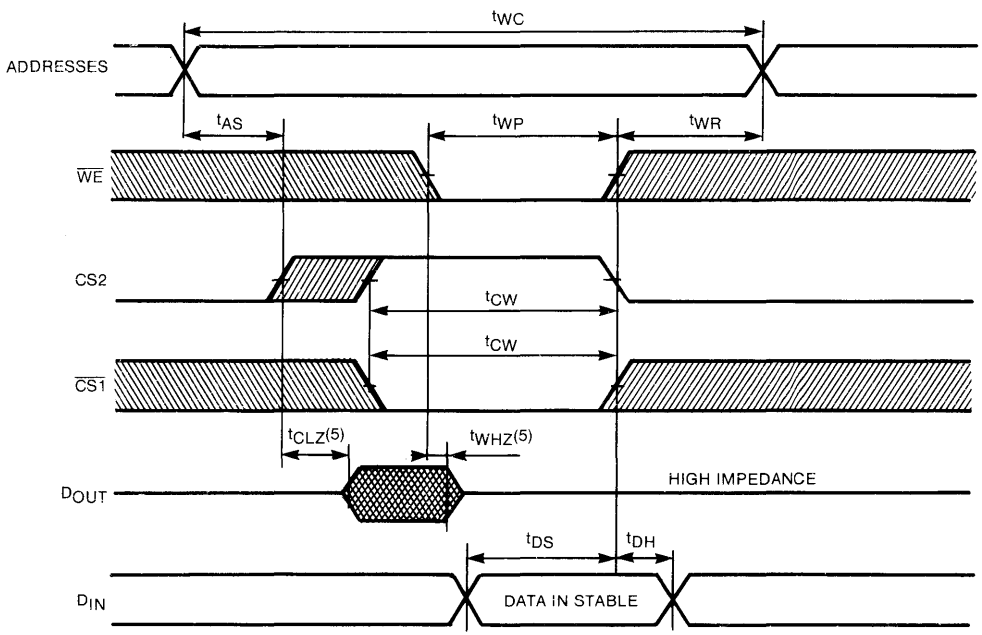
WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note:

1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time

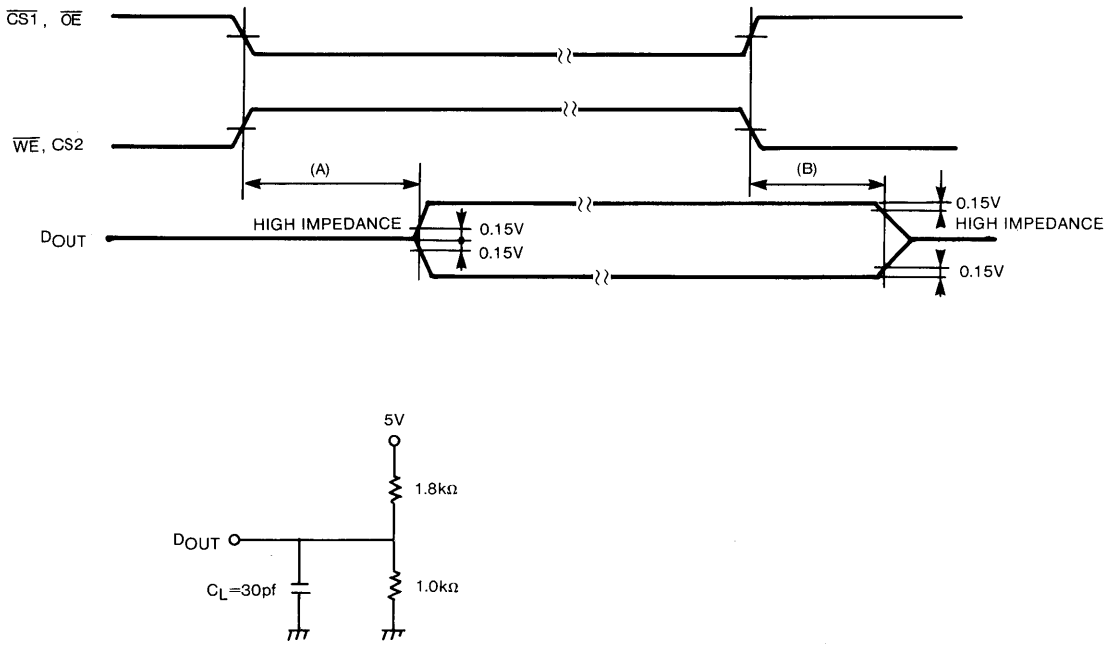
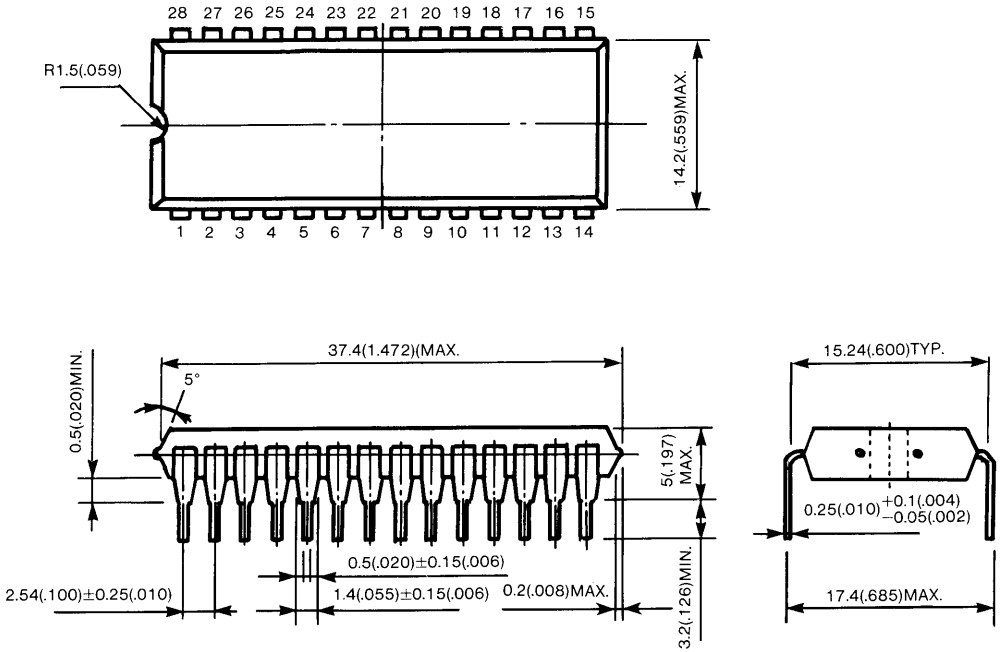


Fig. 1 Output load condition for enable / disable time measurement.

OUTLINE DRAWINGS

Unit: mm (inches)



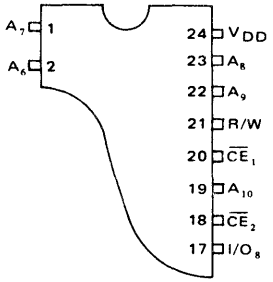
Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.

CMOS Standard Application Static Random Access Memories

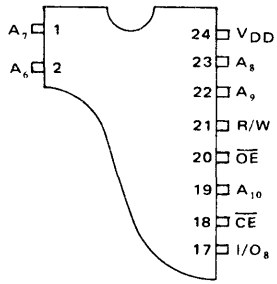
16KBit CMOS STATIC RAM COMPARISON TABLE

PIN CONFIGURATION

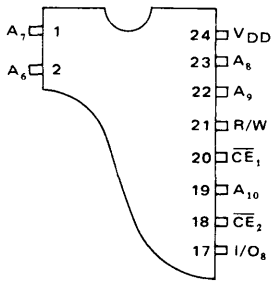
TC5516AP



TC5517AP
TC5517BP



TC5518BP



OPERATION MODE

Device Number	TC5516AP						TC5517AP TC5517BP						TC5518BP					
Pin No. / Mode / Name	18	20	21	1~8, 22 23, 19	9~11 13~17	Power	18	20	21	1~8, 22 23, 19	9~11 13~17	Power	18	20	21	1~8, 22 23, 19	9~11 13~17	Power
	$\overline{CE}_2$	$\overline{CE}_1$	R/W	A_0~A_{10}	$I/O_{1\sim8}$		$\overline{CE}$	$\overline{OE}$	R/W	A_0~A_{10}	$I/O_{1\sim8}$		$\overline{CE}_2$	$\overline{CE}_1$	R/W	A_0~A_{10}	$I/O_{1\sim8}$	
WRITE	L	L	L	Valid	D_{IN}	I_{DDO}	L	*	L	Valid	D_{IN}	I_{DDO}	L	L	L	Valid	D_{IN}	I_{DDO}
READ	L	L	H	Valid	D_{OUT}	I_{DDO}	L	L	H	Valid	D_{OUT}	I_{DDO}	L	L	H	Valid	D_{OUT}	I_{DDO}
STANDBY 1	L	H	*	*	High-Z	I_{DDO}							*	H	*	*	High-Z	I_{DDS}
STANDBY 2	H	*	*	*	High-Z	I_{DDS}	H	*	*	*	High-Z	I_{DDS}	H	*	*	*	High-Z	I_{DDS}
OUTPUT DESELECT							L	H	*	*	High-Z	I_{DDO}						

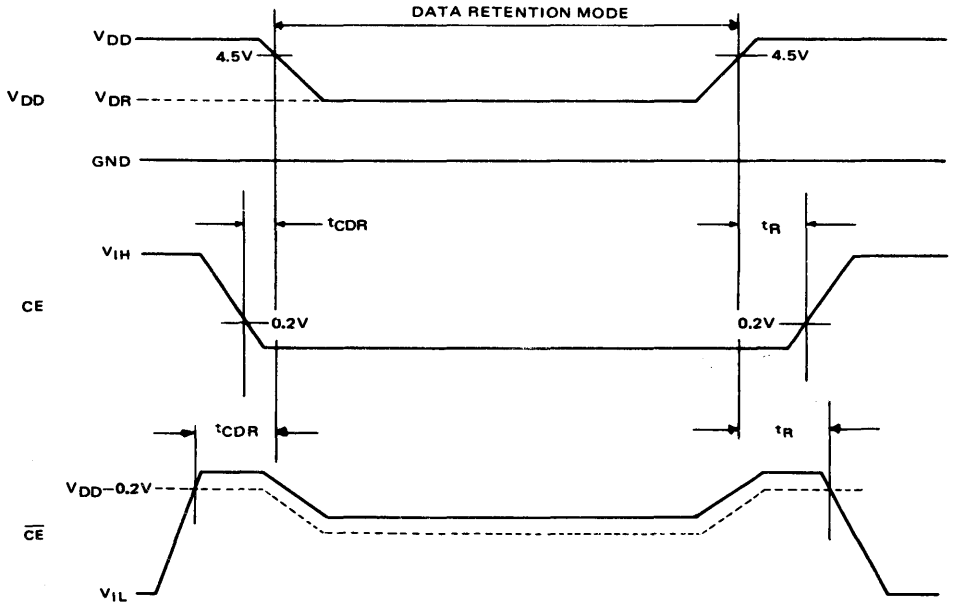
* H or L

DATA RETENTION CHARACTERISTICS (Ta = -30 ~ 85°)

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	UNIT
V_{DR}	Data Retention Voltage	$0V \leqq CE \leqq 0.2V$ or $V_{DD}-0.2V \leqq \overline{CE} \leqq V_{DD}$ *(3)	2.0	5.5	V
I_{DDS}	Data Retention Current		–	Note (1)	μA
t_{CDR}	Chip Deselection to Data Retention Time		0	–	μS
t_R	Recovery Time		t_{RC} Note(2)	–	μS

Note (1) : Refer to I_{DDS} specification in individual data sheet.
(2) : Read cycle time.

TIMING CHART



Note (3) : For 16K Bit CMOS RAM, $V_{DD}-0.5V \leqq \overline{CE} \leqq V_{DD}$
Details are specified in TC5516/17/18 data sheets.

TC5514AP-2/-3
TC5514APL-2/-3

1,024 WORD × 4 BIT CMOS STATIC RAM
SILICON GATE CMOS

DESCRIPTION

The TC5514AP is a 4,096 bit high speed and low power random access memory organized as 1,024 words by 4 bits using CMOS technology, and operates from a single 5-volt supply.

The 5514AP is compatible with the industry produced NMOS 2114 type 4KRAM, yet offers a more than 90% reduction in power of their NMOS equivalents.

The TC5514AP is a fully CMOS RAM, therefore it is suited for use in low power applications where battery operation and battery back up for nonvolatility are required. Furthermore the TC5514APL guaranteed a standby current equal to or less than 1μA at 60℃ ambient temperature is avaliable.

The TC5514AP is guaranteed for data retention at a power supply as low as 2 volts. The TC5514AP is directly TTL compatible in all inputs and outputs.

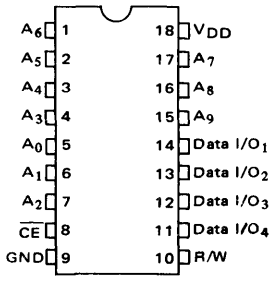
The TC5514AP is offered in standerd 18 pin plastic, 0.3inch in width.

FEATURES

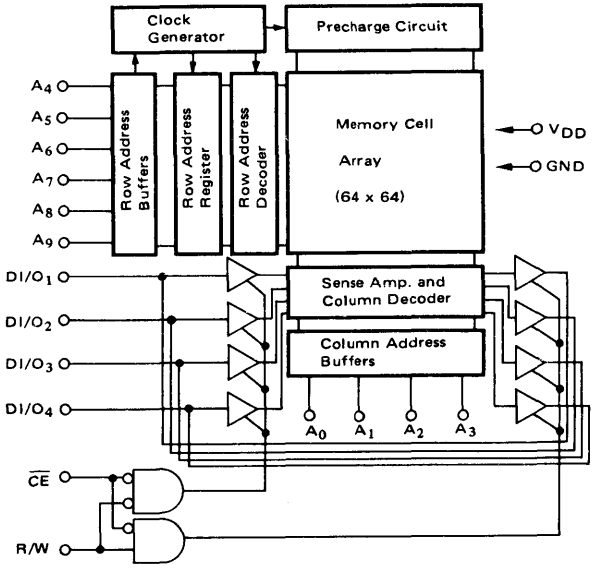
- Standby Current
  0.2μA (Max.) at Ta=25°C } : TC5514APL
  1.0μA (Max.) at Ta=60°C }
  20μA (Max.) : TC5514AP
- Low Power Dissipation : 15mW (Typ.) operating
- Single 5-volt Supply : 5V ± 10%
- Data Retention Supply Voltage : 2 ~ 5.5V
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Access Time
  200ns (Max.) : TC5514AP/APL-2
  300ns (Max.) : TC5514AP/APL-3
- Fully Static Operation
- On-chip Address Transition Detector
- Fully Compatible with TMM2114AP Family (Nch 2114 type 4KRAM)
- Package
  Plastic DIP : TC5514AP/APL

PIN CONNECTION

(TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_9$	Address Inputs
R/W	Read Write Control Input
$\overline{CE}$	Chip Enable Input
Data $I/O_1 \sim_4$	Data Input/Output
V_{DD}/GND	Power Supply Terminals

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3 ~ 7.0	V
$V_{I/O}$	I/O Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation(Ta = 85°C)	550	mW
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−30 ~ 85	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Level Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Level Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = −30 ~ 85°C unless otherwise noted.)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP. (1)	MAX.	UNIT
I_{IL}	Input Leakage Current	$0V \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			–	–	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	–	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	–	–	mA
I_{DDS}	Standby Current	V_{DD} = 2V ~ 5.5V All Inputs = 0.2V or V_{DD} − 0.2V	TC5514APL	Ta = 25°C	–	–	0.2	μA
				Ta = 60°C	–	–	1.0	μA
			TC5514AP		–	0.05	20	μA
I_{DDO1}	Operating Current	t_{cycle} = 1μs, I_{OUT} = 0mA			–	5.0	9.0	mA
I_{DDO2}		t_{cycle} = 1μs, $V_{IH} = V_{DD}$, V_{IL} = 0V, I_{OUT} = 0mA			–	3.0	5.0	

Note (1): V_{DD} = 5V, Ta = 25°C

CAPACITANCE(2)

(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	–	5	10	pF

Note (2): This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = −30 ~ 85°C)

- **READ CYCLE**

SYMBOL	PARAMETER	TC5514AP-2/APL-2		TC5514AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	300	–	ns
t_{ACC}	Access Time	–	200	–	300	ns
t_{CO}	$\overline{CE}$ Access Time	–	70	–	100	ns
t_{OH}	Output Data Hold Time	15	–	20	–	ns
t_{DIS}	Output Disable Time	–	60	–	80	ns
t_{COE}	Output Enable Time	5	–	5	–	ns

- **WRITE CYCLE**

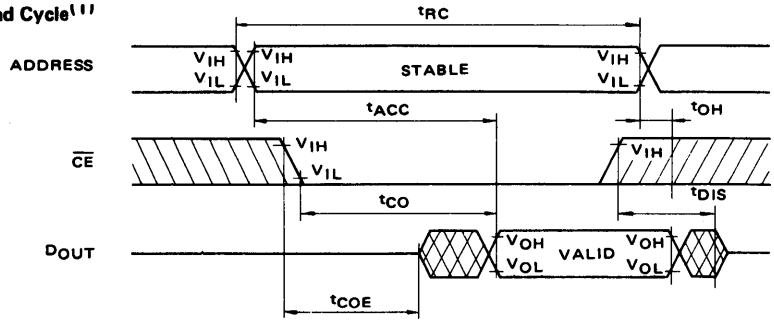
SYMBOL	PARAMETER	TC5514AP-2/APL-2		TC5514AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	300	–	ns
t_{AW}	Address Setup Time	0	–	0	–	ns
t_{WP}	Write Pulse Width	120	–	150	–	ns
t_{DS}	Data Setup Time	120	–	150	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns

A.C. TEST CONDITIONS

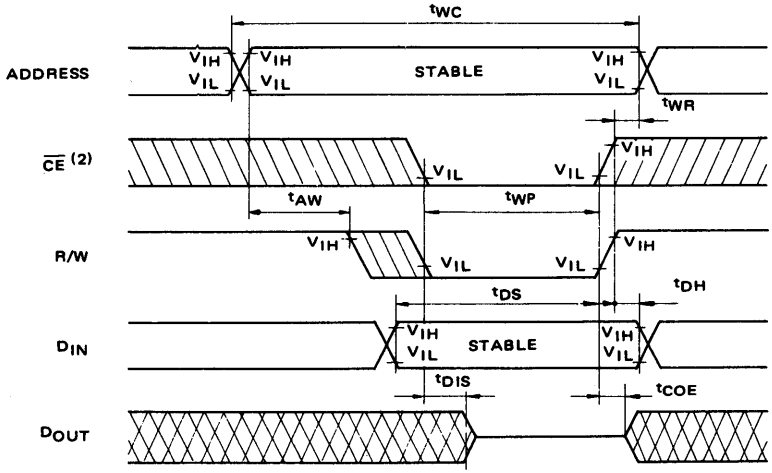
- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V, 2.2V
  - Output : 0.8V, 2.2V
- Input Pulse Rise and Fall Times : 10 ns

TIMING WAVEFORMS

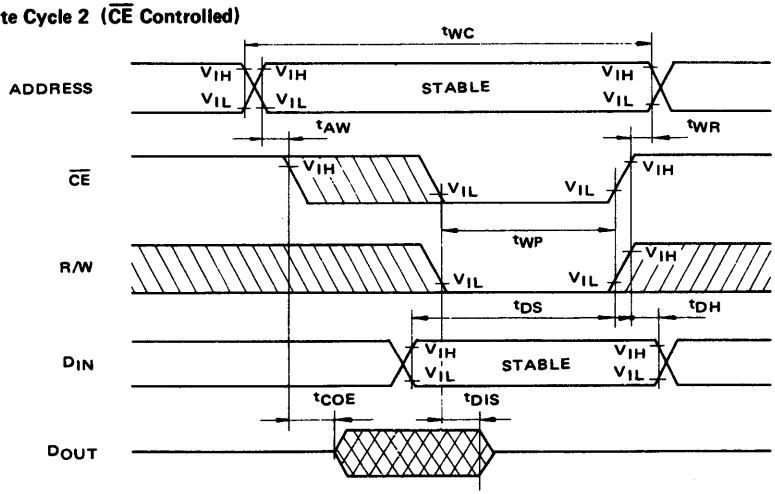
- **Read Cycle[1]**



- **Write Cycle 1 (R/W Controlled)**

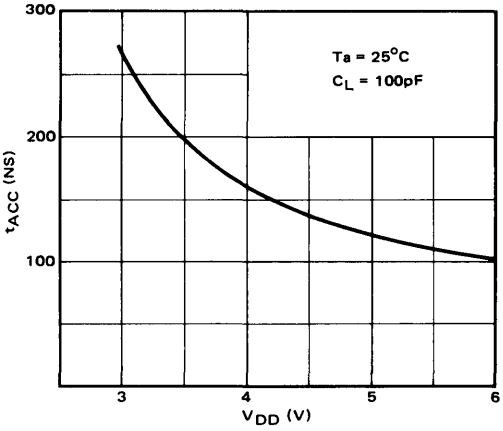


- **Write Cycle 2 ($\overline{CE}$ Controlled)**

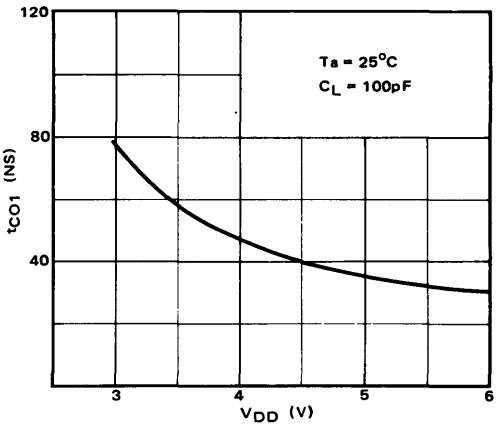


Notes: (1) R/W is high for a Read Cycle.
(2) If the $\overline{CE}$ low transition occurs simultaneously with the R/W low transition, the output buffers remain in a high impedance state.

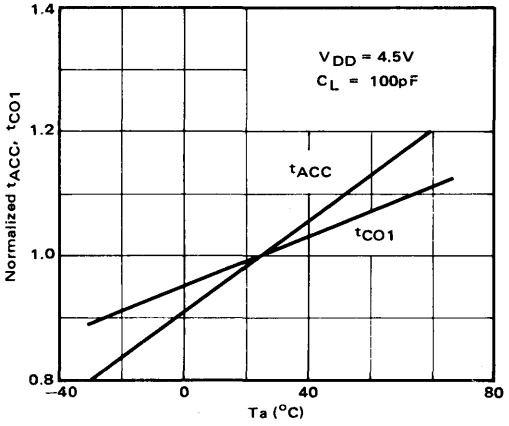
t_{ACC} VS. V_{DD}



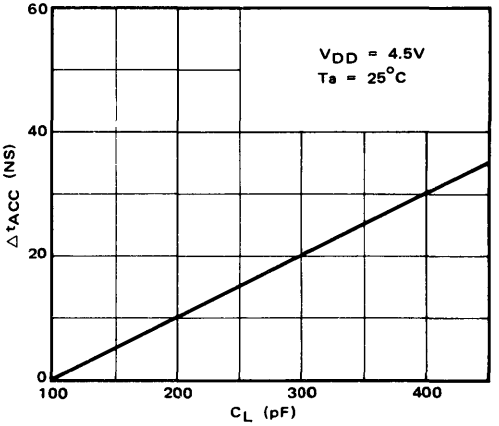
t_{CO1} VS. V_{DD}



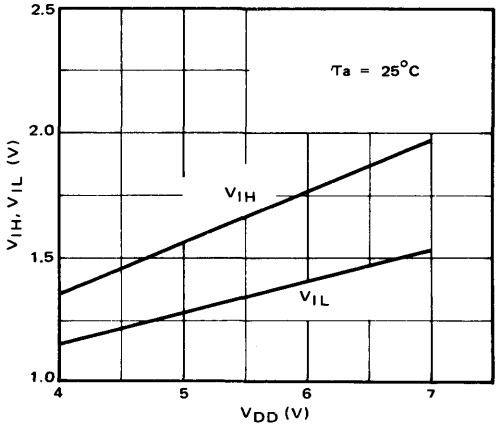
t_{ACC}, t_{CO1} VS. Ta



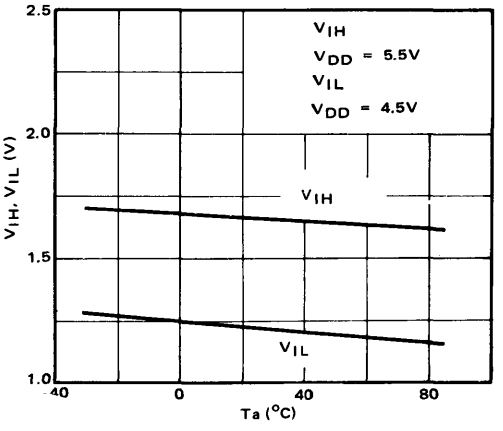
Δt_{ACC} VS. C_L



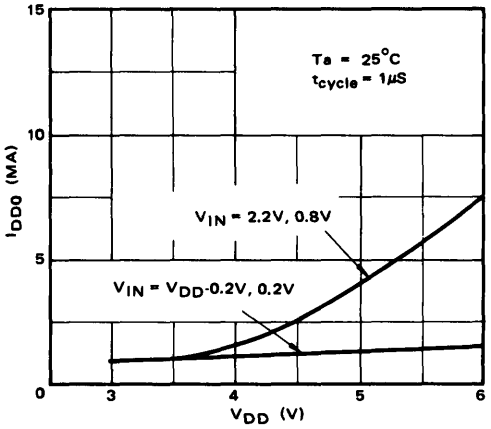
V_{IH}, V_{IL} VS. V_{DD}



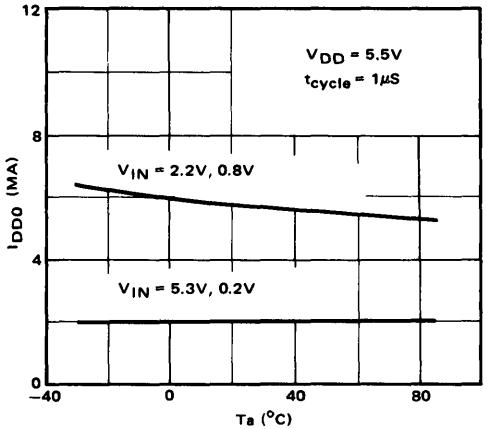
V_{IH}, V_{IL} VS. Ta



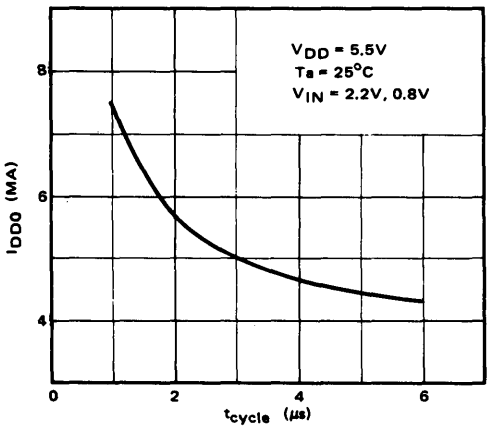
I_{DDO} VS. V_{DD}



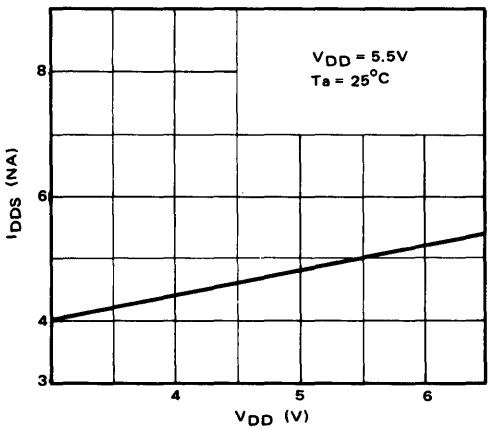
I_{DDO} VS. Ta



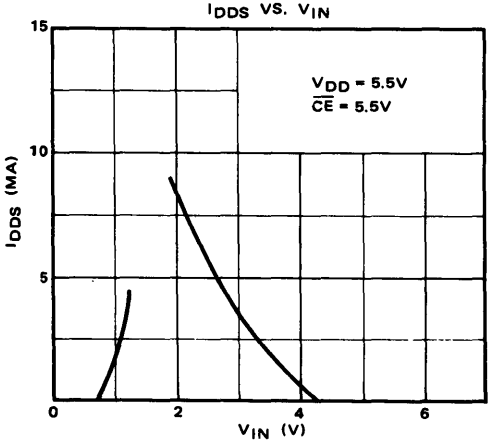
I_{DDO} VS. t_{cycle}



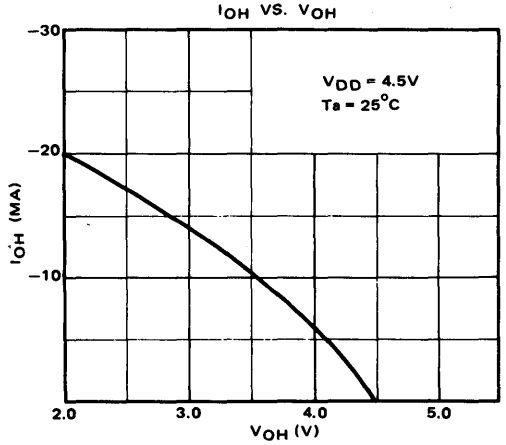
I_{DDS} VS. V_{DD}

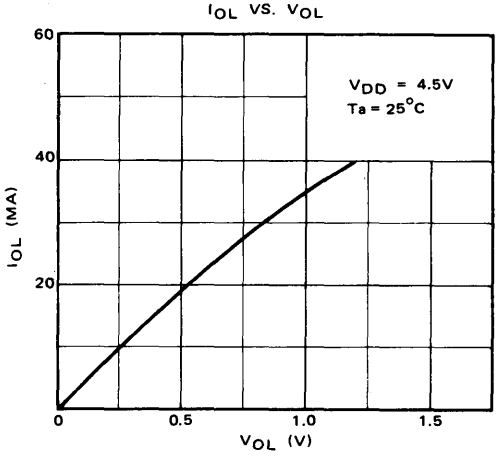


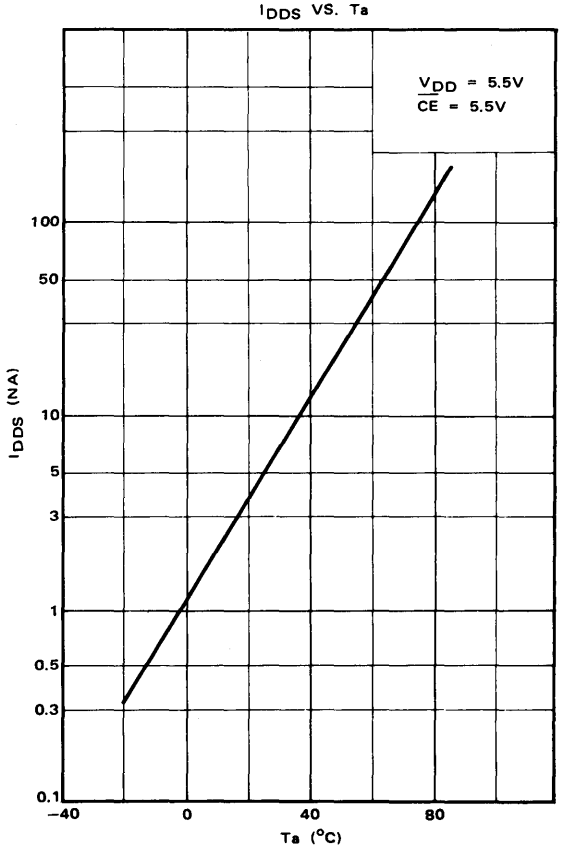
I_{DDS} VS. V_{IN}



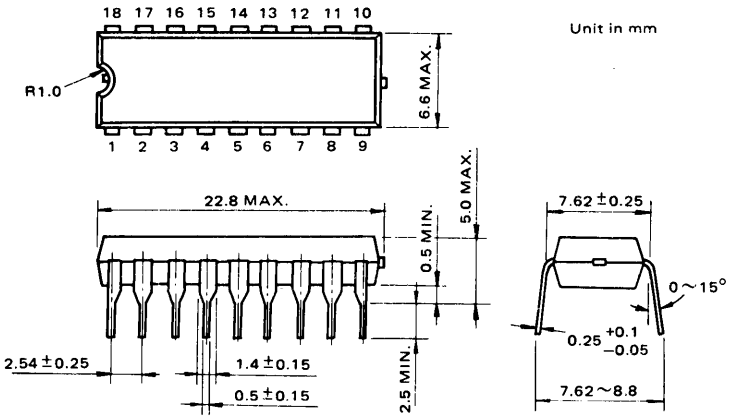
I_{OH} VS. V_{OH}




I_{OL} VS. V_{OL}
V_{DD} = 4.5V
Ta = 25°C
I_{OL} (MA)
60
40
20
0
0.5
1.0
1.5
V_{OL} (V)


I_{DDS} VS. Ta
V_{DD} = 5.5V
$\overline{CE}$ = 5.5V
I_{DDS} (NA)
100
50
10
5
3
1
0.5
0.3
0.1
−40
0
40
80
Ta (°C)

- **PLASTIC PACKAGE**



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.
All dimensions are in millimeters.

2,048 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5516AP/-2, TC5516APL/-2
TC5516AF/-2, TC5516AFL/-2

DESCRIPTION

The TC5516AP/AF is a 16384-bit static random access memory organized as 2048 words by 8 bit using CMOS technology, ad operates from a single 5 volt supply.

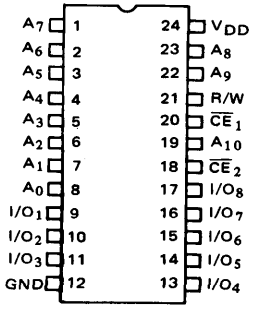
The TC5516AP/AF is featured by two chip enable inputs, that is, $\overline{CE}_1$ for fast memory access and $\overline{CE}_2$ for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for nonvolatility are required. Furthermore the TC5516APL/AFL guaranteed a standby current equal to or less than 1μA at 60℃ ambient temperature is avialable.

The TC5516AP is also featured by pin compatibility with 2716 type EPROM. This means that the TC5516AP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

FEATURES

- Standby Current
  - 0.2μA (Max.) at Ta = 25°C
  - 1.0μA (Max.) at Ta = 60°C } TC5516APL/AFL
  - 1.0μA (Max.) at Ta = 25°C
  - 5.0μA (Max.) at Ta = 60°C } TC5516AP/AF
- Low Power Dissipation : 200mW (Typ.) Operating
- Single 5V Power Supply : 5V ± 10%
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation
- Access Time
  - 250ns (Max.): TC5516AP/APL/AF/AFL
  - 200ns (Max.): TC5516AP-2/APL-2/AF-2/AFL-2
- Two Chip Enable ($\overline{CE}_1$, $\overline{CE}_2$) for Simple Memory Expansion and Battery Back Up.
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
  - Plastic DIP : TC5516AP/APL
  - Plastic FP : TC5516AF/AFL

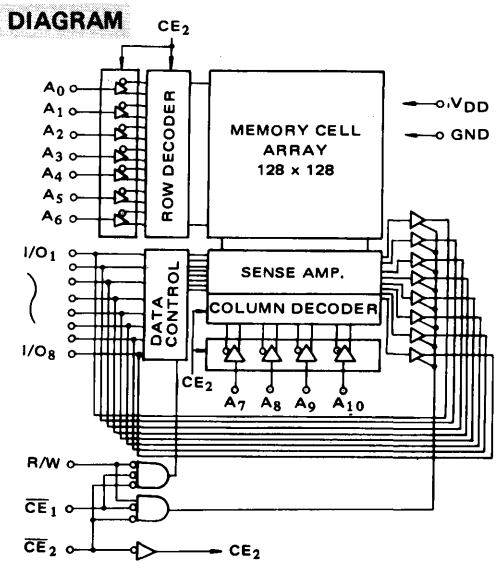
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ V_{DD} + 0.3
$V_{I/O}$	Input/Output Voltage	−0.3V ~ V_{DD} + 0.3
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W)*
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−30°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}_2 = V_{IH}$, $OV \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}_2$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE}_2 = V_{DD}$ −0.5V V_{DD} = 2 ~ 5.5V	TC5516APL/AFL	Ta = 25°C	–	0.005	0.2	μA
				Ta = 60°C	–	–	1.0	
			TC5516AP/AF	Ta = 25°C	–	0.05	1.0	
				Ta = 60°C	–	–	5.0	
				Ta = 85°C	–	–	30	
I_{DDO1}	Operating Current	$\overline{CE}_2$ = OV, $V_{IN} = V_{IH}/V_{IL}$, I_{OUT} = 0mA			–	40	70	mA
I_{DDO2}		$\overline{CE}_2$ = OV, $V_{IN} = V_{DD}/GND$, I_{OUT} = 0mA			–	30	55	

Note: Typical values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ±10%)

● **Read Cycle**

SYMBOL	PARAMETER	TC5516AP-2/APL-2 TC5516AF-2/AFL-2		TC5516AP/APL TC5516AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	250	–	ns
t_{ACC}	Access Time	–	200	–	250	ns
t_{CO1}	$\overline{CE}_1$ to Output Valid	–	100	–	100	ns
t_{CO2}	$\overline{CE}_2$ to Output Valid	–	200	–	250	ns
t_{COE}	$\overline{CE}_1$ or $\overline{CE}_2$ to Output Active	10	–	10	–	ns
t_{OD}	Output High-Z form Deselection	–	80	–	80	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	ns

● **Write Cycle**

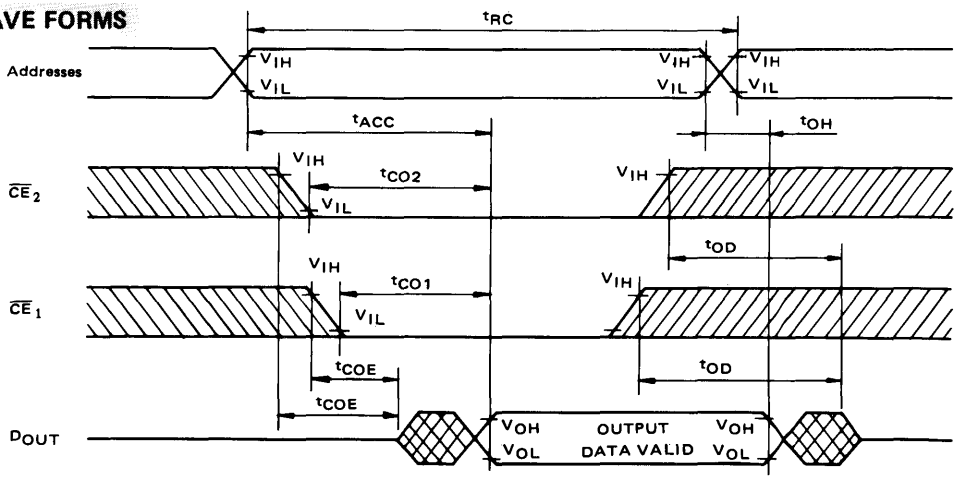
SYMBOL	PARAMETER	TC5516AP-2/APL-2 TC5516AF-2/AFL-2		TC5516AP/APL TC5516AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	250	–	ns
t_{WP}	Write Pulse Width	160	–	200	–	ns
t_{AW}	Addresss Set Up Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	ns
t_{ODW}	Output High-Z from R/W	–	80	–	80	ns
t_{OEW}	Output Active from R/W	10	–	10	–	ns
t_{DS}	Data Set Up Time	80	–	120	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns

A.C. TEST CONDITIONS

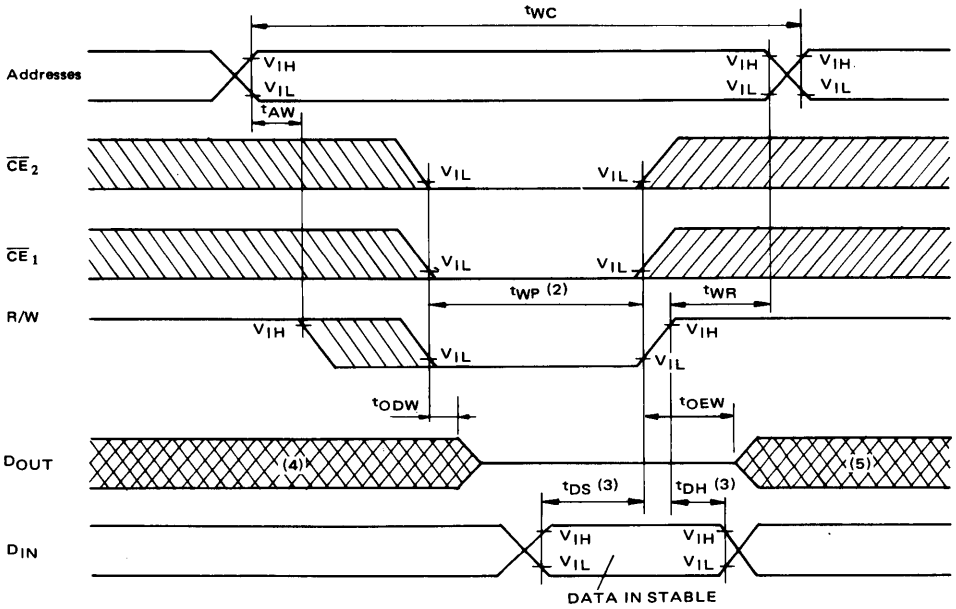
Output Load : 100 pF + ITTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10ns

TIMING WAVE FORMS

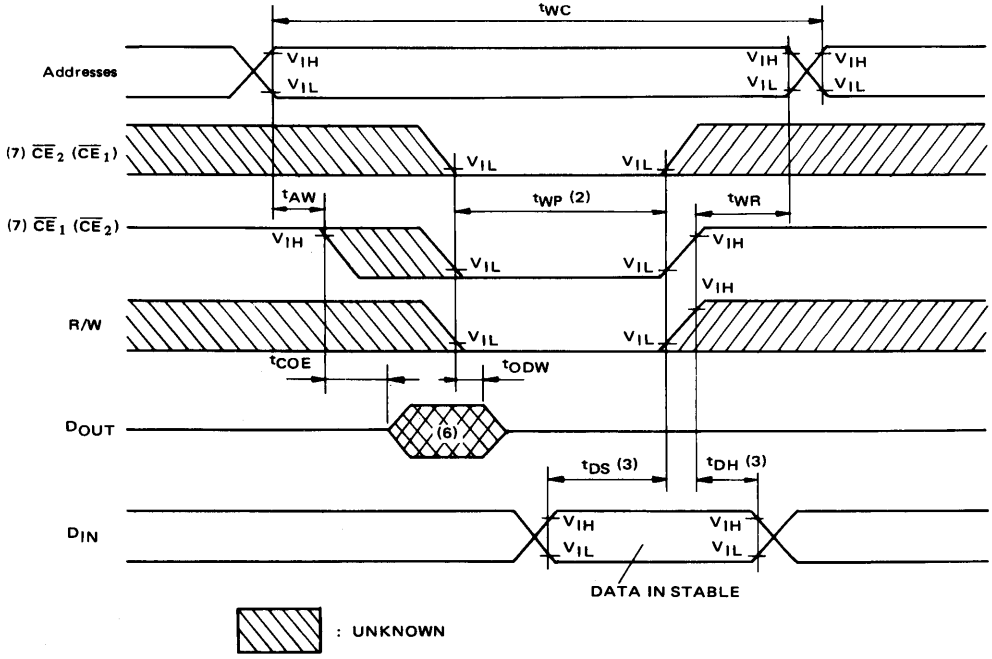
● **Read Cycle**



- **Write Cycle 1**



- **Write Cycle 2**

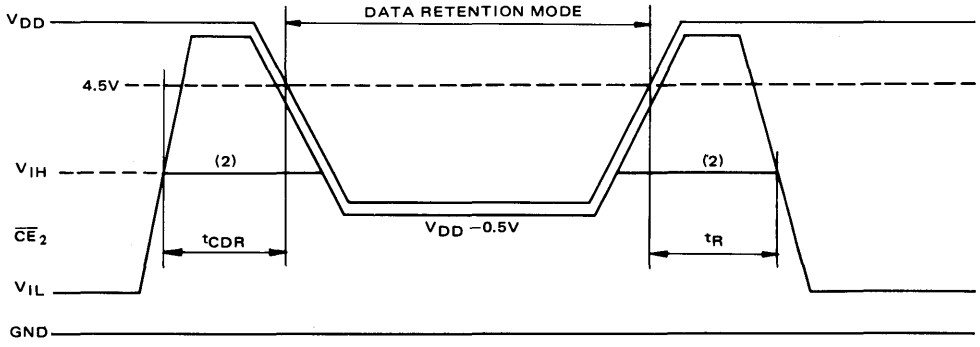


NOTE: (1) R/W is high for a Read Cycle.
(2) t_{WP} is specified as the logical "AND" of $\overline{CE}_1$, $\overline{CE}_2$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going low to the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going high.
(3) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}_1$, $\overline{CE}_2$ or R/W going high.
(4) If the $\overline{CE}_1$, or $\overline{CE}_2$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(5) If the $\overline{CE}_1$ or $\overline{CE}_2$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}_1$ or $\overline{CE}_2$ low transition, the output buffers remain in a high impedance state in this period.
(7) A write occurs during the overlap of a low $\overline{CE}_1$, low $\overline{CE}_2$ and low R/W. In write cycle 2, write is controlled by either $\overline{CE}_1$ or $\overline{CE}_2$.

DATA RETENTION CHARACTERISTICS (Ta = −30 ~ 85°C)

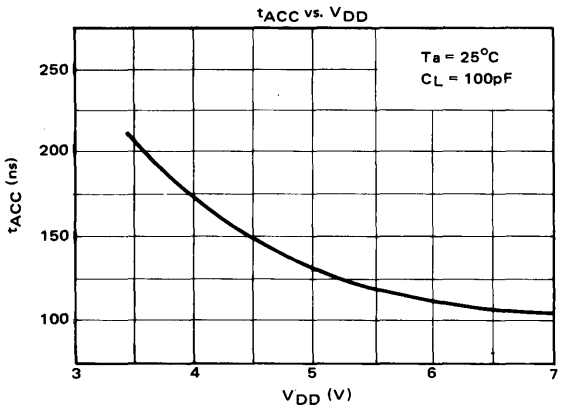
SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5516APL/AFL	Ta = 25°C	–	0.005	0.2	μA
			Ta = 60°C	–	–	1.0	
		TC5516AP/AF	Ta = 25°C	–	0.05	1.0	
			Ta = 60°C	–	–	5.0	
			Ta = 85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recover Time			t_{RC} (1)	–	–	μs

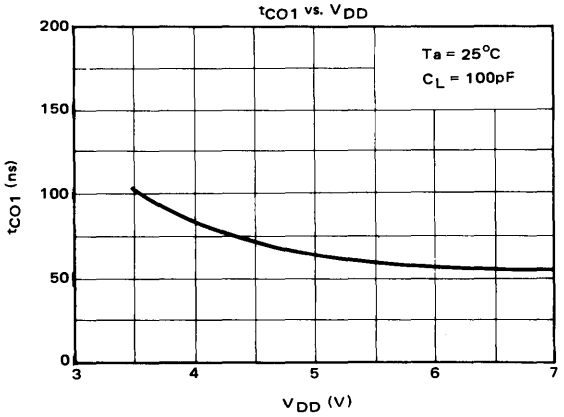
Note (1) t_{RC} : Read Cycle Time.

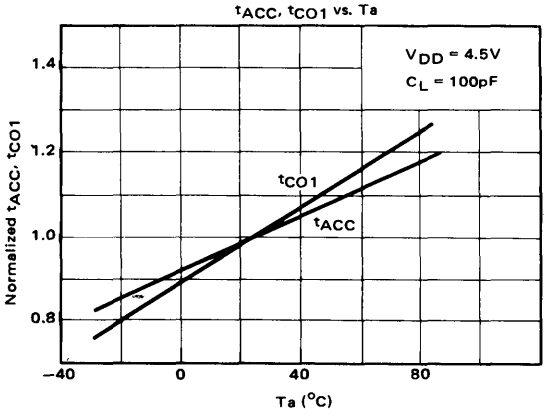


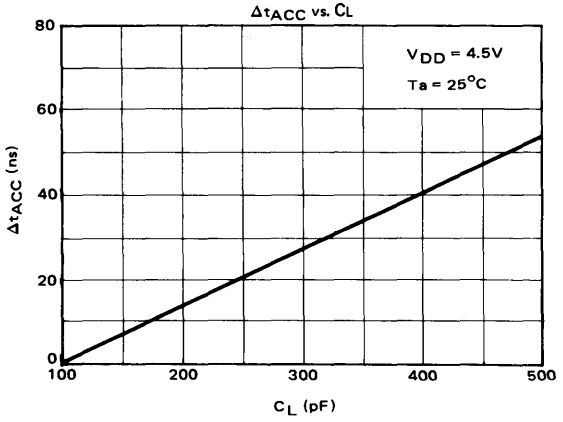
Note: (2) If the V_{IH} level of $\overline{CE}_2$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{SSD1} current flows. (Refer to D.C. CHARACTERISTICS or TYPICAL CHARACTERISTIC FIGURES.)

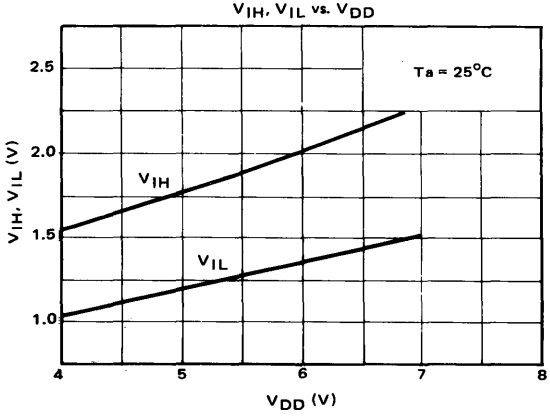
TYPICAL CHARACTERISTICS

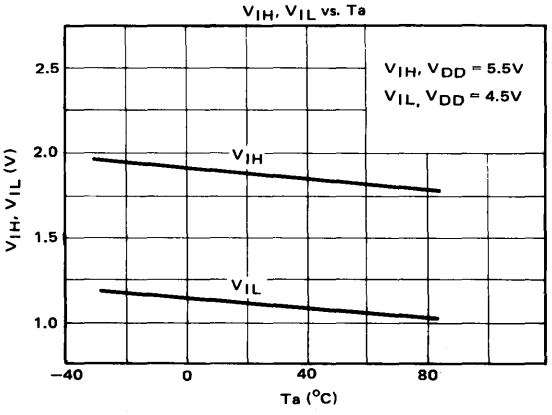


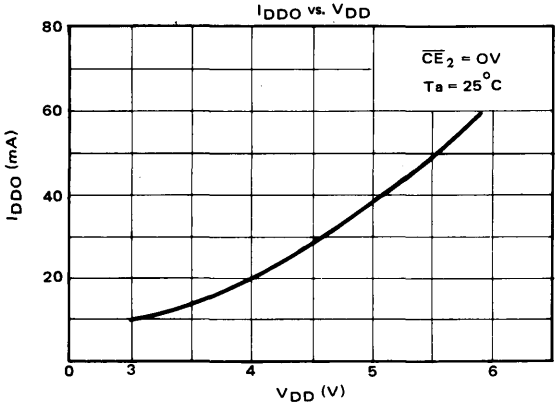


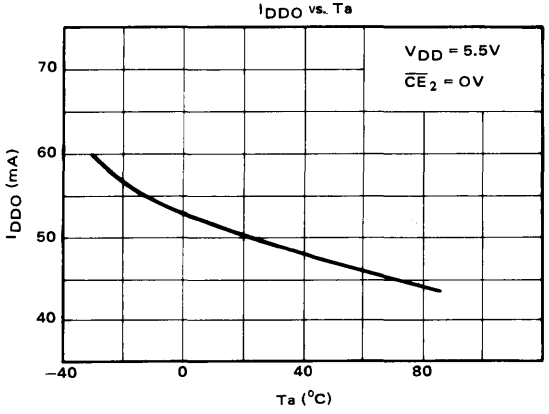


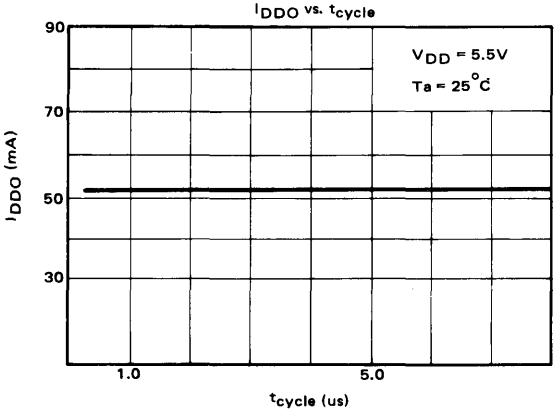


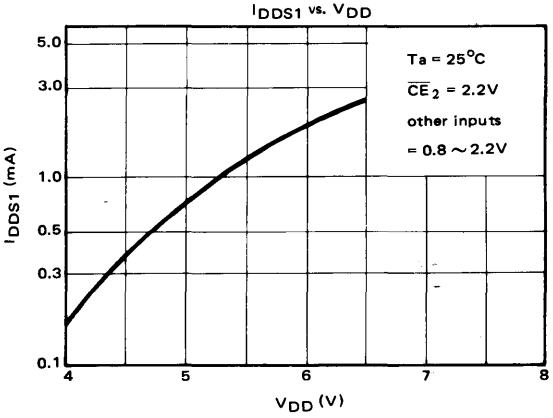


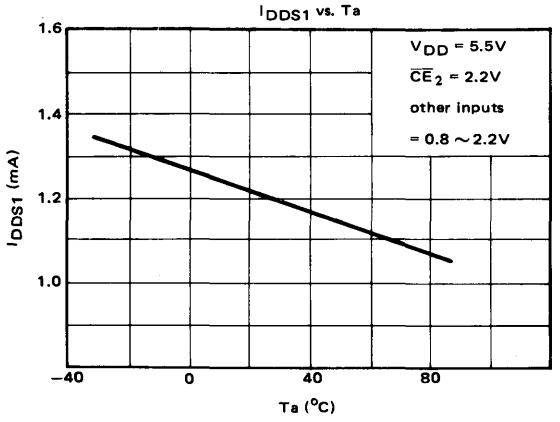


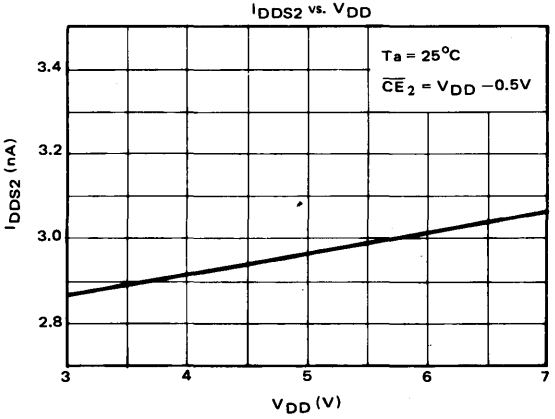

I_{DDO} vs. V_{DD}
$\overline{CE}_2$ = OV
Ta = 25°C
I_{DDO} (mA)
80
60
40
20
0
3
4
5
6
V_{DD} (V)

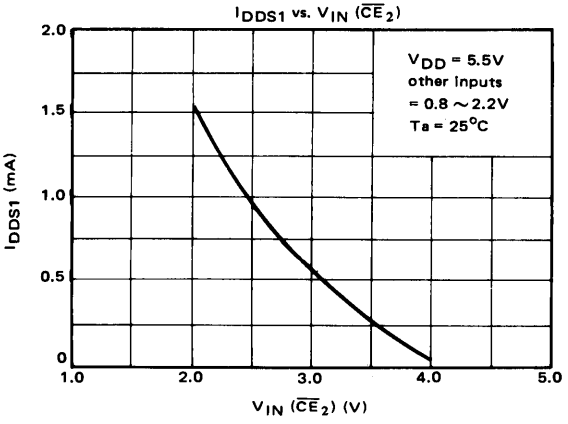

I_{DDO} vs. Ta
V_{DD} = 5.5V
$\overline{CE}_2$ = OV
I_{DDO} (mA)
70
60
50
40
−40
0
40
80
Ta (°C)

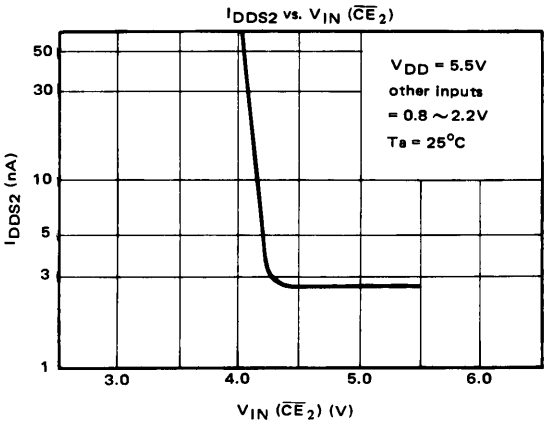

I_{DDO} vs. t_{cycle}
V_{DD} = 5.5V
Ta = 25°C
I_{DDO} (mA)
90
70
50
30
1.0
5.0
t_{cycle} (us)

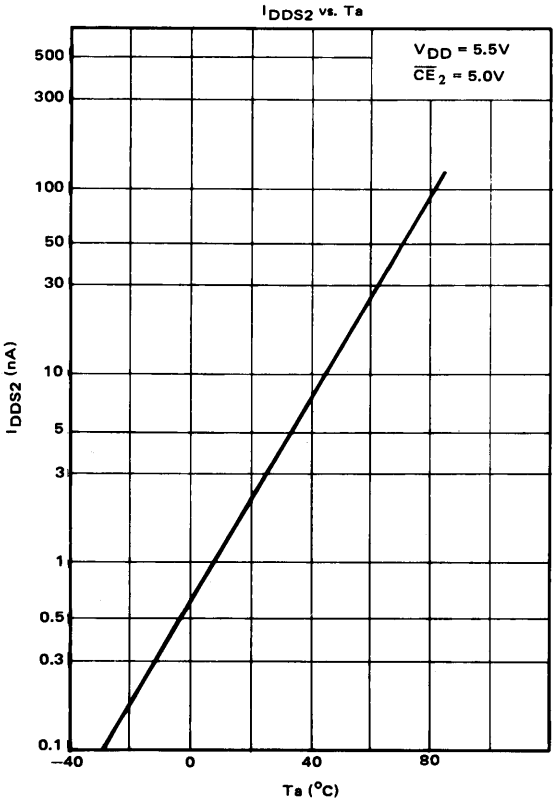

I_{DDS1} vs. V_{DD}
Ta = 25°C
$\overline{CE}_2$ = 2.2V
other inputs
= 0.8 ~ 2.2V
I_{DDS1} (mA)
5.0
3.0
1.0
0.5
0.3
0.1
4
5
6
7
8
V_{DD} (V)

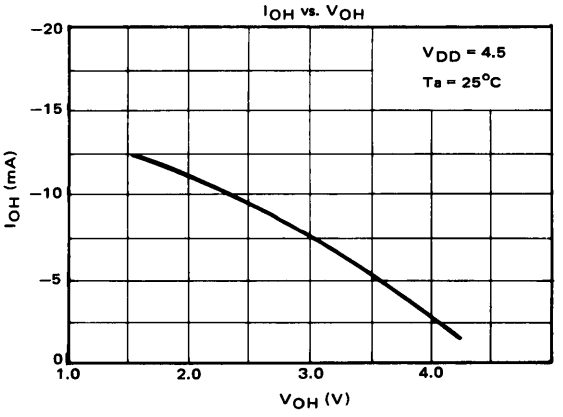

I_{DDS1} vs. Ta
V_{DD} = 5.5V
$\overline{CE}_2$ = 2.2V
other inputs
= 0.8 ~ 2.2V
I_{DDS1} (mA)
1.6
1.4
1.2
1.0
−40
0
40
80
Ta (°C)

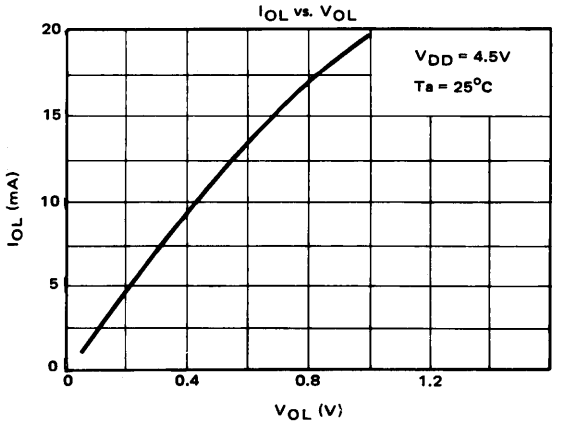

I_{DDS2} vs. V_{DD}
Ta = 25°C
$\overline{CE}_2$ = V_{DD} −0.5V
I_{DDS2} (nA)
3.4
3.2
3.0
2.8
3
4
5
6
7
V_{DD} (V)


I_{DDS1} vs. V_{IN} ($\overline{CE}_2$)
V_{DD} = 5.5V
other inputs
= 0.8 ~ 2.2V
Ta = 25°C
I_{DDS1} (mA)
2.0
1.5
1.0
0.5
0
1.0
2.0
3.0
4.0
5.0
V_{IN} ($\overline{CE}_2$) (V)


I_{DDS2} vs. V_{IN} ($\overline{CE}_2$)
V_{DD} = 5.5V
other inputs
= 0.8 ~ 2.2V
Ta = 25°C
I_{DDS2} (nA)
50
30
10
5
3
1
3.0
4.0
5.0
6.0
V_{IN} ($\overline{CE}_2$) (V)

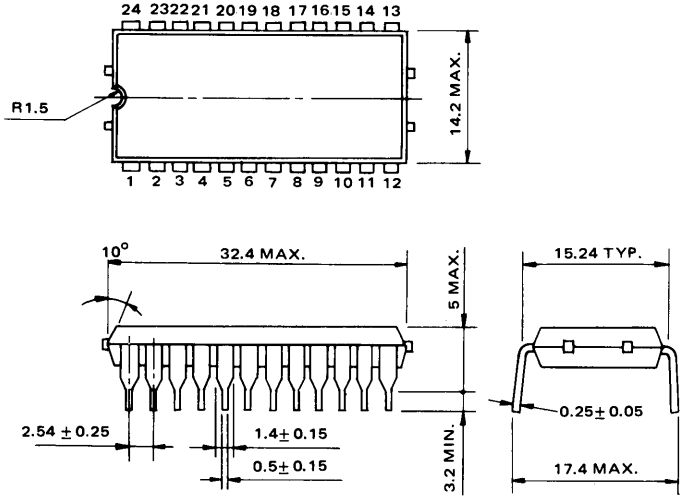

I_{DDS2} vs. Ta
V_{DD} = 5.5V
$\overline{CE}_2$ = 5.0V
I_{DDS2} (nA)
500
300
100
50
30
10
5
3
1
0.5
0.3
0.1
−40
0
40
80
Ta (°C)


I_{OH} vs. V_{OH}
V_{DD} = 4.5
Ta = 25°C
I_{OH} (mA)
−20
−15
−10
−5
0
1.0
2.0
3.0
4.0
V_{OH} (V)


I_{OL} vs. V_{OL}
V_{DD} = 4.5V
Ta = 25°C
I_{OL} (mA)
20
15
10
5
0
0
0.4
0.8
1.2
V_{OL} (V)

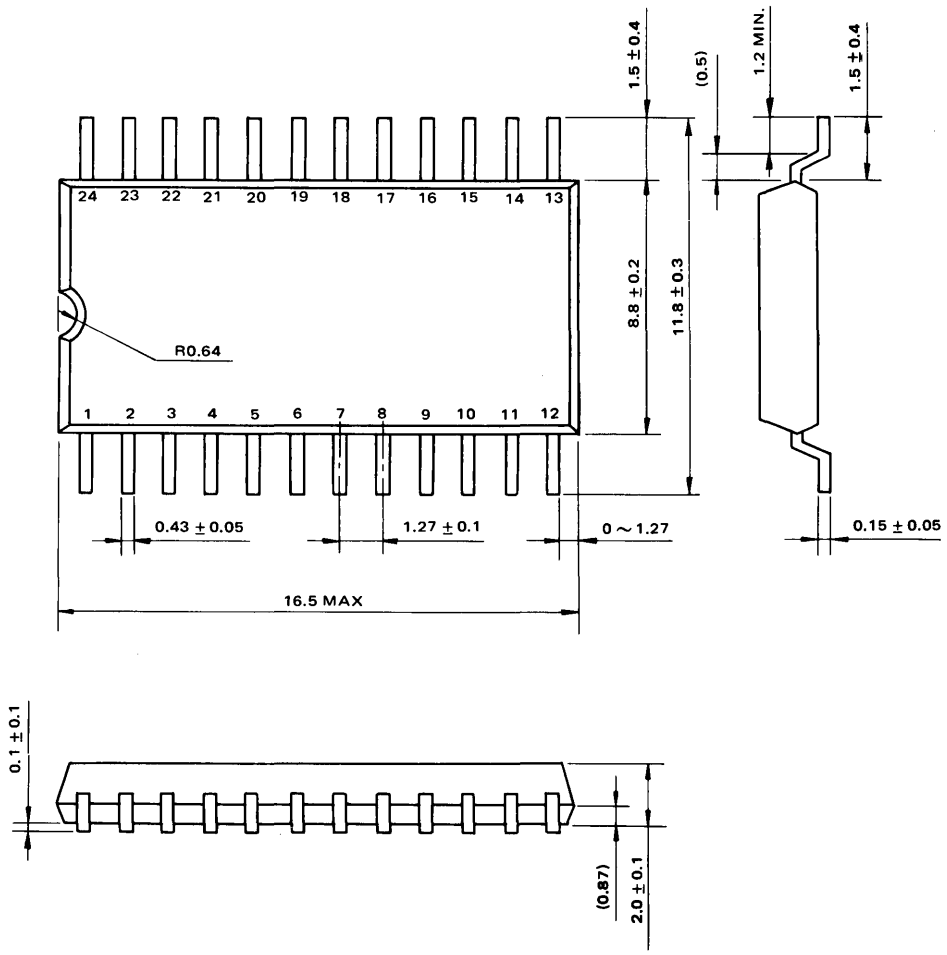
OUTLINE DRAWINGS

- **Plastic DIP**



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

- **Plastic FP**



Note : Each lead pitch is 1.27mm. All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

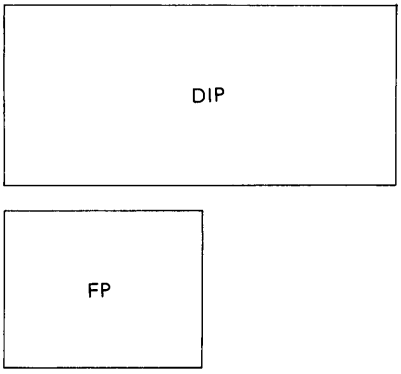
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

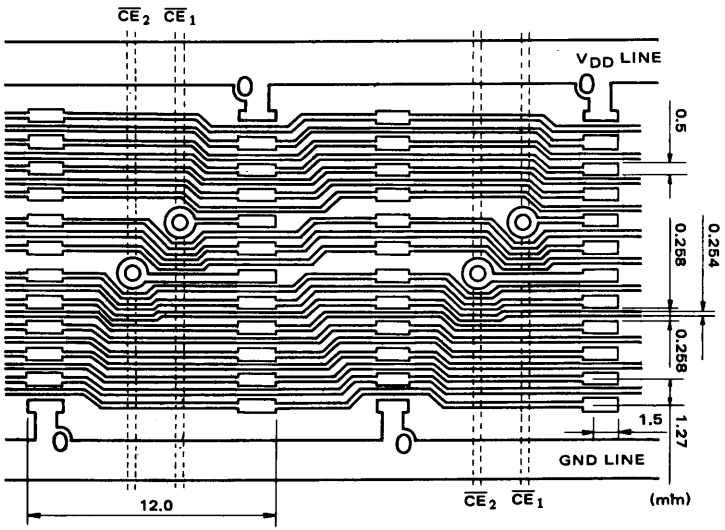
2. Comparison in occupied space.



3. Advantage of this package

- Small dimensions
- Capability of High Density Assembly
- Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5517AP/-2, TC5517APL/-2
TC5517AF/-2, TC5517AFL/-2

DESCRIPTION

The TC5517AP/AF in a 16384-bit static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

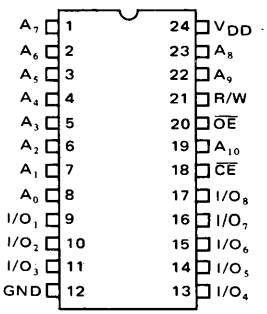
The TC5517AP/AF is featured by output enable and chip enable inputs, that is, $\overline{OE}$ for fast memory access and $\overline{CE}$ for a minimum standby current mode, and is suited for low power application where battery operation or battery back up for novolatility are required. Furthermore the TC5517APL guaranteed a standby current equal to or less than 1μA at 60°C ambient temperature is available.

The TC5517AP is also featured by pin compatibility with 2716 type EPROM. This means that the TC5517AP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM obtained as a result allows the wide application in microcomputer system.

FEATURES

- Standby Current
  - 0.2μA (Max.) at Ta = 25°C } TC5517APL/AFL
  - 1.0μA (Max.) at Ta = 60°C }
  - 1.0μA (Max.) at Ta = 25°C } TC5517AP/AF
  - 5.0μA (Max.) at Ta = 60°C }
- Low Power Dissipation : 200mW (Typ.) operating
- Single 5V Power Supply : 5V ± 10%
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Fully Static Operation
- Access Time
  - 250ns (Max.) : TC5517AP/APL/AF/AFL
  - 200ns (Max.) : TC5517AP-2/APL-2/AF-2/AFL-2
- Two Control Input ($\overline{CE}$, $\overline{OE}$)
- Pin Compatible with Nch Static RAM TMM2016P
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
  - Plastic DIP : TC5517AP/APL
  - Plastic FP : TC5517AF/AFL

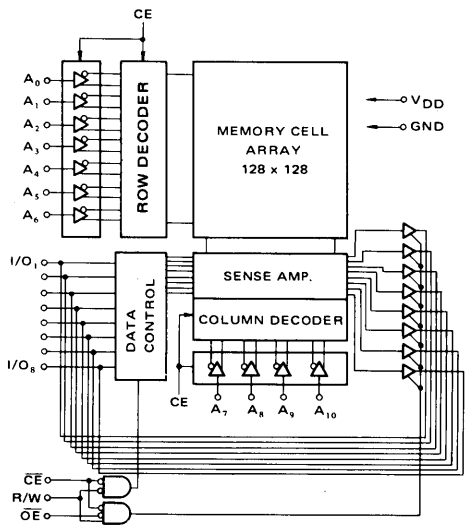
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	-0.3V ~ 7.0V
V_{IN}	Input Voltage	-0.3V ~ V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	-0.3V ~ V_{DD}+0.3V
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W)*
T_{STG}	Storage Temperature	-55°C ~ 150°C
T_{OPR}	Operating Temperature	-30°C ~ 85°C
T_{SOLDER}	Soldering Temperature • Time	260°C • 10 sec.

*Plastic FP

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}$ = V_{IH}, $0V \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			-1.0	-2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.5V V_{DD} = 2 ~ 5.5V	TC5517APL/AFL	Ta = 25°C	–	0.005	0.2	μA
				Ta = 60°C	–	–	1.0	
			TC5517AP/AF	Ta = 25°C	–	0.05	1.0	
				Ta = 60°C	–	–	5.0	
				Ta = 85°C	–	–	30	
I_{DDO1}	Operating Current	$\overline{CE}$ = 0V, V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0mA			–	40	70	mA
I_{DDO2}		$\overline{CE}$ = 0V, V_{IN} = V_{DD}/GND, I_{OUT} = 0mA			–	30	55	

Note : Typical values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = -30 ~ 85°C, V_{DD} = 5V ± 10%)

- **Read Cycle**

SYMBOL	PARAMETER	TC5517AP-2/APL-2 TC5517AF-2/AFL-2		TC5517AP/APL TC5517AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	200	–	250	–	ns
t_{ACC}	Access Time	–	200	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	100	–	100	ns
t_{CO}	$\overline{CE}$ to Output Valid	–	200	–	250	ns
t_{COE}	$\overline{OE}$ or $\overline{CE}$ to Output Active	10	–	10	–	ns
t_{OD}	Output High-Z from Deselection	–	80	–	80	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	ns

- **Write Cycle**

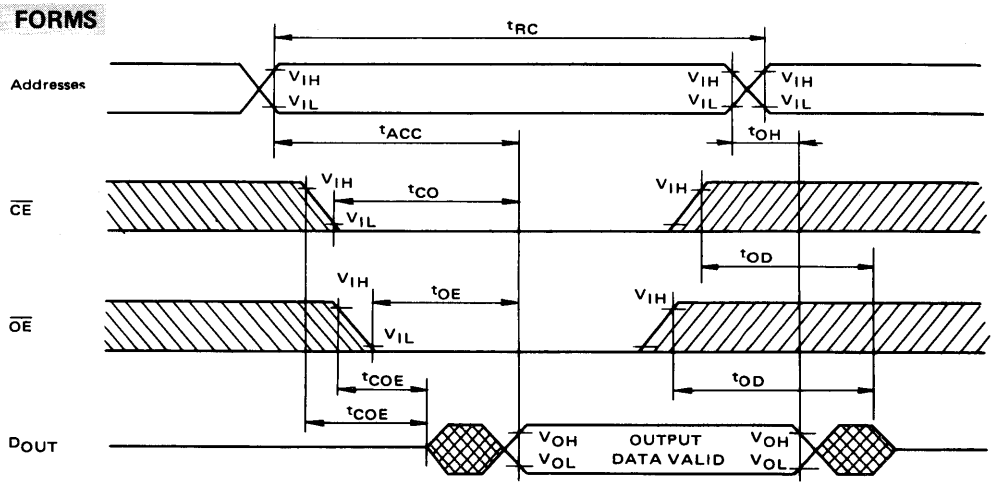
SYMBOL	PARAMETER	TC5517AP-2/APL-2 TC5517AF-2/AFL-2		TC5517AP/APL TC5517AF/AFL		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	200	–	250	–	ns
t_{WP}	Write Pulse Width	160	–	200	–	ns
t_{AW}	Address Set Up Time	0	–	0	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	ns
t_{ODW}	Output High-Z from R/W	–	80	–	80	ns
t_{OEW}	Output Active from R/W	10	–	10	–	ns
t_{DS}	Data Set Up Time	80	–	120	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns

A.C. TEST CONDITIONS

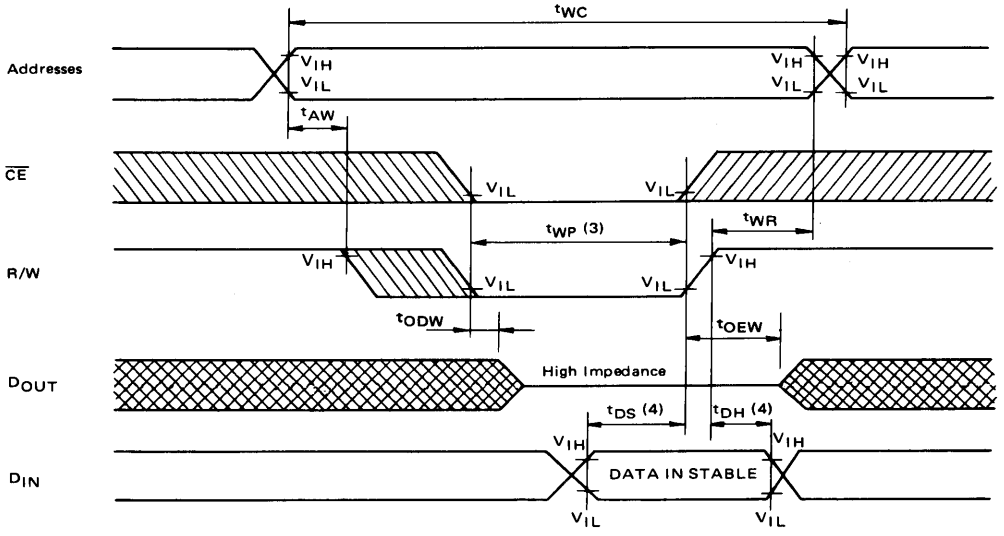
Output Load	:	100pF + 1TTL Gate
Input Pulse Levels	:	0.6V, 2.4V
Timing Measurement Reference Levels		
Input	:	0.8V and 2.2V
Output	:	0.8V and 2.2V
Input Pulse Rise and Fall Times	:	10ns

TIMING WAVE FORMS

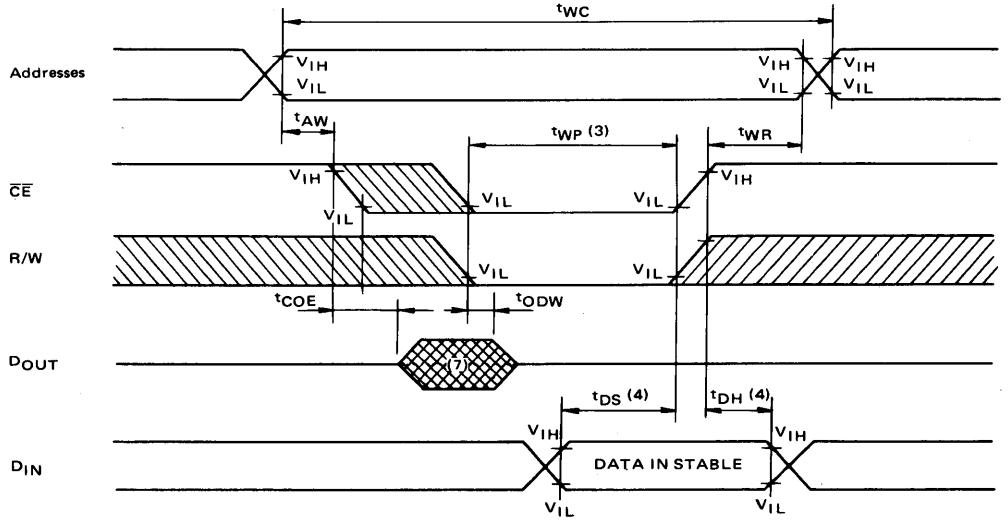
- **Read Cycle (1)**



- **Write Cycle 1 (1)**



- **Write Cycle 2 (2)**



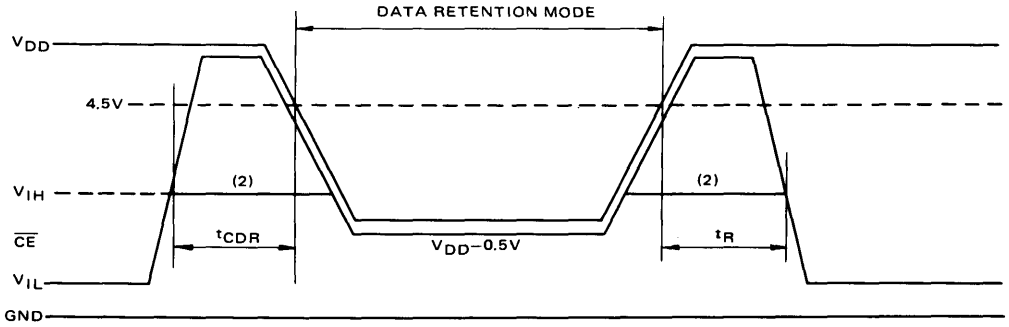
: UNKNOWN

NOTE: (1) R/W is high for a Read Cycle.
(2) $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
(3) t_{WP} is specified as the logical "AND" of $\overline{CE}$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}$ of R/W going low to the earlier of $\overline{CE}$ or R/W going high.
(4) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ of R/W going high.
(5) If the $\overline{CE}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(7) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS (Ta = -30 ~ 85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5517APL/AFL	Ta = 25°C	–	0.005	0.2	μA
			Ta = 60°C	–	–	1.0	
		TC5517AP/AF	Ta = 25°C	–	0.05	1.0	
			Ta = 60°C	–	–	5.0	
			Ta = 85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recovery Time			t_{RC}(1)	–	–	μs

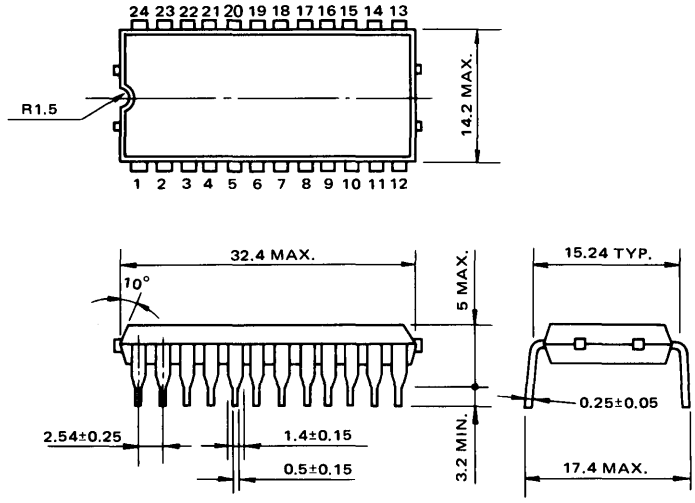
Note (1) t_{RC} : Read Cycle Time



Note (2) If the V_{IH} level of $\overline{CE}$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

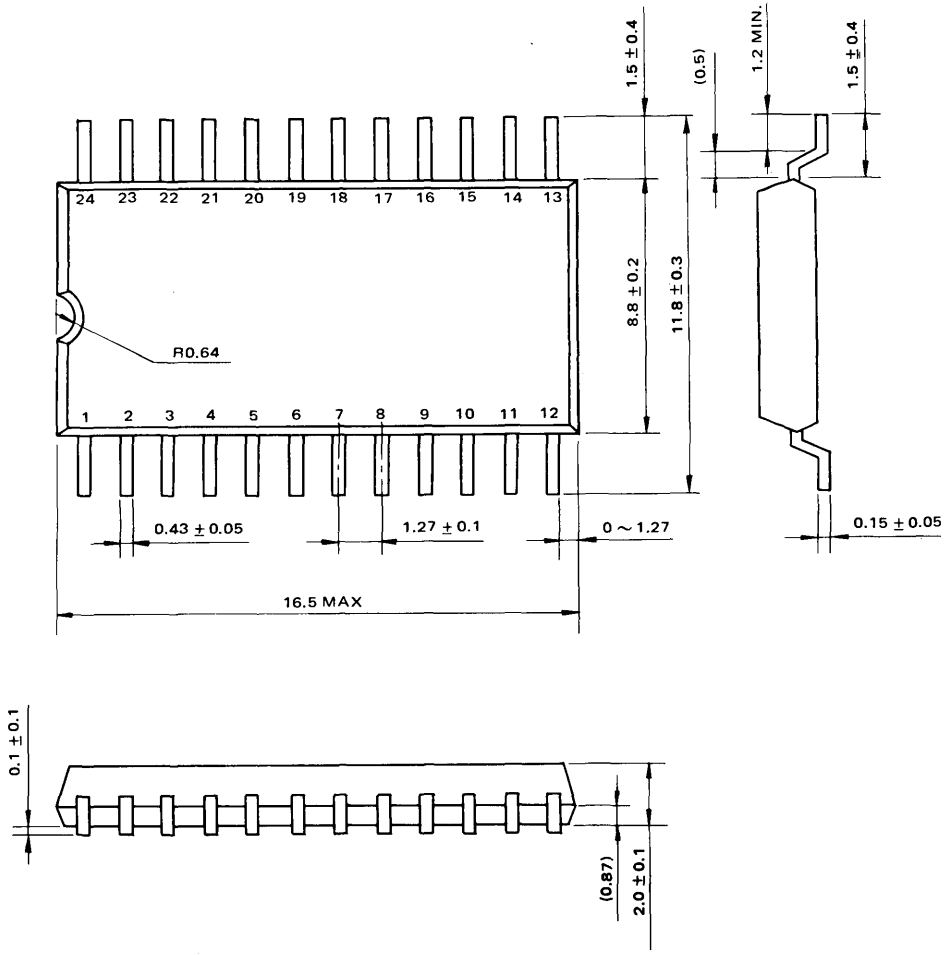
OUTLINE DRAWINGS

- **Plastic DIP**



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

- **Plastic FP**



Note : Each lead pitch is 1.27mm. All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

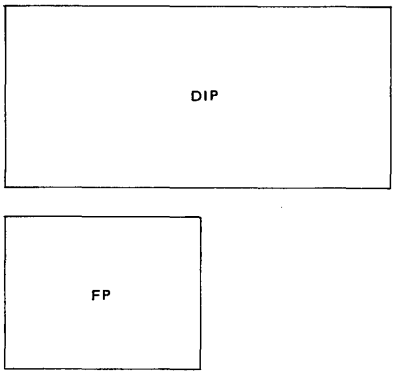
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit: mm

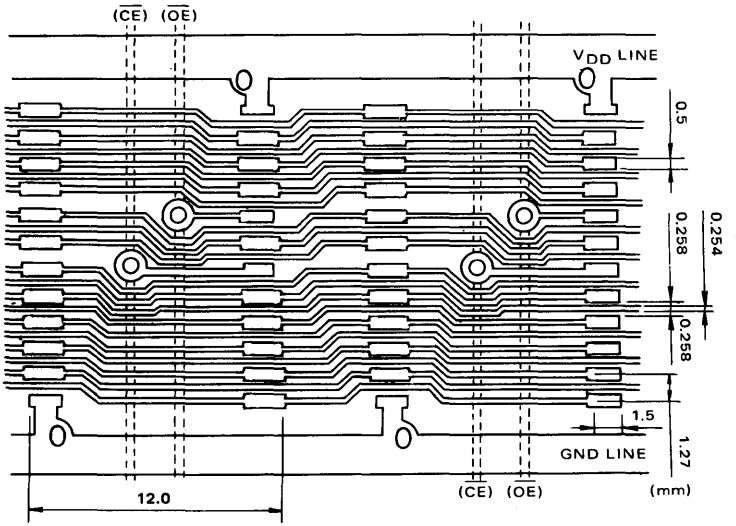
	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2. Comparison in occupied space



3. Advantage of this package
   Small dimensions
   Capability of High Density Assembly
   Capability of thin Assembly——Capability of Assembly on both side of PC board.

4. PC pattern layout example



TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5517BP-20/BPL-20/BP-25/BPL-25
TC5517BF-20/BFL-20/BF-25/BFL-25

DESCRIPTION

The TC5517BP/BF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

The TC5517BP/BF has a output enable input ($\overline{OE}$) for fast memory access and output control and chip enable input ($\overline{CE}$) which is used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up.

Also the high speed and low power characteristics which maximum access time is 200ns and maximum operating current is 5mA/MHz are achieved.

Thus the TC5517BP/BF is most suitable for use in low power applications where battery operations or battery back up for nonvolatility are required. Furthermore the TC5517BPL/BFL guaranteed a standby current equal to or less than 1μA at 60℃ ambient temperature available.

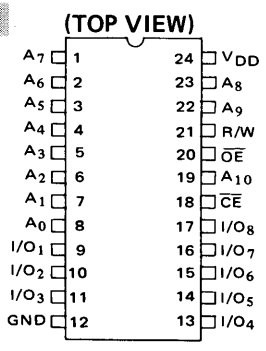
And the TC5517BP is pin compatible with 2716 type EPROM. This means that the TC5517BP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current
  0.2μA (Max.) at Ta=25°C, 1.0μA (Max.) at Ta=60°C } TC5517BPL-20/BPL-25/BFL-20/BFL-25
  1.0μA (Max.) at Ta=25°C, 5.0μA (Max.) at Ta=60°C } TC5517BP-20/BP-25/BF-20/BF-25
- Single 5V Power Supply : 5V±10%
- Data Retention Supply Voltage 2.0 ~ 5.5V
- Fully Static Operation
- Fast Access Time
  t_{ACC}=200ns(Max.) : TC5517BP-20/BPL-20/BF-20/BFL-20
  t_{ACC}=250ns(Max.) : TC5517BP-25/BPL-25/BF-25/BFL-25
- Output Buffer Control : $\overline{OE}$
- On-chip Address Transition Detector
- All inputs and outputs Directly TTL Compatible
- Three State Outputs
- Package
  Plastic DIP : TC5517BP-20/BPL-20/BP-25/BPL-25
  Plastic FP : TC5517BF-20/BFL-20/BF-25/BFL-25

PIN CONNECTION

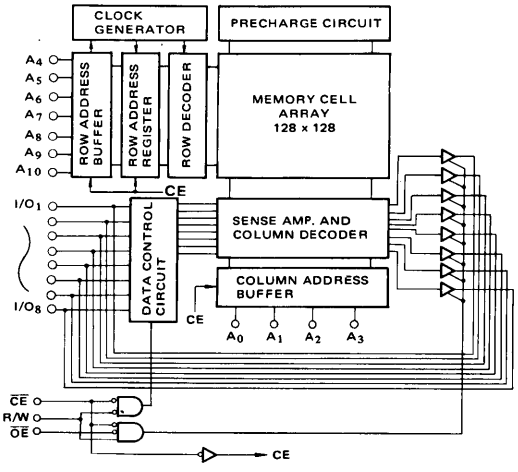
(TOP VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	$A_0 \sim A_{10}$	$I/O_1 \sim_8$	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	*	L	Stable	Data In	I_{DDO}
Output Deselect	L	H	H	*	High Impedance	I_{DDO}
**Standby	H	*	*	*	High Impedance	I_{DDS}

Note: *: H or L **: Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ V_{DD} + 0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V ~ V_{DD} + 0.3V
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W) *
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−30°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260 °C · 10 sec.

* Plastic FP = 0.45W

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE} = V_{IH}$, $OV \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE} \geqq V_{DD}$ −0.5V, V_{DD} = 2 ~ 5.5V	TC5517BPL/BFL	Ta=25°C	–	0.005	0.2	μA
				Ta=60°C	–	–	1.0	
			TC5517BP/BF	Ta=25°C	–	0.05	1.0	
				Ta=60°C	–	–	5.0	
				Ta=85°C	–	–	30	
I_{DDO1}	Operating Current	t_{cycle} = 200ns, $\overline{CE}$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{IH}/V_{IL}$		–	–	30	mA
I_{DDO2}			$V_{IN} = V_{DD}/GND$		–	–	25	
I_{DDO3}		t_{cycle} = 1μs, $\overline{CE}$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{IH}/V_{IL}$		–	–	10	
I_{DDO4}			$V_{IN} = V_{DD}/GND$		–	–	5	

Note: Typical Values are at Ta = 25°C, V_{DD} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMTER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note: This paramter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

- **Read Cycle**

SYMBOL	PARAMETER	TC5517BP-20/BPL-20 TC5517BF-20/BFL-20		TC5517BP-25/BPL-25 TC5517BF-25/BFL-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
tRC	Read Cycle Time	200	—	250	—	ns
tACC	Access Time	—	200	—	250	
tOE	$\overline{OE}$ to Output valid	—	100	—	120	
tCO	$\overline{CE}$ to Output Valid	—	200	—	250	
tCOE	$\overline{OE}$ or $\overline{CE}$ to Output Active	10	—	10	—	
tOD	Output High-Z from Deselection	—	60	—	70	
tOH	Output Hold from Address Change	20	—	20	—	

- **Write Cycle**

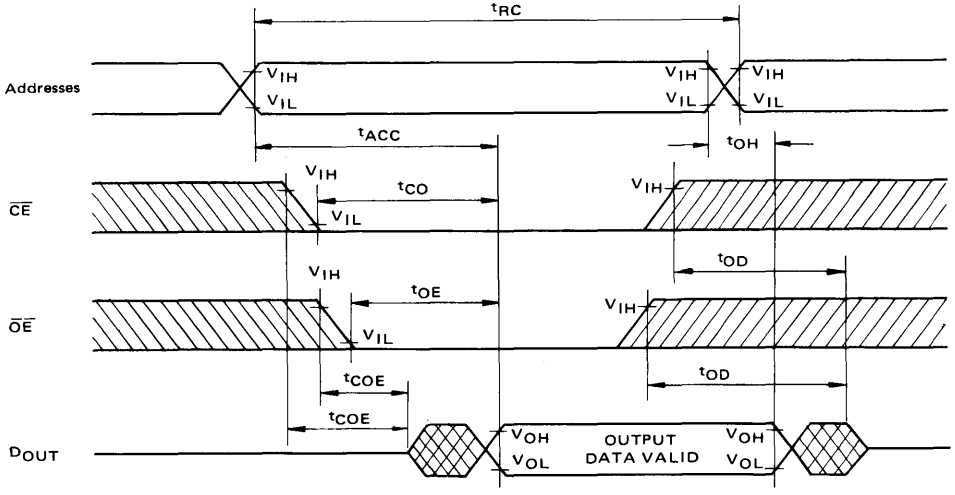
SYMBOL	PARAMETER	TC5517BP-20/BPL-20 TC5517BF-20/BFL-20		TC5517BP-25/BPL-25 TC5517BF-25/BFL-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
tWC	Write Cycle Time	200	—	250	—	ns
tWP	Write Pulse Width	150	—	170	—	
tAW	Address set up Time	0	—	0	—	
tWR	Write Recovery Time	0	—	0	—	
tODW	Outpur High-Z from R/W	—	60	—	70	
tOEW	Output Active from R/W	10	—	10	—	
tDS	Date set up Time	90	—	100	—	
tDH	Data Hold Time	0	—	0	—	

A.C. TEST CONDITIONS

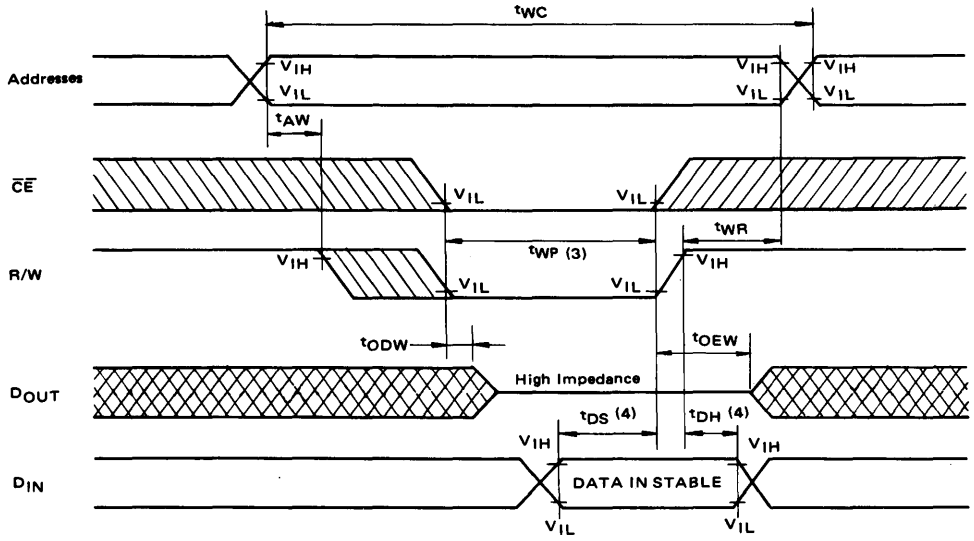
Output Load : 100pF + 1TTL Gate
Input Pulse Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V and 2.2V
Output : 0.8V and 2.2V
Input Pulse Rise and Fall Times : 10ns

TIMING WAVEFORMS

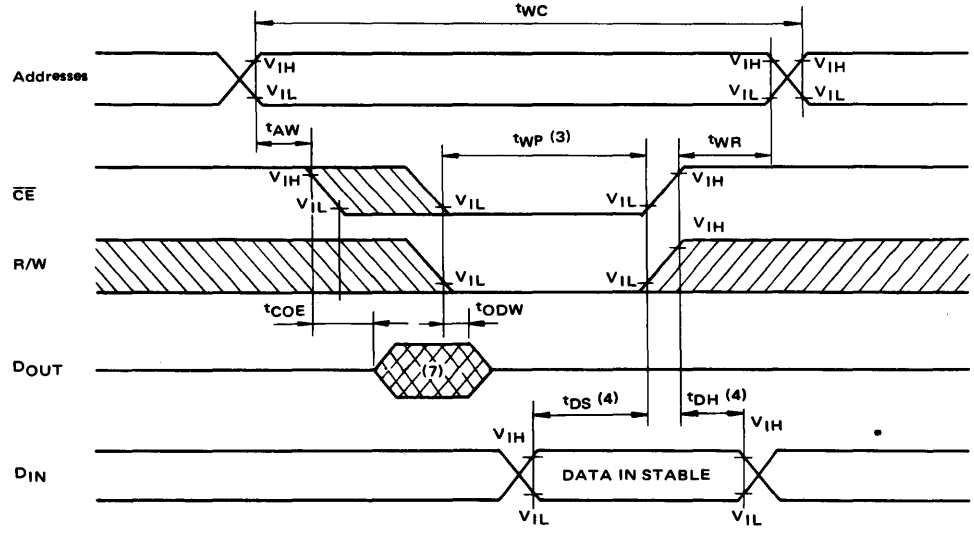
- **Read Cycle (1)**



- **Write Cycle 1 (2)**



- **Write Cycle 2 (2)**

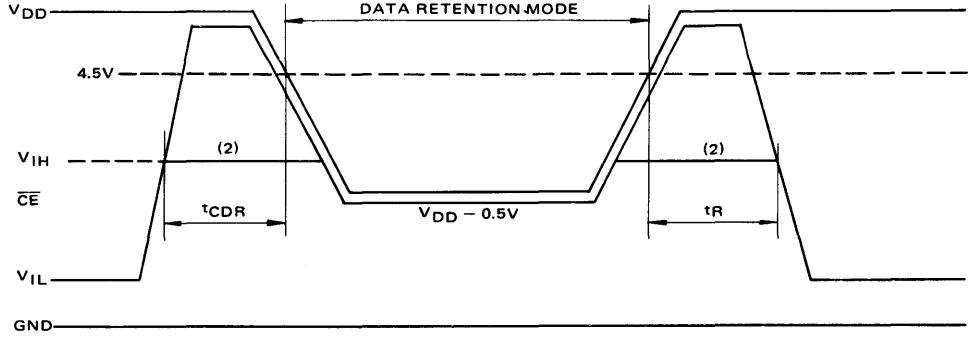


Note: (1) R/W is high for a Read Cycle.
(2) $\overline{OE}$ = V_{IH} or V_{IL}. If, $\overline{OE}$ = V_{IH} during write cycle, the output buffers remain in a high impedance state.
(3) t_{WP} is specified as the logical "AND" of $\overline{CE}$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}$ or R/W going low to the earlier of $\overline{CE}$ or R/W going high.
(4) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or R/W going high.
(5) If the $\overline{CE}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(7) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5517BPL/BFL	Ta=25°C	–	0.005	0.2	μA
			Ta=60°C	–	–	1.0	
		TC5517BP/BF	Ta=25°C	–	0.05	1.0	
			Ta=60°C	–	–	5.0	
			Ta=85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recovery Time			t_{RC}(1)	–	–	μs

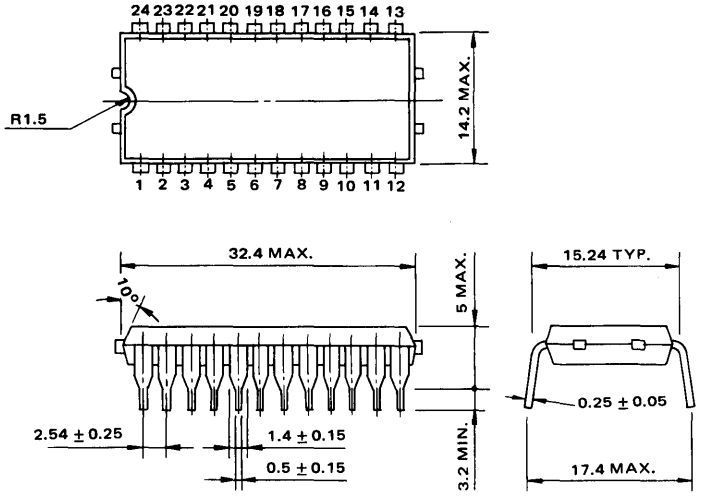
Note (1) t_{RC} : Read Cycle Time



Note (2) If the V_{IH} level of $\overline{CE}$ is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

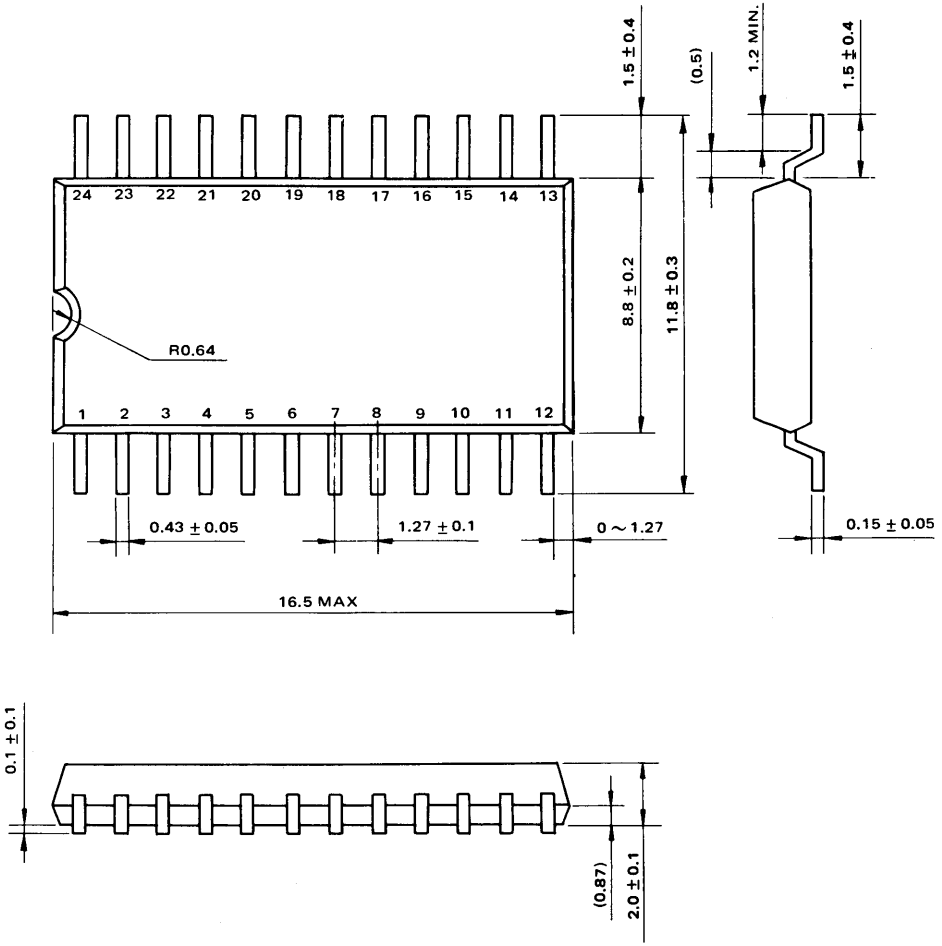
OUTLINE DRAWINGS

- **Plastic DIP**



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

- **Plastic FP**



Note : Each lead pitch is 1.27mm. All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

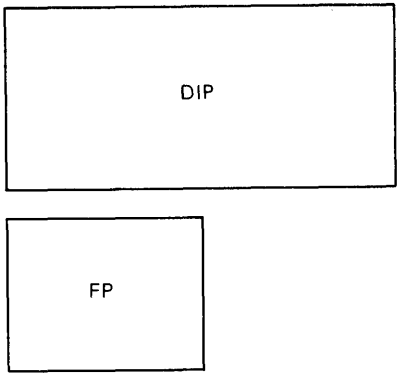
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit :mm

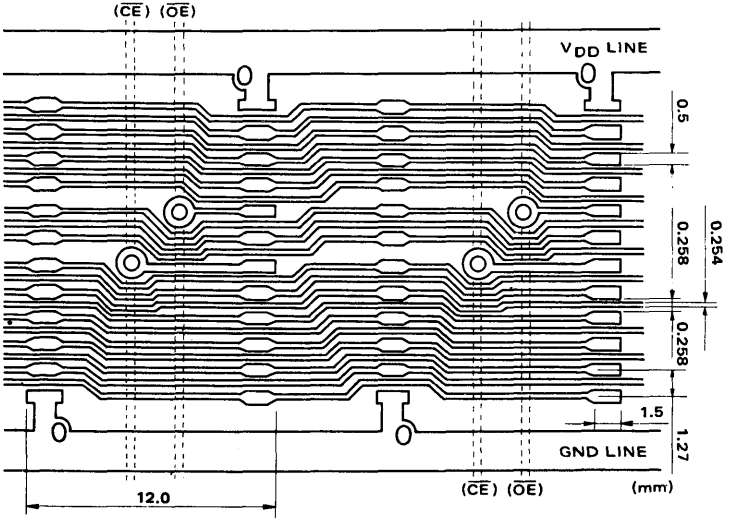
	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2. Comparison in occupied space



3. Advantage of this package
   Small dimensions
   Capability of High Density Assembly
   Capability of thin Assembly —— Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

2,048 WORD × 8 BIT CMOS STATIC RAM

TC5517CP-15/CPL-15/CP-20/CPL-20
TC5517CF-15/CFL-15/CF-20/CFL-20

DESCRIPTION

The TC5517CP/CF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply. The TC5517CP/CF has a output enable input ($\overline{OE}$) for fast memory access and output control and chip enable input ($\overline{CE}$) which is used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are achieved.

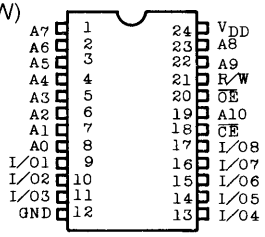
Thus the TC5517CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5517CPL/CFL guaranteed a standby current equal to or less than 1uA at 60℃ ambient temperature avaitble. And the TC5517CP is pin compatible with 2716 type EPROM. This means that the TC5517CP and EPROM can be interchanged in the same socket and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcompute system.

FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current
  0.2μA(Max.) at Ta=25°C, 1.0μA(Max.) at Ta=60°C : TC5517CPL-15/CPL-20, CFL-15/CFL-20
  1.0μA(Max.) at Ta=25°C, 5.0μA(Max.) at Ta=60°C : TC5517CP-15/CP-20, CF-15/CF-20
- Single 5V Power Supply: 5V±10%
- Data Retention Supply Voltage
  2.0~5.5V
- Fully Static Operation
- Fast Access Time
  t_{ACC}=150ns(Max.) : TC5517CP-15/CPL-15, CF-15/CFL-15
  t_{ACC}=200ns(Max.) : TC5517CP-20/CPL-20, CF-20/CFL-20
- Output Buffer Control : $\overline{OE}$
- On-Chip Address Transition Detector
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package;
  Plastic DIP: TC5517CP-15/CPL-15, CP-20/CPL-20 (600 mil)
  Plastic FP : TC5517CF-15/CFL-15, CF-20/CFL-20

PIN CONNECTION

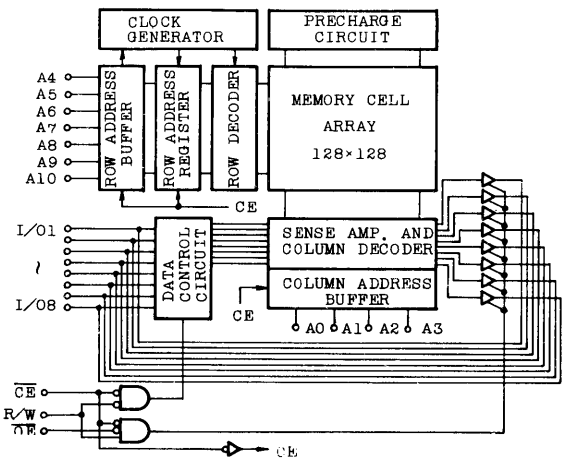
(TOP VIEW)



PIN NAMES

A_0~A_{10}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE}$	$\overline{OE}$	R/W	$A_0 \sim A_{10}$	$I/O_1 \sim I/O_8$	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	*	L	Stable	Data In	I_{DDO}
Output Deselect	L	H	H	*	High Impedance	I_{DDO}
* * Standby	H	*	*	*	High Impedance	I_{DDS}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3~7.0V
V_{IN}	Input Voltage	−0.3V~V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V~V_{DD}+0.3V
P_D	Power Dissipation(Ta=85°C)	0.8W(0.45W)*
T_{STG}	Storage Temperature	−55°C~150°C
T_{OPR}	Operating Temperature	−30°C~85°C
T_{SOLDER}	Soldering Temperature·Time	260°C·10sec.

*Plastic FP=0.45W

RECOMMENDED D. C. OPERATING CONDITIONS (Ta=−30~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Voltage	2.0	—	5.5	V

D. C. CHARACTERISTICS (Ta=30~85°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS			TC5517CP-15/CF-15 MIN.	TC5517CP-15/CF-15 MAX.	TC5517CP-20/CF-20 MIN.	TC5517CP-20/CF-20 MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			—	±1.0		±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}=V_{IH}$, $0V \leqq V_{I/O} \leqq V_{DD}$			—	±5.0		±5.0	μA
I_{OH}	Output High Current	V_{OH}2.4V			−1.0	—	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			2.0	—	2.0	—	mA
I_{DDS1}	Standby Current	$\overline{CE2}$=2.2V			—	3.0	—	3.0	mA
I_{DDS2}		$\overline{CE} \leqq V_{DD}-0.5V$	TC5517CPL/CFL	Ta=25°C	—	0.2	—	0.2	μA
				Ta=60°C	—	1.0	—	1.0	
			TC5517CP/CF	Ta=25°C	—	1.0	—	1.0	
				Ta=60°C	—	5.0	—	5.0	
				Ta=85°C	—	30	—	30	
I_{DDO1}	Operating Current	t_{cycle}=Mini cycle, $\overline{CE}$=0V, I_{OUT}=0mA		$V_{IN}=V_{IH}/V_{IL}$	—	45		30	mA
I_{DDO2}				$V_{IN}=V_{DD}/GND$	—	40		25	
I_{DDO3}		t_{cycle}=1μs, $\overline{CE}$=0V, I_{OUT}=0mA		$V_{IN}=V_{IH}/V_{IL}$	—	10	—	10	
I_{DDO4}				$V_{IN}=V_{DD}/GND$	—	5	—	5	

Note : Typical values are at Ta=25°C, V_{DD}=5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	—	5	10	pF
$C_{I/O}$	Input/Output Capacitance	—	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($Ta = -30 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC5517CP-15/CPL-15 TC5517CF-15/CFL-15		TC5517CP-20/CPL-20 TC5517CF-20/CFL-20		UNITS
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	—	200	—	ns
t_{ACC}	Address Time	—	150	—	200	
t_{OE}	$\overline{CE}$ to Output Valid	—	70	—	100	
t_{CO}	$\overline{CE}$ to Output Valid	—	150	—	200	
t_{COE}	$\overline{CE}$ or $\overline{OE}$ to Output Active	10	—	10	—	
t_{OD}	Output High-Z from Deselection	—	50	—	60	
t_{OH}	Output Hold from Address Change	15	—	20	—	

Write Cycle

SYMBOL	PARAMETER	TC5517CP-15/CPL-15 TC5517CF-15/CFL-15		TC5517CP-20/CPL-20 TC5517CF-20/CFL-20		UNITS
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	200	—	ns
t_{WP}	Write Pulse Width	120	—	150	—	
t_{AW}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{ODW}	Output High-Z from R/W	—	50	—	60	ns
t_{OEW}	Output Active from R/W	10	—	10	—	
t_{DS}	Data Set up Time	60	—	80	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels: 0.6V, 2.4V

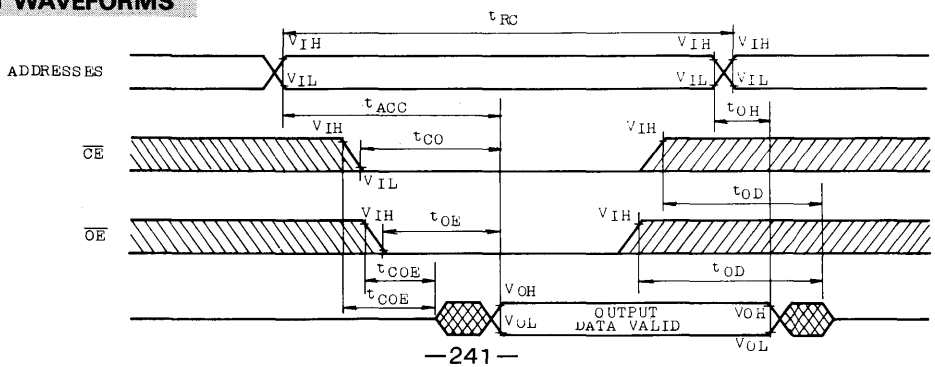
Timing Measurement Reference Levels

Input : 0.8V and 2.2V

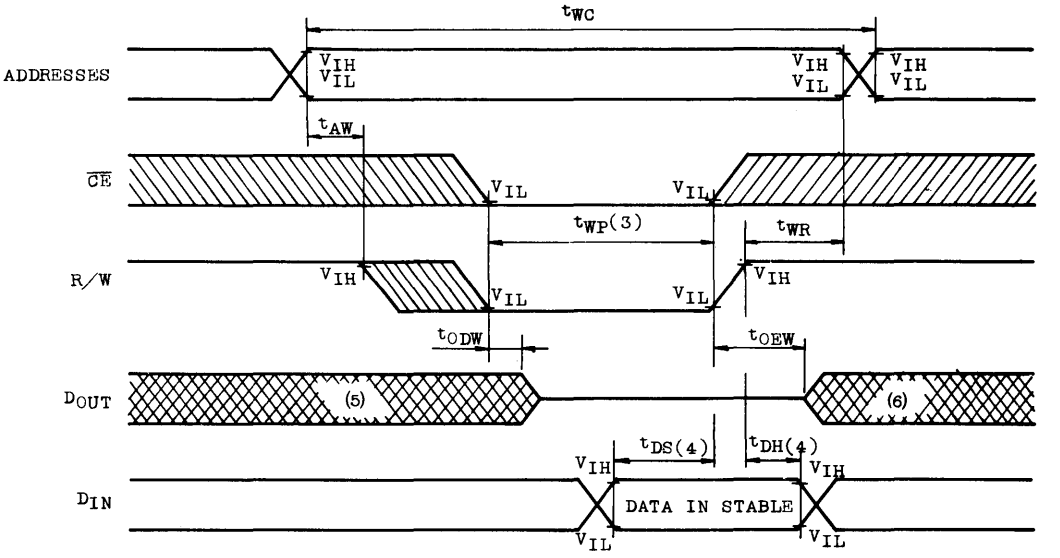
Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

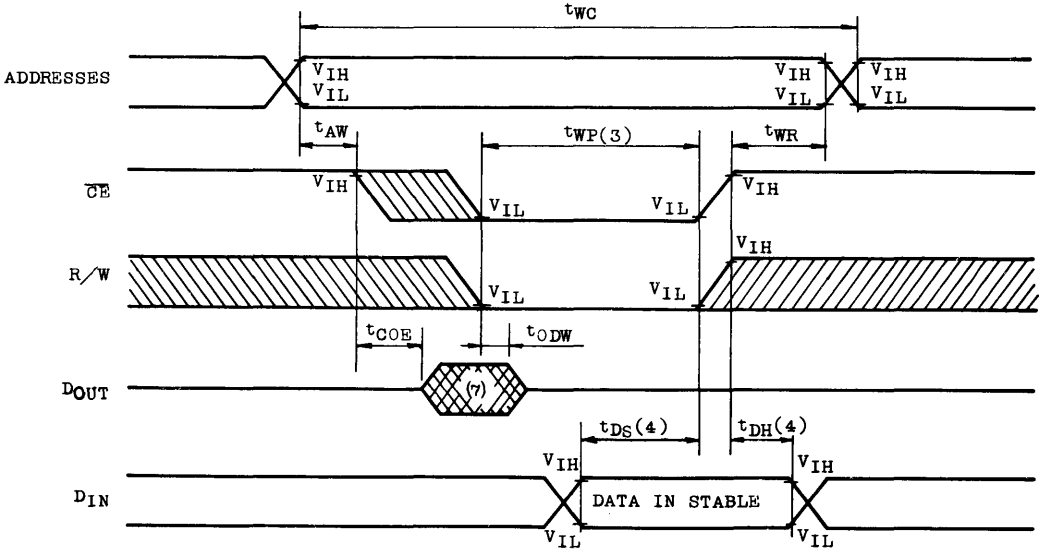
TIMING WAVEFORMS



- Write Cycle 1 (2)



- Write Cycle 2 (2)



: UNKNOWN

Note:

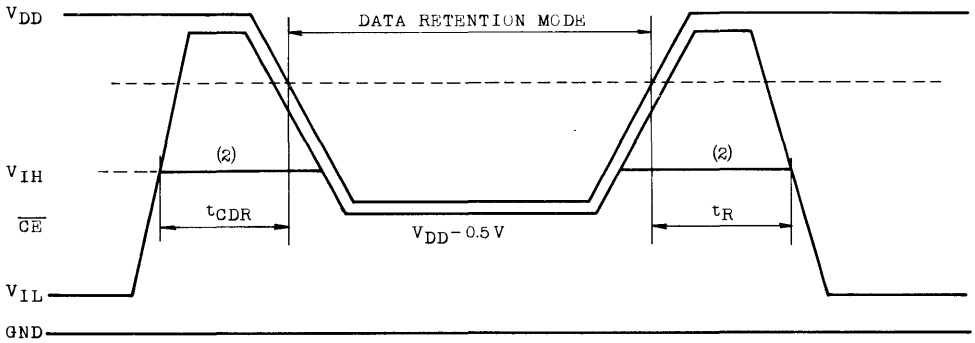
1. R/W is high for a Read Cycle.
2. $\overline{OE}$=V_{IH} or V_{IL}. If, $\overline{OE}$=V_{IH} during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specfied as the logical "AND" of $\overline{CE}$ and R/W.
   t_{WP} is measured from the latter of $\overline{CE}$ or R/W going low to the earlier of $\overline{CE}$ or R/W going high.
4. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}$ or R/W going high.
5. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
7. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in high impedance state in this period.

DATA RETENTION CHARACTERISTICS (Ta=−30~85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	—	5.5	V
I_{DDS2}	Standby Current	TC5517CPL/CFL	Ta=25°C	—	0.005	0.2	μA
			Ta=60°C	—	—	1.0	
		TC5517CP/CF	Ta=25°C	—	0.05	1.0	
			Ta=60°C	—	—	5.0	
			Ta=85°C	—	—	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	—	—	μs
t_R	Recovery Time			t_{RC}(1)	—	—	

Note :

1. t_{RC} : Read Cycle Time

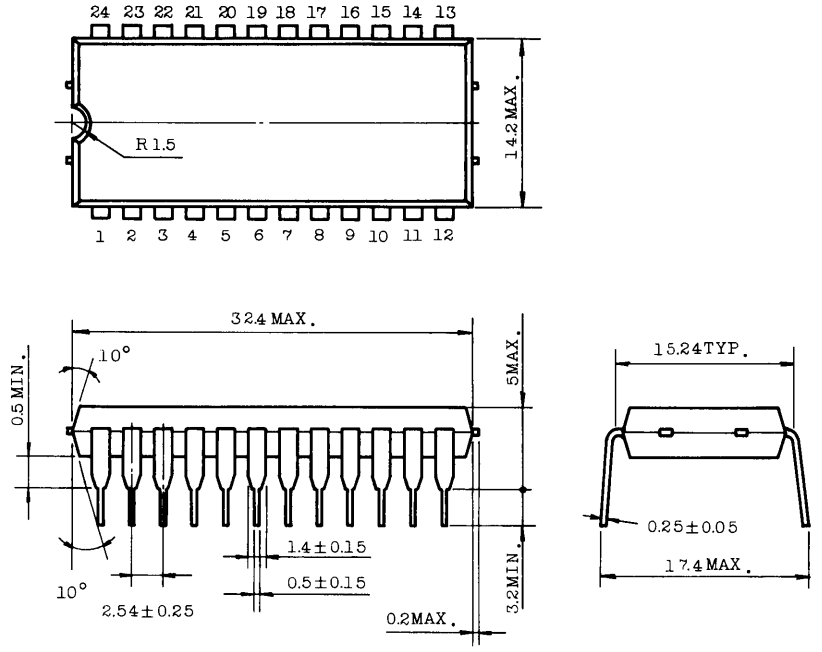


Note :

2. If the V_{IH} level of $\overline{CE}$ is 2.2V, during the period that tne V_{DD} voltage is going down from 4.5V to 2.7V I_{DDS1} current flows.

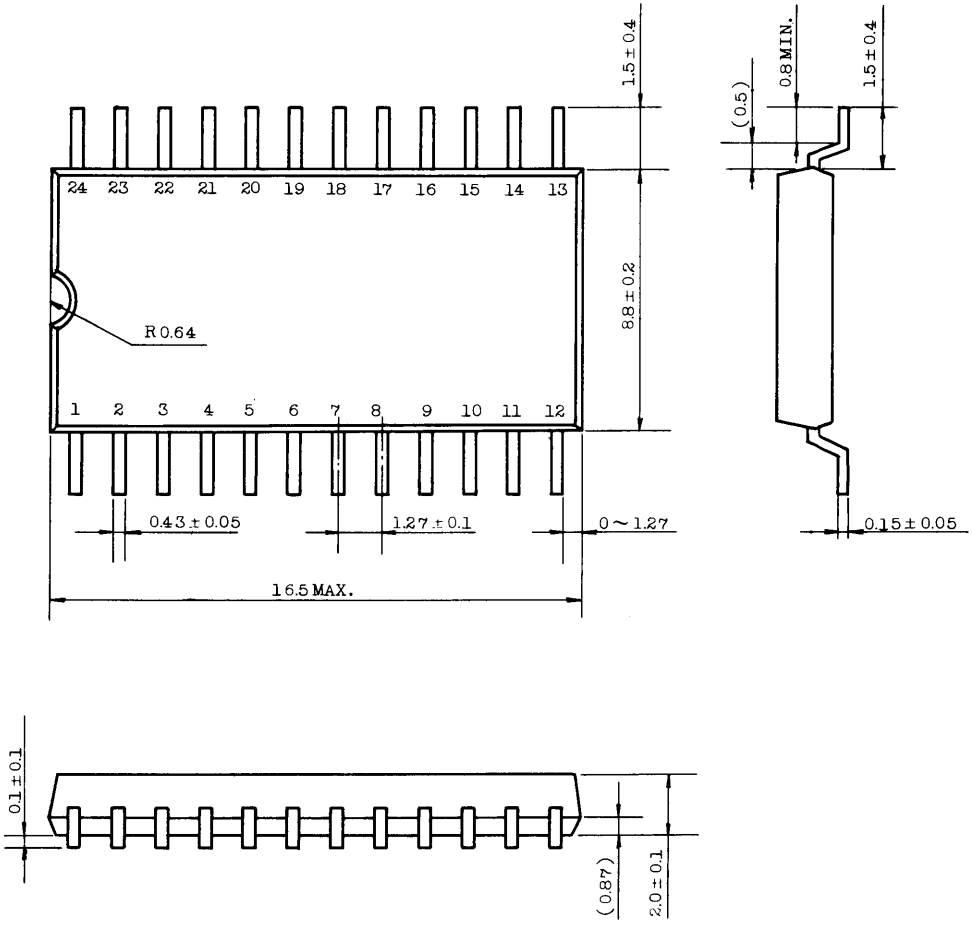
OUTLINE DRAWINGS

- Plastic DIP



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

● Plastic FP



Note : Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

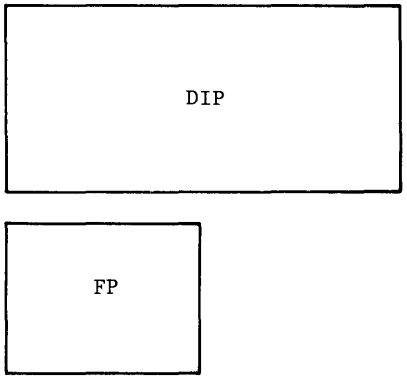
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

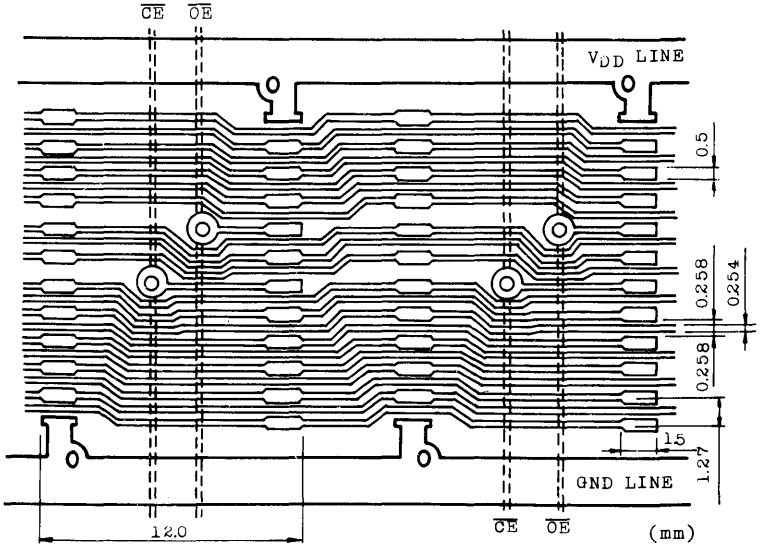
	Flat pacpage	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2. Comparison in occupied space.



3. Advantage of this package
   Small dimensions
   Capability of High Density Assembly
   Capability of thin Assembly——Capability of Assembly on both side of PC board.

4. PC pattern layout example.



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

2,048 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5518BP-20/BPL-20/BP-25/BPL-25
TC5518BF-20/BFL-20/BF-25/BFL-25

DESCRIPTION

The TC5518BP/BF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by 8 bits using CMOS technology, and operates from a single 5 volt supply.

The TC5518BP/BF has two chip enable inputs, $\overline{CE}_1$ and $\overline{CE}_2$, which are used for device selection and can be used in order to achieve the minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 200ns and maximum operating current is 5mA/MHz are achieved.

Thus the TC5518BP/BF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518BPL/BFL guaranteed a standby current equal to or less than 1μA at 60℃ ambient temperature available.

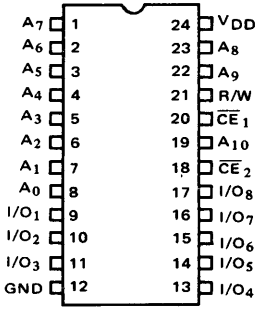
And the TC5518BP is pin compatible with 2716 type EPROM. This means that the TC5518BP and EPROM can be interchanged in the same socket, and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current
  0.2μA (Max.) at Ta = 25°C } TC5518BPL/
  1.0μA (Max.) at Ta = 60°C } BFL-20
  1.0μA (Max.) at Ta = 25°C } TC5518BP/
  5.0μA (Max.) at Ta = 60°C } BF-20
- Single 5V Power Supply: 5V±10%
- Data Retention Supply Voltage
  2.0 ~ 5.5V
- Fully Static Operation
- Fast Access Time
  t_{ACC}=200ns(Max.): TC5518BP-20/BPL-20/BF-20/BFL-20
  t_{ACC}=250ns(Max.): TC5518BP-25/BPL-25/BF-25/BFL-25
- Two Chip Enables ($\overline{CE}_1$, $\overline{CE}_2$) for Simple Memory Expansion and Battery Back Up
- On-chip Address Transition Detector
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package
  Plastic DIP: TC5518BP-20/BPL-20/BP-25/BPL-25
  Plastic FP : TC5518BF-20/BFL-20/BF-25/BFL-25

PIN CONNECTION

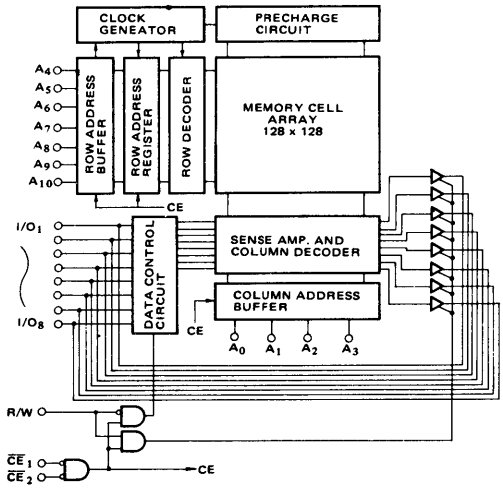
(Top VIEW)



PIN NAMES

$A_0 \sim A_{10}$	Address Inputs
R/W	Read/Write Control Input
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE}_2$	$\overline{CE}_1$	R/W	$A_0 \sim A_{10}$	$I/O_1 \sim_8$	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	L	L	Stable	Data In	I_{DDO}
** Standby 1	*	H	*	*	High Impedance	I_{DDS}
** Standby 2	H	*	*	*	High Impedance	I_{DDS}

Note; *: H or L **: Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3V ~ 7.0V
V_{IN}	Input Voltage	−0.3V ~ V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V ~ V_{DD}+0.3V
P_D	Power Dissipation (Ta = 85°C)	0.8W (0.45W)*
T_{STG}	Storage Temperature	−55°C ~ 150°C
T_{OPR}	Operating Temperature	−30°C ~ 85°C
T_{SOLDER}	Soldering Temperature · Time	260°C · 10 sec

*: Plastic FP = 0.45W

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{DH}	Data Retention Voltage	2.0	–	5.5	V

D.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			–	–	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE}_2 = V_{IH}$, $OV \leqq V_{I/O} \leqq V_{DD}$			–	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−1.0	−2.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			2.0	3.0	–	mA
I_{DDS1}	Standby Current	$\overline{CE}_2$ = 2.2V or $\overline{CE}_1$ = 2.2V			–	1.0	3.0	mA
I_{DDS2}		$\overline{CE}_2 \geqq V_{DD}$ −0.5V or $\overline{CE}_1 \leqq V_{DD}$ −0.5V, V_{DD} = 2 ~ 5.5V	TC5518BPL/BFL	Ta=25°C	–	0.005	0.2	mA
				Ta=60°C	–	–	1.0	μA
			TC5518BP/BF	Ta=25°C	–	0.05	1.0	
				Ta=60°C	–	–	5.0	
				Ta=85°C	–	–	30	
I_{DDO1}	Operating Current	t_{cycle} = 200ns, $\overline{CE}_1$ = $\overline{CE}_2$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{IH}/V_{IL}$		–	–	30	mA
I_{DDO2}			$V_{IN} = V_{DD}$/GND		–	–	25	
I_{DDO3}		t_{cycle} = 1μs, $\overline{CE}_1$ = $\overline{CE}_2$ = OV, I_{OUT} = 0mA	$V_{IN} = V_{IH}/V_{IL}$		–	–	10	
I_{DDO4}			$V_{IN} = V_{DD}$/GND		–	–	5	

Note: Typical Values are at Ta = 25°C, V_{DD} = 5V

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	–	5	10	pF
$C_{I/O}$	Input/Output Capacitance	–	5	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = −30 ~ 85°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC5518BP-20/BPL-20 TC5518BF-20/BPL-20		TC5518BP-25/BPL-25 TC5518BF-25/BFL-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
tRC	Read Cycle Time	200	—	250	—	ns
tACC	Access Time	—	200	—	250	
tCO1	$\overline{CE1}$ to Output Valid	—	200	—	250	
tCO2	$\overline{CE2}$ to Output Valid	—	200	—	250	
tCOE	$\overline{CE1}$ or $\overline{CE2}$ to Output Active	10	—	10	—	
tOD	Output High-Z Deselection	—	60	—	70	
tOH	Output Hold from Address Change	20	—	20	—	

Write Cycle

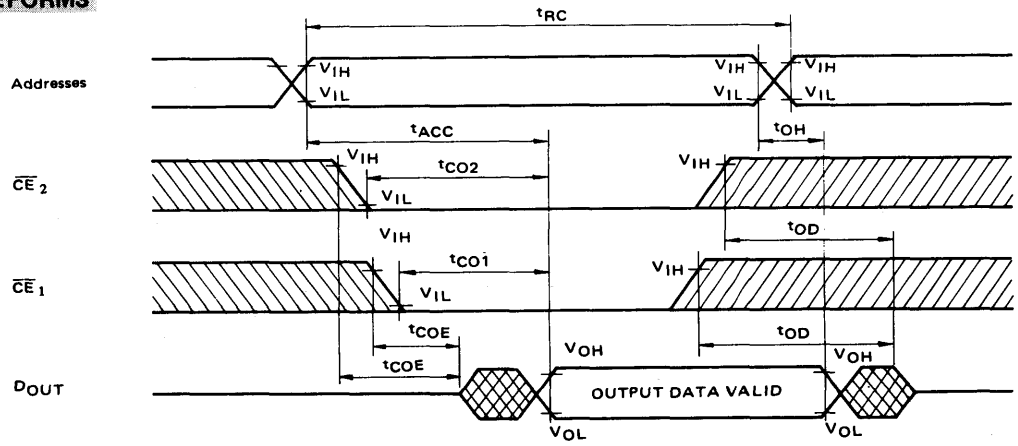
SYMBOL	PARAMETER	TC5518BP-20/BPL-20 TC5518BF-20/BFL-20		TC5518BP-25/BPL-25 TC5518BF-25/BFL-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
tWC	Write Cycle Time	200	—	250	—	ns
tWP	Write Pulse Width	150	—	170	—	
tAW	Address set up Time	0	—	0	—	
tWR	Write Recovery Time	0	—	0	—	
tODW	Outpur High-Z from R/W	—	60	—	70	
tOEW	Output Active from R/W	10	—	10	—	
tDS	Data set up Time	90	—	100	—	
tDH	Data Hold Time	0	—	0	—	

A.C. TEST CONDITIONS

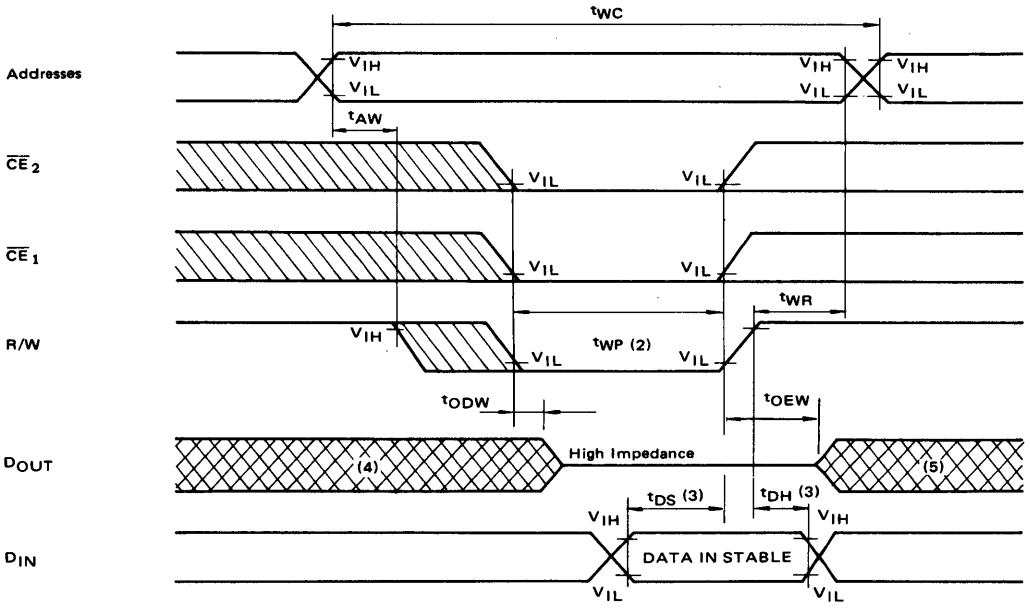
Output Load	:	100pF + 1TTL Gate
Input Pulse Levels	:	0.6V, 2.4V
Timing Mesurement Reference Levels		
Input	:	0.8V and 2.2V
Output	:	0.8V and 2.2V
Input Pulse Rise and Fall Times	:	10 ns

TIMING WAVEFORMS

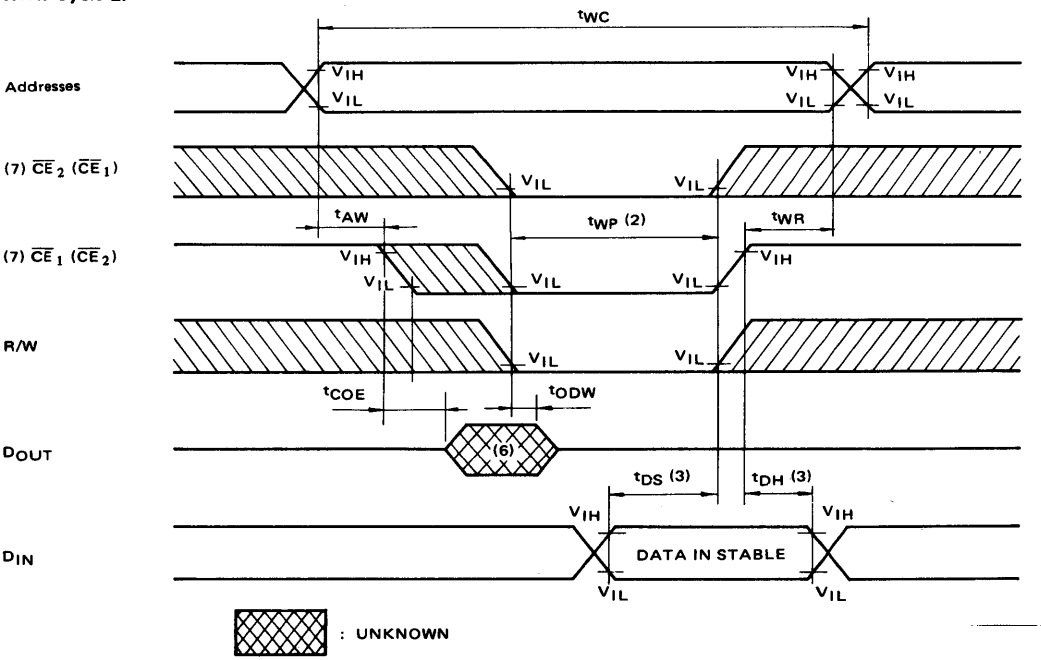
Read Cycle (1)



Write Cycle 1.



Write Cycle 2.

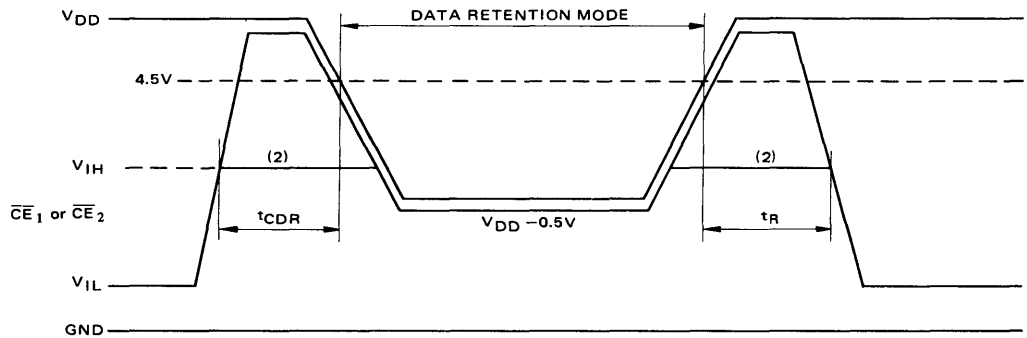


Note: (1) R/W is high for a Read Cycle.
(2) t_{WP} is specified as the logical "AND" or $\overline{CE}1$, $\overline{CE}2$ and R/W.
t_{WP} is measured from the latter of $\overline{CE}1$, $\overline{CE}2$ or R/W going low to the earlier of $\overline{CE}1$, $\overline{CE}2$ or R/W going high.
(3) t_{DH}, t_{DS} are measured from the earlier of $\overline{CE}1$, $\overline{CE}2$ or R/W going high.
(4) If the $\overline{CE}1$, or $\overline{CE}2$ low transition occurs simultaneously with or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(5) If the $\overline{CE}1$ or $\overline{CE}2$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
(6) If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE}1$ or $\overline{CE}2$ low transition, the output buffers remain in a high impedance state in this period.
(7) A write occurs during the overlap of a low $\overline{CE}1$, low $\overline{CE}2$ and low R/W.
In write cycle 2, write is controlled by either $\overline{CE}1$ or $\overline{CE}2$.

DATA RETENSION CHARACTERISTICS (Ta = −30 ~ 85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	–	5.5	V
I_{DDS2}	Standby Current	TC5518BPL/BFL	Ta = 25°C	–	0.005	0.2	μA
			Ta = 60°C	–	–	1.0	
		TC5518BP/BF	Ta = 25°C	–	0.05	1.0	
			Ta = 60°C	–	–	5.0	
			Ta = 85°C	–	–	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	–	–	μs
t_R	Recover Time			t_{RC}(1)	–	–	μs

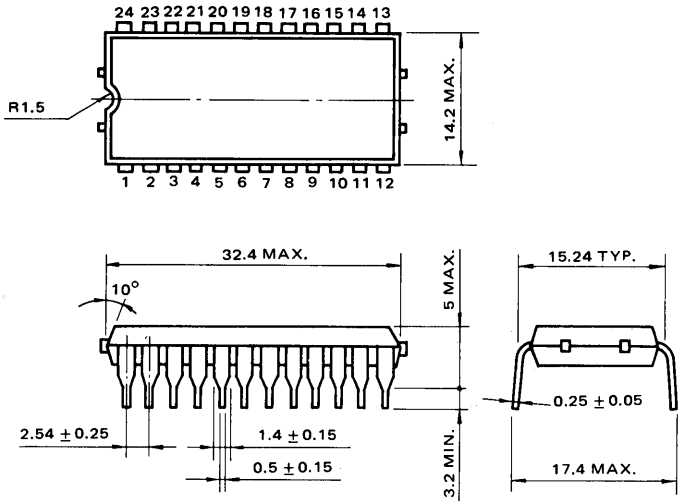
Note (1) t_{RC} : Read Cycle Time



Note (2) if the V_{IH} level of $\overline{CE}_2$ ($\overline{CE}_1$) is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

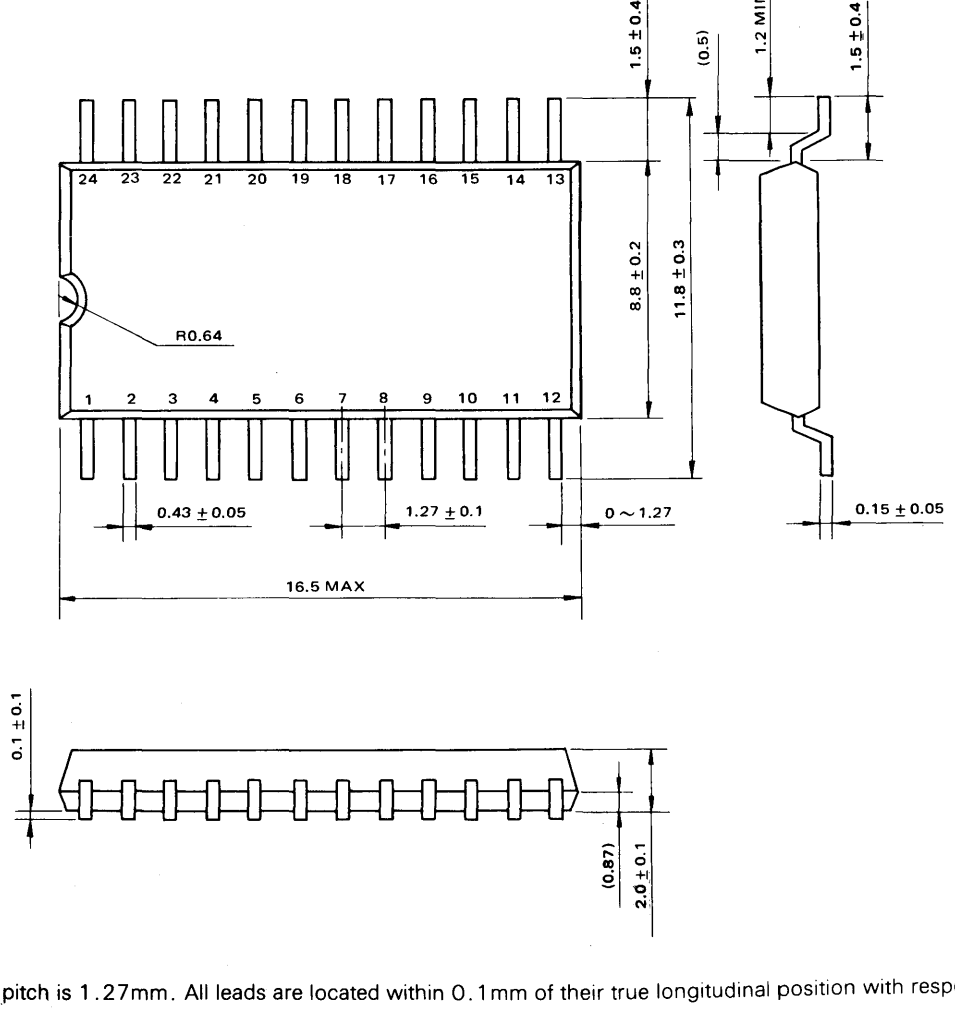
OUTLINE DRAWINGS

- **Plastic DIP**



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

- **Plastic FP**



Note : Each lead pitch is 1.27mm. All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKAGE INFORMATION FOR FLAT PACKAGE

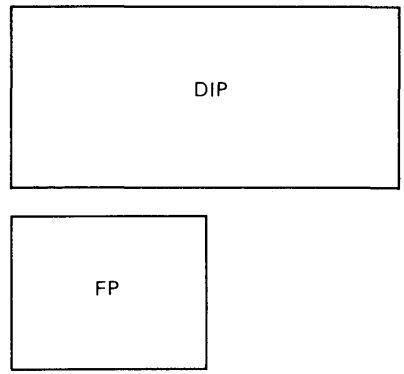
This new flat package is a very small and thin compared with conventional standard dual-in-line package. Differences are as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

	Flat package	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

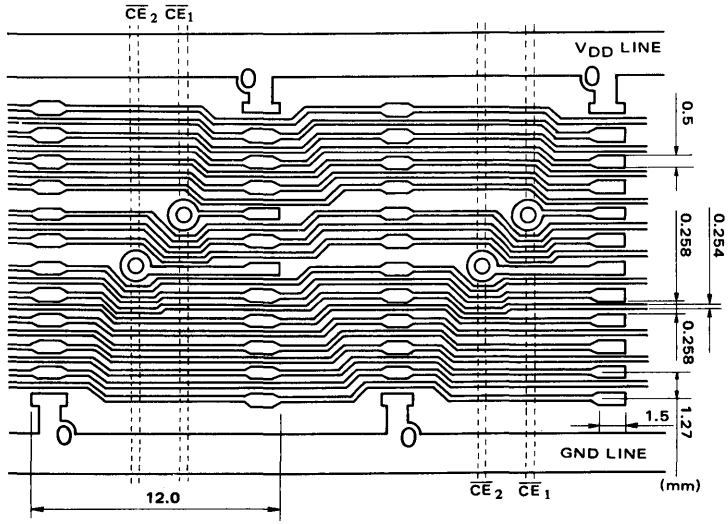
2. Comparison in occupied space



3. Advantage of this package

Small dimensions
Capability of High Density Assembly
Capability of thin Assembly — Capability of Assembly on both side of PC board.

4. PC pattern layout example



2,048 WORD × 8 BIT CMOS STATIC RAM

TC5518CP-15/CPL-15/CP-20/CPL-20
TC5518CF-15/CFL-15/CF-20/CFL-20

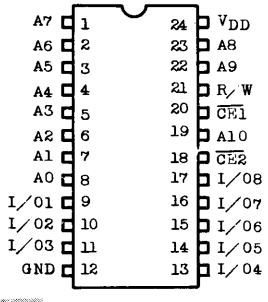
DESCRIPTION

The TC5518CP/CF is a 16384-bit high speed and low power fully static random access memory organized as 2048 words by a 8 bits using CMOS technology, and operates from a single 5 volt supply. The TC5518CP/CF has two chip enable inputs, $\overline{CE_1}$ and $\overline{CE_2}$, which are used for device selection and can be used in order to achieve minimum standby current mode easily for battery back up. Also the high speed and low power characteristics which maximum access time is 150ns, 200ns and maximum operating current is 5mA/MHz are achieved. Thus the TC5518CP/CF is most suitable for use in low power applications where battery operation or battery back up for nonvolatility are required. Furthermore the TC5518CPL/CFL guaranteed a standby current epual to or less then 1μA at 60°C ambient temperature avaitble. And the TC5518CP is pin compatible with 2716 type EPROM. This means that the TC5518CP and EPROM can be interchanged in the same socket and the flexibility in the definition of the quantity of RAM versus EPROM allows the wide application in microcomputer system.

FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current
  0.2μA(Max.) at Ta=25°C, 1.0μA(Max.) at Ta=60°C } TC5518CPL-15/CPL-20 CFL-15/CFL-20
  1.0μA(Max.) at Ta=25°C, 5.0μA(Max.) at Ta=60°C } TC5518CP-15/CP-20 CF-15/CF-20
- Single 5V Power Supply : 5V±10%
- Data Retention Supply Voltage : 2.0~5.5V
- Fully Static Operation
- Fast Access Time
  t_{ACC}=150ns(Max,) : TC5518CP-15/CPL-15 CF-15/CFL-15
  t_{ACC}=200ns(Max,) : TC5518CP-20/CPL-20 CF-20/CFL-20
- Two Chip Enables ($\overline{CE_1}$, $\overline{CE_2}$) for Simple Memory Expansion and Battery Back Up
- On-Chip Address Transition Detector
- All Inputs and Outputs Directly TTL Compatible
- Three State Outputs
- Package ; Plastic DIP (600 mil) : TC5518CP-15/CPL-15 CP-20/CPL-20
  Plastic FP : TC5518CF-15/CFL-15 CF-20/CFL-20

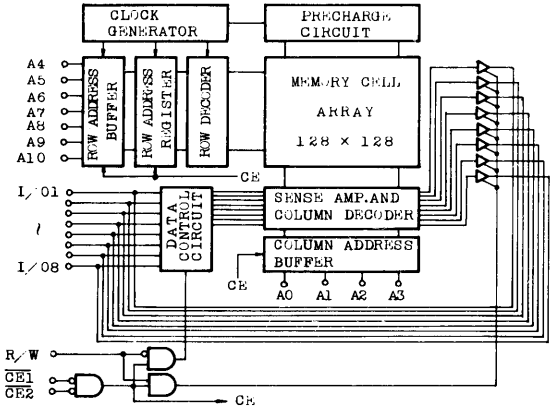
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{10}	Address Inputs
R/W	Read/Write Control Input
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enable Inputs
I/O_1 I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE_2}$	$\overline{CE_1}$	R/W	A_0~A_{10}	I/O_1~I/O_8	POWER
Read	L	L	H	Stable	Data Out	I_{DDO}
Write	L	L	L	Stable	Data In	I_{DDO}
** Standby 1	*	H	*	*	High Impedance	I_{DDS}
** Standby 2	H	*	*	*	High Impedance	I_{DDS}

Note : * : H or L ** : Data Retention Mode

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{DD}	Power Supply Voltage	−0.3~7.0V
V_{IN}	Input Voltage	−0.3V~V_{DD}+0.3V
$V_{I/O}$	Input/Output Voltage	−0.3V~V_{DD}+0.3V
P_D	Power Dissipation(Ta=85°C)	0.8W(0.45W)*
T_{STG}	Storage Temperature	−55°C~150°C
T_{OPR}	Operating Temperature	−30°C~85°C
T_{SOLDER}	Soldering Temperature·Time	260°C·10sec.

*Plastic FP=0.45W

RECOMMENDED D. C. OPERATING CONDITIONS (Ta=−30~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Voltage	2.0	—	5.5	V

D. C. CHARACTERISTICS (Ta=30~85°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS			TC5518CP-15/CF-15 MIN.	TC5518CP-15/CF-15 MAX.	TC5518CP-20/CF-20 MIN.	TC5518CP-20/CF-20 MAX.	UNIT
I_{IL}	Input Leakage Current	$0 \leqq V_{IN} \leqq V_{DD}$			—	±1.0	—	±1.0	μA
I_{LO}	I/O Leakage Current	$\overline{CE_2}$=V_{IH}, $OV \leqq V_{I/O} \leqq V_{DD}$			—	±5.0		±5.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			−1.0	—	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			2.0	—	2.0	—	mA
I_{DDS1}	Standby Current	$\overline{CE_2}$=2.2V or $\overline{CE_1}$=2.2V			—	3.0	—	3.0	mA
I_{DDS2}		$\overline{CE_2}$=V_{DD}−0.5V or $\overline{CE_1}$=V_{DD}−0.5V V_{DD}=2~5.5V	TC5518CPL/CFL	Ta=25°C	—	0.2	—	0.2	μA
				Ta=60°C	—	1.0	—	1.0	
			TC5518CP/CF	Ta=25°C	—	1.0	—	1.0	
				Ta=60°C	—	5.0	—	5.0	
				Ta=85°C	—	30	—	30	
I_{DDO1}	Operating Current	t_{cycle}=Mini cycle, $\overline{CE_1}$=$\overline{CE_2}$=OV, I_{OUT}=0mA		V_{IN}=V_{IH}/V_{IL}	—	45		30	mA
I_{DDO2}				V_{IN}=V_{DD}/GND	—	40		25	
I_{DDO3}		t_{cycle}=1μs, $\overline{CE_1}$= $\overline{CE_2}$=OV, I_{OUT}=0mA		V_{IN}=V_{IH}/V_{IL}	—	10	—	10	
I_{DDO4}				V_{IN}=V_{DD}/GND	—	5	—	5	

Note : Typical values are at Ta=25°C, V_{DD}=5V.

CAPACITANCE

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	—	5	10	pF
C_{OUT}	Input/Output Capacitance	—	5	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($Ta = -30 \sim 85°C$, $V_{DD}5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15		TC5518CP-20/CPL-20 TC5518CF-20/CFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	—	200	—	ns
t_{ACC}	Address Time	—	150	—	200	
t_{CO1}	$\overline{CE_1}$ to Output Valid	—	150	—	200	
t_{CO2}	$\overline{CE_2}$ to Output Valid	—	150	—	200	
t_{COE}	$\overline{CE_1}$ or $\overline{CE_2}$ to Output Active	10	—	10	—	
t_{OD}	Output High-Z Deselection	—	50	—	60	
t_{OH}	Output Hold from Address Change	15	—	20	—	

SYMBOL	PARAMETER	TC5518CP-15/CPL-15 TC5518CF-15/CFL-15		TC5518CP-20/CPL-20 TC5518CF-20/CFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	150	—	200	—	ns
t_{WP}	Write Pulse Width	120	—	150	—	
t_{AW}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	Output High-Z from R/W	—	50	—	60	
t_{OEW}	Output Active from R/W	10	—	10	—	
t_{DS}	Data Set up Time	60	—	80	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate

Input Pulse Levels : 0.6V, 2.4V

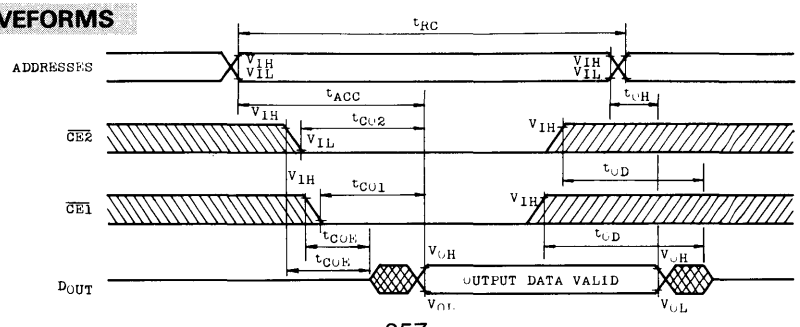
Timing Measurement Reference Levels

Input : 0.8V and 2.2V

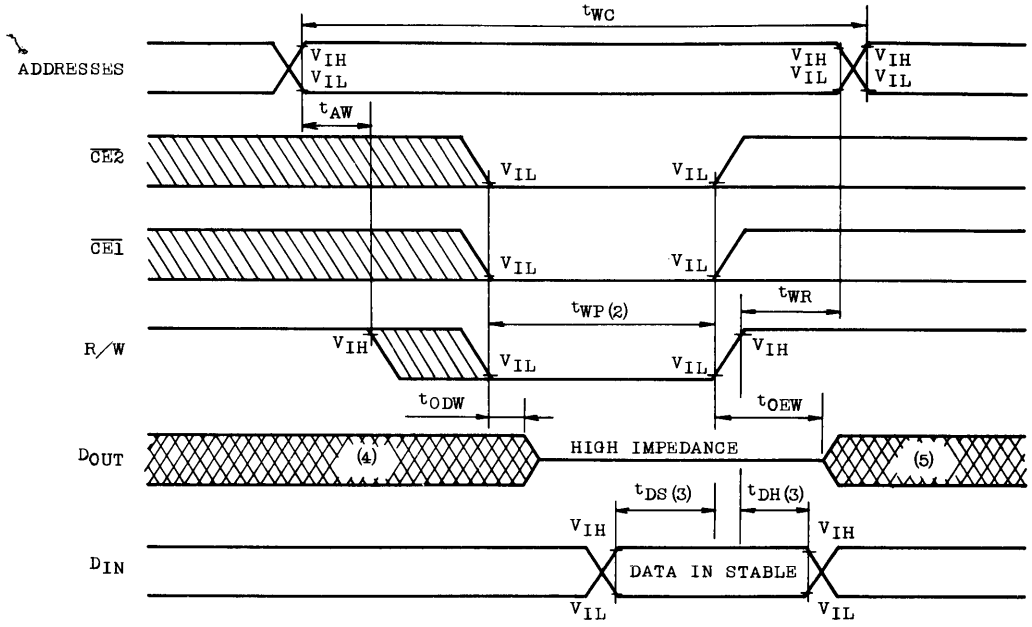
Output : 0.8V and 2.2V

Input Pulse Rise and Fall Times : 10ns

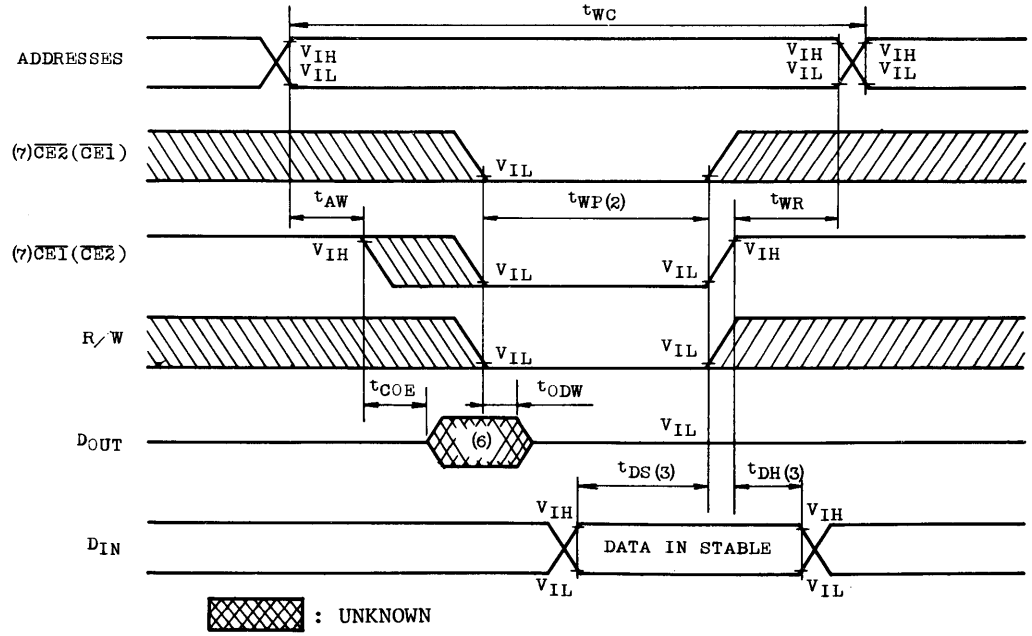
TIMING WAVEFORMS



- Write Cycle 1 (2)



- Write Cycle 2 (2)



Note :

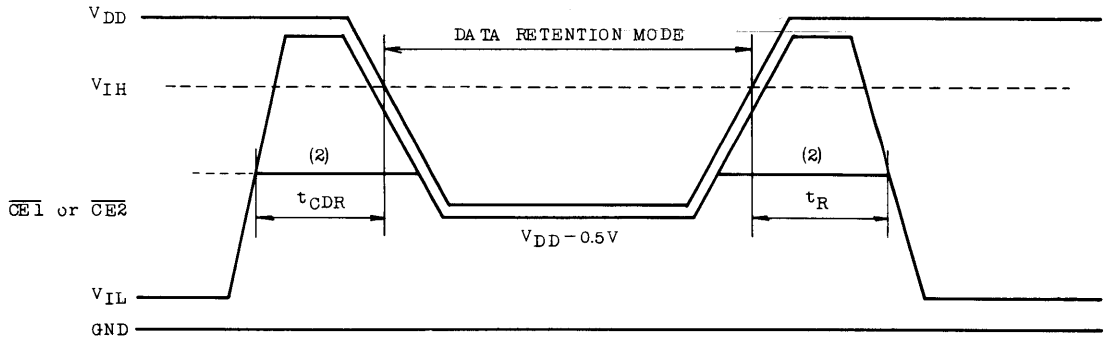
1. R/W is high for a read Cycle.
2. t_{WP} is specified as logical "AND" of $\overline{CE_1}$, $\overline{CE_2}$ and R/W.
   t_{WP} is measured from the latter of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going low to the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going high.
3. t_{DH}, t_{DS} are measured from the earlier of $\overline{CE_1}$, $\overline{CE_2}$ or R/W going high.
4. If the $\overline{CE_1}$ or $\overline{CE_2}$ low transition occurs simultaneously or latter from the R/W low transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
5. If the $\overline{CE_1}$ or $\overline{CE_2}$ high transition occurs prior to or simultaneously with the R/W high transition in a Write Cycle 1, the output buffers remain in a high impedance state in this period.
6. If the R/W is low or the R/W low transition occurs prior to or simultaneously with the $\overline{CE_1}$ or $\overline{CE_2}$ low transition, the output buffers remain in a high impedance state in this peried.
7. A write occurs during the overlap of a low $\overline{CE_1}$, low $\overline{CE_2}$ and low R/W.
   In write cycle 2, write is controlled by either $\overline{CE_1}$ or $\overline{CE_2}$.

DATA RETENTION CHARACTERISTICS (Ta = −30~85°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Power Supply Voltage			2.0	—	5.5	V
I_{DDS2}	Standby Current	TC5518CPL/CFL	Ta=25°C	—	0.005	0.2	μA
			Ta=60°C	—	—	1.0	
		TC5518CP/CF	Ta=25°C	—	0.05	1.0	
			Ta=60°C	—	—	5.0	
			Ta=85°C	—	—	30	
t_{CDR}	From Chip Deselection to Data Retention Mode			0	—	—	μs
t_R	Recovery Time			t_{RC}(1)	—	—	μs

Note :

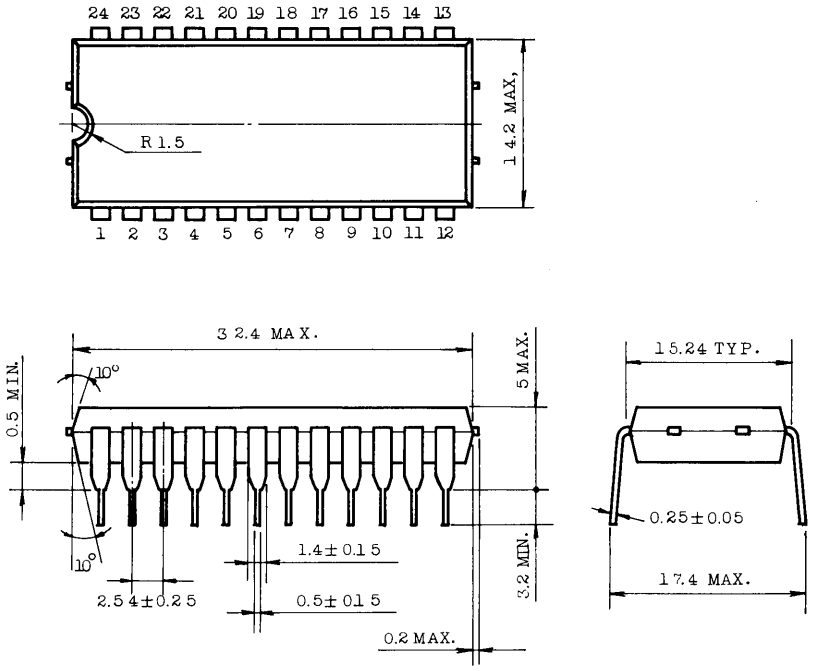
1. t_{RC} : Read Cycle Time



2. If the V_{IH} level of $\overline{CE_2}$ ($\overline{CE_1}$) is 2.2V, during the period that the V_{DD} voltage is going down from 4.5V to 2.7V, I_{DDS1} current flows.

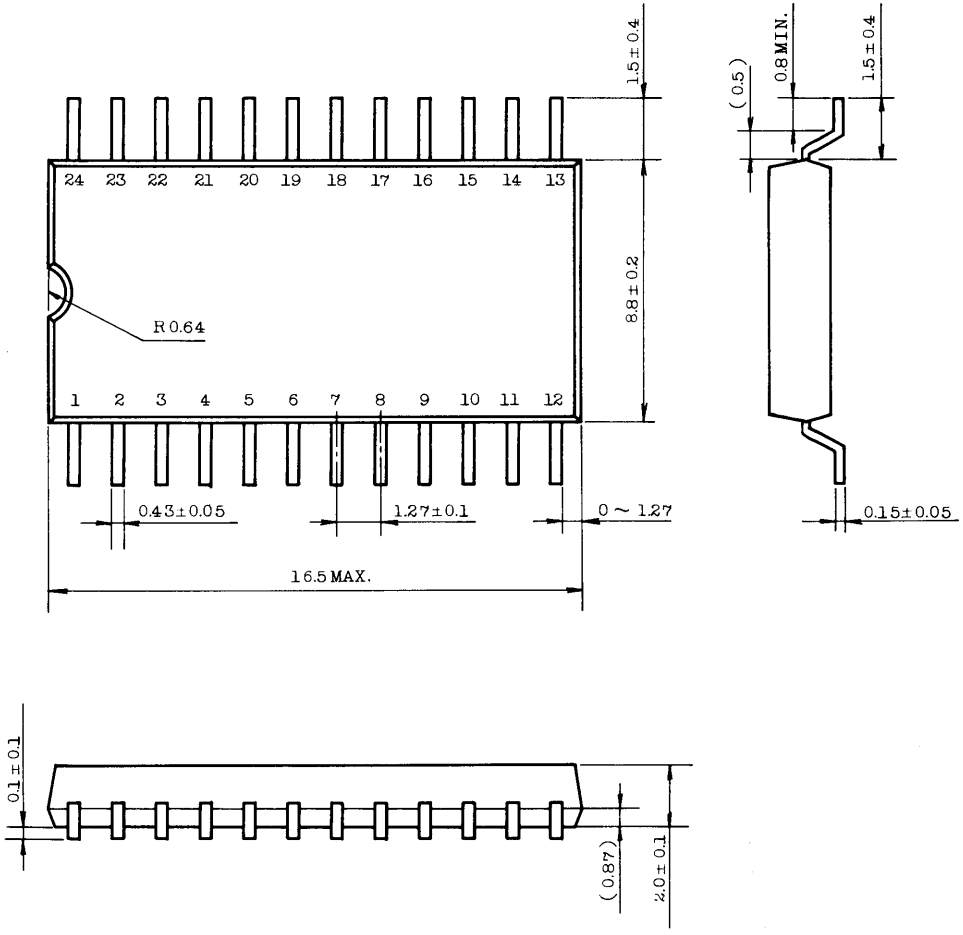
OUTLINE DRAWINGS

- Plastic DIP



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.
All dimensions are in millimeters.

● Plastic FP



Note : Each lead pitch is 1.27mm.
All leads are located within 0.1mm of their true longitudinal position with respect to No.1 and No.24 leads.

PACKGE INFORMATION FOR FLAT PACKAGE

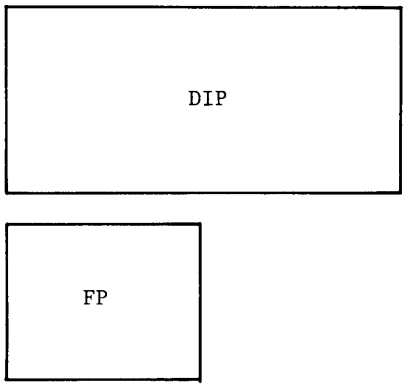
This new flat package is a very small and this compared with conventional standard dual-in-line package. Differences as follows.

1. Difference in dimension between flat and standard package.

Unit : mm

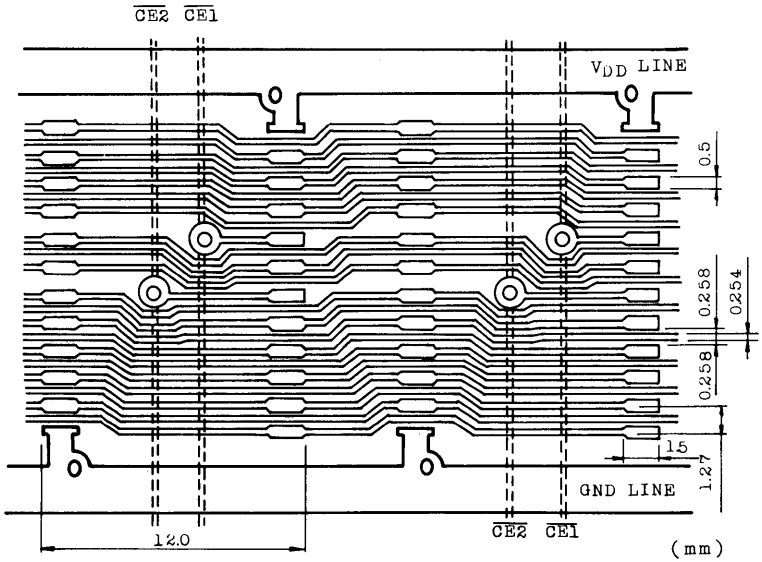
	Flat pacpage	Standard package
Length	16.5	32.4
Width	9.0	14.2
Lead Pitch	1.27	2.54
Thickness	2.1	5

2, Comparison in occupied space



3. Advantage of this package
   Small dimensions
   Capability of High Density Assembly
   Capability of thin Assembly ——
   Capability of Assembly on both side of PC board.

4. PC pattern layout example



Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE MOS

TC5563APL-10, TC5563APL-12
TC5563APL-15

DESCRIPTION

The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.
When CE_2 is a logical low or $\overline{CE}_1$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5563APL has three control inputs. Two chip enables ($\overline{CE}_1$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}_1$) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.
The TC5563APL is offered in dual-in-line 28 pin 0.3 inch width plastic package.

FEATURES

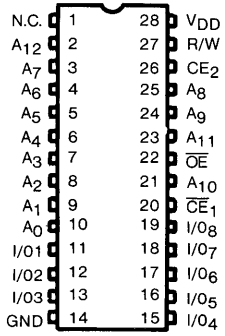
- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current: 100μA (Max.) Ta=70°C
- Access Time
  TC5563APL-10 : 100ns (Max.)
  TC5563APL-12 : 120ns (Max.)
  TC5563APL-15 : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features: CE_2, $\overline{CE}_1$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- 0.3 inch width Plastic Package
- TC5563APL Family (Package Type)

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package (SOP)	*TC5565AFL

*) See TC5565APL/AFL Technical Data

PIN CONNECTION (TOP VIEW)

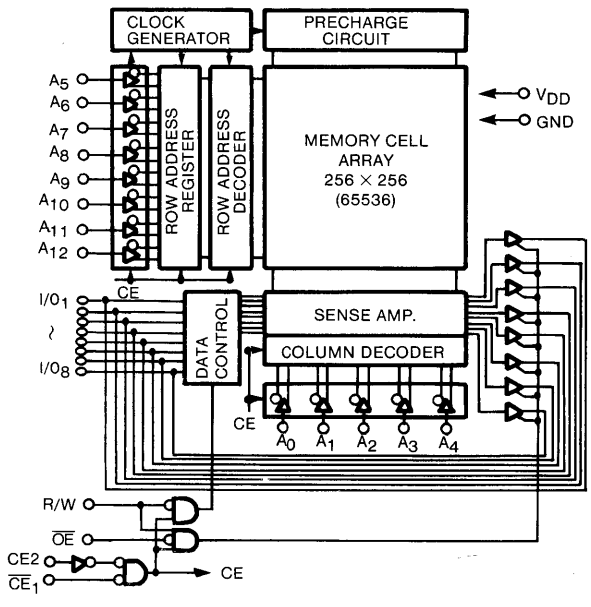
TC5563APL



PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}_1$ CE_2	Chip Enable Input
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	*−0.3~7.0	V
$V_{I/O}$	Input and Output Voltage	$-0.5 \sim V_{DD}+0.5$	V
P_D	Power Dissipation	0.8	W
T_{solder}	Soldering Temperature	260 · 10	°C · sec
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	0~70	°C

* −3.0V at pulse width 50ns MAX.

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	−0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}			-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			−1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}_1$=V_{IH} or CE_2=V_{IL} or R/$\overline{W}$=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0~V_{DD}			-	-	±1.0	μA
I_{DD01}	Operating Current	V_{DD}=5.5V $\overline{CE}_1$=V_{IL} CE_2=V_{IH} Other input=V_{IH}/V_{IL}	t_{cycle}=1.0μs		-	-	10	mA
			TC5563APL-10	t_{cycle}=100ns	-	-	45	mA
			TC5563APL-12	t_{cycle}=120ns	-	-	40	mA
			TC5563APL-15	t_{cycle}=150ns	-	-	35	mA
I_{DD02}		V_{DD}=5.5V $\overline{CE}_1$=0.2V CE_2=V_{DD}−0.2V Other input=V_{DD}−0.2V/0.2V	t_{cycle}=1.0μs		-	-	5	mA
			TC5563APL-10	t_{cycle}=100ns	-	-	40	mA
			TC5563APL-12	t_{cycle}=120ns	-	-	35	mA
			TC5563APL-15	t_{cycle}=150ns	-	-	30	mA
I_{DDS1}	Standby Current	$\overline{CE}_1$=V_{IH} or CE_2=V_{IL}			-	-	3	mA
*I_{DDS2}		$\overline{CE}_1$=V_{DD}−0.2V or CE_2=0.2V		V_{DD}=5.5V	-	2	100	μA
				V_{DD}=3.0V	-	1	50	μA

Note * : In standby mode with $\overline{CE}_1 \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geqq V_{DD}-0.2V$ or $CE_2 \leqq 0.2V$.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	-	-	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	-	-	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	ns
t_{CO1}	$\overline{CE}_1$ Access Time	-	100	-	120	-	150	ns
t_{CO2}	CE_2 Access Time	-	100	-	120	-	150	ns
t_{OE}	Output Enable to Output Valid	-	50	-	60	-	70	ns
t_{COE}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in Low-Z	10	-	10	-	15	-	ns
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	ns
t_{OD}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in High-Z	-	35	-	40	-	50	ns
t_{ODO}	Output Enable to Output in High-Z	-	35	-	40	-	50	ns
t_{OH}	Output Data Hold Time	20	-	20	-	20	-	ns

Write Cycle

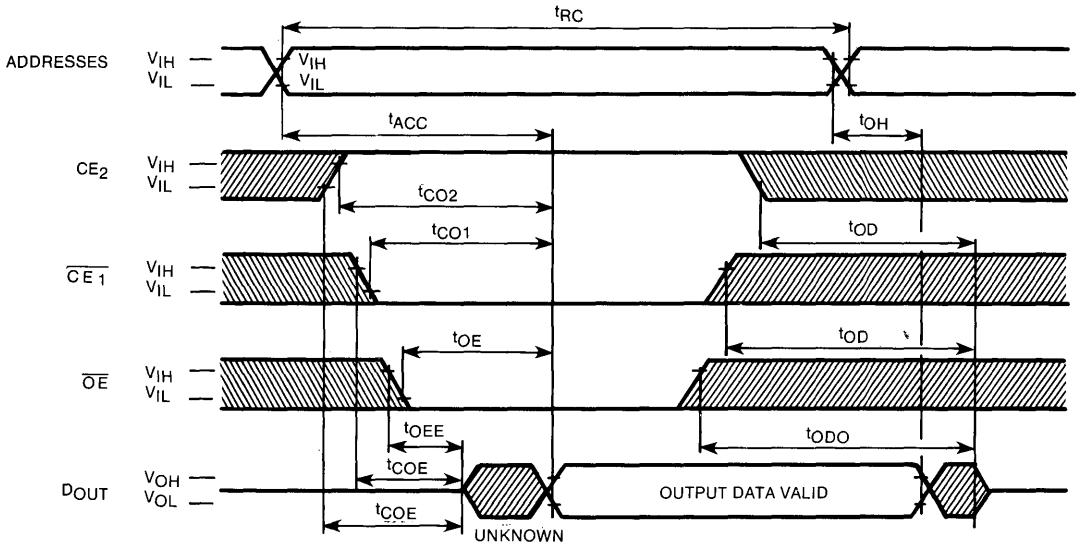
SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	90	-	ns
t_{CW}	Chip Selection to End of Write	80	-	85	-	100	-	ns
t_{AS}	Address Set Up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{ODW}	R/W to Output High-Z	-	35	-	40	-	50	ns
t_{OEW}	R/W to Output Low-Z	5	-	5	-	10	-	ns
t_{DS}	Data Set up Time	40	-	50	-	60	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns

A.C. TEST CONDITION

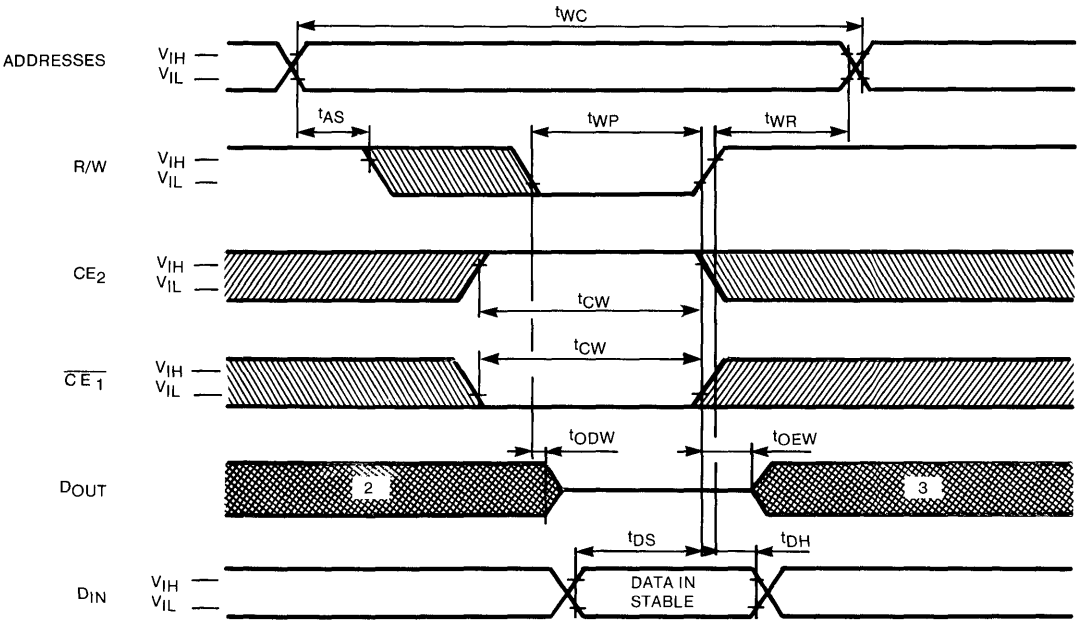
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V_{IN}	: 0.8V, 2.2V
Reference Level	V_{OUT}	: 0.8V, 2.2V
t_r, t_f		: 5ns

TIMING WAVEFORMS

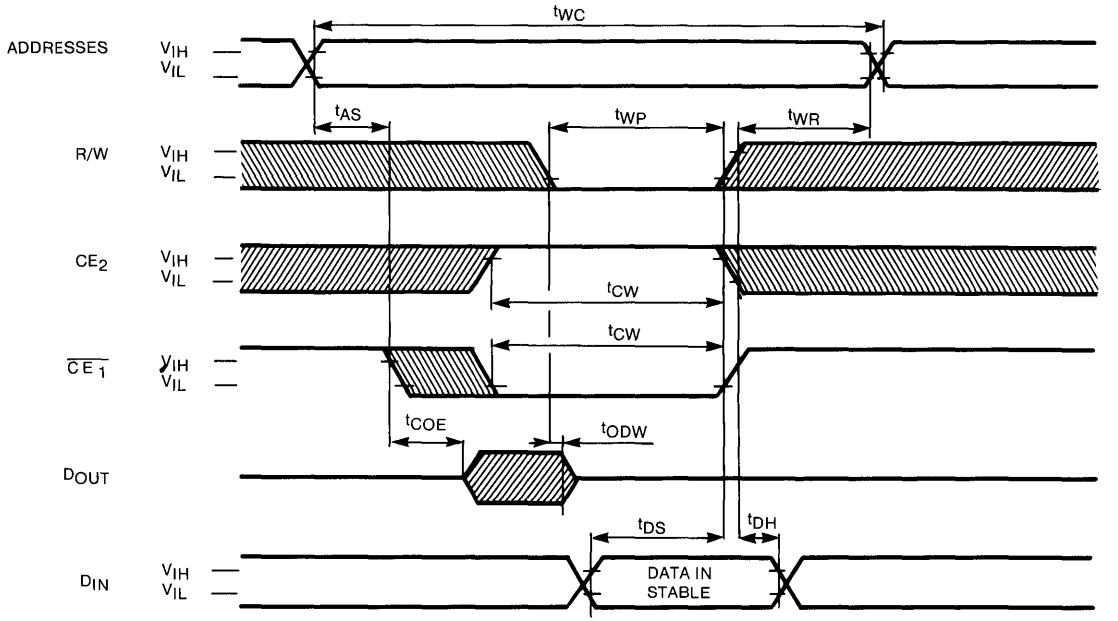
READ CYCLE (1)



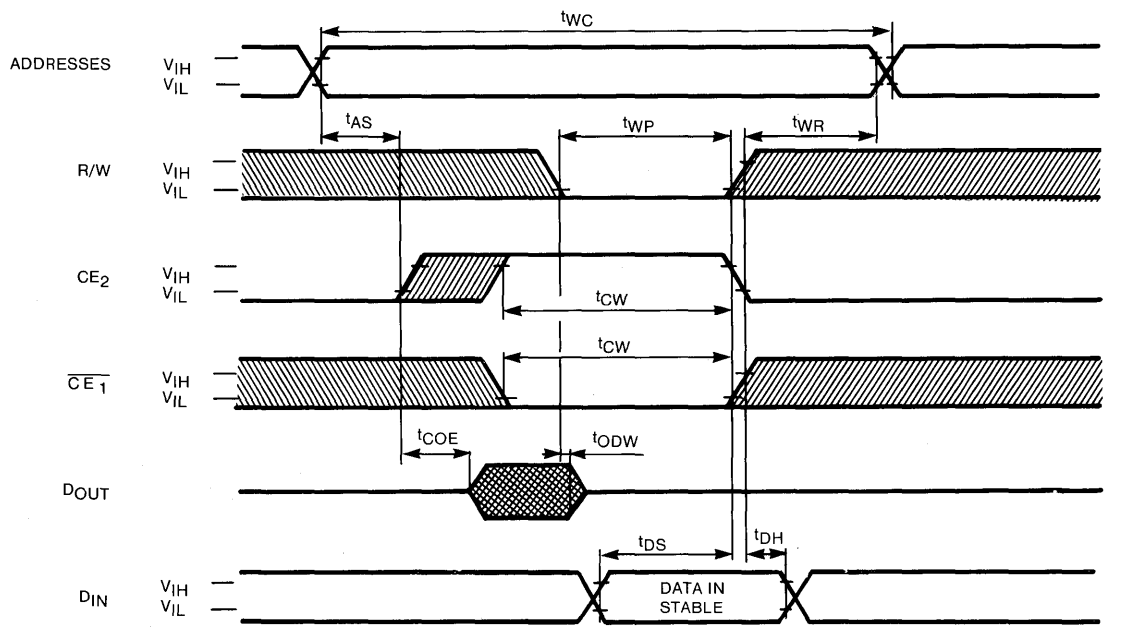
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE_1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}_1$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}_1$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in high impedance state.

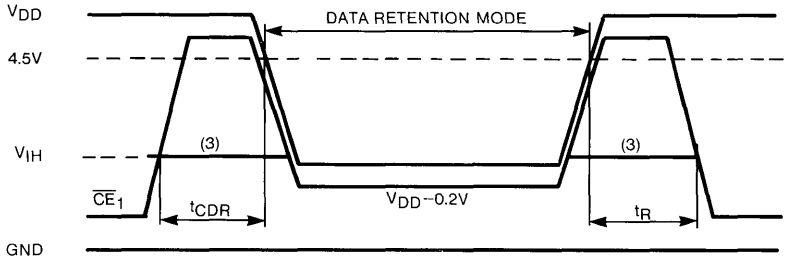
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION (Ta=0~70°C)

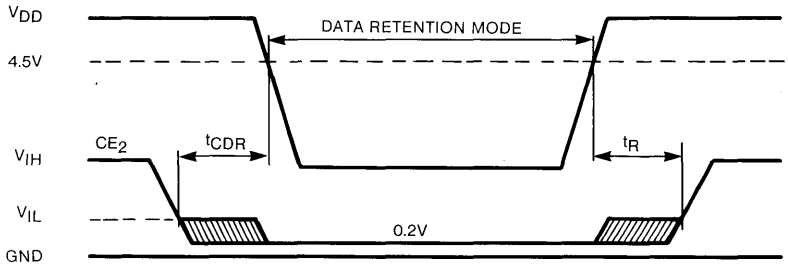
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	-	-	50	μA
		V_{DD}=5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		$t_{RC(1)}$	-	-	μs

Note (1) : Read cycle time.

$\overline{CE}_1$ Controlled Data Retention Mode (2)



CE_2 Controlled Data Retention Mode (4)



Note 2 : In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD}-0.2V$.

3 : If the V_{IH} of $\overline{CE}_1$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

4 : In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5563APL is an synchronous RAM using address activated circuit technology. Thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.
This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

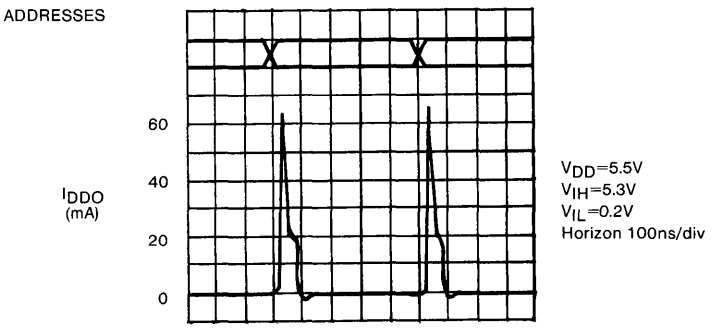
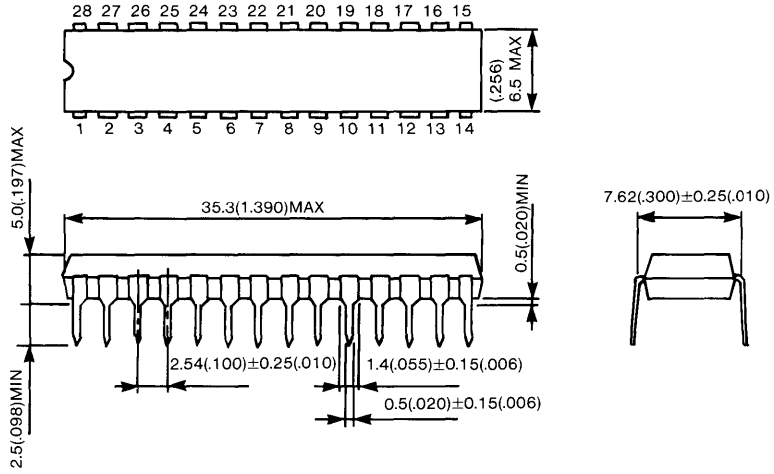


Fig. TYPICAL CURRENT WAVEFORMS

DIP 28 PIN OUTLINE DRAWING (3D28A-P) **Unit in mm (inches)**



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

TC5564PL-15
TC5564PL-20

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

DESCRIPTION

TC5564PL is 65536 bits static random access memory organized as 8192 words by 8 bits using CMOS technology, and operates with a single 5V power supply.

Advanced circuit techniques provides low power feafure with a maximum operating current of 5mA/MHz. Operation current depends on cycle time.

TC5564PL has three control inputs. Two chip enables($\overline{CE_1}$, CE_2) allow for device selection and data retention control. Output enable($\overline{OE}$) input provides fast memory access. When device is placed in standby mode with chip off state, standby current is typically 0.01μA. So the TC5564PL is suitable for use in various microprocessor application systems where low power and battery back up are required. Ultra low standby power allow not only battery but capacitance backup.

Pin assignment of TC5564PL is pin compatible with the 64K bits EPROM(TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems,

TC5564PL is offered in a standard dual-in-line 28pin plastic package, 0.6 inch width.

FEATURES

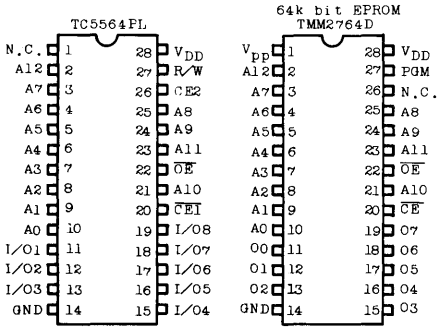
- Standby Current
  0.2μA(MAX.) at Ta=25°C
  1.0μA(MAX.) at Ta=60°C
- Low Power Dissipation
  27.5mW/MHz(MAX.) Operating
- 5V Single Power Supply
- 8,192 Word×8Bit
- Fully Static Operation
- Data Retention Voltage : 2.0~5.5V

- Access Time

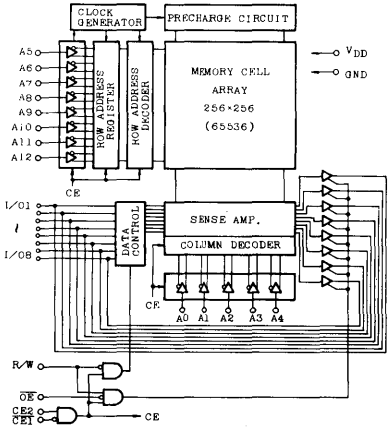
	TC5564PL-15	TC5564PL-20
Address Access Time (MAX.)	150ns	200ns
$\overline{CE_1}$ Access Time (MAX.)	150ns	200ns
CE_2 Access Time (MAX.)	150ns	200ns
Output Enable Time (MAX.)	70ns	100ns

- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 Pin DIP
- Pin compatible with 2764 type EPROM

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

OPERATING MODE

Operation Mode	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	I/O_1~I/O_8	Power
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	*	*	H	*	High-Z	I_{DDO}
Standby	H	*	*	*	"	I_{DDS}
	*	L	*	*	"	I_{DDS}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3 ~7.0*	V
V_{IN}	Input Voltage	−0.3**~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature	260·10	°C·Sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	−30~85	°C

* 8.5V at Pulse width 100ns
** −3.0V at Pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* −3.0V at Pulse width 50ns

D.C. and OPERATING CHARACTERISTICS

($Ta=-30\sim85°C$, $V_{DD}=5V\pm10\%$ Unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$			—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$			−1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$			4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$ or R/W=V_{IL}, or $\overline{OE}=V_{IH}$ $V_{OUT}=0\sim V_{DD}$			—	—	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE_1}=V_{IL}$ and $CE_2=V_{IH}$ Other Input=V_{IH}/V_{IL} I_{OUT}=0mA	$t_{cycle}=1\mu s$		—	—	10	mA
			MIN CYCLE	TC5564PL-15	—	—	45	
				TC5564PL-20	—	—	40	
I_{DDO2}	Operating Current	$\overline{CE_1}=0.2V$ and $CE_2=V_{DD}-0.2V$ Other Input =$V_{DD}-0.2V/0.2V$ I_{OUT}=0mA	$t_{cycle}=1\mu s$		—	—	5	mA
			MIN CYCLE	TC5564PL-15	—	—	40	
				TC5564PL-20	—	—	35	
I_{DDS1}	Standby Current	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$			—	—	2	mA
I_{DDS2}	Standby Current	$\overline{CE_1}=V_{DD}-0.2V$ or $CE_2=0.2V$ $V_{DD}=2.0\sim5.5V$		Ta=25°C	—	0.01	0.2	μA
				Ta=60°C	—	—	1.0	

Note : In standby mode with $\overline{CE_1}\geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2\geqq V_{DD}-0.2V$ or $CE_2\leqq 0.2V$.

CAPACITANCE

($Ta=25°C$, $f=1MHz$)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($Ta = -30 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

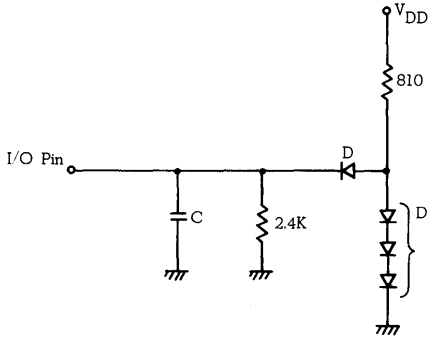
SYMBOL	PARAMETER	TC5564PL-15		TC5564PL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	—	200	—	ns
t_{ACC}	Address Access Time	—	150	—	200	
t_{CO1}	$\overline{CE_1}$ Access Time	—	150	—	200	
t_{CO2}	CE_2 Access Time	—	150	—	200	
t_{OE}	Output Enable to Output in Valid	—	70	—	100	
t_{COE}	Chip Enable ($\overline{CE_1}$), CE_2 to Output in Low-Z	10	—	10	—	
t_{OEE}	Output Enable to Output Low-Z	5	—	5	—	
t_{OD}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in High-Z	—	70	—	100	
t_{ODO}	Output Enable to Output High-Z	—	60	—	80	
t_{OH}	Output Data Hold Time	20	—	20	—	

Write Cycle

SYMBOL	PARAMETER	TC5564PL-15		TC5564PL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	150	—	200	—	ns
t_{WP}	Write Pulse Width	100	—	150	—	
t_{CW}	Chip Selection to End of Write	120	—	180	—	
t_{AW}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W to Output High-Z	—	70	—	100	
t_{OEW}	R/W to Output Low-Z	10	—	10	—	
t_{DS}	Data Set Up Time	70	—	80	—	
t_{DH}	Data Hold Time	0	—	0	—	

A.C. TEST CONDITIONS

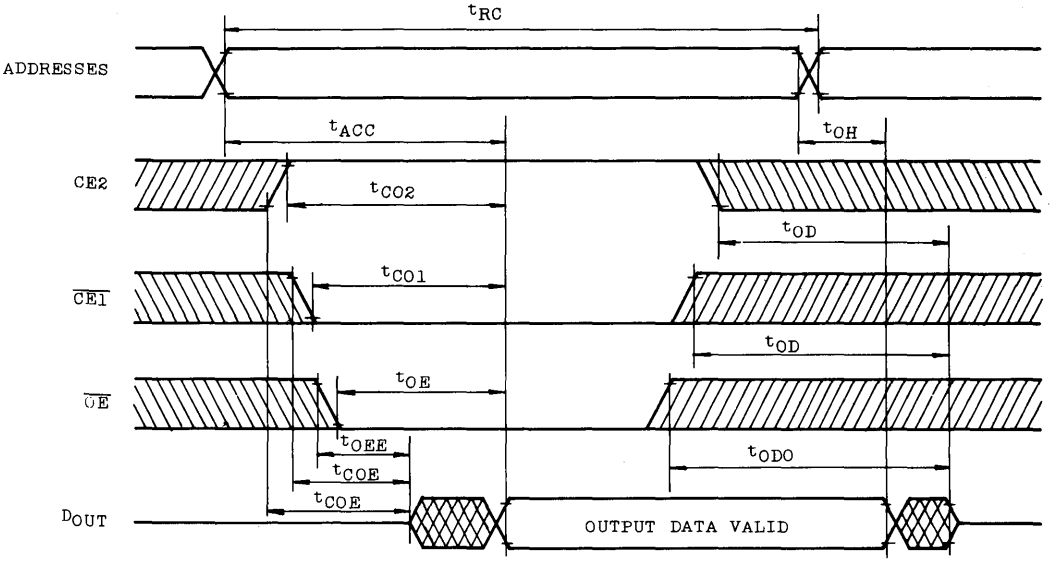
Input Pulse Levels : 2.4V/0.6V
Timing Measurement Reference levels : Input ; 2.2V/0.8V
: Output; 2.2V/0.8V
Input Pulse Rise and Fall Times : 5ns
Output Load : See Fig. 1



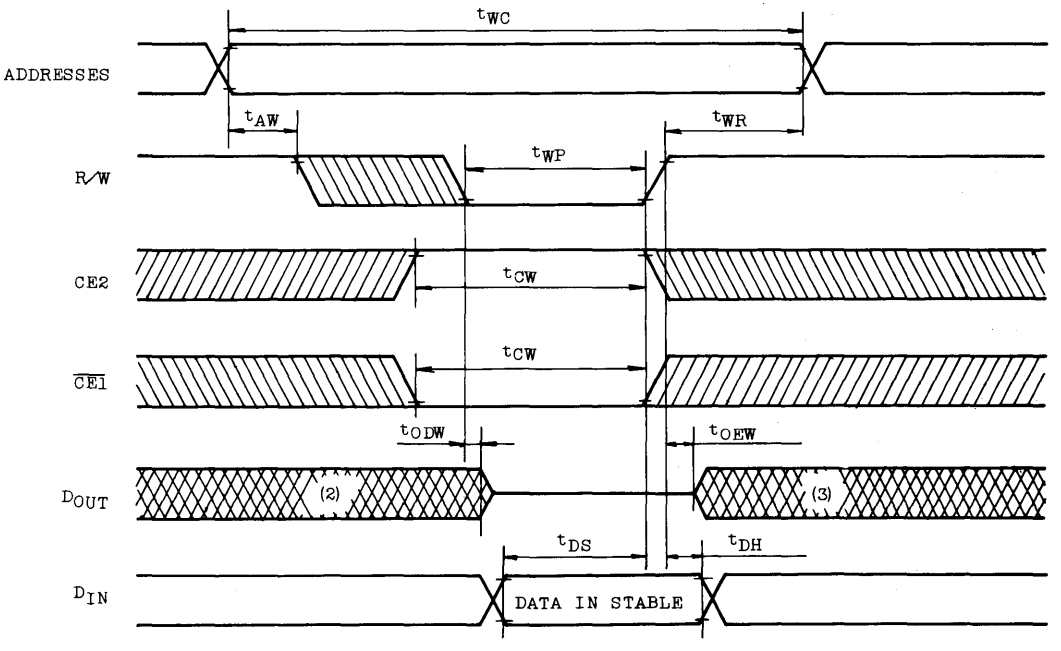
C : 100pF (Including Jig)
D : 1S1588 or Equivarent
Fig. 1 Output Load

TIMING WAVEFORMS

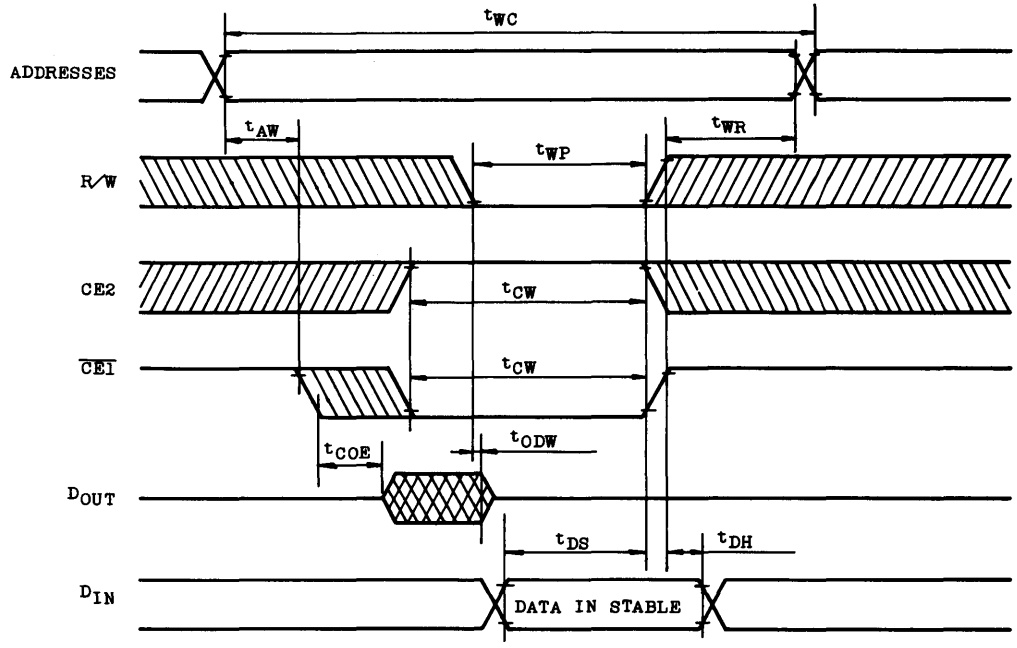
- READ CYCLE (1)



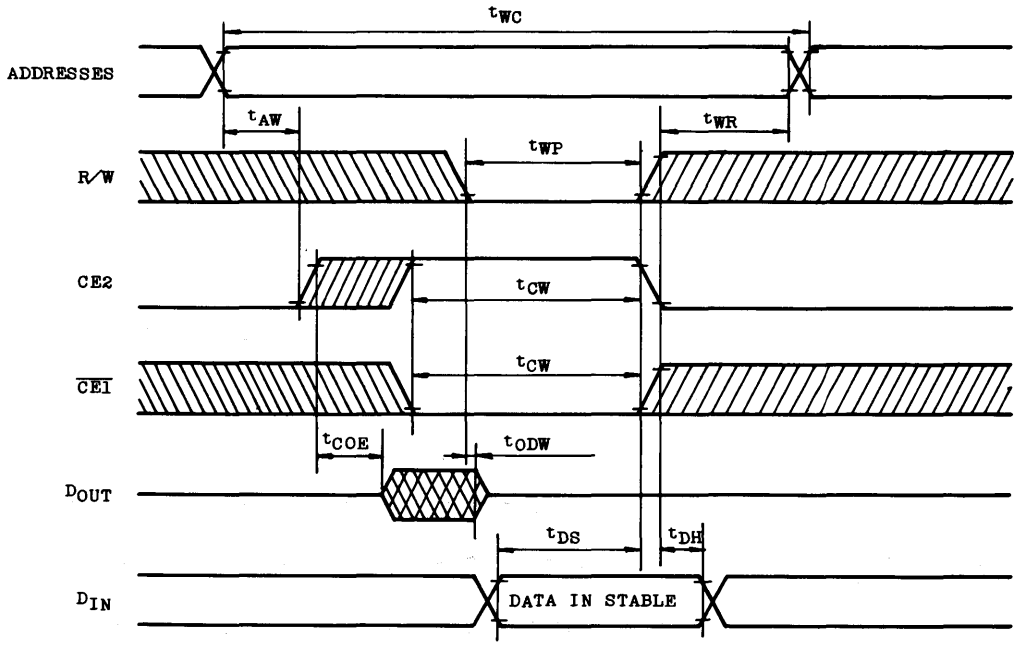
- WRITE CYCLE 1 (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



- WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note :

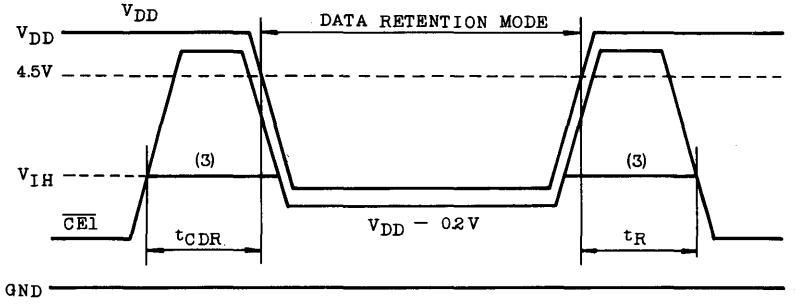
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE_1}$ Low transition or CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = −30~85°C)

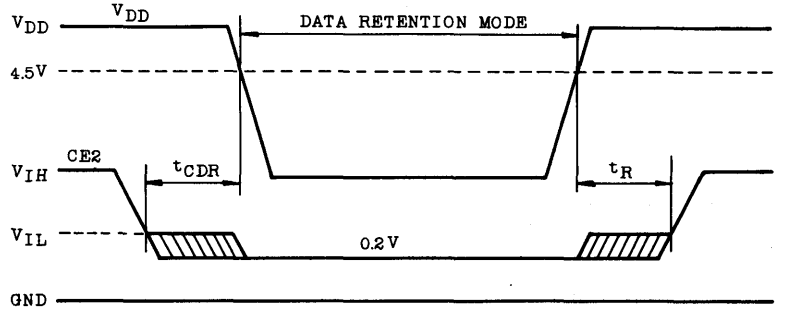
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Current	Ta=25°C	—	0.01	0.2	μA
		Ta=60°C	—	—	1.0	
t_{CDR}	Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}(1)	—	—	μs

Note (1) : Read cycle time.

- $\overline{CE_1}$ Controlled Data Retention Mode (2)



- CE_2 Controlled Data Retention Mode (4)



Note :

2. In $\overline{CE_1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD}-0.2V$.
3. If the V_{IH} of $\overline{CE_1}$ is 2.2V in operation, during the period that the V_{DD} Voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.
4. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5564PL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only row address change, as is shown in the following figure.

This peak current may induce the noise on V_{DD}/GND line. Thus the use of about 0.1μF decoupling capacitor every device is recommended to eliminate such noise.

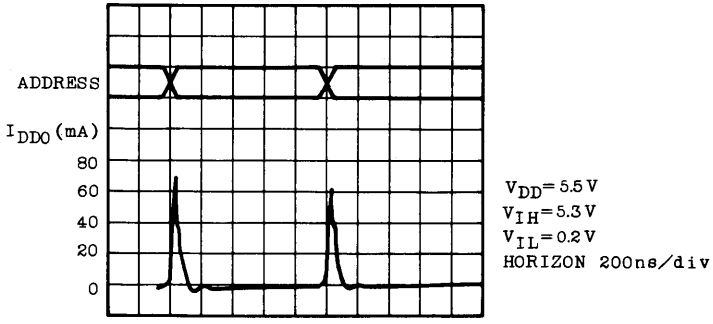
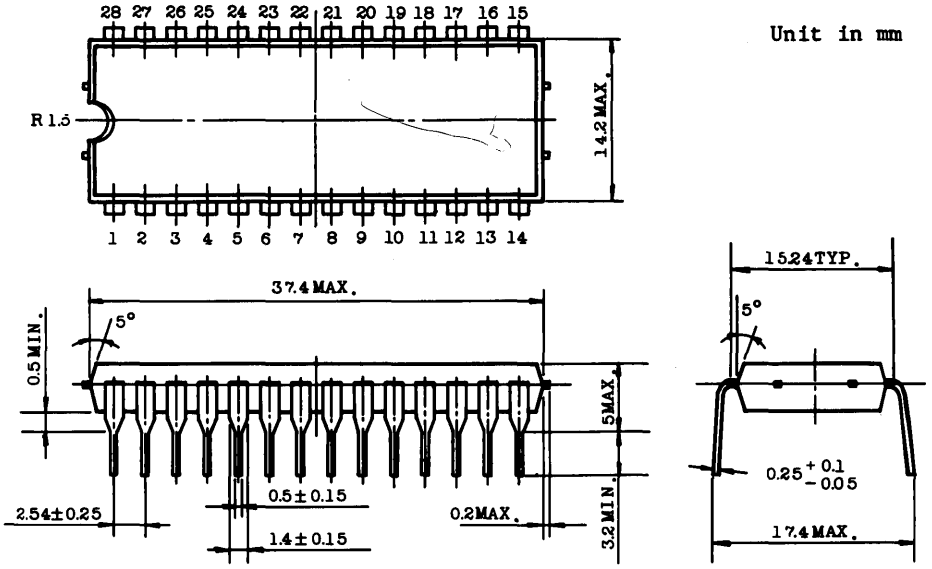


Fig. TYPICAL CURRENT WAVEFORMS

OUTLINE DRAWINGS

Unit in mm



NOTES : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS
PRELIMINARY

TC5564APL-12, TC5564APL-15
TC5564AFL-12, TC5564AFL-15

DESCRIPTION

TC5564APL is 65536 bits of static random access memory organized as 8192 words by 8 bits using CMOS technology, and operates with a single 5V power supply.

Advanced circuit techniques provides a low power feature, a maximum operating current of 5mA/MHz. Operational current depends on cycle time.

TC5564APL has three control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control. Output enable ($\overline{OE}$) input provides fast memory access. When device is placed in standby mode with chip off state, standby current is typically 0.01μA. So the TC5564APL is suitable for use in various microprocessor application systems where low power and battery back up are required. Ultra low standby power allow not only battery but capacitance backup.

Pin assignment of TC5564APL is pin-compatible with the 64K bits EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application system.

TC5564APL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

FEATURES

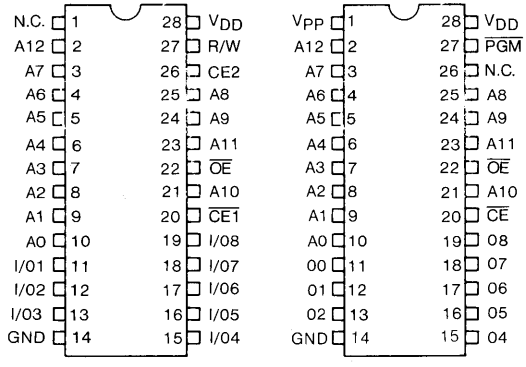
- Low Power Dissipation
  - 5mA/MHz (MAX.) — Operating
  - 0.2μA (MAX.) at Ta=25°C — Standby
  - 1.0μA (MAX.) at Ta=60°C — Standby
- 5V Single Power Supply
- Low Voltage Operation: V_{DD}=3V
  T_{CO}=1μs (MAX.) Ta=60°C
- Fully Static Operation
- Data Retention Voltage: 2.0~5.5V
- Plastic DIP and Plastic FP Package
- Pin Compatible with 2764 type EPROM

- Access Time

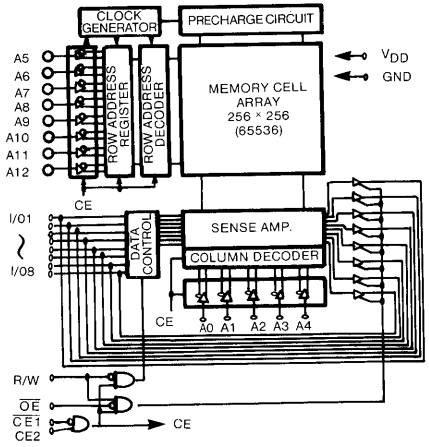
	TC5564APL-12 TC5564AFL-12	TC5564APL-15 TC5564AFL-15
Address Access Time (MAX.)	120ns	150ns
$\overline{CE1}$ Access Time (MAX.)	120ns	150ns
CE2 Access Time (MAX.)	120ns	150ns
Output Enable Time (MAX.)	60ns	70ns

- Directly TTL Compatible: All Inputs and Outputs
- Wide Teperature Operation: −40~85°C

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ~ A12	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Input
I/01 ~ I/08	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

OPERATING MODE

Operation Mode	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/01 ~ I/08	Power
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	
Output Deselect	*	*	H	*	High-Z	
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
*V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~V_{DD}	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0 (0.6)*	W
T_{solder}	Soldering Temperature	260 · 10	°C · sec
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	−40~85	°C

* 8.5V at 100ns
* −3V Pulse width 50ns

* SOP

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=−40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C. and OPERATING CHARACTERISTIC (Ta=−40~85°C, V_{DD}=5V±10% Unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{IN}	Input Leakage Current	V_{IN}=0~V_{DD}			-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			-1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			4.0	-	-	mA
V_{OH}	Output High Voltage	I_{OH}=−20μA			V_{DD}−0.1	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=20μA			-	-	0.1	V
I_{LO}	Output Leakage Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or R/W=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0~V_{DD}			-	-	±1.0	μA
I_{DD01}	Operating Current	$\overline{CE1}$=V_{IL} and CE2=V_{IH}, Other Input=V_{IH}/V_{IL}, I_{OUT}=0mA	t_{cycle}=1μs		-	-	10	mA
			MIN CYCLE	TC5564APL-12 TC5564AFL-12	-	-	45	
				TC5564APL-15 TC5564AFL-15	-	-	40	
I_{DD02}	Operating Current	$\overline{CE1}$=0.2V and CE2=V_{DD}−0.2V, Other Input=V_{DD}−0.2V/0.2V, I_{OUT}=0mA	t_{cycle}=1μs		-	-	5	mA
			MIN CYCLE	TC5564APL-12 TC5564AFL-12	-	-	40	
				TC5564APL-15 TC5564AFL-15	-	-	35	
I_{DDS1}	Standby Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL}			-	-	2	mA
I_{DDS2}	Standby Current	$\overline{CE1}$=V_{DD}−0.2V or CE2=0.2V, V_{DD}=2.0~5.5V	Ta=25°C		-	0.01	0.2	μA
			Ta=60°C		-	-	1.0	

Note: (1) In standby mode with CE1≧V_{DD}−0.2V, those specification limits are guaranteed under the condition of CE2 ≧V_{DD}−0.2V or CE2≦0.2V.

(2) All voltage is measured from GND

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

* This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=−40~85°C, V_{DD}=5V±10%)

READ CYLCE

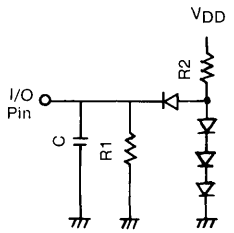
SYMBOL	PARAMETER	TC5564APL-12 TC5564AFL-12		TC5564APL-15 TC5564AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	120	-	150	-	ns
t_{ACC}	Address Access Time	-	120	-	150	
t_{CO1}	$\overline{CE1}$ Access Time	-	120	-	150	
t_{CO2}	CE2 Access Time	-	120	-	150	
t_{OE}	Output Enable to Output in Valid	-	60	-	70	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) Output in Low-Z	10	-	10	-	
t_{OEE}	Output Enable to Output Low-Z	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) Output in High-Z	-	60	-	70	
t_{ODO}	Output Enable to Output in High-Z	-	50	-	60	
t_{OH}	Output Data Hold Time	20	-	20	-	

WRITE CYCLE

SYMBOL	PARAMETER	TC5564APL-12 TC5564AFL-12		TC5564APL-15 TC5564AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	120	-	150	-	ns
t_{WP}	Write Pulse Width	80	-	100	-	
t_{CW}	Chip Selection to End of Write	100	-	120	-	
t_{AS}	Address Set Up Time	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{ODW}	R/W to Output High-Z	-	60	-	70	
t_{OEW}	R/W to Output Low-Z	10	-	10	-	
t_{DS}	Data Set Up Time	50	-	60	-	
t_{DH}	Data Hold Time	0	-	0	-	

AC TEST CONDITIONS

- Input Pulse Levels : 2.4V/0.6V
- Timing Measurement Reference Levels : 2.2V/0.8V
- Output Reference Levels : 2.2V/0.8V
- Input Pulse Rise and Fall Time : 5ns
- Output Load : See Fig. 1



R1 : 2.4kΩ
R2 : 810Ω
C : 100pF (Include Jig)
D : 1S1588 (or Equivaler

Fig. 1 Output Load

3V OPERATION SPECIFICATION

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=−10~60°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V_{IH}	Input High Voltage	$V_{DD}-0.2$	-	V_{DD}	V
V_{IL}	Input Low Voltage	0	-	0.2	V

D.C. AND OPERATING CHARACTERISTICS (Ta=−10~60°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IN}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$		-	-	1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE1}=V_{IH}$ or CE2=V_{IL} or R/W=V_{IL} or $\overline{OE}=V_{IH}$, $V_{OUT}=0\sim V_{DD}$		-	-	1.0	μA
I_{OH}	Output High Current	$V_{OH}=V_{DD}-0.2V$		-100	-	-	μA
I_{OL}	Output Low Current	$V_{OL}=0.2V$		100	-	-	μA
V_{OH}	Output High Voltage	$I_{OH}=-20\mu A$		$V_{DD}-0.1$	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=20\mu A$		-	-	0.1	V
I_{DDO}*	Operating Current	$\overline{CE1}=V_{IL}$ and CE2=V_{IH} Other input = $V_{DD}-0.2V/0.2V$ I_{OUT}=0mA, duty 100%	$t_{cycle}=1\mu s$	-	2.0	3.0	mA
			$t_{cycle}=10\mu s$	-	-	0.5	
I_{DDS}	Standby Current	$\overline{CE1}=V_{IL}$ and CE2=V_{IH} or CE2=V_{IL}	Ta=25°C	-	0.01	0.2	μA
			Ta=60°C	-	-	1.0	

· All voltage is measured from GND.

* I_{DDO} is slightly dependent on input pulse t_r, t_f. If a long t_r, t_f pulse is applied, there is some transient current at the input stage. These specifications are guaranteed with t_r, $t_f \leqq 20ns$.

3V OPERATE SPECIFICATION

A.C. CHARACTERISTICS (Ta=−10~60°C, V_{DD}=3V±10%)

READ CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t_{RC}	Read Cycle Time	1000	-	-	ns
t_{ACC}	Address Access Time	-	300	1000	
t_{CO1}	$\overline{CE1}$ Access Time	-	300	1000	
t_{CO2}	CE2 Access Time	-	300	1000	
t_{OE}	Output Enable to Output Valid	-	100	200	
t_{OH}	Output Data Hold Time	20	-	-	
t_{COE}	Chip Enable to Output in Low Z	10	-	-	
t_{OEE}	Output Enable to Output in Low Z	5	-	-	
t_{OD}	Chip Enable to Output in High Z	-	-	200	
t_{ODO}	Output Enable to Output in High Z	-	-	150	

WRITE CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t_{WC}	Write Cycle Time	1000	-	-	ns
t_{WP}	Write Pulse Width	500	-	-	
t_{CW}	Chip Selection to End of Write	800	-	-	
t_{AS}	Address Set Up Time	100	-	-	
t_{WR}	Write Recovery Time	100	-	-	
t_{DS}	Data Set Up Time	400	-	-	
t_{DH}	Data Hold Time	50	-	-	
t_{ODW}	R/W to Output High Z	-	-	200	
t_{OEW}	R/W to Output Low Z	10	-	-	

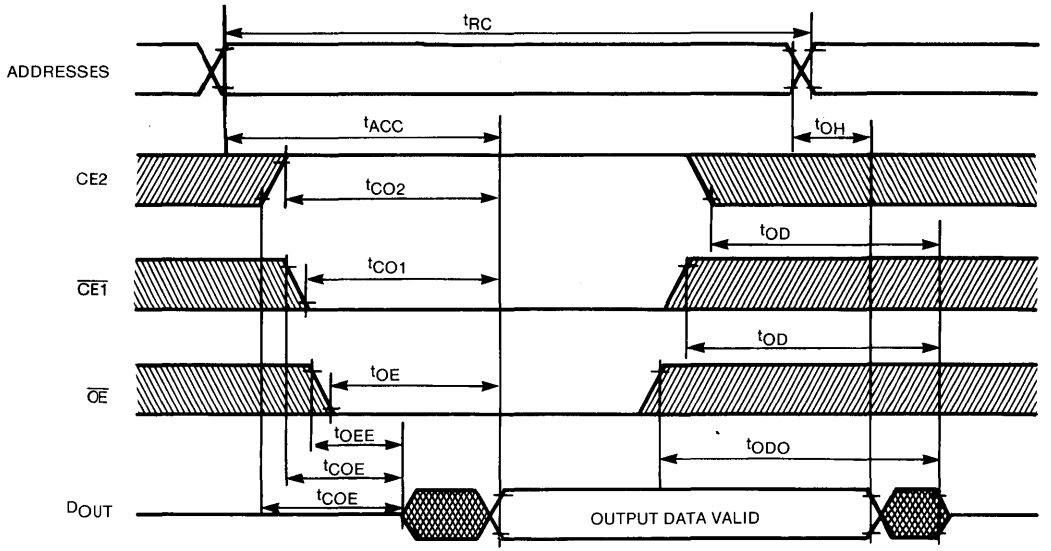
* Typ. condition is Ta=25°C, V_{DD}=3V

A.C. TEST CONDITIONS

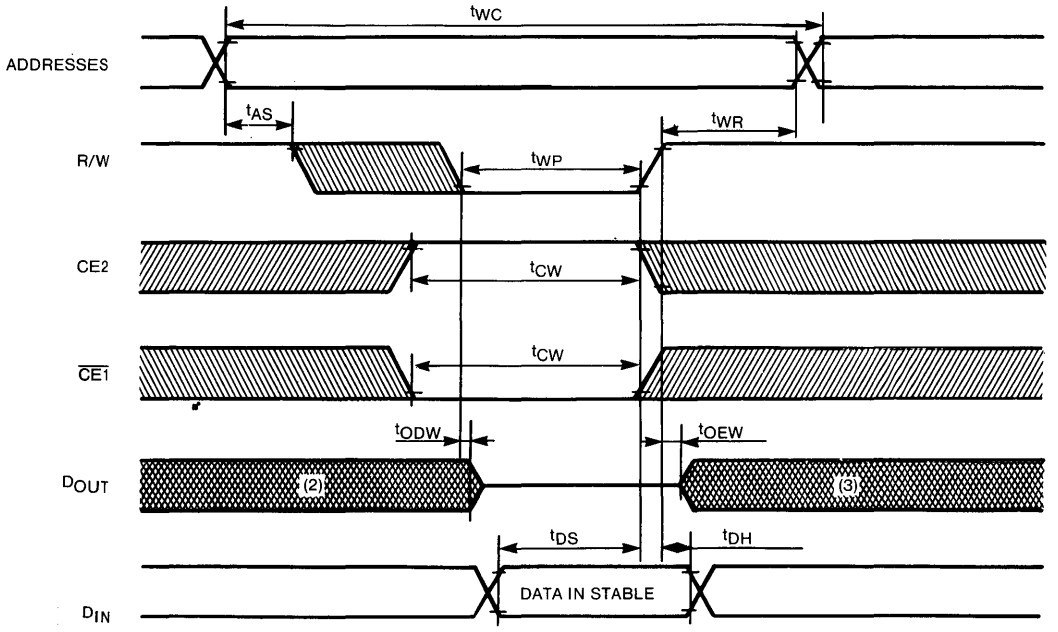
- $V_{IN}=V_{DD}-0.2V/0.2V$
- Output Reference Level: 1.5V/1.5V
- Timing Measurement Level: 1.5V/1.5V
- Input Pulse Rise and Fall Time: ≤ 20ns
- Output Load: 100pF (Include Jig)

TIMING WAVEFORMS

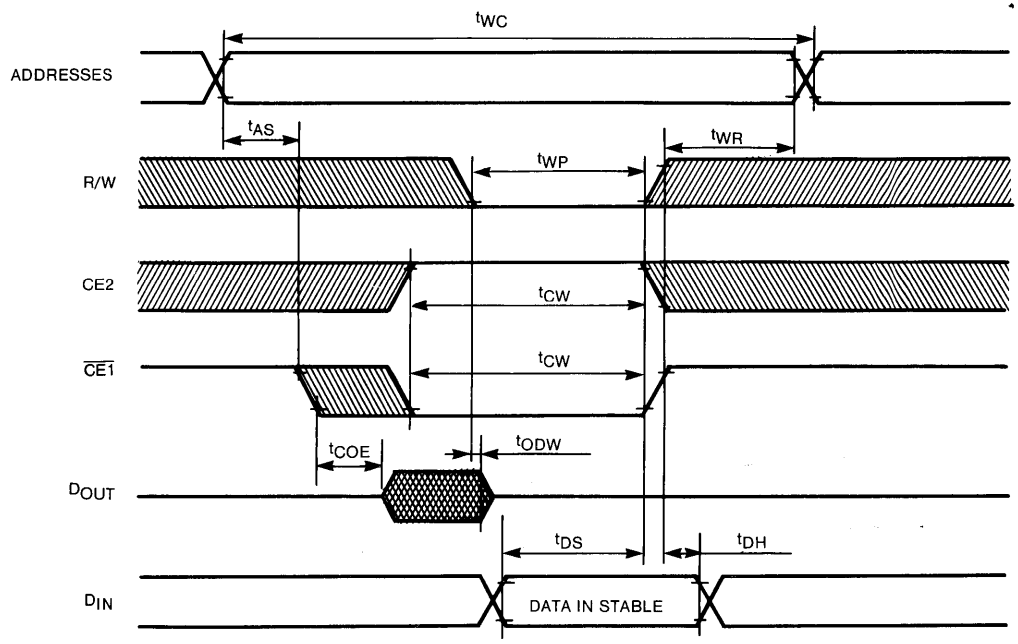
READ CYCLE (1)



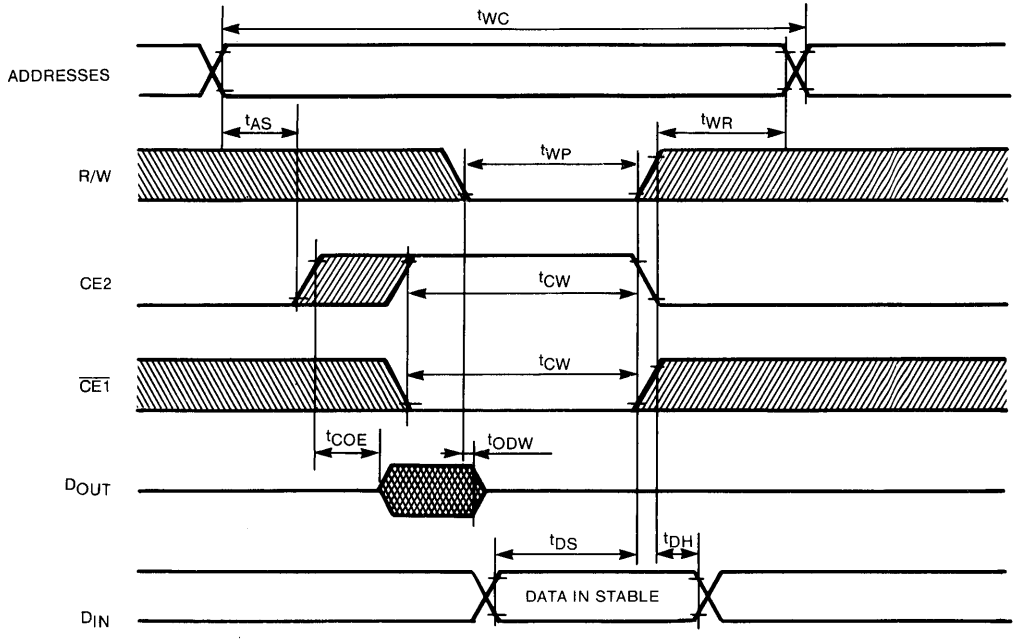
WRITE CYCLE 1 (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



NOTE: (1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

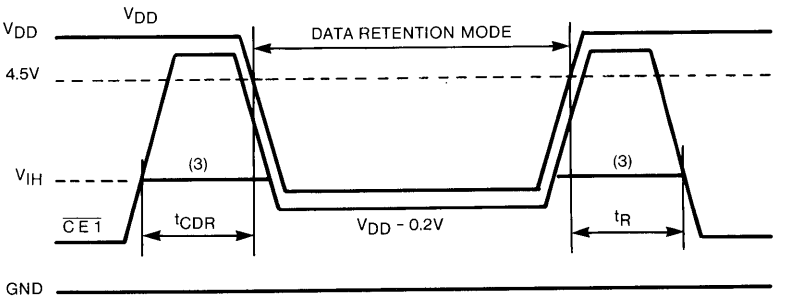
(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

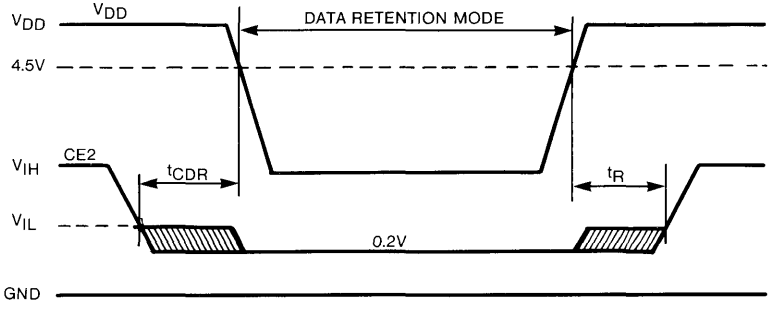
DATA RETENTION CHARACTERISTICS (Ta=−40~85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Current	Ta=25°C	-	0.01	0.2	μA
		Ta=60°C	-	-	1.0	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		$t_{RC(1)}$	-	-	μs

$\overline{CE1}$ Controlled Data Retention Mode (2)



CE2 Controlled Data Retention Mode (4)



Note: (1) t_{RC}: Read Cycle Time

(2) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V or CE2 $\geqq$ V_{DD}−0.2V.

(3) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} Voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(4) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V.

DEVICE INFORMATION

The TC5564APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Once a row address change occurs, the precharge operation is executed by an internal pulse generated from the row address transients. Therefore the peak current flows after only row address changes, as is shown in the following figure.

This peak current may induce the noise on V_{DD}/GND line. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

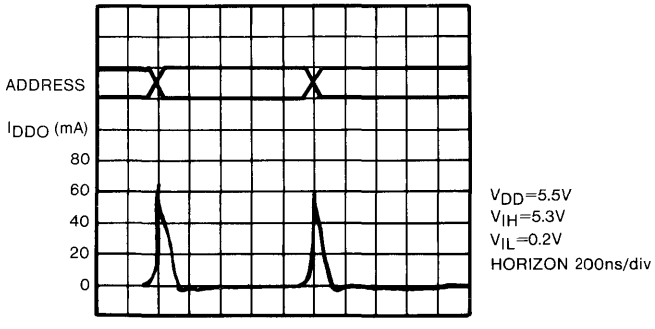
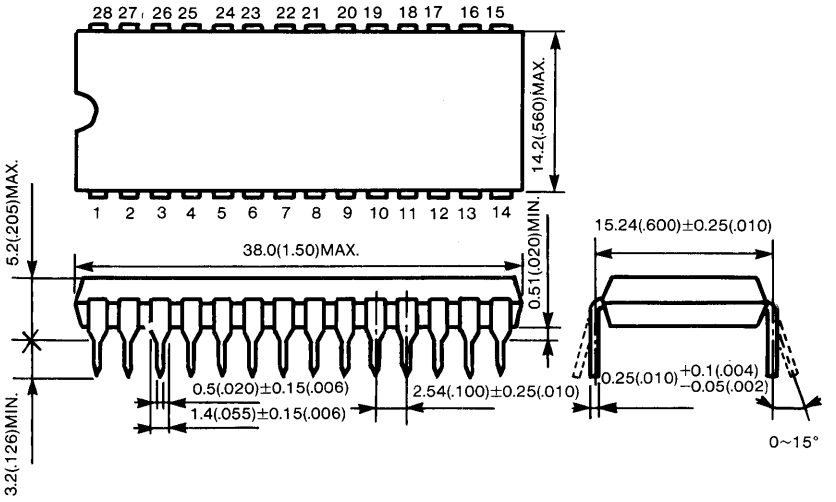


Fig. TYPICAL CURRENT WAVEFORMS

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

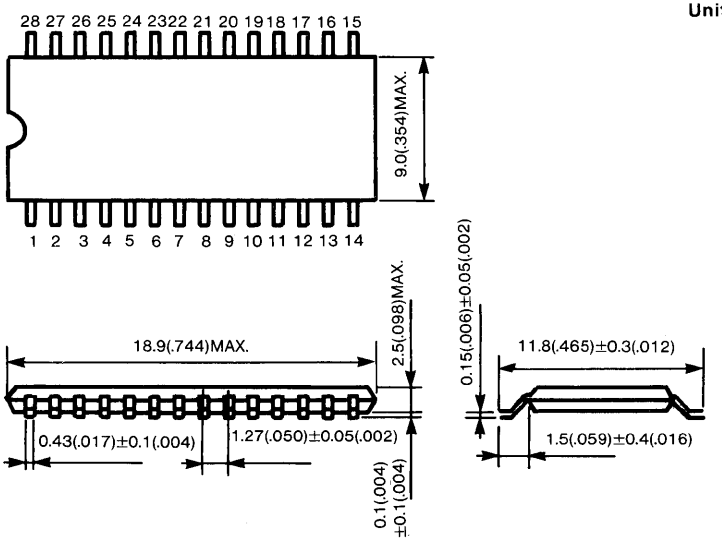
Unit in mm (inches)



Note: Lead pitch is 2.54mm and tolerance is ±0.25mm against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

MFP 28 PIN OUTLINE DRAWINGS (F28GA-P)

Unit in mm (inches)



Note: Lead pitch is 1.27mm and tolerance is ±0.12mm against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5565PL-12, TC5565PL-15
TC5565FL-12, TC5565FL-15

DESCRIPTION

The TC5565P is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 120ns/150ns.

When CE_2 is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5565P has three control inputs. Two chip enables ($\overline{CE_1}$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565P is suitable for use in various microprocessor application systems where high speed, low power, and bettery back up are required.

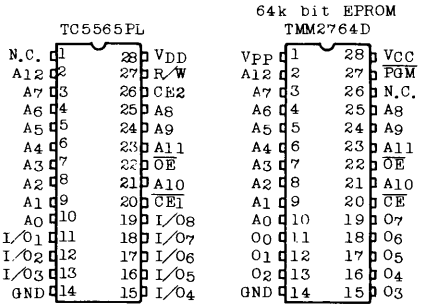
The TC5565P also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5565P is offered in a dual-in-line 28 pin standard plastic package.

FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current : 100mA(MAX.)
- 5V Single Power Supply
- Power Down Features : CE_2, $\overline{CE_1}$
- Fully Static Operation
- Data Retention Supply Voltage
  : 2.0~5.5V

PIN CONNECTION (TOP VIEW)



PIN NAMES

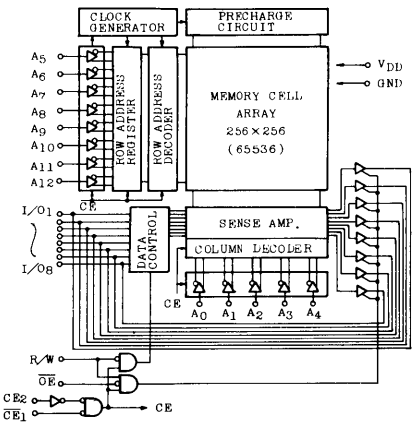
A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

- Access Time

	TC5565PL-12 TC5565FL-12	TC5565PL-15 TC5565FL-15
Address Access Time (MAX.)	120ns	150ns
$\overline{CE_1}$ Access Time (MAX.)	120ns	150ns
CE_2 Access Time (MAX.)	120ns	150ns
Output Enable Time (MAX.)	60ns	70ns

- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 Pin DIP : TC5565PL-12/PL-15
- Plastic Flat Package : TC5565FL-12/FL-15
- Pin Compatible with 2764 type EPROM

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature	260·10	°C·Sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

*……−2.0V at Pulse width 10ns　　**…Flat package

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

D. C and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$		—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		−1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$		4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IH}$ or R/W=V_{IL} or $\overline{OE}=V_{IH}$ $V_{OUT}=0\sim V_{DD}$		—	—	±1.0	μA
I_{DDO1}	Operating Current	$V_{DD}=5.5V$ $\overline{CE_1}=V_{IL}$ $CE_2=V_{IH}$ Other Input =V_{IH}/V_{IL}	$t_{CYCLE}=1\mu s$	—	—	10	mA
			t_{CYCLE} = Min. cycle	—	—	45	mA
I_{DDO2}	Operating Current	$V_{DD}=5.5V$ $\overline{CE_1}=0.2V$ $CE_2=V_{DD}-0.2V$ Other Input =$V_{DD}-0.2V/0.2V$	$t_{CYCLE}=1\mu s$	—	—	5	mA
			t_{CYCLE} = Min. cycle	—	—	40	mA
I_{DDS1}	Standby Current	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$		—	—	3	mA
*I_{DDS2}	Standby Current	$\overline{CE_1}=V_{DD}-0.2V$ or $CE_2=0.2V$ $V_{DD}=2.0\sim5.5V$		—	2	100	μA

Note : In standby mode with $\overline{CE_1}\geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2\geqq V_{DD}-0.2V$ or $CE_2\leqq 0.2V$.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS ($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC5565PL-12 TC5565FL-12		TC5565PL-15 TC5565FL-15		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	V_{IN}=2.4V/0.6V	120	—	150	—	ns
t_{ACC}	Address Access Time	V_{IH}=2.2V	—	120	—	150	ns
t_{CO1}	$\overline{CE_1}$ Access Time	V_{IL}=0.8V	—	120	—	150	ns
t_{CO2}	CE_2 Access Time	tr, tf≦5ns	—	120	—	150	ns
t_{OE}	Output Enable to Output in Valid	V_{OH}=2.2V	—	60	—	70	ns
t_{COE}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in Low-Z	V_{OL}=0.8V	10	—	10	—	ns
t_{OEE}	Output Enable to Output Low-Z	Output Load : C_L(100pF)and 1·TTL Gate	5	—	5	—	ns
t_{OD}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in High-Z		—	60	—	70	ns
t_{ODO}	Output Enable to Output in High-Z		—	50	—	60	ns
t_{OH}	Output Data Hold Time		20	—	20	—	ns

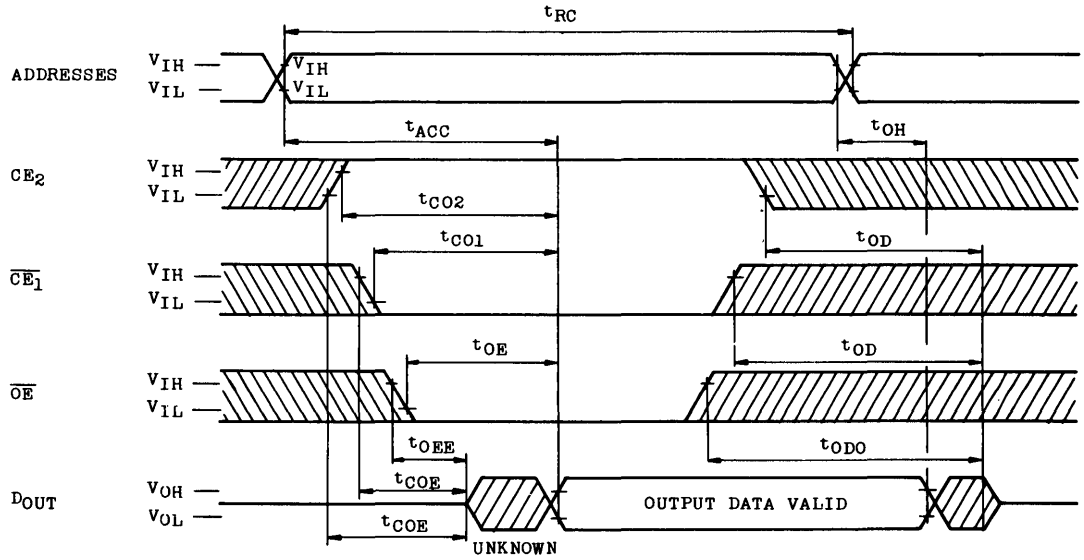
Write Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC5565PL-12 TC5565FL-12		TC5565PL-15 TC5565FL-15		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	V_{IN}=2.4V/0.6V	120	—	150	—	ns
t_{WP}	Write Pulse Width	V_{IH}=2.2V	80	—	100	—	ns
t_{CW}	Chip Selecion to End of Write	V_{IL}=0.8V	100	—	120	—	ns
t_{AS}	Address Set up Time	tr, f≦5ns	0	—	0	—	ns
t_{WR}	Write Recovery Time		0	—	0	—	ns
t_{WRI}	Write Recovery Time ($\overline{CE_1}$, CE_2)		10	—	10	—	ns
t_{ODW}	R/W to Output High-Z		—	50	—	70	ns
t_{OEW}	R/W to Output Low-Z		10	—	10	—	ns
t_{DS}	Data Set Up Time		50	—	60	—	ns
t_{DH}	Data Hold Time		0	—	0	—	ns
t_{DHI}	Data Hold Time ($\overline{CE_1}$, CE_2)		10	—	10	—	ns

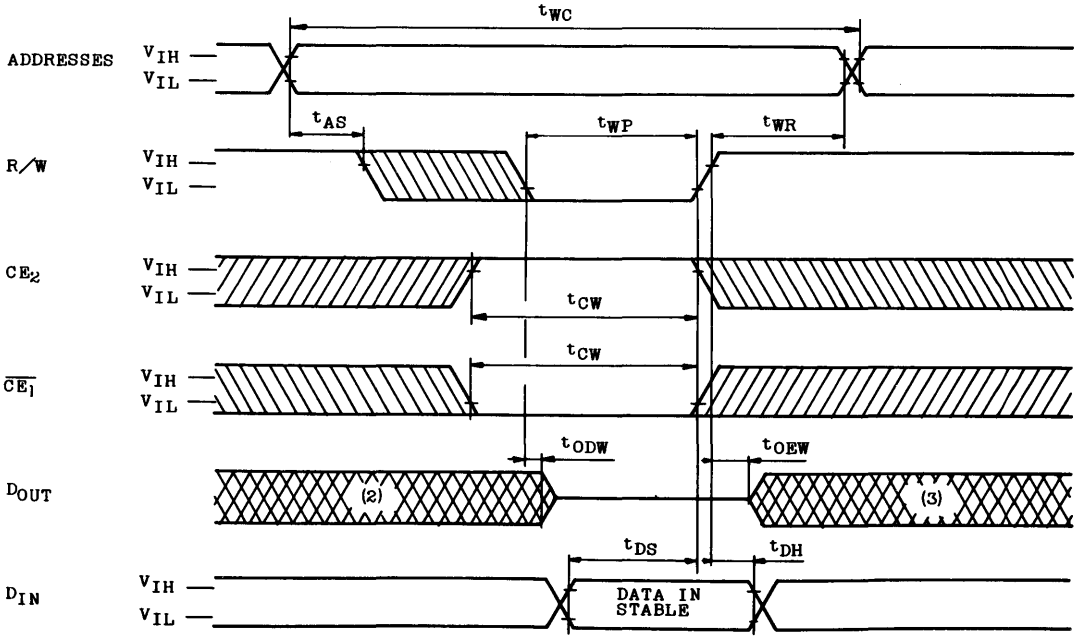
Note : Input Pulse Levels=V_{IN}
Timing Measurement Reference Levels=V_{IH}, V_{IL}

TIMING WAVEFORMS

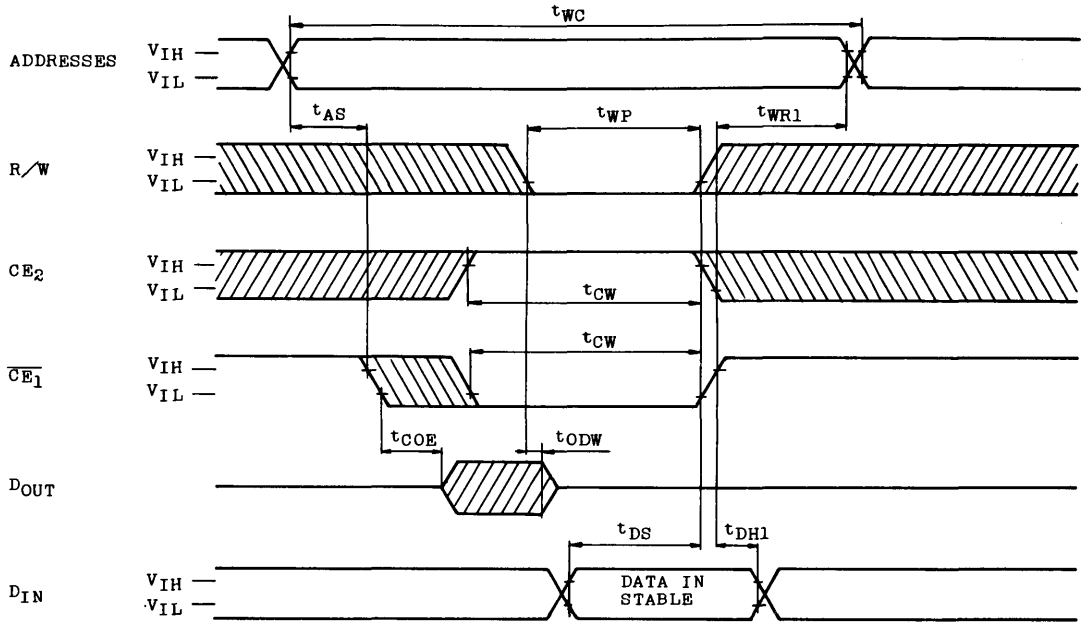
- READ CYCLE (1)



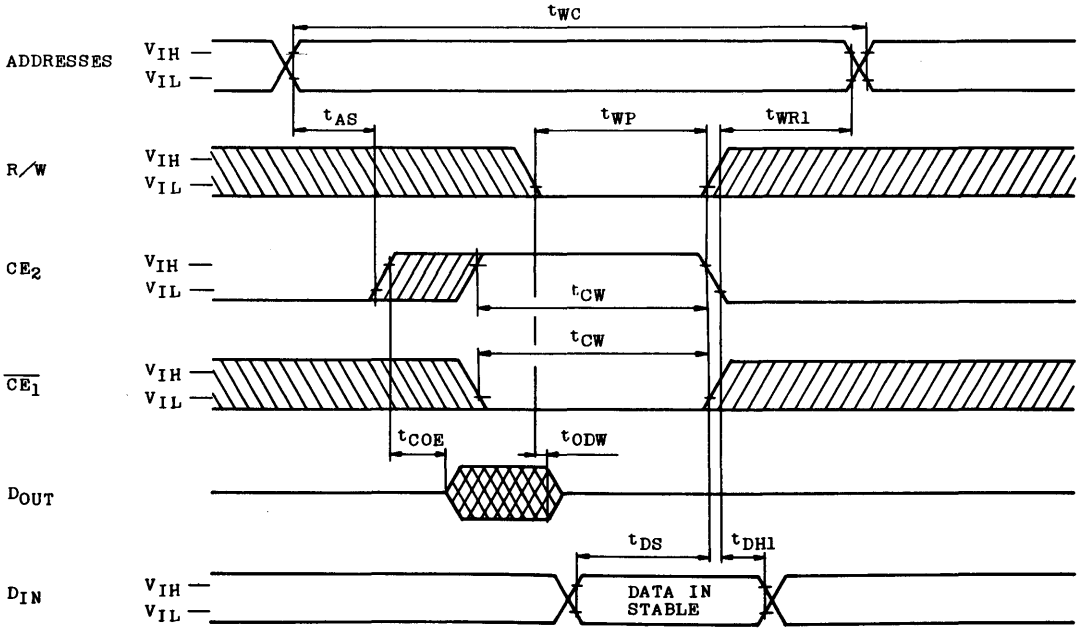
- WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



- WRITE CYCLE 3 (4) (CE2 Controlled Write)



Note :

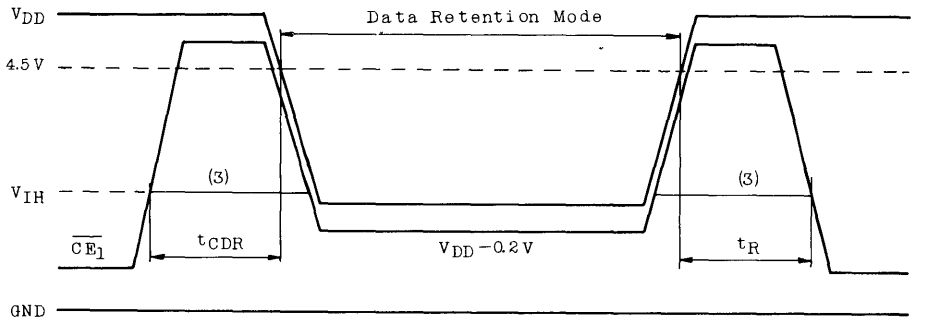
1. R/W is High for Read cycle,
2. Assuming that $\overline{CE_1}$ low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedane state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

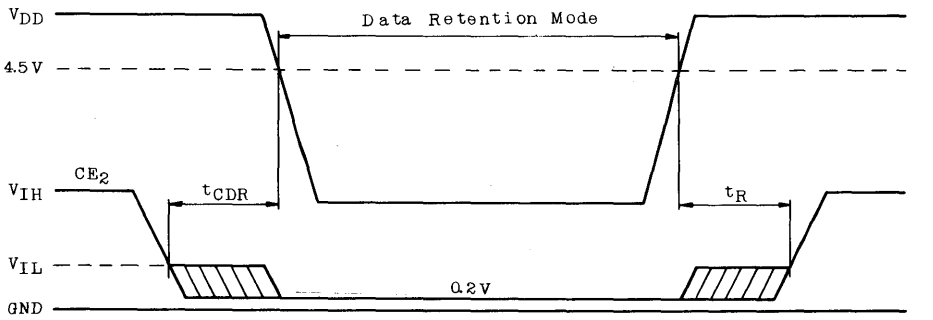
SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage			2.0	—	5.5	V
I_{DDS2}	Standby Supply Current	TC5565PL-12 PL-15 FL-12 FL-15	V_{DD}=3.0V	—	—	50	μA
			V_{DD}=5.5V	—	—	100	μA
t_{CDR}	Chip Deselection to Data Retntion Mode			0	—	—	μs
t_R	Recovery Time			t_{RC}(1)	—	—	μs

Note (1) : Read cycle time.

- $\overline{CE1}$ Controlled Data Retention Mode (2)



- CE2 Controlled Data Retention Mode (4)



Note :

2. In $\overline{CE_1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
3. If the V_{IH} of $\overline{CE_1}$ is 2.2V in operation, I_{DDS1} current flows the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
4. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5565P is an asyncnronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the percharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF. decoupling capacitor for every device is recommended to eliminate such noise.

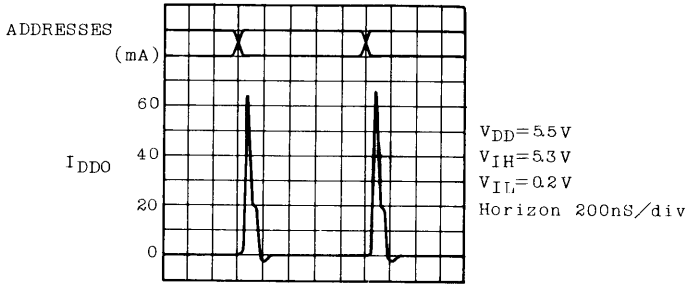
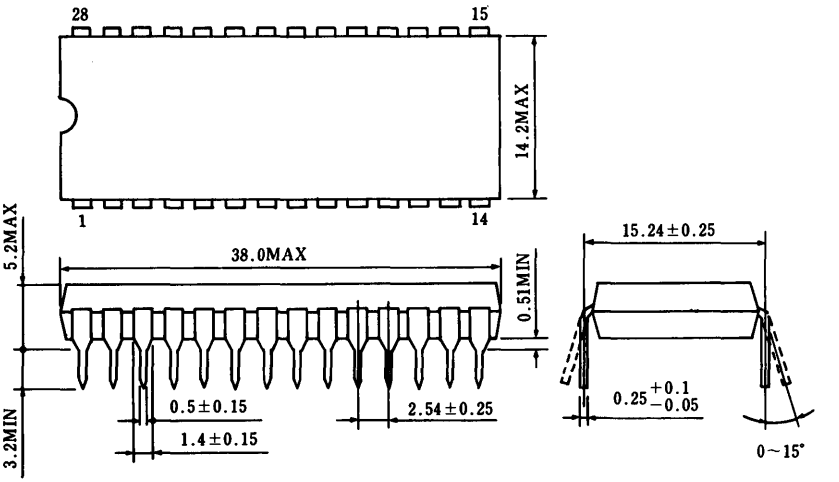


Fig. TYPICAL CURRENT WAVEFORMS

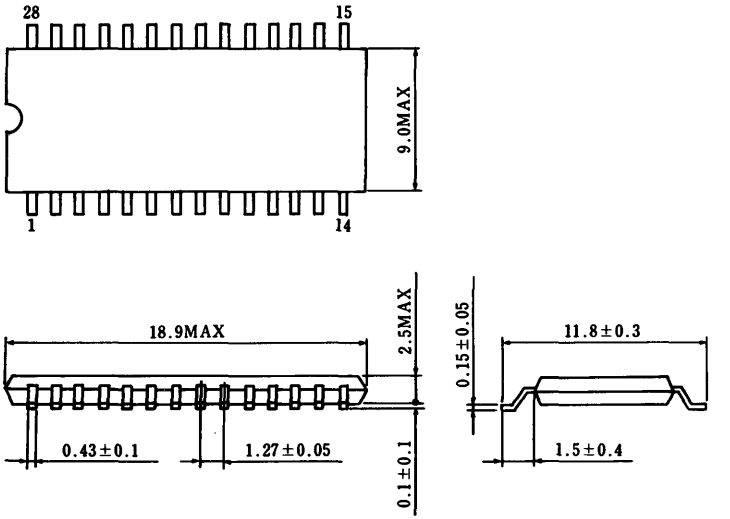
OUTLINE DRAWINGS

- DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

- MFP 28 PIN OUTLINE DRAWING (F28GC-P)



Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5565PL-12L, TC5565PL-15L
TC5565FL-12L, TC5565FL-15L

DESCRIPTION

The TC5565P/F is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 120ns/150ns. When CE_2 is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5565P/F has three control inputs. Two chip enables ($\overline{CE_1}$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565P/F is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565P also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5565P is offered in a dual-in-line 28 pin standard plastic package.

FEATURES

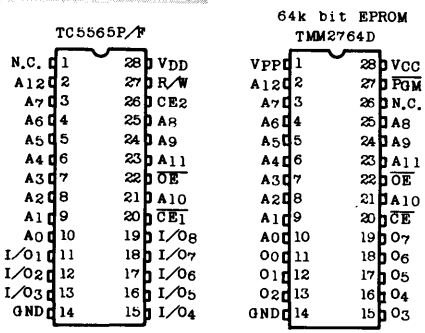
- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current : IμA(Max.) Ta=25°C
- 5V Single Power Supply
- Power Down Features : CE_2, $\overline{CE_1}$
- Fully Static Operation
- Data Retention Supply Voltage
  : 2.0~5.5V

- Access Time

	TC5565PL-12L TC5565FL-12L	TC5565PL-15L TC5565FL-15L
Address Access Time (MAX.)	120ns	150ns
$\overline{CE_1}$ Access Time (MAX.)	120ns	150ns
CE_2 Access Time (MAX.)	120ns	150ns
Output Enable Time (MAX.)	60ns	70ns

- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 Pin DIP : TC5565PL-12L/PL-15L
- Plastic Flat Package : TC5565FL-12L/FL-15L
- Pin Compatible with 2764 type EPROM

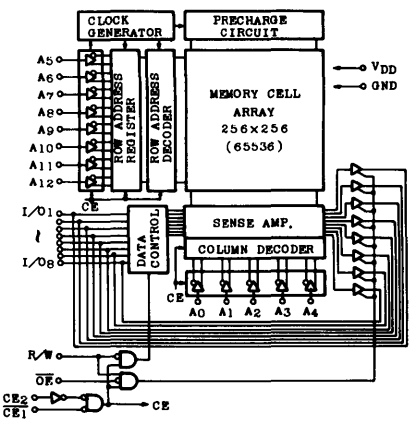
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{SOLDER}	Soldering Temperature	260·10	°C·Sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

*……−2.0V at Pulse width 10ns
**…Flat package

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

D. C and OPERATING CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$		−1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		—	—	±1.0	μA
I_{DDO1}	operating Current	$V_{DD} = 5.5V$ $\overline{CE_1} = V_{IL}$ $CE_2 = V_{IH}$ Other Input $= V_{IH}/V_{IL}$	$t_{CYCLE} = 1\mu s$	—	—	10	mA
			t_{CYCLE} = Min. cycle	—	—	45	
I_{DDO2}	Operating Current	$V_{DD} = 5.5V$ $\overline{CE_1} = 0.2V$ $CE_2 = V_{DD} - 0.2V$ Other Input $= V_{DD} - 0.2V/0.2V$	$t_{CYCLE} = 1\mu s$	—	—	5	mA
			t_{CYCLE} = Min. cycle	—	—	40	
I_{DDS1}	Standby Current	$\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$		—	—	3	mA
*I_{DDS2}	Standby Current	$\overline{CE_1} = V_{DD} - 0.2V$ or $CE_2 = 0.2V$	Ta = 25°C	—	0.6	1.0	μA
			Ta = 0 ~ 70°C	—	—	30	

Note : In standby mode with $\overline{CE_1} \geqq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geqq V_{DD} - 0.2V$ or $CE_2 \leqq 0.2V$.

CAPACITANCE

($Ta = 25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC5565PL-12L TC5565FL-12L		TC5565PL-15L TC5565FL-15L		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	V_{IN}=2.4V/0.6V	120	—	150	—	ns
t_{ACC}	Address Access Time	V_{IH}=2.2V	—	120	—	150	ns
t_{CO_1}	$\overline{CE_1}$ Access Time	V_{IL}=0.8V	—	120	—	150	ns
t_{CO_2}	CE_2 Access Time	t_R, t_F≦5ns	—	120	—	150	ns
t_{OE}	Output Enable to Output in Valid	V_{OH}=2.2V	—	60	—	70	ns
t_{COE}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in Low-Z	V_{OL}=0.8V	10	—	10	—	ns
t_{OEE}	Output Enable to Output Low-Z	Output Load : C_L(100pF) and 1·TTL Gate	5	—	5	—	ns
t_{OD}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in High-Z		—	60	—	70	ns
t_{ODO}	Output Enable to Output in High-Z		—	50	—	60	ns
t_{OH}	Output Data Hold Time		10	—	10	—	ns

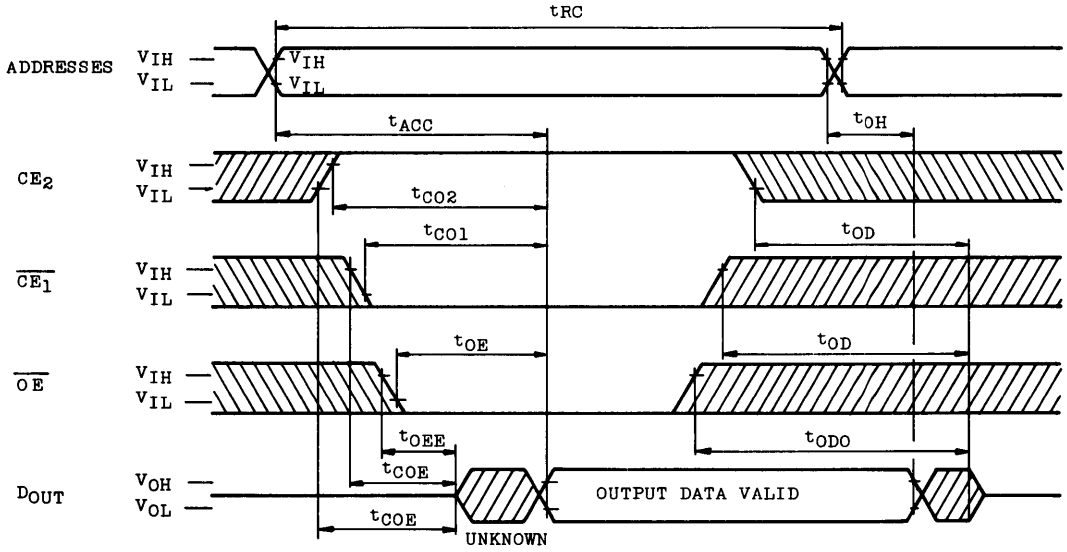
Write Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC5565PL-12L TC5565FL-12L		TC5565PL-15L TC5565FL-15L		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	V_{IN}=2.4V/0.6V	120	—	150	—	ns
t_{WP}	Write Pulse Width	V_{IH}=2.2V	80	—	100	—	ns
t_{CW}	Chip Selection to End of Write	V_{IL}=0.8V	100	—	120	—	ns
t_{AS}	Address Set up Time	t_R, t_F≦5ns	0	—	0	—	ns
t_{WR}	Write Recovery Time		0	—	0	—	ns
t_{WRI}	Write Recovery Time ($\overline{CE_1}$, CE_2)		10	—	10	—	ns
t_{ODW}	R/W to Output High-Z		—	50	—	70	ns
t_{OEW}	R/W to Output Low-Z		10	—	10	—	ns
t_{DS}	Data Set Up Time		50	—	60	—	ns
t_{DH}	Data Hold Time		0	—	0	—	ns
t_{DHI}	Data Hold Time ($\overline{CE_1}$, CE_2)		10	—	10	—	ns

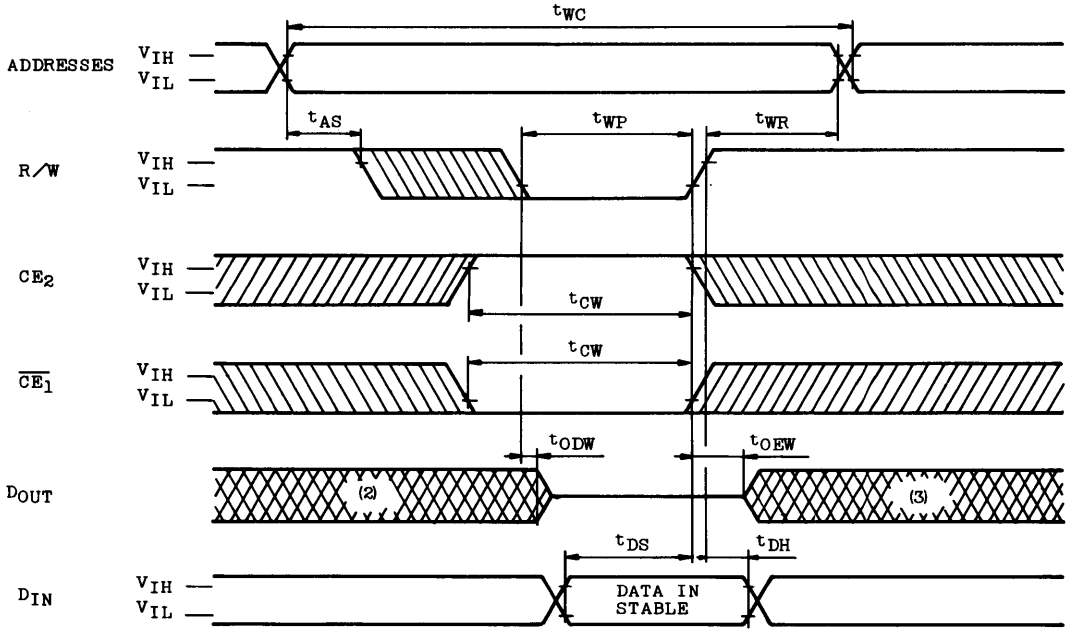
Note : Input Pulse Levels=V_{IN}
Timing Measurement Reference Levels=V_{IH}, V_{IL}

TIMING WAVEFORMS

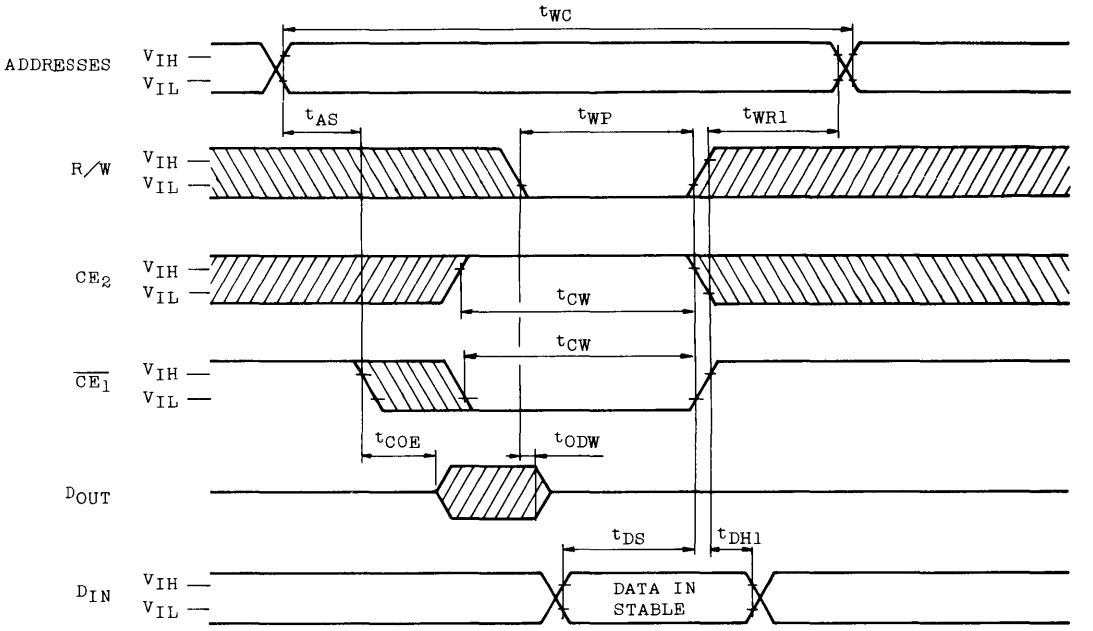
● READ CYCLE (1)



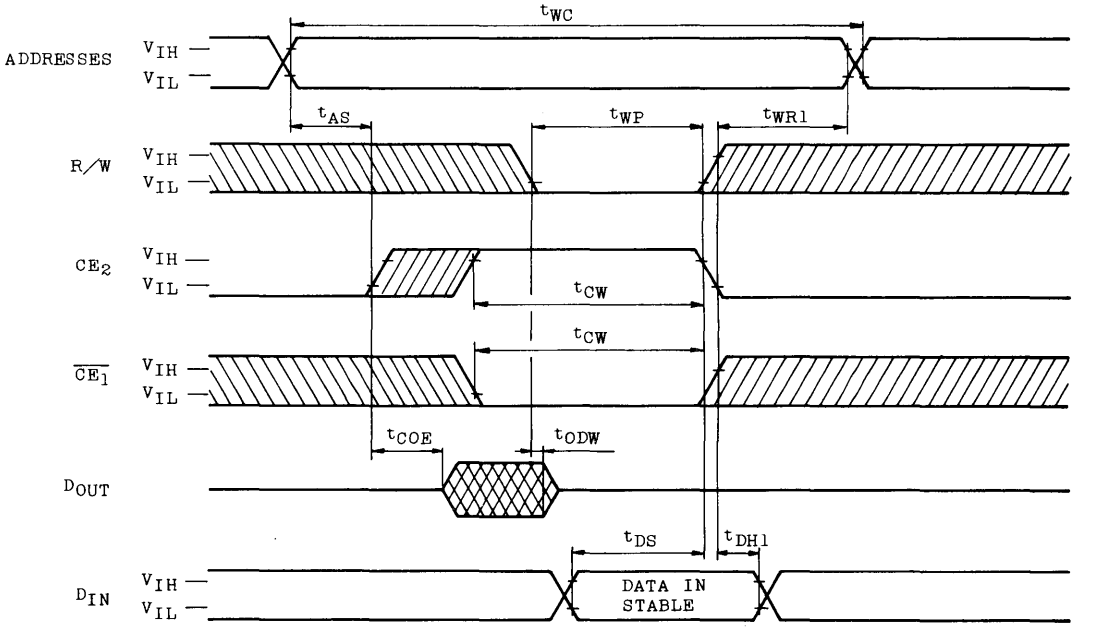
● WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



- WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note :

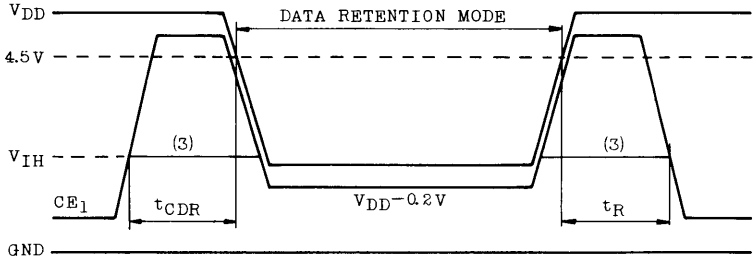
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE}_1$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}_1$ High transition or CE_2 Low transition occure coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

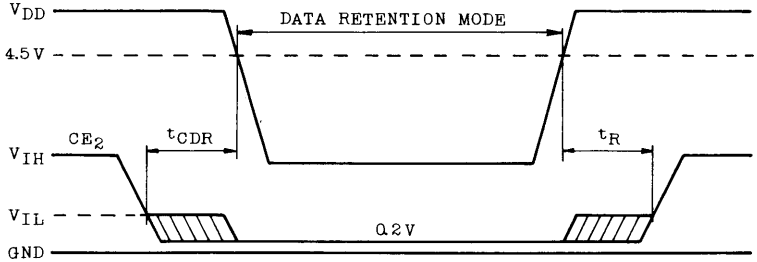
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	—	—	15	μA
		V_{DD}=5.5V	—	—	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}(1)	—	—	μs

Note (1) : Read cycle time.

- $\overline{CE}_1$ Controlled Data Retention Mode (2)



- CE_2 Controlled Data Retention Mode (4)



Note :

2. In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
3. If the V_{IH} of $\overline{CE}_1$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
4. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5565P/F is an synchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the percharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

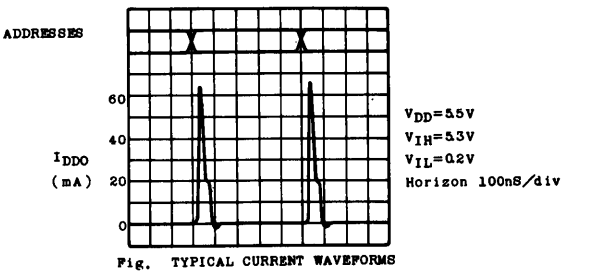
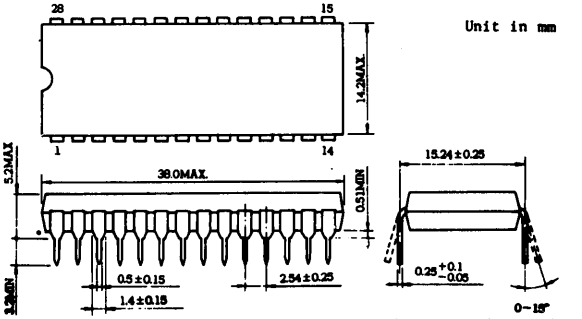


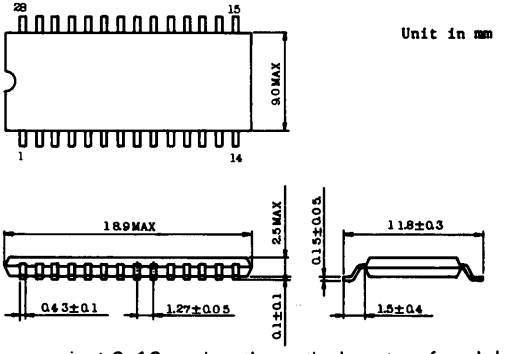
Fig. TYPICAL CURRENT WAVEFORMS

- **DIP 28 PIN OUTLINE DRAWING (6D28A-P)**



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

- **MFP 28 PIN OUTLINE DRAWING (F28GC-P)**



Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

8,192 WORD 8 BIT CMOS STATIC RAM
SILICON GATE MOS

TC5565APL-10, TC5565AFL-10
TC5565APL-12, TC5565AFL-12
TC5565APL-15, TC5565AFL-15

DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.
When CE2 is a logical low or $\overline{CE1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5565APL/AFL has three control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.
The TC5565APL also features pin compatibility with the 64K bit EPROM (TMM2764D).
RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.
The TC5565APL is offered in a dual-in-line 28 pin standard plastic package. The TC5565AFL is offered in 28 pin mini Flat Package

FEATURES

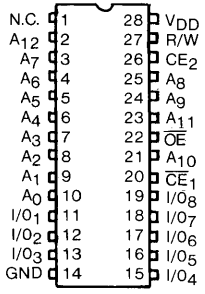
- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current : 100μA (Max.) Ta=70°C
- Access Time
  TC5565APL/AFL-10 : 100ns (Max.)
  TC5565APL/AFL-12 : 120ns (Max.)
  TC5565APL/AFL-15 : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features: CE_2, $\overline{CE_1}$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package (SOP)	TC5565AFL

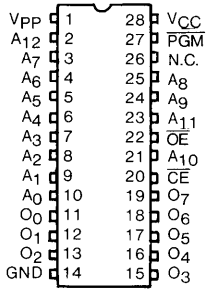
* See TC5563APL Technical Data.

PIN CONNECTION (TOP VIEW)

TC5565APL/AFL



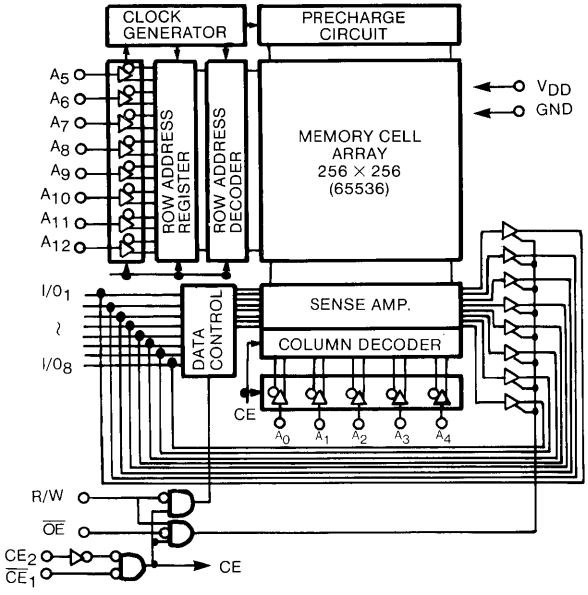
64k bit EPROM
TMM2764D



PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Input
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}_1$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	*−0.3~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{solder}	Soldering Temperature	260 · 10	°C · sec
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	0~70	°C

* −3.0V at pulse width 50ns MAX. ** Flat package

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}			-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			−1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}_1$=V_{IH} or CE_2=V_{OL} or R/W=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0~V_{DD}			-	-	±1.0	μA
I_{DD01}	Operating Current	V_{DD}=5.5V $\overline{CE}_1$=V_{IL} CE_2=V_{IH} Other input = V_{IH}/V_{IL}	t_{cycle}=1.0μs		-	-	10	mA
			TC5565APL-10 TC5565AFL-10	t_{cycle} =100ns	-	-	45	mA
			TC5565APL-12 TC5565AFL-12	t_{cycle} =120ns	-	-	40	mA
			TC5565APL-15 TC5565AFL-15	t_{cycle} =150ns	-	-	35	mA
I_{DD02}		V_{DD}=5.5V $\overline{CE}_1$=0.2V CE_2=V_{DD}−0.2V Other input= V_{DD}−0.2V/0.2V	t_{cycle}=1.0μs		-	-	5	mA
			TC5565APL-10 TC5565AFL-10	t_{cycle} =100ns	-	-	40	mA
			TC5565APL-12 TC5565AFL-12	t_{cycle} =120ns	-	-	35	mA
			TC5565APL-15 TC5565AFL-15	t_{cycle} =150ns	-	-	30	mA
I_{DDS1}	Standby Current	$\overline{CE}_1$=V_{IH} or CE_2=V_{IL}			-	-	3	mA
*I_{DDS2}		$\overline{CE}_1$=V_{DD}−0.2V or CE_2=0.2V	V_{DD}=5.5V		-	2	100	μA
			V_{DD}=3.0V		-	1	50	μA

Note * : In standby mode with $\overline{CE}_1 \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geqq V_{DD}-0.2V$ or $CE_2 \leqq 0.2V$.

CAPACITANCE (Ta=24°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	-	-	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	-	-	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	ns
t_{CO1}	$\overline{CE_1}$ Access Time	-	100	-	120	-	150	ns
t_{CO2}	CE_2 Access Time	-	100	-	120	-	150	ns
t_{OE}	Output Enable to Output Valid	-	50	-	60	-	70	ns
t_{COE}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in Low-Z	10	-	10	-	15	-	ns
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	ns
t_{OD}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in High-Z	-	35	-	40	-	50	ns
t_{ODO}	Output Enable to Output in High-Z	-	35	-	40	-	50	ns
t_{OH}	Output Data Hold Time	20	-	20	-	20	-	ns

Write Cycle

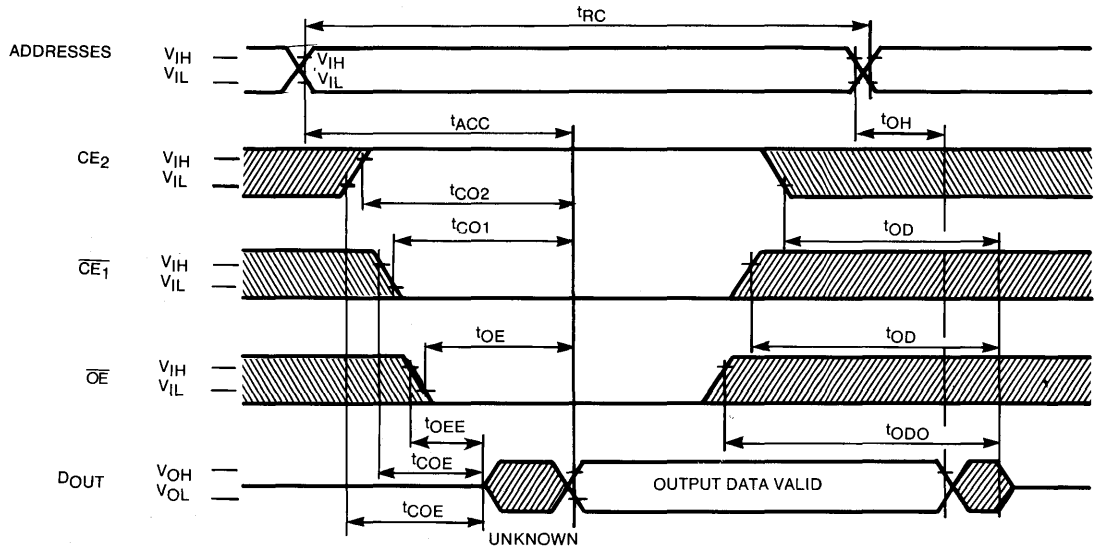
SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	90	-	ns
t_{CW}	Chip Selection to End of Write	80	-	85	-	100	-	ns
t_{AS}	Address Set Up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{ODW}	R/W to Output High-Z	-	35	0	40	-	50	ns
t_{OEW}	R/W to Output Low-Z	5	-	5	-	10	-	ns
t_{DS}	Data Set up Time	40	-	50	-	60	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns

A.C. TEST CONDITION

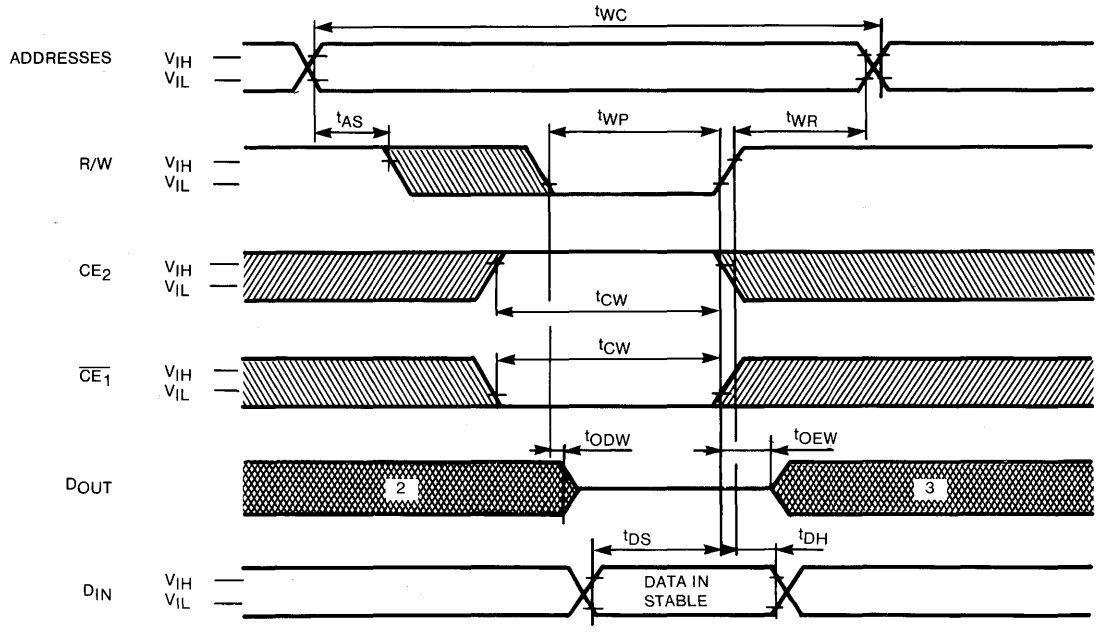
Output Load	: 100pF + 1 TTL Gate
Input Pulse Level	: 0.6V, 2.4V
Timing Measurement V_{IN}	: 0.8V, 2.2V
Reference Level V_{OUT}	: 0.8V, 2.2V
t_r, t_f	: 5ns

TIMING WAVEFORMS

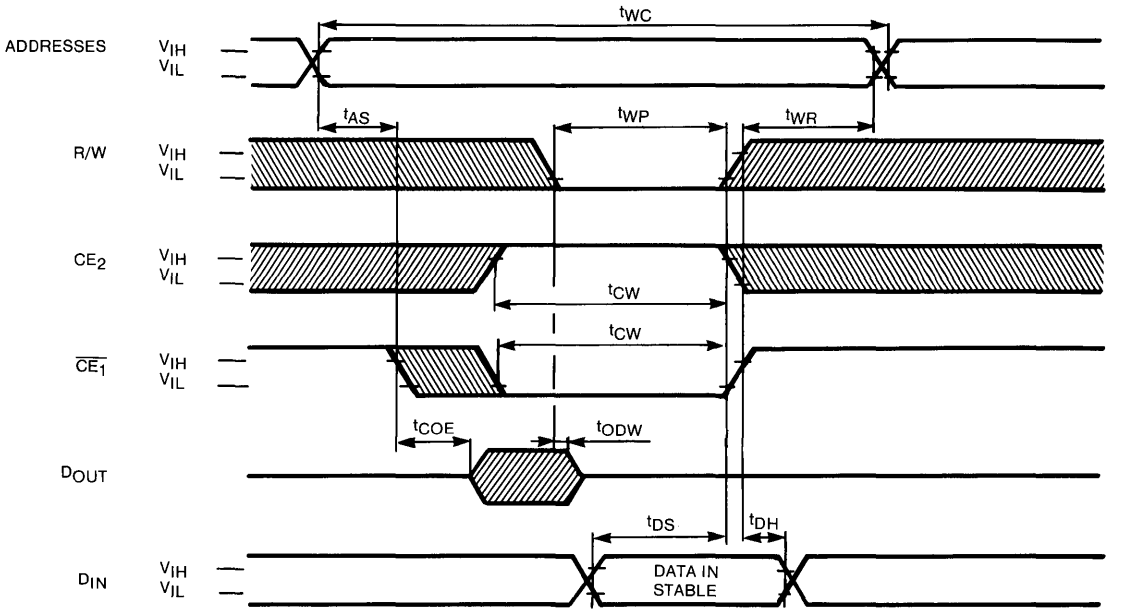
READ CYCLE (1)



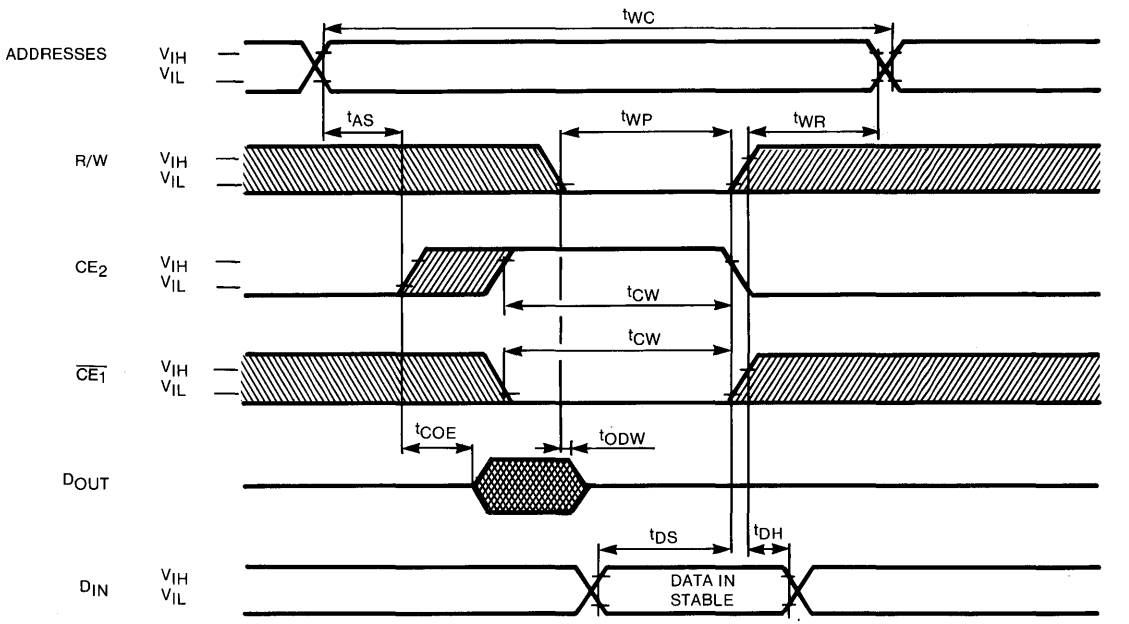
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}_1$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}_1$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in high impedance state.

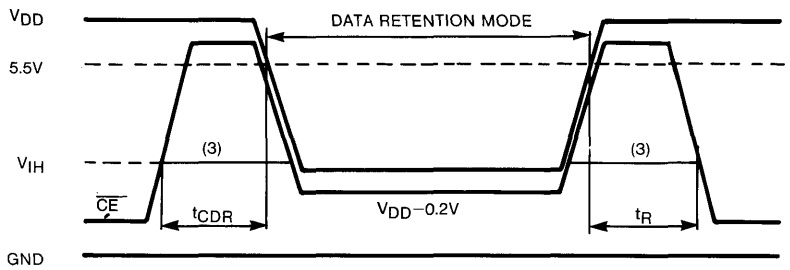
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION (Ta=0~70°C)

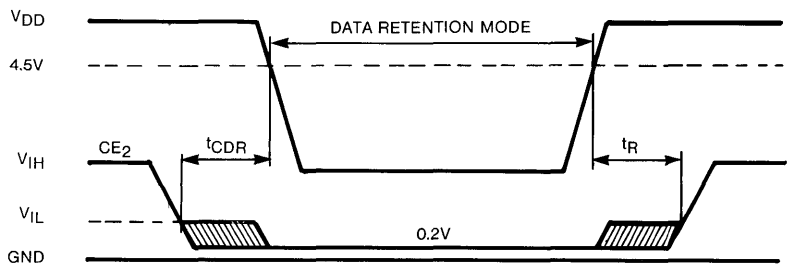
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	-	-	50	μA
		V_{DD}=5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		t_{RC}(1)	-	-	μs

Note (1) : Read cycle time.

$\overline{CE}_1$ Controlled Data Retention Mode (2)



CE_2 Controlled Data Retention Mode (4)



Note 2 : In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD}-0.2V$.

3 : If the V_{IH} of $\overline{CE}_1$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

4 : In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5565APL/AFL is an synchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.
This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

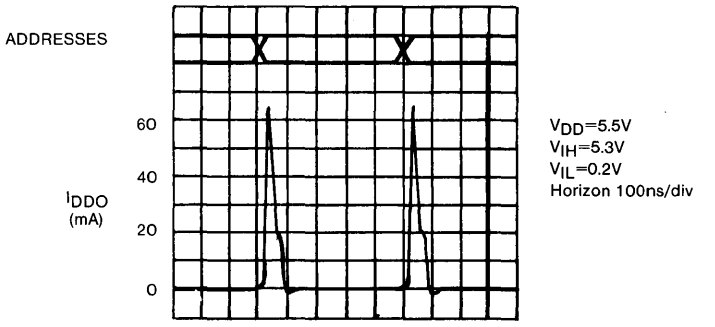
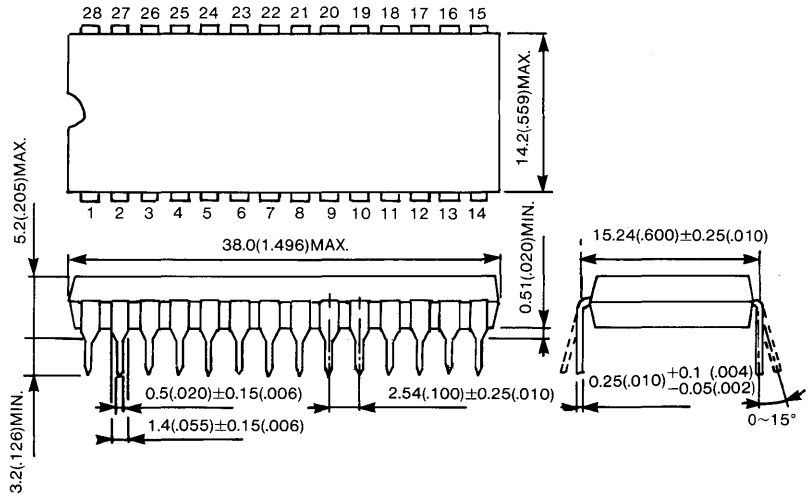


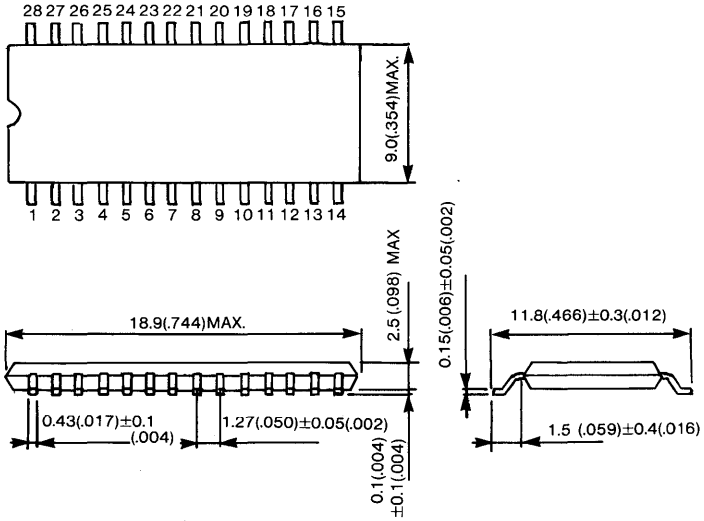
Fig. TYPICAL CURRENT WAVEFORMS

DIP 28 PIN OUTLINE DRAWING (6D28A-P) Unit in mm (inches)



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

MFP 28 PIN OUTLINE DRAWING (F28GC-P) Unit in mm (inches)



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC55257P-10/PL-10
TC55257P-12/PL-12

PRELIMINARY

DESCRIPTION

The TC55257P is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and mimimum cycle time of 100ns/120ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC55257P has two control inputs. Chip enable input ($\overline{CE}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257P is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257P is offered in a dual-in-line 28 pin standard plastic package.

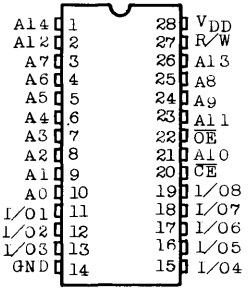
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current
  100μA(Max.) : TC55257PL-10/PL-12
  1mA(Max.) TC55257P-10/P-12
- 5V Single Power Supply
- Power Down Feature : $\overline{CE}$
- Data Retention Supply Voltage : 2.0~5.5V
- Access Time

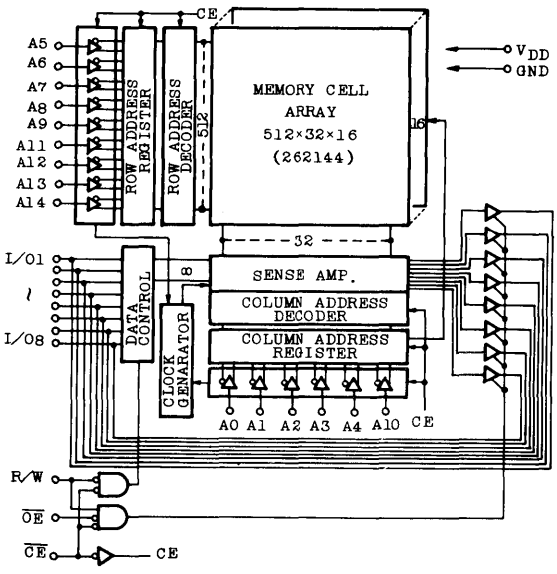
	TC55257P-10 TC55257PL-10	TC55257P-12 TC55257PL-12
Access Time (MAX.)	100ns	120ns
$\overline{CE}$ Access Time (MAX.)	100ns	120ns
Output Enable Time (MAX.)	50ns	60ns

- Directly TTL Compatible : All Inputs and Outputs
- Standard 28 pin DIP

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature	260·10	°C·sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

D. C. and OPERATING CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$		−1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V_{IL} or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		—	—	±1.0	μA
I_{DDO1}	Operating Current (Read Cycle)*	$V_{DD} = 5.5V$ $\overline{CE} = V_{IL}$, R/W = V_{IH} Other Input = V_{IH}/V_{IL}	$t_{cycle} = 1\mu s$	—	—	10	mA
			t_{cycle} = Min. cycle	—	—	45	
I_{DDO2}		$V_{DD} = 5.5V$ $\overline{CE} = 0.2V$ R/W = $V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V/0.2V$	$t_{cycle} = 1\mu s$	—	—	5	mA
			t_{cycle} = Min. cycle	—	—	40	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		—	—	3	mA
I_{DDS2}	Standby Current	$\overline{CE} = V_{DD} - 0.2V$ $V_{DD} = 2.0 \sim 5.5V$	TC55257PL	—	2	100	μA
			TC55257P	—	—	1.0	mA

* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is High for Write Cycle.

CAPACITANCE (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257P-10 TC55257PL-10		TC55257P-12 TC55257PL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	V_{IN}=2.4V/0.6V	100	—	120	—	ns
t_{ACC}	Address Access Time	V_{IH}=2.2V	—	100	—	120	
t_{CO}	$\overline{CE}$ Access Time	V_{IL}=0.8V	—	100	—	120	
t_{OE}	Output Enable to Output in Valid	t_r, t_f≦10ns	—	50	—	60	
t_{COE}	Chip Enable($\overline{CE}$)to Output in Low-Z	V_{OH}=2.2V	10	—	10	—	
t_{OEE}	Output Enable to Output Low-Z	V_{OL}=0.8V	5	—	5	—	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	Output Load : C_L(100pF)and 1TTL Gate	—	50	—	60	
t_{ODO}	Output Enable to Output in High-Z		—	40	—	50	
t_{OH}	Output Data Hold Time		10	—	10	—	

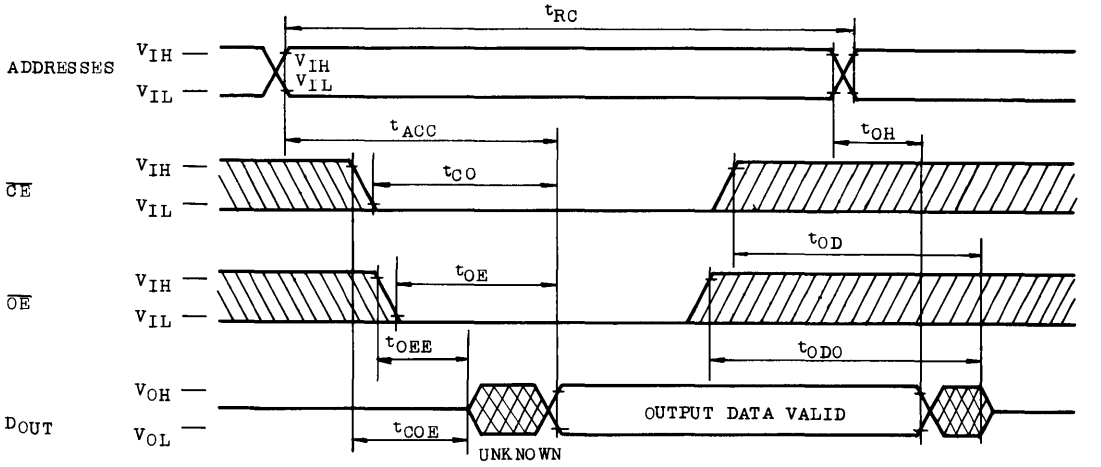
Write Cycle

SYMBOL	PARAMETER	TEST CONDITION	TC55257P-10 TC55257PL-10		TC55257P-12 TC55257PL-12		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	V_{IN}=2.4V/0.6V	100	—	120	—	ns
t_{WP}	Write Pulse Width	V_{IH}=2.2V	70	—	80	—	
t_{CW}	Chip Selection to End of Write	V_{IL}=0.8V	90	—	100	—	
t_{AS}	Address Set up Time	t_r, t_f≦10ns	0	—	0	—	
t_{WR}	Write Recovery Time		0	—	0	—	
t_{ODW}	R/W to Output High-Z		—	50	—	60	
t_{OEW}	R/W to Output Low-Z		10	—	10	—	
t_{DS}	Data Set Up Time		40	—	50	—	
t_{DH}	Data Hold Time		0	—	0	—	

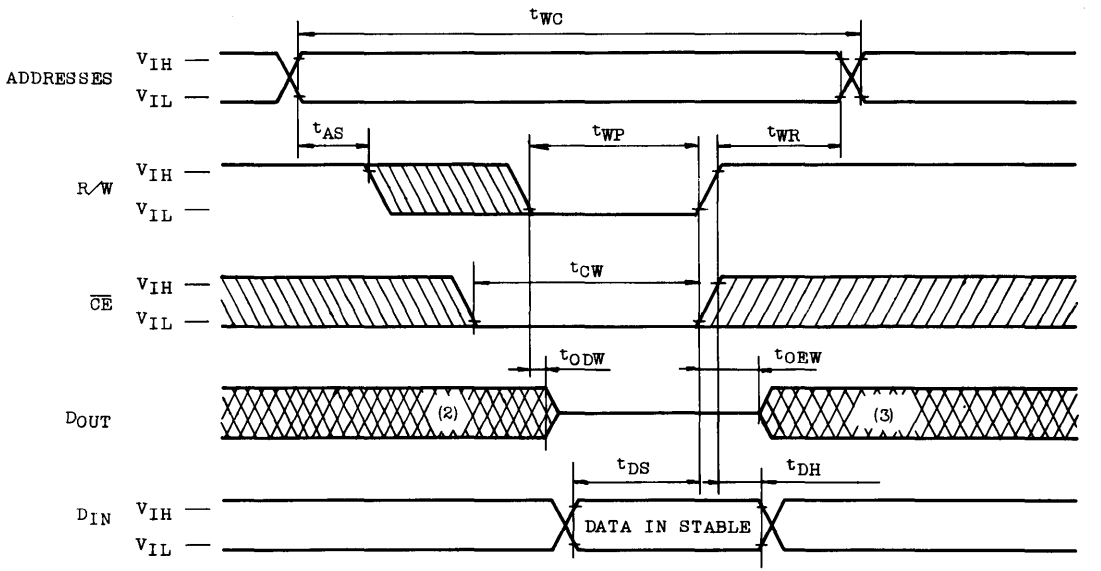
Note : Input pulse levels=V_{IN}
Timing Measurement Reference levels=V_{IH}, V_{IL}

TIMING WAVEFORMS

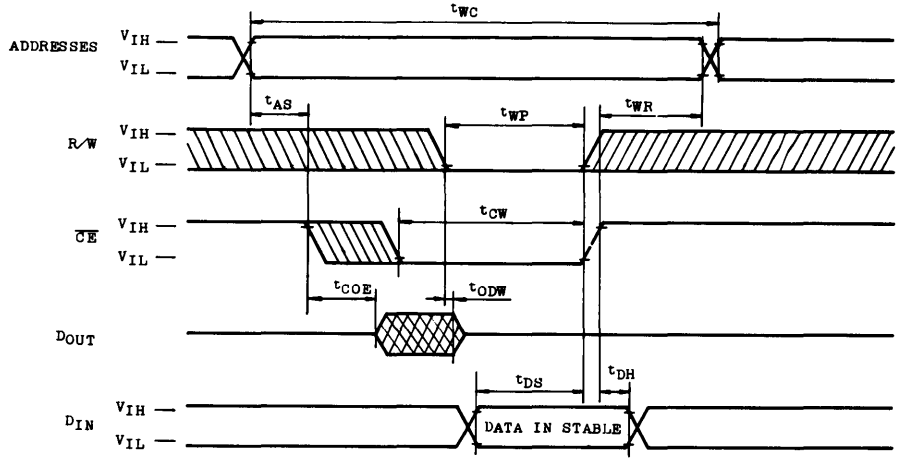
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



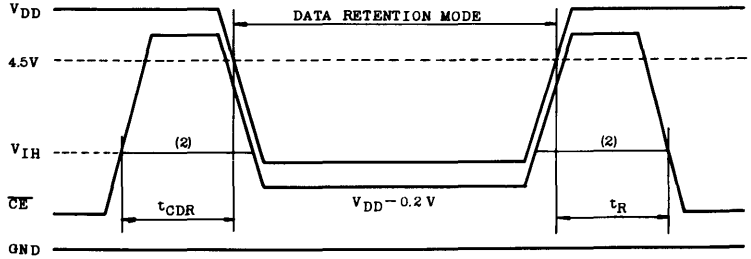
Note: 1. R/W is High for Read cycle.
2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage			2.0	—	5.5	V
I_{DDS2}	Standby Supply Current	TC55257PL	V_{DD}=3.0V	—	—	50	μA
			V_{DD}=5.5V	—	—	100	
		TC55257P		—	—	1.0	mA
t_{CDR}	Chip Deselection to Data Retention Mode			0	—	—	μs
t_R	Recovery Time			t_{RC}(1)	—	—	

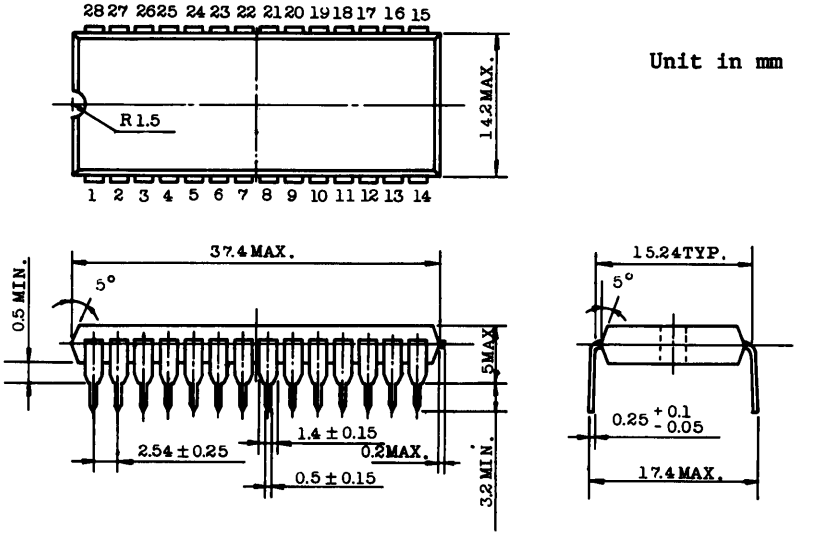
Note (1): Read cycle time.

$\overline{CE}$ Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.4V in operation, I_{DDSI} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

OUTLINE DRAWINGS



Unit in mm

NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

NMOS High Speed Static Random Access Memories

TOSHIBA MOS MEMORY PRODUCTS

4,096 WORD × 4 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2068D-35, TMM2068D-45 TMM2068D-55

DESCRIPTION

The TMM2068D is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns/55ns and maximum operating current of 150mA/120mA/120mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.

Thus the TMM2068D is most suitable for use in cache memory and high speed storage.

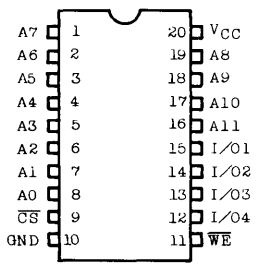
The TMM2068D is offered in a 20 pin standard cerdip package with 0.3 inch width for high density assembly.

The TMM2068D is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

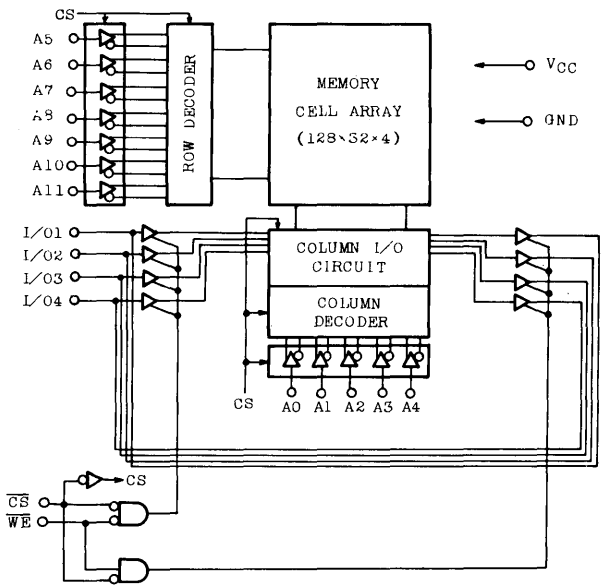
FEATURES

- Fast access time
  t_{ACC}=35ns : TMM2068D-35
  t_{ACC}=45ns : TMM2068D-45
  t_{ACC}=55ns : TMM2068D-55
- Low Power dissipation
  I_{CC}=150mA : TMM2068D-35
  I_{CC}=120mA : TMM2068D-45/55
  I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs
  Directly TTL compatible
- Power down feature : $\overline{CS}=V_{IH}$
- Three state outputs
- Inputs protected : All inputs protection against static charge.
- Package : 20pin standard cerdip package, 0.3 inch width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{11}	Address Inputs
I/O_1~I/O_4	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power(+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−3.5~7.0	V
V_{IN}	Input Voltage	−3.5~7.0	V
$V_{I/O}$	Input/Output Voltage	−3.5~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STRG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D. C. Output Current	20	mA

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−3.0*	—	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

* Pulse Width : 10ns, DC : −0.5V(Min.)

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{CC}		—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−4.0mA		2.4	—	V
V_{OL}	Output Low Voltage	I_{OL}=0.8mA		—	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0~V_{CC} $\overline{CS}$=V_{IH}		—	±50	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	−35	—	150	mA
			−45/55	—	120	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		—	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC} V_{CC}=0~5.5V		—	40	mA

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	

* Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2068D-35		TMM2068D-45		TMM2068D-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{ACC}	Address Access Time	—	35	—	45	—	55	
t_{CO}	Chip Select Access Time	—	35	—	45	—	55	
t_{CLZ}	Chip Selection to Output in Low-Z	5	—	5	—	5	—	
t_{CHZ}	Chip Deselection to Output in High-Z	0	20	0	20	0	20	
t_{OH}	Output Data Hold Time	5	—	5	—	5	—	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	30	—	30	—	30	

Write Cycle

SYMBOL	PARAMETER	TMM2068D-35		TMM2068D-45		TMM2068D-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	30	—	40	—	50	—	
t_{AS}	Address Set Up Time	0	—	0	—	0	—	
t_{WP}	Write Pulse Width	30	—	35	—	40	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	—	0	—	0	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	0	15	0	15	0	20	
t_{DS}	Data Set Up Time	15	—	20	—	20	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	0~3.5V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

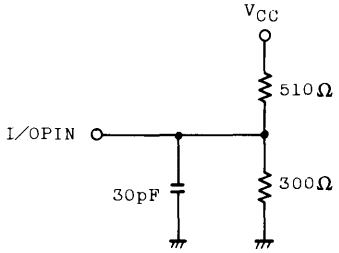
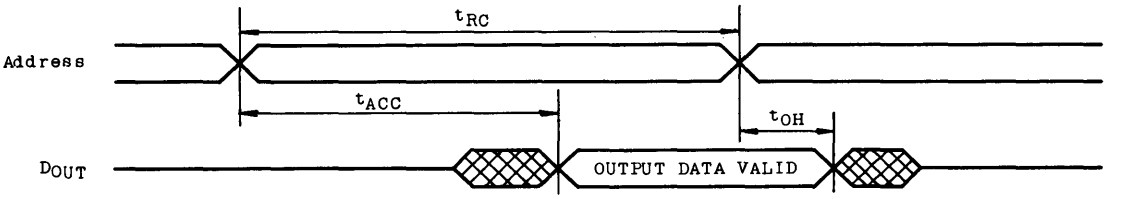


Fig.1 Output Load

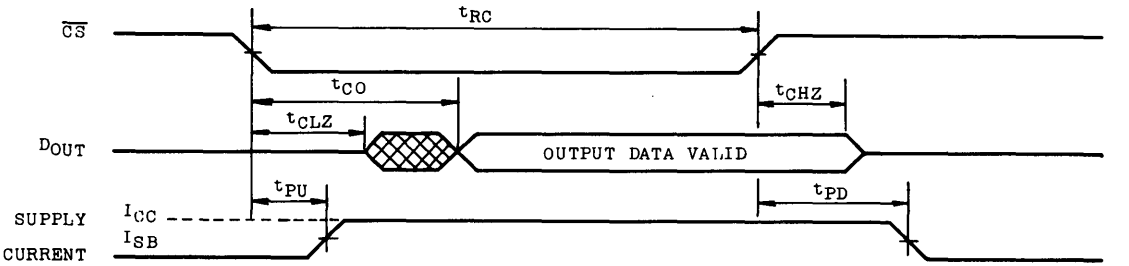
* Note : In all condition, t_{CHZ} max is less than t_{CLZ} min both for a given device and from device to device.

TIMING WAVEFORMS

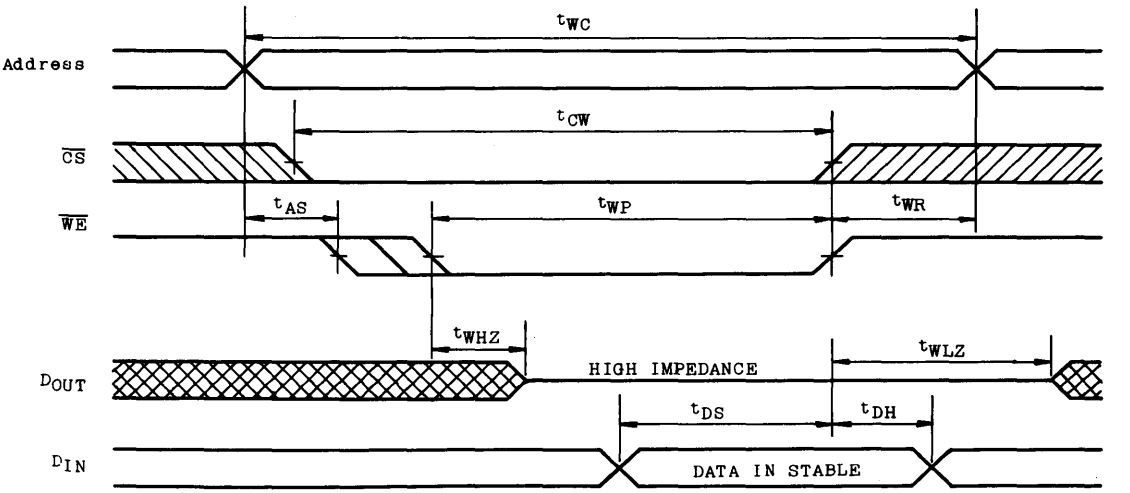
- **Read Cycle 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})**



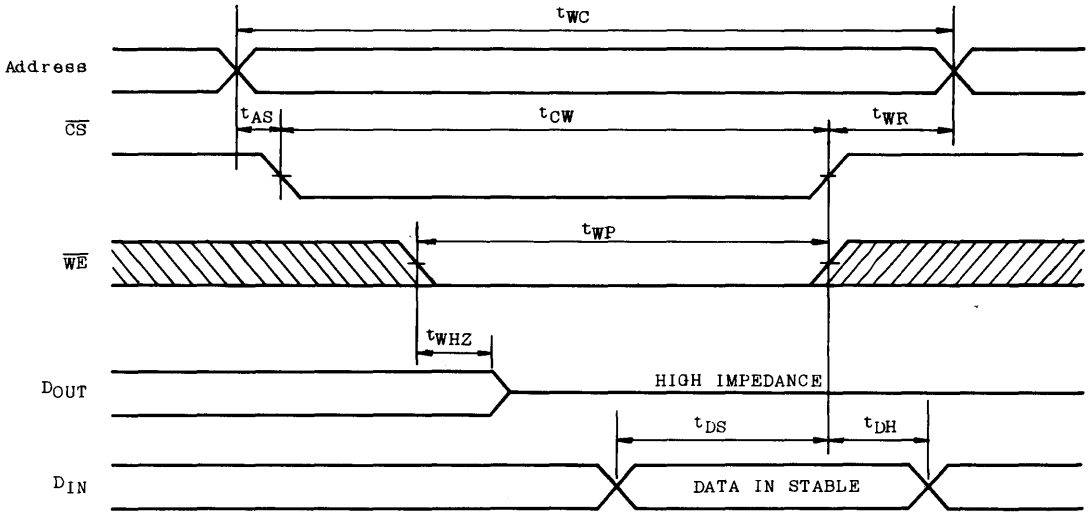
- **Read Cycle 2. ($\overline{WE}$=V_{IH})**



- **Write Cycle 1.**



- **Write Cycle 2.**

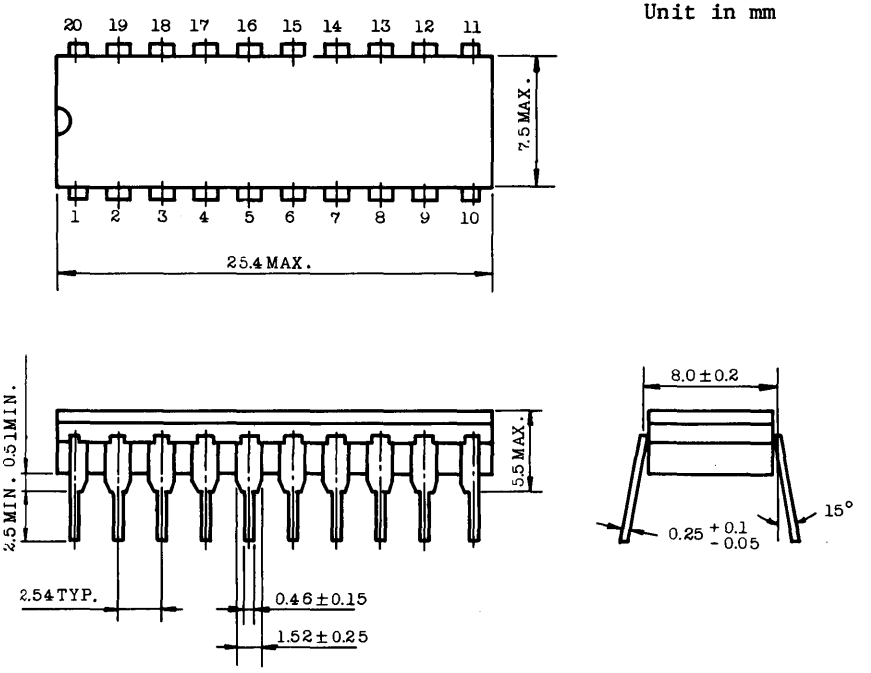


Note :

1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.
2. The operating temperature(Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.20 leads.

4,096 WORD × 4 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2078D-35, TMM2078D-45 TMM2078D-55

PRELIMINARY

DESCRIPTION

The TMM2078D is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns/55ns and maximum operating current of 150mA/120mA/120mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.

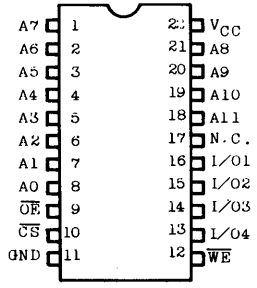
Thus the TMM2078D is most suitable for use in cache memory and high speed storage. The TMM2078D is offered in a 22 pin standard cerdip package with 0.3 inch width for high density assembly.

The TMM2078D is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

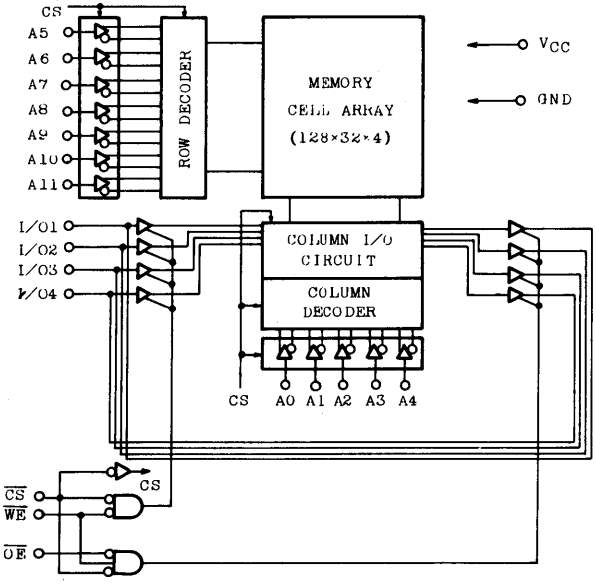
FEATURES

- Fast access time
  t_{ACC}=35ns : TMM2078D-35
  t_{ACC}=45ns : TMM2078D-45
  t_{ACC}=55ns : TMM2078D-55
- Low power dissipation
  I_{CC}=150mA : TMM2078D-35
  I_{CC}=120mA : TMM2078D-45/55
  I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs Directly TTL compatible
- Power down feature : $\overline{CS}$ =V_{IH}
- Output buffer control : $\overline{OE}$
- Three state outputs
- Inputs protected : All inputs protection against static charge.
- Package : 22 pin standard cerdip package, 0.3 inch width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{11}	Address Inputs
I/O_1~I/O_4	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power(+5V)
GND	Ground
N. C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−3.5~7.0	V
V_{IN}	Input Voltage	−3.5~7.0	V
$V_{I/O}$	Input/Output Voltage	−3.5~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STRG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D. C. Output Current	20	mA

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Vovtage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−3.0*	—	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

* Pulse Width : 10ns, DC : −0.5V(Min.)

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{CC}		—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−4.0mA		2.4	—	V
V_{OL}	Output Low Voltage	I_{OL}=0.8mA		—	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0~V_{CC} $\overline{CS}$=V_{IH}		—	±50	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	−35	—	150	mA
			−45/55	—	120	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		—	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC} V_{CC}=0~5.5V		—	40	mA

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=OV	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=OV	10	

* Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2078D-35		TMM2078D-45		TMM2078D-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{ACC}	Address Access Time	—	35	—	45	—	55	
t_{CO}	Chip Select Access Time	—	35	—	45	—	55	
t_{OE}	Output Enable to Output Valid	—	20	—	20	—	25	
t_{CLZ}	Chip Selection to Output in Low-Z	5	—	5	—	5	—	
t_{CHZ}	Chip Deselection to Output in High-Z	0	20	0	20	0	20	
t_{OLZ}	Output Enable to Output in Low-Z	0	—	0	—	0	—	
t_{OHZ}	Output Disable to Output in High-Z	0	15	0	15	0	20	
t_{OH}	Output Data Hold Time	5	—	5	—	5	—	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	30	—	30	—	30	

Write Cycle

SYMBOL	PARAMETER	TMM2078D-35		TMM2078D-45		TMM2078D-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	30	—	40	—	50	—	
t_{AS}	Address Set Up Time	0	—	0	—	0	—	
t_{WP}	Write Pulse Width	30	—	35	—	40	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	—	0	—	0	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	0	15	0	15	0	20	
t_{DS}	Data Set Up Time	15	—	20	—	20	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	0~3.5V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig.1

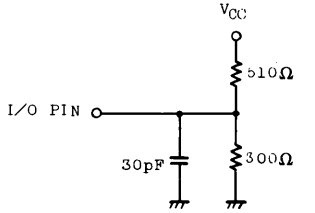
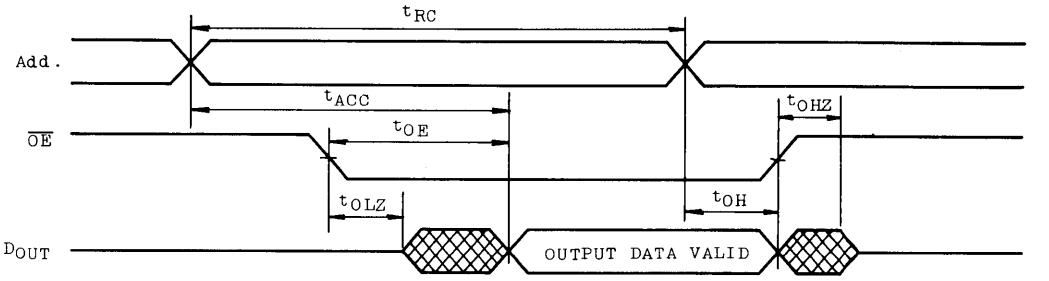


Fig.1 Output Load

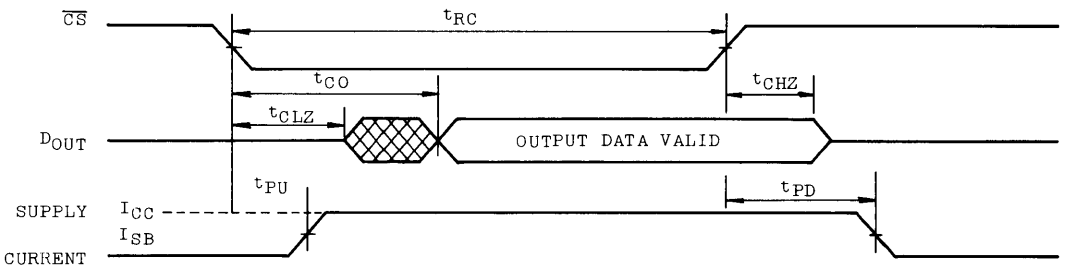
* Note : In all condition, t_{CHZ} max is less than t_{CLZ} min both for a given device and from device to device.

TIMING WAVEFORMS

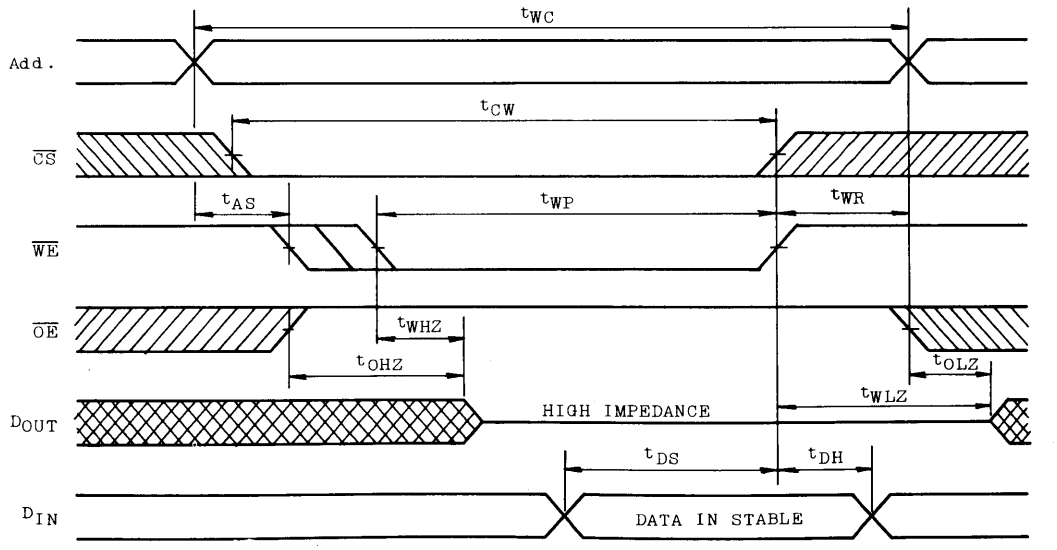
- Read Cycle 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



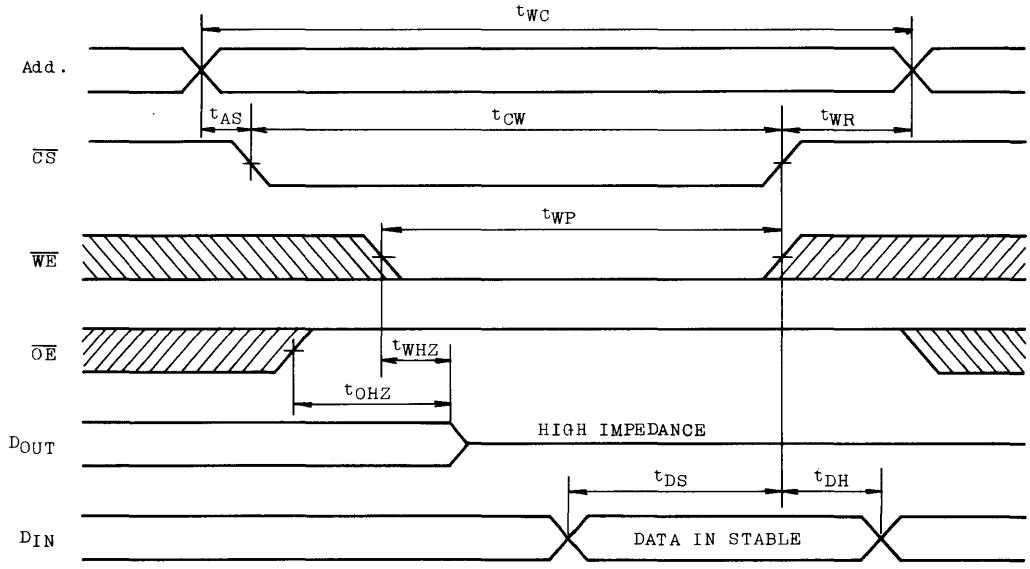
- Read Cycle 2. ($\overline{WE}$=V_{IH}, $\overline{OE}$=V_{IL})



- Write Cycle 1.



- Write Cycle 2.

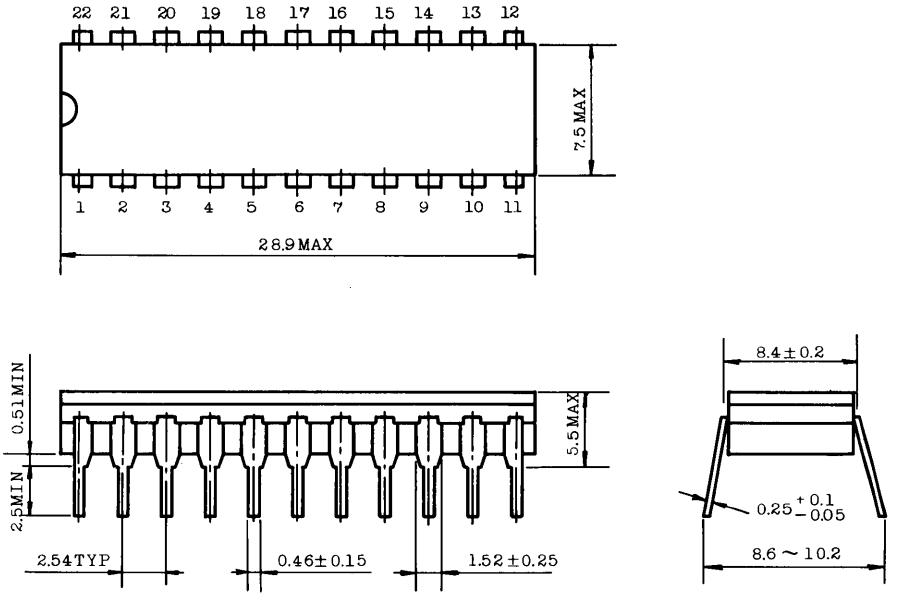


Note :

1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.
2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.22 Leads.

2,048 WORD × 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2018D-35, TMM2018D-45 TMM2018D-55

DESCRIPTION

The TMM2018D is a16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns/55ns and maximum operating current of 150mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.

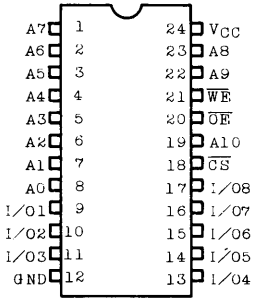
Thus the TMM2018D is most suitable for use in cache memory and high speed storage. The TMM2018D is offered in 24 pin standard cerdip package with 0.3 inch width for high density assembly.

The TMM2018D is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

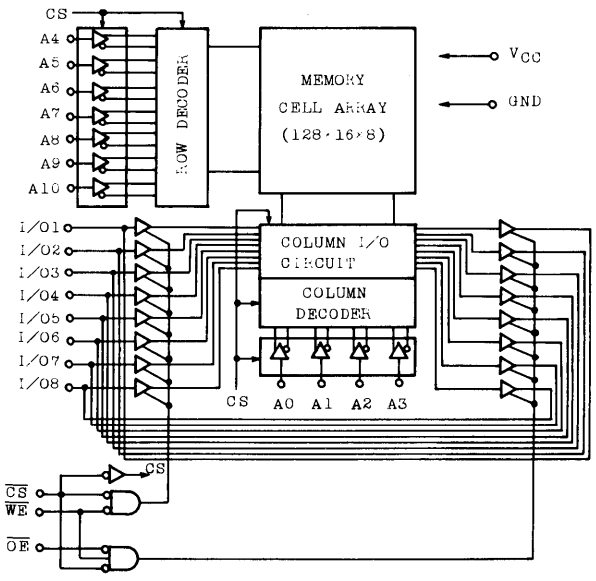
FEATURES

- Fast access time
  t_{ACC} = 35ns : TMM2018D-35
  t_{ACC} = 45ns : TMM2018D-45
  t_{ACC} = 55ns : TMM2018D-55
- Low power dissipation
  I_{CC} = 150mA
  I_{SB} = 20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs
  Directly TTL Compatible
- Power down feature : $\overline{CS}$ = V_{IH}
- Output buffer control : $\overline{OE}$
- Three state outputs
- Inputs protected : All inputs protection against static charge.
- Package : 24 pin standard cerdip, 0.3 inch width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{10}	Address Inputs
I/O_1~I/O_8	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−3.5~7.0	V
V_{IN}	Input Voltage	−3.5~7.0	V
$V_{I/O}$	Input/Output Voltage	−3.5~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D. C. Output Current	20	mA

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−3.0*	—	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

* Pulse Width : 10ns, DC : −0.5V(Min.)

D. C. CHARACTERISTICS

(T_a=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0~V_{CC}	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−4.0mA	2.4	—	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA	—	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0~V_{CC} $\overline{CS}$=V_{IH}	—	±50	μA
I_{CC}	Operating	$\overline{CS}$=V_{IL}	—	150	mA
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}	—	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC} V_{CC}=0~5.5V	—	40	mA

CAPACITANCE*

(T_a=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	

* Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2018D-35		TMM2018D-45		TMM2018D-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{ACC}	Address Access Time	—	35	—	45	—	55	
t_{CO}	Chip Select Access Time	—	35	—	45	—	55	
t_{OE}	Output Enable to Output Valid	—	20	—	20	—	25	
t_{CLZ}	Chip Selection to Output in low-Z	—	5	—	5	—	5	
t_{CHZ}	Chip Deselection to Output in High-Z	0	20	0	20	0	20	
t_{OLZ}	Output Enable to Output in Low-Z	0	—	0	—	0	—	
t_{OHZ}	Output Disable to Output in High-Z	0	15	0	15	0	20	
t_{OH}	Output Data Hold Time	5	—	5	—	5	—	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	30	—	30	—	30	

Write Cycle

SYMBOL	PARAMETER	TMM2018D-35		TMM2018D-45		TMM2018D-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{CW}	Chip Selection to End of Write	30	—	40	—	50	—	
t_{AS}	Address Set Up Time	0	—	0	—	0	—	
t_{WP}	Write Pulse Width	30	—	35	—	40	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	—	0	—	0	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	0	15	0	15	0	20	
t_{DS}	Data Set Up Time	15	—	20	—	20	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	0~3.5V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

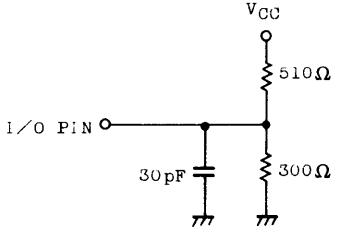
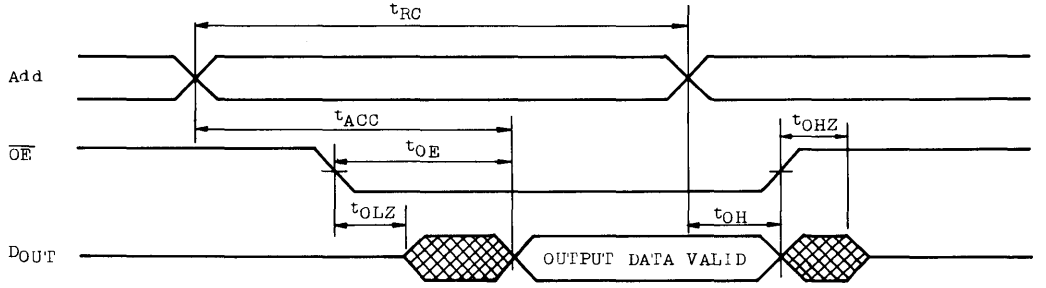


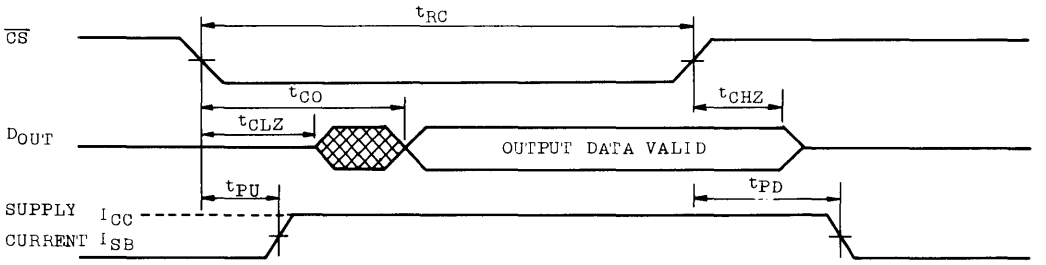
Fig.1 Output Load

TIMING WAVEFORMS

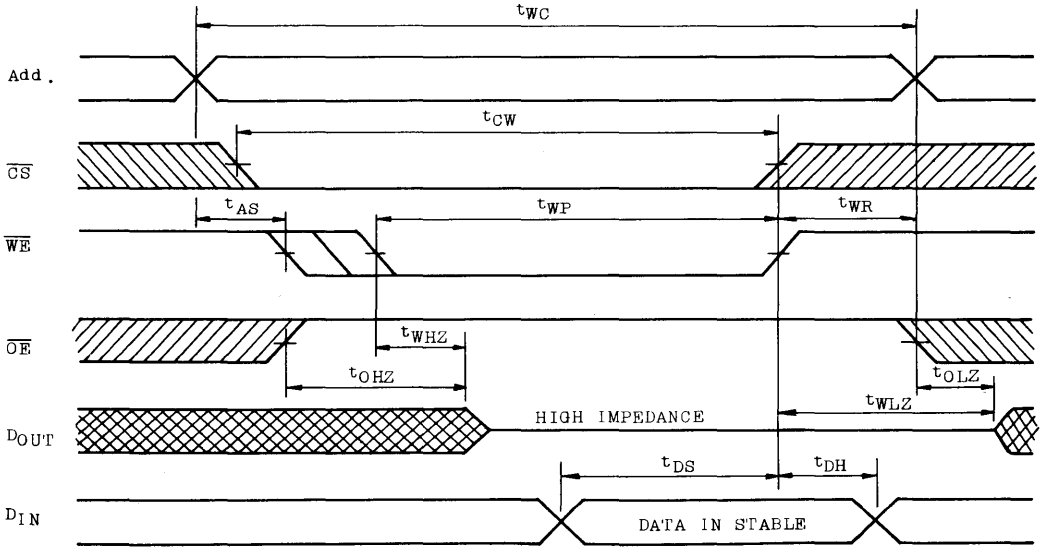
- Read Cycle 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



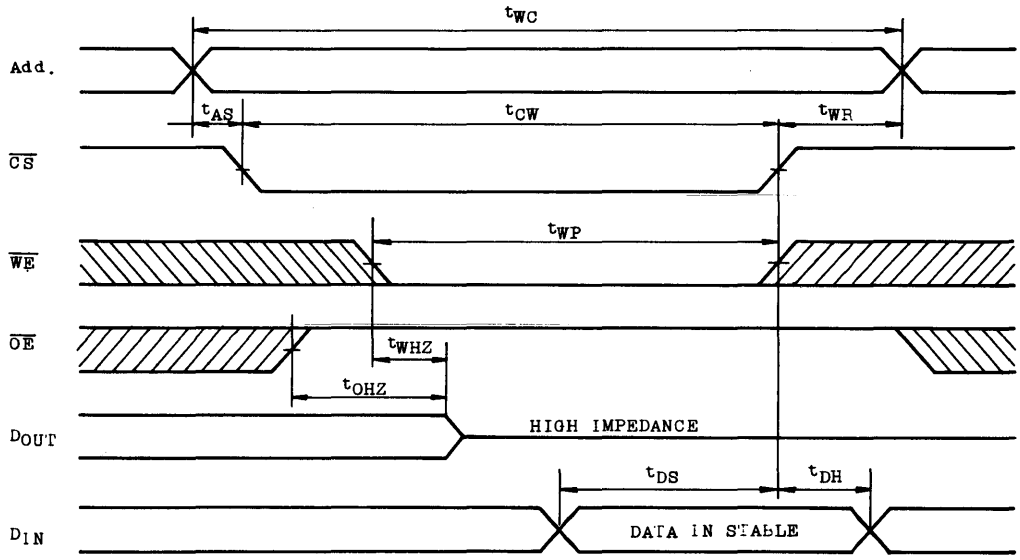
- Read Cycle 2. ($\overline{WE}$=V_{IH}, $\overline{OE}$=V_{IL})



- Write Cycle 1.



- **Write Cycle 2.**

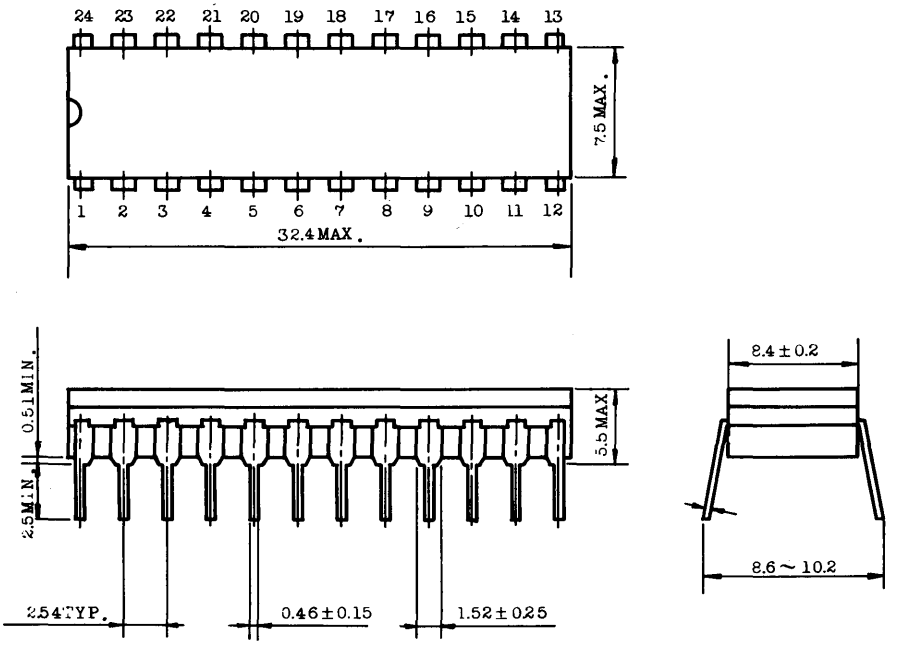


Note :

1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.
2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.

8,192 WORD × 9 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS
PRELIMINARY

TMM2089C-35, TMM2089C-45
TMM2089C-55

DESCRIPTION

The TMM2089C is a 73,728 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 9 bits and operates from a single 5-volt supply. The TMM2089C is features an automatic stand-by mode when deselect by $\overline{CS1}$ signal. Thus the TMM2089C is suitable for use in cache memory and high speed storage. The TMM2089C has nine I/O terminals, therefore it is most suitable for MEMORY SYSTEM with Parity bit. The TMM2089C is offered in a 28 pin standard ceramic dual in-line package with 0.3 inch width for high density assembly.

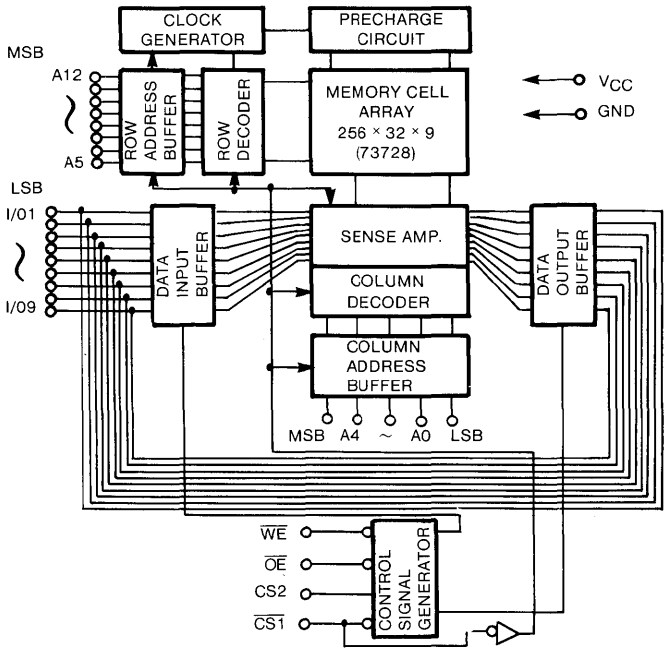
FEATURES

- Access Time and Current

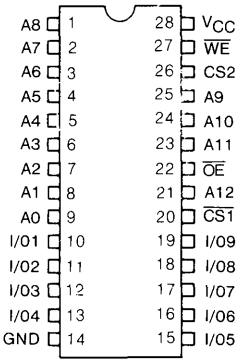
Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2089C-35	35ns	120mA	10mA
TMM2089C-45	45ns	120mA	10mA
TMM2089C-55	55ns	120mA	10mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: ($\overline{CS1}$)
- Output Buffer Control: ($\overline{OE}$)
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Compatible)
- Inputs Protected: (All inputs have protection against static charge.)

BLOCK DIAGRAM



PIN CONNECTION



PIN NAMES

SYMBOL	NAME
A0 ~ A12	Address Inputs
$\overline{CS1}$, CS2	Chip Select Input
$\overline{WE}$	Write Enable Input
I/01 ~ I/09	Data Input/Output
$\overline{CS1}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

OPERATION MODE

Mode	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/01 ~ I/09	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

* Don't Care

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−3.5~7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	−3.5~7.0	V
$T_{opr.}$	Operating Temperature	0~70	°C
$T_{stg.}$	Storage Temperature	−55~150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

*Pulse Width: 10ns, DC: −0.5V (Min.)

D.C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	-1.0	-1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-4.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	-	8.0	mA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	-1.0	1.0	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	-	30	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL}, I_{OUT}=0mA	-	10	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, I_{OUT}=0mA	-	120	mA

CAPACITANCE * (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	55	-	ns
t_{ACC}	Address Access Time	-	35	-	45	-	55	
t_{CO1}	$\overline{CS1}$ Access Time	-	35	-	45	-	45	
t_{CO2}	CS2 Access Time	-	25	-	25	-	30	
t_{OE}	$\overline{OE}$ Access Time	-	20	-	20	-	25	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	-	5	-	5	-	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	-	20	-	20	-	20	
t_{OLZ}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	
t_{OHZ}	Output Disable Time from $\overline{OE}$	-	10	-	10	-	15	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	30	-	30	-	30	

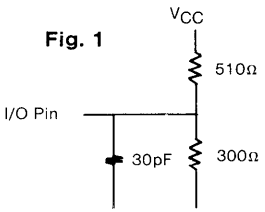
WRITE CYCLE

SYMBOL	PARAMETER	TMM2089C-35		TMM2089C-45		TMM2089C-55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	55	-	ns
t_{CW}	Chip Selection to End of Write	30	-	40	-	50	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	25	-	35	-	45	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	15	-	20	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	
t_{WLZ}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	
t_{WHZ}	Output Disable Time from $\overline{WE}$	-	10	-	10	-	15	

A.C. TEST CONDITIONS

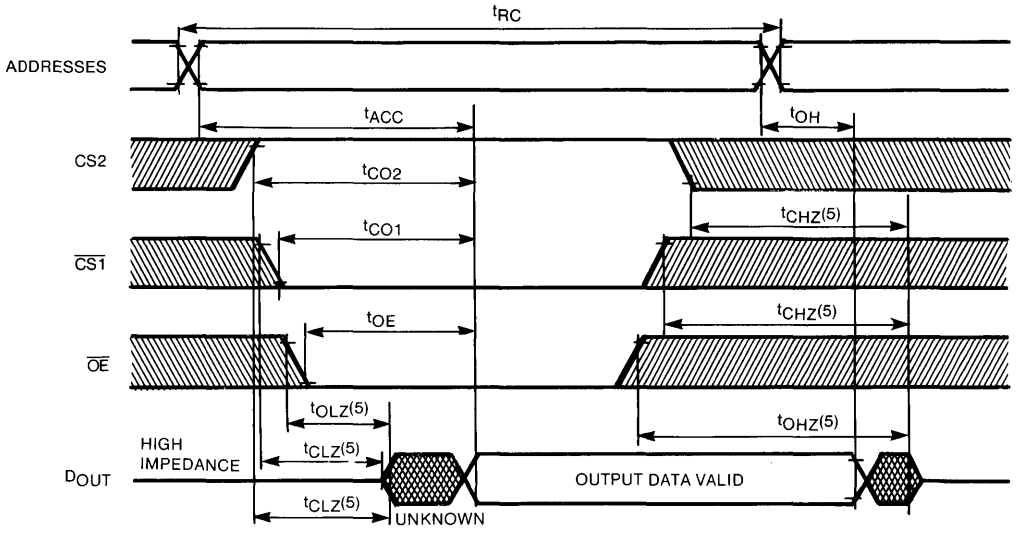
Input Pulse Levels	0.6~2.2V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

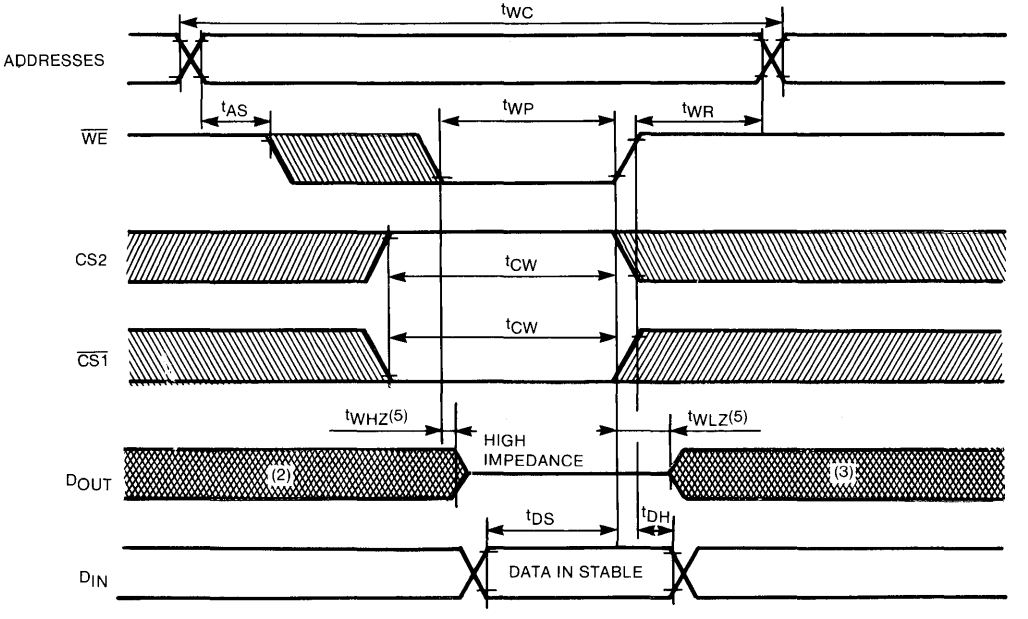


TIMING WAVEFORMS

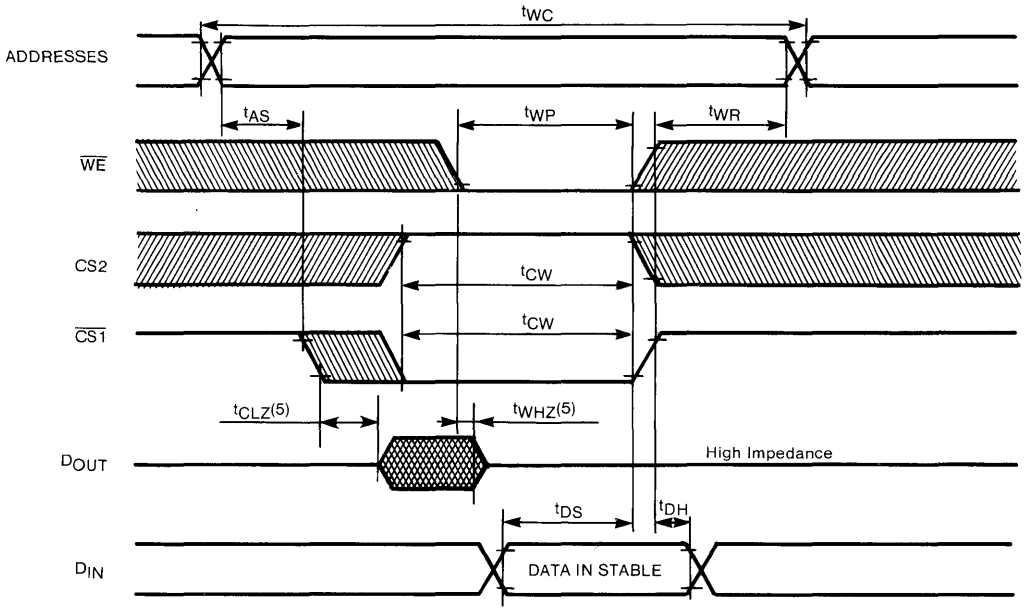
READ CYCLE (1)



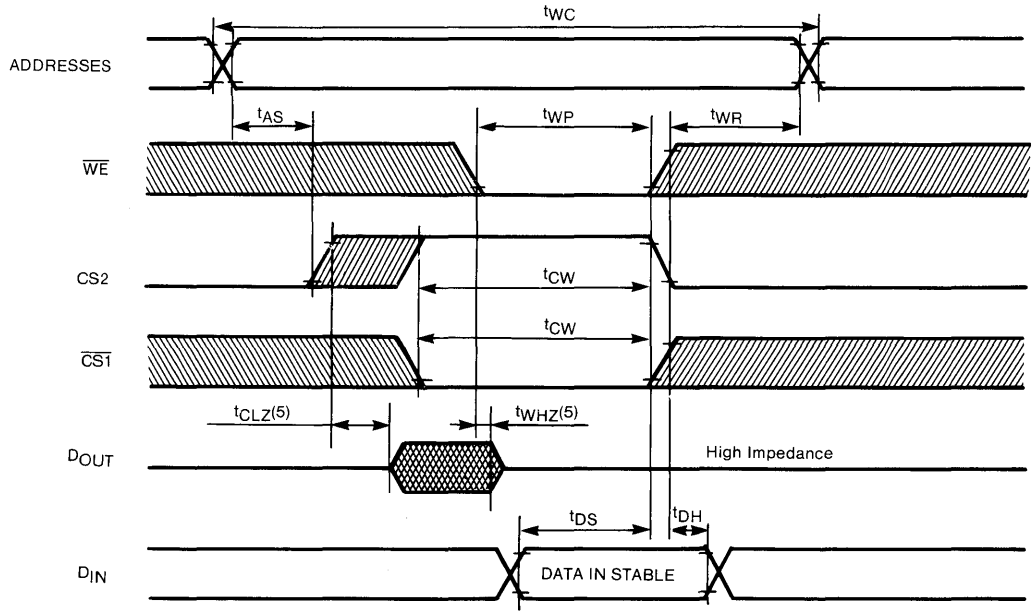
WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note:

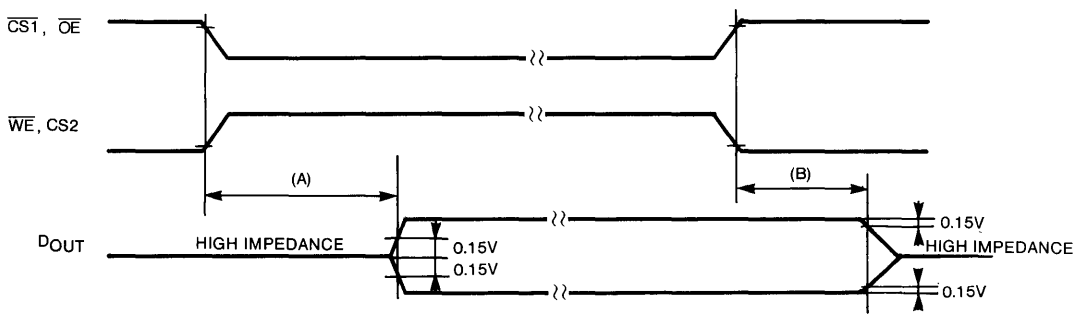
1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

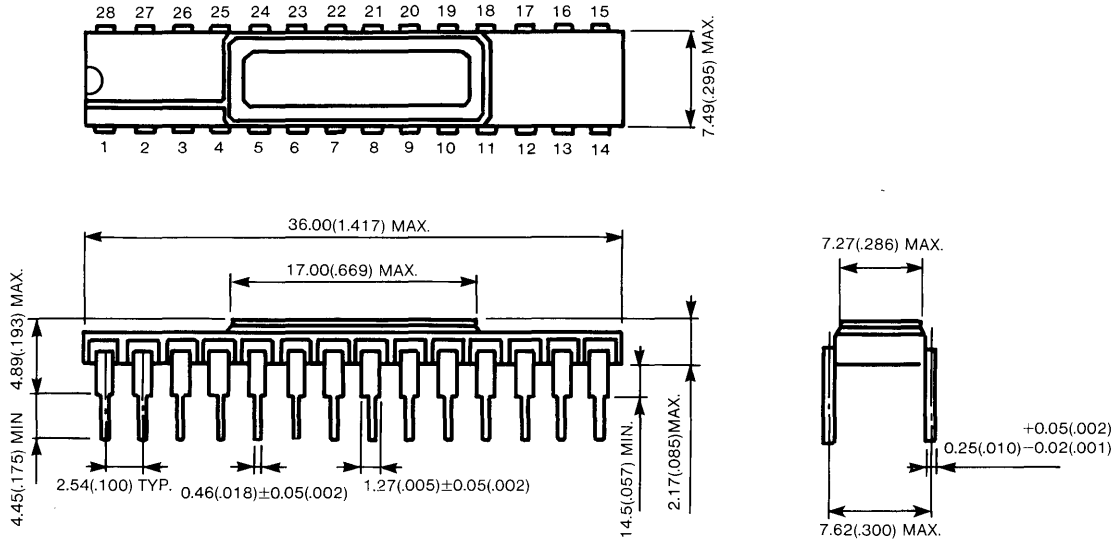
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time



OUTLINE DRAWINGS

Unit: mm (inches)



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their longitudinal position with respect No. 1 and No. 28 leads.

CMOS High Speed Static Random Access Memories

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5561P-55
TC5561P-70

PRELIMINARY

DESCRIPTION

The TC5561P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and Operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 55ns/70ns and maximum operating current of 100mA at minimum cycle time.

The TC5561P also features an automatic stand-by mode. When deselected by Chip Enable (CE), the operating current is reduced from 100mA to 100μA.

The TC5561P is suitable for use in main memory of high speed computer and pattern memory, where high speed/low power/high density are required.

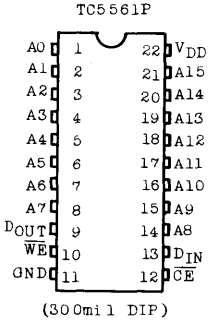
The TC5561P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

The TC5561P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

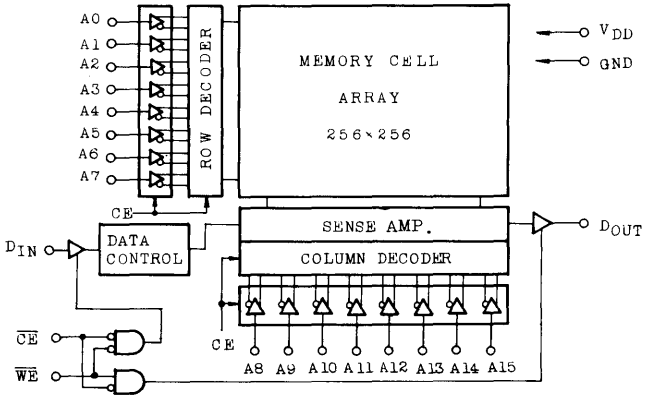
FEATURES

- Fast access time : TC5561P-55 55ns(MAX.)
  TC5561P-70 70ns(MAX.)
- Low power dissipation : Operation100mA(MAX.)
  Standby100μA(MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{15}	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{SOLDER}	Soldering Temperature	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V

D. C. and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IN}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$	—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$	−8	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0\sim V_{DD}$	—	—	±1.0	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, t_{cycle}=Min cycle, $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	—	—	100	mA
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$	—	—	2	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$	—	—	100	μA

CAPACITANCE

($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

(Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC5561P-55		TC5561P-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{ACC}	Address Access Time	—	55	—	70	
t_{CO}	Chip Enable Access Time	—	55	—	70	
t_{COE}	Chip Enable to Output in Low-Z	5	—	5	—	
t_{COD}	Chip Disable to Output in High-Z	—	30	—	30	
t_{OH}	Output Data Hold Time	5	—	5	—	

Write Cycle

SYMBOL	PARAMETER	TC5561P-55		TC5561P-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{WP}	Write Pulse Width	35	—	35	—	
t_{CW}	Chip Enable to End of Write	35	—	35	—	
t_{AS}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	$\overline{WE}$ to Output Low-Z	—	30	—	30	
t_{OEW}	$\overline{WE}$ to Output High-Z	5	—	5	—	
t_{DS}	Data Set up Time	35	—	35	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	0 ~ 3.5V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

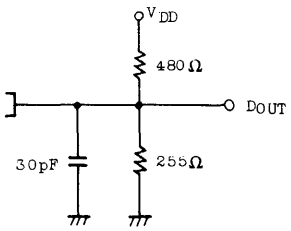
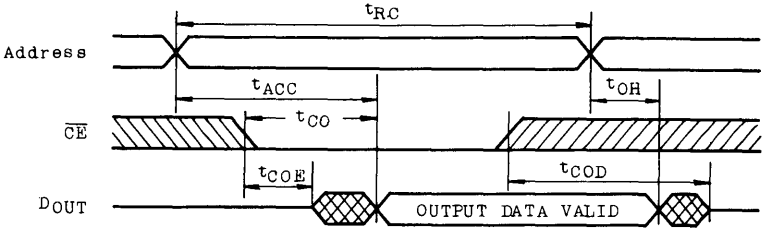


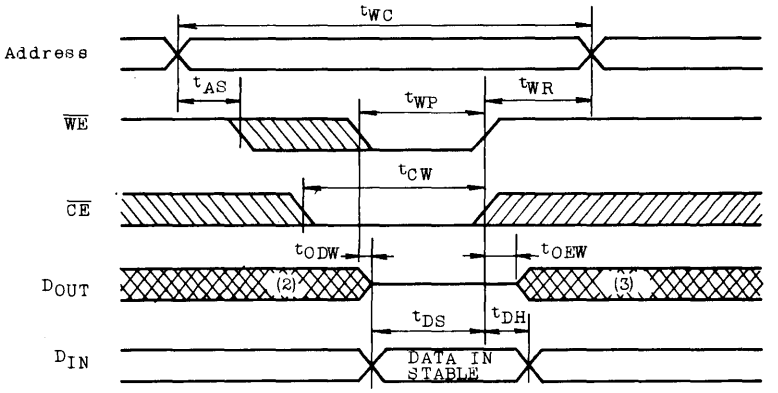
Fig.1 Output Load

TIMING WAVEFORMS

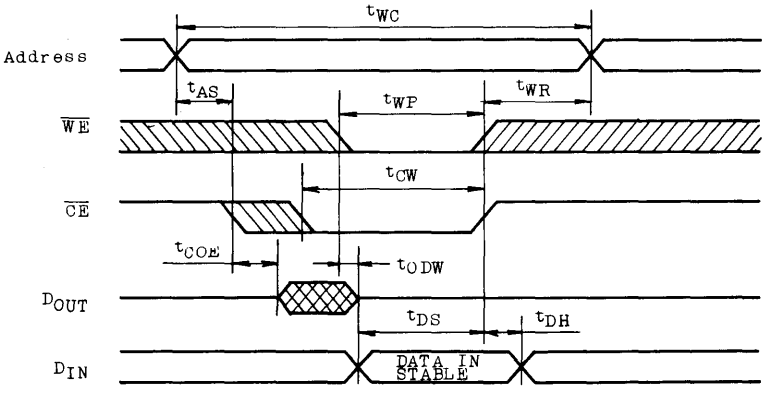
- READ CYCLE (1)



- WRITE CYCLE 1 ($\overline{WE}$ Controled Write)



- WRITE CYCLE 2 ($\overline{CE}$ Controled Write)

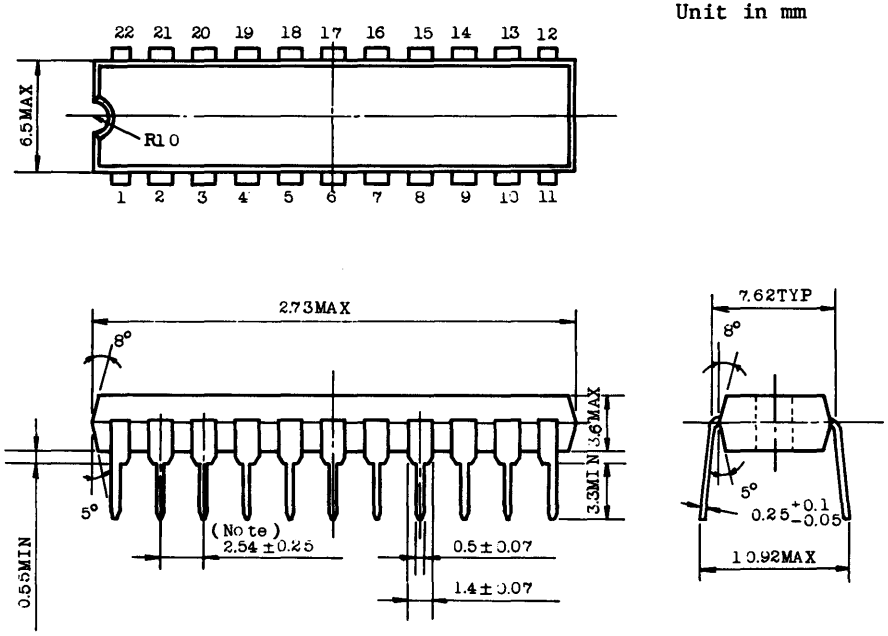


Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The operating temperature(Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5562P-45
TC5562P-55

PRELIMINARY

DESCRIPTION

The TC5562P is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 45ns/55ns and maximum operating current of 100mA at minimum cycle time.

The TC5562P also features and automatic stand-by mode. When deselected by chip Enable($\overline{CE}$), the operating current is reduced from 100mA to 20mA.

The TC5562P is suitable for use in main memory of high speed/high density are required.

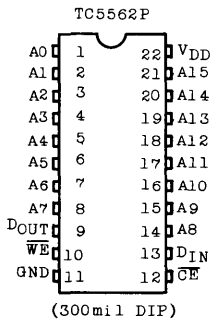
The TC5562P is moulded in a 22 pin standard plastic package with 0.3 inch width for high density assembly.

The TC5562P is fabricated with ion implanted COMS silicon gate MOS technology for high performance and high reliability.

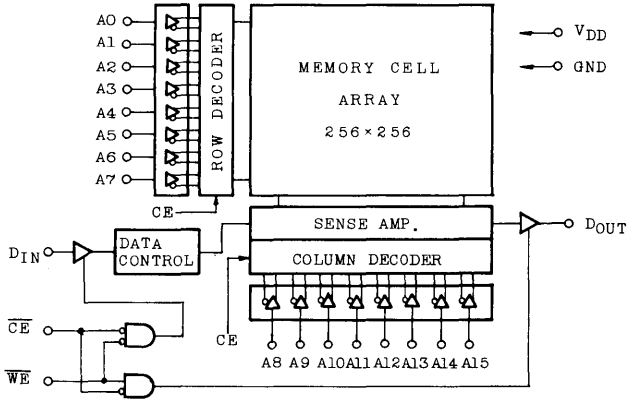
FEATURES

- Fast access time : TC5562P-45 45ns(MAX.)
  TC5562P-55 55ns(MAX.)
- Low power dissipation : Operation 100mA(MAX.)
  Standby 20mA(MAX.)
- 5V single power supply
- Fully Static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{15}$	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{SOLDER}	Soldering Temperature	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

D. C and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$	—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$	−8	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0\sim V_{DD}$	—	—	±1.0	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, tcycle=Min cycle, $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	—	—	100	mA
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$	—	—	20	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$ Other Input=$V_{DD}-0.2V$ or $0.2V$	—	—	2	

CAPACITANCE

($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC5562P-45		TC5562P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	45	—	55	—	ns
t_{ACC}	Address Access Time	—	45	—	55	
t_{CO}	Chip Enable Access Time	—	45	—	55	
t_{COE}	Chip Enable to Output in Low-Z	5	—	5	—	
t_{COD}	Chip Disable to Output in High-Z	—	25	—	30	
t_{OH}	Output Data Hold Time	5	—	5	—	

Write Cycle

SYMBOL	PARAMETER	TC5562P-45		TC5562P-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	45	—	55	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	
t_{CW}	Chip Enable to End of Write	30	—	35	—	
t_{AS}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	$\overline{WE}$ to Output Low-Z	—	25	—	30	
t_{OEW}	$\overline{WE}$ to Output High-Z	5	—	5	—	
t_{DS}	Data Set up Time	30	—	35	—	
t_{DH}	Data Hold Time	0	—	0	—	

A. C. TEST CONDITIONS

Input Pulse Levels	0~3.5V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

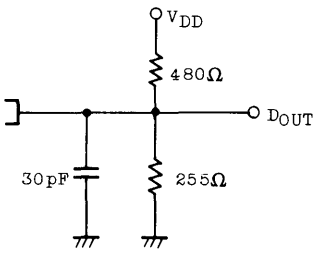
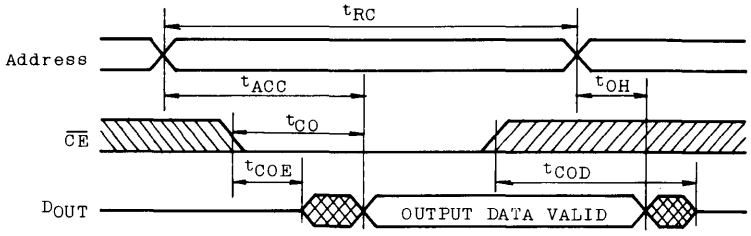


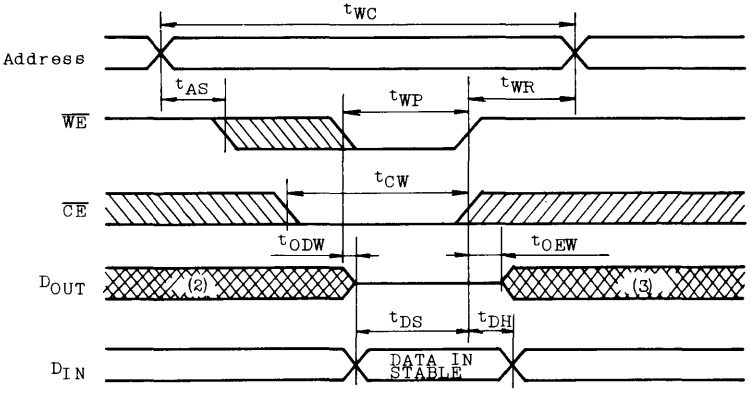
Fig.1 Output Load

TIMING WAVEFORMS

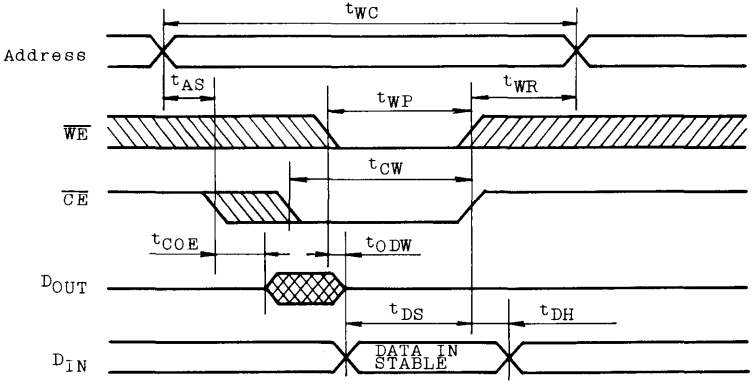
- READ CYCLE (1)



- WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

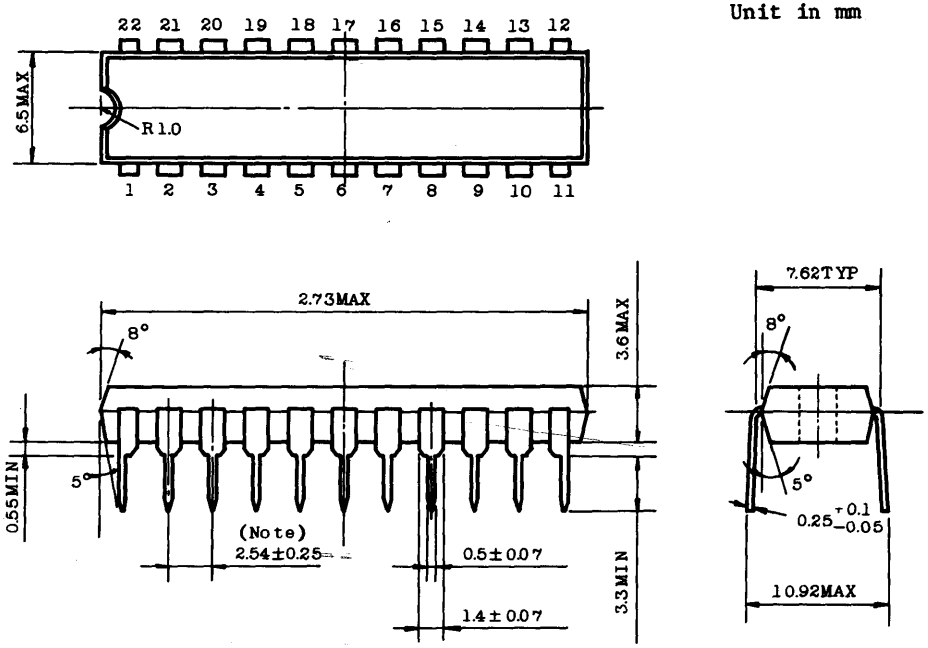


Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The operating temperature(Ta) in guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

NMOS Erasable Programmable Read Only Memories

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD×8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM2764D-15, TMM2764D-2 TMM2764D

DESCRIPTION

The TMM2764D is a 8192 word×8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764D's access time is 150ns(TMM2764D-15)/200ns (TMM2764D-2)/250ns(TMM2764D), and the TMM2764D operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

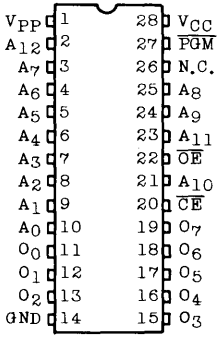
The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

The maximum active current is 100mA and the maximum standby current is 25mA. For program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the $\overline{PGM}$ input, and it is possible to program sequentially, individually, or at random.

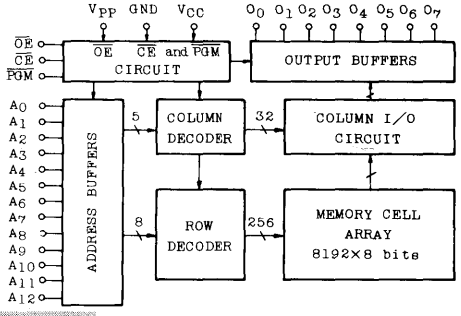
FEATURES

- Single 5-volt power supply
- Fast access time : TMM 2764D-15 : 150ns(Max.)
  TMM2764D-2 : 200ns(Max.)
  TMM2764D : 250ns(Max.)
- Power dissipation : 100mA (active current) Max.
  25mA (standby current) Max.
- Low Power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Fully static operation
- Programs with one 50ms pulse or high speed programming mode(2 types)
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 and ROM TMM2364P

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N. C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC}Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	21V	5V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~22.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−65~125	°C
$T_{OPR.}$	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS

(T_a=0~70°C, V_{CC}=5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	25	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS

(T_a=0~70°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V, Unless otherwise noted)

SYMBOL	PARAMETER	TMM2764D-15		TMM2764D-2		TMM2764D		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	—	100	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	—	0	—	0	—	ns

A. C. Test Conditions

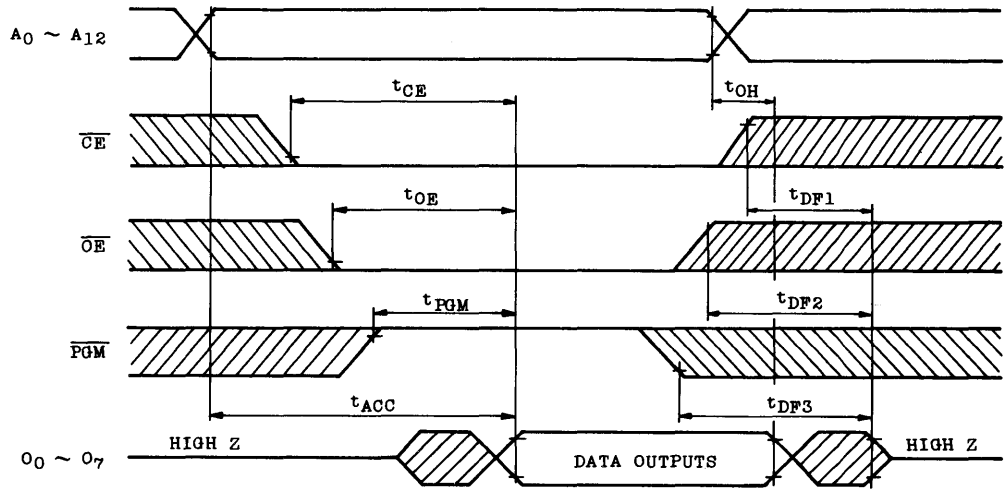
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.8V to 2.2V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25C°, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFROM (READ)



PROGRAM OPERATION

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=21.5V	—	—	30	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

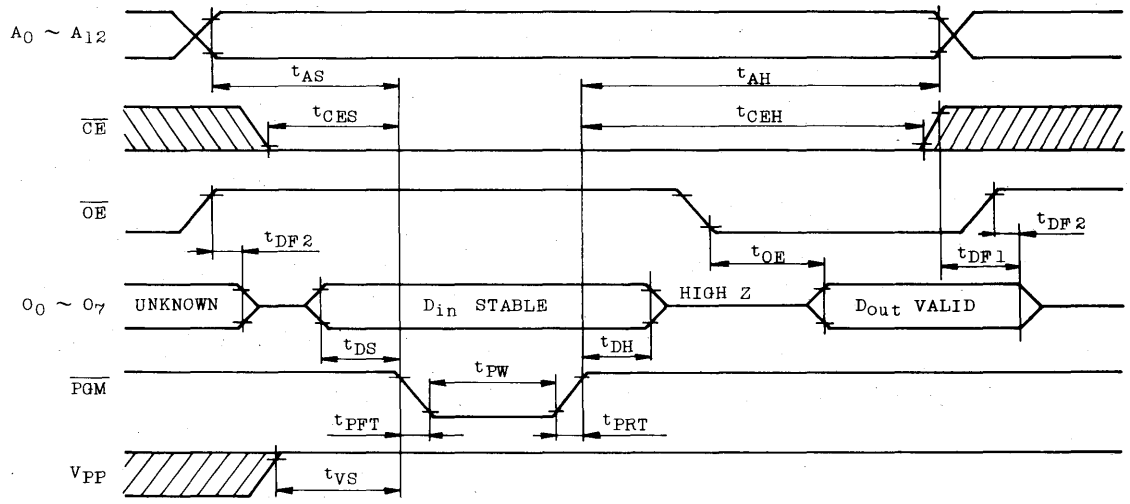
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{PS}	$\overline{PGM}$ Setup Time	—	2	—	—	μs
t_{PH}	$\overline{PGM}$ Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	$\overline{PGM} = \overline{CE} = V_{IL}$	45	50	55	ms
t_{CP}	Program Recovery Time	—	0	—	—	μs
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	—	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	—	—	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	90	ns

A. C. Test Conditions

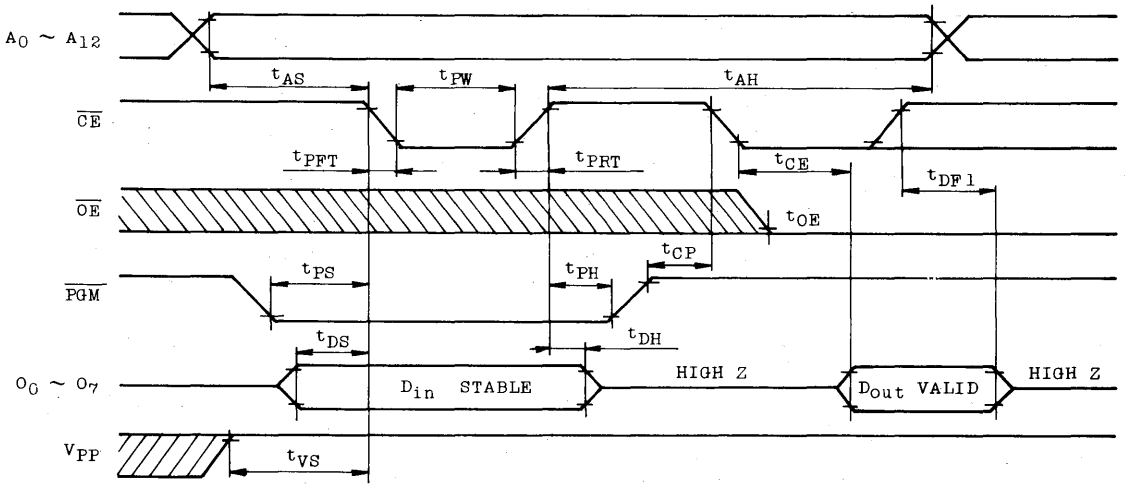
- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.8~2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and2.0V

TIMING WAVEFORMS (PROGRAM)

- PROGRAM OPERATION 1. (V_{PP}=21V±0.5V)



- PROGRAM OPERATION 2. (V_{PP}=21V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=21V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.

When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM2764D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W. sec/cm²] .

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²] .)

The TMM2764D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM2764D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	21V	5V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IL}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM2764D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM2764D can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM2764D is placed in the standby mode which reduce the operating current from 100mA to 25mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Intially, when received by customers, all bits of the TMM2764D are in the "1" state which is erased state.

Therefore the program operation is to introduce "Os" data into the desired bit locations by electrically programming.

The TMM2764D is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE}=\overline{PGM}=\overline{OE}=V_{IH}$.

The program operation occurs during the overlap of the $\overline{CE}$ low and the $\overline{PGM}$ low.

Then the programming is achieved by applying a 50ms (t_{pw}) active low program pulse to the $\overline{CE}$ or the $\overline{PGM}$ input after the addresses and data are stable. This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM2764D can be programmed any location at anytime——either individually, sequentially, or at random.

The TMM2764D should not be programmed with D. C. signal applied to both $\overline{CE}$ and $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The Verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764D from being programmed.

Programming of two or more TMM2764Ds in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE(2 TYPES)

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. A times)

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

TYPE 1 : A=15, B=4
TYPE 2 : A=20, B=1

HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25+5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=21V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=21.5V$	—	—	30	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=21V\pm0.5V$)

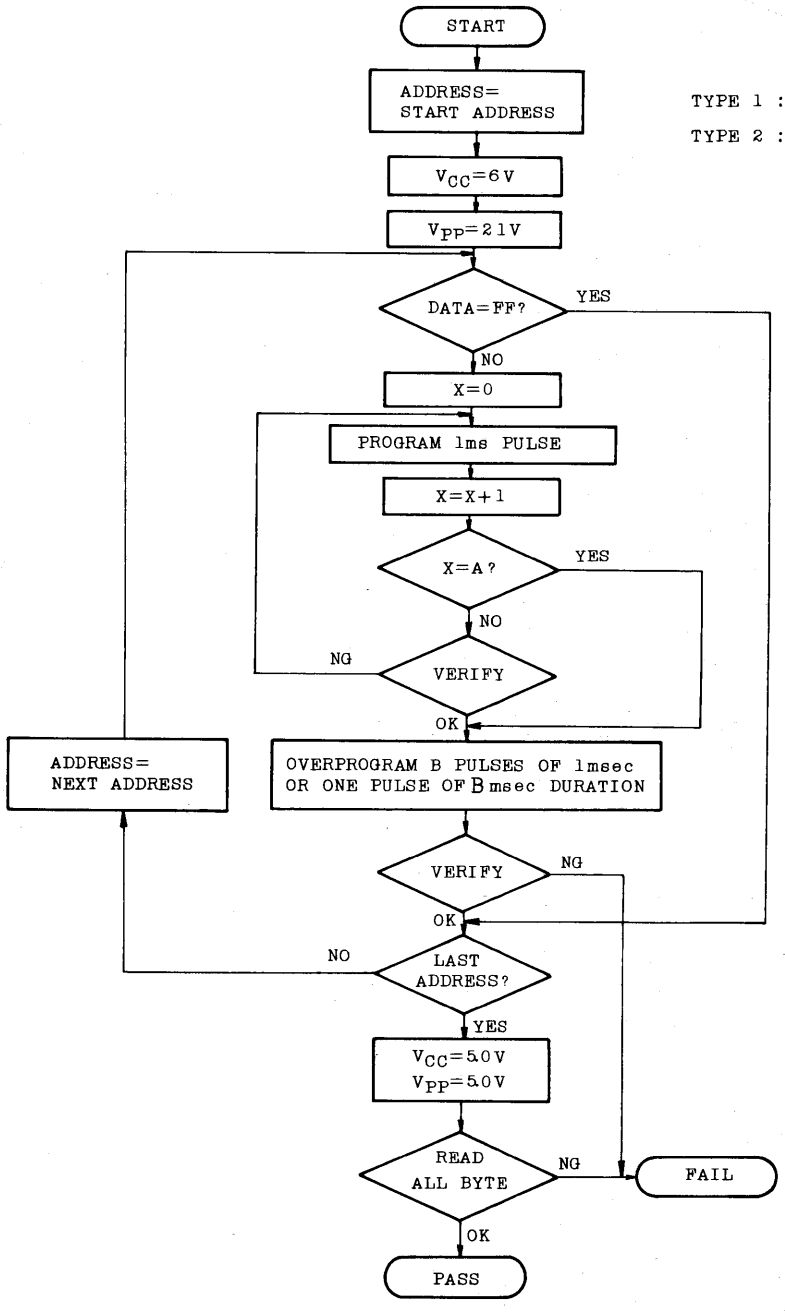
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	A	—	B	ms
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. Test Conditions

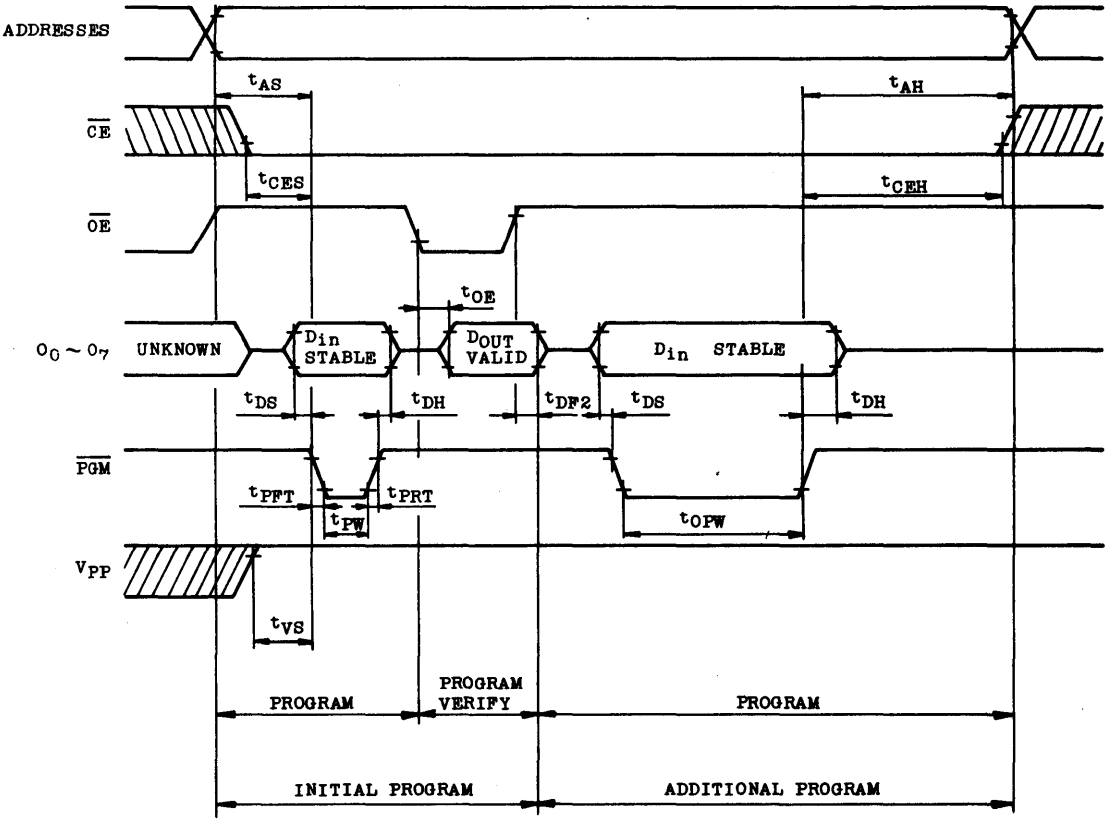
- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.8V and 2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t_{opw} depeds on the program pulse width which is required in the initail Program.
(TYPE 1 : A=3.8, B=63 TYPE 2 : A=0.95, B=21)

HIGH SPEED PROGRAM MODE FLOW CHART

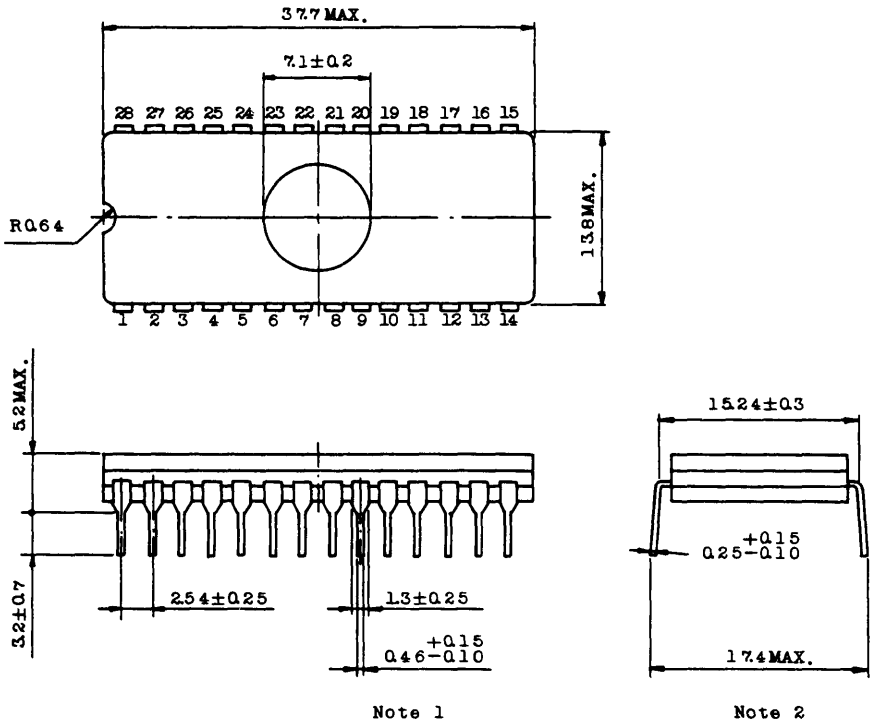


TIMING WAVEFORM (HIGH SPEED PROGRAM)



OUTLINE DRAWINGS

Unit in mm



Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied,, and Toshiba reserves the right, at any time without notice, to change said circuitry.

8,192 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM2764DI-15, TMM2764DI-2 TMM2764DI

DESCRIPTION

The TMM2764DI is a 8192 word×8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM 2764DI's access time is 150ns(TMM2764DI-15)/ 200ns(TMM2764DI-2)/250ns(TMM2764DI), and the TMM2764DI operates from a single 5-Volt power supply and has low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved applying a TTL-high level signal to the $\overline{CE}$ input.

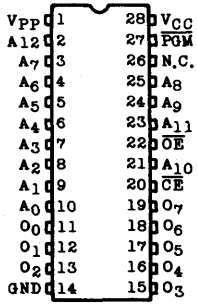
The maximum active current is 100mA and the maximum standby current is 25mA.

For program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the $\overline{PGM}$ input, and it is possible to program sequencially, individually, or at random.

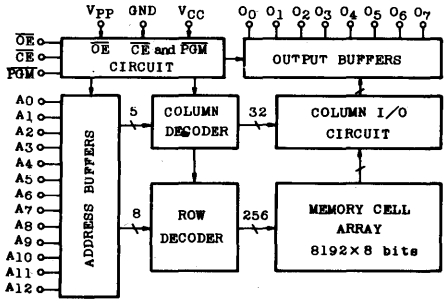
FEATURES

- Wide operating temperature range : −40~85°C
- Single 5-volt power supply
- Fast access time: TMM2764DI-15: 150ns(Max.)
  TMM2764DI-2: 200ns(Max.)
  TMM2764DI : 250ns(Max.)
- Power dissipation : 100mA (active current) Max.
  25mA (standby current) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Fully static operation
- Programs with one 50ms pulse or high speed programming mode(2 types)
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764 and ROM TMM2364P

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{12}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N. C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	21V	5V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~22.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STRG}	Storage Temperature	−65~125	°C
$T_{OPR.}$	Operating Temperature	−40~85	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	—	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.2	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS

(T_a=−40~85°C, V_{CC}=5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	25	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS

(T_a=−40~85°C, V_{CC}=5V±5%, V_{PP}=2.2V~V_{CC}+0.6V, Unless otherwise noted)

SYMBOL	PARAMETER	TMM2764DI-15		TMM2764DI-2		TMM2764DI		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	—	100	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	0	—	ns

A. C. Test Conditions

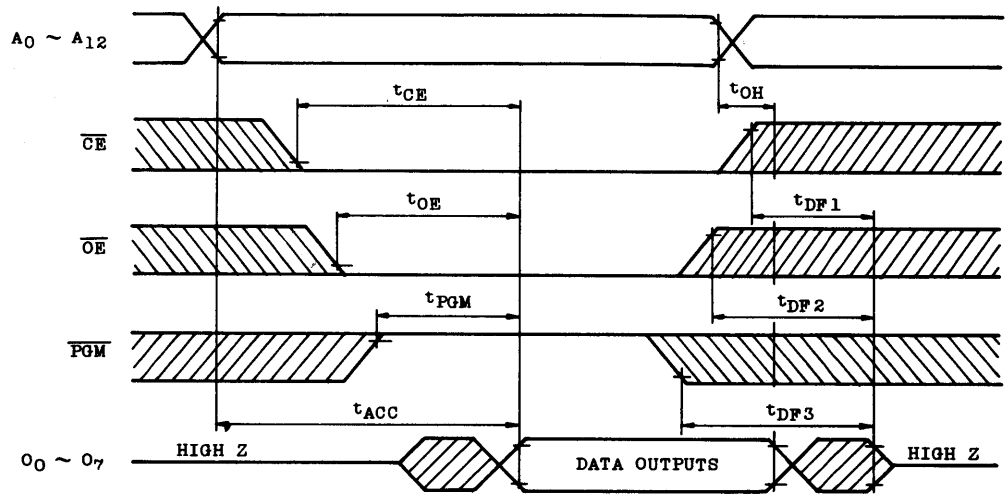
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25C°, f=1MHz)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=OV	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=OV	—	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=21.5V	—	—	30	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

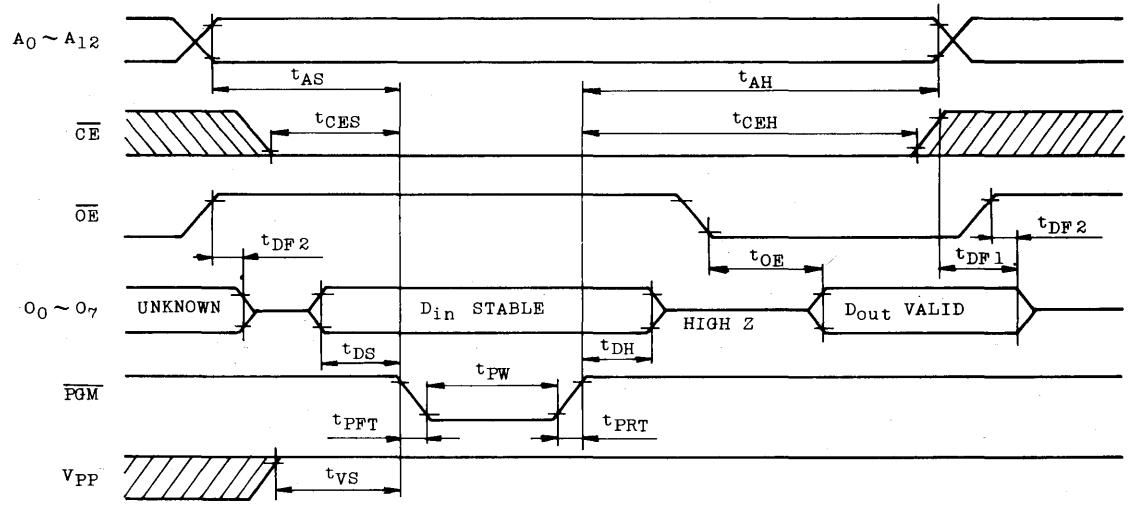
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{PS}	$\overline{PGM}$ Setup Time	—	2	—	—	μs
t_{PH}	$\overline{PGM}$ Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	$\overline{PGM} = \overline{CE} = V_{IL}$	45	50	55	ms
t_{CP}	Program Recovery Time	—	0	—	—	μs
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	—	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	—	—	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	—	—	90	ns

A. C. Test Conditions

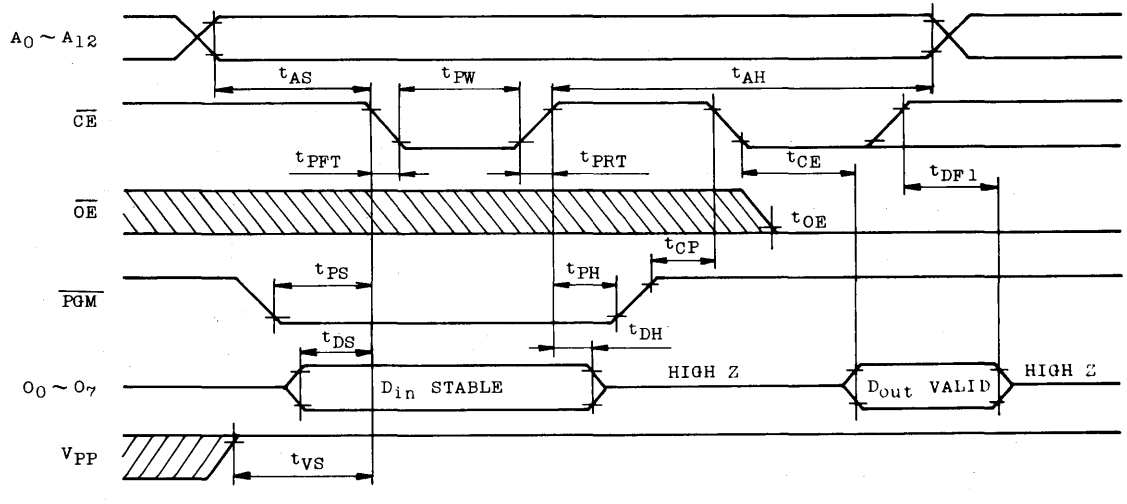
- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.6~2.4V
- Timing Meausrement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

- PROGRAM OPERATION 1. (V_{PP}=21V±0.5V)



- PROGRAM OPERATION 2. (V_{PP}=21V±0.5V)



Note: 1. V_{CC} must be applied simulataneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP} = 21V may cause permanent damage to the device,
3. The V_{PP} supply Voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM2764DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537A (Angstroms) to the chip through the transparent window.

Then integrated dose (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w. sec/cm²]

When the Toshiba sterilizing GL-15 is used and the device is exposed at a distance of 1 cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20 × 60) [sec] ≒ 15 [w.sec/cm²] .)

The TMM2764DI's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the flourescent lamps will include 3000~4000A wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM2764DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=−40~85°C)	Read	H	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	21V	5V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM2764DI has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM2764DI can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764DI has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM2764DI is placed in the standby mode which reduce the operating current from 100mA to 25mA, and then the outpus are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "Os" data into the desired bit locations by electrically programming.

The TMM2764DI is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE}=\overline{PGM}=\overline{OE}=V_{IH}$.

The program operation occurs during the overlap of the $\overline{CE}$ low and the $\overline{PGM}$ low.

Then the programming is achieved by applying a 50ms (t_{pw}) active low program pulse to the $\overline{CE}$ or the $\overline{PGM}$ input after the addresses and data are stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM 2764DI can be programmed any location at anytime —— either individually, sequentially, or at random.

The TMM2764DI should not be programmed with D. C. signal applied to both $\overline{CE}$ and $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGARM INHIBIT MODE

Under the condition that the program voltage (± 21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764DI from being programmed.

Programming of two or more TMM2764DIs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE(2 TYPES)

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. A times)

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

TYPE 1 : A=15, B=4
TYPE 2 : A=20, B=1

HIGH SPEED PROGRAM OFERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=21V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$ •	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=21.5V$	—	—	30	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=21V\pm0.5V$)

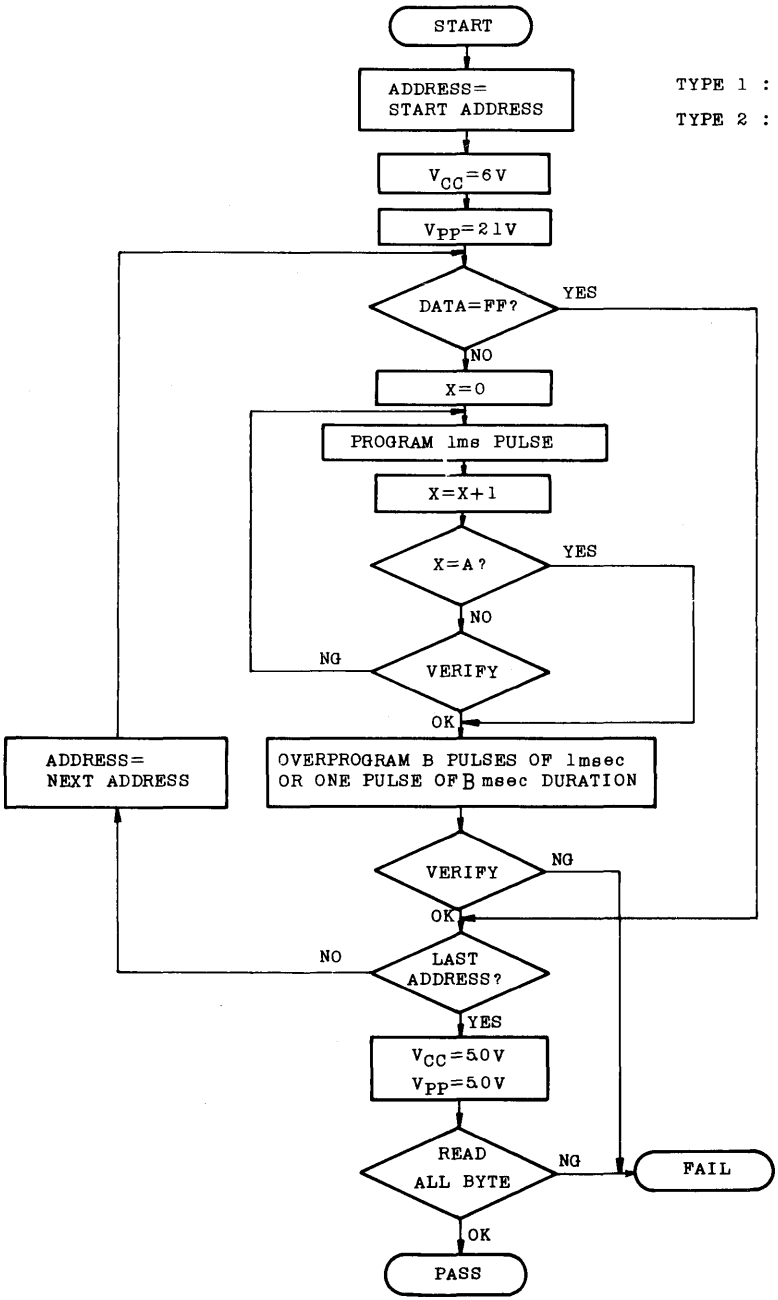
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	A	—	B	ms
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. Test Conditions

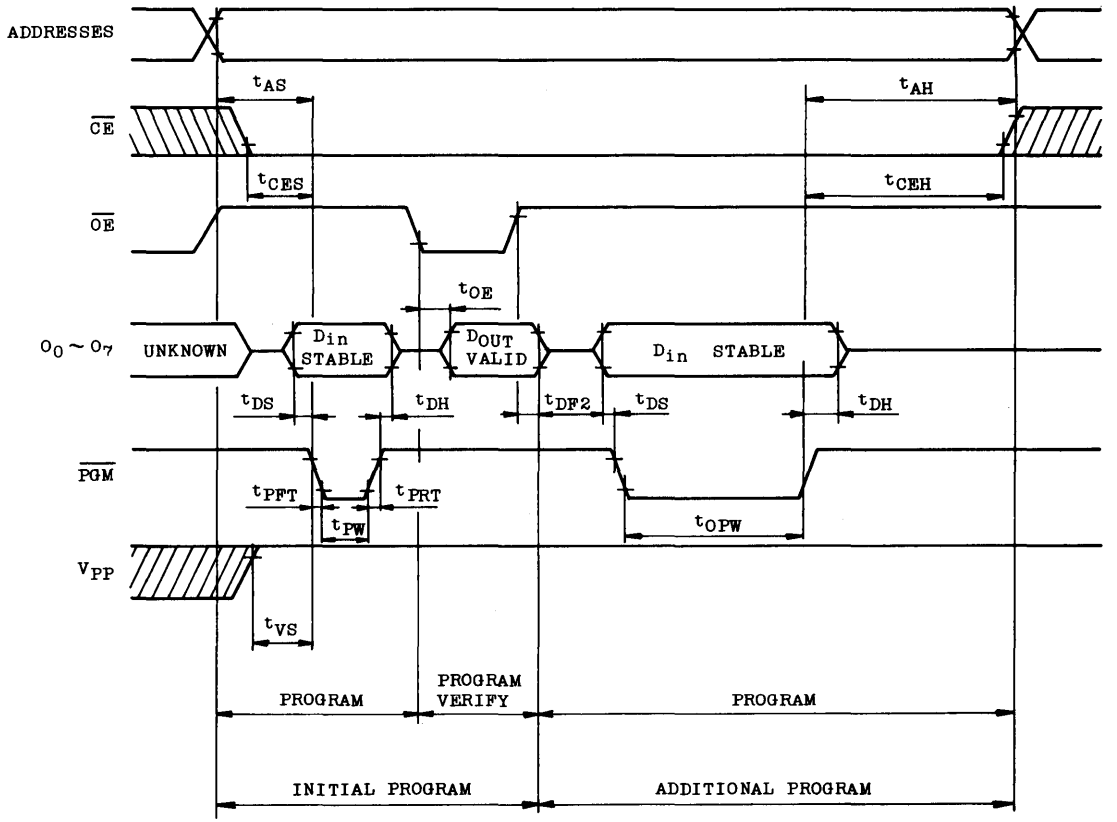
- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.6V and 2.4V
- Timing Measurement Referene Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note: 1. t_{opw} **depends on the program pulse width which is required in the initial Program.**
(TYPE 1 : A=3.8, B=63, TYPE 2 : A=0.95, B=21)

HIGH SPEED PROGRAM MODE FLOW CHART

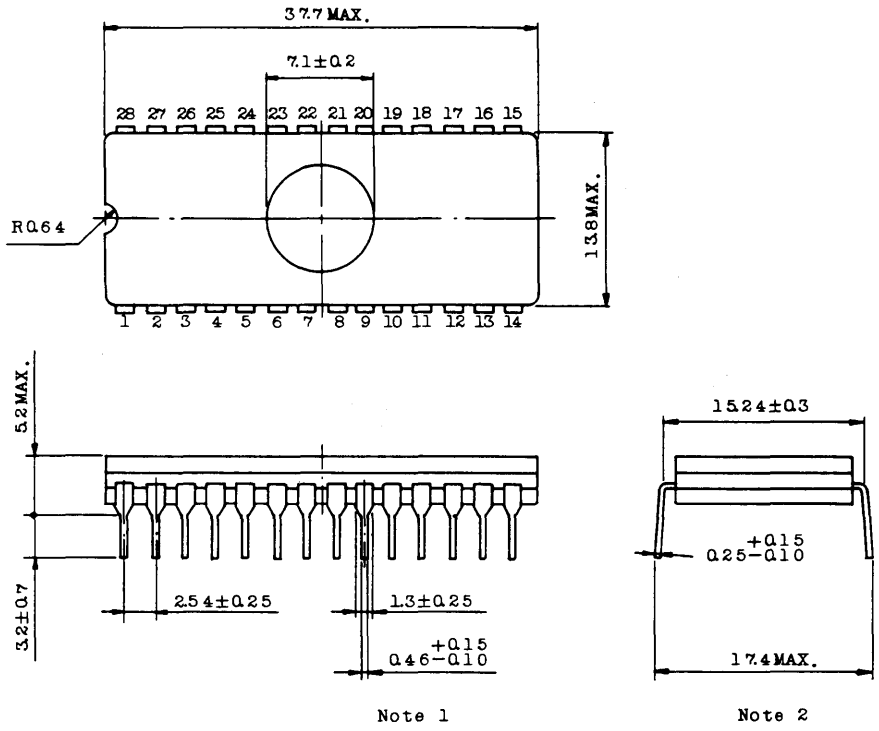


TIMING WAVEFORM (HIGH SPEED PROGRAM)



OUTLINE DRAWINGS

Unit in mm



Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY PRELIMINARY

N CHANNEL SILICON STACKED GATE MOS

TMM2764AD-15, TMM2764AD-150
TMM2764AD-20, TMM2764AD-200

DESCRIPTION

The TMM2764AD Is a 8192 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764AD's access time is 150ns/200ns, and the TMM2764AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. The maximum active current is 100mA and the maximum standby current is 30mA. For program operation, the programming is achieved by using the high speed programming mode. The TMM2764AD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

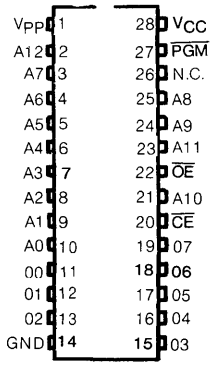
	-15	-20	-150	-120
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA			
I_{CC1}	30mA			

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764A

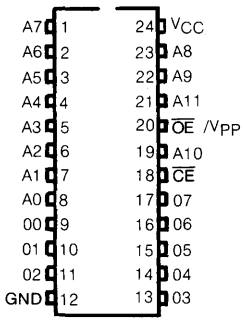
PIN CONNECTION

(TOP VIEW)

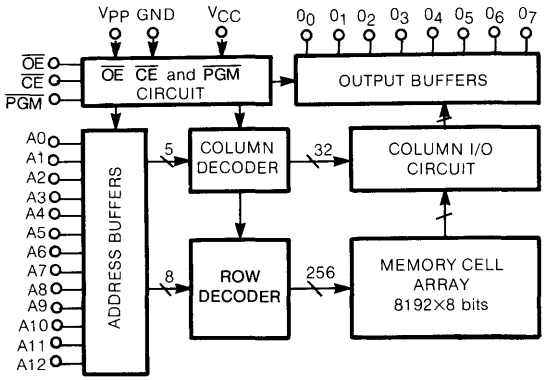
Lower 24 pins compatible with 32 bit EPROM TMM2732D



TMM2732D (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ~ A13	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* Don't Care

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM2764AD-15/20	TMM2764AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}+0.6V	2.0~V_{CC}+0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-	-	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-	-	100	mA
V_{IH}	Input High Voltage	-	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-	-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM2764AD-15/150		TMM2764AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	
t_{PGM}	$\overline{PGM}$ to Output Valid	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output High-Z	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output High-Z	0	60	0	60	
t_{DF3}	PGM to Output High-Z	0	60	0	60	
t_{OH}	Output Data Hold Time	0	-	0	-	

AC TEST CONDITIONS

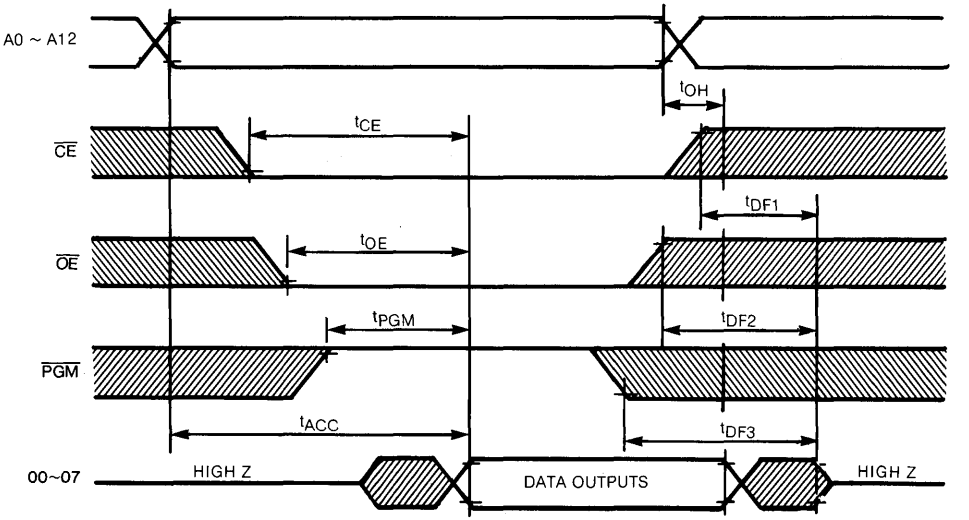
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage		6.0*		V
V_{PP}	Vpp Power Supply Voltage	12.0	12.5	13.0	V

* -150/200 ± 10%; -15/20±5%

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{DD}=6V±0.25V, Vpp=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	100	mA
I_{PP2}	Vpp Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, Vpp=12.5V±0.5V)

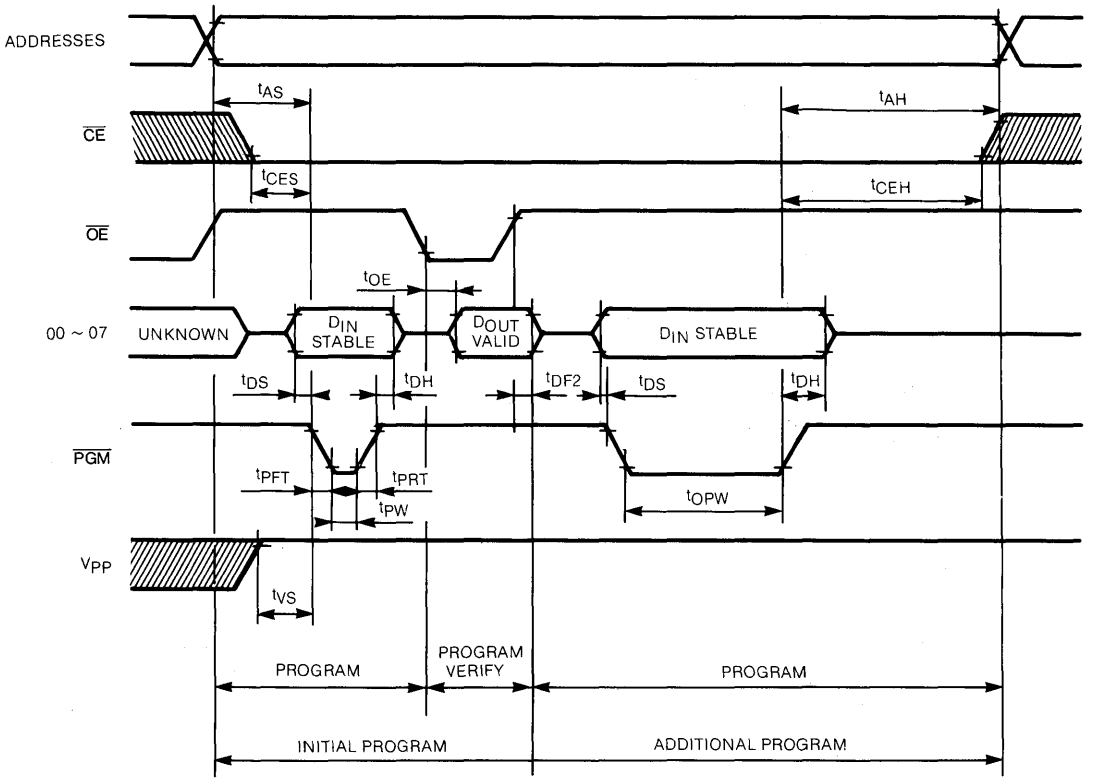
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	Vpp Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	-	78.75	ms
t_{PRT}	Program Pulse Rise Time	-	5	-	-	ns
t_{PFT}	Program Pulse Fall Time	-	5	-	-	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input/Output 0.8V and 2.0V

Note 1: t_{opw} depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS (HIGH SPEED PROGRAM)



Note:

1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket or setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so a voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TMM2764AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w sec/cm].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. Using commercial lamps whose ultraviolet light intensity is 12000 [μw · cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] × (20 × 60) [sec] ≅ 15 [w · sec/cm²].)

The TMM2764AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TMM2764AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES (Number)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM2764AD has three control functions. The chip enable ($\overline{CE}$) controls the operational power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the outputs after address access time from the stabilization of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

When $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM2764AD can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM2764AD Is placed in the standby mode which reduces the operating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Intially, when received by customers, all bits of the TMM2764AD are in the "1' state which is the erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TMM2764AD locations can be programmed either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed into the device.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that a program voltage (12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764AD from being programmed.

Programming of two or more TMM2764ADs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ or $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}.

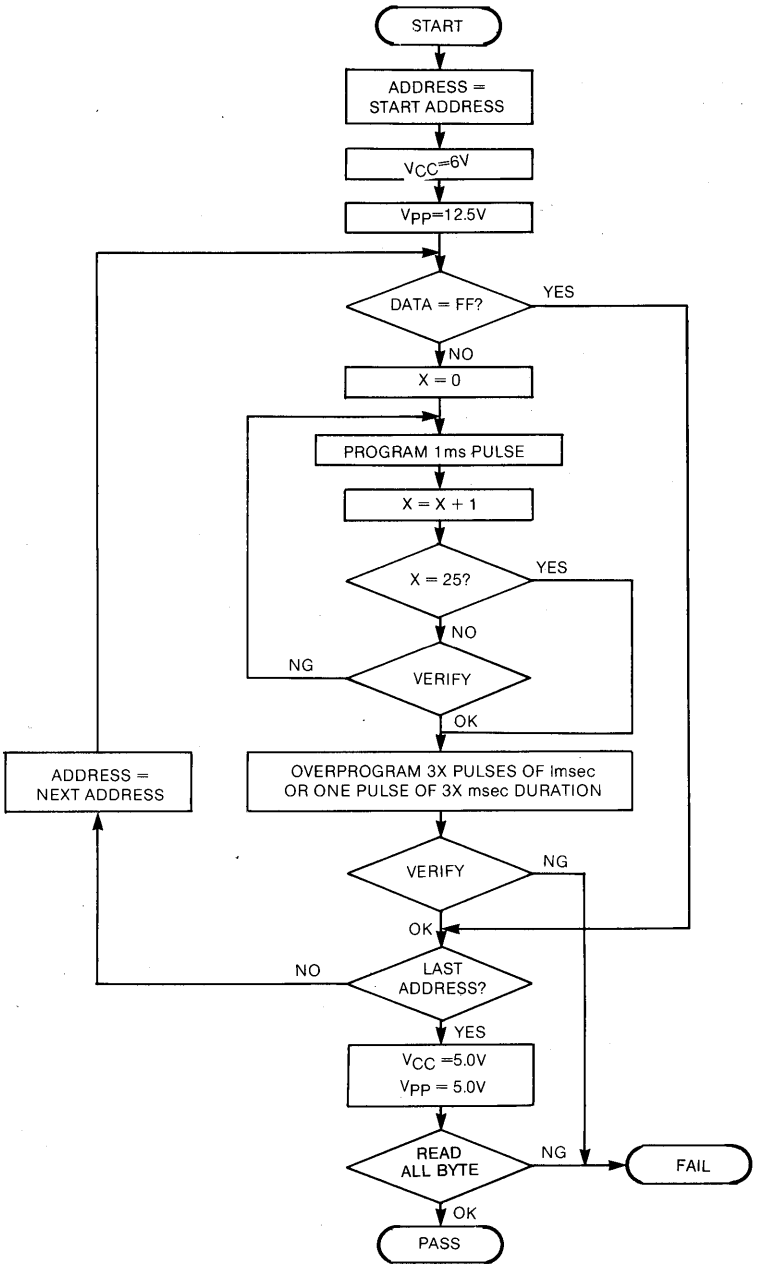
The programming is achieved by applying a single TTL low level 1ms pulse to $\overline{CE}$ input after addresses and data are stable. Then the programmed data are verified using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program verifies (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows reading out a code from the TMM2764AD which identifies its manufacturer and device type.

The programming equipment may read out manufacturer and device code from the TMM2764AD by using this mode before program operation to automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

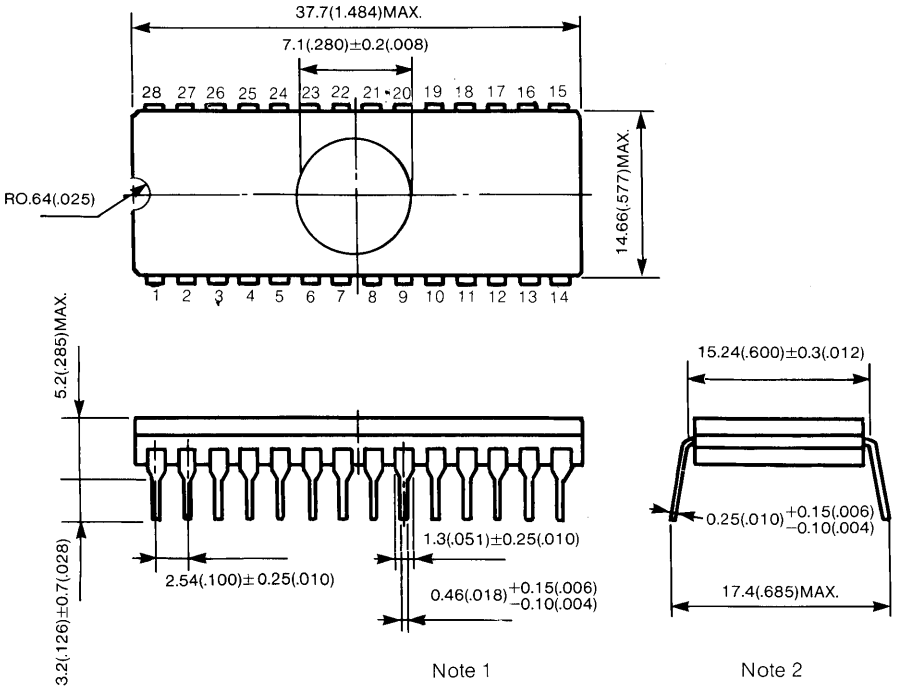
The following table shows electric signature of TMM2764AD.

PINS / SIGNATURE	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	0	1	0	52

Notes: A9=12V±0.5V
A1~A8, A10~A12, $\overline{CE}$, $\overline{OE}$=V_{IL}
$\overline{PGM}$=V_{IH}

OUTLINE DRAWINGS

Unit in mm (inches)



Note:

1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.

2. This value is measured at the end of leads.

TOSHIBA MOS MEMORY PRODUCTS

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM27128D-15, TMM27128D-20 TMM27128D-25

DESCRIPTION

The TMM27128D is a 16384 word ×8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM 27128D's access time is 150ns/200ns/250ns, and the TMM27128D operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

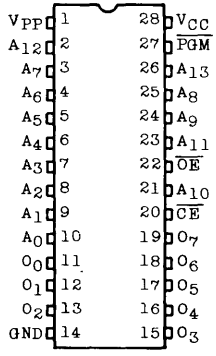
The maximum active current is 100mA and the maximum standby current is 25mA.

For program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the $\overline{PGM}$ input, and it is possible to program sequentially, in individually, or at random.

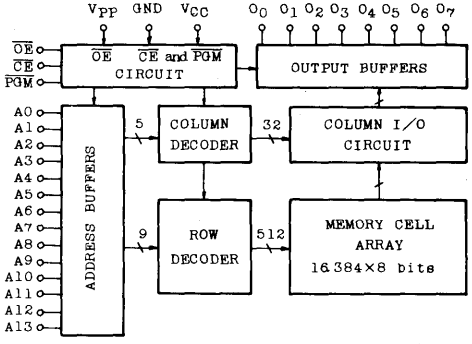
FEATURES

- Single-5Volt power supply
- Fast access time : TMM27128D-15 150ns
  TMM27128D-20 200ns
  TMM27128D-25 250ns
- Power dissipation : 100mA (active current) Max.
  25mA (standby current) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Fully static operation
- Programs with one 50ms pulse or high speed programming mode(2 types)
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	21V	5V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~22.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−65~125	°C
$T_{OPR.}$	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS

(T_a=0~70°C, V_{CC}=5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	25	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS

(T_a=0~70°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V, Unless otherwise noted)

SYMBOL	PARAMETER	TMM27128D-15		TMM27128D-20		TMM27128D-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	—	100	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	—	0	—	0	—	ns

A. C. Test Conditions

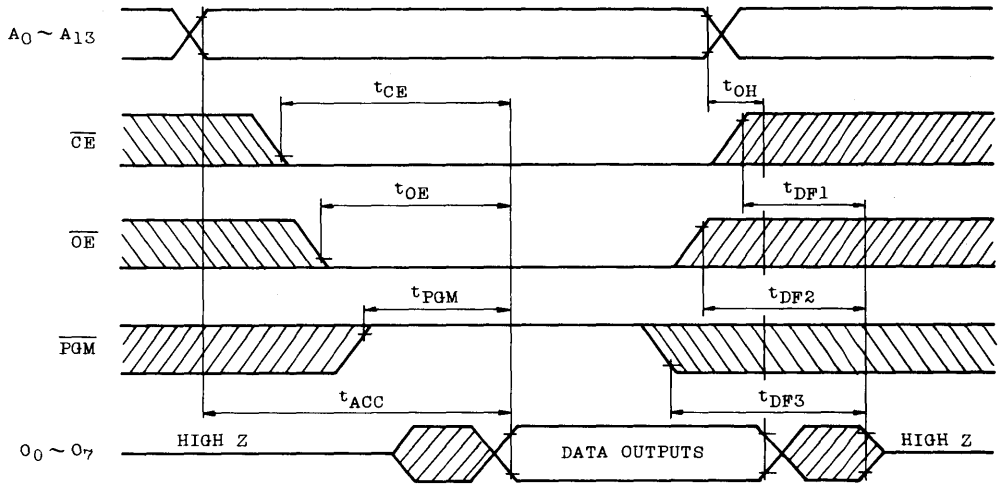
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Iput Pulse Levels : 0.8V to 2.2V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	—	8	12	pF

* This paramater is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=21.5V	—	—	30	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

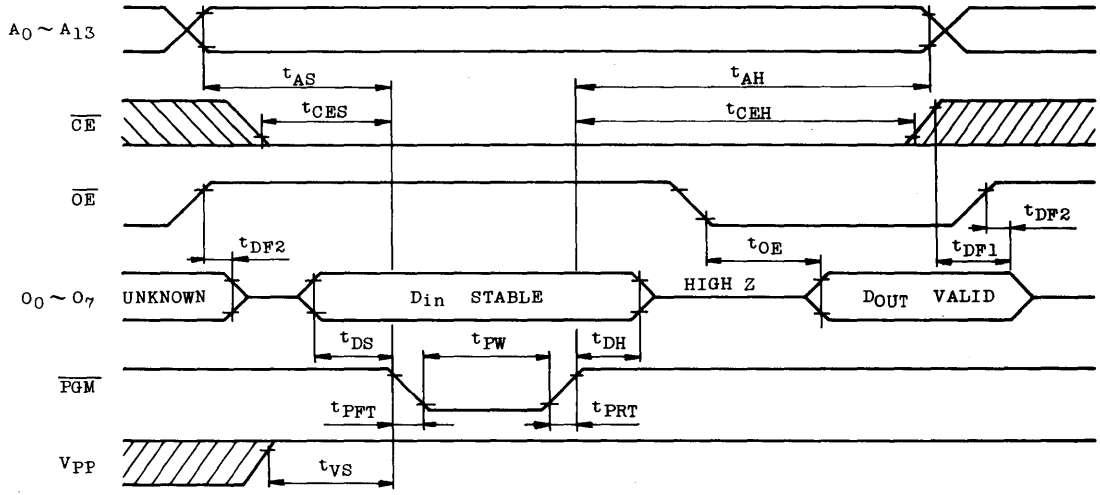
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{PS}	$\overline{PGM}$ Setup Time	—	2	—	—	μs
t_{PH}	$\overline{PGM}$ Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	$\overline{PGM} = \overline{CE} = V_{IL}$	45	50	55	ms
t_{CP}	Program Recovery Time	—	0	—	—	μs
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	—	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High Z	$\overline{OE} = V_{IL}$	—	—	90	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE} = V_{IL}$	—	—	90	ns

A. C. Test Conditions

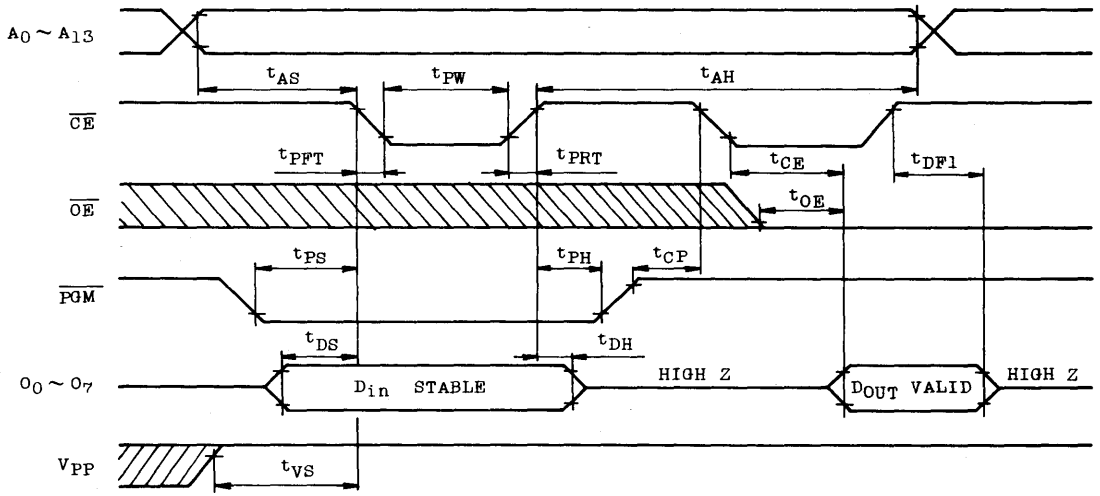
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.8V and 2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

- PROGRAM OPERATION 1. (V_{PP}=21V±0.5V)



- PROGRAM OPERATION 2. (V_{PP}=21V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=21V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM27128D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated does (Ultraviolet light intensity [w/cm²] ×exposure time [sec.]) for erasure should be a minimum of 15 [w. sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] ×(20×60) [sec] ≅15 [w·sec/cm²] .)

The TMM27128D's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the flourescent lamps will include 3000~4000A wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27128D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	21V	5V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IH}, L : : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM 27128D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in high impedance state.

So two or more TMM27128D can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM27128D is placed in the standby mode which reduce operating current from 100mA to 25mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TMM27128D is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE}=\overline{PGM}=\overline{OE}=V_{IH}$.

The program operation occurs during the overlap of the $\overline{CE}$ low and the $\overline{PGM}$ low.

Then the programming is achieved by applying a 50ms (t_{pw}) active low program pulse to the $\overline{CE}$ or the $\overline{PGM}$ input after the addresses and data stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM27128D can be programmed any location at anytime —— either individually, sequentially, or at random.

The TMM27128D should not be programmed with D. C. signal applied to both $\overline{CE}$ and $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128D from being programmed.

Programming of two or more TMM27128Ds in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE (2 TYPES)

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. A times)

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

TYPE 1 : A=15, B=4
TYPE 2 : A=20, B=1

HIGH SPEED RPOGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=21V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=21.5V$	—	—	30	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=21V\pm0.5V$)

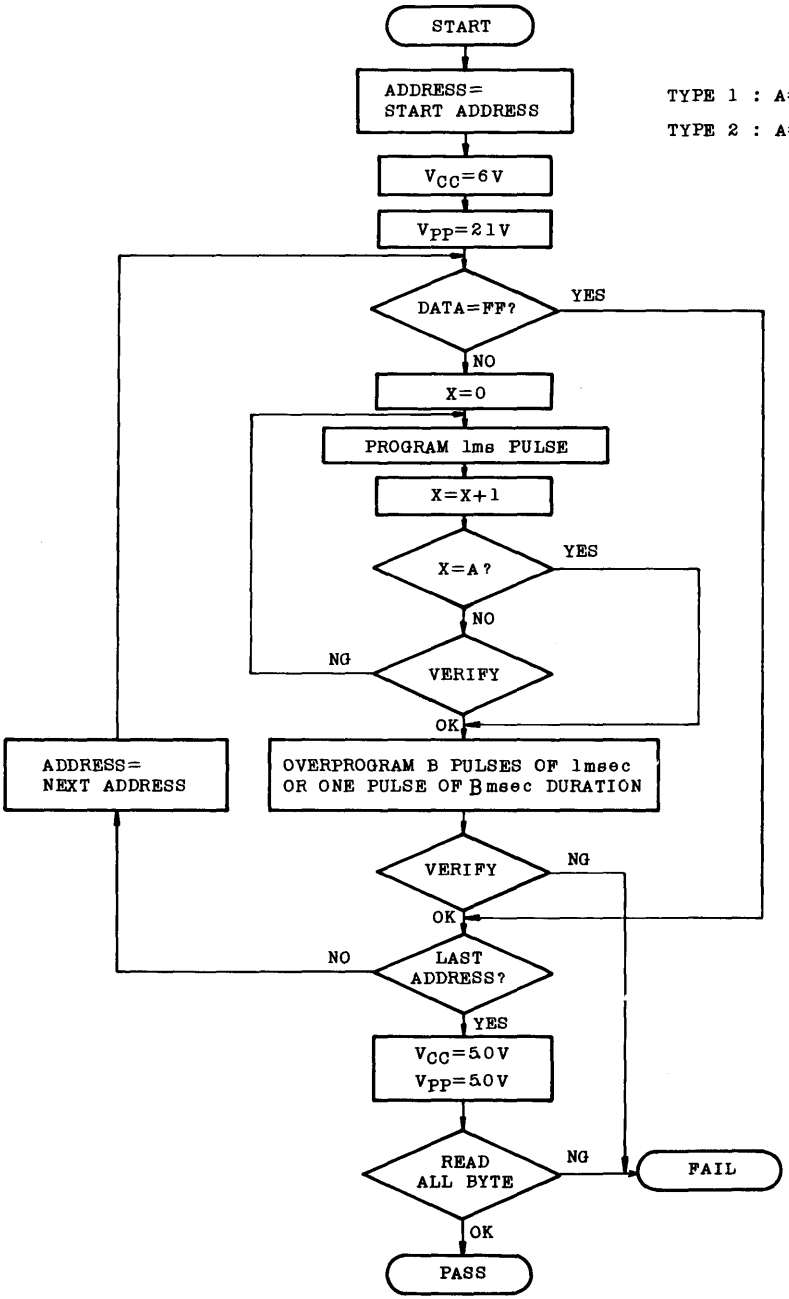
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	A	—	B	ms
t_{PRT}	Program pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. Test Conditions

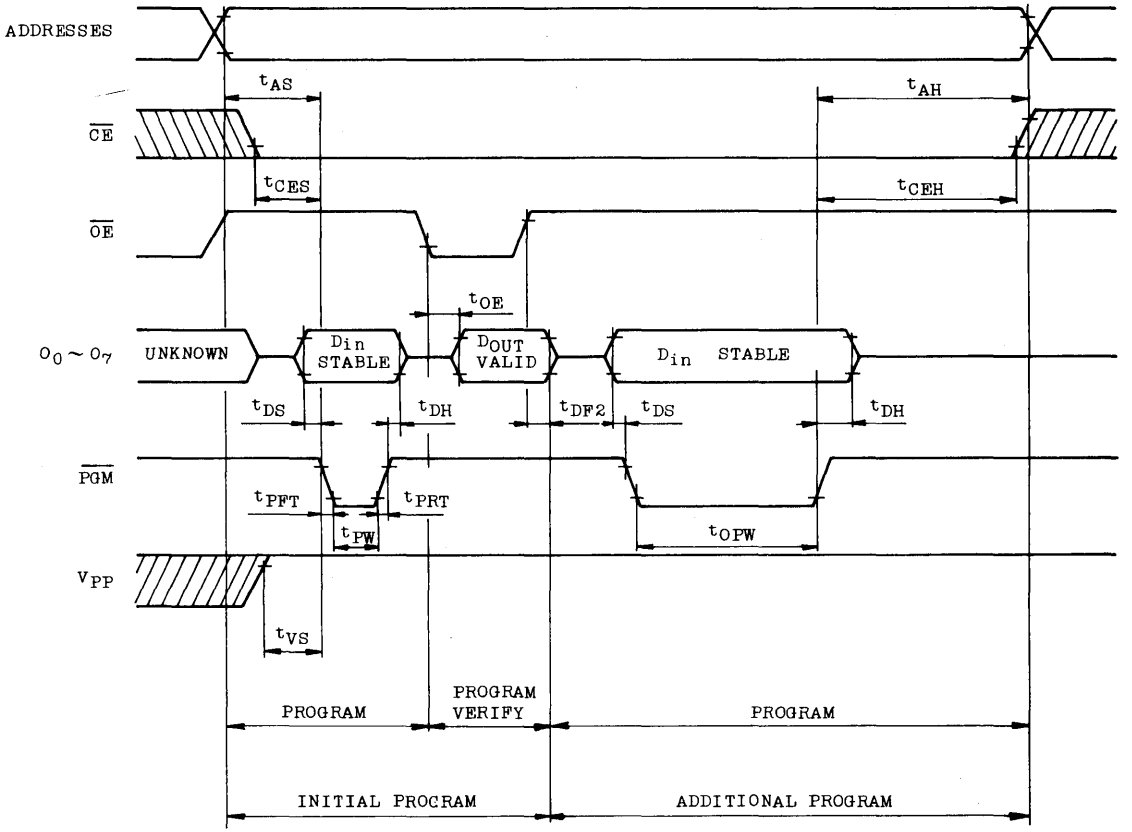
- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.8V and 2.2V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t_{OPW} depends on the program pulse width which is required in the initial program.
(TYPE 1 : 3.8, B=63, TYPE 2 : A=0.95, B=21)

HIGH SPEED PROGRAM MODE FLOW CHART

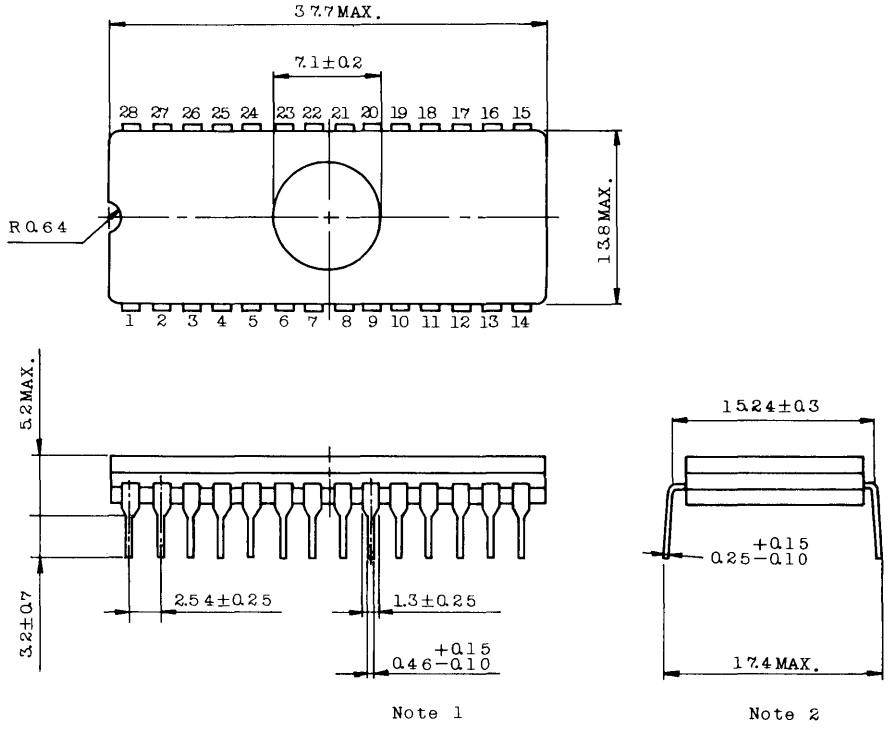


TIMING WAVEFORM (HIGH SPEED PROGRAM)



OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM27128DI-15, TMM27128DI-20 TMM27128DI-25

DESCRIPTION

The TMM27128DI is a 16384 word×8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27128DI's access time is 150ns/200ns/250ns, and the TMM27128DI operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

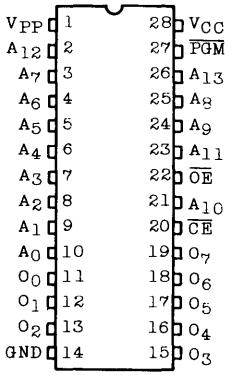
The maximum active current is 100mA and the maximum standby current is 25mA.

For Program operation, the programming is achieved by applying a 50ms active TTL low program pulse to the $\overline{PGM}$ input, and it is possible to program sequentially, individually, or at random.

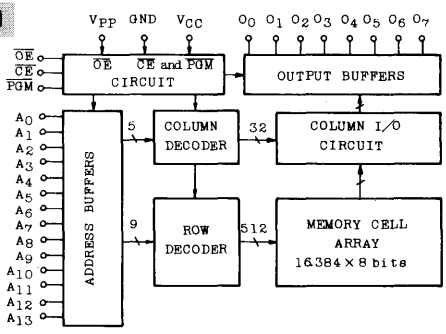
FEATURES

- Wide operating temperature range : −40~85°C
- Single 5-volt power supply
- Fast access time : TMM27128DI-15 150ns
  TMM27128DI-20 200ns
  TMM27128DI-25 250ns
- Power dissipation : 100mA (active current) Max.
  25mA (standby currest) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Fully static operation
- Programs with one 50ms pulse or high speed programming mode(2 types)
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{13}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	21V	5V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~22.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−65~125	°C
$T_{OPR.}$	Operating Temperature	−40~85	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.2	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS

(Ta = −40~85°C, V_{CC} = 5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$ = V_{IH}	—	—	25	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$ = V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = 0~V_{CC}+0.6	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS

(Ta = −40~85°C, V_{CC} = 5V±5%, V_{PP} = 2.2V~V_{CC}+0.6V, Unless otherwise noted)

SYMBOL	PARAMETER	TMM27128DI-15		TMM27128DI-20		TMM27128DI-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	—	100	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	—	0	—	0	—	ns

A. C. Test Conditions

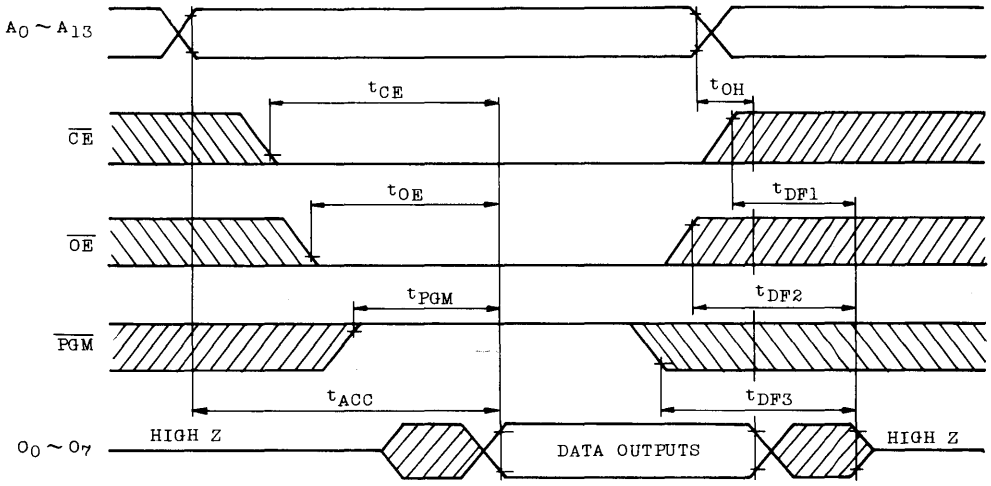
- Output Load : 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Level : Inputs 1V and 2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	—	8	12	pF

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=5V±5%, V_{PP}=21V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=21.5V	—	—	30	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$)

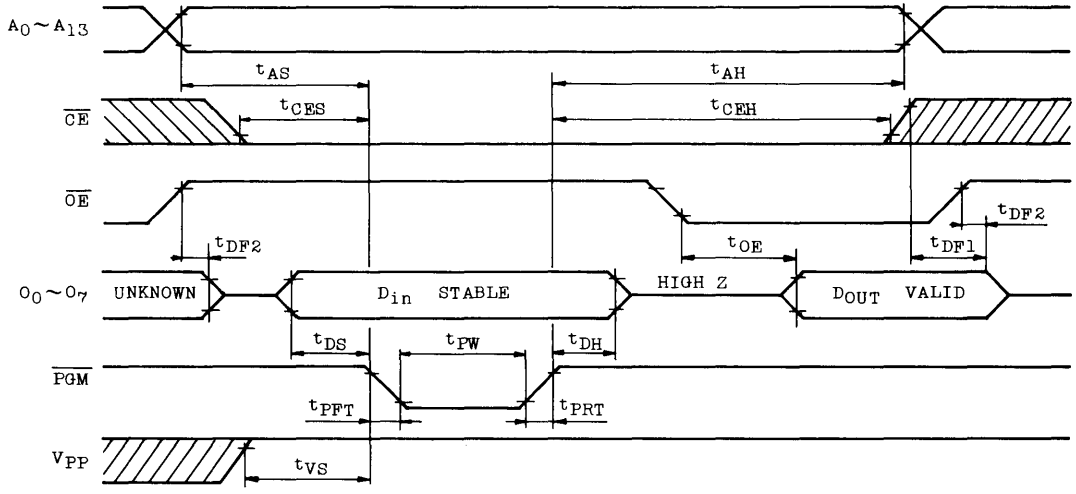
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{PS}	$\overline{PGM}$ Setup Time	—	2	—	—	μs
t_{PH}	$\overline{PGM}$ Hold time	—	2	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	$\overline{PGM} = \overline{CE} = V_{IL}$	45	50	55	ms
t_{CP}	Program Recovery Time	—	0	—	—	μs
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Tim	—	5	—	—	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	—	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High Z	$\overline{OE} = V_{IL}$	—	—	90	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE} = V_{IL}$	—	—	90	ns

A. C. Test Conditions

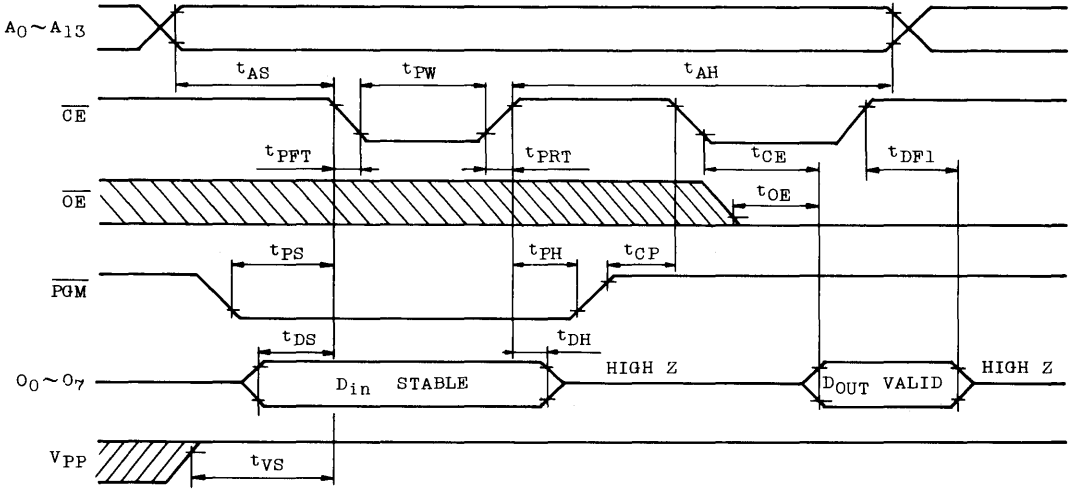
- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.6V and 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

- PROGRAM OPERATION 1. (V_{PP}=21V±0.5V)



- PROGRAM OPERATION 2. (V_{PP}=21V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=21V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM27128DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated does (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W · sec/cm²] .

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μW/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²] .)

The TMM27128DI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals-Toshiba EPROM Protect Seal AC901 are available.

OPERATION INFORMATION

The TMM27128DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES (NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta = −40~85°C)	Read	H	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	21V	5V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H				
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27128DI has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM27128DI can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128DI has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM27128DI is placed in the standby mode which reduce the operating current from 100mA to 25mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TMM27128DI is set up in the program operation mode when applied the program voltage (+21V) to the V_{PP} terminal under $\overline{CE}=\overline{PGM}=\overline{OE}=V_{IH}$.

The program operation occurs during the overlap of the $\overline{CE}$ low and the $\overline{PGM}$ low.

Then the programming is achieved by applying a 50ms (t_{pw}) active low program pulse to the $\overline{CE}$ or the $\overline{PGM}$ input after the addresses and data are stable.

This program pulse should be a single pulse with 50ms pulse width per address word, and its maximum value is 55ms.

The levels required for all inputs are TTL.

The TMM27128DI can be programmed any location at anytime——either individually, sequentially, or at random.

The TMM27128DI should not be programmed with D.C. signal applied to both $\overline{CE}$ and $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128DI from being programmed.

Programming of two or more TMM27128DIs in parallel with different data is easily accomplished. That is , all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE (2 TYPES)

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$ and $\overline{PGM}=V_{IH}$.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. A times)

After correctly programming the selected address, one additional program pulse with pulse width B times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

TYPE 1 : A=15, B=4
TYPE 2 : A=20, B=1

HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=21V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=21.5V$	—	—	30	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=21V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	A	—	B	ms
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE}=V_{IL}$	—	—	90	ns

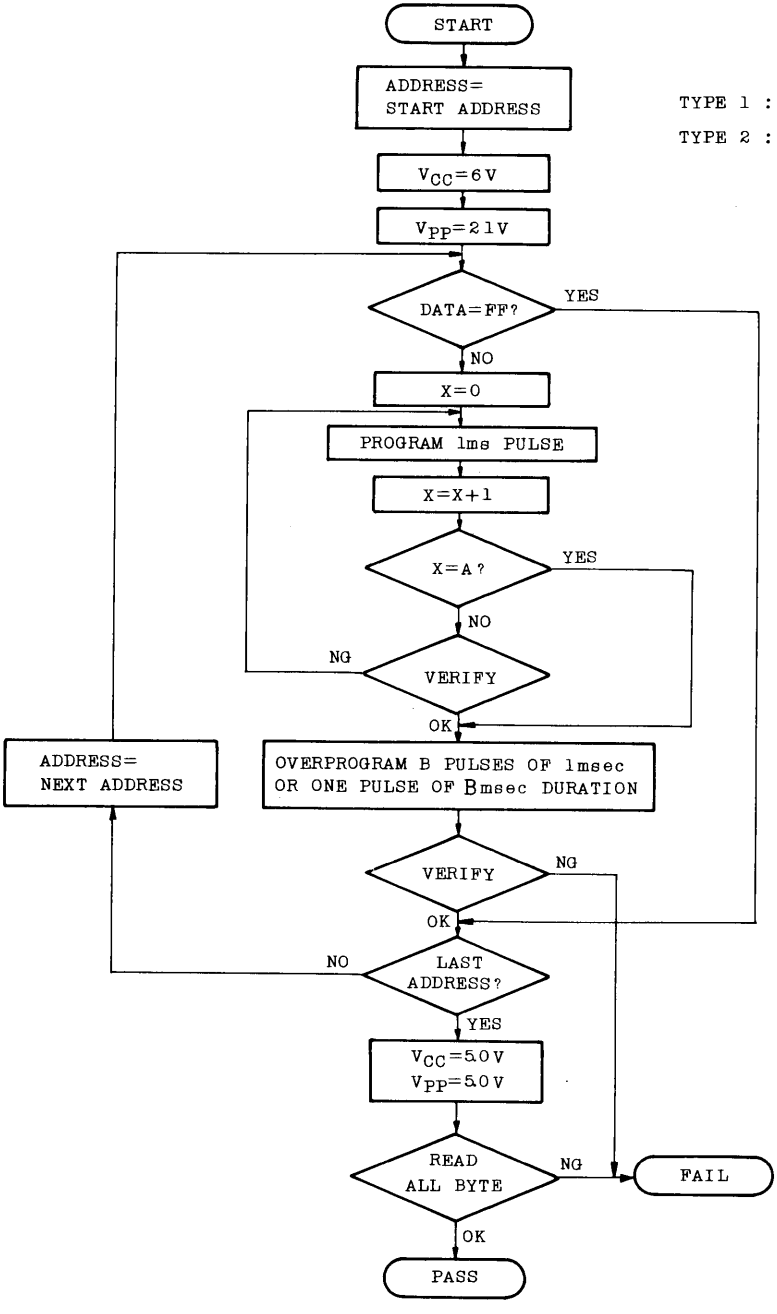
A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.6V and 2.4V
- Timing Measurement Reference Level : Input 1V and 2V : Output 0.8V and 2.0V

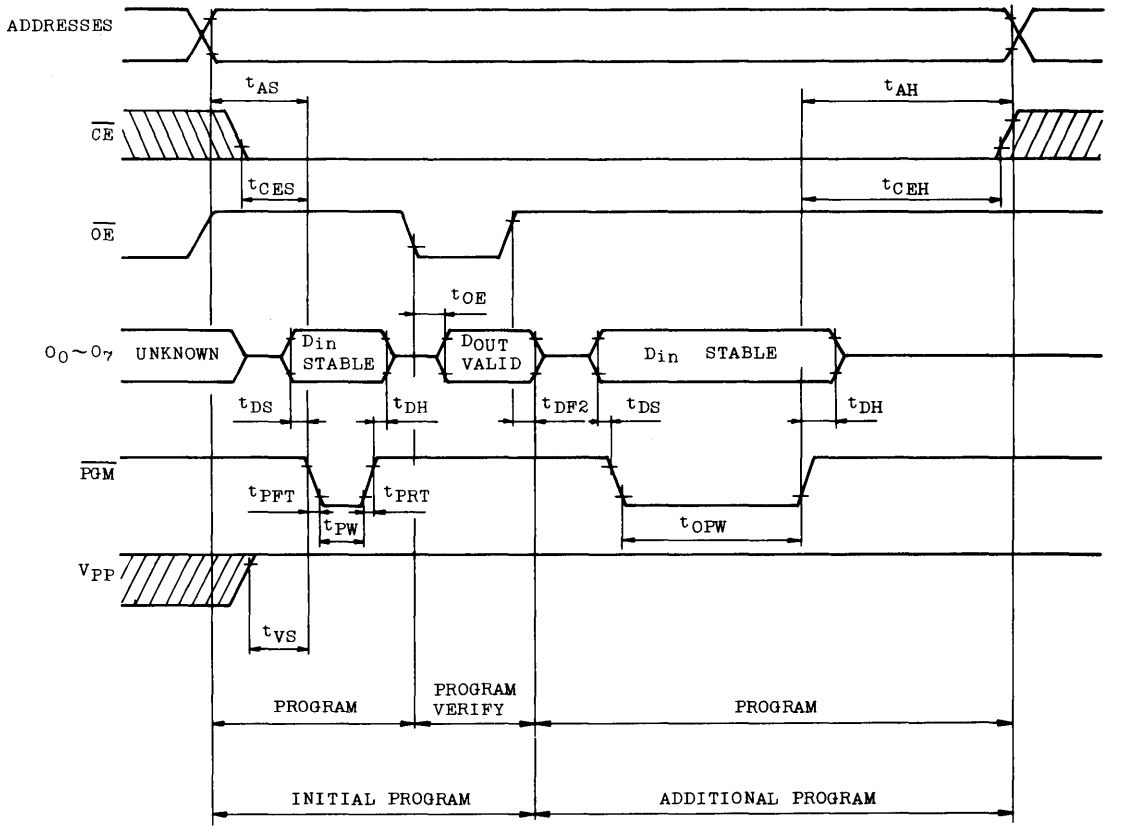
Note :

1. **t_{opw} depends on the program pulse width which is required in the initial Program. (TYPE 1 : A=3.8, B=63, TYPE 2 : A=0.95, B=21)**

HIGH SPEED PROGRAM MODE FLOW CHART

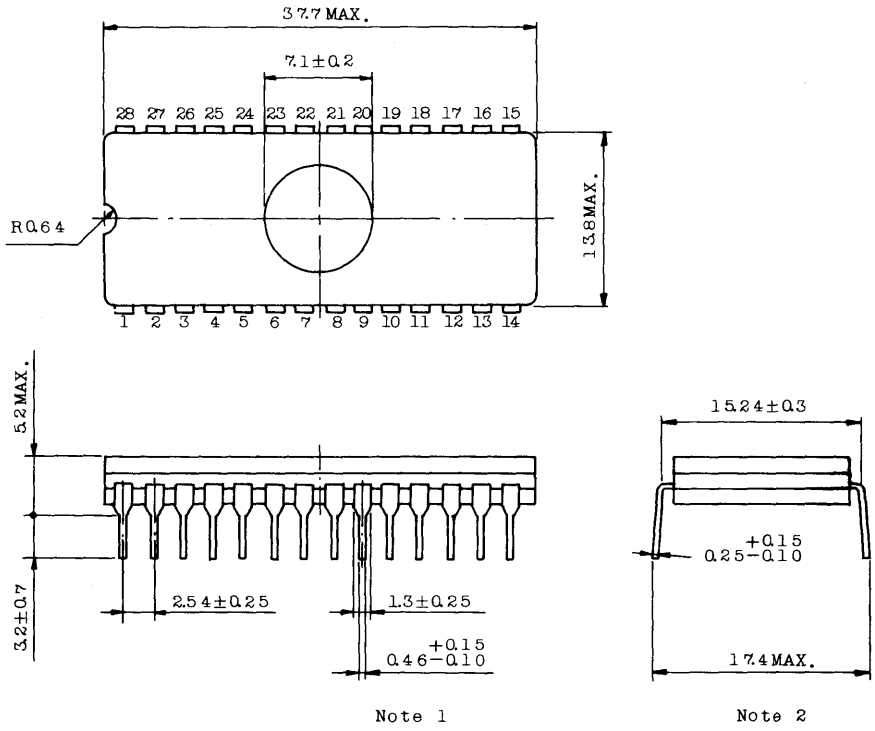


TIMING WAVEFORM (HIGH SPEED PROGRAM)



OUTLINE DRAWINGS

Unit in mm



Note 1 Note 2

Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the and of leads.
3. All dimensions are in millimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described ; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N CHANNEL SILICON STACKED GATE MOS PRELIMINARY

TMM27128AD-15, TMM27128AD-150
TMM27128AD-20, TMM27128AD-200

DESCRIPTION

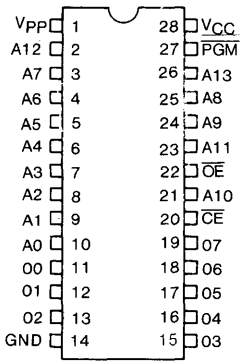
The TMM27128AD is a 16,384 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM27128AD's access time is 150ns/200ns, and the TMM27128AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. The maximum active current is 100mA and the maximum standby current is 30mA. For program operation, the program is achieved by using the high speed programming mode. The TMM27128AD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

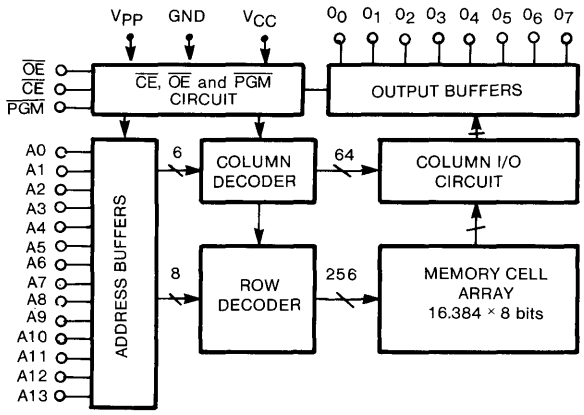
	-15	-20	-150	-200
V_{CC}	5V±5%		5V±10%	
T_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA			
I_{CC1}	30mA			

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128A

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ~ A13	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* Don't Care

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27128AD-15/20	TMM27128AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}+0.6V	2.0~V_{CC}+0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-	-	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-	-	100	mA
V_{IH}	Input High Voltage	-	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-	-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27128AD-15/150		TMM27128AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	
t_{PGM}	$\overline{PGM}$ to Output Valid	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	
t_{OH}	Output Data Hold Time	0	-	0	-	

A.C. TEST CONDITIONS

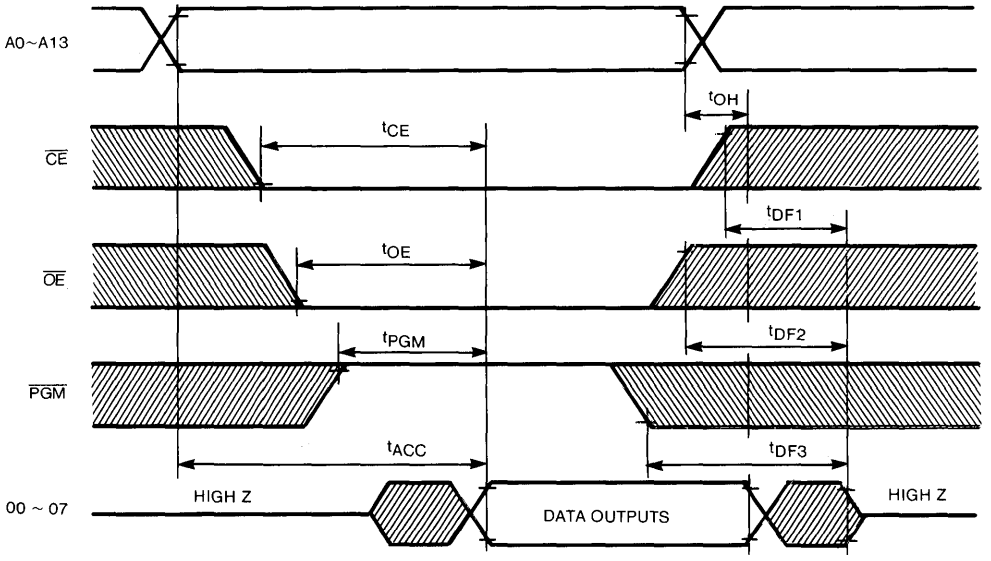
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=OV	-	4	6	pF
C_{OUT}	Output Capcitance	V_{OUT}=OV	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

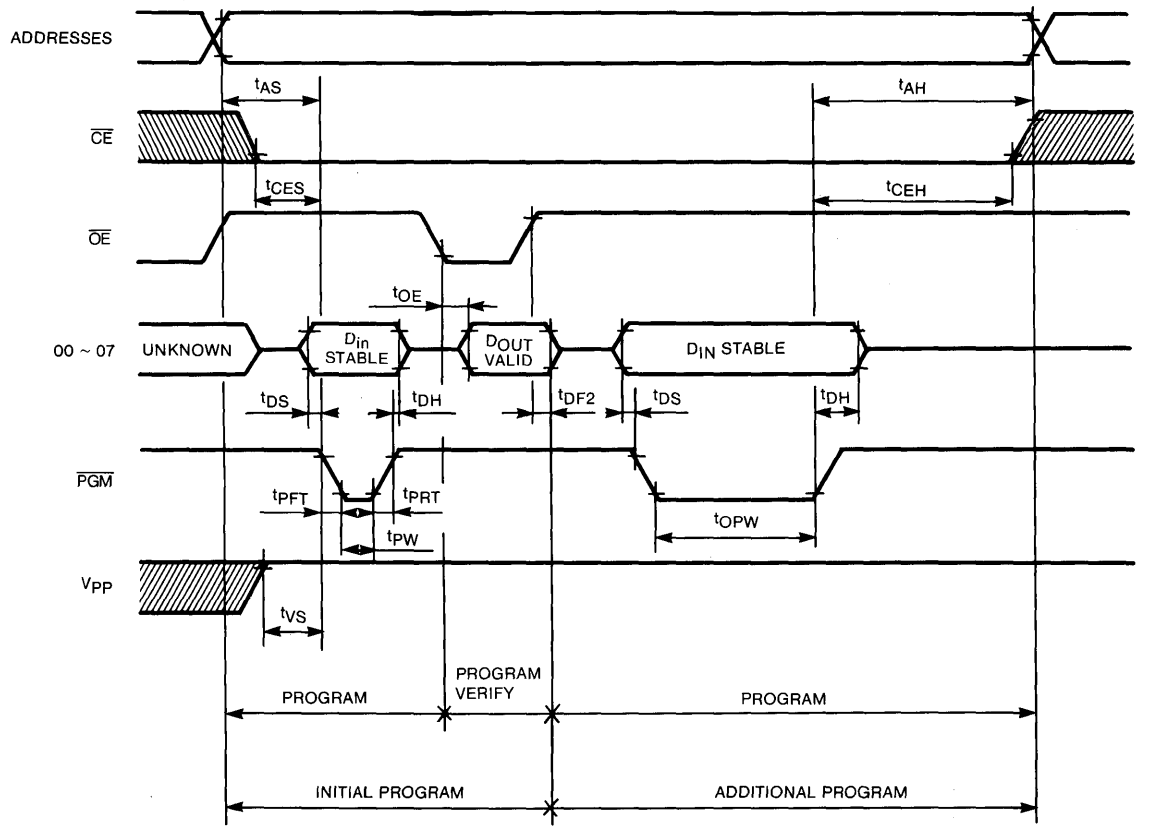
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	-	78.75	ms
t_{PRT}	Program Pulse Rise Time	-	5	-	-	ns
t_{PFT}	Program Pulse Fall Time	-	5	-	-	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input; Output 0.8V and 2.0V

Note 1: t_{OPW} depends on the program pulse width which is required in the initial program.

TIMING WAVEFORMS (HIGH SPEED PROGRAM)



Note:

1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from or setting the device into a socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so a voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TMM27128AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. Using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20 × 60) [sec] ≅ 15 [W · sec/cm²].)

The TMM27128AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TMM27128AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES (NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, * : Don't Care

READ MODE

The TMM27128AD has three control functions. The chip enable ($\overline{CE}$) controls the operational power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from the stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming the $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

When $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TMM27128AD s can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM27128AD is placed in the standby mode which reduces the supply current from 100mA to 30mA, and the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TMM27128AD locations can be programmed either individually, sequentially, or at random

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed into the device.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128AD from being programmed.

Programming of two or more TMM27128ADs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decrease by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}+6V and $\overline{PGM}=V_{IH}$.

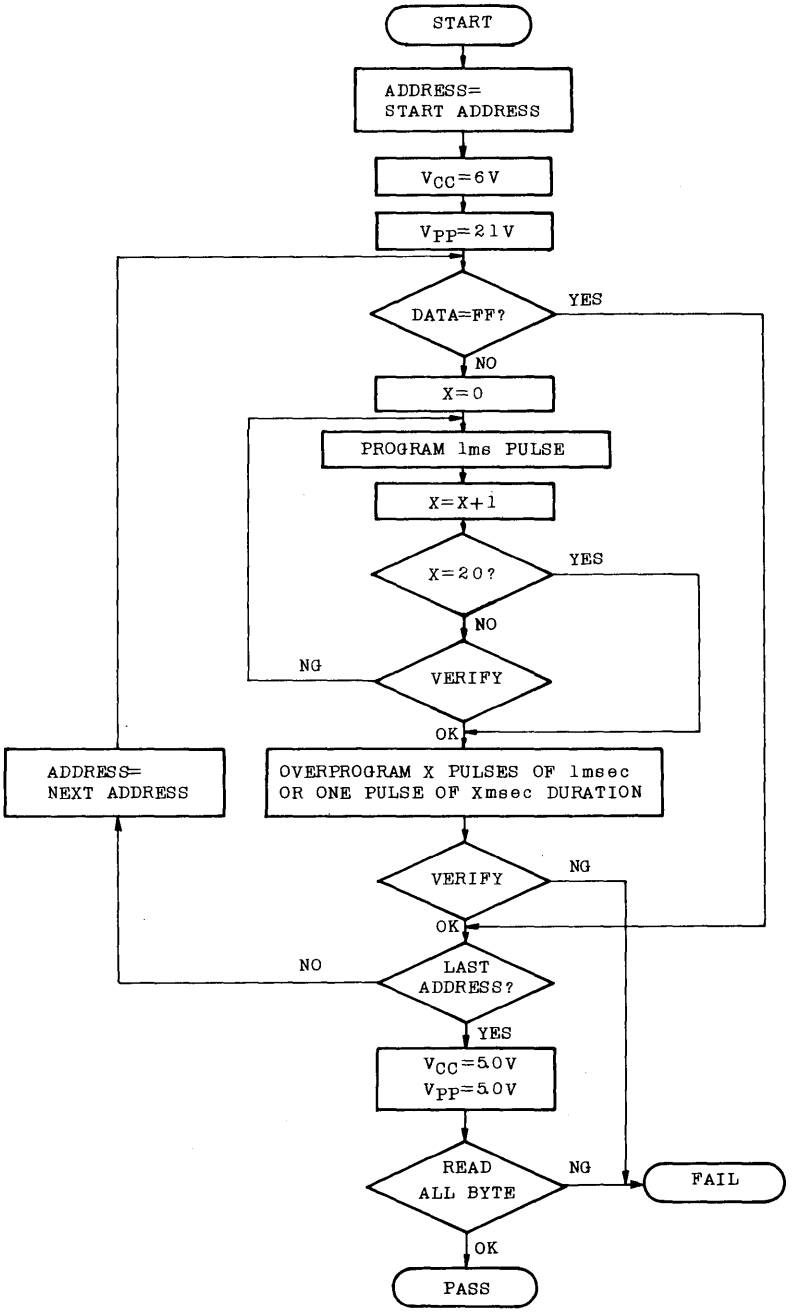
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program verifies (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

IGH SPEED PROGRAM MODE FLOW CHART



PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "0s" data into the desired bit locations by electrically programming.

The TMM 27256DI is in the programming m
when the V_{PP} input is at 21V and $\overline{CE}$ is at TTL-
under $\overline{OE}=V_{IH}$.

The TMM27256DI can be programmed
location at anytime either individually, sequentia
or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TMM 27256DI from being programmed.

Programming of two or more TMM27256DIs in parallel with different data is easily accomplished.

That is, all inputs except for $\overline{CE}$ may be comm
connected, and a TTL low level program puls
applied to the $\overline{CE}$ of the desired device only and
high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The Program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 20 tin

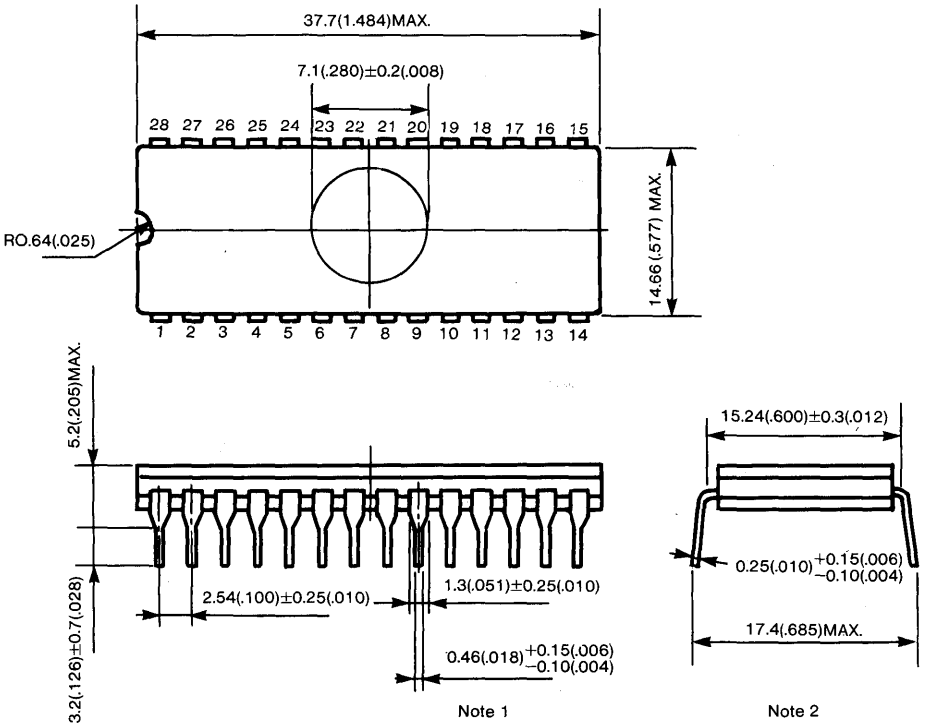
After correctly programming the selec
address, the additional program pulse with w
equal to that needed for initial programming
applied.

When programming has been completed,
data in all addresses should be verified with $V_{CC}=$
$=5V$.

This high speed program algorithm allows
programming of the TMM27256DI to be acc
plished within one and a half minutes (typ.).

OUTLINE DRAWINGS

Unit in mm (inches)



Note:

1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.

2. This value is measured at the end of leads.

TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM27256D-15
TMM27256D-20

DESCRIPTION

The TMM27256D is a 32,768 word×8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27256D's access time is 150ns/200ns, and the TMM27256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V which is the same voltage as TMM2764D, TMM27128D and TC57256D.

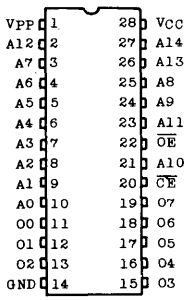
The programming of TMM27256D is accomplished within about one and a half minutes (typ.).

The TMM27256D is fabricated with the N-channel silicon double layer gate MOS technology.

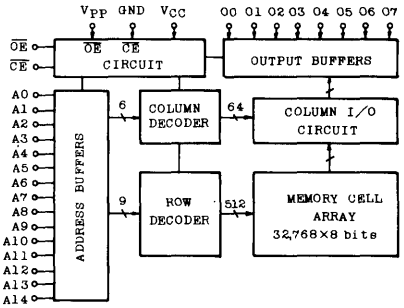
FEATURES

- Fast access time TMM27256D-15 150ns
  TMM27256D-20 200ns
- Low power dissipation
  Active : 100mA
  Standby : 25mA
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P and TMM23256P and CMOS EPROM TC57256D.
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	21V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	L	L			Data Out	

Note * : H or L

CHARACTERISTICS

BOL	PARAMETER	TMM27256AD-15/150		TMM27256AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
C	Address Access Time	-	150	-	200	ns
	$\overline{CE}$ to Output Valid	-	150	-	200	ns
	$\overline{OE}$ to Output Valid	-	70	-	70	ns
1	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
2	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
H	Output Data Hold Time	0	-	0	-	ns

TEST CONDITIONS

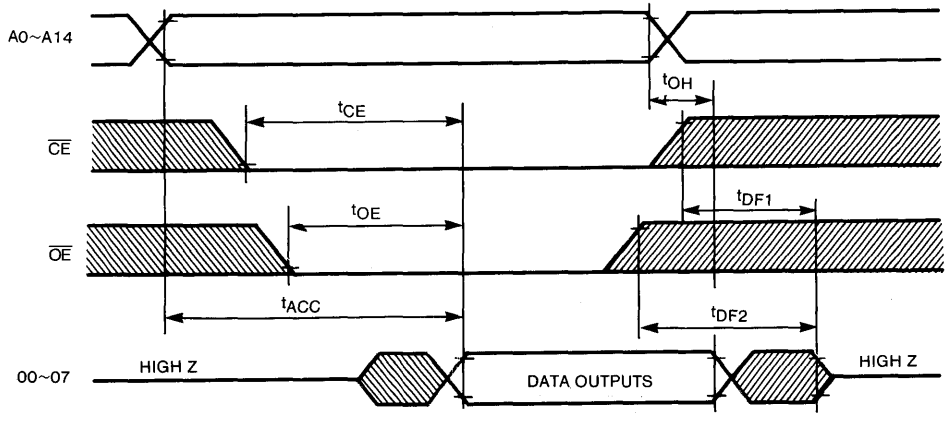
Output Load	:	1 TTL Gate and C_L=100pF
Input Pulse Rise and Fall Times	:	10ns Max.
Input Pulse Levels	:	0.45V ~ 2.4V
Timing Measurement Reference Level	:	Inputs 0.8V and 2V, Outputs 0.8V and 2.0V

PACITANCE * (Ta=25°C, f=1MHz)

BOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
	Input Capacitance	V_{IN}=OV	-	4	6	pF
UT	Output Capcitance	V_{OUT}=OV	-	8	12	pF

is parameter is periodically sampled and is not 100% tested.

ING WAVEFORMS (READ)



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~75	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27256AD-15/20	TMM27256AD-150/20
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}+0.6V	2.0~V_{CC}+0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UI
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μ
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	-	-	±10	μ
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-	-	30	m
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-	-	100	m
V_{IH}	Input High Voltage	-	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-	-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	-	-	±10	μ

A. C. PROGRAMMING CHARACTERISTICS

($T_a = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{OEH}	$\overline{OE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Intial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ns
t_{OPW}	Overprogram Pulse Width	Note 1	0.95	1	21	ms
t_{DV}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	—	—	1	μs
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	—	—	150	ns

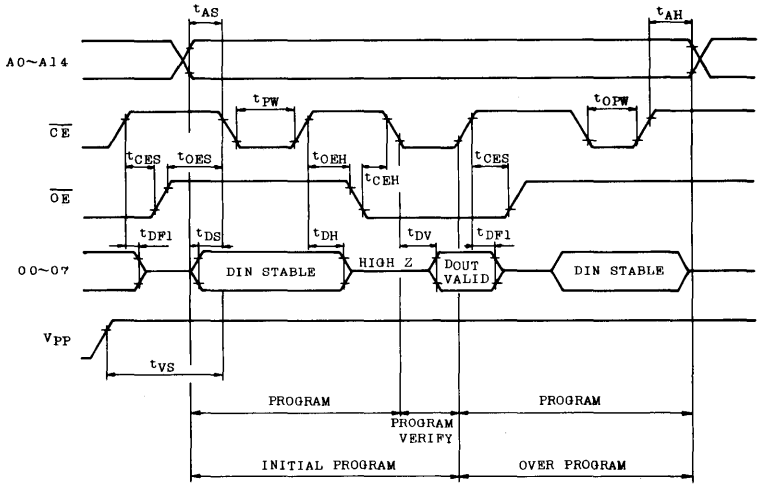
A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

- ($V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with $V_{PP} = 21V$ may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V

ERASURE CHARACTERISTICS

The TMM27256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²] .)

The TMM27256D's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the flourescent lamps will include 3000~4000A wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27256D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	21V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	L	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27256D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

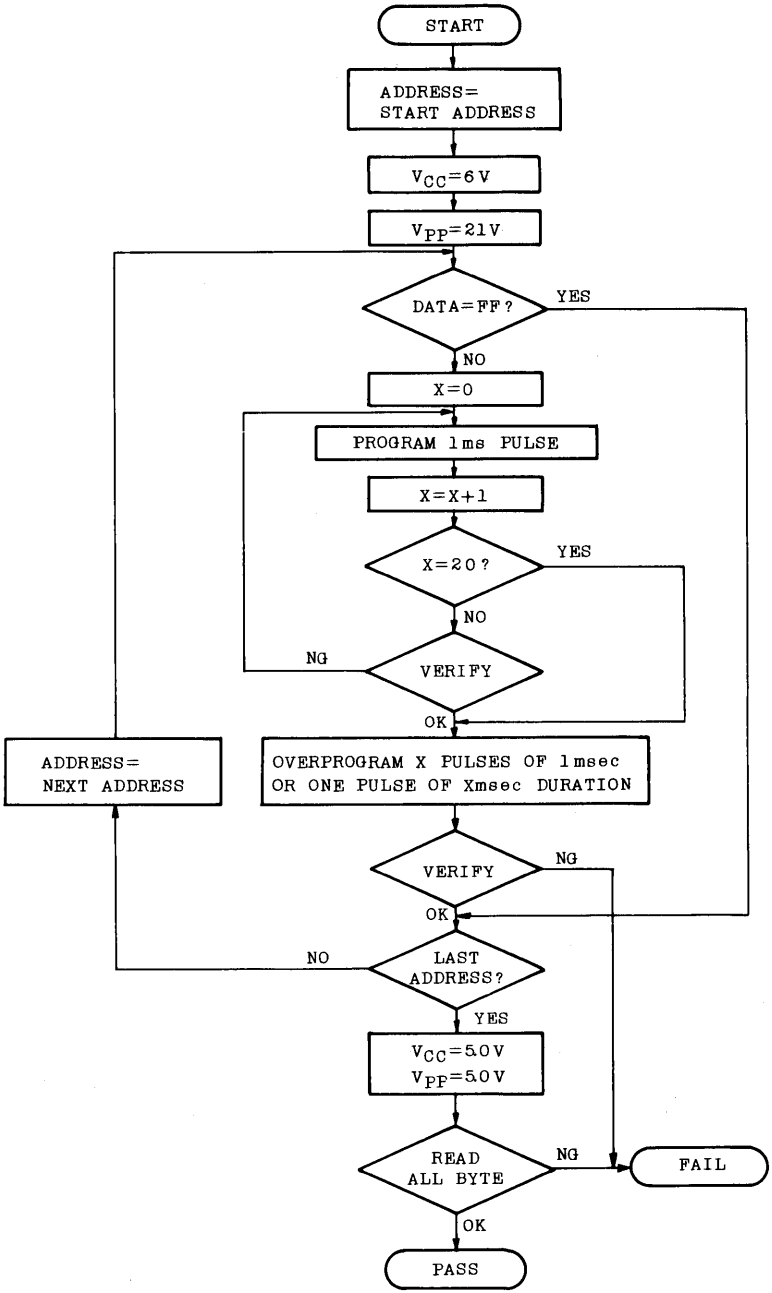
OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$.the outputs will be in a high impedance state.

So two or more TMM27256Ds can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

HIGH SPEED PROGRAM MODE FLOW CHART



STANDBY MODE

The TMM27256D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27256D in placed in the standby mode which reduce the operating current to 25mA from 100mA (about 75% reduction) by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256D are in the "1" state which is erased state.

Therefore the program operation is to introduce "Os" data into the desired bit locations by electrically programming.

The TMM27256D is in the programming mode when the V_{PP} input is at 21V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.

The TMM27256D can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TMM27256D from being programmed.

Programming of two or more TMM27256Ds in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 20 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

This high speed program algorithm allows the programming of the TMM27256D to be accomplished within one and a half minutes (typ.).

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27256D which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM27256D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applined to address line A_9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A_0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O_7).

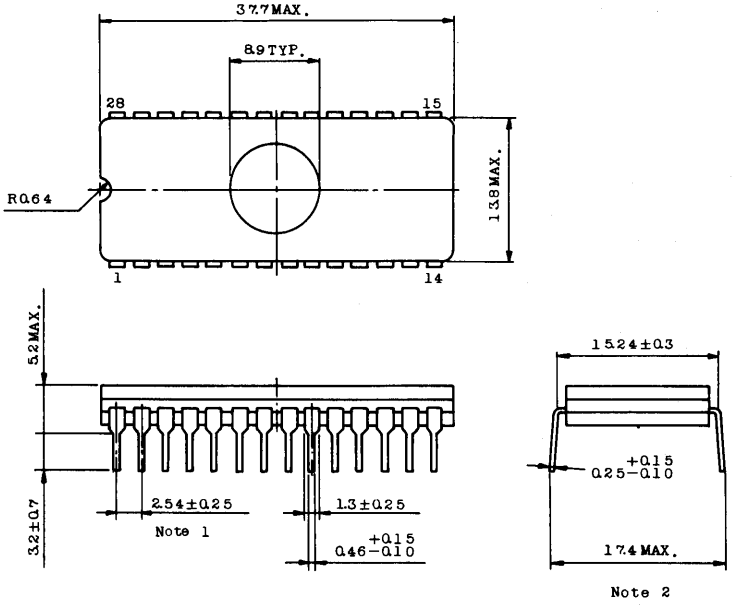
The following table shows electric signature of TMM27256D.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	1	0	1	0	0	94

Notes : $A_9 = 12V \pm 0.5V$
A_1-A_8, A_{10}-A_{14}, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

32,768 WORD × 8 BIT NMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM27256DI-15
TMM27256DI-20

DESCRIPTION

The TMM27256DI is a 32,768 word×8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27256DI's access time is 150ns/200ns, and the TMM27256DI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V which is the same voltage as TMM2764D, TMM27128D and TC57256D.

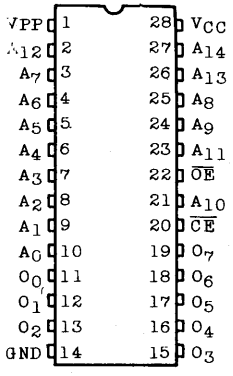
The programming of TMM27256DI is accomplished within about one and a half minutes (typ.).

The TMM27256DI is fabricated with the N-channel silicon double layer gate MOS technology.

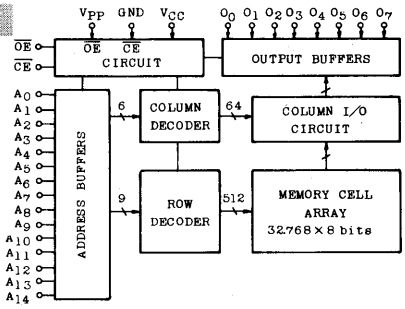
FEATURES

- Wide operating temperature range : −40~85°C
- Fast access time : TMM27256DI-15 150ns
  TMM27256DI-20 200ns
- Low power dissipation
  Active : 120mA
  Standby : 25mA
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P and TMM23256P and CMOS EPROM TC57256D.
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	21V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	L	L			Data Out	

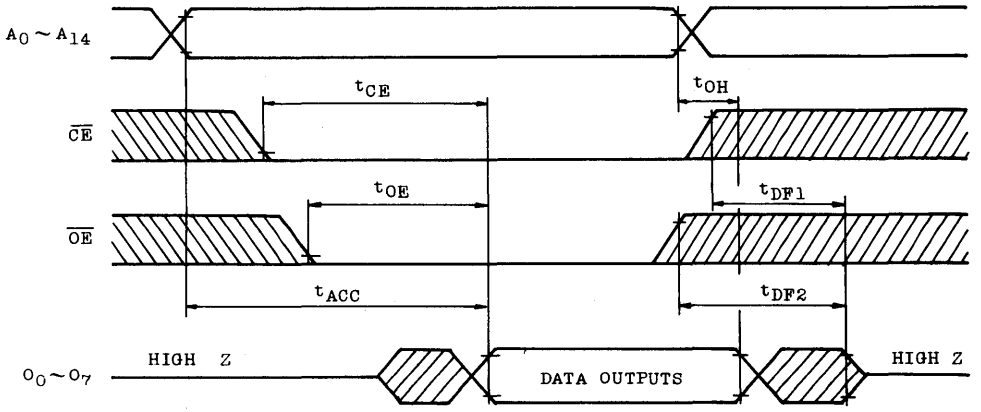
Note * : H or L

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=OV	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=OV	—	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. and RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25, V_{PP}=21V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=21.5V	—	—	30	mA

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~22.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	−40~85	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	−	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.2	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS

($Ta=-40\sim85°C$, $V_{CC}=5V\pm5\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{IH}$	—	—	25	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}=V_{IL}$	—	—	120	mA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=0\sim V_{CC}+0.6$	—	—	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4\sim V_{CC}$	—	—	±10	μA

A. C. CHARACTERISTICS

($Ta=-40\sim85°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=2.2V\sim V_{CC}+0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	TMM27256DI-15		TMM27256DI-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	−	150	−	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	−	150	−	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	−	70	−	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	−	0	−	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

A. C. PROGRAMMING CHARACTERISTICS

(T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{OEH}	$\overline{OE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	0.95	1	21	ms
t_{DV}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	—	—	1	μs
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	—	—	150	ns

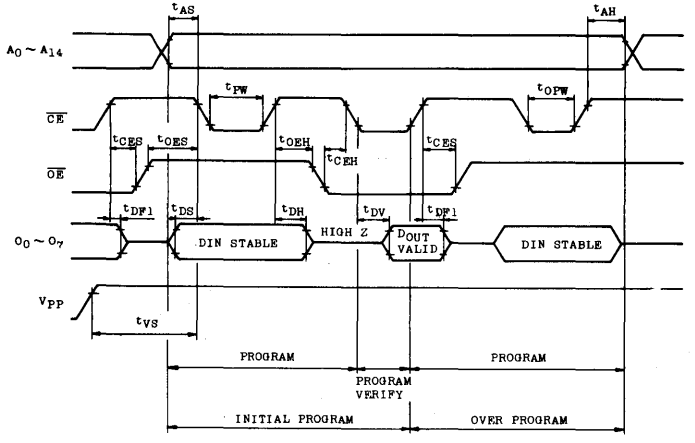
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

- (V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=21V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TMM27256DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537A (Angstroms) to the chip through the transparent window.

Then integrated dose (ultraviolet light intensity [w/cm²] ×exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅15 [w·sec/cm²] .)

The TMM27256DI's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the flourescent lamps will include 3000~4000A (wavelength components.)

Therefore when used under such lighting for extended periods of time, the opeque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27256DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read operation (Ta=40~85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	21V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	L	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27256DI has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM27256DIs can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27256DI has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27256DI is placed in the standby mode which reduce the operating current to 25mA from 120mA (about 80% reduction) by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state. independent of the $\overline{OE}$ inputs.

ECTRIC SIGNATURE MODE

Electric signature mode allows reading out a code from the TMM27128AD which identifies its nufacturer and device type.

The programming equipment may read out a manufacturer and device code from the TMM27128AD using this mode before program operation to automatically set program voltage (V_{PP}) and algorithm.

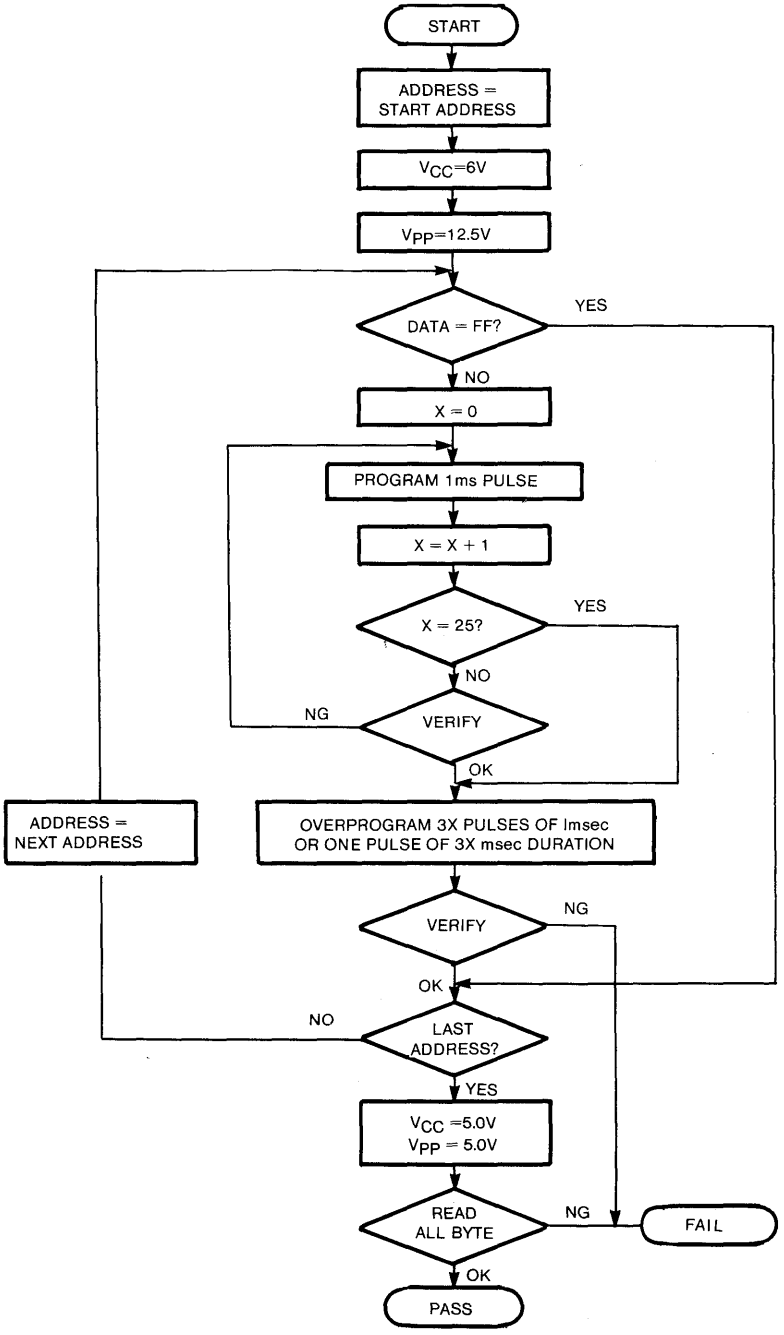
Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address es are set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code dentified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of SB (07).

The following table shows electric signature of TMM27128AD.

PINS / IGNATURE	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
anufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
evice Code	V_{IH}	1	1	0	1	0	0	1	1	D3

tes: A9=12V±0.5V
A1~A8, A10~A13, $\overline{CE}$, $\overline{OE}$=V_{IL}
$\overline{PGM}$=V_{IH}

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27256DI which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM27256DI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up then 12V is applied to address line A_9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A_0 is set to V_{IH}.

These two codes possess an odd parity with the parity bit of MSB (O_7).

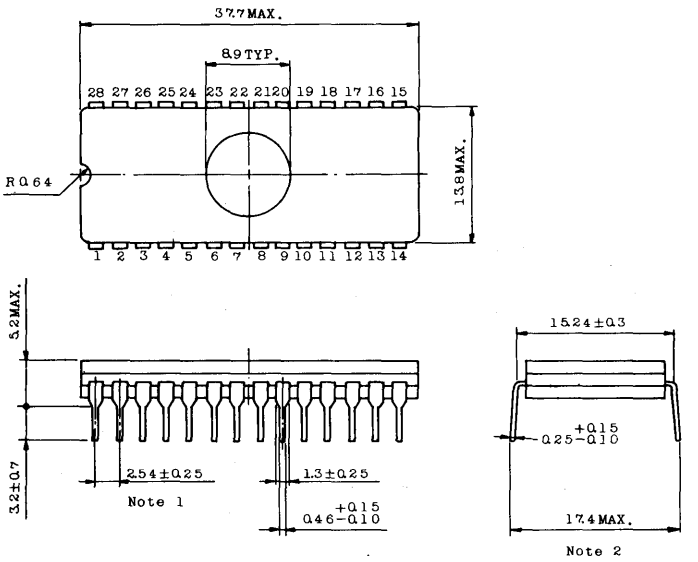
The following table shows electric signature of TMM27256DI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	0	0	1	0	1	0	0	94

Notes: $A_9 = 12V \pm 0.5V$
A_1-A_8, A_{10}-A_{14}, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

PRELIMINARY

TMM27256AD-15, TMM27256AD-150
TMM27256AD-20, TMM27256AD-200

DESCRIPTION

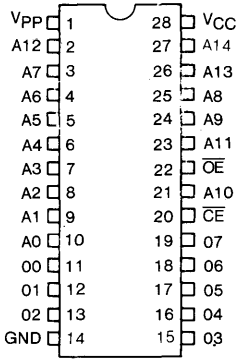
The TMM27256AD is a 32,768 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM27256AD's access time is 150ns/200ns, and the TMM27256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.
For program operation, the programming is achieved by using the high speed programming mode. The TMM27256AD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

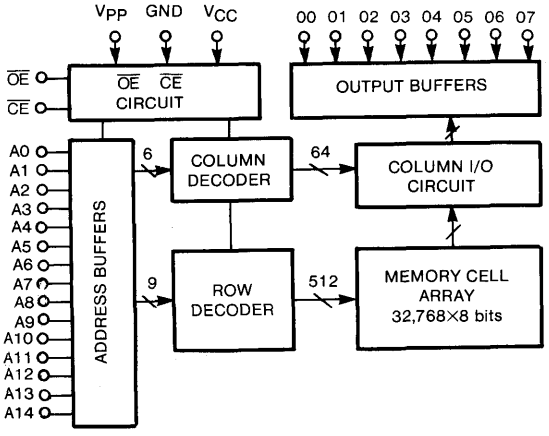
	-15	-20	-150	-200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		100mA	
I_{CC1}	30mA		30mA	

- Fully static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27256
- Standard 28 pin DIP cerdip package

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0 ~ O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

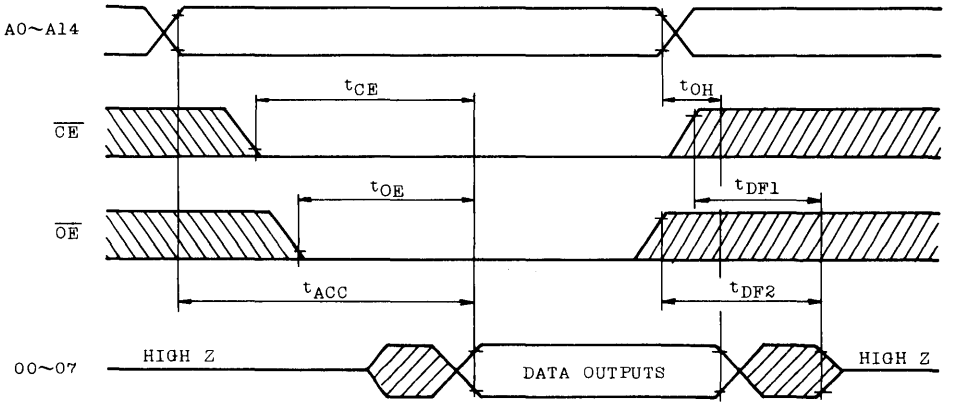
* H or L

APACITANCE * (Ta=25°C, f=1MHz)

MBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
N	Input Capacitance	V_{IN}=0V	—	4	6	pF
OUT	Output Capacitance	V_{OUT}=0V	—	8	12	pF

his paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



OGRAM OPERATION

C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

MBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=21.5V	—	—	30	mA

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~22.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·se
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UN
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μ
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{IH}$	—	—	25	m
I_{CC2}	Supply Current (Active)	$\overline{CE}=V_{IL}$	—	—	100	m
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=0\sim V_{CC}+0.6$	—	—	±10	μ
I_{LO}	Output Leakage Current	$V_{OUT}=0.4\sim V_{CC}$	—	—	±10	μ

A. C. CHARACTERISTICS

($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=2.0V\sim V_{CC}+0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	TMM27256D-15		TMM27256D-20		U
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	—	150	—	200	n
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	—	150	—	200	n
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	—	70	—	70	n
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	n
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	n
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	—	0	—	n

A. C. Test Conditions

- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

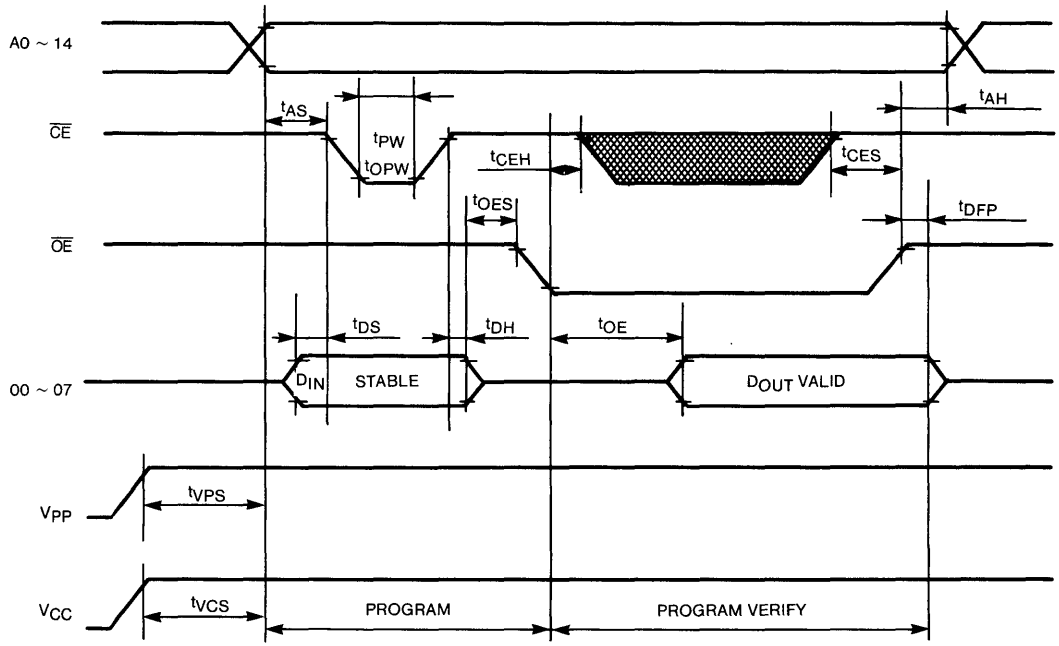
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note:

1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from or setting the device into a socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So a voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TMM27256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w sec/cm²].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. Using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (10 × 60) [sec] ≅ 15 [w · sec/cm²].)

The TMM27256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TMM27256AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	Active
	Program Verify	*	L			Data Out	Active

* : Don't Care

READ MODE

The TMM27256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from the stabilization of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

When $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM27256AD's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27256AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27256AD is placed in the standby mode which reduces the operating current to 30mA from 100mA (about 70% reduction) and the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256AD are in the "1" state which is the erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TMM27256AD is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$.

The TMM27256AD can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed into the device.

The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that a program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM27256AD from being programmed.

Programming of two or more TMM27256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using the high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

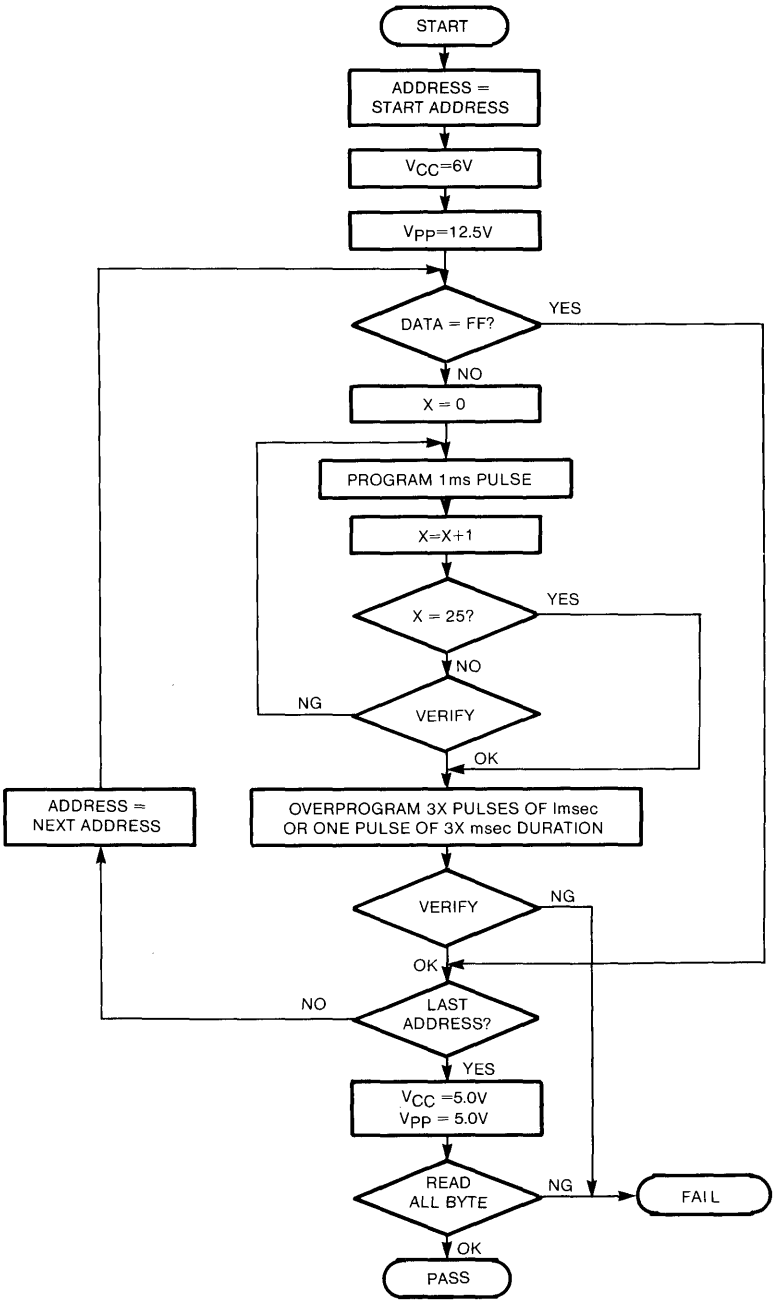
The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program verifies (max. 25 times).

After correctly programming the selected address, the additional program pulse with width equal to 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows reading out a code from the TMM27256AD which identifies its manufacturer and device type.

The programming equipment may read out a manufacturer and device code from the TMM27256AD by using this mode before program operation to automatically set program voltage (V_{PP}) and algorithm.

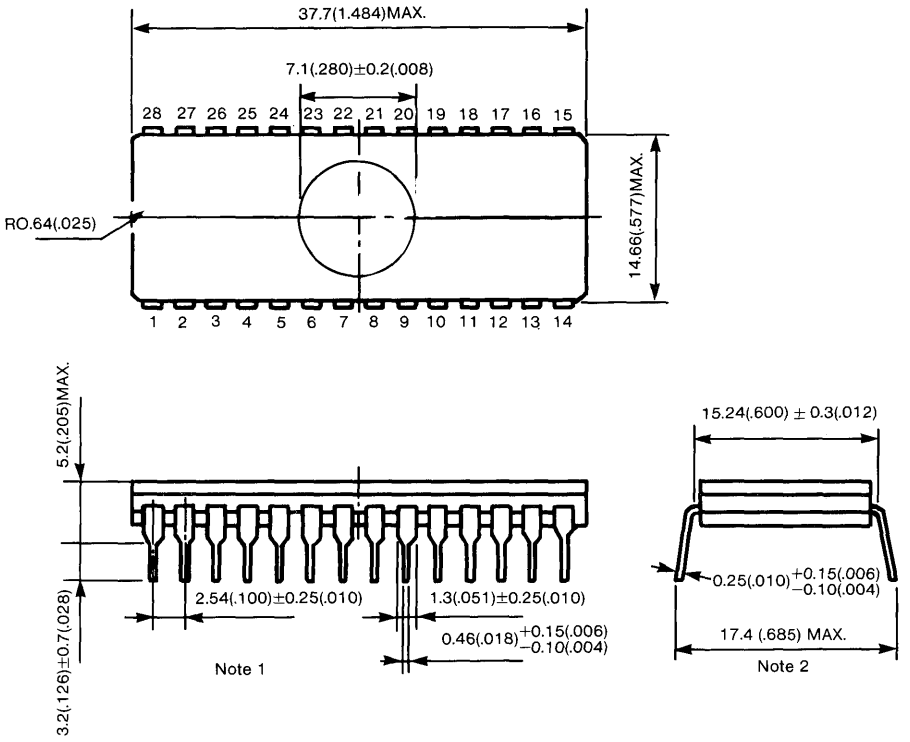
Electric Signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

The following table shows electric signature of TMM27256AD.

PINS / SIGNATURE	A0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

Notes: A9=12V±0.5V
A1~A8, A10~A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS **Unit in mm (inches)**



Note:

1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.

2. This value is measured at the end of leads.

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
PRELIMINARY

TMM27512D-20, TMM27512D-200
TMM27512D-25, TMM27512D-250

DESCRIPTION

The TMM27512D is a 65,536 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM27512D's access time is 200ns/250ns, and the TMM27512D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.
For program operation, the programming is achieved by using the high speed programming mode. The TMM27512D is fabricated with the N-channel silicon double layer gate MOS technology.

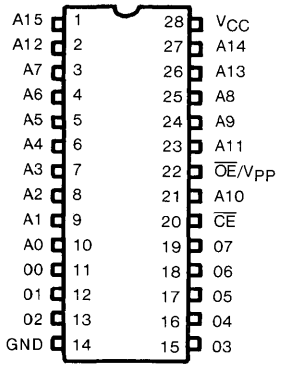
FEATURES

	-20	-25	-200	-250
V_{CC}	5V±5%		5V±10%	
t_{ACC}	200ns	250ns	200ns	250ns
I_{CC2}	100mA		100mA	
I_{CC1}	30mA		30mA	

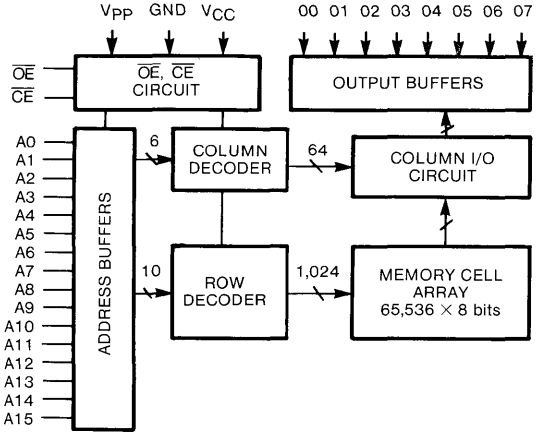
FEATURES

- Fully static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ~ A12	Address Inputs
O_0 ~ O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N.C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* Don't Care

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input / Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~75	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27512D-20/25	TMM27512D-200/250
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}+0.6V	2.0~V_{CC}+0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-	-	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-	-	100	mA
V_{IH}	Input High Voltage	-	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-	−0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6V	-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMTER	TMM27512D-20/200		TMM27512D-25/250		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	200	-	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	200	-	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	-	0	-	ns

A.C. TEST CONDITIONS

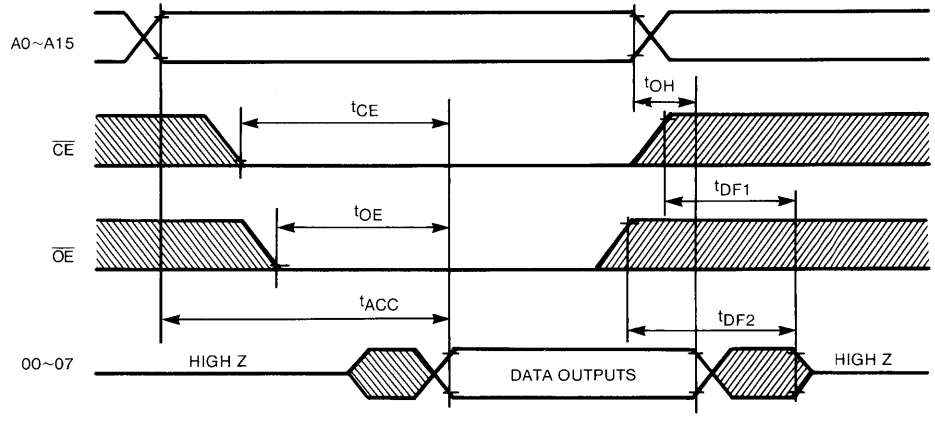
- Output Load : 1 TTL Gate and C_L=100 pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	V_{IN}=OV	-	4	6	pF
C_{IN2}	$\overline{OE}$ /V_{PP} Input Capacitance	V_{IN}=OV	-	50	60	pF
C_{OUT}	Output Capacitance	V_{OUT}=OV	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$ /V_{PP} Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$ /V_{PP} Hold Time	-	2	-	-	μs
t_{PRT}	$\overline{OE}$ /V_{PP} Pulse Rise Time	-	50	-	-	ns
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VR}	$\overline{OE}$ /V_{PP} Recovery Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$/V_{PP}=V_{PP}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}$/V_{PP}=V_{IL}	-	-	1	μs
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

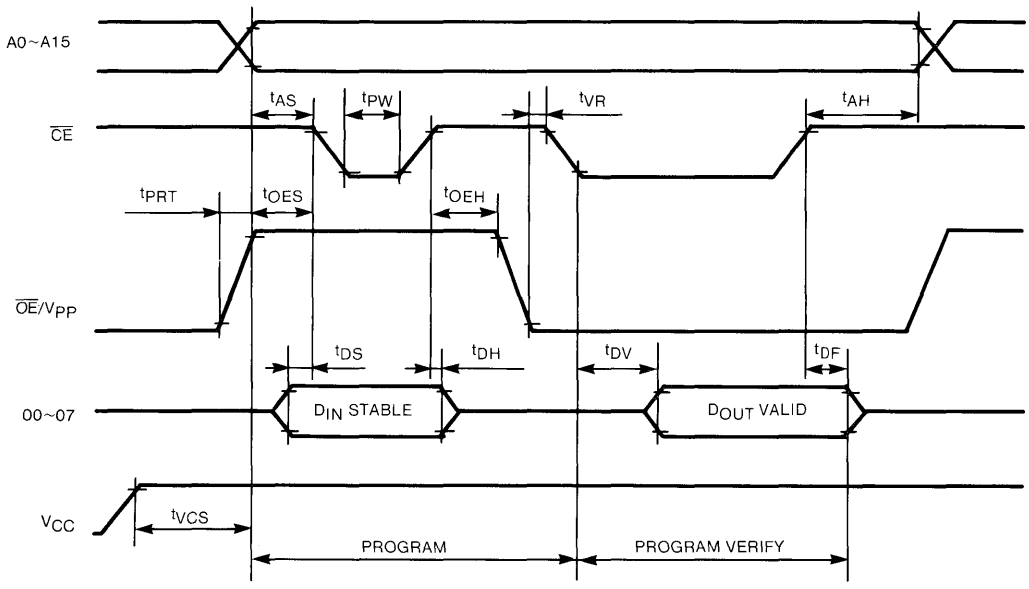
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V~2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27512D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w · sec/cm²].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (10 × 60) [sec] ≅ 15 [w · sec/cm²].)
The TMM27512D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the fluorescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27512D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	Active
	Standby	H	*		High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	V_{PP}	6V	Data In	Active
	Program Inhibit	H	V_{PP}		High Impedance	Active
	Program Verify	L	L		Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM27512D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM27512D's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27512D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM27512D is placed in the standby mode which reduce the operating current to 30mA from 100mA (about 70% reduction) by applying TTL-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27512D are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TMM27512D is in the programming mode when the V_{PP} input is at 12.5V and CE is at TTL-Low level under $\overline{OE}=V_{IH}$.
The TMM27512D can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IL}.

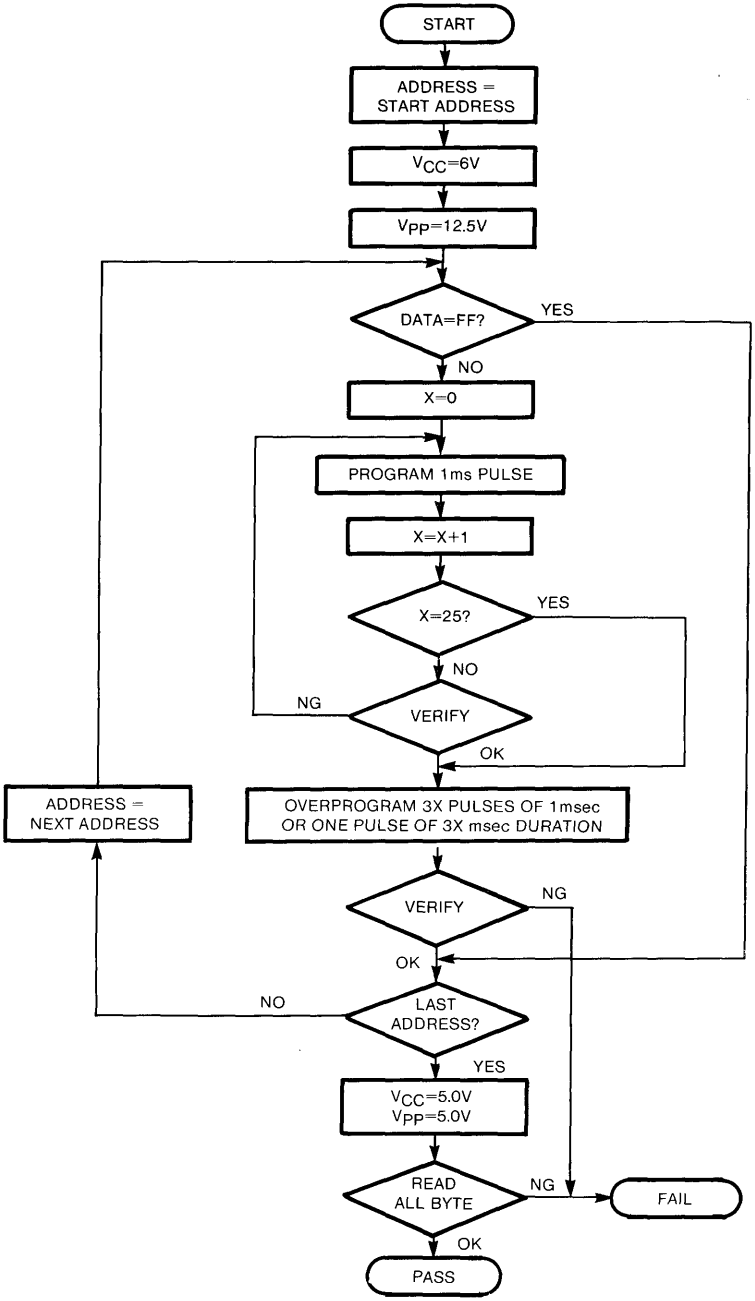
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM27512D from being programmed.
Programming of two or more TMM27512D's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

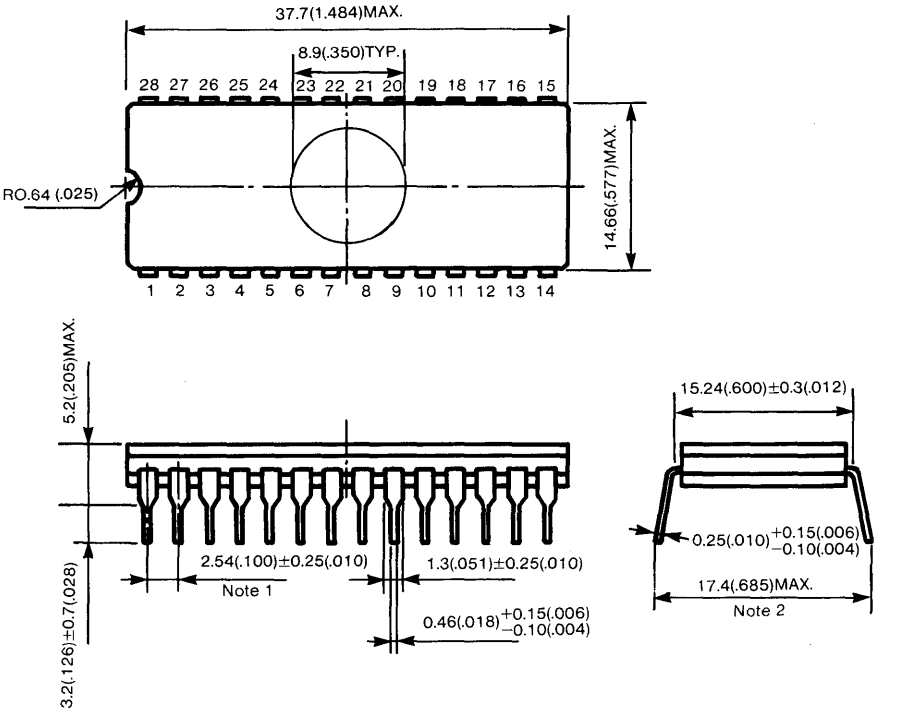
Electric signature mode allows to read out a code from TMM27512D which identifies its manufacturer and device type.
The programming equipment may read out manufacturer code and device code from TMM27512D by using this mode before program operation automatically set program voltage (V_{PP}) and algorithm.
Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07.)
The following table shows electric signature of TMM27512D.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	1	0	1	0	1	15

Notes: A9=12V±0.5V
A1~A8, A10~A15, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWING

Unit in mm (inches)



Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.

2. This value is measured at the end of leads.

CMOS Erasable/Programmable Read Only Memories

TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD X 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABEL READ ONLY MEMORY

TC57256D-20
TC57256D-25

SILICON STACKED GATE MOS

DESCRIPTION

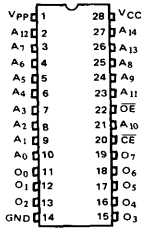
The TC57256D is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC 57256D's access time is 200ns, and the TC57256D operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technnology reduces the maximum active current to 30 mA/5MHz and standby current to 100μA.

For program operation, the programming is achieved by using the high speed programming mode. Program supply voltage is 21V which is the same voltage as TMM2764D and TMM27128D. The programming of TC57256D is accomplished within about one and a half minutes (typ.) TC57256D is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

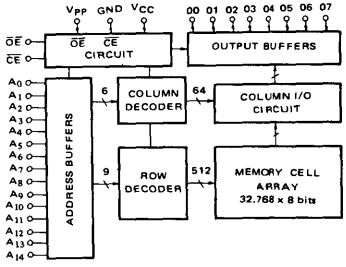
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  30mA/5MHZ (active)
  100μA (standby)
- Fast access time TC57256D-20 200 ns
  TC57256D-25 250 ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P and TMM23256P
- Standard 28 pin DIP cerdip Package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H		5V	High Impedance	
Standby	H	*		5V	High Impedance	Standby
Program	L	H	21V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	L	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	−0.6 ~ 22.0	V
V_{IN}	Input Voltage	−0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	−65 ~ 125	°C
T_{OPR}	Operating Temperature	−40 ~ 85	°C

READ OPERATION
D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC} + 0.3	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input current	V_{IN} = 0 ~ V_{CC}		–	–	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$ = 0	f = 5MHz	–	–	30	mA
I_{CC02}			f = 1MHz	–	–	10	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}		–	–	1	mA
I_{CCS2}		$\overline{CE}$ = V_{CC} −0.2V		–	–	100	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA		2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		–	–	0.4	V
I_{PP1}	V_{PP} Current	V_{PP} = 0 ~ V_{CC} + 0.3V		–	–	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V ~ V_{CC}		–	–	±10	μA

A. C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{CC} = 5V ±5%, V_{PP} = 2.0V ~ V_{CC} + 0.3V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256D-20		TC57256D-25		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	200	–	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}	–	200	–	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}	–	70	–	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	0	60	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

A. C. TEST CONDITIONS

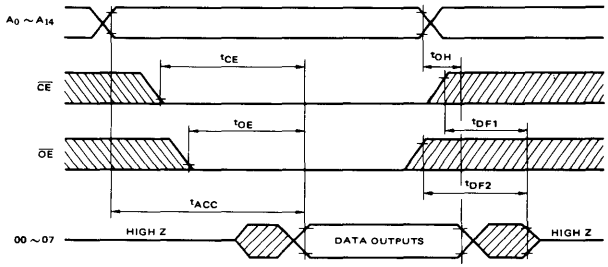
Output Load : 1 TTL Gate and C_L = 100pF
Input Pulse Rise and Fall Times : 10 ns Max.
Input Pulse Levels : 0.45 ~ 2.4V
Timing Mesurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	–	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	–	8	12	pF

*This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION
D.C. RECOMMENDED OPERATING CONDITONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D.C. and OPERATING CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 21.5V	–	–	30	mA

A.C. PROGRAMMING CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 21V \pm 0.5$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	μs
t_{OEH}	$\overline{OE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	0.95	1	21	ms
t_{DV}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	–	–	1	μs
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	–	–	150	ns

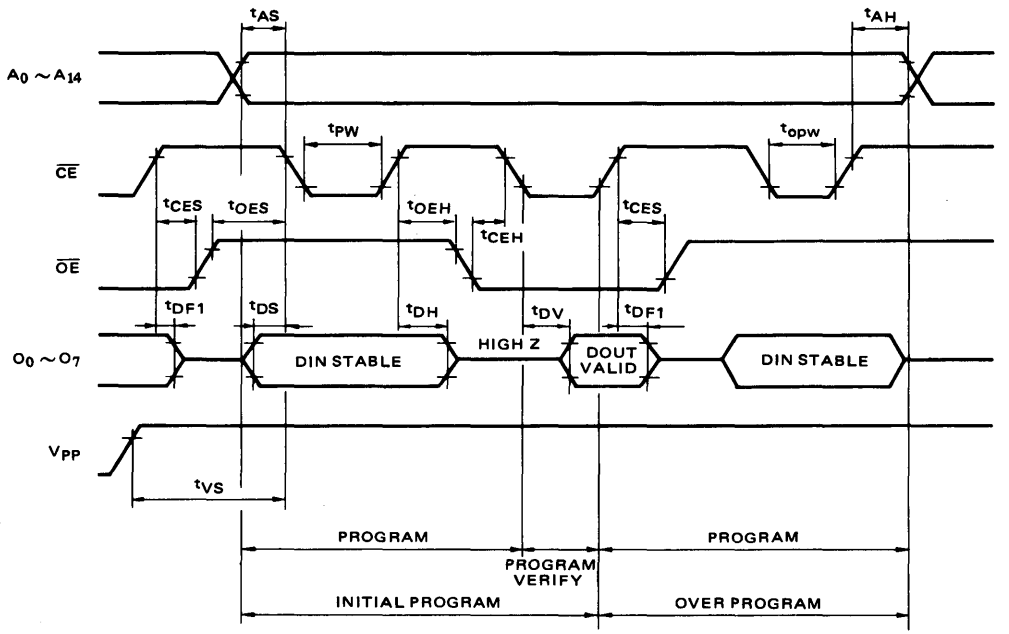
A. C. TEST CONDITIONS

Output Load	:	1 TTL Gate and C_L (100pF)
Input Pulse Rise and Fall Times	:	10 ns Max.
Input Pulse Levels	:	0.45 ~ 2.4V
Timing Measurement Reference Level	:	Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1 : The length of the overprogram pulse may vary as function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC} = 6V ±0.25V, V_{PP} = 21V ± 0.5V)



Note: (1) V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
(2) Removing the device from socket and setting the device in socket with V_{PP} = 21V may cause permanent damage to the device.
(3) The V_{PP} supply voltage is permitted up to 22V for program operation, so the voltage over 22V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pluse should not be exceeded 22V.

ERASURE CHARACTERISTICS

The TC57256D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.

Then integrated does (ultraviolet light intensity [w/cm^2] x exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm^2].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm^2] x (20 x 60) [sec.] $\cong$ 15 [w·sec/cm^2].)

The TC57256D's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000 ~ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seal Toshiba EPROM Protect Seal AC901 is available.

OPERATION INFORMATION

The TC57256D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read Operation (Ta = −40 ~ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta = 25 ±5°C)	Program	L	H	21V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	L	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{CE}$ = $\overline{OE}$ = V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$ = V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, the outputs will be in a high impedance state. So two or more TC57256D's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256D has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC57256D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256D are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TC57256D is in the programming mode when the V_{PP} input is at 21V and $\overline{CE}$ is at TTL-Low under $\overline{OE}$ = V_{IH}.

The TC57256D can be programmed any location at anytime eitehr individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The varify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC57256D from being programmed.

Programming of two or more TC57256Ds in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with V_{CC} = 6V.

The programming is acheived by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

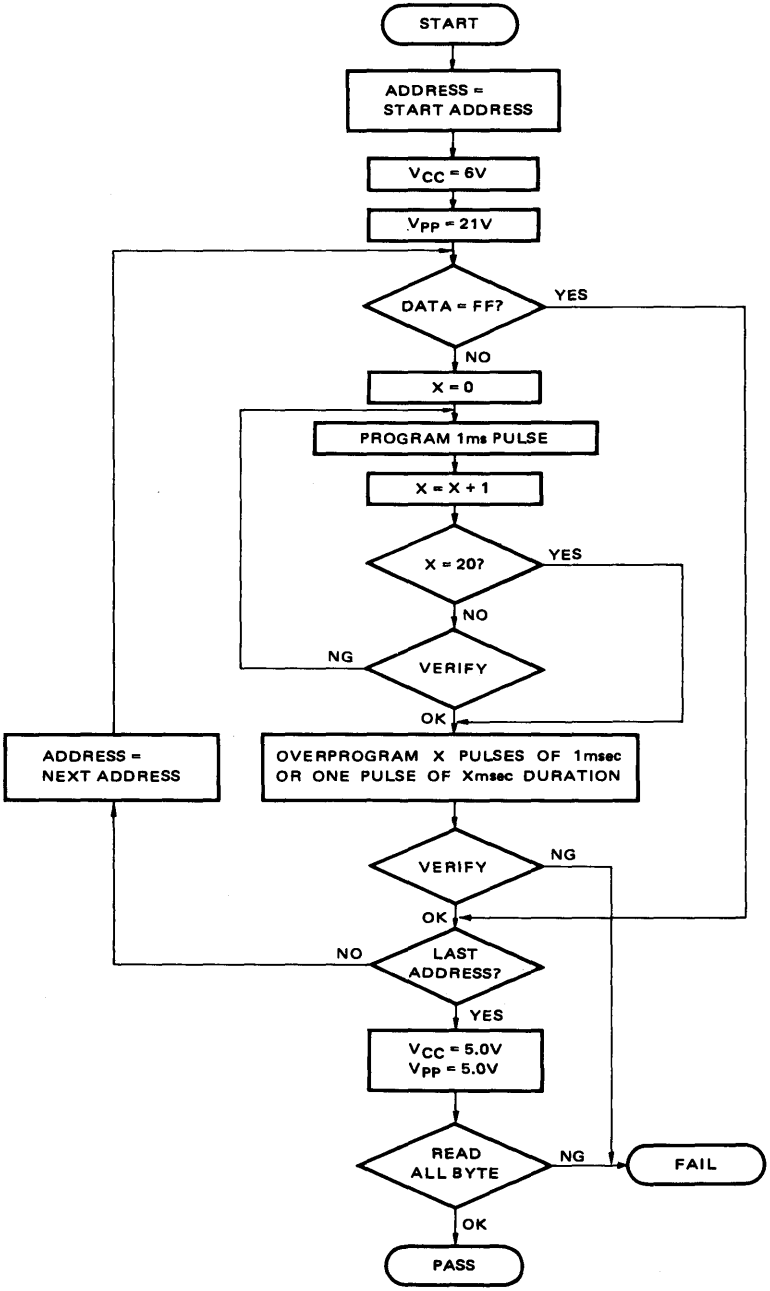
If the programmed data is not correct, another program pulse of 1ms is applied and the programmed data is verified. This should be repeated until the program operates correctly (max. 20 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be varified with V_{CC} = V_{PP} = 5V.

This high speed program algorithm allows the programming of the TC57256D to be accomplished within one and a half minutes (typ.).

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256D which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

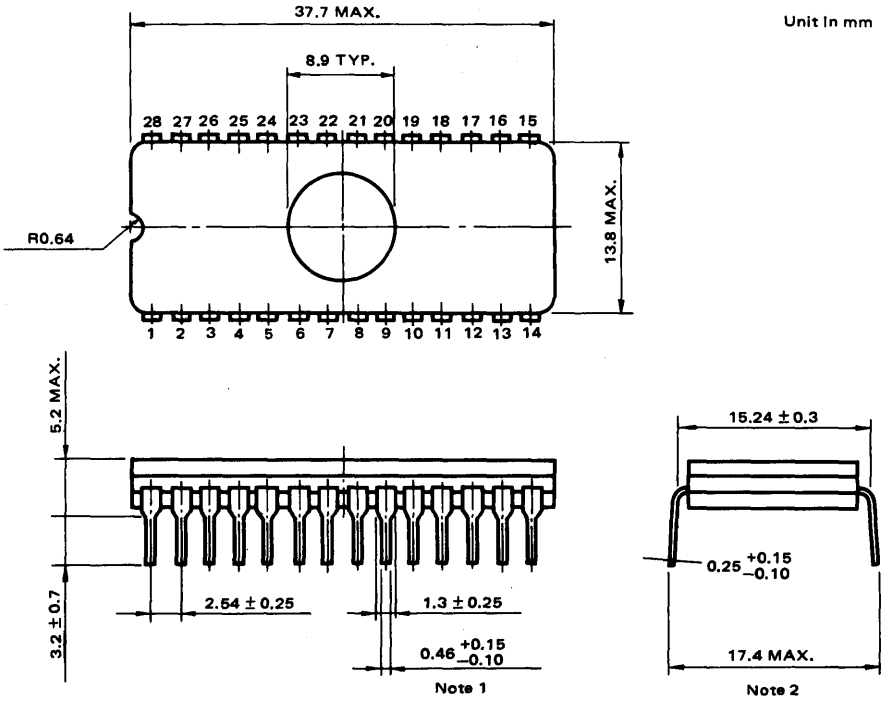
Electric Signature mode is set up when 12V is applied to address line A_9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A_0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O_7).

The following table shows electric signature of TC57256D.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

Notes: $A_9 = 12V \pm 0.5V$
$A_1 - A_8$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS



Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.
2. This value is meesured at the end of leads.
3. All dimensions are in millimeters.

NMOS One Time Programmable Memories

TOSHIBA MOS MEMORY PRODUCTS

TMM2464AP

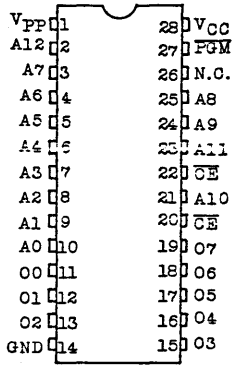
DESCRIPTION

The TMM2464AP/AF is a 8,192 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic DIP.
The TMM2464AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time.
The electrical characteristics and programming method are the same as U.V. EPROM TMM2764AD's.
Once programed, the TMM2464AP/AF can not be erased because of using plastic DIP without transparent window.

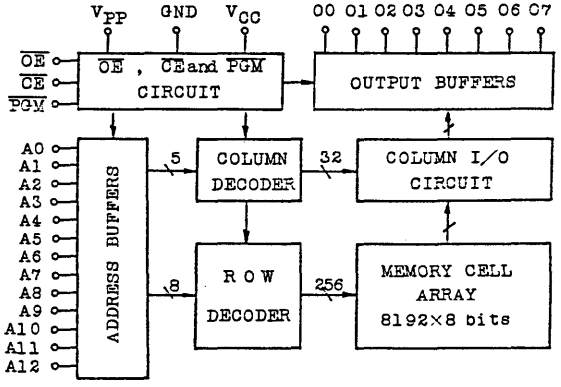
FEATURES

- Single 5 volt power supply
- Fast access time: 200ns (Max.)
- Power dissipation: 100mA(active current) Max.
  30mA(standby current) Max.
- Low power standby mode: $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Compatible with TMM2764AD and ROM TMM2365P, TC5365P.
- 28 PIN standard plastic package : TMM2464AP
- 28 PIN flat package: TMM2464AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A12	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N.C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verity	H	L	L			Data Out	

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V_{IN}	Input Voltage	-0.6 ~ 7.0	V
V_{OUT}	Output Voltage	-0.6 ~ 7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
$T_{STRG.}$	Storage Temperature	-55 ~ 150	°C
$T_{OPR.}$	Operating Temperature	0 ~ 70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	

D.C. and OPERATING CHARACTERISTICS

(Ta=0 ~ 70°C, V_{CC}=5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ~ V_{CC}	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-	-	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-	-	100	mA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0 ~ V_{CC}+0.6	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ~ V_{CC}	-	-	±10	μA

A.C. CHARACTERISTICS

($Ta=0 \sim 70°C$, $V_{CC}=5V \pm 5\%$, $V_{PP}=2.0V \sim V_{CC}+0.6V$, Unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	-	70	ns
t_{DF1}	$\overline{CE}$ to Output to High-Z	0	60	ns
t_{DF2}	$\overline{OE}$ to Output to High-Z	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output High-Z	0	60	ns
t_{OH}	Output Data Hold Time	0	-	ns

AC TEST CONDITIONS

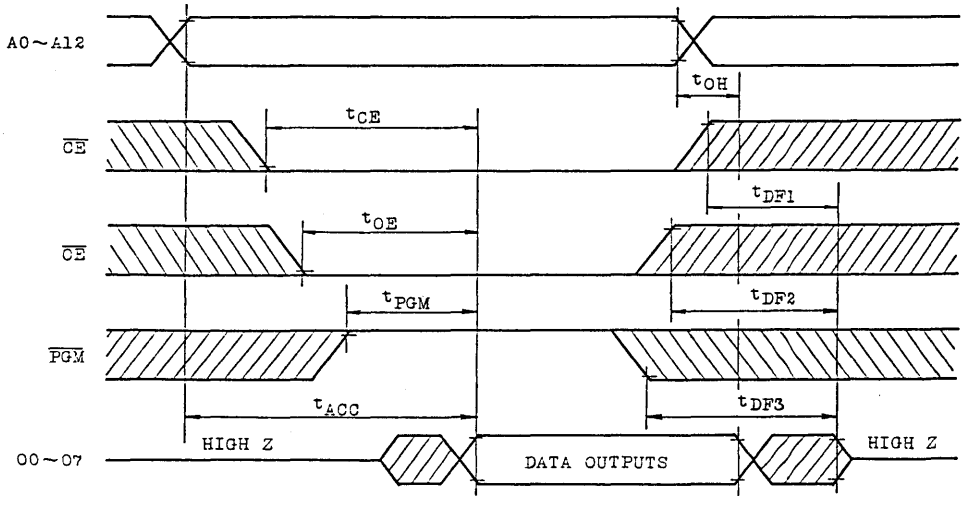
- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * ($Ta=25°C$, $f=1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS ($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

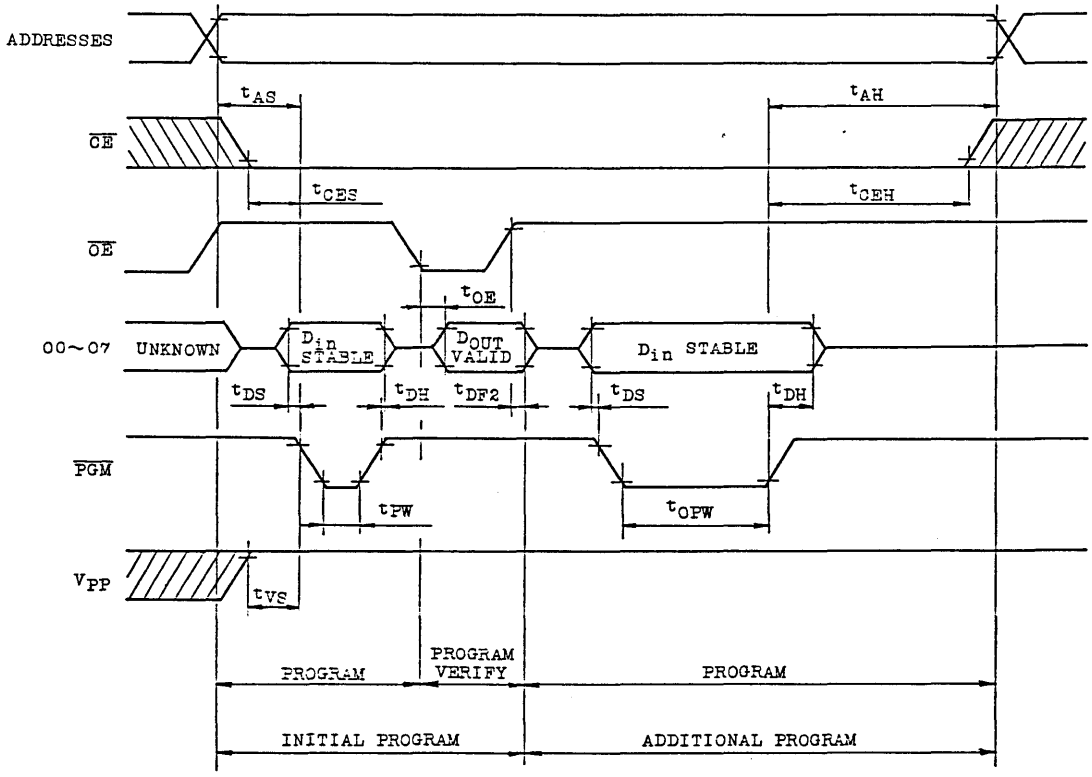
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: t_{OPW} depend on the program pulse width which is required in the initial program.

TIMING WAVEFORMS (HIGH SPEED PROGRAM)



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM2464AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
READ OPERATION (Ta=0 ∿ 70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM2464AP/AF has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.
And assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM2464AP/AF can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2464AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a TTL high level to the $\overline{CE}$ input, the TMM2464AP/AF is placed in the standby mode which reduce the operating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

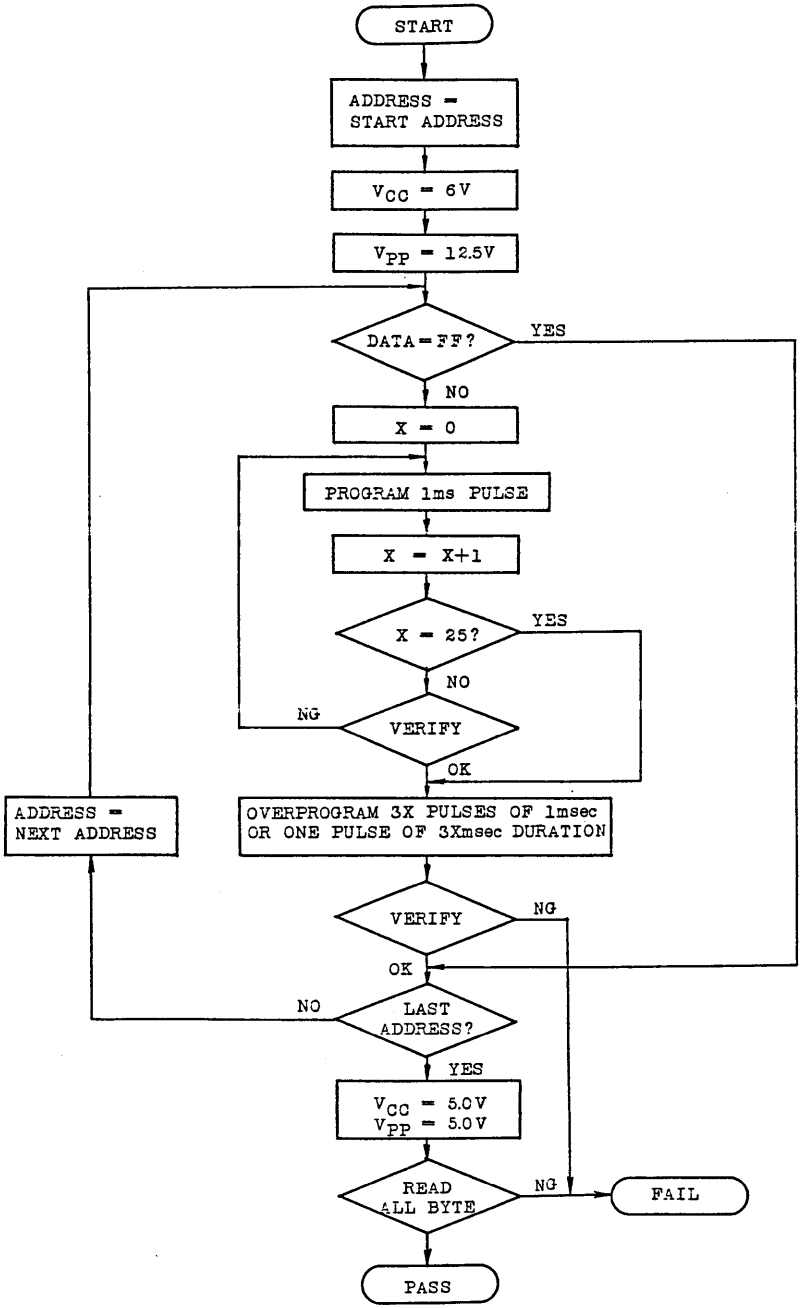
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2464AP/AF from being programmed. Programming of two or more TMM2464AP/AF in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}.
The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.
When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM2464AP/AF which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TMM2464AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

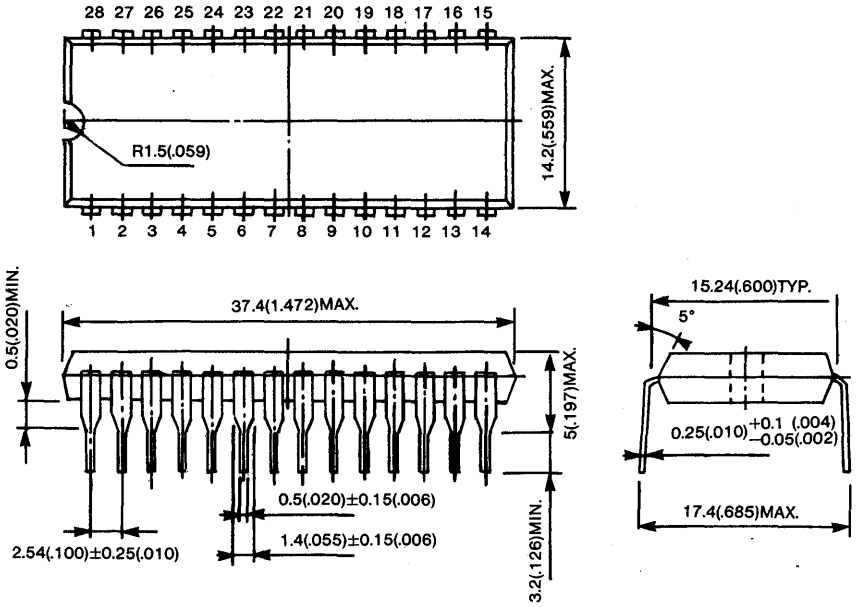
The following table shows electric signature of TMM2464AP/AF.

PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	0	1	0	52

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A12, $\overline{CE}$, $\overline{OE}=V_{IL}$ $\overline{PGM}=V_{IH}$

OUTLINE DRAWINGS (TMM2464AP)



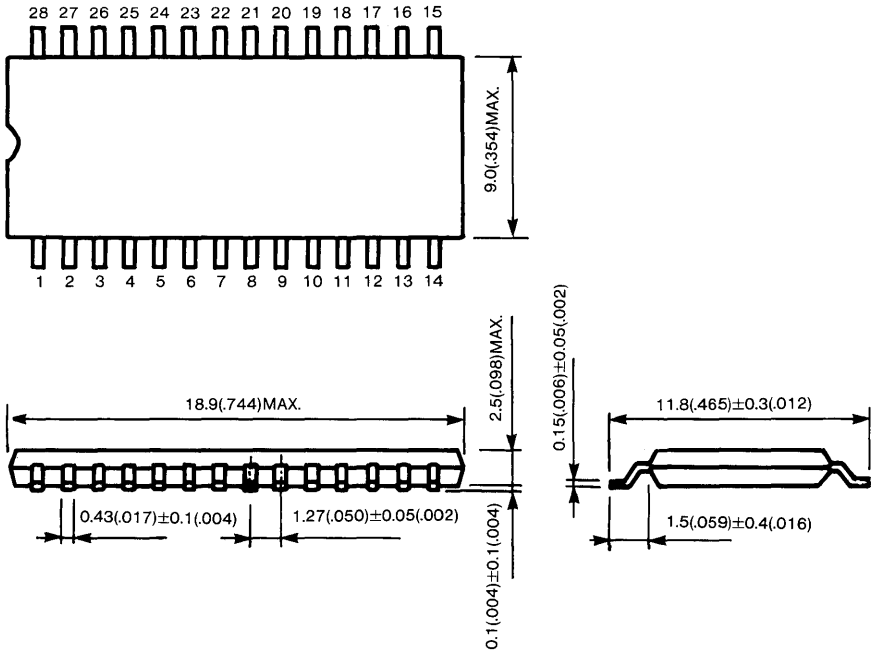
Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM2464AF)

Unit in mm (inches)



Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TMM24128AP

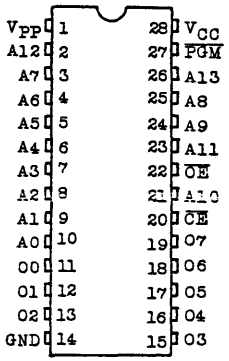
DESCRIPTION

The TMM24128AP/AF is a 16,384 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic DIP. TMM24128AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TMM27128AD's. Once programed, the TMM24128AP/AF can not be erased because of using plastic DIP without transparent window.

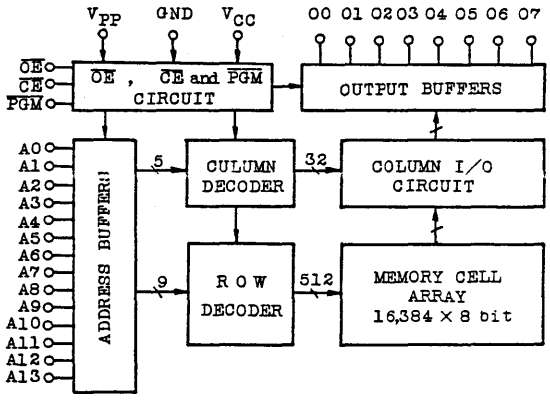
FEATURES

- Single 5 volt power supply
- Fast access time: 200ns (Max.)
- Power dissipation: 100mA (active current) Max.
  30mA (standby current) Max.
- Low power standby mode: $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Compatible with TMM27128AD and MASK ROM TMM23128P
- 28 PIN standard plastic package :TMM24128AP
- 28 PIN flat package: TMM24128AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A13	Address Inputs
D0 ∿ D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
V_{OUT}	Output Voltage	-0.6 ∿ 7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
$T_{STRG.}$	Storage Temperature	-55 ∿ 150	°C
$T_{OPR.}$	Operating Temperature	0 ∿ 70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D.C. and OPERATING CHARACTERISTICS

(Ta=0 ∿ 70°C, V_{CC}=5V±5% Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-	-	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-	-	100	mA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0 ∿ V_{CC}+0.6	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ∿ V_{CC}	-	-	±10	μA

A.C. CHARACTERISTICS

($Ta=0 \sim 70°C$, $V_{CC}=5V \pm 5\%$, $Vpp=2.0V \sim V_{CC}+0.6V$, Unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	ns
t_{OH}	Output Data Hold Time	0	-	ns

A.C. TEST CONDITION

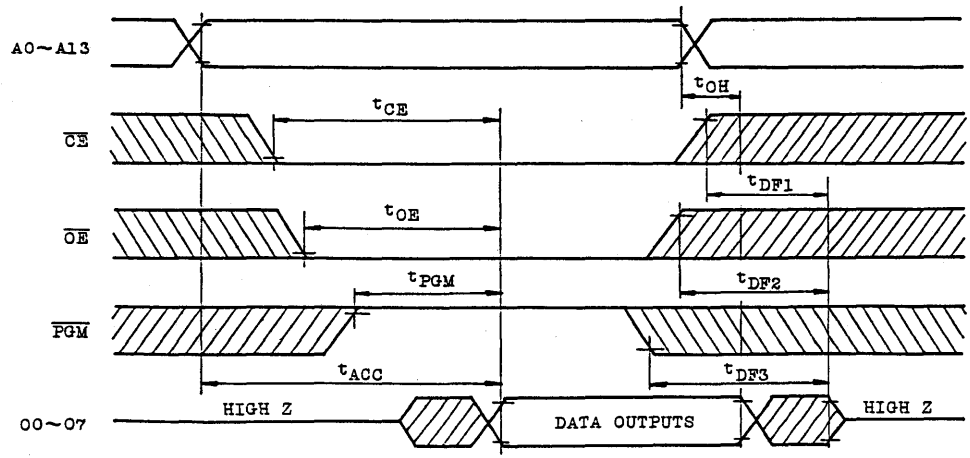
- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * ($Ta=25°C$, $f=1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	-	8	12	pF

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

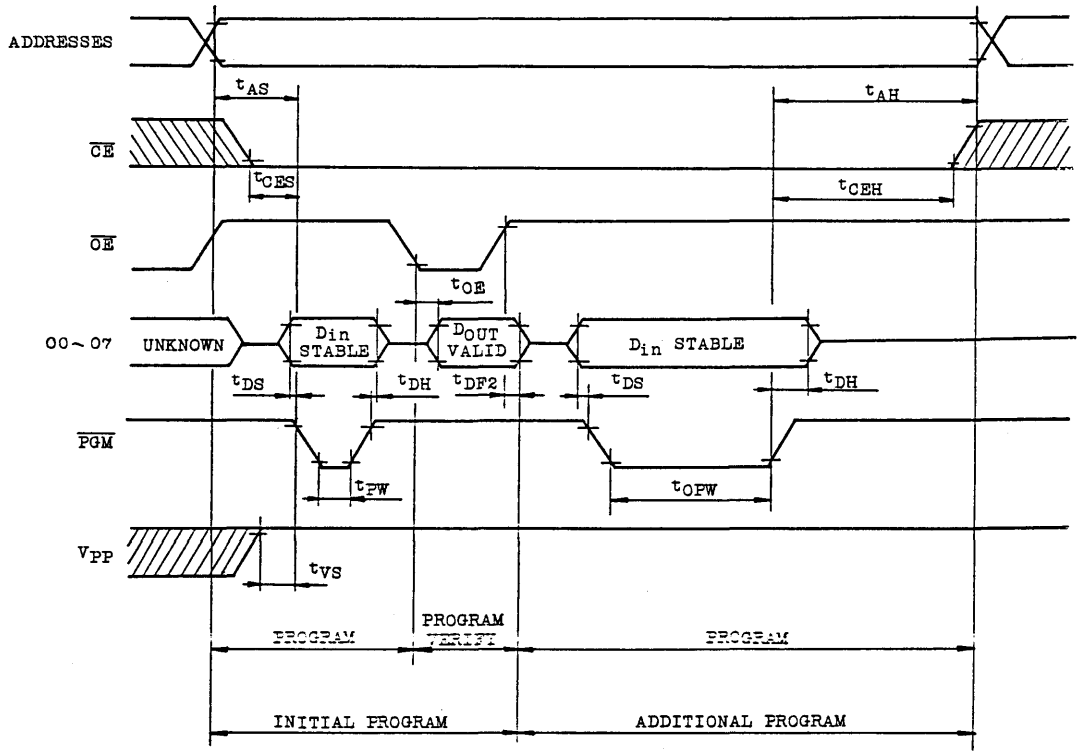
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	-	-	90	ns

A.C. TEST CONDITIONS

Output Load : 1 TTL Gate and C_L(100pF)
Input Pulse Rise and Fall Time : 10ns Max.
Input Pulse Levels : 0.45V and 2.4V
Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: t_{OPW} depens on the program pulse width which is required in the initial program.

TIMING WAVEFORMS (HIGH SPEED PROGRAM)



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24128AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
READ OPERATION (Ta=0 ∿ 70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM24128AP/AF has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.
And assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM24128AP/AF can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24128AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a TTL high level to the $\overline{CE}$ input, the TMM24128AP/AF is placed in the standby mode which reduce the operating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

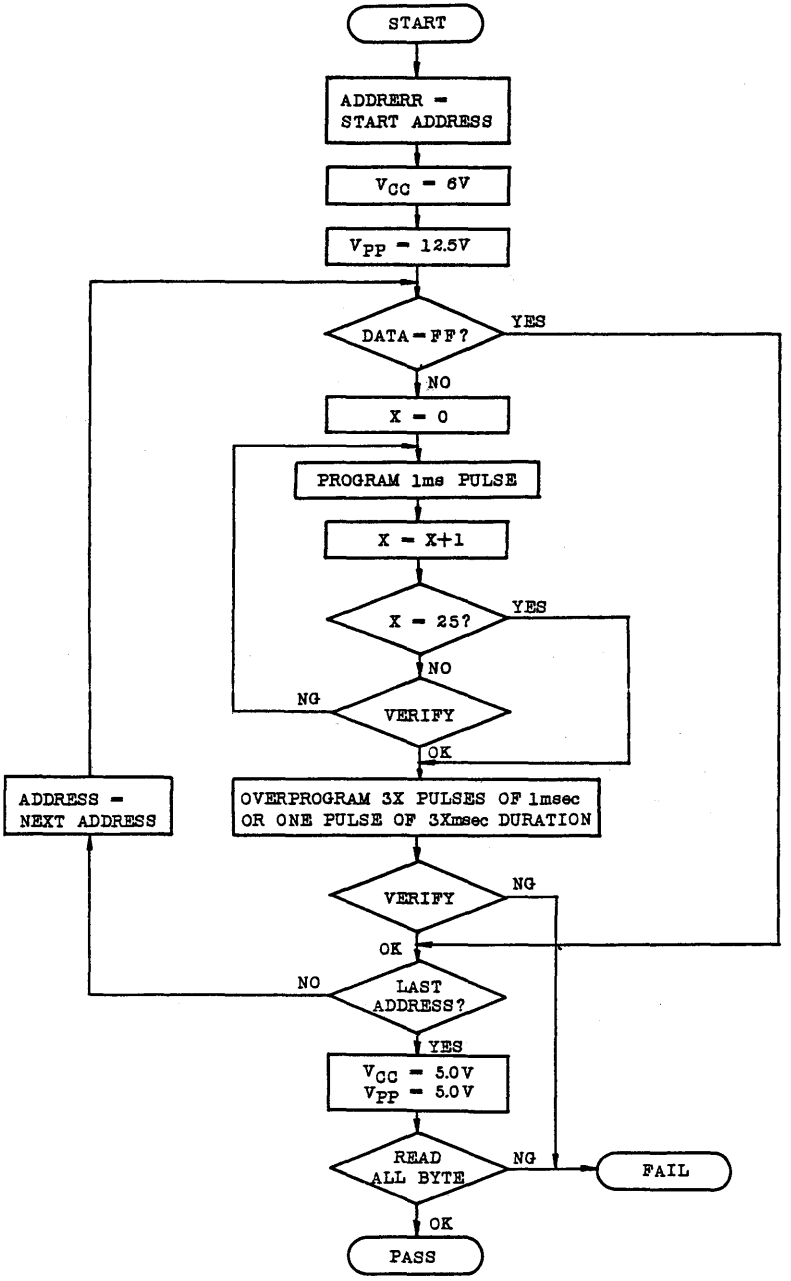
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to Vpp terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM24128AP/AF from being programmed. Programming of two or more TMM24128AP/AF in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the Vpp terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}.
The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.
When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24128AP/AF which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TMM24128AP/AF by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

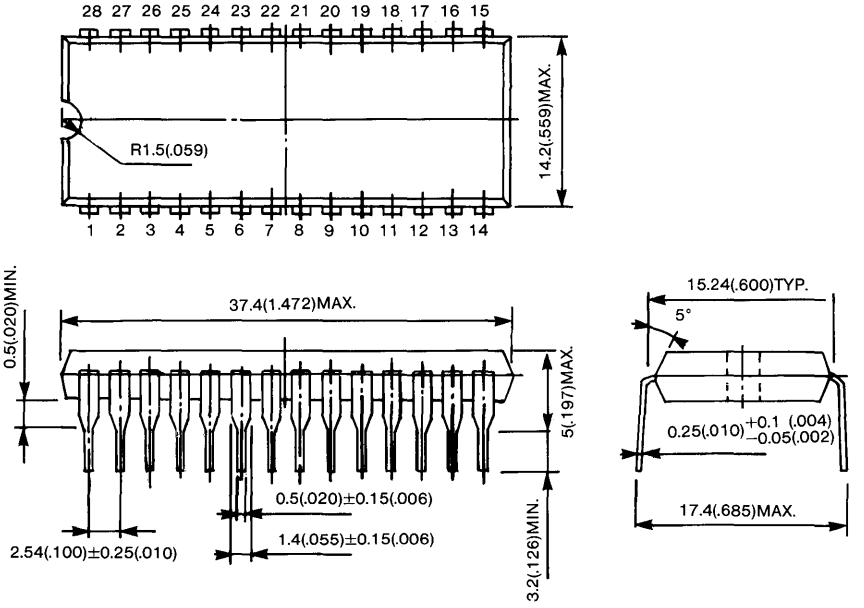
Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7). The following table shows electric signature of TMM24128AP/AF.

PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	1	0	0	1	1	D3

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A13, $\overline{CE}$, $\overline{CE}$=V_{IL} $\overline{PGM}$=V_{IH}

OUTLINE DRAWINGS (TMM24128AP)



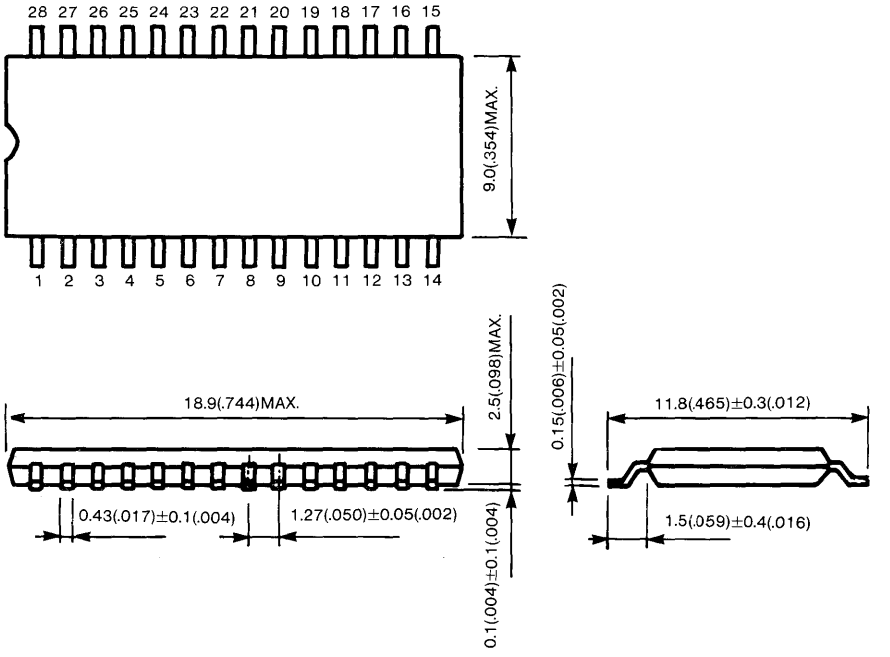
Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24128AF)

Unit in mm (inches)



Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No. 28 leads.

TOSHIBA MOS MEMORY PRODUCTS

32,763 WORD × 8 BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY

SILICON STACKED GATE MOS

TMM24256AP/AF

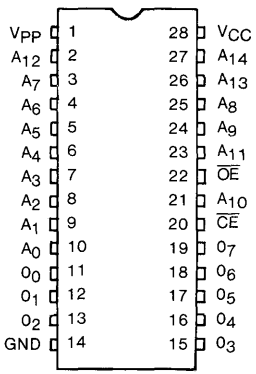
DESCRIPTION

The TMM24256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic Package.
The TMM24256AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time.
The electrical characteristics and programming method are the same as U.V. EPROM TMM27256AD's.
Once programmed, the TMM24256AP/AF can not be erased because of using plastic DIP without transparent window.

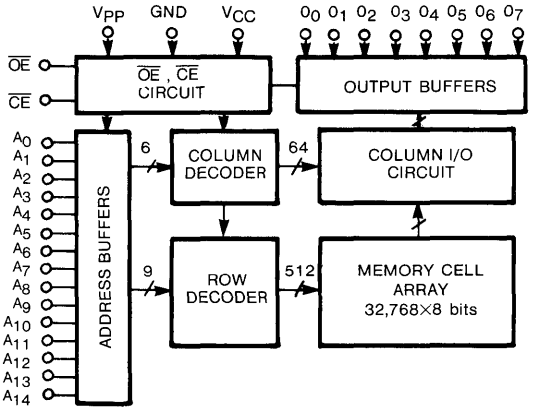
FEATURES

- Fast access time : 200ns
- Low power dissipation
  Active : 100 mA
  Standby : 30 mA
- Single 5V power supply
- Fully static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD and TC57256D
- Standard 28 pin DIP plastic package : TMM24256AP
- Plastic Flat Package : TMM24256AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibits	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input / Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature	260 · 10	°C · sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D.C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$ =V_{IH}	-	-	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$ =V_{IL}	-	-	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6V	-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}	-	-	±10	μA

A.C. CHARACTERISTICS ($Ta=0\sim70°C$, $V_{CC}=5V\pm5\%$, $V_{PP}=2.0V\sim V_{CC}+0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	ns
t_{OH}	Output Data in Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L=100$ pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Level : 0.45V~2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

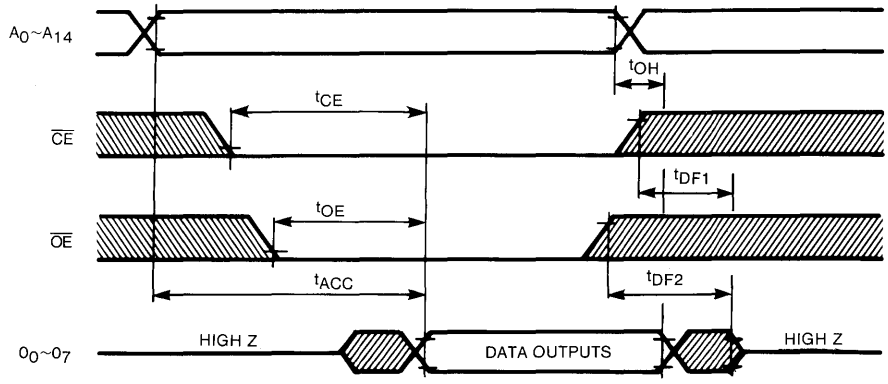
CAPACITANCE * ($Ta=25°C$, $f=1MHz$))

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

(READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

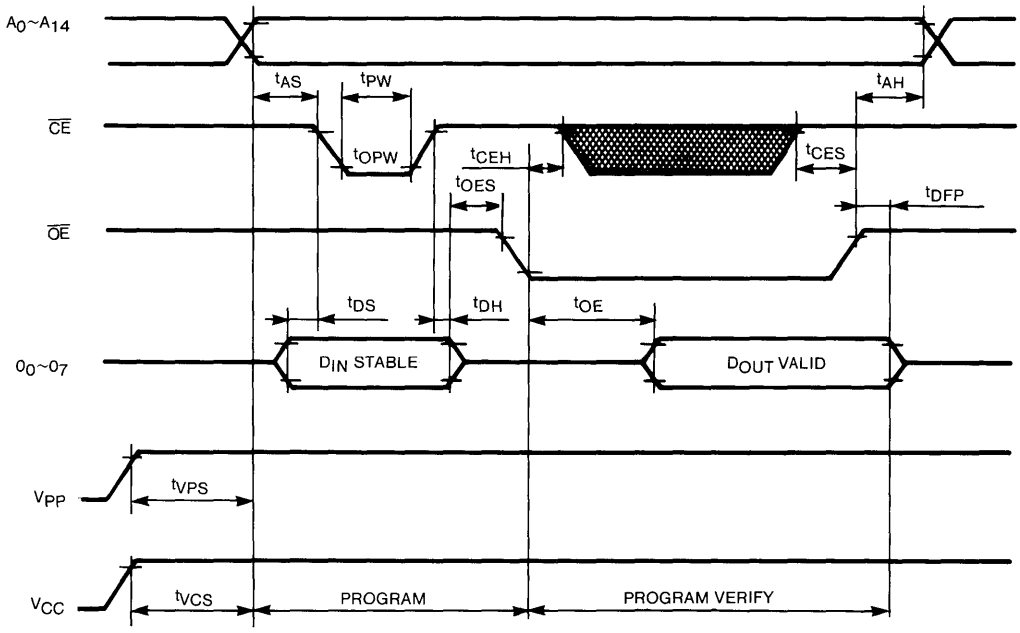
A.C. TEST CONDITIONS

Output Load : 1 TTL Gate and C_L (100pF)
Input Pulse Rise and Fall Times : 10ns Max.
Input Pulse Levels : 0.45V~2.4V
Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM24256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming the $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TMM24256AP/AF's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ inputs, the TMM24256AP/AF is placed in the standby mode which reduces the operating current to 30mA from 100mA (about 70% reduction) and the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM24256AP/AF are in the "1" state which is erased state.
Therefore the program operation is to introduce "O's" data into the desired bit locations by electrically programming.
The TMM24256AP/AF is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$.
The TMM24256AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

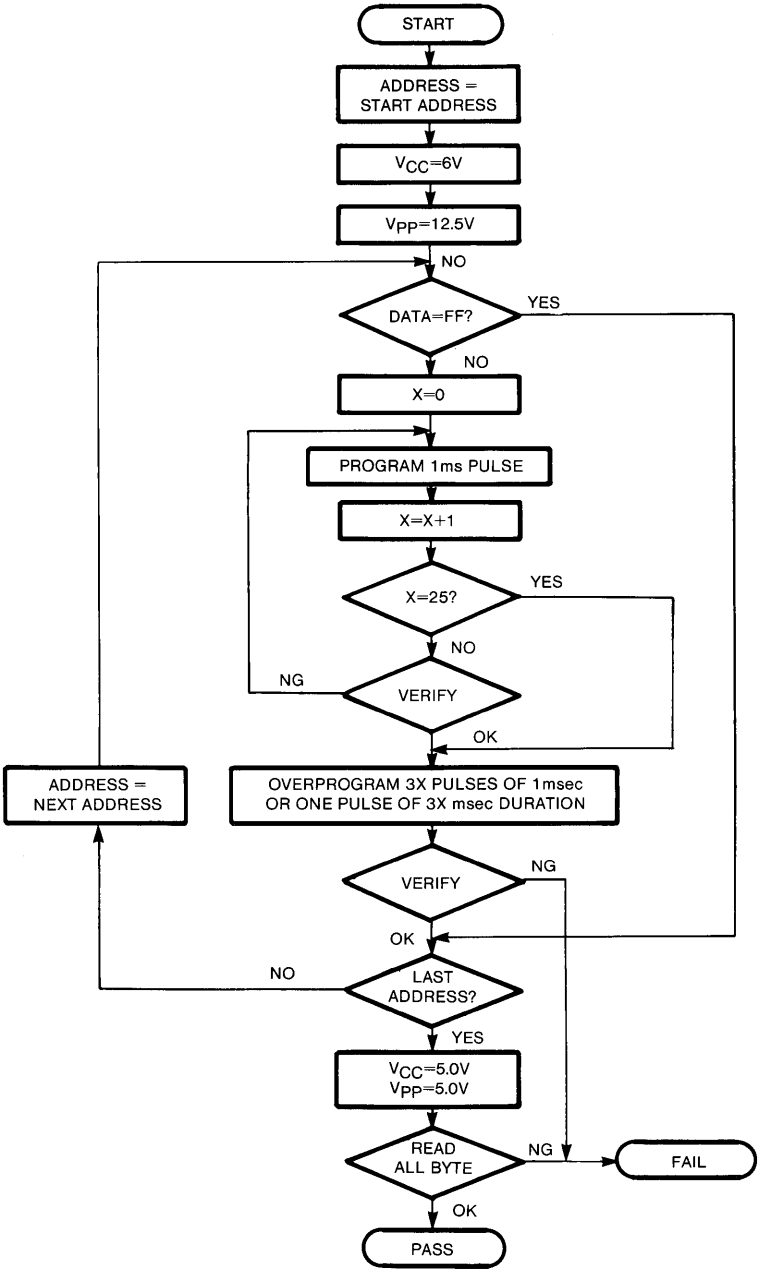
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM24256AP/AF from being programmed.
Programming of two or more TMM24256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24256AP/AF by using this mode before program operation automatically set program voltage (V_{PP}) and algorithm. Electric Signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} for read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07)

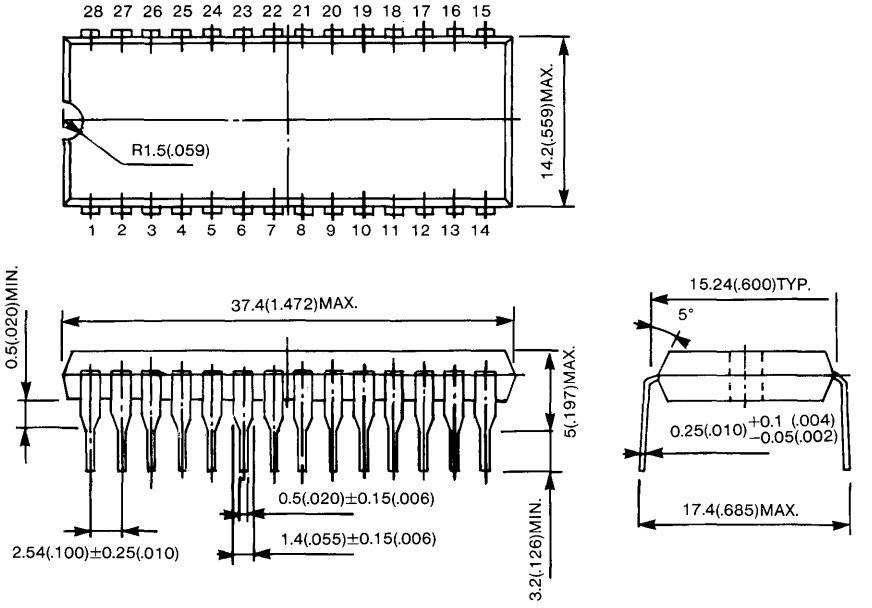
The following table shows electric signature of TMM24256AP/AF.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

Notes: A9=12V±0.5V
A1~A8, A10~A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

OUTLINE DRAWING (TMM24256AP)

Unit in mm (inches)

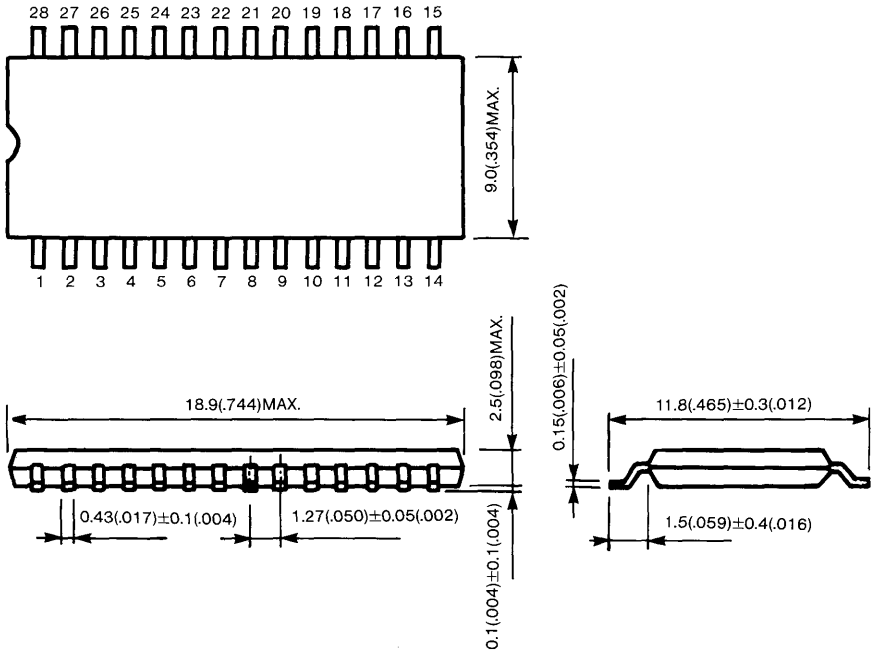


Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.

2. This value is measured at the end of leads.

OUTLINE DRAWING (TMM24256AF)

Unit in mm (inches)



Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

NMOS Mask Read Only Memories

TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM2365P

DESCRIPTION

The TMM2365P is a 65536 bit fully static read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using microprocessor.

The TMM2365P is fully compatible with a 64 K bits EPROM TMM2764D, so completely replace EPROM socket.

The TMM2365P also features an automatic standby power mode. When deselected by Chip Enable ($CE_1 \sim {}_3/\overline{CE_1 \sim {}_3}$), the operating current is reduced from 100mA (MAX) to 25mA(MAX). Output Enable ($\overline{OE}$) is effective in preventing data confliction of a common bus line.

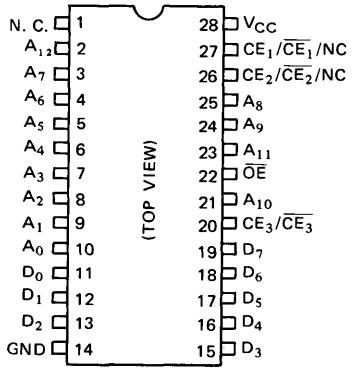
The TMM2365P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production of high performance.

The TMM2365P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V power Supply
- Access Time: 200ns max.
- Power Dissipation
  - Average Current: 100mA max.
  - Standby Current: 25mA max.
- Input and Output: TTL Compatible
- Three State Outputs: Wired OR Capability
- Output Buffer Control: $\overline{OE}$
- Programmable Chip Enable: $CE_1/\overline{CE_1}$, CE_2/CE_2 $CE_3/\overline{CE_3}$
  Easy Memory Expansion
- Compatible with 64K EPROM TMM2764D

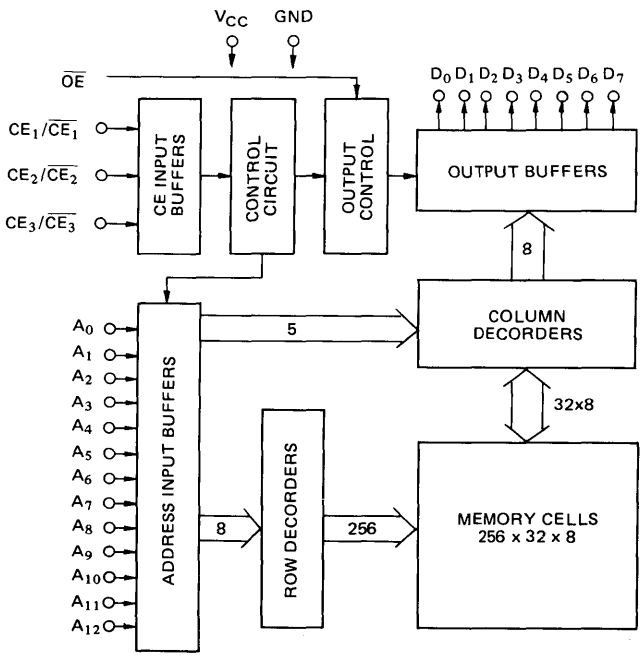
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
$\overline{OE}$	Output enable input
$CE_1/\overline{CE_1}$, $CE_2/\overline{CE_2}$, $CE_3/\overline{CE_3}$	Chip enable inputs
N. C.	No connection
V_{CC}	Power supply terminal
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{SD}	Soldering Temperature • Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	–	2.0	–	V_{CC}+1	V
V_{IL}	Input Low Voltage	–	−0.5	–	0.8	V
V_{CC}	Power Supply Voltage	–	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.5V	–	10	μA
I_{IL}	Input Low Current	V_{IN} = GND	–	−10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA	–	0.4	V
I_{LO}	Output Leakage Current	$0V \leqq V_{OUT} \leqq Vcc$	−10	10	μA
I_{CC1}	Standby Current	$\overline{CE}$ = 2.0V, CE = 0.8V	–	25	mA
I_{CC2}	Average Current	t_{CYC}=200nS, I_{OUT}=0mA	–	100	mA

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	200	ns
t_{CE}	Output Delay Time from $CE_{1\sim3}/\overline{CE_{1\sim3}}$	–	200	ns
t_{OE}	Output Delay Time from $\overline{OE}$	–	70	ns
t_{OD}	Output Turn off Delay	–	60	ns
t_{CYC}	Cycle Time	200	–	ns

A.C. TEST CONDITIONS

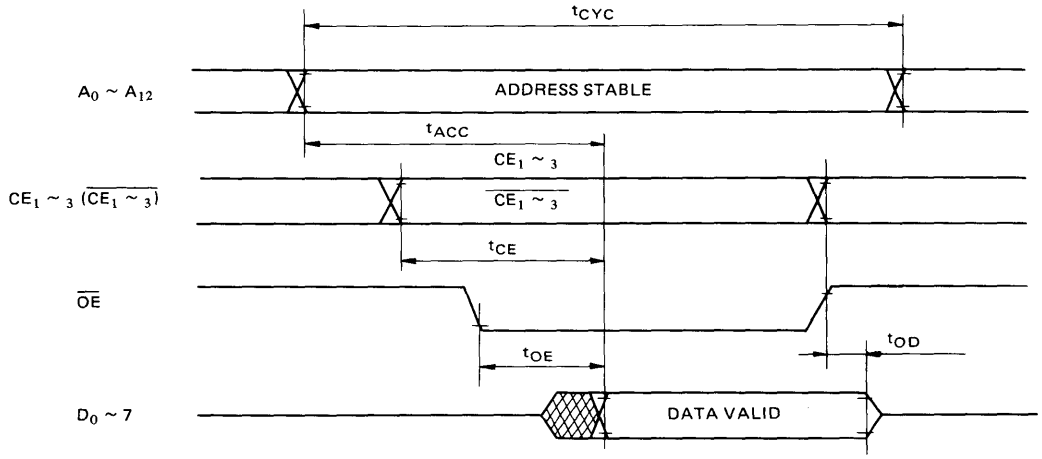
- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5 ns
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Levels :
  Input ; 1V and 2.0V
  Output; 0.8V and 2.0V

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. GND	–	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. GND	–	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

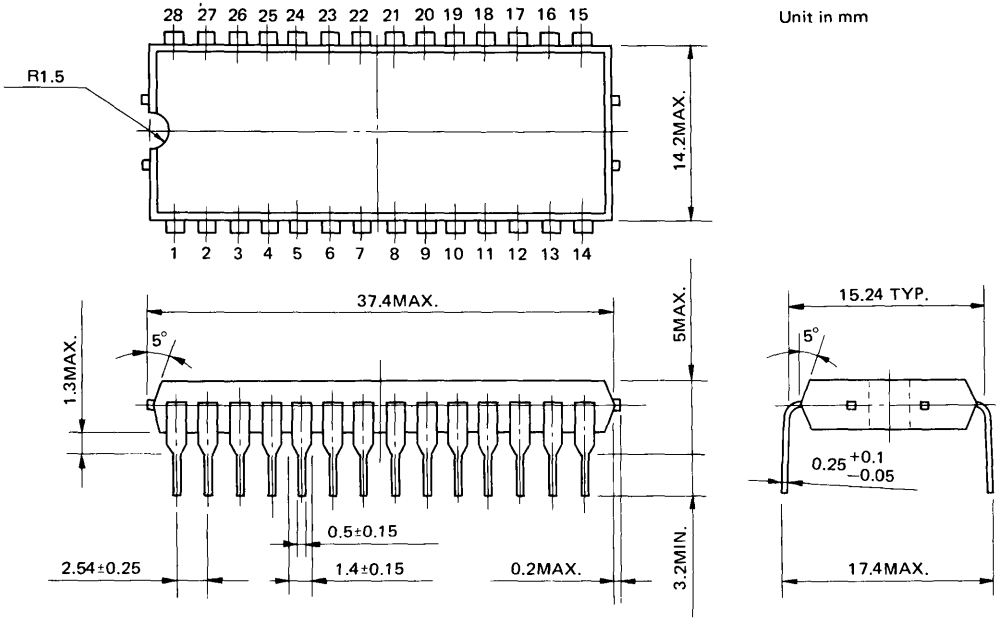


Note: t_{OD} is specified from $\overline{OE}$ or CE/$\overline{CE}$, whichever occurs first.

POWER ON

The TMM2365 has self substrate-bias generator internally. So a minimum 100μs time delay is required after the application of V_{CC} (4.5 ~ 5.5V) before proper device operation is achieved.

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCTS

64K BIT (8K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE MOS

TMM2366P

DESCRIPTION

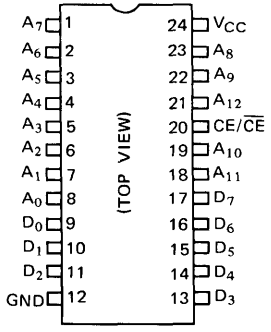
The TMM2366P is a 65536 bit fully static read only memory organized as 8192 words by 8 bits with a low bit cost, thus being most suitable for use in programming of production apparatus using microprocessor.
The TMM2366P also features an automatic standby power mode. When deselected by Chip Enable (CE/$\overline{CE}$), the operating current is reduced from 100mA (MAX) to 25mA (MAX).

The TMM2366P is fabricated with ion implanted N-channel silicon gate technology.
This technology allows a production of high performance.
The TMM2366P is moulded in a 24 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V power Supply
- Access Time: 200ns max.
- Power Dissipation
  Average Current: 100mA max.
  Standby Current: 25mA max.
- Input and Output: TTL Compatible
- Three State Outputs: Wired OR Capability
- Programmable Chip Enable: CE/$\overline{CE}$
- Compatible with TMS4764

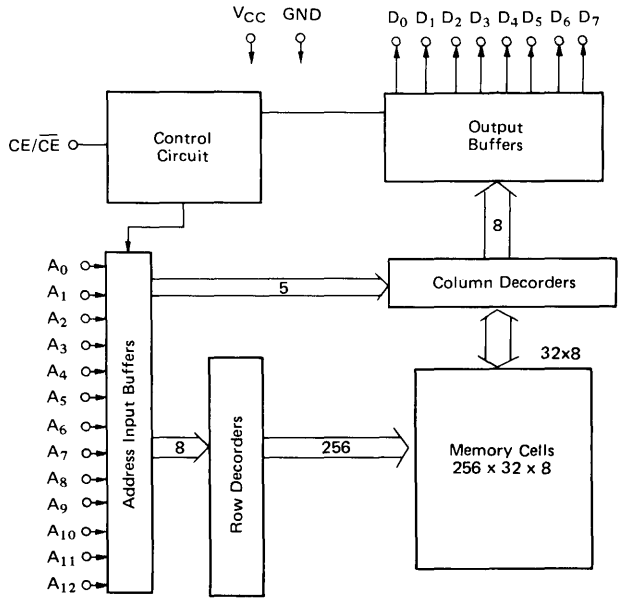
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
CE/$\overline{CE}$	Chip enable input
V_{CC}	Power supply terminal
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	−55 ~ 150	°C
T_{SD}	Soldering Temperature Time	260 • 10	°C • sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	–	2.0	–	V_{CC}+1	V
V_{IL}	Input Low Voltage	–	−0.5	–	0.8	V
V_{CC}	Power Supply Voltage	–	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.5V	–	10	μA
I_{IL}	Input Low Current	V_{IN} = GND	–	−10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA	–	0.4	V
I_{LO}	Output Leakage Current	$0V \leqq V_{OUT} \leqq V_{CC}$	−10	10	μA
I_{CC1}	Standby Current	$\overline{CE}$ = 2.0V, CE = 0.8V	–	25	mA
I_{CC2}	Average Current	t_{CYC} = 200ns, I_{OUT} = 0mA	–	100	mA

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	200	ns
t_{CE}	Output Delay Time from CE/$\overline{CE}$	–	200	ns
t_{OD}	Output Turn off Delay	–	60	ns
t_{CYC}	Cycle Time	200	–	ns

A.C. TEST CONDITIONS

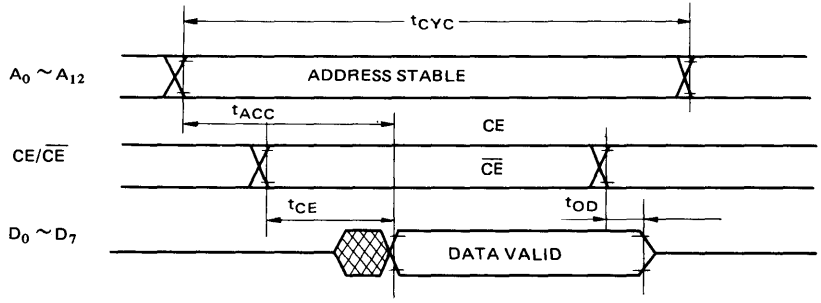
- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5 ns
- Input Pulse Levels : 0.8 ~ 2.2V
- Timing Measurement Reference Levels : Input; 1V and 2.0V
  Output; 0.8V and 2.0V

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitnace	V_{IN} = A.C. GND	–	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. GND	–	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

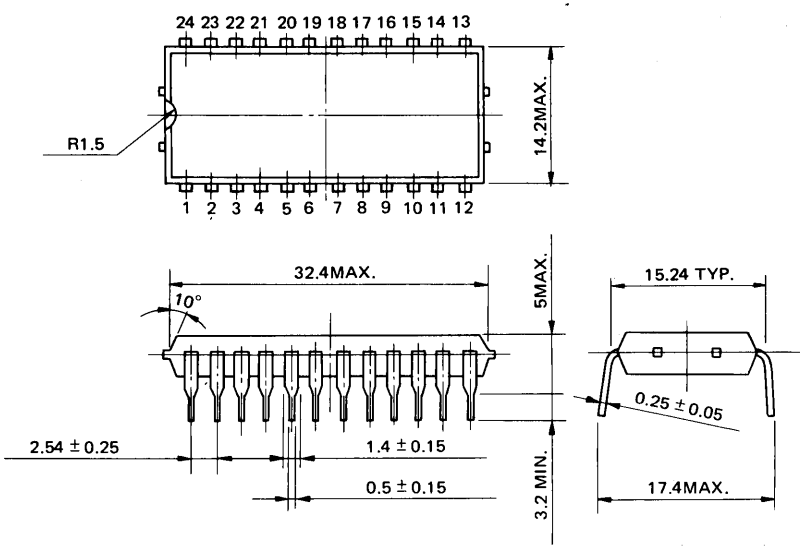
TIMING WAVEFORMS



POWER ON

The TMM2366 has a self substrate-bias generator internaly. So a minimum 100 μs time delay is required after the application of V_{CC} (4.5 ~ 5.5V) before proper device operation is achieved.

OUTLINE DRAWING



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

128K BIT (16K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM23128P

DESCRIPTION

The TMM23128P is a 131,072 bit read only memory organized as 16,384 words by 8 bits with low bit cost, thus being suitable for use in program memory for microprocessor and character generator.

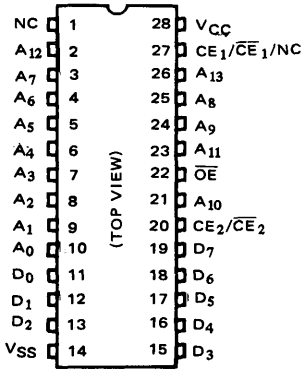
The TMM23128P is fully compatible with a 128K bits EPROM TMM27128D, so completely replace EPROM socket.

The TMM23128P also features an automatic standby power mode. When deselected by Chip Enable (CE_1, $2/\overline{CE}_1$, 2), the operating current is reduced form 80mA (Max.) to 20mA (Max.). Output Enable ($\overline{OE}$) is effective in preventing data confliction of a common bus line. The TMM23128P is fabricated with ion implanted N-channel silicon gate technology. The TMM23128P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

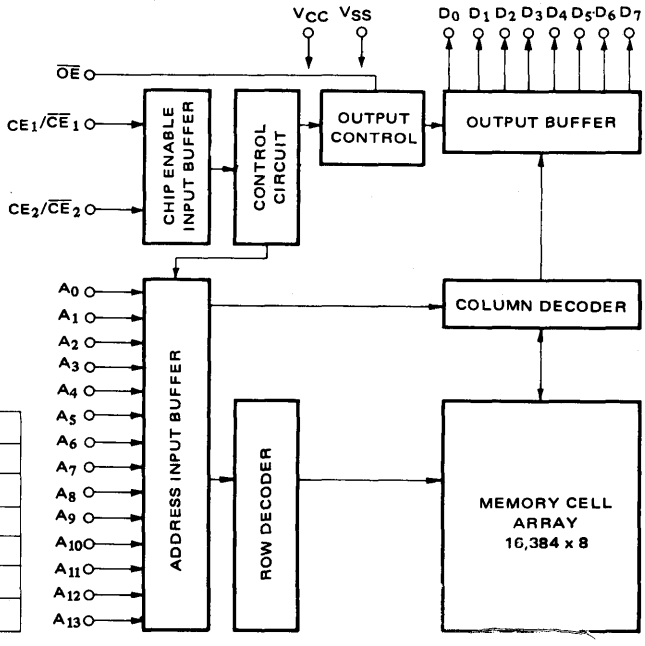
FEATURES

- Fully Static Operation
- 16,384 word x 8 bit Structure
- Single 5V Power Supply
- t_{ACC} = 200ns Max.
- T_{opr} = 0 ~ 70°C
- I_{CC} ope = 80mA Max.
- I_{CC} sby = 20mA Max.
- Input and Output TTL Compatible
- Three State Outputs
- Programmable Chip Enable
- Pin Compatible with EPROM TMM27128D
- 28 pin 600 mil. width DIP Plastic Package

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
$CE_1 \sim {}_2/\overline{CE}_1 \sim {}_2$	Chip Enable Inputs
$\overline{OE}$	Output Enable Input
NC	No Connection
V_{CC}	5V Power Supply
V_{SS}	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
P_D	Power Dissipation (Ta = 70°C)	1.0	W
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	ITEM	MIN.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{CC} + 1	V
V_{IL}	Input Low Voltage	−0.5	0.8	V

D.C. AND OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	ITEM	CONDITIONS	MIN.	MAX.	UNIT
I_{IN}	Input Current	$0V \leqq V_{IN} \leqq V_{CC}$	−	±10	μA
I_{LO}	Output Leakage Current	$0V \leqq V_{OUT} \leqq V_{CC}$	−	±10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−400	−	μA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	−	mA
I_{CC} ope	Operating Current	Min. Cycle	−	80	mA
I_{CC} sby	Standby Current	Note 1	−	20	mA

Note 1: Standby state occurs when either $CE_1/\overline{CE}_1$ or $CE_2/\overline{CE}_2$ is disenabled.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	ITEM	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = AC GND	−	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = AC GND	−	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

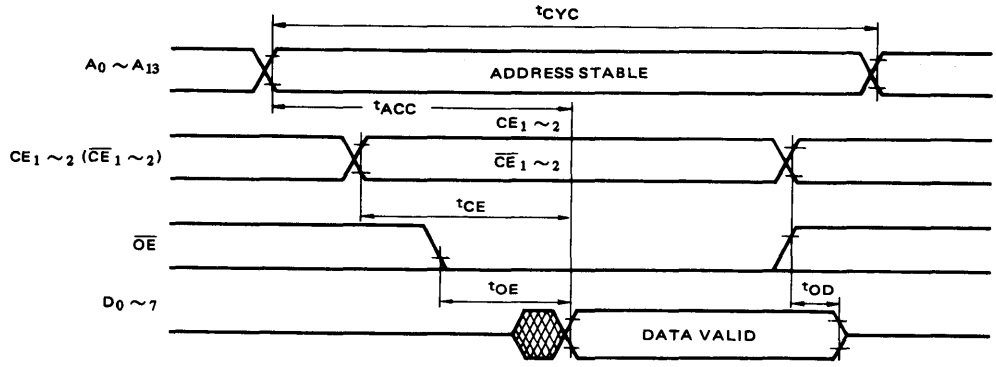
A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

SYMBOL	ITEM	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	200	ns
t_{CE}	Output Delay Time from $CE_{1\sim2}/\overline{CE}_{1\sim2}$	–	200	ns
t_{OE}	Output Delay Time from $\overline{OE}$	–	70	ns
t_{OD}	Output Turn Off Delay	–	60	ns
t_{CYC}	Cycle Time	200	–	ns

AC Test Conditions

- Output Load : 1 TTL + 100pF
- Input Rise and Fall Times (10% to 90%) : 5 ns
- Input Pulse Levels : 0.6V to 2.4V
- Timing Measurement Reference Levels : Input : 0.8V and 2.2V
  Output : 0.8V and 2.0V

TIMING WAVEFORMS



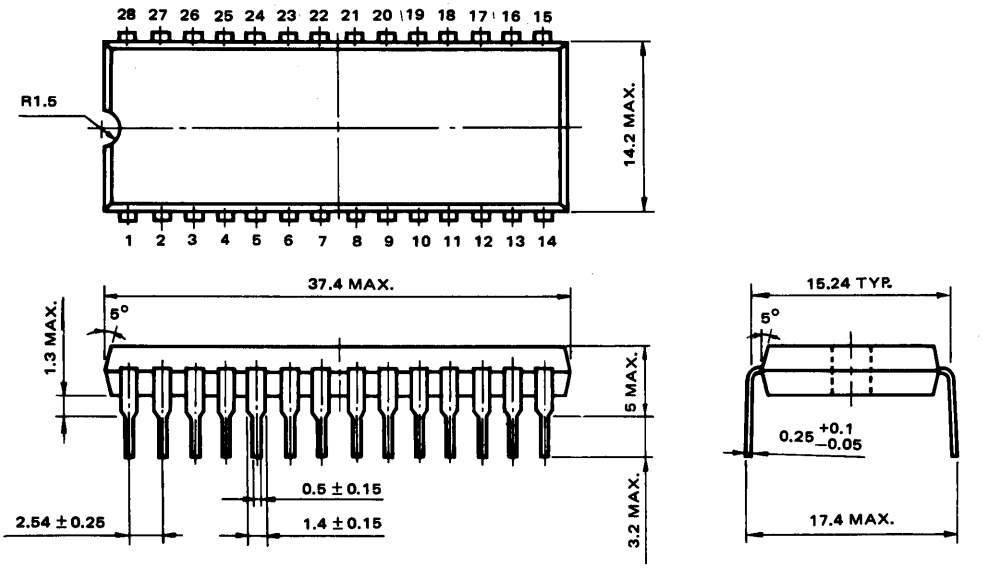
Note:
1) t_{CE} specifies the time interval of $CE_1 \sim 2$ ($\overline{CE}_1 \sim 2$) to become active until it is actually being output.
2) t_{OD} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

APPLICATION INFORMATION

TMM23128P has self substrate-bias generator internally. So a minimum 100μs time delay is required after the application of V_{CC} (4.5V to 5.5V) before proper device operation is achieved.

OUTLINE DRAWINGS

Unit in mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

256K BIT (32K WORD × 8 BIT) MASK ROM
N-CHANNEL SILICON GATE

TMM23256P

DESCRIPTION

The TMM23256P is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, thus being most suitable for use in character generator.

Consisting of static memory cells and clocked peripheral circuitry, the TMM23256P provides a high speed and low power dissipation (access time 150ns, operating current 40mA).

The TMM23256P also features an automatic standby power mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced from 40mA to 10mA. Output Enable ($\overline{OE}$) is effective in preventing data confliction on a common bys line.

The TMM23256P uses the address latch system that the falling edge of $\overline{CE}$ latches all inputs except for $\overline{OE}$, thus can be easily connected to a system where address and data buses are commonly used.

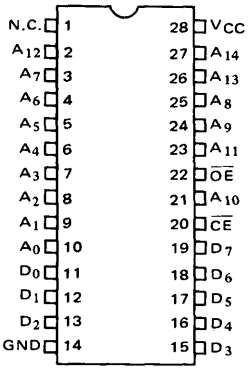
The TMM23256P is fabricated with ion implanted N-channel silicon gate technology. This technology allows a production on high performance.

The TMM23256P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V Power Supply
- Fast Access Time : 150ns (Max.)
- Low Power Dissipation
  - Average Current : 40mA (Max.)
  - Standby Current : 10mA (Max.)
- Inputs protected : All Inputs have Protection Against Static Charge
- Edge Enabled Operation : $\overline{CE}$
- Output Buffer Control : $\overline{OE}$
- Input and Output : TTL Compatible
- Three State Outputs : Wired OR Capability
- 28 pin Standard Plastic DIP

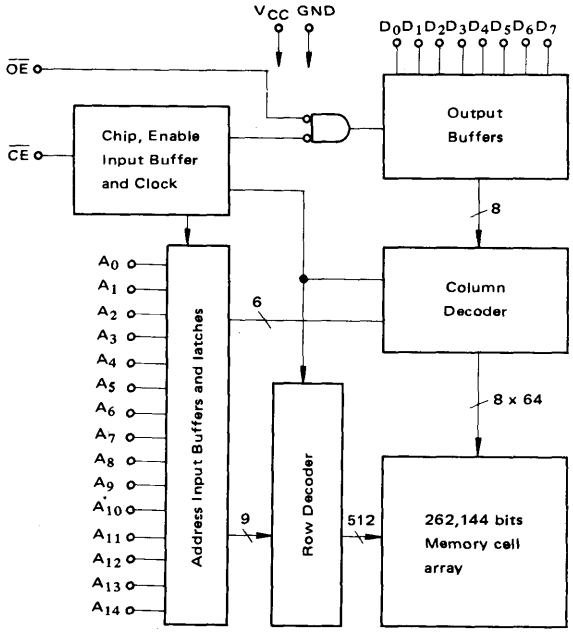
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
N.C.	No Connection
V_{CC}	Power Supply Terminal
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}, V_{OUT}	Input and Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STRG}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	1.0	W

D.C. OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	–	2.2	–	V_{CC} + 1	V
V_{IL}	Input Low Voltage	–	−0.5	–	0.8	V
V_{CC}	Power Supply Voltage	–	4.5	5.0	5.5	V

D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{IH}	Input High Current	V_{IN} = 5.5V		–	0.05	10	μA
I_{IL}	Input Low Current	V_{IN} = GND		–	−0.05	−10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA		2.4	3.3	–	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA		–	0.3	0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 5.5V	$\overline{CE}$ = 2.2V or	–	0.05	10	μA
I_{LOL}		V_{OUT} = 0.4V	$\overline{OE}$ = 2.2V	–	−0.1	−20	μA
I_{CC1}	Standby Current	$\overline{CE}$ = 2.2V		–	–	10	mA
I_{CC2}	Average Current	t_{CYC} = 230ns, I_{OUT} = 0mA		–	–	40	mA

• Typical values are at Ta = 25°C and V_{CC} = 5V.

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = A.C. GND	–	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = A.C. GND	–	8	15	pF

Note : This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

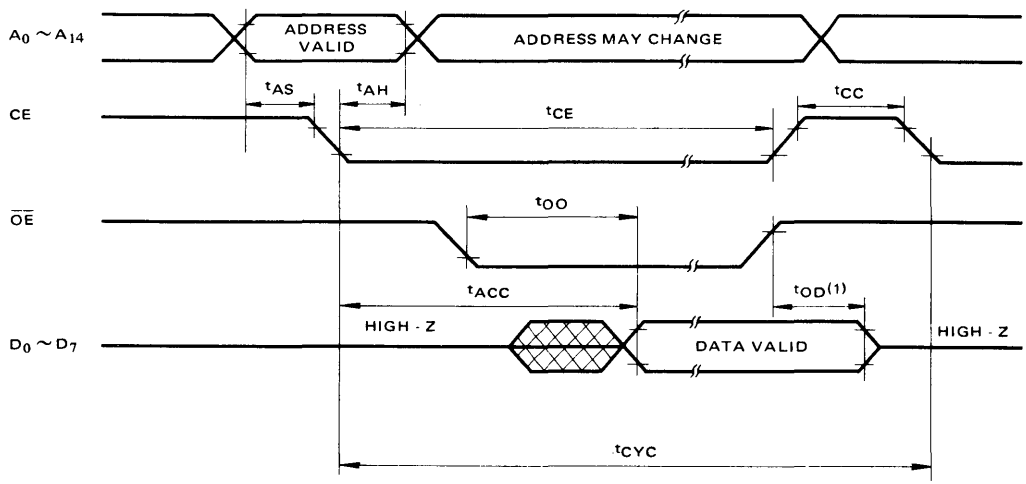
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{CE}	$\overline{CE}$ pulse width	–	150	–	–	ns
t_{AS}	Address Setup Time	–	0	–	–	ns
t_{AH}	Address Hold Time	–	30	–	–	ns
t_{ACC}	Access Time	–	–	–	150	ns
t_{OO}	Output Delay Time form $\overline{OE}$	–	–	–	70	ns
t_{OD}	Output Turn off Delay	–	–	–	70	ns
t_{CC}	$\overline{CE}$ off Time	–	70	–	–	ns
t_{CYC}	Cycle Time	t_{AS} = 0ns, t_r, t_f = 5ns	230	–	–	ns

- Typical values are at $Ta = 25°C$ and $V_{CC} = 5V$.

A.C. TEST CONDITIONS

- Output Load : 1TTL Gate + 100pF
- Input Rise and Fall Times (10% ~ 90%) : 5ns
- Input Pulse Levels : 0.8 ~ 2.4V
- Timing Measurement Reference Levels : Input ; 1V and 2.2V
  Output ; 0.8V and 2.0V

TIMING WAVEFORMS



Note (1) t_{OD} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

OPERATION INFORMATION

The TMM23256P has two control functions.

The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The falling edge of the $\overline{CE}$ will activate the device and latch the addresses. The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming that $\overline{OE}$ = V_{IL}, the output data is valid at the outputs after t_{ACC} (150ns) from the falling edge of the $\overline{CE}$.

The operation modes of the TMM23256P are listed in the following table.

MODE	$\overline{CE}$	ADDRESS	$\overline{OE}$	OUTPUT	POWER
Standby	H	*	*	High Impedance	Standby
Latch	⊓	Valid	*	High Impedance	–
Read	L	**	L	Data Out	Active
Output Deselect	L	*	H	High Impedance	Active

Note * : Don't care

** : Address may change after t_{AH}.

APPLICATION INFORMATION

1. POWER SUPPLY DECOUPLING

The operating current I_{CC} waveforms for TMM 23256P are shown in Fig. 1, 2.

The TMM23256P is a clocked device, so the transient current peaks are produced on the $\overline{CE}$ transition and $\overline{CE}$ active level.

The I_{CC} current transients require adequate decoupling of V_{CC} power supply.

2. POWER ON

The TMM23256P requires initialization prior to normal operation. Two initialization methods are as follows:

(1) A minimum 100μs time delay is required after the application of V_{CC} (+5V) before proper device operation is achieved. And during this period, $\overline{CE}$ must be at V_{IH} level.

(2) A minimum 100μs time delay is required after the application of V_{CC} (5V), and then a minimum of one initialization cycle must be performed before proper device operation is acheived.

Initialization cycle : An initialization cycle is one Chip Enable clock cycle from the first down edge of the $\overline{CE}$ till the next down edge.

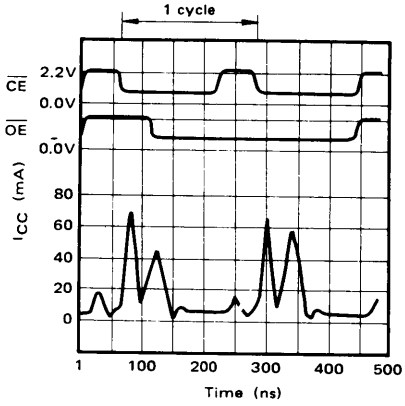


Fig. 1 I_{CC} vs. Time (1)

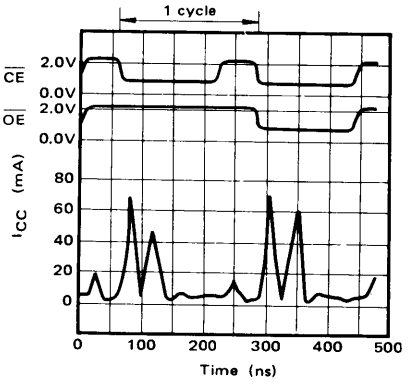
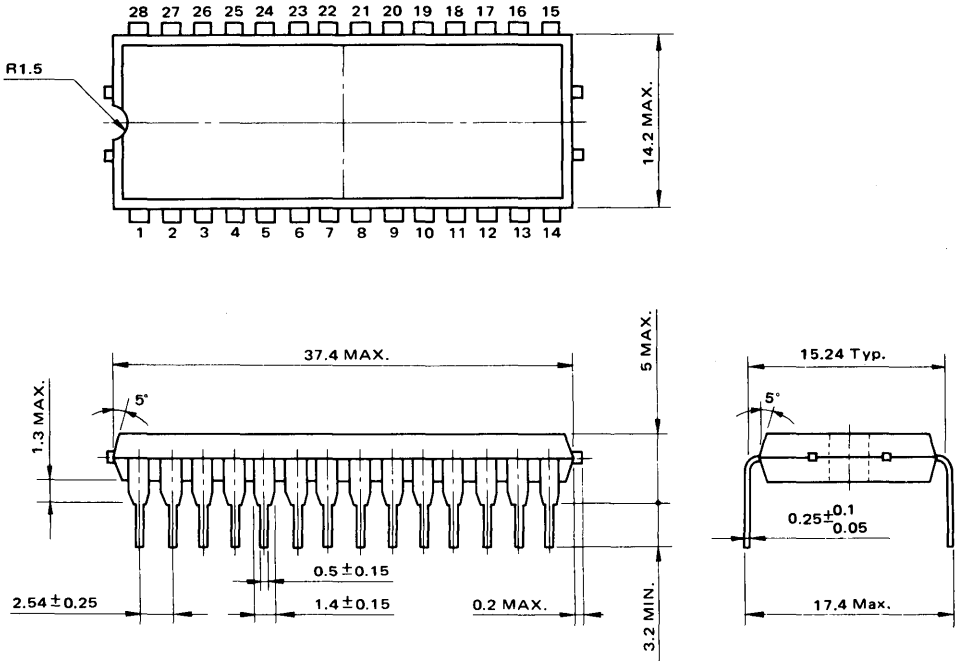


Fig. 2 I_{CC} vs. Time (2)

OUTLINE DRAWINGS

Unit : mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

CMOS Mask Read Only Memories

64K BIT (8K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC5364P

DESCRIPTION

The TC5364P is a 65,536 bit read only memory organized as 8,192 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor and character generator. The TC5364P using CMOS technology is most suitable for low power applications such as battery operated system.

The TC5364P is asynchronous type ROM which is consisting of address latch circuit, static memory cells and clocked peripheral circuitry. The falling edge of $\overline{CE_3}$ (or rising edge of CE_3) latches all inputs except for $\overline{OE}$ and PD/$\overline{PD}$.

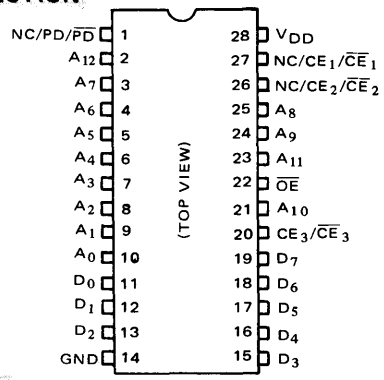
The TC5364P has a PD/$\overline{PD}$ (optional) input for device power saving, and also has three programmable chip enable inputs ($CE_1 \sim 3/\overline{CE_1} \sim 3$) and one output enable input ($\overline{OE}$) for fast memory access and output control.

The TC5364P is moulded in a 28 pin standard plastic package.

FEATURES

- Single Power Supply: 5V
- Access Time: 250 ns
- Low Power Dissipation
  Operating Current: 7mA (Max.)
  Standby Current: 20μA (Max.)
- Wide Operating Temperature Range: −40 ~ 85°C
- Pin Compatible with 64K EPROM TMM2764 and NMOS ROM TMM2364/2365
- Edge Enable Operation: $CE_3/\overline{CE_3}$
- Address Latch Type
- Programmable Power Saving Input PD/$\overline{PD}$/NC
- Programmable Chip Select: CE_1, CE_2, CE_3, Easy Memory Expansion
- All Inputs and Outputs: TTL Compatible
- Three State Outputs

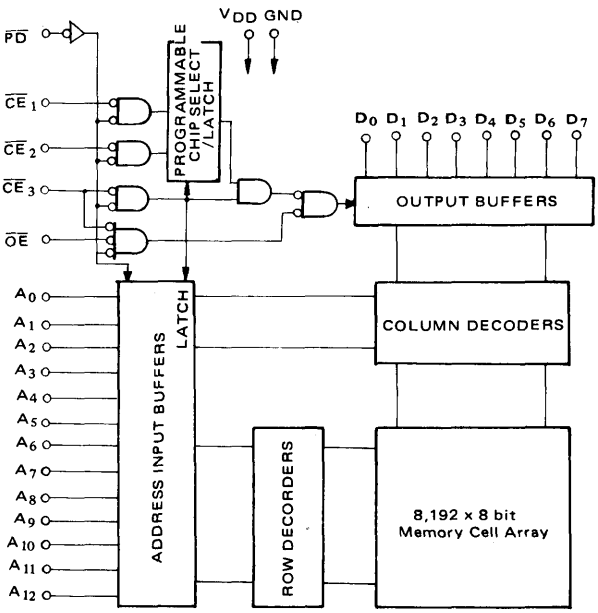
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
$CE_1 \sim CE_3$	Chip enable inputs
P_D	Power down input
$\overline{OE}$	Output enable input
NC	No connection
V_{DD}	Power Supply
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ 7.0	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{opr}	Operating Temperature	−40 ~ 85	°C
T_{stg}	Storage Temperature	−55 ~ 150	°C
T_{SOLDR}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
I_{IN}	Input Leakage Current	$OV \leqq V_{IN} \leqq V_{DD}$	−	±1.0	μA
I_{LO}	Output Leakage Current	$OV \leqq V_{OUT} \leqq V_{DD}$	−	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	−	mA
I_{DDO1}	Operating Current	($\overline{CE}$, V_{IH}) = 2.2V ($\overline{CE}$, V_{IL}) = 0.8V t_{CYC} = 1μs	−	10	mA
I_{DDO2}		($\overline{CE}$, V_{IH}) = V_{DD} −0.2V ($\overline{CE}$, V_{IL}) = 0.2V t_{CYC} = 1μs	−	7	mA
I_{DDS1}	Standby Current	($\overline{CE}$, V_{IH}) = 2.2V $\overline{CE}$ = 0.8V (CE, V_{IL}) = 0.8V $\overline{CE}$ = 2.2V Output = OPEN	−	5	mA
I_{DDS2}		(CE) = 0.2V, ($\overline{CE}$) = V_{DD} −0.2V V_{IN} = 0.2V or V_{DD} −0.2V Output = OPEN	−	20	μA

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	10	pF

*This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

($Ta = -40 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

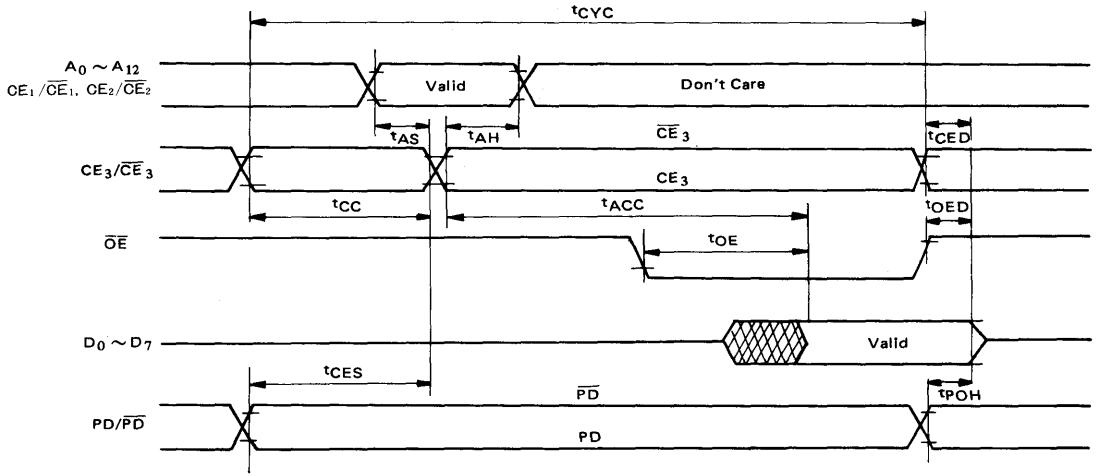
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Chip Enable Access Time	–	250	ns
t_{OE}	Output Enable Access Time	–	100	ns
t_{AS}	Address Set up Time	0	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{CC}	Chip Enable Off Time	90	–	ns
t_{CES}	Chip Enable Setup Time from PD /$\overline{PD}$	90	–	ns
t_{OED}	Output Disable Time from $\overline{OE}$	–	90	ns
t_{CED}	Output Disable Time from $CE_3/\overline{CE_3}$	–	90	ns
t_{POH}	Output Hold Time from PD/$\overline{PD}$	–	90	ns
t_{CYC}	Cycle Time	350	–	ns

Note 1: Assumes than $\overline{OE}$ delay time to $CE_3/\overline{CE_3} \geqq t_{ACC} - t_{OE}$

A.C. TEST CONDITIONS

- Output Load: 100pF + 1 TTL Gate
- Input Levels: V_{IL} = 0.6V, V_{IH} = 2.4V
- Timing Measurement Rference Levels
  - Input: 0.8V, 2.2V
  - Output: 0.8V, 2.2V
- Input Rise and Fall Time: 5 ns

TIMING WAVE FORMS



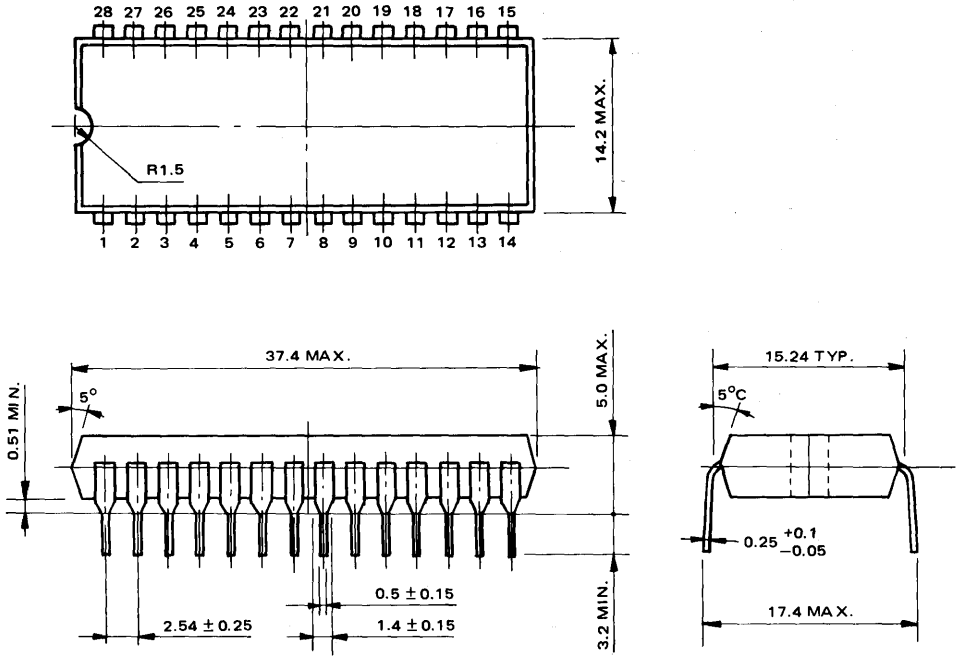
OPERATION MODE

MODE	PD ($\overline{PD}$)	CE_1 ($\overline{CE_1}$)	CE_2 ($\overline{CE_2}$)	CE_3 ($\overline{CE_3}$)	$\overline{OE}$	Outputs
Read	L(H)	H(L)	H(L)	H↑(L↓)	L	Valid
Output Deselect	H(L)	*	*	*	*	High-Z
	*	L(H)	*	*	*	
	*	*	L(H)	*	*	
	*	*	*	L(H)	*	
	*	*	*	*	H	

Note: H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWING

Unit: mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

64K BIT (8K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE MOS

TC5365P
TC5365F

DESCRIPTION

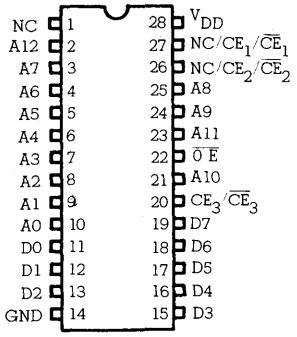
The TC5365P/F is a 65,536 bit read only memory organized as 8,192 words by 8 bit with a low bit cost, thus being suitable for use in program memory of microprocessor, and in character generator. The TC5365P/F using CMOS technology is most suitable for low power applications where battery operation is required.

The TC5365P/F has three programmable chip enable input $CE_1 \sim CE_3/\overline{CE_1} \sim \overline{CE_3}$, for device selection and one output enable input ($\overline{OE}$) for fast memory access and output control.

FEATURES

- single 5V Power Supply
- Access Time : 250ns(Max.)
- Power Dissipation
  Operating Current : 7mA(Max.)
  Standby Current : 20μA(Max.)
- Pin Compatible with 64K EPROM TMM 2764D
- Full Static Operation
- Programmable Chip Enable
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Package
  Plastic DIP: TC5365P
  Plastic FP : TC5365F

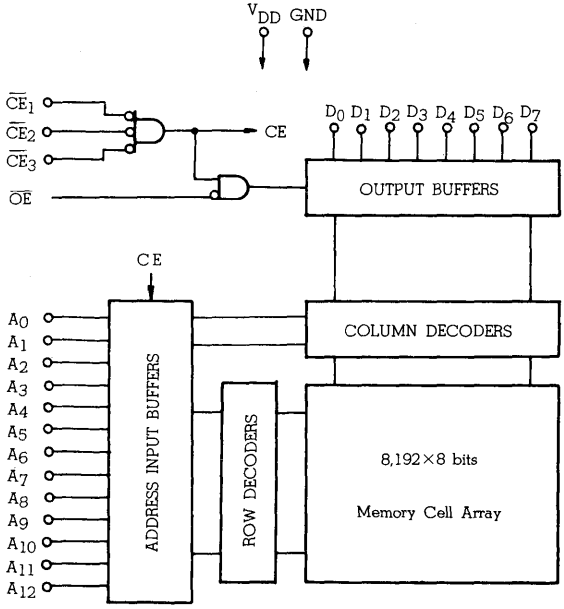
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$D_0 \sim D_7$	Data Outputs
NC	No connection
$CE_1 \sim CE_3/\overline{CE_1} \sim \overline{CE_3}$	Chip enable inputs
$\overline{OE}$	Output enable input
V_{DD}	Power supply
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~7.0	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{OPR}	Operating Temperature	−40~85	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec

NOTE : * Plastic FP

D. C. OPERATING CONDITIONS

(Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D. C. and OPERATING CHARACTERISTICS

(Ta = −40~85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IN}	Input Leakage Current	$0V \leqq V_{IN} \leqq V_{DD}$	—	±1.0	μA
I_{LO}	Output Leakage Current	$0V \leqq V_{OUT} \leqq V_{DD}$	—	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	—	mA
I_{DDO1}	Operating Current	($\overline{CE}$, V_{IH}) = 2.2V (CE, V_{IL}) = 0.8V t_{CYC} = 1μs	—	10	mA
I_{DDO2}		($\overline{CE}$, V_{IH}) = V_{DD} − 0.2V (CE, V_{IL}) = 0.2V t_{CYC} = 1μs	—	7	mA
I_{DDS1}	Standby Current	($\overline{CE}$, V_{IH}) = 2.2V (CE, V_{IL}) = 0.8V Output = OPEN	—	2	mA
I_{DDS2}		(CE) = 0.2V, ($\overline{CE}$) = V_{DD} − 0.2V V_{IN} = 0V~V_{DD} Output = OPEN	—	20	μA

A. C. CHARACTERISTICS

(Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	—	250	ns
t_{CE}	Chip Enable Access Time	—	250	ns
t_{OE}	Output Enable Access Time	—	100	ns
t_{CED}	Output Disable Time from $CE_{1\sim3}/\overline{CE_{1\sim3}}$	0	90	ns
t_{OED}	Output Disable Time from $\overline{OE}$	0	90	ns
t_{OH}	Output Hold Time	0	—	ns
t_{CYC}	Cycle Time	250	—	ns

Note 1 : Assumes that $\overline{OE}$ delay to $CE_{1\sim3}/\overline{CE_{1\sim3}} \geqq t_{ACC}$-$t_{OE}$

Note 2 : Output disable time (t_{CED}, t_{OED}) is specified from $CE_{1\sim3}$/, $\overline{CE_{1\sim3}}$, $\overline{OE}$ whichever occurs first.

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL

Input Levels : V_{IL} = 0.6V, V_{IH} = 2.4V

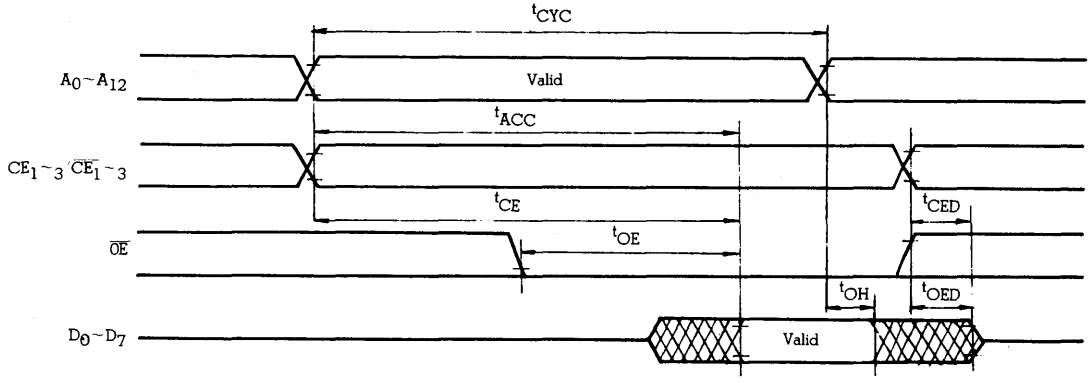
Timing Measurement Reference Levels

Input : 0.8V, 2.2V

Output : 0.8V, 2.2V

Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



CAPACITANCE

(Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

OPERATION MODE

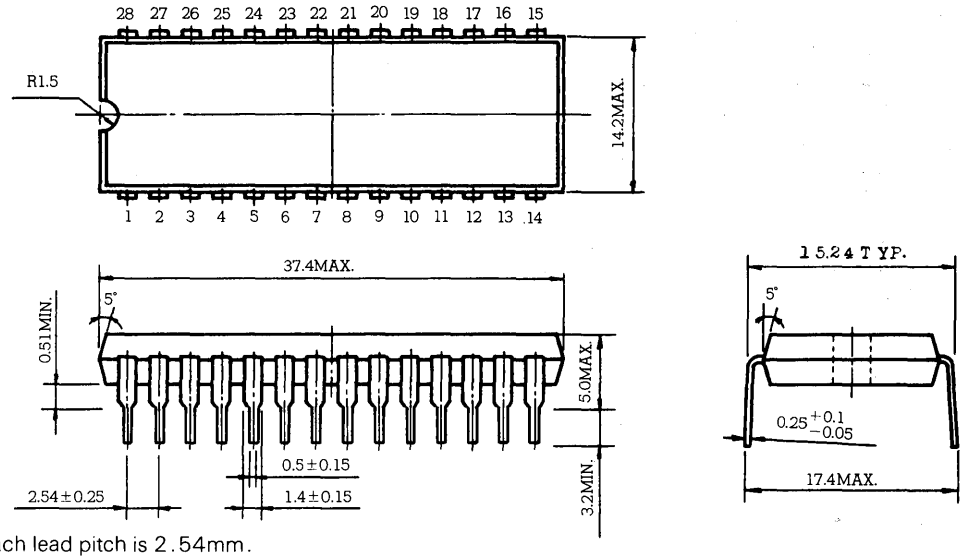
H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

MODE	$CE_1(\overline{CE_1})$	$\overline{CE_2}(CE_2)$	$CE_3(\overline{CE_3})$	$\overline{OE}$	Outputs
Read	H(L)	H(L)	H(L)	L	Valid
Outputs Deselect	L(H)	*	*	*	High-Z
	*	L(H)	*	*	
	*	*	L(H)	*	
	*	*	*	H	

OUTLINE DRAWINGS

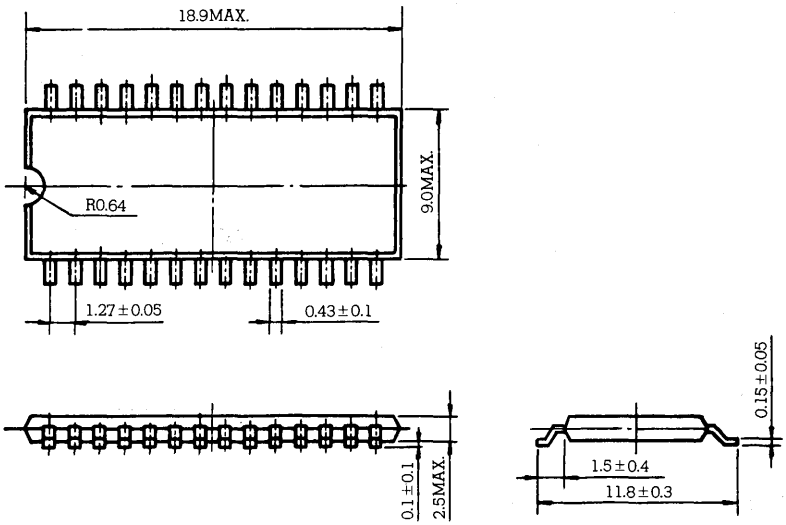
- Plastic DIP

Unit: mm



NOTE : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

- Plastic FP



NOTE : Each lead pitch is 1.27mm.
All leads are located within 0.12mm of their true longitudinal position with respect to No.1 and No.28 leads.

64K BIT (8K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC5366P

DESCRIPTION

The TC5366P is a 65,536 bit read only memory organized as 8,192 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor and character generator.

The TC5366P using CMOS technology is most suitable for low power applications such as battery operated system.

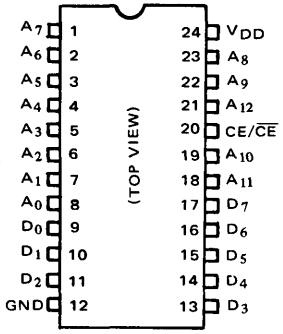
The TC5366P is an asynchronous type ROM and has a programmable chip enable input for device selection and device power saving.

The TC5366P is moulded in a 24 pin standard plastic package.

FEATURES

- Single Power Supply: 5V
- Access Time: 250 ns
- Low Power Dissipation
  Operating Current: 7mA (Max.)
  Standby Current: 20μ A (Max.)
- Fully Static Operation
- Programmable Chip Enable: CE/$\overline{CE}$
- All Inputs and Outputs: TTL Compatible
- Three State Outputs

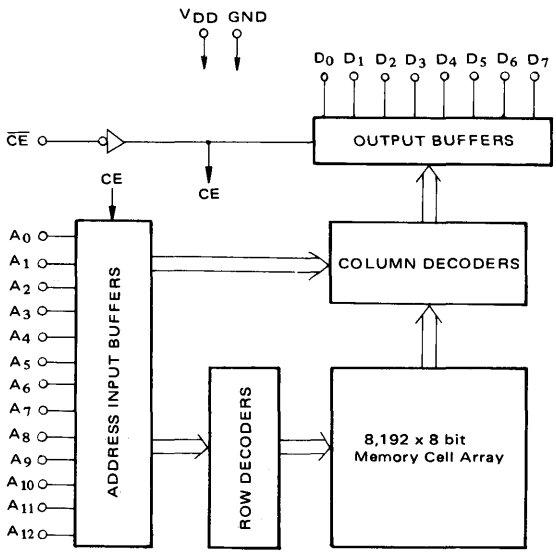
PIN CONNECTION



PIN NAMES

$A_0 \sim A_{12}$	Address inputs
$D_0 \sim D_7$	Data outputs
CE/$\overline{CE}$	Chip enable input
V_{DD}	Power supply
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ 7.0	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{opr}	Operating Temperature	−40 ~ 85	°C
T_{stg}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.5	V
V_{IH}	Input High Voltage	2.2	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IN}	Input Leakage Current	$OV \leqq V_{IN} \leqq V_{DD}$	–	±1.0	μA
I_{LO}	Output Leakage Current	$OV \leqq V_{OUT} \leqq V_{DD}$	–	±0.5	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	–	mA
I_{DDO1}	Operating Current	$(\overline{CE}, V_{IH})$ = 2.2V $(\overline{CE}, V_{IL})$ = 0.8V t_{CYC} = 1μs	–	10	mA
I_{DDO2}		$(\overline{CE}, V_{IH})$ = V_{DD} −0.2V $(\overline{CE}, V_{IL})$ = 0.2V t_{CYC} = 1μs	–	7	mA
I_{DDS1}	Standby Current	$(\overline{CE}, V_{IH})$ = 2.2V (CE, V_{IL}) = 0.8V Output = OPEN	–	2	mA
I_{DDS2}		(CE) = 0.2V, $(\overline{CE})$ = V_{DD} −0.2V V_{IN} = OV ~ V_{DD} Output = OPEN	–	20	μA

CAPACITANCE* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = OV	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = OV	10	pF

*This parameter is periodically sampled and is not 100% tested.

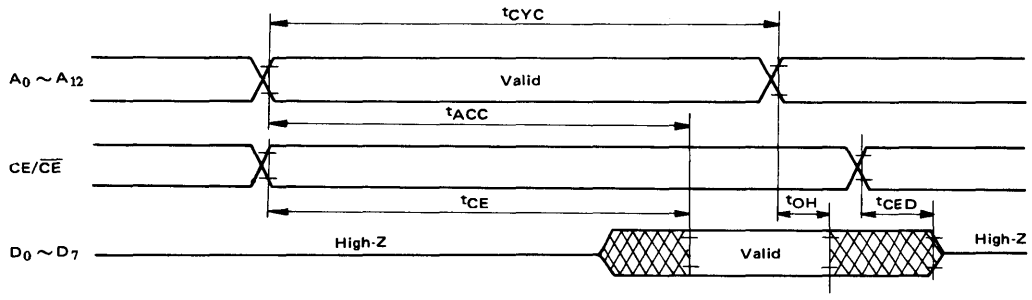
A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ±10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Access Time	–	250	ns
t_{CE}	Chip Enable Access Time	–	250	ns
t_{CED}	Output Disable Time from CE /$\overline{CE}$	0	90	ns
t_{OH}	Output Hold Time	0	–	ns
t_{CYC}	Cycle Time	250	–	ns

A.C. TEST CONDITIONS

- Output Load: 100pF + 1 TTL
- Input Levels: V_{IL} = 0.6V, V_{IH} = 2.4V
- Timing Measurement Reference Levels
  - Input: 0.8V, 2.2V
  - Output: 0.8V, 2.2V
- Input Rise and Fall Time: 5ns

TIMING WAVE FORMS

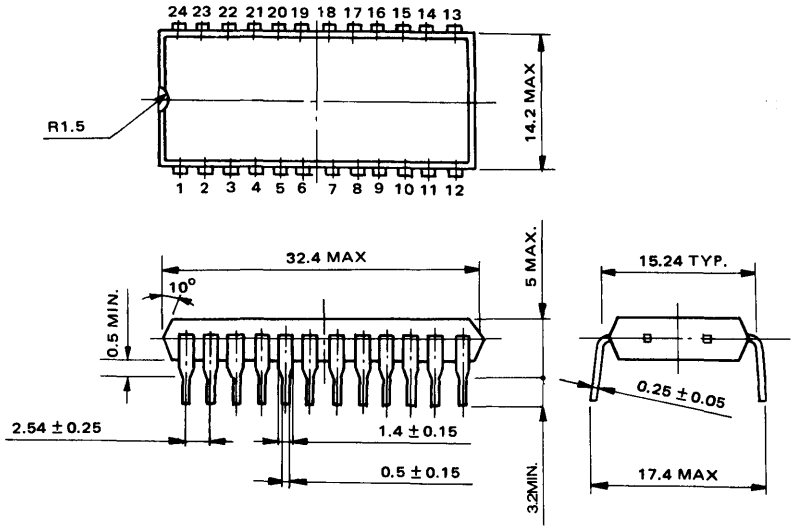


OPERATION MODE

MODE	CE ($\overline{CE}$)	Output
Read	H(L)	Valid
Output Deselect	L(H)	High-Z

Note: H: V_{IH}, L: V_{IL}

OUTLINE DRAWINGS



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.24 leads.

256K BIT (32K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE MOS

TC53257P
TC53257F

DESCRIPTION

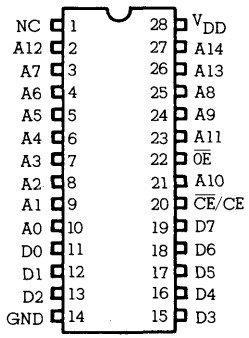
The TC53257P/F is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, this being suitable for use in program memory of microprocessor, and in character generator. The TC53257P/F using CMOS technology is most suitable for low power applications where battery operation is required.

The TC53257P/F has one programmable chip enable input $\overline{CE}$/CE, for device selection and one output enable input ($\overline{OE}$) for fast memory access and output control.

FEATURES

- Single 5V Power Supply
- Access Time : 200ns(Max.)
- Power Dissipation
  Operating Current : 25mA(Max.)
  Standby Current : 20μA(Max.)
- Pin Compatible with 256K EPROM TC57256D
- Full Static Operation
- Programmable Chip Enable
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Package
  Plastic DIP : TC53257P
  Plastic FP : TC53257F

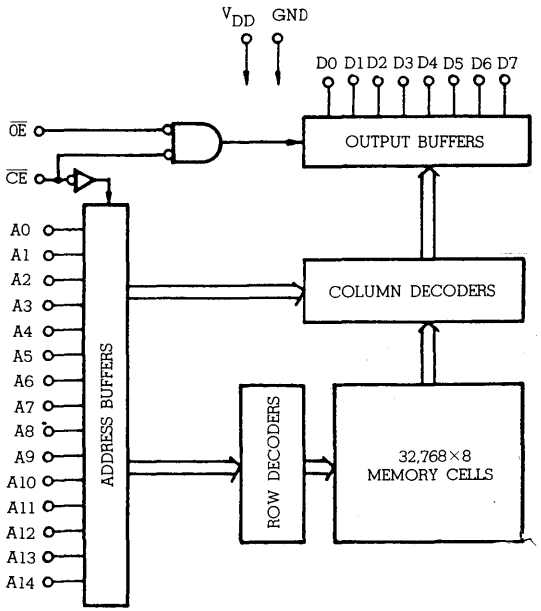
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{14}	Address Inputs
D_0~D_7	Data Outputs
NC	No connection
$\overline{CE}$/CE	Chip enable input
$\overline{OE}$	Output enable input
V_{DD}	Power supply
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~7.0	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	−40~85	°C
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec

Note : *Plastic FP

D. C. OPERATING CONDITINS (Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V

D. C. and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V~V_{DD}	—	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} V_{OUT} = 0V~V_{DD}	—	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	—	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} CE = V_{IL}	—	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD}−0.2V, CE = 0.2V	—	20	μA
I_{DDO1}	Operating Current	V_{IH} = $V_{IH\ VIL}$, t_{CYCLE} = 200ns	—	40	mA
I_{DDO2}		V_{IN} = V_{DD}−0.2V/0.2V, t_{CYCLE} = 200ns	—	25	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	—	8	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	—	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

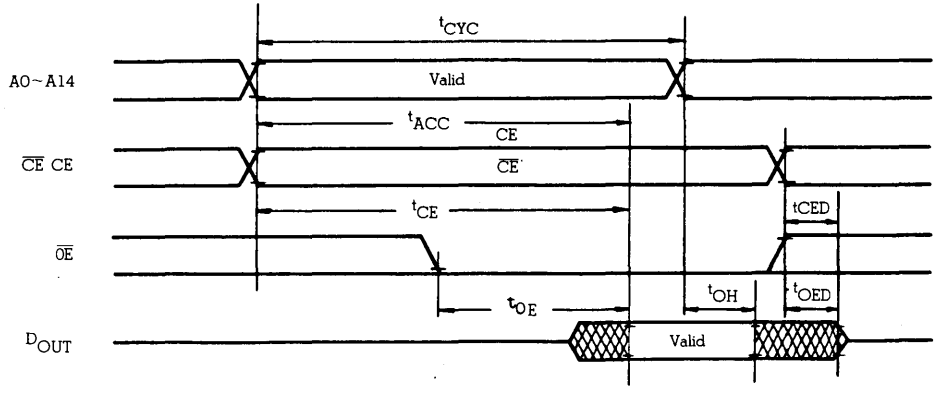
($Ta = -40 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	200	—	ns
t_{ACC}	Access Time	—	200	ns
t_{CE}	Chip Enable Access Time from CE/$\overline{CE}$	—	200	ns
t_{OE}	Output Enable Access Time from $\overline{OE}$	—	70	ns
t_{CED}, t_{OED}	Output Disable Time from CE/$\overline{CE}$, $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	0	—	ns

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL
Input Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V, 2.2V
Output : 0.8V, 2.2V
Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

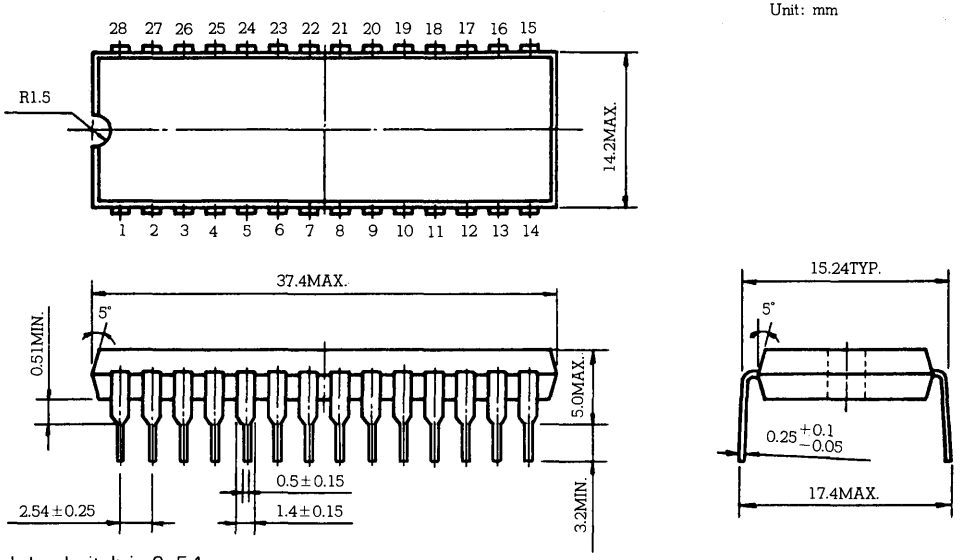
H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

MODE	$\overline{CE}$(CE)	$\overline{OE}$	$A_{0 \sim 14}$	Outputs	Power
Read	L(H)	L	Valid	Data out	Operating
Output Deselect	L(H)	H	*	High-Z	Operating
	H(L)	*	*		Standby

OUTLINE DRAWINGS

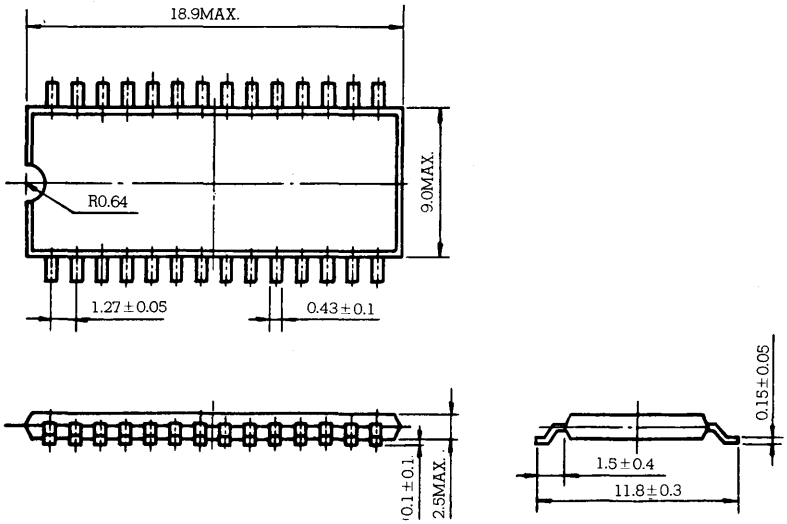
- Plastic DIP

Unit: mm



NOTE : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

- Plastic FP



NOTE : Each lead pitch is 1.27mm.
All leads are located within 0.12mm of their true longitudinal position with respect to No.1 and No.28 leads.

1M BIT (128K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC531000P

DESCRIPTION

The TC531000P is a 1,048,576 bit read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000P using CMOS technology is most suitable for low power applications where battery operation are required.

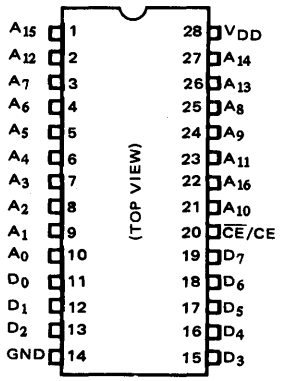
The TC531000P has one chip enable input $\overline{CE}$/CE, programmable for device selection.

The TC531000P is moulded in a 28 pin standard plastic package, 0.6 inch in width.

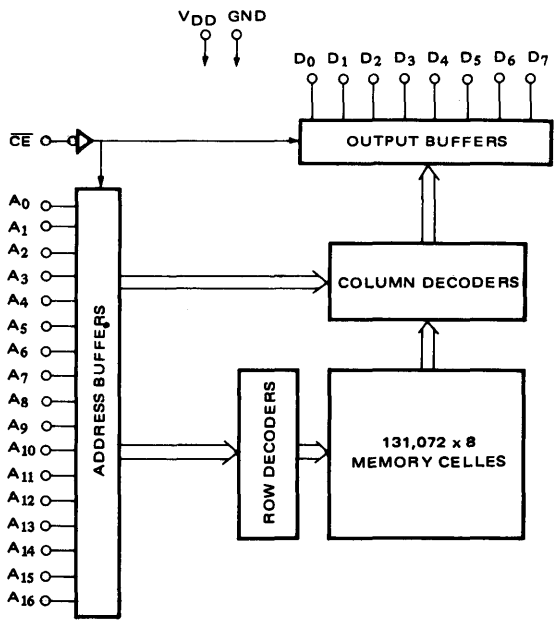
FEATURES

- Single 5V Power Supply
- Access Time: 200 ns (Max.)
- Power Dissipation
  Operating Current: 30mA (Max.)
  Standby Current: 20μA (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- 28 pin 600 mil width DIP Plastic package
- Fully Static Operation
- Programmable Chip Enable

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{16}$	Address inputs
$D_0 \sim D_7$	Data outputs
$\overline{CE}$/CE	Chip enable input
V_{DD}	Power supply
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ V_{DD}	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−40 ~ 85	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = OV ~ V_{DD}	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	–	mA
I_{DDS1}	Standby Current	($\overline{CE}$, V_{IH}) = 2.2V, (CE, V_{IL}) = 0.8V	–	5	mA
I_{DDS2}	Standby Current	(CE) = 0.2V, ($\overline{CE}$) = V_{DD} − 0.2V, V_{IN} = 0V ~ V_{DD}	–	20	μA
I_{DD01}	Operating Current	V_{IN} = V_{IH}/V_{IL}, t_{cycle} = 200 ns	–	50	mA
I_{DD02}		V_{IN} = V_{DD} − 0.2V/0.2V, t_{cycle} = 200 ns	–	30	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	–	8	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	–	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

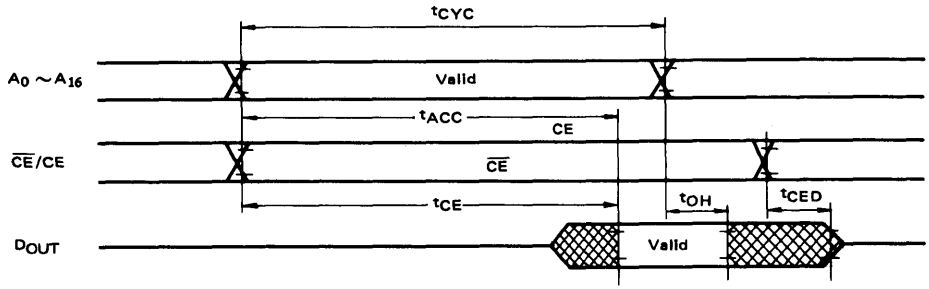
A.C. CHARACTERISTICS ($Ta = -40 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	200	–	ns
t_{ACC}	Access Time	–	200	ns
t_{CE}	Chip Enable Access Time from CE/$\overline{CE}$	–	200	ns
t_{CED}	Output Disable Time from CE/$\overline{CE}$	0	70	ns
t_{OH}	Output Hold Time	0	–	ns

AC TEST CONDITIONS

Output Load : 100pF + 1TTL
Input Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V, 2.2V
Output : 0.8V, 2.0V
Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



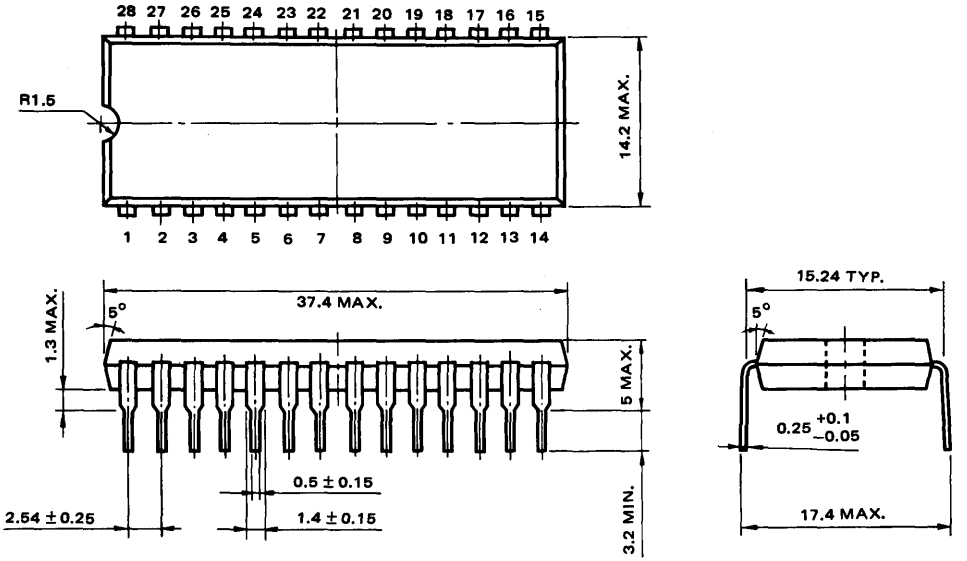
OPERATION MODE

MODE	$\overline{CE}$(CE)	$A_0 \sim 16$	Outputs	Power
Read	L(H)	Valid	Data out	Operating
Output Deselect	H(L)	*	High-Z	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

OUTLINE DRAWINGS

Unit: mm



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

MEMO

MEMO

MEMO

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