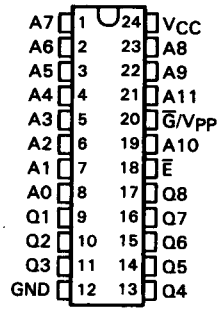
AUGUST 1983—REVISED FEBRUARY 1988

- **Organization . . . 4096 × 8**
- **Single 5-V Power Supply**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Times**
  TMS2732A-17 170 ns
  TMS2732A-20 200 ns
  TMS2732A-25 250 ns
  TMS2732A-45 450 ns
- **Low Standby Power Dissipation . . . 158 mW (Maximum)**
- **JEDEC Approved Pinout . . . Industry Standard**
- **21-V Power Supply Required for Programming**
- **N-Channel Silicon-Gate Technology**
- **PEP4 Version Available with 168 Hour Burn-In, and Extended Guaranteed Operating Temperature Range from −10°C to 85°C (TMS2732A-_ _JP4)**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$/VPP	Output Enable/21 V
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

description

The TMS2732A is an ultraviolet light-erasable, electrically programmable read-only memory. It has 32,768 bits organized as 4,096 words of 8-bit length. The TMS2732A only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS2732A provides two output control lines: Output Enable ($\overline{G}$/VPP) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$/VPP control line to eliminate bus contention in multibus microprocessor systems. The TMS2732A has a power-down mode that reduces maximum power dissipation from 657 mW to 158 mW when the device is placed on standby.

This EPROM is supplied in a 24-pin dual-in-line ceramic package and is designed for operation from 0°C to 70°C. The TMS2732A is also offered in the PEP4 version with an extended guaranteed operating temperature range of −10°C to 85°C and 168 hour burn-in (TMS2732A-_ _JP4).

operation

The six modes of operation for the TMS2732A are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{E}$ (18)	V_{IL}	X†	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}/V_{PP}$ (20)	V_{IL}	V_{IH}	X†	21 V	V_{IL}	21 V
V_{CC} (24)	5 V	5 V	5 V	5 V	5 V	5 V
Q1-Q8 (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	Q	HI-Z

†X = V_{IH} or V_{IL}

read/output disable

The two control pins ($\overline{E}$ and $\overline{G}/V_{PP}$) must have low-level TTL signals in order to provide data at the outputs Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}/V_{PP}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum power dissipation from 657 mW to 158 mW. A TTL high-leve signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state independent of $\overline{G}/V_{PP}$.

erasure

The TMS2732A is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time is fifteen watt-seconds per square centimeter. The lamp should be located about 2.5 centimeters (1 inch above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambien light contains the correct wavelength for erasure. Therefore, when using the TMS2732A, the window shoul be covered with an opaque label.

programming

Note that the application of a voltage in excess of 22 V to $\overline{G}/V_{PP}$ may damage the TMS2732A.

After erasure (all bits in logic 1 state), logic 0s are programmed into the desired locations. A logic 0 can onl be erased by ultraviolet light. In the program mode, $\overline{G}/V_{PP}$ is taken from a TTL low level to 21 V and data to b programmed are applied in parallel to output pins Q1-Q8. The location to be programmed is addressed. Onc data and addresses are stable, a 10-millisecond TTL low-level pulse is applied to $\overline{E}$. The maximum width c this pulse is 11 milliseconds. The programming pulse must be applied at each location that is to be programmec Locations may be programmed in any order.

Several TMS2732As can be programmed simultaneously by connecting them in parallel and following th programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS2732As connected in parallel with different data Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ of the device that is not to be programme

program verify

After the EPROM has been programmed, the programmed bits should be verified. To verify bit states, $\overline{G}/V_P$ and $\overline{E}$ are set to V_{IL}.

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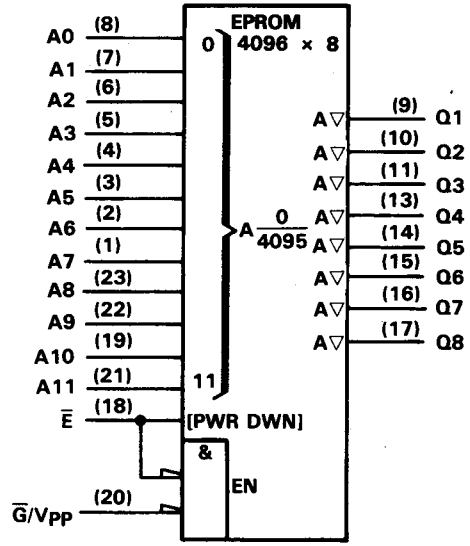
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.3 V to 7 V
Supply voltage range, V_{PP} . . . . . −0.3 V to 22 V
Input voltage range (except program) . . . . . −0.3 to 7 V
Output voltage range . . . . . −0.3 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.75	5	5.25	V
V_{PP}	Supply voltage (see Note 2)		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
2. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 21 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA		0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V		±10	μA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}, $\overline{G}/V_{PP}$ at V_{IL}		30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}/V_{PP}$ at V_{IL}		125	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER			TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	All except $\overline{G}/V_{PP}$	V_I = 0 V	6	9	pF
		$\overline{G}/V_{PP}$			20	
C_o	Output capacitance		V_O = 0 V	8	12	pF

†These parameters are tested on sample basis only.
‡Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS2732A-17		TMS2732A-20		TMS2732A-25		TMS2732A-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \le 20$ ns, $t_f \le 20$ ns, See Figure 1 and Note 3		170		200		250		450	ns
$t_{a(E)}$	Access time from $\overline{E}$			170		200		250		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}/V_{PP}$			65		70		100		150	ns
t_{dis}†	Output disable time from $\overline{E}$ or G, whichever occurs first		0	60	0	60	0	85	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}/V_{PP}$, whichever occurs first		0		0		0		0		ns

NOTE 3: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output reference levels are 0.8 V and 2.0 V.
†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled, not 100% tested.

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recommended conditions for programming, T_A = 25°C (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	20.5	21	21.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
$t_{w(E)}$	$\overline{E}$ pulse duration	9	10	11	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	$\overline{G}$/V_{PP} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(VPP)}$	$\overline{G}$/V_{PP} hold time	2			μs
$t_{rec(PG)}$	$\overline{G}$/V_{PP} recovery time	2			μs
$t_{r(PG)G}$	$\overline{G}$/V_{PP} rise time during programming	50			ns
t_{EHD}	Delay time, data valid after $\overline{E}$ low			1	μs

NOTE 4: When programming the TMS2732A, connect a 0.1 μF capacitor between $\overline{G}$/V_{PP} and GND to suppress spurious voltage transients which may damage the device.

programming characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{OH}	High-level output voltage (verify)	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage (verify)	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
I_{PP}	Supply current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$			50	mA
I_{CC}	Supply current				125	mA
$t_{dis(PR)}$	Output disable time		0		130	ns

PARAMETER MEASUREMENT INFORMATION

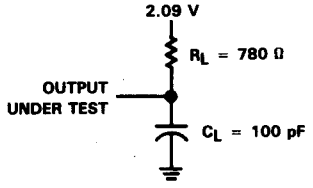
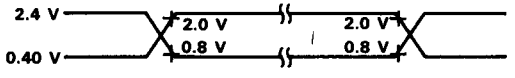


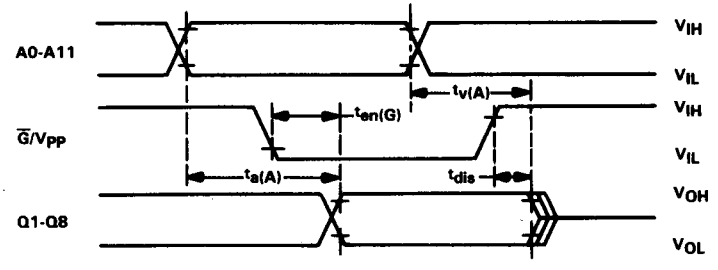
FIGURE 1. TYPICAL OUTPUT LOAD CIRCUIT

AC testing input/output wave forms

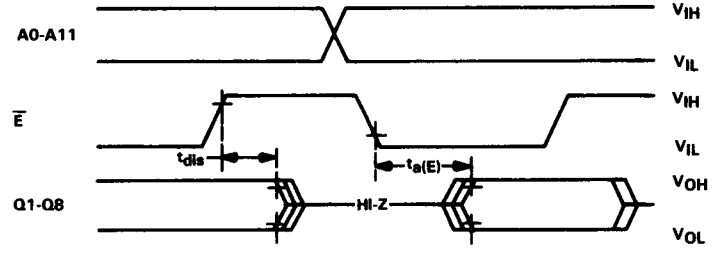


A.C. testing inputs are driven at 2.4 V for logic 1 and 0.4 V for logic 0. Timing measurements are made at 2.0 V for logic 1 and 0.8 V for logic 0 for both inputs and outputs.

read cycle timing



standby mode



NOTE 3: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2.0 V.

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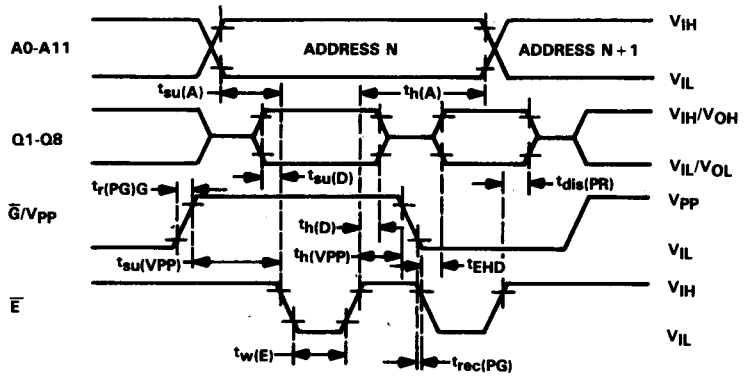
program cycle timing



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