ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

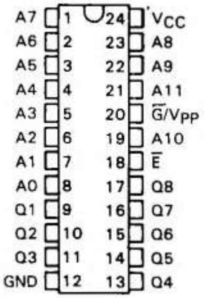
Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *''Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies.''*

TMS2732A
32,768-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

AUGUST 1983 – REVISED NOVEMBER 1985

- **Organization . . . 4096 X 8**
- **Single 5-V Power Supply**
- **All Inputs and Outputs Are TTL Compatible**
- **Max Access/Min Cycle Time**
  TMS2732A-17 170 ns
  TMS2732A-20 200 ns
  TMS2732A-25 250 ns
  TMS2732A-45 450 ns
- **Low Standby Power Dissipation . . . 158 mW (Maximum)**
- **JEDEC Approved Pinout . . . Industry Standard**
- **21-V Power Supply Required for Programming**
- **N-Channel Silicon-Gate Technology**
- **PEP4 Version Available with 168 Hour Burn-in and Guaranteed Operating Temperature Range from – 10 °C to 85 °C (TMS2732A-_ _JP4)**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
E̅	Chip Enable
G̅/V_{PP}	Output Enable/21 V
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

description

The TMS2732A is an ultraviolet light-erasable, electrically programmable read-only memory. It has 32,768 bits organized as 4,096 words of 8-bit length. The TMS2732A only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS2732A provides two output control lines: Output Enable (G̅) and Chip Enable (E̅). This feature allows the G̅ control line to eliminate bus contention in multibus microprocessor systems. The TMS2732A has a power-down mode that reduces maximum power dissipation from 657 mW to 158 mW when the device is placed on standby.

This EPROM is supplied in a 24-pin dual-in-line ceramic package and is designed for operation from 0 °C to 70 °C.

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TEXAS INSTRUMENTS

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operation

The six modes of operation for the TMS2732A are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Deselect	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{E}$ (18)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}/V_{PP}$ (20)	V_{IL}	V_{IH}	X	21 V	V_{IL}	21 V
V_{CC} (24)	5 V	5 V	5 V	5 V	5 V	5 V
Q1-Q8 (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IH} or V_{IL}

read

The two control pins ($\overline{E}$ and $\overline{G}/V_{PP}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}/V_{PP}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum power dissipation from 657 mW to 158 mW. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}/V_{PP}$.

program

The programming procedure for the TMS2732A is the same as that for the TMS2532, except that in the program mode, $\overline{G}/V_{PP}$ is taken from a TTL low level to 21 V.

The program mode consists of the following sequence of events. With the level on $\overline{G}/V_{PP}$ equal to 21 V, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a 10-millisecond TTL low-level pulse is applied to $\overline{E}$. The maximum width of this pulse is 11 milliseconds. The programming pulse must be applied at each location that is to be programmed. Locations may be programmed in any order.

Several TMS2732As can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program verify

After the EPROM has been programmed, the programmed bits should be verified. To verify bit states, $\overline{G}/V_{PP}$ and $\overline{E}$ are set to V_{IL}.

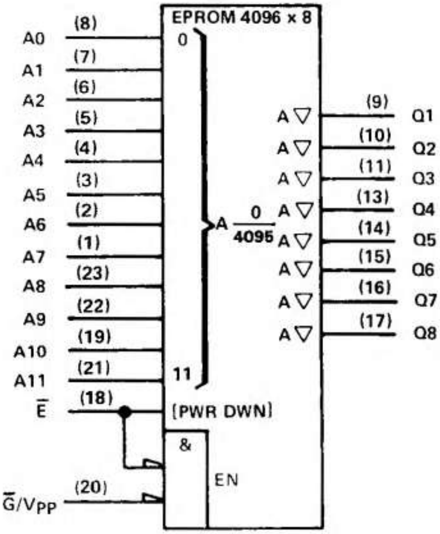
program inhibit

The program inhibit is useful when programming multiple TMS2732As connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ of the device that is not to be programmed.

erasure

The TMS2732A is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2732A, the window should be covered with an opaque label.

logic symbol†



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†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.3 V to 7 V
Supply voltage range, V_{PP}	−0.3 V to 22 V
Input voltage range (except program)	−0.3 V to 7 V
Output voltage range	−0.3 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

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† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.75	5	5.25	V
V_{PP}	Supply voltage (see Note 2)		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

2. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 21 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 2.1$ mA		0.45	V
I_I	Input current (leakage)	$V_I = 0$ V to 5.25 V		±10	μA
I_O	Output current (leakage)	$V_O = 0.4$ V to 5.25 V		±10	μA
I_{CC1}	VCC supply current (standby)	$\overline{E}$ at V_{IH}, $\overline{G}$ at V_{IL}		30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		125	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz[†]

PARAMETER			TEST CONDITIONS	TYP[‡]	MAX	UNIT
C_i	Input capacitance	All except $\overline{G}/V_{PP}$	$V_I = 0$ V	4	6	pF
		$\overline{G}/V_{PP}$			20	
C_o	Output capacitance		$V_O = 0$ V	8	12	pF

[†] These parameters are tested on sample basis only.
[‡] Typical values are at $T_A = 25\,°C$ and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS2732A-17		TMS2732A-20		TMS2732A-25		TMS2732A-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	$C_L = 100$ pF, 1 Series 74 TTL Load, $t_r \le 20$ ns, $t_f \le 20$ ns, See Figure 1 and Note 3		170		[illegible]		250		450	ns
$t_{a(E)}$	Access time from $\overline{E}$			170		200		250		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			65		70		100		150	ns
t_{dis}[†]	Output disable time from $\overline{E}$ or $\overline{G}$, whichever occurs first		0	60	0	60	0	85	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		0		ns

NOTE 3: The timing reference levels for inputs and outputs are 0.8 V and 2 V. Input pulse levels are 0.40 V and 2.4 V.
[†] Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended conditions for programming, $T_A = 25°C$ (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	20.5	21	21.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
$t_{w(E)}$	$\overline{E}$ pulse duration	9	10	11	ms
$t_{su(A)}$	Address [illegible]	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs
$t_{h(VPP)}$	V_{PP} hold time	2			µs
$t_{rec(PG)}$	V_{PP} recovery time	2			µs
$t_{r(PG)G}$	$\overline{G}$ rise time during programming	50			ns
t_{EHD}	Delay time, data valid after $\overline{E}$ low			1	µs

NOTE 4: When programming the TMS2732A, connect a 0.1 µF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.

programming characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level [illegible]		2		$V_{CC}+1$	V
V_{IL}	Low-level [illegible]		−0.1		0.8	V
V_{OH}	High-level output voltage (verify)	$I_{OH} = -400$ µA	2.4			V
V_{OL}	Low-level output voltage (verify)	$I_{OL} = 2.1$ mA			0.45	V
I_I	Input current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	µA
I_{PP}	[illegible]	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$			50	mA
I_{CC}	[illegible]				[illegible]	mA
$t_{dis(PR)}$	Output disable time		0		130	ns

PARAMETER MEASUREMENT INFORMATION

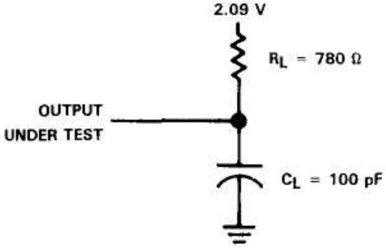
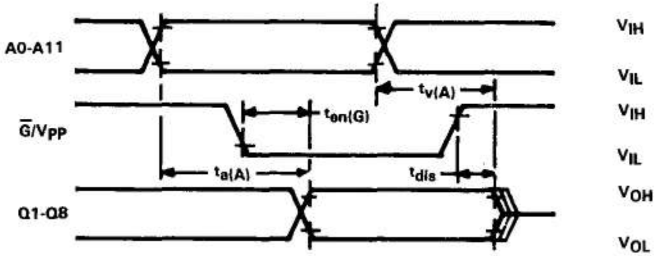
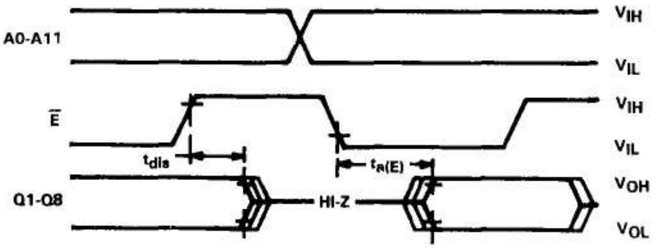


FIGURE 1. TYPICAL OUTPUT LOAD CIRCUIT

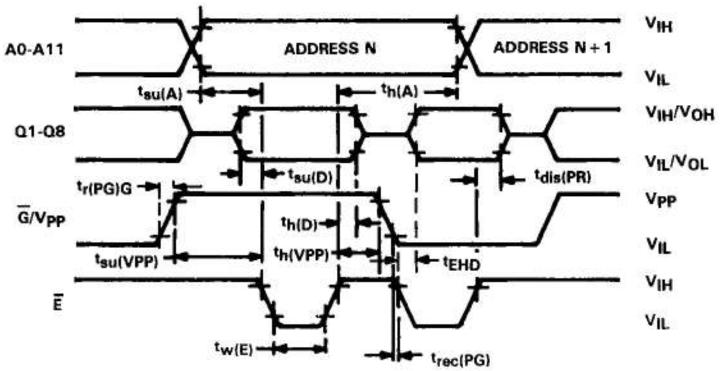
read cycle timing



standby mode



program cycle timing



TMS2764
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

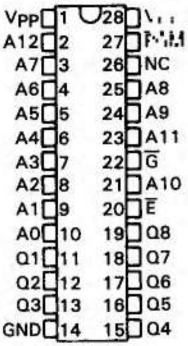
JULY 1983 — REVISED NOVEMBER 1985

- **Organization . . . 8192 X 8**
- **Single 5-V Power Supply**
- **Pin Compatible with TMS2732A EPROM**
- **All Inputs and Outputs Are TTL Compatible**
- **Max Access/Min Cycle Time**

TMS2764-17	**170 ns**
TMS2764-20	**200 ns**
TMS2764-25	**250 ns**
TMS2764-45	**450 ns**

- **Low Standby Power Dissipation . . . 184 mW (Maximum)**
- **JEDEC Approved Pinout**
- **21-V Power Supply Required for Programming**
- **Fast Programming Algorithm**
- **N-Channel Silicon-Gate Technology**
- **PEP4 Version Available with 168 Hour Burn-in and Guaranteed Operating Temperature Range from −10 °C to 85 °C (TMS2764-__JP4)**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8.	Outputs
V_{CC}	5-V Power Supply
V_{PP}	21-V Power Supply

description

The TMS2764 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS2764-17 only requires a single 5-volt power supply with a tolerance of ±5%, and has a maximum access time of 170 ns. This access time is compatible with high-performance microprocessors.

The TMS2764 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS2764 has a power-down mode that reduces maximum power dissipation from 150 mA to 35 mA when the device is placed on standby.

This EPROM is supplied in a 28-pin, 15,2-mm (600-mil) dual-in-line ceramic package and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMS2764 are listed in the following table.

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FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X
[illegible] (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP} or V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IH} or V_{IL}

read

The two control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 150 mA to 35 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

erasure

Before programming, the TMS2764 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 mW/cm2 UV lamp will erase the device in approximately 20 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2764, the window should be covered with an opaque label.

fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS2764.

After erasure, logic "0's" are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addresed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied, if correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and V_{PP} = 21.0 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V. A flowchart of the fast programming routine is shown in Figure 1.

multiple device programming

Several TMS2764's can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS2764's connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

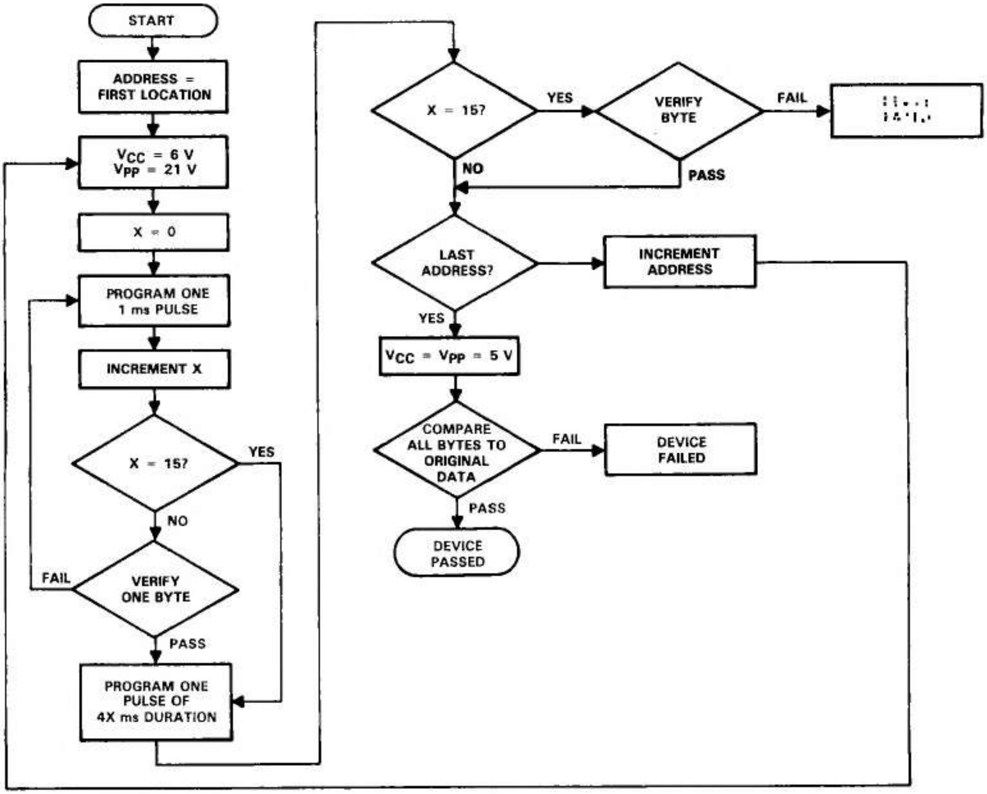
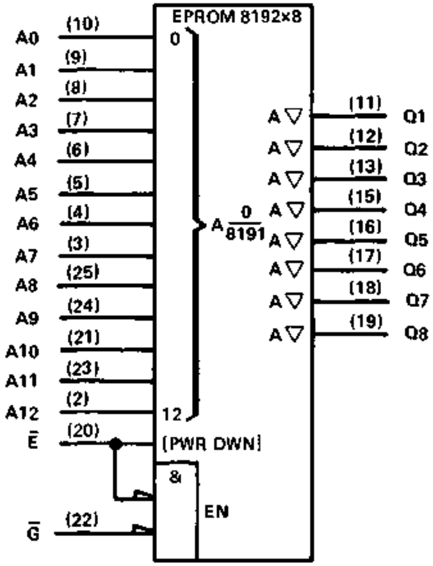


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}	−0.6 V to 7 V
Supply voltage range, V_{PP}	−0.6 V to 22 V
Input voltage range	−0.6 V to 7 V
Output voltage range	−0.6 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

[‡] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 1)	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 2.1$ mA		0.45	V
I_I	Input current (load)	$V_I = 0$ V to 5.25 V		±10	μA
I_O	Output current (leakage)	$V_O = 0.4$ V to 5.25 V		±10	μA
I_{PP1}	V_{PP} supply current (read)	$V_{PP} = 5.25$ V		15	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and $\overline{PGM}$ at V_{IL}		50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}		35	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		150	mA

capacitance over recommended supply voltage range and operating free-air temperature range, $f = 1$ MHz[†]

PARAMETER		TEST CONDITIONS	TYP[‡]	MAX	UNIT
C_i	Input capacitance	$V_I = 0$ V	4	6	pF
C_o	Output capacitance	$V_O = 0$ V	8	12	pF

[†] Capacitance measurements are made on a sample basis only.

[‡] Typical values are at $T_A = 25\,°C$ and nominal voltage.

switching characteristics over recommended supply voltage range and operating free-air temperature range, $C_L = 100$ pF, 1 Series 74 TTL load (see Note 2 and Figure 2)

PARAMETER		TMS2764-17		TMS2764-20		TMS2764-25		TMS2764-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		170		[illegible]		250		4[illegible]	ns
$t_{a(E)}$	Access time from $\overline{E}$		170		200		250		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		65		75		100		150	ns
$t_{dis(G)}$[‡]	Output disable time from $\overline{G}$	0	60	0	60	0	85	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		0		ns

NOTE 2: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2 V.

[‡] Value claculated from 0.5 volt delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read cycle timing diagram. This parameter is only sampled and is not 100% tested.

recommended conditions for fast programming routine, T_A = 25 °C (see Note 2 and fast programming cycle timing diagram)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Program voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs

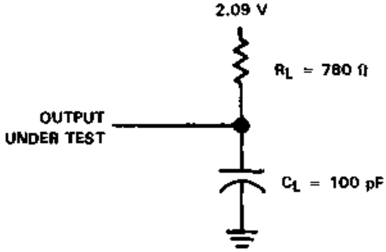
fast programming characteristics, T_A = 25 °C (see Note 2 and fast programming cycle timing diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0		130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL Load			150	

NOTES: 2. For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2 V.

3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS2764, connect a 0.1 µF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The Initial program pulse duration tolerance is 1 ms ±5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of Initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

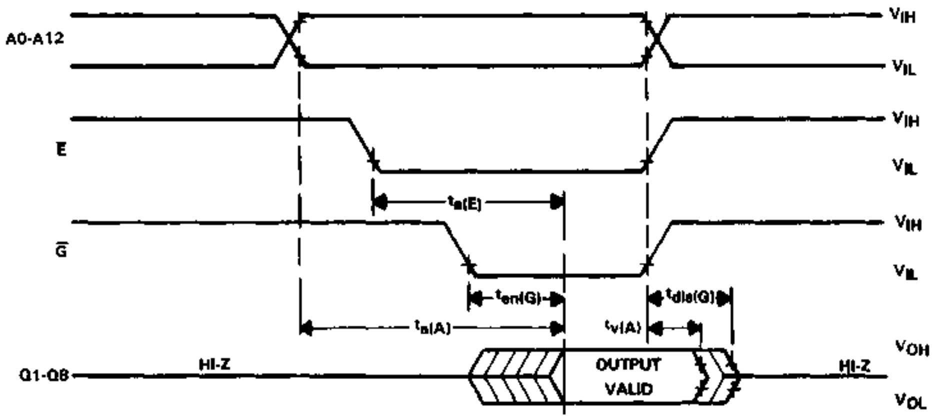
PARAMETER MEASUREMENT INFORMATION



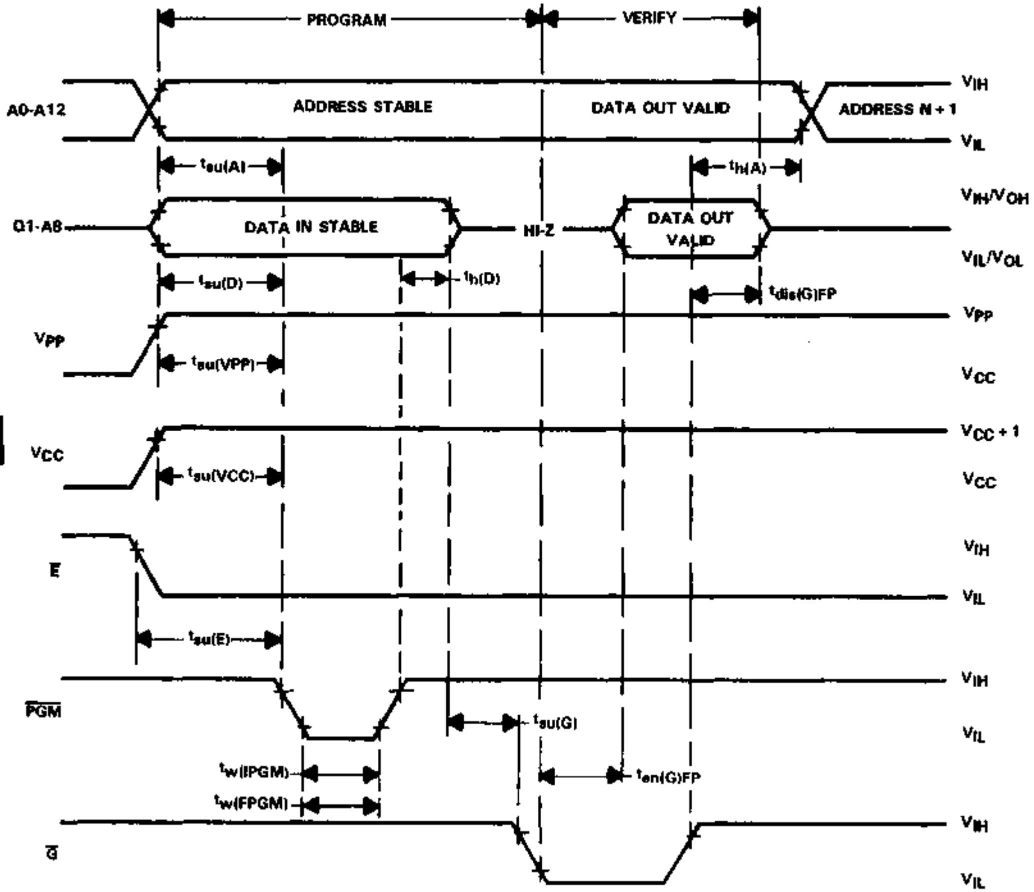
NOTE 8: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

FIGURE 2. TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



fast program cycle timing



ERASABLE PROGRAMMABLE READ-ONLY MEMORY

ENHANCED PERFORMANCE EPROMS — PEP4

- 168 *hr* ± 8 hr Burn-in at 125°C
- Tested to 0.1% AQL
- Extended Temperature Range

Texas Instruments offers extended temperature range EPROMs which provide an enhanced degree of reliability.

The PEP4 designation signifies:

- Devices Subjected to Electrical Testing over a Temperature Range Exceeding Commercial Requirements.
- All Devices Have Received a 168 hr ± 8 hr 125°C Burn-in with a PDA of 2%.

This combination results in an improved quality and reliability level for those applications which deem it necessary. The user benefits from improved long term cost realized through reduced system down-time.

PEP4 PRODUCT FAMILY

DEVICE	ORGANIZATION	MAXIMUM ACCESS TIME (ns)	V_{CC} SUPPLY VOLTAGE (V) MIN	V_{CC} SUPPLY VOLTAGE (V) MAX	OPERATING TEMPERATURE RANGE (°C)
TMS2732A-__JP4	4096 X 8	250	4.5	5.5	−10 to 85
		450	4.5	5.5	−10 to 85
TMS2764-__JP4	8192 X 8	250	4.5	5.5	−10 to 85
		450	4.5	5.5	−10 to 85

ELECTRICAL CHARACTERISTICS

PEP4 EPROM devices meet or exceed all the electrical and timing parameters specified in the standard data sheet with the following exceptions.

PARAMETER		TMS2732A-__JP4 MAX	TMS2764-__JP4 MAX	UNIT
I_{CC1}	V_{CC} supply current (standby)	35	40	mA
I_{CC2}	V_{CC} supply current (active)	[illegible]		mA

ADVANCE
INFORMATION

TMS27C64
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

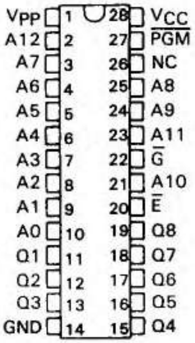
NOVEMBER 1985

- Organization . . . 8K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K EPROMs and TMS2732A
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27C64-1,	'27C64-15	150 ns
'27C64-2,	'27C64-20	200 ns
'27C64,	'27C64-25	250 ns
'27C64-3,	'27C64-30	300 ns
'27C64-4,	'27C64-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  - —Active . . . 210 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{\mathrm{E}}$	Chip Enable/Power Down
$\overline{\mathrm{G}}$	Output Enable
GND	Ground
NC	No Connection
$\overline{\mathrm{PGM}}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMS27C64 series are 65,536-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS27C64 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the TMS27C64 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

ADVANCE INFORMATION documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	CODE MFG 97	 DEVICE 07

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C64's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the TMS27C64, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 40 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the TMS27C64 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C64, the window should be covered with an opaque label.

fast programming

After erasure (all bits in logic '1' state), logic '0's are programmed into the desired locations. A programmed '0' can only be erased by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, $\overline{PGM}$ = V_{IL}, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one TMS27C64 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full fast programming routine is complete, all bits are verified with $V_{CC} = V_{PP}$ = 5 V (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$ and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10) i.e., A0 = V_{IL} − manufacturer; A0 = V_{IH} − device. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 07.

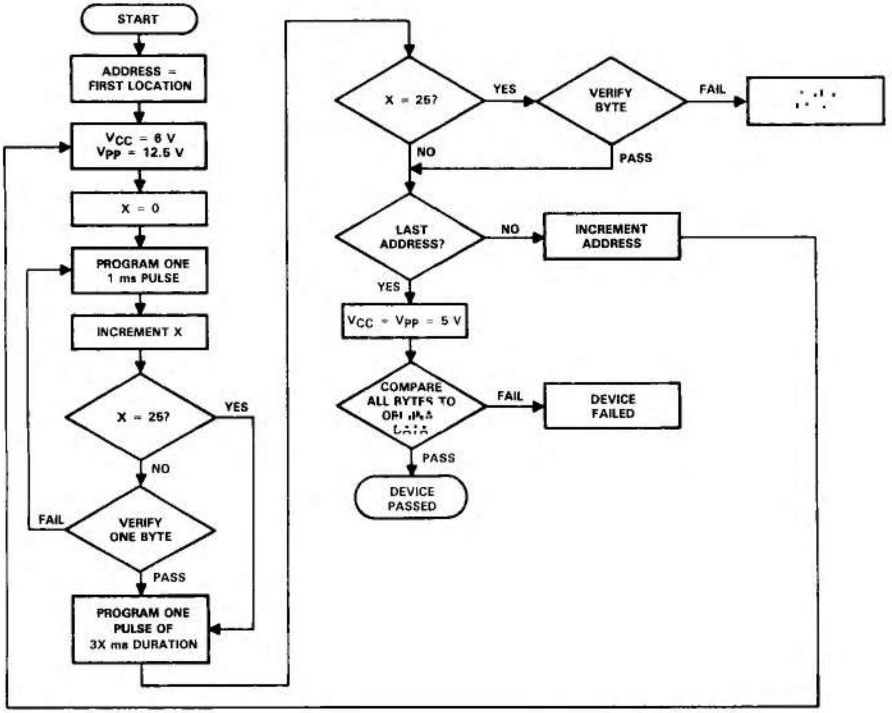
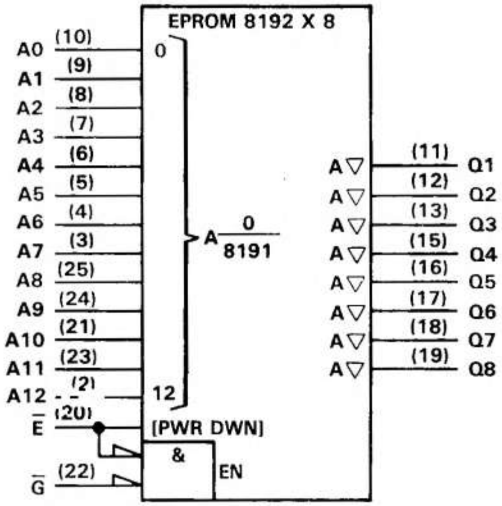


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	−0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9	−0.6 V to 6.5 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 1)	−0.6 V to V_{CC} + 1 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			TMS27C64-1 TMS27C64-2 TMS27C64 TMS27C64-3 TMS27C64-4			TMS27C64-15 TMS27C64-20 TMS27C64-25 TMS27C64-30 TMS27C64-45			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA			0.4	V
I_I	Input current (leakage)		$V_I = 0$ V to 5.5 V			±10	µA
I_O	Output current (leakage)		$V_O = 0$ V to V_{CC}			±10	µA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V			100	µA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP} = 13$ V		30	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$			500	µA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$			250	µA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		30	40	mA

†Typical values are at $T_A = 25°C$ and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I = 0$ V, f = 1 MHz		6	9	pF
C_o	Output capacitance	$V_O = 0$ V, f = 1 MHz		8	12	pF

†Capacitance measurements are made on sample basis only.
‡Typical values are at $T_A = 25°C$ and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C64-1 '27C64-15		'27C64-2 '27C64-20		'27C64 '27C64-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		150		200		250	ns
$t_{a(E)}$	Access time from chip enable			150		[illegible]		[illegible]	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C64-3 '27C64-30		'27C64-4 '27C64-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		300		450	ns
$t_{a(E)}$	Access time from chip enable			300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			120		150	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, $T_A = 25\,°C$, $V_{CC} = 6$ V, $V_{PP} = 12.5$ V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.

5. Common test conditions apply for $t_{dis(G)}$ except during programming.

PARAMETER MEASUREMENT INFORMATION

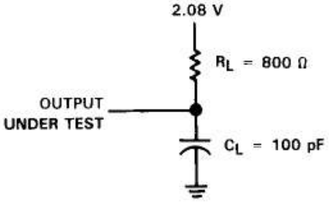
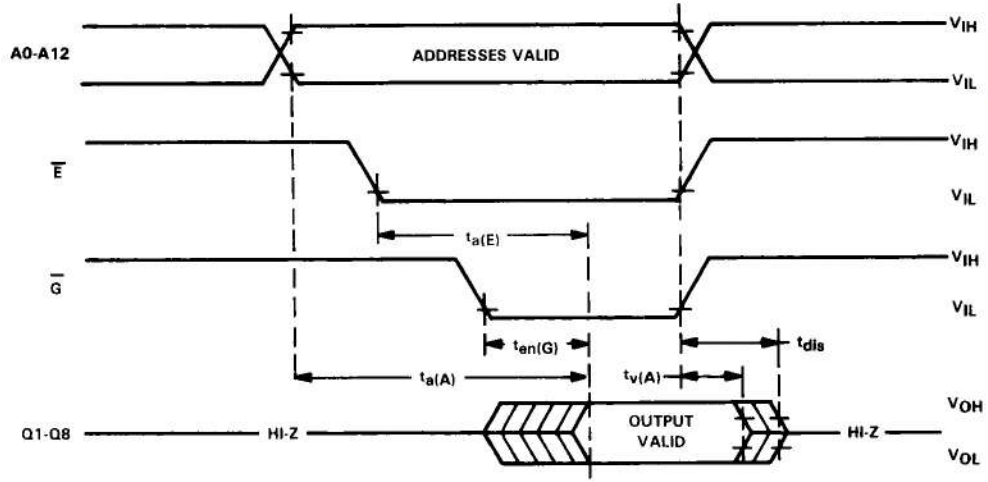
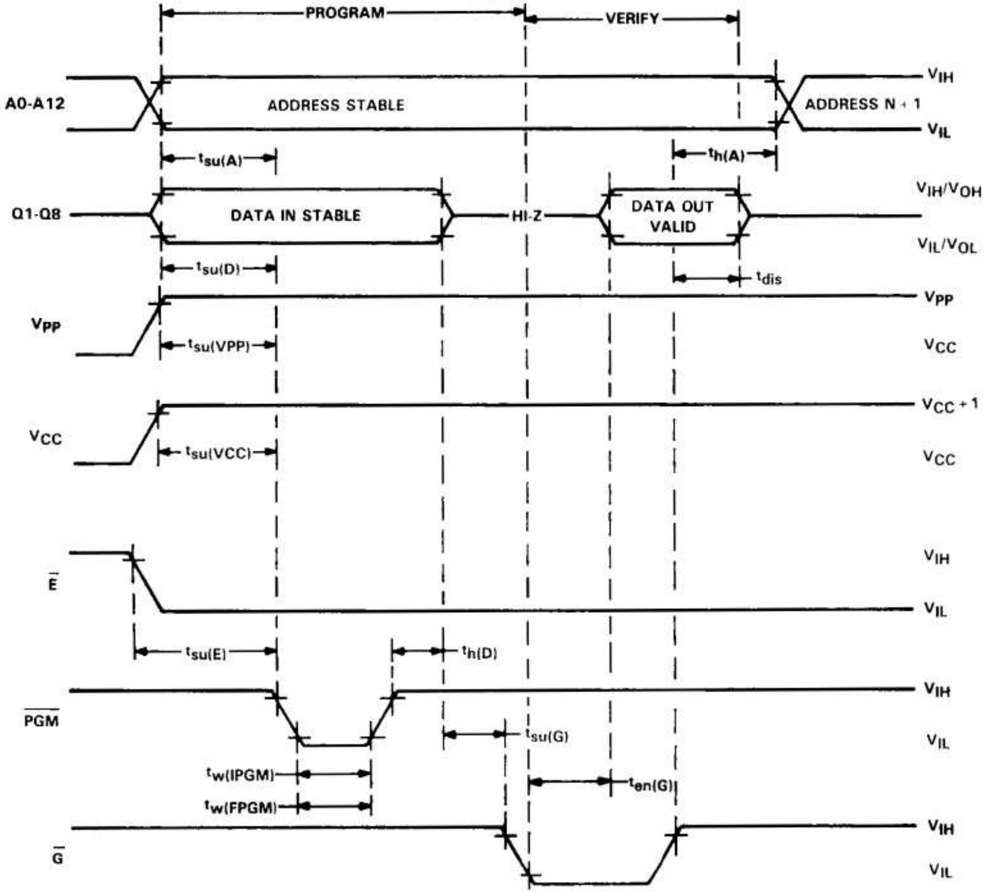


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



TMS27C128
131,072-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

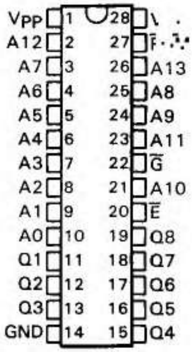
OCTOBER 1984 – REVISED NOVEMBER 1985

- **Organization . . . 16K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 64K and 128K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

'27C128-1,	**'27C128-15**	**150 ns**
'27C128-2,	**'27C128-20**	**200 ns**
'27C128,	**'27C128-25**	**250 ns**
'27C128-3,	**'27C128-30**	**300 ns**
'27C128-4,	**'27C128-45**	**450 ns**

- **HVCMOS Technology**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity with Standard TTL Loads**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **—Active . . . 210 mW Worst Case**
  - **—Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0-A13	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMS27C128 series are 131,072-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMS27C128 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operete from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the TMS27C128 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X	V_{IH}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	[illegible] MFG 97	 DEVICE 83

†X can be V_{IL} or V_{IH}.
‡$V_H = 12\ V \pm 0.5\ V$.

read/output disable

When the outputs of two or more TMS27C128's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the TMS27C128, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 40 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the TMS27C128 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C128, the window should be covered with an opaque label.

fast programming

After erasure (all bits are in logic '1' state), logic '0's are programmed into the desired locations. A programmed '0' can only be erased by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{PGM}$ is pulsed. The programming mode is achieved when $V_{PP} = 12.5\ V$, [illegible] $= V_{IL}$, $V_{CC} = 6.0\ V$, $\overline{G} = V_{IH}$, and $\overline{E} = V_{IL}$. More than one TMS27C128 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional 1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at $V_{CC} = 6.0$ V and $V_{PP} = 12.5$ V. When the full fast programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5$ V (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin or $\overline{PGM}$ pin.

program verify

Programmed bits may be verified with $V_{PP} = 12.5$ V when $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and $\overline{PGM} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10) i.e., $A0 = V_{IL}$ – manufacturer; $A0 = V_{IH}$ – device. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 83.

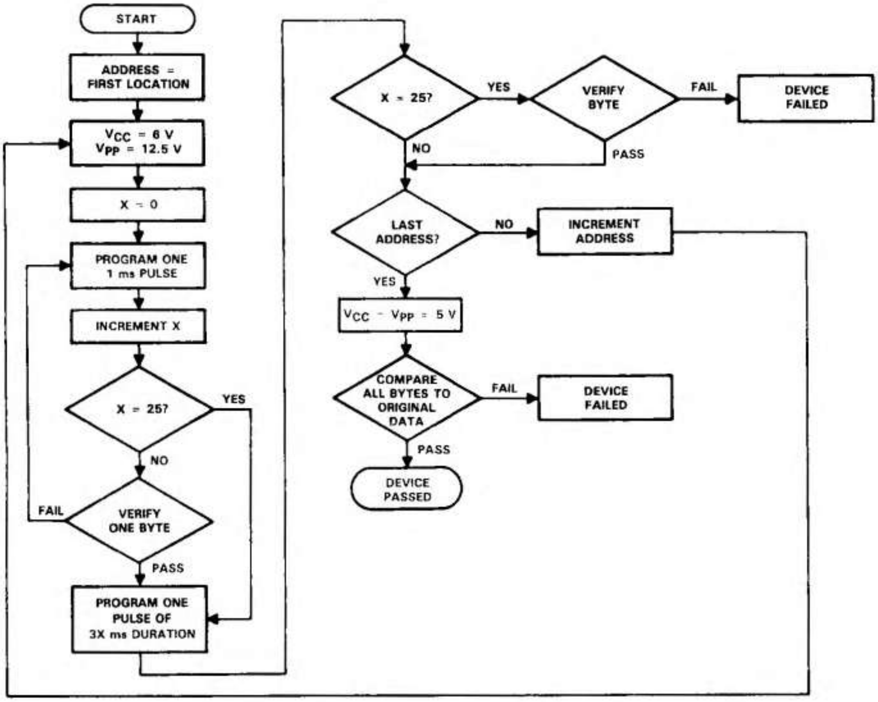
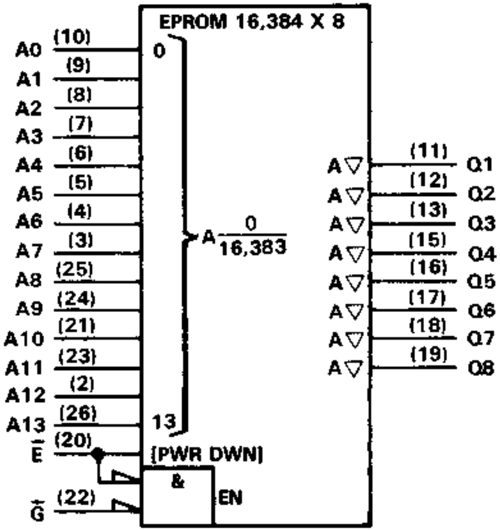


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	−0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9	−0.6 V to 6.5 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 1)	−0.6 V to V_{CC} + 1 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

recommended operating conditions

			TMS27C128-1 TMS27C128-2 TMS27C128 TMS27C128-3 TMS27C128-4			TMS27C128-15 TMS27C128-20 TMS27C128-25 TMS27C128-30 TMS27C128-45			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA			0.4	V
I_I	Input current (leakage)		$V_I = 0$ V to 5.5 V			±10	μA
I_O	Output current (leakage)		$V_O = 0$ V to V_{CC}			±10	μA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V			100	μA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP} = 13$ V		30	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$			500	μA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$			250	μA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		30	40	mA

[†] Typical values are at $T_A = 25°C$ and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz[†]

PARAMETER		TEST CONDITIONS	MIN	TYP[‡]	MAX	UNIT
C_i	Input capacitance	$V_I = 0$ V, f = 1 MHz		6	9	pF
C_o	Output capacitance	$V_O = 0$ V, f = 1 MHz		8	12	pF

[†] Capacitance measurements are made on sample basis only.

[‡] Typical values are at $T_A = 25°C$ and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-1 '27C128-15		'27C128-2 '27C128-20		'27C128 '27C128-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		150		[illegible]		250	ns
$t_{a(E)}$	Access time from chip enable			150		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C128-3 '27C128-30		'27C128-4 '27C128-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		300		450	ns
$t_{a(E)}$	Access time from chip enable			300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			120		150	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		ns

†Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, $T_A = 25°C$, $V_{CC} = 6$ V, $V_{PP} = 12.5$ V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and V_{PP} = 12.5 V ±0.5 V during programming.
5. Common test conditions apply for $t_{dis(G)}$ except during programming.

PARAMETER MEASUREMENT INFORMATION

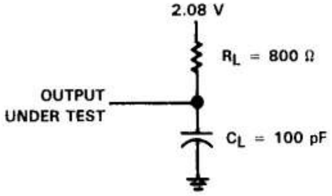
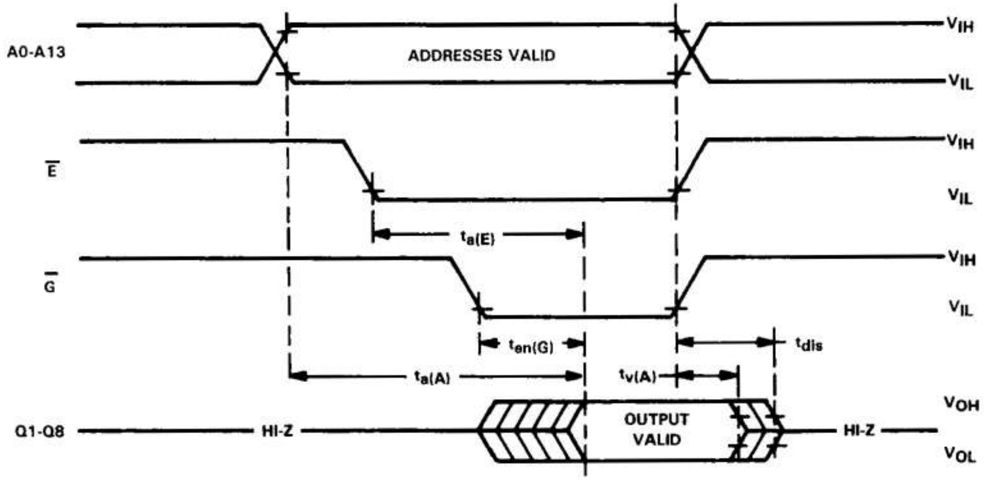
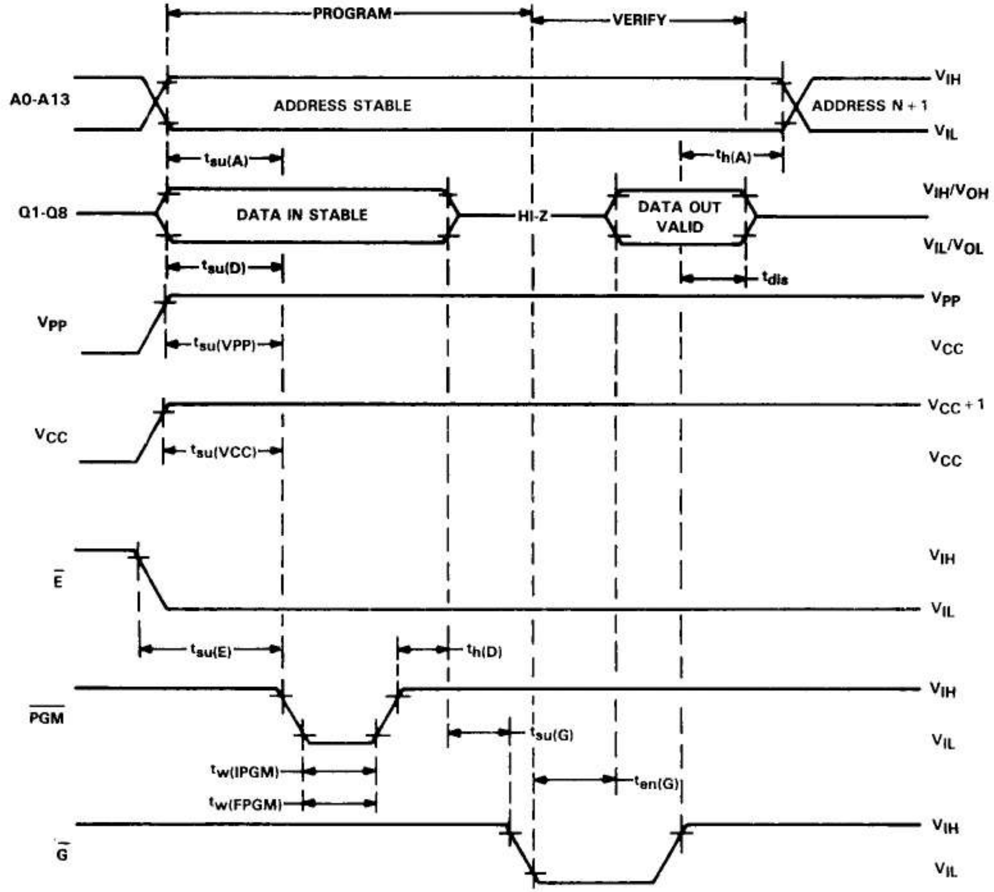


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



TMS27C256
262,144-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

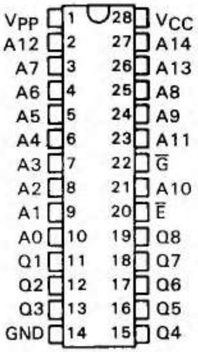
SEPTEMBER 1984 — REVISED NOVEMBER 1985

- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 128K and 256K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

'27C256-1,	'27C256-17	170 ns
'27C256-2,	'27C256-20	200 ns
'27C256,	'27C256-25	250 ns
'27C256-3,	'27C256-30	300 ns
'27C256-4,	'27C256-45	450 ns

- **HVCMOS Technology**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity with Standard TTL Loads**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **—Active . . . 210 mW Worst Case**
  - **—Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)**

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMS27C256 series are 262,144-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMS27C256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation for the TMS27C256 listed on the following page. Read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (12.5 V) and 12 V on A9 for signature mode.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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FUNCTION (PINS)	MODE							
	Read	Output Disable	Standby	Programming	Verify	Program Inhibit	Signature Mode	
$\overline{E}$ (20)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$ (22)	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	V_{IH}	V_{IL}	
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9 (24)	X	X	X	X	X	X	V_H‡	V_H‡
A0 (10)	X	X	X	X	X	X	V_{IL}	V_{IH}
Q1-Q8 (11-13, 15-19)	D_{OUT}	HI-Z	HI-Z	D_{IN}	D_{OUT}	HI-Z	MFG 97	DEVICE 04

†X can be V_{IL} or V_{IH}.
‡V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C256's are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the TMS27C256, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active I_{CC} current can be reduced from 40 mA to 500 μA (TTL-level inputs) or 250 μA (CMOS-level inputs) by applying a high TTL signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state.

erasure

Before programming, the TMS27C256 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwat per square centimeter, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C256, the window should be covered with an opaque label.

fast programming

After erasure (all bits in logic '1' state), logic '0's are programmed into the desired locations. A programmed '0' can only be erased by ultraviolet light. Data is presented in parallel (eight bits) on pins Q1 to Q8. Once addresses and data are stable, $\overline{E}$ is pulsed. The programming mode is achieved when V_{PP} = 12.5 V, V_{CC} = 6.0 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. More than one TMS27C256 can be programmed when the devices are connected in parallel. Locations can be programmed in any order.

Programming uses two types of programming pulses: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each Prime pulse, the byte being programmed is verified. If the correct data is read, the Final programming pulse is applied; if correct data is not read, an additional

1 millisecond pulse is applied up to a maximum X of 25. The Final programming pulse is 3X long. This sequence of programming and verification is performed at V_{CC} = 6.0 V and V_{PP} = 12.5 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V (see Figure 1).

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with V_{PP} = 12.5 V when $\overline{G}$ = V_{IL}, and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 24) is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0 (pin 10) i.e., A0 = V_{IL} − manufacturer; A0 = V_{IH} − device. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit Q8. The manufacturer code for this device is 97, and the device code is 04.

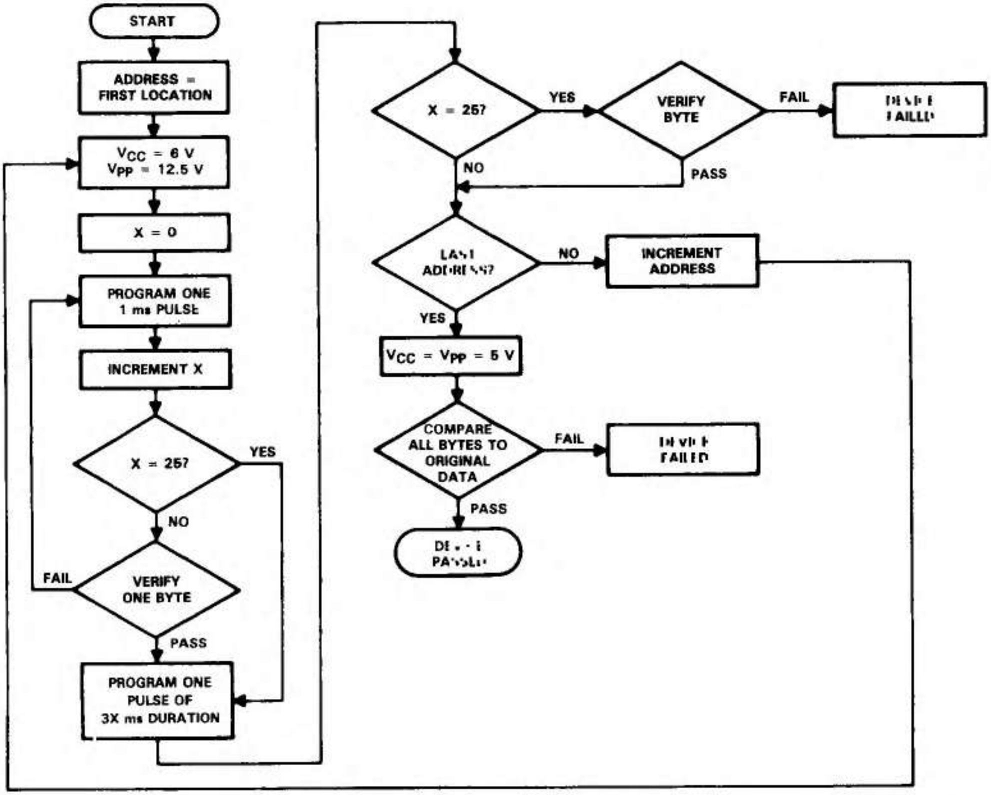
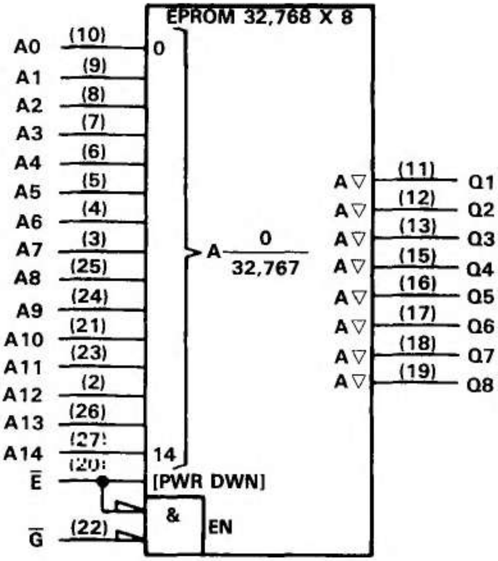


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Supply voltage range, V_{PP} (see Note 1)	−0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9	−0.6 V to 6.5 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 1)	−0.6 V to V_{CC} + 1 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to GND.

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			TMS27C256-1 TMS27C256-2 TMS27C256 TMS27C256-3 TMS27C256-4			TMS27C256-17 TMS27C256-20 TMS27C256-25 TMS27C256-30 TMS27C256-45			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		4.75	5	5.25	4.5	5	5.5	V
V_{PP}	Supply voltage (see Note 3)			V_{CC}			V_{CC}		V
V_{IH}	High-level input voltage	TTL	2		$V_{CC}+1$	2		$V_{CC}+1$	V
		CMOS	$V_{CC}-0.2$		$V_{CC}+0.2$	$V_{CC}-0.2$		$V_{CC}+0.2$	V
V_{IL}	Low-level input voltage	TTL	−0.5		0.8	−0.5		0.8	V
		CMOS	GND−0.2		GND+0.2	GND−0.2		GND+0.2	V
T_A	Operating free-air temperature		0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 12.5 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low-level output voltage		$I_{OL} = 2.1$ mA			0.4	V
I_I	Input current (leakage)		$V_I = 0$ V to 5.5 V			±10	μA
I_O	Output current (leakage)		$V_O = 0$ V to V_{CC}			±10	μA
I_{PP1}	V_{PP} supply current		$V_{PP} = V_{CC} = 5.5$ V			100	μA
I_{PP2}	V_{PP} supply current (during program pulse)		$V_{PP} = 13$ V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$			500	μA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$			250	μA
I_{CC2}	V_{CC} supply current (active)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, t_{cycle} = minimum cycle time, outputs open		30	40	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz[†]

PARAMETER		TEST CONDITIONS	MIN	TYP[‡]	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		6	9	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		8	12	pF

[†] Capacitance measurements are made on sample basis only.

[‡] Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-1 '27C256-17		'27C256-2 '27C256-20		'27C256 '27C256-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first[†]		0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first[†]		0		0		0		ns

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	'27C256-3 '27C256-30		'27C256-4 '27C256-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \leq 20$ ns, Input $t_f \leq 20$ ns		300		450	ns
$t_{a(E)}$	Access time from chip enable			300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			120		150	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first[†]		0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first[†]		0		0		ns

[†] Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended timing requirements for programming, $T_A = 25°C$, $V_{CC} = 6$ V, $V_{PP} = 12.5$ V (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(IPGM)}$	Initial program pulse duration	0.95	1	1.05	ms
$t_{w(FPGM)}$	Final pulse duration	2.85		78.75	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.40 V to 2.4 V and $V_{PP} = 12.5$ V ±0.5 V during programming.

5. Common test conditions apply for $t_{dis(G)}$ except during programming.

PARAMETER MEASUREMENT INFORMATION

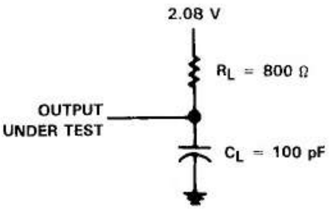
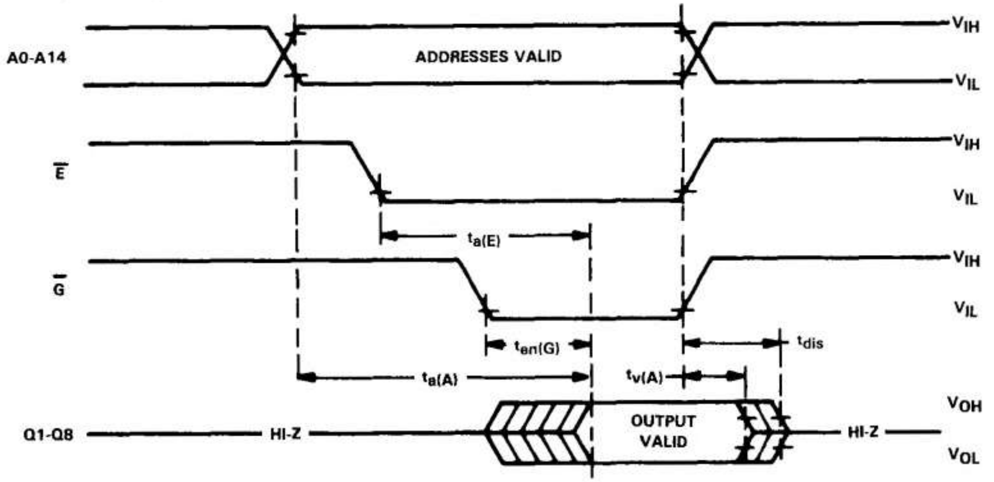
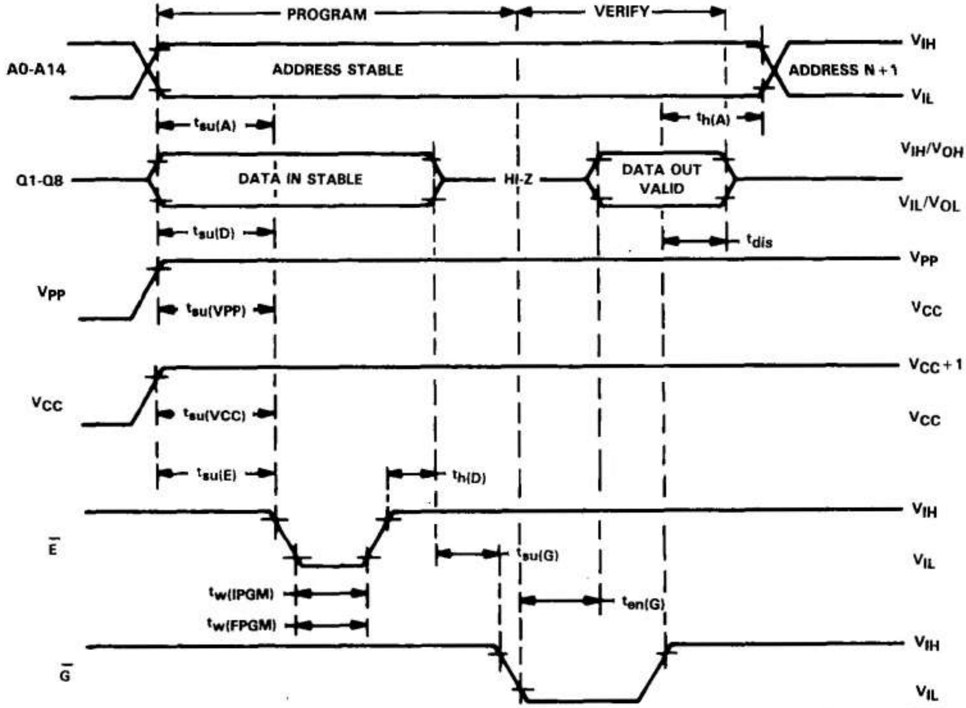


FIGURE 2. OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



PRODUCT PREVIEW

TMX27C512
524,288-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

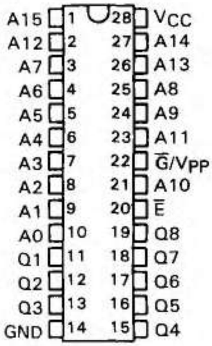
NOVEMBER 1985

- Organization . . . 64K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 512K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27C512-2,	'27C512-20	200 ns
'27C512,	'27C512-25	250 ns
'27C512-3,	'27C512-30	300 ns
'27C512-4,	'27C512-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  - —Active . . . 263 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

J PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A15	Address Inputs
$\overline{E}$	Chip Enable/Power Down
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
$\overline{G}/V_{PP}$	12.5-V Power Supply/ Output Enable

description

The TMX27C512 series are 524,288-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMX27C512 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line ceramic package (J suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

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ADVANCE INFORMATION

TMS27P32A
32,768-BIT PROGRAMMABLE READ-ONLY MEMORY

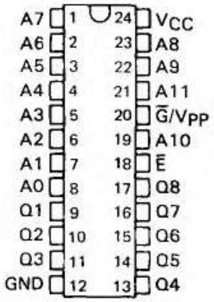
NOVEMBER 1985

- **Organization . . . 4096 X 8**
- **Single 5-V Power Supply**
- **All Inputs and Outputs Are TTL Compatible**
- **Max Access/Min Cycle Time**

TMS27P32A-25	**250 ns**
TMS27P32A-30	**300 ns**
TMS27P32A-45	**450 ns**

- **Low Standby Power Dissipation . . . 158 mW (Maximum)**
- **JEDEC Approved Pinout . . . Industry Standard**
- **21-V Power Supply Required for Programming**
- **N-Channel Silicon-Gate Technology**

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A11	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}/V_{PP}$	Output Enable/21 V
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply

description

The TMS27P32A is a one-time, electrically programmable read-only memory. It has 32,768 bits organized as 4,096 words of 8-bit length. The TMS27P32A only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS27P32A provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in multibus microprocessor systems. The TMS27P32A has a power-down mode that reduces maximum power dissipation from 657 mW to 158 mW when the device is placed on standby.

This PROM is supplied in a 24-pin dual-in-line plastic package and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMS27P32A are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Deselect	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{E}$ (18)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}/V_{PP}$ (20)	V_{IL}	V_{IH}	X	21 V	V_{IL}	21 V
V_{CC} (24)	5 V	5 V	5 V	5 V	5 V	5 V
Q1-Q8 (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IH} or V_{IL}

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read

The two control pins ($\overline{\mathrm{E}}$ and $\overline{\mathrm{G}}/V_{PP}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{\mathrm{E}}$) should be used for device selection. Output enable ($\overline{\mathrm{G}}/V_{PP}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum power dissipation from 657 mW to 158 mW. A TTL high-level signal applied to $\overline{\mathrm{E}}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{\mathrm{G}}/V_{PP}$.

program

The programming procedure for the TMS27P32A is the same as that for the TMS2732A.

The program mode consists of the following sequence of events. With the level on $\overline{\mathrm{G}}/V_{PP}$ equal to 21 V, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a 10-millisecond TTL low-level pulse is applied to $\overline{\mathrm{E}}$. The maximum width of this pulse is 11 milliseconds. The programming pulse must be applied at each location that is to be programmed. Locations may be programmed in any order.

Several TMS27P32As can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

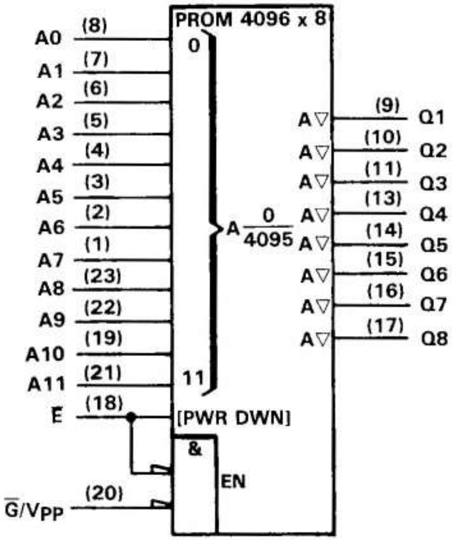
program verify

After the PROM has been programmed, the programmed bits should be verified. To verify bit states, $\overline{\mathrm{G}}/V_{PP}$ and $\overline{\mathrm{E}}$ are set to V_{IL}.

program inhibit

The program inhibit is useful when programming multiple TMS27P32As connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{\mathrm{E}}$ of the device that is not to be programmed.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.3 V to 7 V
Supply voltage range, V_{PP}	−0.3 V to 22 V
Input voltage range (except program)	−0.3 V to 7 V
Output voltage range	−0.3 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)	4.75	5	5.25	V
V_{PP}	Supply voltage (see Note 2)		V_{CC}		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 1. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

2. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 21 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -400\ \mu A$	2.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 2.1$ mA		0.45	V
I_I	Input current (leakage)	$V_I = 0$ V to 5.25 V		±10	µA
I_O	Output current (leakage)	$V_O = 0.4$ V to 5.25 V		±10	µA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}, $\overline{G}$ at V_{IL}		30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		125	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz[†]

PARAMETER			TEST CONDITIONS	TYP[‡]	MAX	UNIT
C_i	Input capacitance	All except $\overline{G}/V_{PP}$	$V_I = 0$ V	4	6	pF
		$\overline{G}/V_{PP}$			20	
C_o	Output capacitance		$V_O = 0$ V	8	12	pF

[†] Capacitance measurements are made on a sample basis only.
[‡] Typical values are at $T_A = 25\,°C$ and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS (SEE NOTE 3)	TMS27P32A-25		TMS27P32A-30		TMS27P32A-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	$C_L = 100$ pF, 1 Series 74 TTL Load, $t_r \leq 20$ ns, $t_f \leq 20$ ns, See Figure 1		[illegible]		300		[illegible]	ns
$t_{a(E)}$	Access time from $\overline{E}$			250		300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			100		150		150	ns
t_{dis}[†]	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first		0	85	0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		ns

NOTE 3: The timing reference levels for inputs and outputs are 0.8 V and 2 V. Input pulse levels are 0.40 V and 2.4 V.
[†] Value calculated from 0.5 V delta to measured output level. This parameter is only sampled and not 100% tested.

recommended conditions for programming, $T_A = 25°C$ (see Note 4)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	20.5	21	21.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
$t_{w(E)}$	$\overline{E}$ pulse duration	9	10	11	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(VPP)}$	V_{PP} hold time	2			μs
$t_{rec(PG)}$	V_{PP} recovery time	2			μs
$t_{r(PG)G}$	$\overline{G}$ rise time during programming	50			ns
t_{EHD}	Delay time, data valid after $\overline{E}$ low			1	μs

NOTE 4: When programming the TMS27P32A, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.

programming characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{OH}	High-level output voltage (verify)	$I_{OH} = -400$ μA	2.4			V
V_{OL}	Low-level output voltage (verify)	$I_{OL} = 2.1$ mA			0.45	V
I_I	Input current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
I_{PP}	Supply current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$			50	mA
I_{CC}	Supply current				[illegible]	mA
$t_{dis(PR)}$	Output disable time		0		130	ns

PARAMETER MEASUREMENT INFORMATION

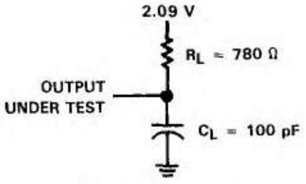
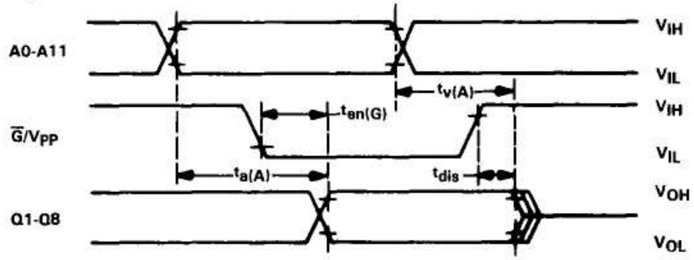
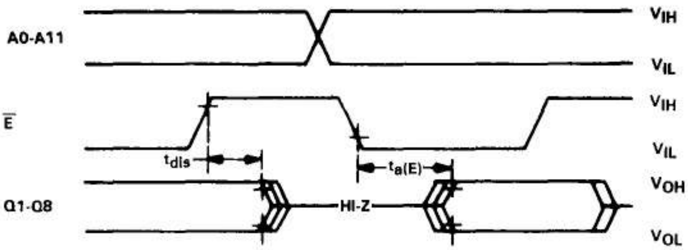


FIGURE 1. TYPICAL OUTPUT LOAD CIRCUIT

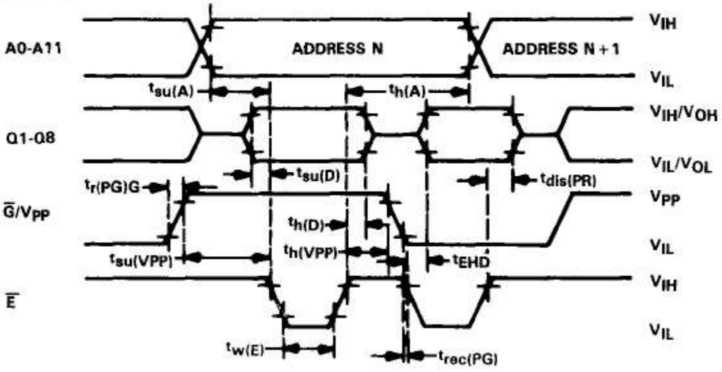
read cycle timing



standby mode



program cycle timing

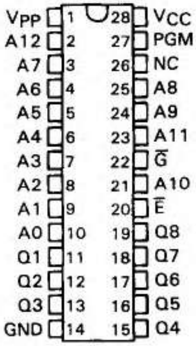


TMS27P64
65,536-BIT PROGRAMMABLE READ-ONLY MEMORY

NOVEMBER 1985

- **Organization . . . 8192 X 8**
- **Single 5-V Power Supply**
- **Pin Compatible with TMS2732A and TMS2764 EPROMs**
- **All Inputs and Outputs Are TTL Compatible**
- **Max Access/Min Cycle Time**
  - **TMS27P64-25 250 ns**
  - **TMS27P64-30 300 ns**
  - **TMS27P64-45 450 ns**
- **Low Standby Power Dissipation . . . 184 mW (MAX)**
- **JEDEC Approved Pinout**
- **21-V Power Supply Required for Programming**
- **Fast Programming Algorithm**
- **N-Channel Silicon-Gate Technology**

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	21-V Power Supply

description

The TMS27P64 is a one-time, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS27P64-25 only requires a single 5-volt power supply with a tolerance of ±5%, and has a maximum access time of 250 ns.

The TMS27P64 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS27P64 has a power-down mode that reduces maximum active current from 150 mA to 35 mA when the device is placed on standby.

This PROM is supplied in a 28-pin, 15,24-mm (600-mil) dual-in-line plastic package and is designed for operation from 0°C to 70°C.

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operation

The six modes of operation for the TMS27P64 are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP} or V_{CC}
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IL} or V_{IH}

read

The dual control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 150 mA to 35 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS27P64.

Initially all locations are logic "1's," logic "0's" are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied, if correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at $V_{CC} = 6.0$ V and $V_{PP} = 21.0$ V. When the full fast programming routine is complete, all bits are verified with $V_{CC} = V_{PP} = 5$ V. A flowchart of the fast programming routine is shown in Figure 1.

multiple device programming

Several TMS27P64's can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS27P64's connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

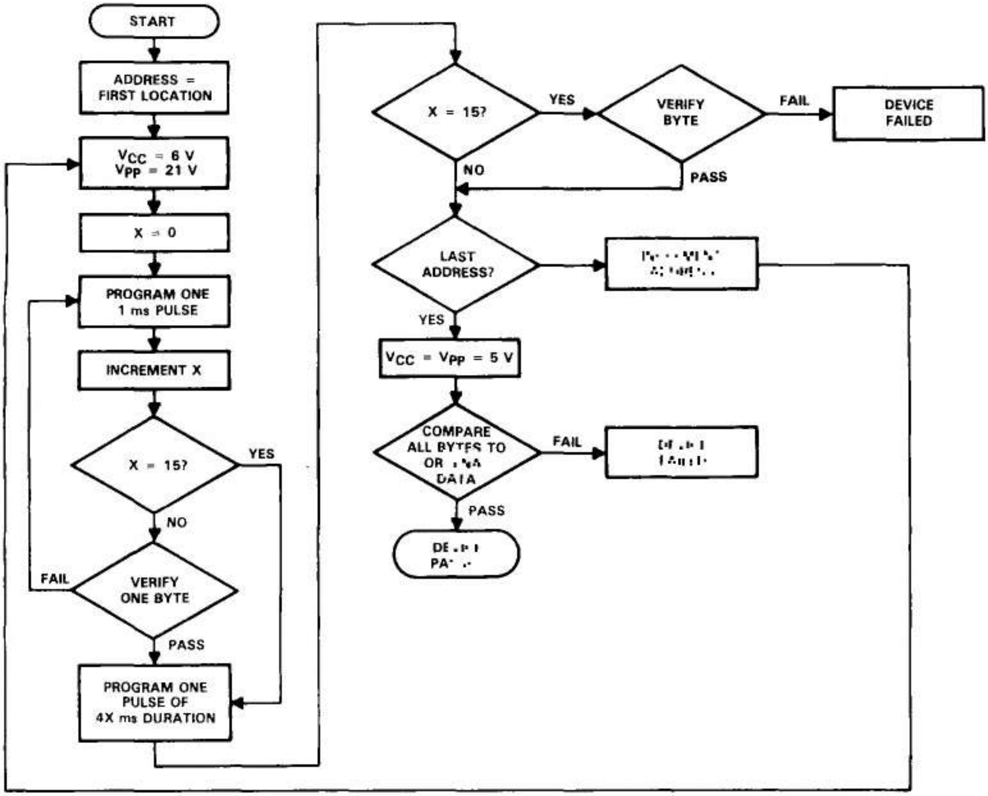
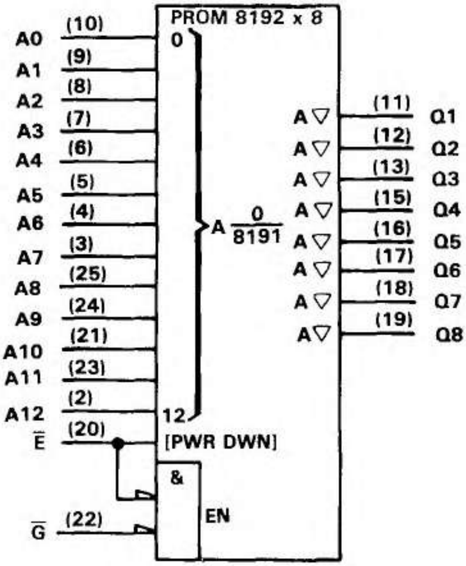


FIGURE 1. FAST PROGRAMMING FLOWCHART

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.6 V to 7 V
Supply voltage range, V_{PP}	−0.6 V to 22 V
Input voltage range	−0.6 V to 7 V
Output voltage range	−0.6 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage		VCC		V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 1)	−0.1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -400\ \mu A$	2.4		[illegible]
V_{OL}	Low-level output voltage	$I_{OL} = 2.1$ mA		0.45	V
I_I	Input current (load)	$V_I = 0$ V to 5.25 V		±10	μA
I_O	Output current (leakage)	$V_O = 0.4$ V to 5.25 V		±10	μA
I_{PP1}	V_{PP} supply current (read)	$V_{PP} = 5.25$ V		15	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and [illegible] at V_{IL}		50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}		35	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		150	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I = 0$ V	4	6	pF
C_o	Output capacitance	$V_O = 0$ V	8	12	pF

†Capacitance measurements are made on a sample basis only.
‡Typical values are at $T_A = 25°C$ and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range, C_L = 100 pF, 1 Series 74 TTL load (see Note 2 and Figure 2)

PARAMETER		TMS27P64-25		TMS27P64-30		TMS27P64-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		250		300		450	ns
$t_{a(E)}$	Access time from $\overline{E}$		250		300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		100		120		150	ns
$t_{dis(G)}$‡	Output disable time from $\overline{G}$	0	85	0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		ns

NOTE 2: For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2 V.

‡Value claculated from 0.5 volt delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read cycle timing diagram. This parameter is only sampled and is not 100% tested.

recommended conditions for fast programming routine, T_A = 25 °C (see Note 2 and fast programming cycle timing diagram)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Supply voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs

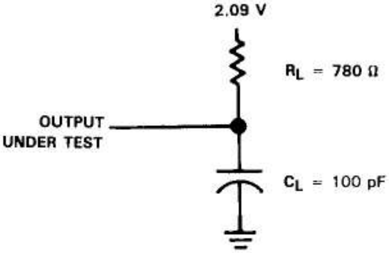
fast programming characteristics, T_A = 25 °C (see Note 2 and fast programming cycle timing diagram)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0	130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL load		150	

NOTES: 2. For all switching characteristics and timing measurements, input pulse levels are 0.40 V and 2.4 V. Input and output timing reference levels are 0.8 V and 2 V.

3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS27P64, connect a 0.1 µF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The Initial program pulse duration tolerance is 1 ms ± 5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of Initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

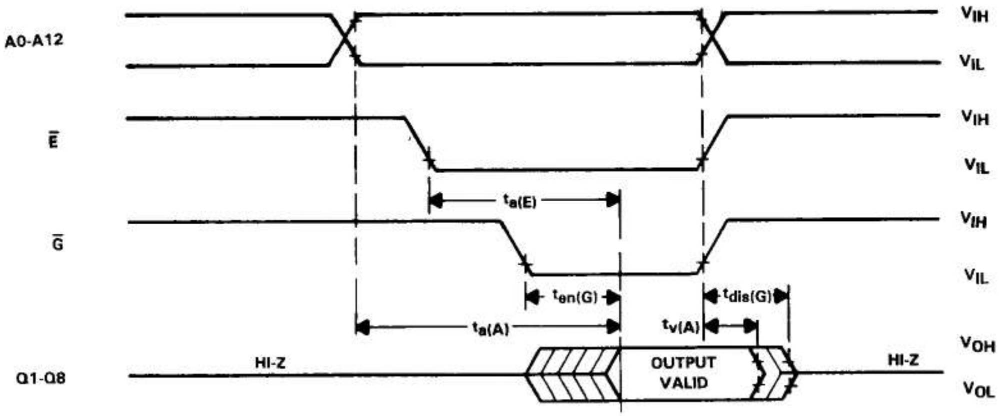
PARAMETER MEASUREMENT INFORMATION



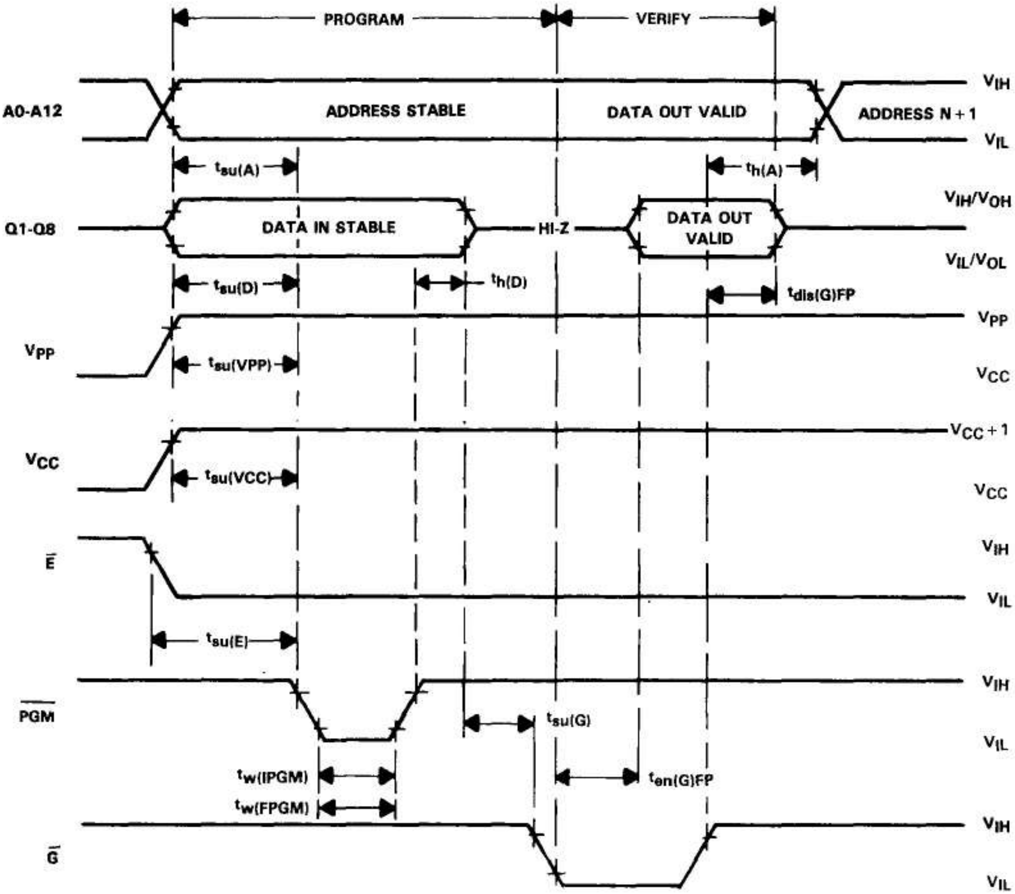
NOTE 8: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

FIGURE 2. TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



fast program cycle timing



PRODUCT PREVIEW

TMX27PC128
131,072-BIT PROGRAMMABLE READ-ONLY MEMORY

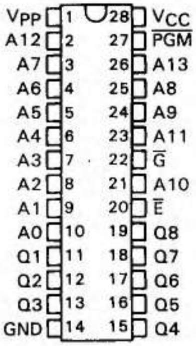
NOVEMBER 1985

- Organization . . . 16K × 8
- Single 5-V Power Supply
- Pin Compatible with Existing 64K and 128K EPROMs
- All Inputs/Outputs Fully TTL Compatible
- Max Access/Min Cycle Time

'27PC128-2,	'27PC128-20	200 ns
'27PC128,	'27PC128-25	250 ns
'27PC128-3,	'27PC128-30	300 ns
'27PC128-4,	'27PC128-45	450 ns

- HVCMOS Technology
- 3-State Output Buffers
- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads
- Low Power Dissipation (V_{CC} = 5.25 V)
  - —Active . . . 210 mW Worst Case
  - —Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMX27PC128 series are 131,072-bit, one-time, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMX27PC128 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line plastic package (N suffix) rated for operation from 0°C to 70°C.

Since these PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

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PRODUCT PREVIEW

TMX27PC256
262,144-BIT PROGRAMMABLE READ-ONLY MEMORY

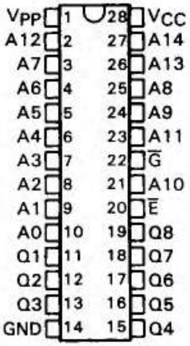
NOVEMBER 1985

- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Pin Compatible with Existing 64K, 128K and 256K EPROMs**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**

'27PC256-2,	'27PC256-20	200 ns
'27PC256,	'27PC256-25	250 ns
'27PC256-3,	'27PC256-30	300 ns
'27PC256-4,	'27PC256-45	450 ns

- **HVCMOS Technology**
- **3-State Output Buffers**
- **400 mV Guaranteed DC Noise Immunity with Standard TTL Loads**
- **Low Power Dissipation (V_{CC} = 5.25 V)**
  - **—Active . . . 210 mW Worst Case**
  - **—Standby . . . 1.4 mW Worst Case (CMOS-Input Levels)**

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
Q1-Q8	Outputs
V_{CC}	5-V Power Supply
V_{PP}	12.5-V Power Supply

description

The TMX27PC256 series are 262,144-bit, one-time, electrically programmable read-only memories. These devices are fabricated using HVCMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three state for connecting multiple devices to a common bus. The TMX27PC256 is pin compatible with existing 28-pin ROMs and EPROMs. It is offered in a dual-in-line plastic package (N suffix) rated for operation from 0°C to 70°C.

Since these PROMs operate from a single 5-V supply (in the read mode), they are ideal for use in microprocessor-based systems. One other (12.5 V) supply is needed for programming, but all programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

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